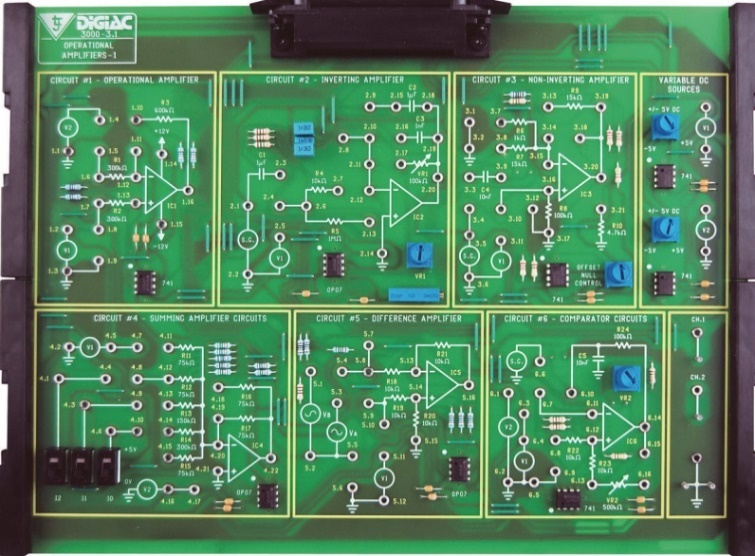
# Designing the Circuit

## Requirements

The task was to design and build an audio circuit which takes a sinusoidal input, with the following requirements:

|  |  |
| --- | --- |
| **Input** | **Output** |
| 100mVp-p | 2Vp-p |
| Symmetrical about 0V | Symmetrical about +2V |

It was assumed that the input frequency was 1kHz, though that did not affect the output. Another requisite was that the output signal needed to remain in phase with the input signal.

The circuit had to be implemented on the D3000, “*3.1 Operational Amplifiers-1*” board. This offered a certain challenge as there was a limited assortment of components to choose from. The circuit specifications imply a two-stage amplification using op-amps, as there is a sine wave input (from the signal generator (S.G. on the D3000 board)) which is amplified and added to a DC offset. The first stage would be a summing stage. The output of a summing amplifier results in an inversion so it needs the summing output needs to be inverted, hence the need of an inverting op-amp as the second stage of the circuit.

To figure out the components to use, the overall gain must first be calculated. As mentioned above, the input sinusoidal input is 100mVp-p and the output must be 2Vp-p. Eqs.1-3 show the overall gain for the circuit.

|  |  |
| --- | --- |
|  | (1) |
|  | (2) |
|  | (3) |

The other requirement was that the output offset must be of +2V. For simplicity and ease of design it is easier to apply the same voltage gain to both the sinusoidal input as well as the offset. Eqs.4-7 show the input offset voltage for this circuit.

|  |  |
| --- | --- |
|  | (4) |
|  | (5) |
|  | (6) |
|  | (7) |

## Multisim Implementation

Figure shows the initial design of the circuit. U1 being the summing stage and U2 being the inverting stage. The resistors are all found on the board, labelled respectively. Furthermore, V1 is the DC offset and VR1 is the 100k potentiometer, both located on the D3000 board. The overall gain in the circuit in figure was set so that the summing stage has a gain of 1 and the inverting stage has a gain of 20; arithmetic gains are multiplied together bringing the overall gain to 20, as per the calculation from the previous section. Eqs.8-10 show the derivation of the output for summing stage.

|  |  |
| --- | --- |
|  | (8) |
|  | (9) |
|  | (10) |
|  | (11) |
|  | (12) |
|  | (13) |

Eqs. 14-16 show the derivation for the inverting stage. in this case is the from the summing stage.

|  |  |
| --- | --- |
|  | (14) |
|  | (15) |
|  | (16) |

Eqs. 17-19 show the derivation of the overall output. S.G is the AC component while V1 is the DC component of the output sinusoid.

|  |  |
| --- | --- |
|  | (17) |
|  | (18) |
|  | (19) |

Substituting the initially required AC and calculated DC voltages, Eqs. 20-23 show that the resulting output voltages are per requirement.

|  |  |
| --- | --- |
|  | (20) |
|  | (21) |
|  | (22) |
|  | (23) |

Now that the initial design had been finished on Multisim, it was implemented onto the D3000 board.

## D3000 implementation

### Design

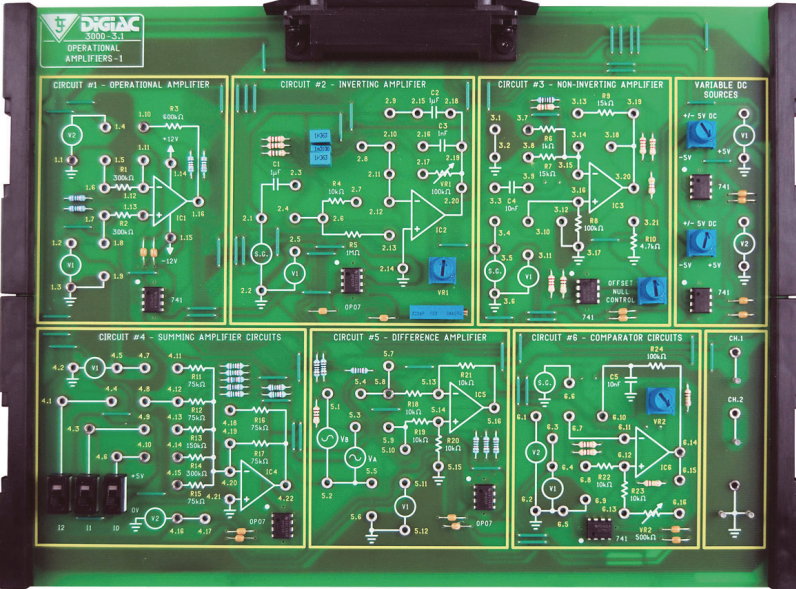


Figure shows the connections made on the board, following the circuit designed on Multisim. Before it was turned on, the signal generator was set to 100mVp-p sine wave with 0 DC offset, V1 on the top right of the board was set to 100mV and the resistance of VR1 was set to 20kΩ, both with the help of a DVM.

### Results

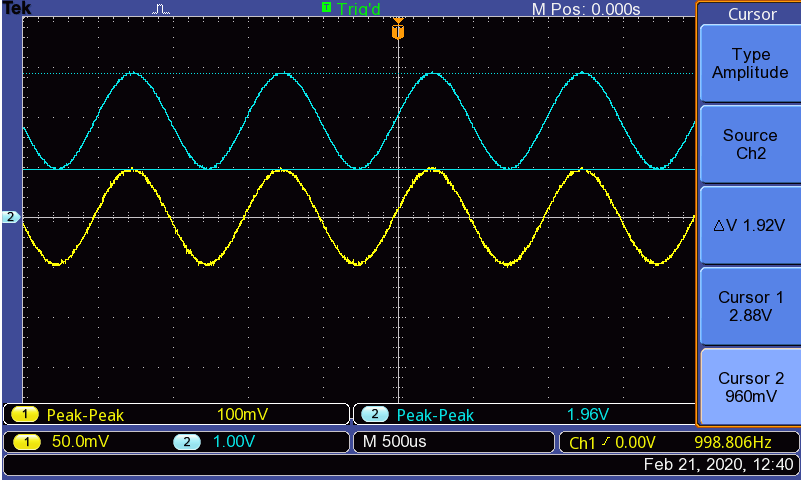


Figure shows the input sine wave (yellow) and the overall output (blue). With the help from the cursors of the digital oscilloscope, as well as the measure functions, it was shown that the output was approximately 2Vp-p, symmetrical about 2V; the output is two (1V) divisions above the axis. The reason why it was not exactly 2Vp-p,was very likely due to VR1 being hard to fine tune and not staying at exactly 20kΩ, making the gain slightly greater or lesser than 20.

While the output satisfied the requirements, the offset fluctuated unusually and was not stable, this was seen in the oscilloscope as the offset changing quite drastically. In order to fix this, a minor change was made to the original design, while maintaining the use of the components found on the D3000.

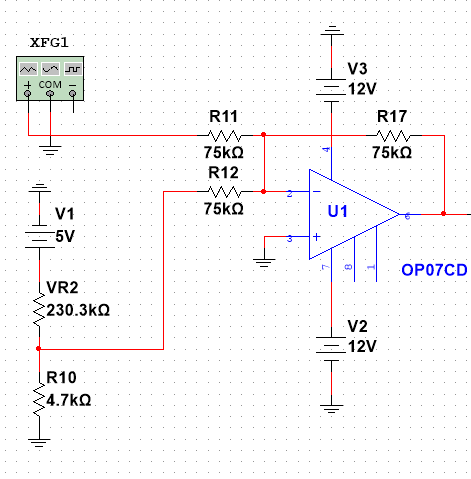


Figure shows the minor change to the summing stage by adding a potential divider instead of connecting V1 directly. It was decided that the input voltage of the divider would be 5V (the maximum voltage of the V1 source), and one of the resistors was going to be , which was directly connected to ground. Eqs. show the calculation for finding the second resistor value, which would result in an output of 100mV.

|  |  |
| --- | --- |
|  | (24) |
|  | (25) |
|  | (26) |
|  | (27) |
|  | (28) |
|  | (29) |

As shown in the modified design, this value was obtained by VR2, the 500kΩ potentiometer on the D3000 board.

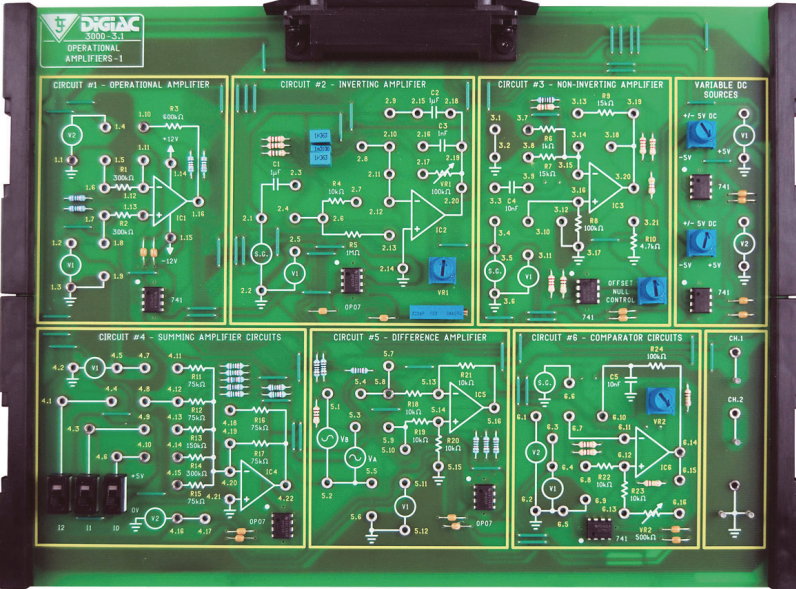


Figure shows the new board connections, before the power was turned on, the resistance of VR2 was set to 230.3kΩ and the voltage of V1 was set to 5V. The voltage was measured across the voltage divider to be 100mV, as expected. The oscilloscope showed the same output, except now the offset was stable and there was no noticeable drift.

b

# Measuring the slew rate

## Theory

## Methodology

In order to measure the slew rate, the first stage of the circuit was probed on the oscilloscope and the input signal was changed to a square wave.

The same process was carried out using the circuit built in Multisim. The first stage was probed and the slope

## Results & Analysis

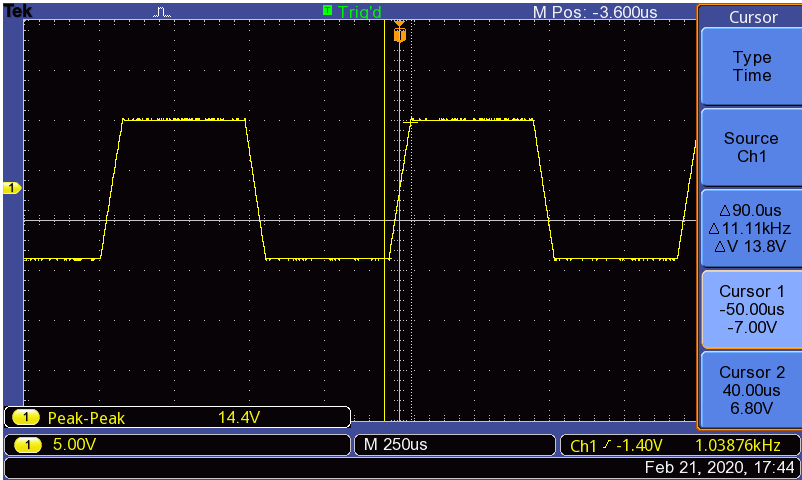


Figure shows the oscilloscope output for the summing stage, using a square wave. At the required voltage of 100mV, the square wave was not perfect, and it was not easy to measure the slew rate. However, after increasing the input amplitude to around 15Vp-p, the square wave was clearer, and the slew rate was easier to visualize and measure. From the figure, the cursors were positioned at either end of the slope, the ‘scope automatically measured the change in voltage and time; and respectively. As mentioned above, the slew rate is given in V/µs and is independent of the gain-defining resistors, Eqs.30-32 show the measured slew rate for the OP07.

|  |  |
| --- | --- |
|  | (30) |
|  | (31) |
|  | (32) |

According to the OP07 datasheet, the slew rate for the op-amp has a minimum value of 0.1 V/µs and a typical value of 0.3 V/µs. Eqs.33-35 show the geometric mean of the slew rate.

|  |  |
| --- | --- |
|  | (33) |
|  | (34) |
|  | (35) |

The measured slew rate is almost identical to the geometric mean calculated with the data provided from the OP07 datasheet.

# Measuring the bandwidth

## Theory

The 3dB point of the frequency response is also known as the cutoff frequency or where the gain is 70.7% <https://www.electronics-tutorials.ws/opamp/opamp_1.html>

## Methodology

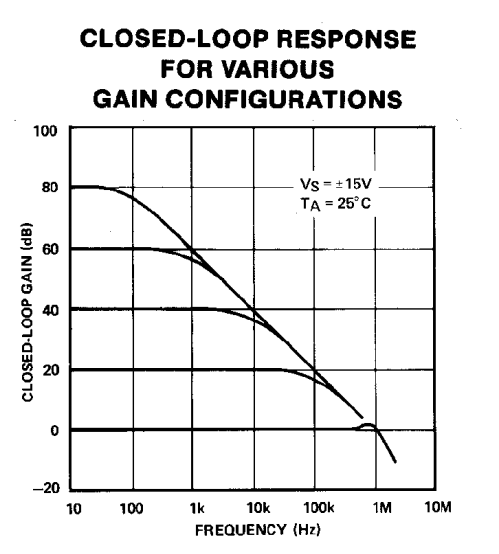
For this measurement, the 3dB point of the frequency response of a single stage of the circuit designed in the previous section, was measured. First, the OP07 datasheet was consulted for a frequency response of the closed-loop gain.

Figure shows a closed loop frequency response for various gains for the OP07 op-amp. Before the cutoff was measured using the circuit built on the D3000 board, a gain of 20dB was chosen (= to arithmetic gain of 10), shown in Eqs.36-40.

|  |  |
| --- | --- |
|  | (36) |
|  | (37) |
|  | (38) |
|  | (39) |
|  | (40) |

Since the summing stage has a gain of 1, the inverting stage was used to measure the cutoff frequency. Based on the calculations, the gain of the inverting stage was halved from 20, by changing the potentiometer “VR1” from 20kΩ to 10kΩ.

As in the previous sections, the input from the signal generator was a sine wave of 100mVp-p. Since the gain was 10, the output was 1Vp-p. The frequency was then increased until the output was around 707mVp-p. The frequency was then recorded and compared to the datasheet.

## Results & Analysis

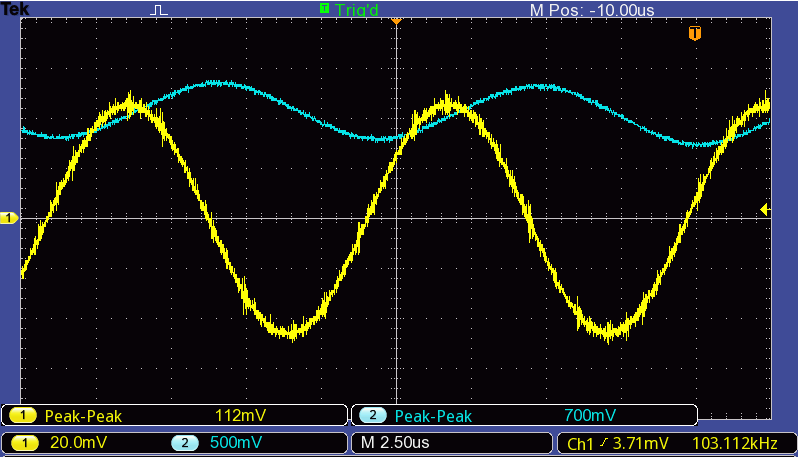


Figure shows the oscilloscope output at the cutoff frequency of the inverting stage of the circuit. The frequency was shown to be approximately 100kHz, according to the datasheet, this was the cutoff frequency of the OP07 at a closed loop gain of 20dB. There were a few sources of error when this measurement was taken: The input and output voltages were not exactly 100mVp-p and 700mVp-p. The resistances of the potentiometers were not exact, so the gain was not exactly 10. The datasheet assumed a Vs = but the in the D3000, Vs =.

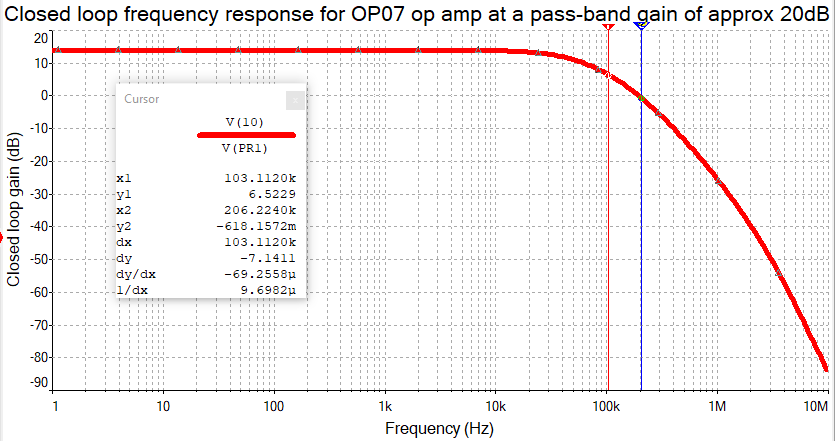
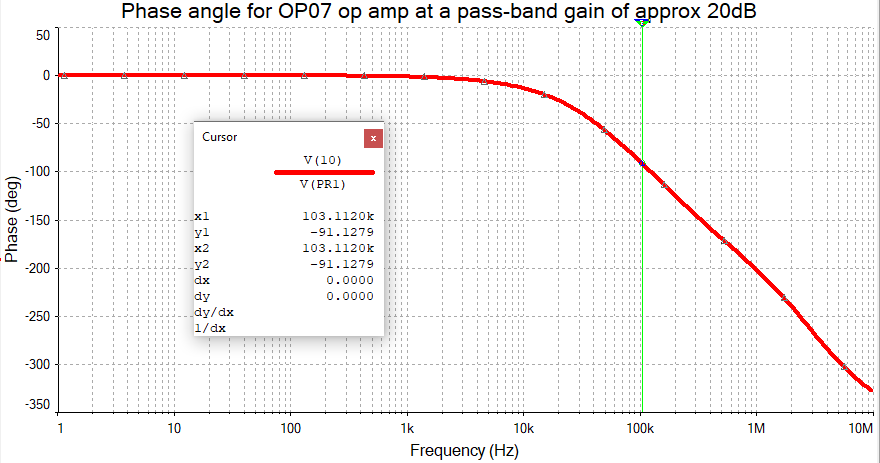


Figure shows the frequency response from the multisim simulation. The first cursor was placed at 103.112kHz, as in the measurement from the D3000 board. It was shown that it is a first order filter because the second cursor was placed an octave above (206.224kHz) and the slope was approximately -6dB/octave. As mentioned earlier, the phase shift at the cut off frequency is 90n where n is the type of order. This is true for the multisim simulation as it can be seen that the phase shift is almost 90 degrees (figure).

Include multisim for slew rate and all the theories