

HD74LS138

3-Line-to-8-Line Decoders / Demultiplexers

REJ03D0434-0300

Rev.3.00

Jul.13.2005

The HD74LS138 decodes one-of-eight line dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

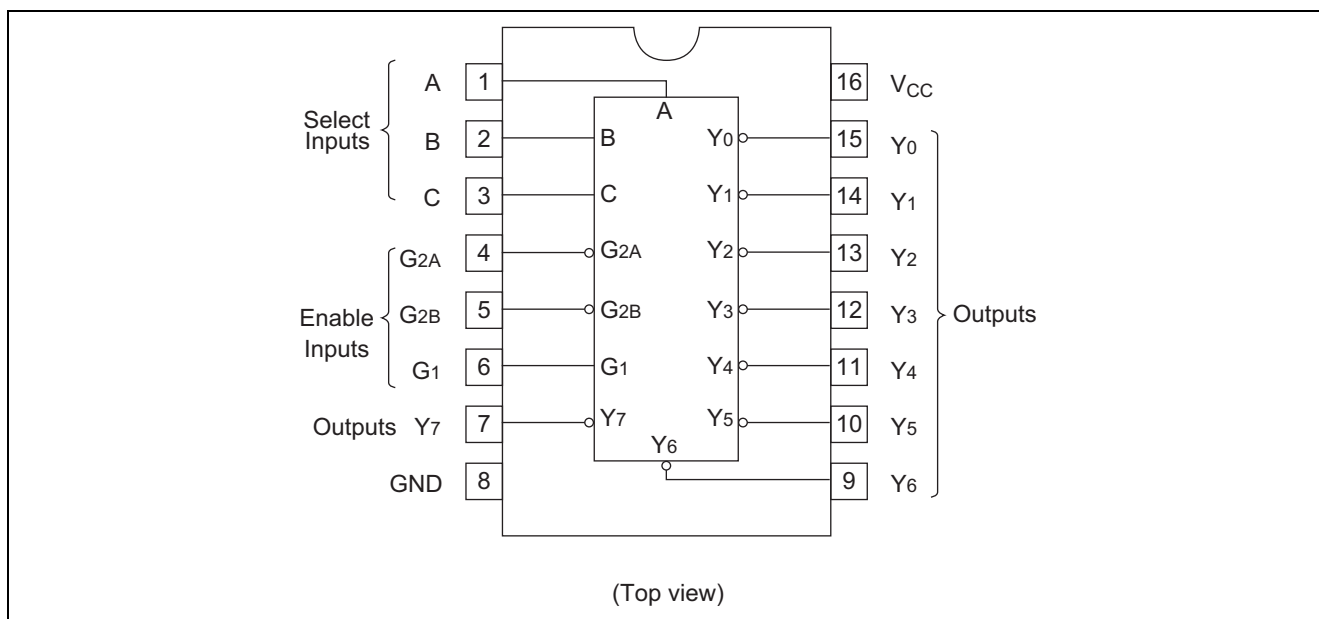
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS138P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	-
HD74LS138FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS138RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



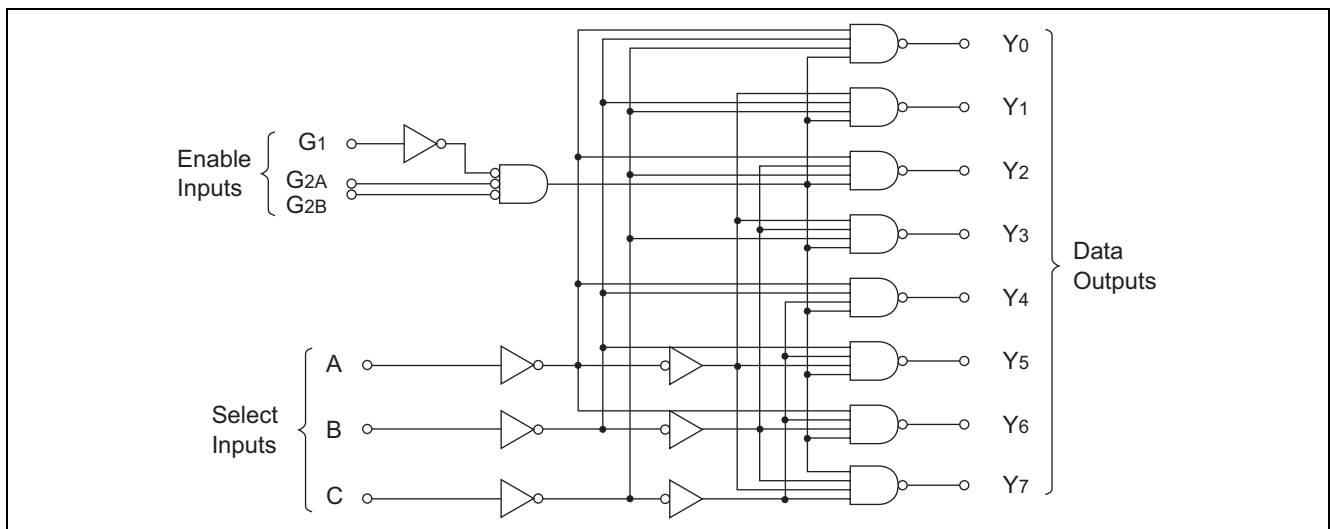
Function Table

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H ; high level, L ; low level, X ; irrelevant

* ; $G_2 = G_{2A} + G_{2B}$

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	-400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	-20	25	75	°C

Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V _{IH}	2.0	—	—	V	
	V _{IL}	—	—	0.8	V	
Output voltage	V _{OH}	2.7	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA
	V _{OL}	—	—	0.4	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V
		—	—	0.5		
	I _{OL}	—	—	—	—	I _{OL} = 4 mA
Input current	I _{IH}	—	—	20	μA	V _{CC} = 5.25 V, V _I = 2.7 V
	I _{IL}	—	—	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V
	I _I	—	—	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V
Short-circuit output current	I _{OS}	-20	—	-100	mA	V _{CC} = 5.25 V
Supply current	I _{CC}	—	6.3	10	mA	V _{CC} = 5.25 V, Outputs enabled and open
Input clamp voltage	V _{IK}	—	—	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA

Note: * V_{CC} = 5 V, Ta = 25°C

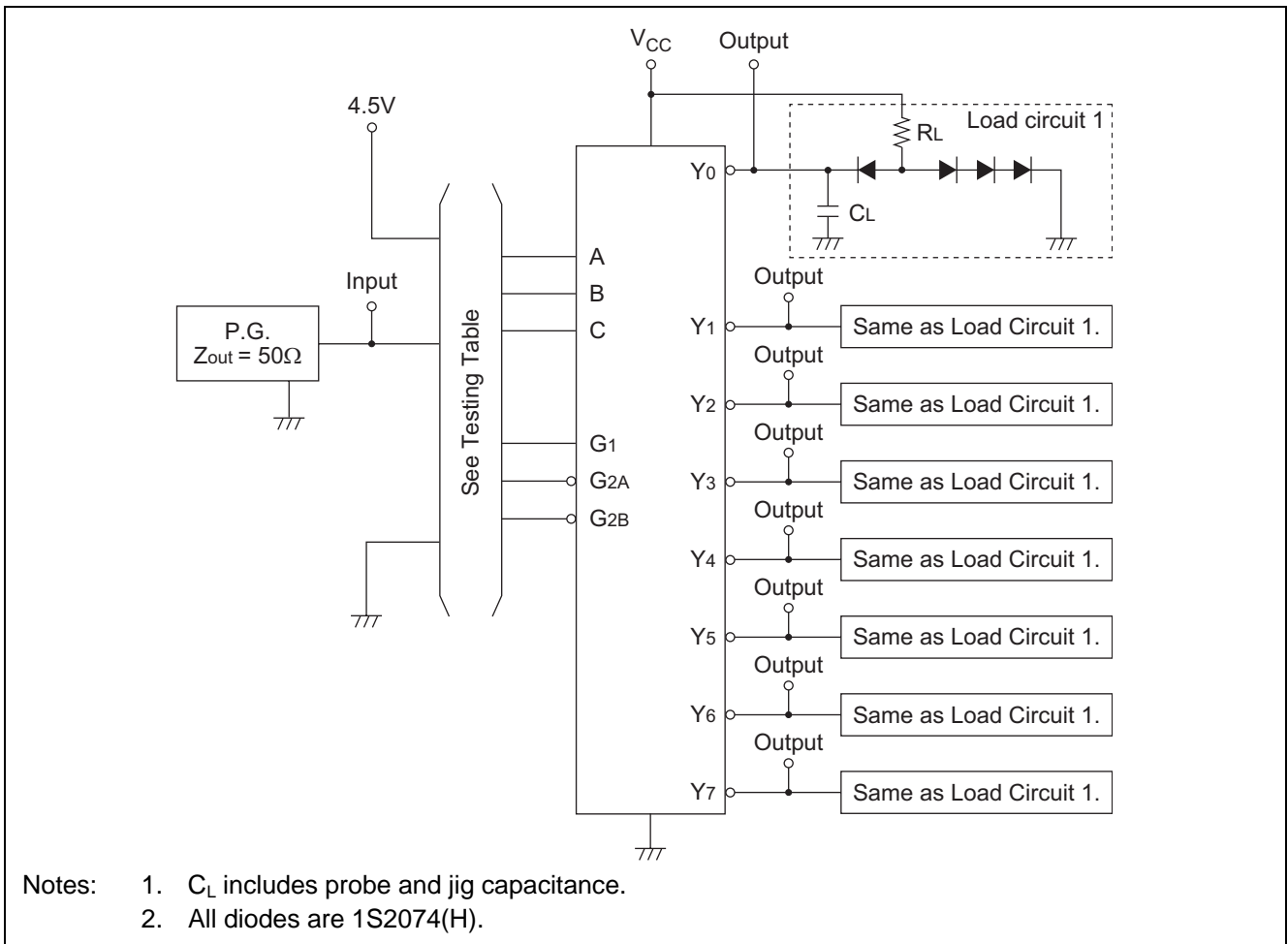
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

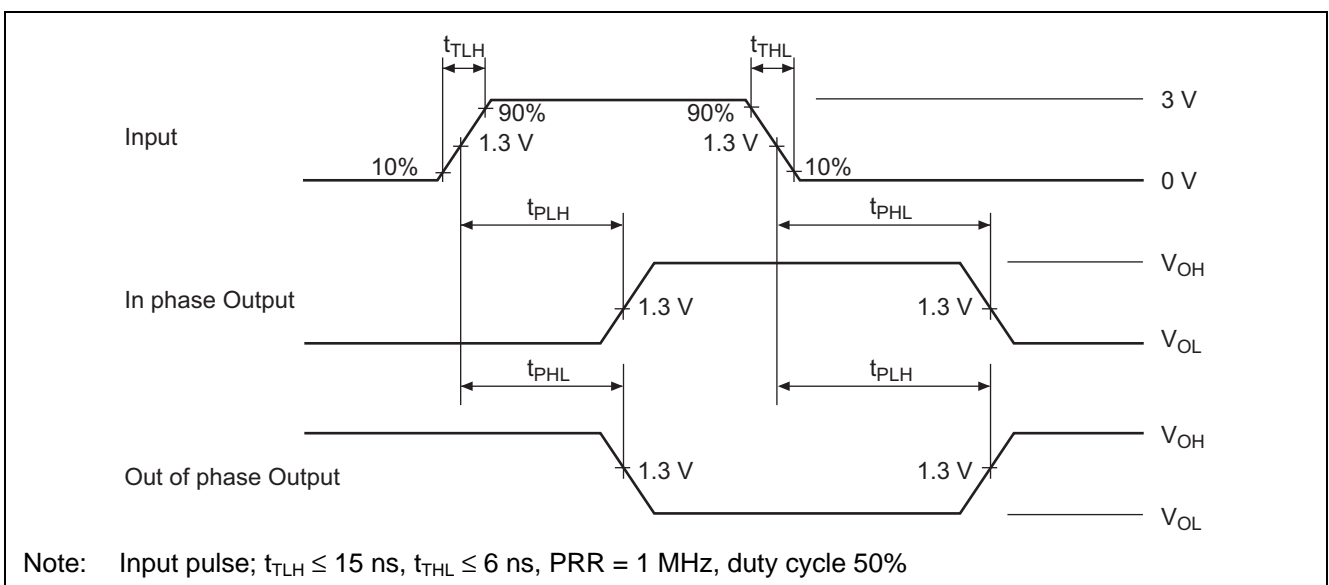
Item	Symbol	Inputs	Output	Levels of delay	min.	typ.	max.	Unit	Condition
Propagation delay time	t _{PLH}	Binary select A, B, C	Y	2	—	13	20	ns	C _L = 15 pF, R _L = 2 kΩ
	t _{PHL}				—	27	41	ns	
	t _{PLH}			3	—	18	27	ns	
	t _{PLH}				—	26	39	ns	
	t _{PLH}	Enable G _{2A} , G _{2B}	Y	2	—	12	18	ns	
	t _{PHL}				—	21	32	ns	
	t _{PLH}	Enable G ₁		3	—	17	26	ns	
	t _{PLH}				—	25	38	ns	

Testing Method

Test Circuit



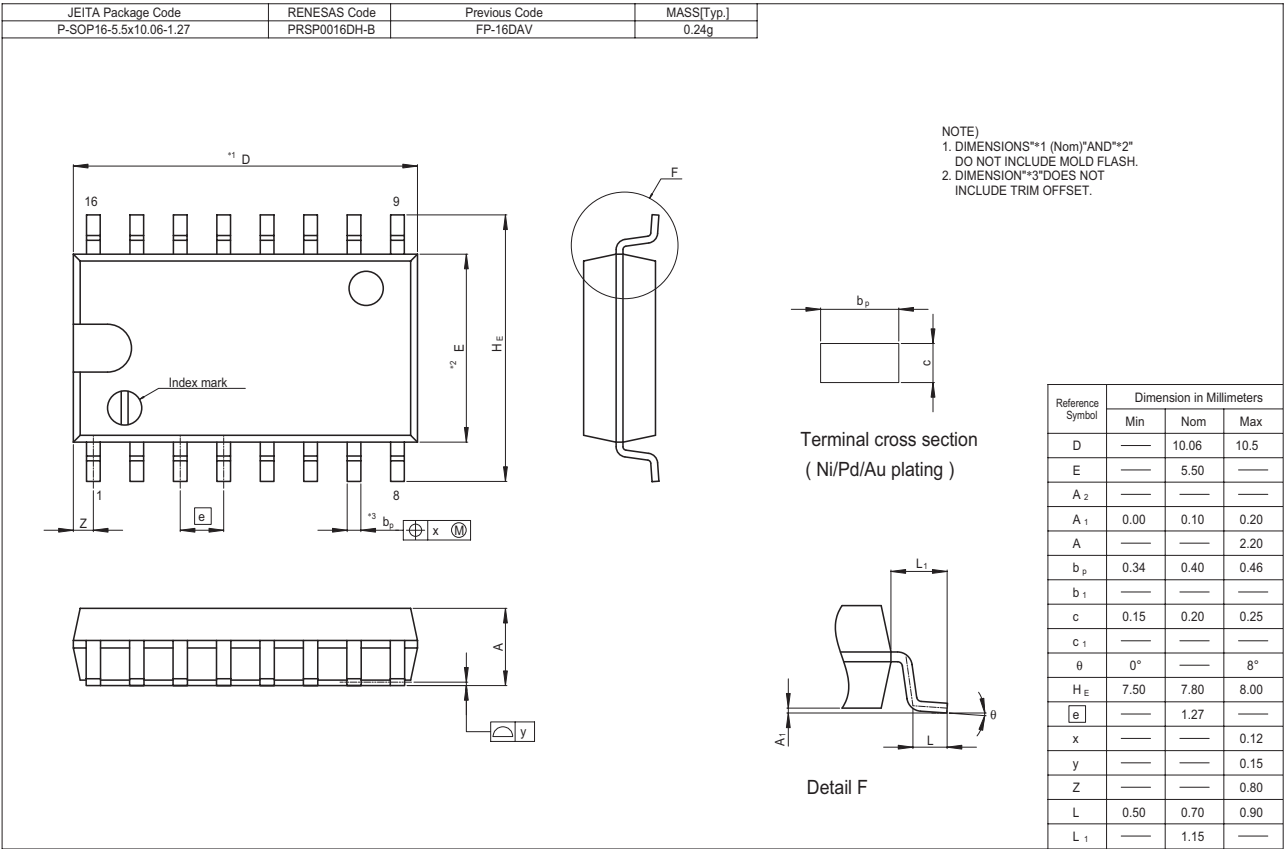
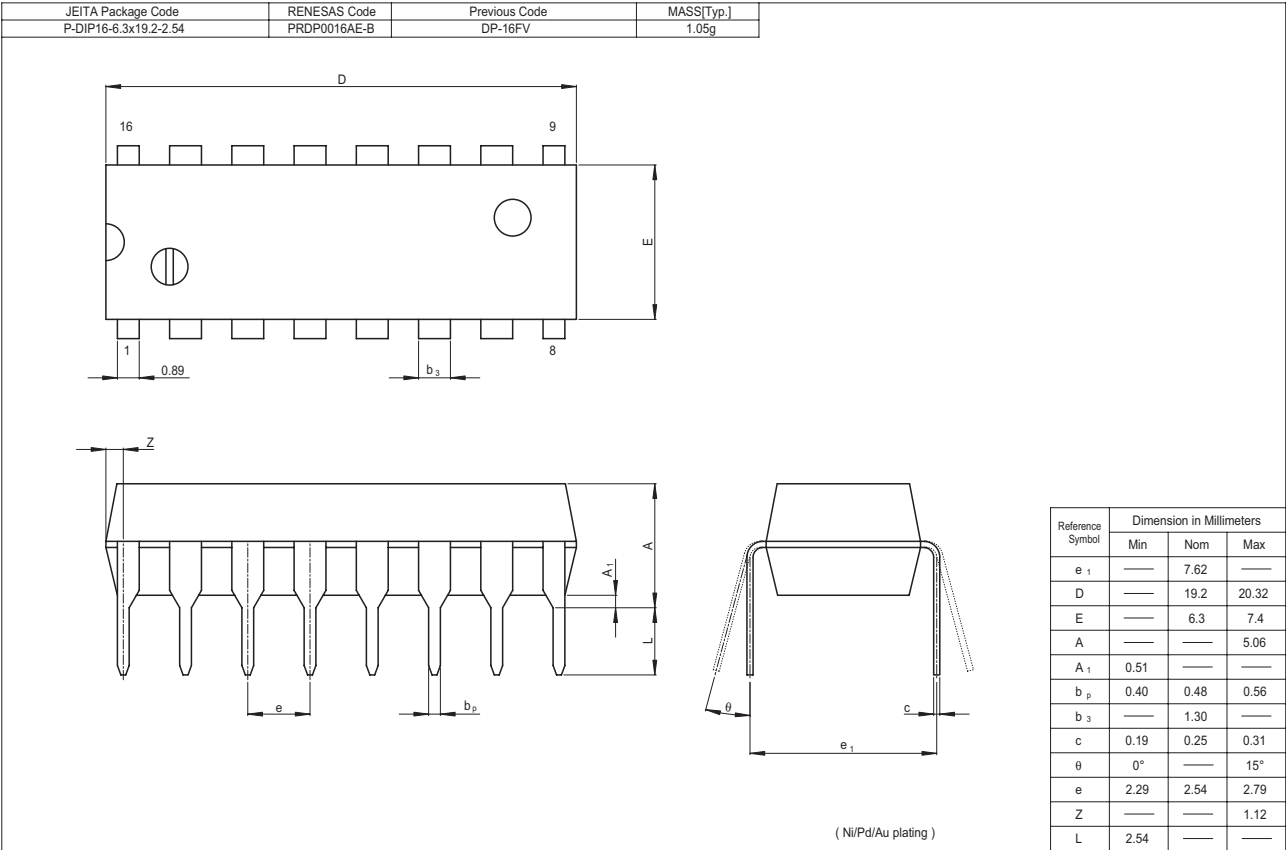
Waveform

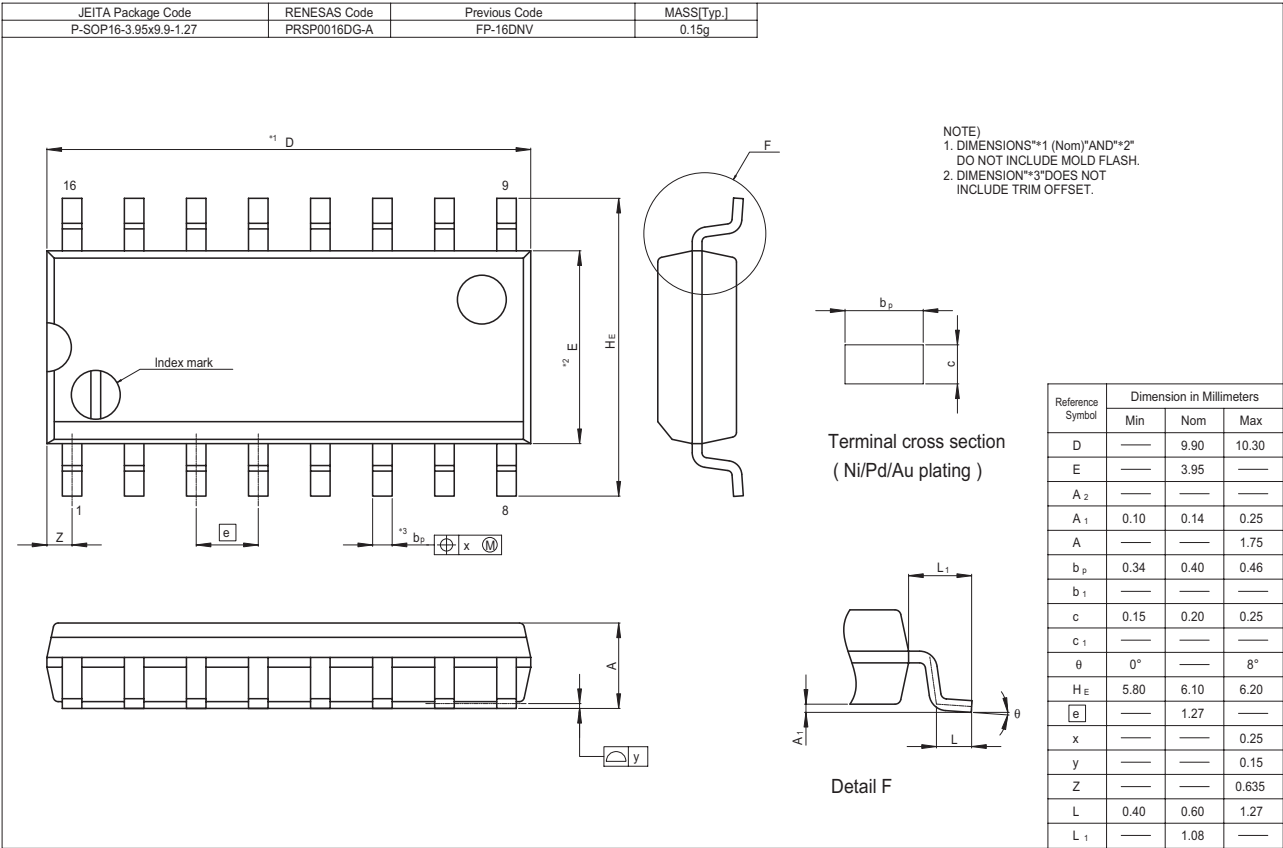


Relation Between Input and Output to Levels of Delay

Inputs	Outputs							
	2 levels of delay				3 levels of delay			
A	Y ₀	Y ₂	Y ₄	Y ₆	Y ₁	Y ₃	Y ₅	Y ₇
B	Y ₀	Y ₁	Y ₄	Y ₅	Y ₂	Y ₃	Y ₆	Y ₇
C	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
G ₁					Y ₀ to Y ₇			
G _{2A} , G _{2B}	Y ₀ to Y ₇							

Package Dimensions





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