HEF4093B

Quad 2-input NAND Schmitt trigger

Rev. 9 — 15 December 2015

Product data sheet

1. General description

The HEF4093B is a quad two-input NAND gate. Each input has a Schmitt trigger circuit. The gate switches at different points for positive-going and negative-going signals. The difference between the positive voltage (V_{T+}) and the negative voltage (V_{T-}) is defined as hysteresis voltage (V_H) .

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Schmitt trigger input discrimination
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

4. Ordering information

Table 1. Ordering information

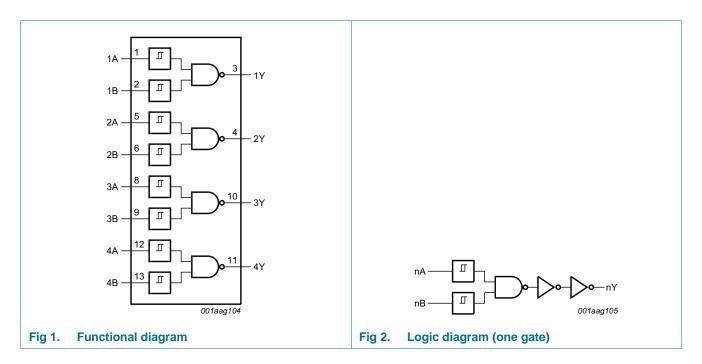
All types operate from -40 °C to +125 °C

Type number	Package						
	Name	Description	Version				
HEF4093BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1				



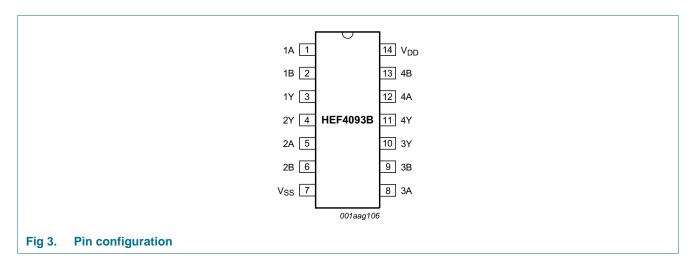
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5. Functional diagram



6. Pinning information

6.1 Pinning



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6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 5, 8, 12	input
1B to 4B	2, 6, 9, 13	input
1Y to 4Y	3, 4, 10, 11	output
V_{DD}	14	supply voltage
V _{SS}	7	ground (0 V)

7. Functional description

Table 3. Function table[1]

Input	Output	
nA	nB	
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

^[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0 \text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
VI	input voltage		-0.5	$V_{DD} + 0.5$	V
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$			
		SO14 <u>[1</u>	-	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

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9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
VI	input voltage		0	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	+125	°C

10. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	–40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} = -	+125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level	$ I_{O} < 1 \mu A$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level	$ I_{O} < 1 \mu A$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
	output current	V _O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I _{OL}	LOW-level	V _O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
	output current	V _O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V _O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
II	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{DD}	supply current	all valid input	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μΑ
		combinations;	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μΑ
		$I_O = 0 A$	15 V	-	1.0	-	1.0	-	30.0	-	30.0	μΑ
Cı	input capacitance			-	-	-	7.5	-	-	-	-	pF

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11. Dynamic characteristics

Table 7. Dynamic characteristics

 T_{amb} = 25 °C; C_L = 50 pF; t_r = $t_f \le$ 20 ns; wave forms see <u>Figure 4</u>; test circuit see <u>Figure 5</u>; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	nA or nB to nY	5 V	63 ns + (0.55 ns/pF)C _L	-	90	185	ns
	propagation delay		10 V	29 ns + (0.23 ns/pF)C _L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C _L	-	30	60	ns
t _{PLH}	LOW to HIGH	nA or nB to nY	5 V	58 ns + (0.55 ns/pF)C _L	-	85	170	ns
	propagation delay		10 V	29 ns + (0.23 ns/pF)C _L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C _L	-	30	60	ns
t _{THL}	HIGH to LOW output	nY to LOW	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
	transition time		10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{TLH}	LOW to HIGH output	nA or nB to	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
	transition time	HIGH	10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns

^[1] Typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

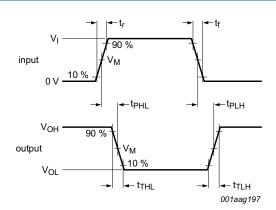
Table 8. Dynamic power dissipation

 $V_{SS} = 0 \ V; \ t_f = t_f \le 20 \ ns; \ T_{amb} = 25 \ ^{\circ}C.$

Symbol	Parameter	V_{DD}	Typical formula	where:
P_D	dynamic power	5 V	$P_D = 1300 \times f_i + \Sigma (f_0 \times C_L) \times V_{DD}^2 (\mu W)$	f_i = input frequency in MHz;
	dissipation	10 V	$P_D = 6400 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	f _o = output frequency in MHz;
		15 V	$P_D = 18700 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	C _L = output load capacitance in pF;
				$\Sigma(f_0 \times C_L) = \text{sum of the outputs};$
				V _{DD} = supply voltage in V.

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12. Waveforms



Measurement points are given in Table 9.

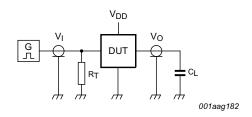
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

 t_r , t_f = input rise and fall times.

Fig 4. Propagation delay and output transition time

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V _M	V _M
5 V to 15 V	0.5V _{DD}	0.5V _{DD}



Test data given in Table 10.

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

 R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

Fig 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load	
V_{DD}	VI	t _r , t _f	CL
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

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13. Transfer characteristics

Table 11. Transfer characteristics

 $V_{SS} = 0 \text{ V; } T_{amb} = 25 \text{ °C; see } \underline{Figure 6} \text{ and } \underline{Figure 7}.$

Symbol	Parameter	Conditions	V_{DD}	Min	Тур	Max	Unit
V_{T+}	positive-going threshold voltage		5 V	1.9	2.9	3.5	V
			10 V	3.6	5.2	7	V
			15 V	4.7	7.3	11	V
V_{T-}	negative-going threshold voltage		5 V	1.5	2.2	3.1	V
			10 V	3	4.2	6.4	V
			15 V	4	6.0	10.3	V
V _H	hysteresis voltage		5 V	0.4	0.7	-	V
			10 V	0.6	1.0	-	V
			15 V	0.7	1.3	-	V

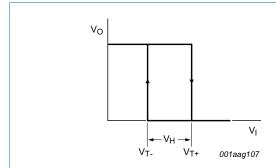


Fig 6. Transfer characteristic

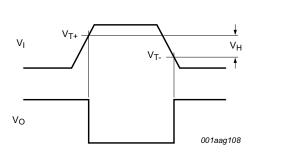
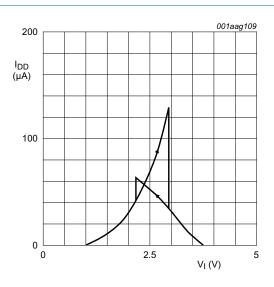
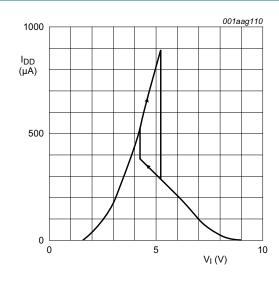


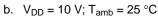
Fig 7. Waveforms showing definition of V_{T+} and V_{T-} (between limits at 30 % and 70 %) and V_{H}

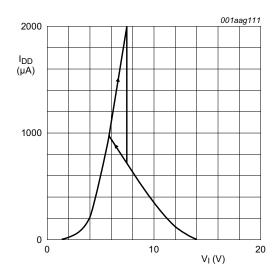
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a. $V_{DD} = 5 \text{ V}$; $T_{amb} = 25 \,^{\circ}\text{C}$

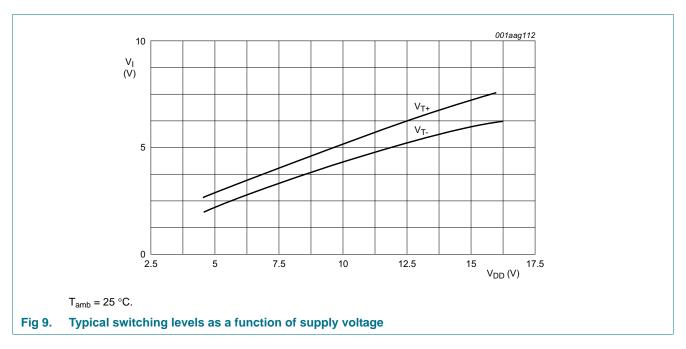




c. $V_{DD} = 15 \text{ V}$; $T_{amb} = 25 \,^{\circ}\text{C}$

Fig 8. Typical drain current as a function of input

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14. Application information

Some examples of applications for the HEF4093B are:

- · Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

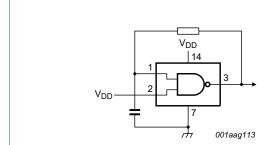


Fig 10. Astable multivibrator

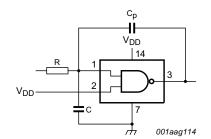


Fig 11. Schmitt trigger driven via a high-impedance input

If a Schmitt trigger is driven via a high-impedance (R > 1 k Ω), then it is necessary to incorporate a capacitor C with a value of $\frac{C}{C_P} > \frac{V_{DD} - V_{SS}}{V_H}$; otherwise oscillation can occur on the edges of a pulse.

 C_{p} is the external parasitic capacitance between inputs and output; the value depends on the circuit board layout.

Remark: The two inputs may be connected together, but this will result in a larger through-current at the moment of switching.

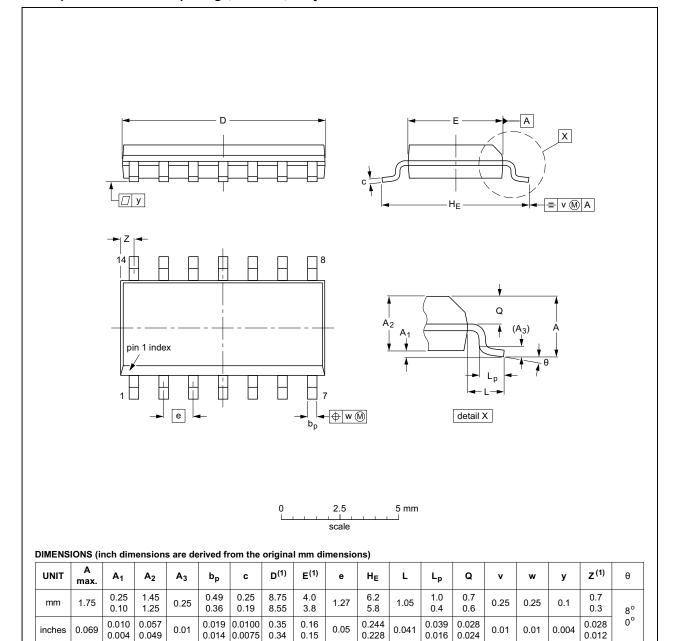
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15. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

Fig 12. Package outline SOT108-1 (SO14)

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16. Abbreviations

Table 12. Abbreviations

Acronym	Description
DUT	Device Under Test

17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4093B v.9	20151215	Product data sheet	-	HEF4093B v.8
Modifications:	Type number	r HEF4093BP (SOT27-1) remo	ved.	
HEF4093B v.8	20111121	Product data sheet	-	HEF4093B v.7
Modifications:	Table 6: I _{OH} minimum values changed to maximum			
HEF4093B v.7	20100901	Product data sheet	-	HEF4093B v.6
HEF4093B v.6	20091202	Product data sheet	-	HEF4093B v.5
HEF4093B v.5	20090728	Product data sheet	-	HEF4093B v.4
HEF4093B v.4	20080612	Product data sheet	-	HEF4093B_CNV v.3
HEF4093B_CNV v.3	19950101	Product specification	-	HEF4093B_CNV v.2
HEF4093B_CNV v.2	19950101	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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