廣東工業大學

本科毕业设计（论文）

外文参考文献译文及原文

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专　　业　自动化

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2016　年　5　月

目录

摘要

升压变换器被广泛用于功率因素预调节器。在大功率应用中，常将两个或多个升压变换器交错连接以此提高输出功率同时降低输出波纹。其中一个关键的设计标准是确保变换器之间电流均衡。本文提出一个由两个互相耦合并交错连接的升压变换器构成的变换器组，该变换器组即使在较大的占空比不匹配情况下仍有出色的电流均衡特性。另外，该变换器组能设计成具有更小的输入电流波纹和零开关损耗。本文会说明其工作原理，分析电路的稳态特性，同时将该电路与常规电路进行比较。文章最后还会给出电路的仿真和实验结果。

关键词：耦合电感、电流均衡、交错并联升压变换器。

1、 简介

随着电力质量要求的大幅提高，离线电力要求从直流母线获取大功率因素和包含小谐波系数的电流。输入侧使用 LC 电路滤波以减少谐波的传统方法在很多大功率应用场景不满足使用要求。因此提出了使用降压、升压、升降压、cuk、sepic 变换器提高功率因数。在这些变换器中单相升压变换器作为前置功率因数调节器被广泛使用。其原因归纳为升压变换器结构和系统简单、小电压波纹和相比其他拓扑结构更高的转换效率。再者，阶跃变换使其适用于广泛的输入电压应用。

工作在连续电感电流模式的 PFC 升压变换器有更高的电力利用效率、更低的传输损失和更小的输入电流波纹。在另一方面，工作在非

连续电感电流模式的升压变换器有更低的升压整流反向恢复损失和更低的晶体管开关损失。为了减少输入电流波纹，文献[3]-[5]提出了改进的升压变换器拓结构。

在大功率应用中，升压变换器往往是采用交错并联的方法提高输出电流以及减少输入电流波纹。然而，电流在平行支路中的均衡问题是设计难点。可以证明，当

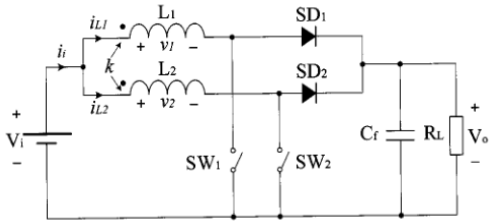


图 1 由两个交错连接内耦合升压变换器单元组成的变换器

两路相似但独立控制的升压变换电路平行连接（具有同样的输入输出电压），大占空比支路可能工作在 CICM 模式，而另一个会自动工作在 DICM 模式。在这个条件下，任何额外的流入电流会被工作在 CICM 模式下的变换器所占据。因此，电流均衡在空比不匹配时十分敏感。电流均衡电路的设计在文献[1],[6],[7]有所讨论。文献[8]中提出一个在一对还有耦合电感的升压变换器中使用电流滞后控制的方法。

本文提出并研究一个变换器组，它由两个交错连接并内耦合的升压变换器构成。这个变换器的电路设计简单，而且具有出色的电流均衡特性、小输入电流波纹、零升压整流反向恢复损失等优点。文中讨论了该变换器的工作原理和稳态分析并且与传统的升压变换器进行了对比。文中的概念由仿真和实验进行说明验证。

2、 工作原理

图 1 展示了我们提出的变换器的结构，它由两个交错连接并内耦合的变换器单元组成。电感 L1 和 L2 近距离耦合，两者具有同样的绕线方向。耦合电感可由图 2 中三个非耦合电感等效电路代替。电感之间具有以下关系。

$$L_1^{'} = L_1 - L_m \qquad (1)$$

$$L_2^{'} = L_2 - L_m \qquad (2)$$

$$L_m = k\sqrt{L_1 L_2} \qquad (3)$$

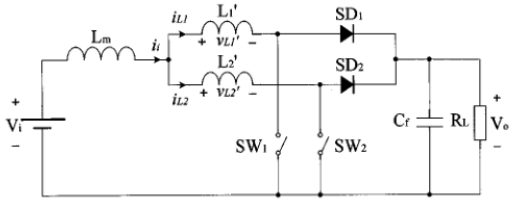


图 2 变换器等效电路

其中

L_1, L_2 两个电感的电感值

k 耦合系数

$L_1^{'}, L_2^{'}$ 等效电路里的漏磁电感值

L_m 互感

参照图 3 的不同开关状态等效电路以及图 4 的波形，变换器的工作过程说明如下：

1）状态 1[图 3-1]：

在时刻 t_0，SW_1 关闭。电感 $L_1^{'}$ 的电流开始上升而 $L_2^{'}$ 电流继续放电（$L_2^{'}$ 在

最后一个开关周期获得电流。）i_{L2} 充电速度比近似为：

$$\frac{di_{L2}}{dt}=\frac{-V_o}{L_1^{'}+L_2^{'}} \qquad (4)$$

2）状态 2[图 3-2]：

在 t_1 时刻，i_{L1} 降低为 0，i_{L1} 继续上升，i_{L1} 充电比速度比为：

$$\frac{di_{L1}}{dt}=\frac{V_i}{L_1} \qquad (5)$$

其中 $L_1=L_1^{'}+L_m$

3）状态 3[图 3-3]：

在 t_2 时刻，SW1 打开。存储在电感 L1 中的电能通过升压整流器 SD1 传送给负载。i_{L1} 充电比率为

$$\frac{di_{L1}}{dt}=\frac{-(V_o-V_i)}{L_1} \qquad (6)$$

4）状态 4[图 3-4]：

时刻 t3，开关 SW2 关闭，L2’电流开始上升，L1’继续放电，i_{L1} 充电比率为

$$\frac{di_{L1}}{dt}=\frac{-V_o}{L_1^{'}+L_2^{'}} \qquad (7)$$

5）状态 5[图 3-5]：

在时刻 t_4，电感电流 i_{L2} 上升速度诶

$$\frac{di_{L2}}{dt}=\frac{V_i}{L_2} \qquad (8)$$

其中 $L_2=L_2^{'}+L_m$

6）状态 7[图 3-6]：

在时刻 t_5，SW2 打开，L2’通过输出电路放电，i_{L2} 充电速度为

$$\frac{di_{L2}}{dt}=\frac{-(V_o-V_i)}{L_2} \qquad (9)$$

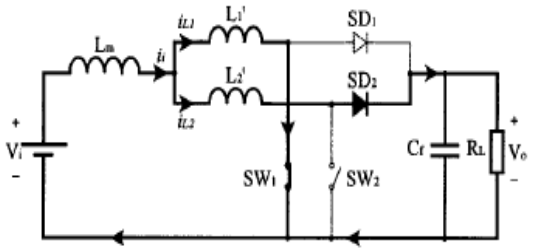
时刻 t0，SW1 打开，开关周期重复。

由图 4 的波形可看出如下规律：

1) 观察输入电流i_i ，变换器工作在 CICM 模式（由于i_i是连续的）。因此电感/开关的峰值电压和输入电流波形可以维持在相当低的水平。

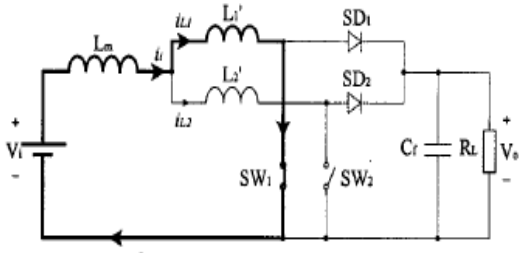
2) 然而，观察分立的升压变换器单元，由于 IL 和 i12 是不连续的，这些升压变换器单元实际上工作在 DICM 模式。这有助于解决电流不均衡问题。另外由于升压二极管 SD1、SD2 在 SW1、SW2 开通前关闭，二极管的反向截止损失可以消除。

如图 4 所示，假设 SW2 占空比（标为 D2）远大于 SW1 占空比（记为 D1）。然而这个结果在两个电感均流时变化不大（L1、L2 如图 1 所示）。这是因为i_i在半个开关周期流过 L1，另一半开关周期流过 L2。如果 使保持恒定， 和 会近似相等。



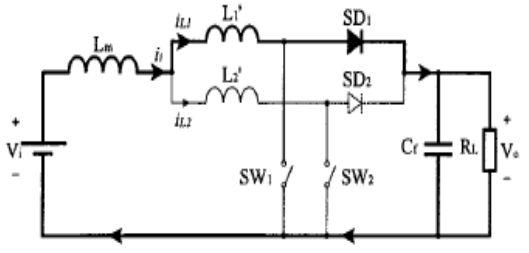
Time t_0–t_1

(a)



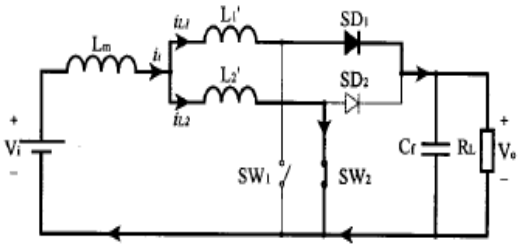
Time t_1–t_2

(b)



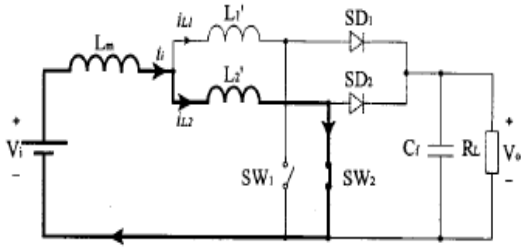
Time t_2–t_3

(c)



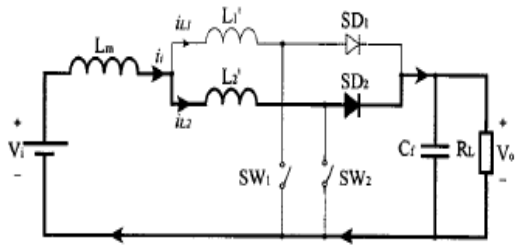
Time t_3–t_4

(d)



Time t_4–t_5

(e)



Time t_5–t_6

(f)

3、 稳态分析

假设图 4 所示的电流波形达到稳定，从图 4 中i_{L1}波形可以发现：

$$\begin{aligned}&\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T+\frac{V_i}{L_1}(D_1-D_{11})T\\&=\frac{V_o-V_i}{L_1}(0.5-D_1)T+\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T\end{aligned}\qquad(10)$$

从图 4 中i_{L2}波形可以发现：

$$\begin{aligned}&\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T+\frac{V_i}{L_2}(D_2-D_{21})T\\&=\frac{V_o-V_i}{L_2}(0.5-D_2)T+\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T\end{aligned}\qquad(11)$$

由 4 可以看出，i_{L2}和i_{L1}平均值（记为I_1,I_2 ）可分别为：

$$I_1=\frac{1}{T}\left\{\begin{aligned}&\frac{1}{2}D_{11}T\,\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T\\&+\frac{1}{2}(D_1-D_{11})T*[\frac{2V_o}{L_1^{'}+L_2^{'}}D_{11}T\\&+\frac{V_i}{L_1}(D_1-D_{11})T]\\&+\frac{1}{2}(0.5-D_1)T\\&*[\frac{V_o}{L_1^{'}+L_2^{'}}(D_{11}+D_{21})T\\&+\frac{V_i}{L_1}*(D_1-D_{11})]T\\&+\frac{1}{2}D_{21}T\,\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T\end{aligned}\right\}\qquad(12)$$

$$I_2=\frac{1}{T}\left\{\begin{array}{l}\frac{1}{2}D_{21}T\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T+\frac{1}{2}(D_2-D_{21})T\\ *[\frac{2V_o}{L_1^{'}+L_2^{'}}D_{21}T\\ +\frac{V_i}{L_2}(D_2-D_{21})T]\\ +\frac{1}{2}(0.5-D_2)T\\ *[\frac{V_o}{L_1^{'}+L_2^{'}}(D_{11}+D_{21})T\\ +\frac{V_i}{L_2}*(D_2-D_{21})]T\\ +\frac{1}{2}D_{11}T\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T\end{array}\right\} \quad (13)$$

假设变换器是理想的没有能量损失，输入功率 P_i 等于输出功率 P_o

$$P_i=P_o$$

$$V_i(I_1+I_2)=\frac{V_o^2}{R_L} \quad (14)$$

其中 R_L 负载电阻。

联合（10）-（14）可以推出 Vo。为简化计算，假设

$$D_1=D, D_2=D+\delta D, L_1=L_2=L,$$
$$L_1^{'}=L_2^{'}=(1-k)L$$

经计算可推出输出电压 Vo 表达式(式 15)，详细推导见附录 A21。

值得注意的是式 15 只有在 Vo 是实数才有成立（没有虚部）。文章后面式 16 说明其物理意义。

当 R_L 比式 16 给定值小，输出电压会趋向于等于下面的值

$$V_o=\frac{V_i}{1-(2D+\delta D)}$$

或 $$V_o=\frac{V_i}{1-(D_1+D_2)}$$

这个值等于工作在 CICM 模式下占空比为 D1+D2 的传统升压变换器的输出电压。

在附录中可以看到 I_1 与 I_2 之间的区别由下面式子给出：

$$I_1 - I_2 \cong \frac{T\delta D}{4L}[V_o(2\mathrm{D}+\delta\mathrm{D}) - V_i] \quad (18)$$

在式 18，如果 $\delta D \ll 2D$ ，有：

$$I_1 - I_2 \cong \frac{T\delta D}{4L}[2\mathrm{D}V_o - V_i] \quad (19)$$

值得注意的是：

1) I_1 和 I_2 之差正比于&D，而且这个差值可以通过增加电感值 L 来减小。

2) 当 D = 0.25 时，有：

$$V_o = 2V_i \quad (20)$$

$$I_1 - I_2 = 0 \quad (21)$$

因此，对电流均衡来说，D= 0.25 是（每个开关二极管）最好的工作点。

4、 与传统升压变换器比较和设计考虑

在本章中，先对比传统升压变换器和文章提出的变换器的特性。然后简单讨论文中变换器的设计特点。

1) 与传统升压变换器比较

表 1 列出了传统升压变换器和文中提出的变换器的区别。

2) 电磁设计

对于文中提出的变换器，如果两个耦合电感更紧密耦合，即 L1’和 L2’相对 Lm 来说更小，那么电流波形会变得更规整。然而如果 L1’和 L2’太小，SD1 和 SD2 趋向于同时导通，对应状态 c 和 f。文中提出的变换器性能和带有并联开关的单一升压变换一样。为防止这种情况，我们需要保证（Vo-Vi）L1’/L1 或者（Vo-Vi）L2’/L1 大于 1V，因此导通的电感有足够大的反电动势使二极管截止。实际的耦合系数 k 可以在 0.9-0.98 范围内选择。在实际的耦合电感结构中，可以物理上分离两个线圈或者两者之间尽可能留有空隙使漏磁通较大以此获得较小的 k 值。

3）反馈设计

在反馈控制电路设计中，文中提出的变换器被视为占空比为 2D 的单一升压变换器，然后设计步骤和传统的升压变换器一致。

5、 仿真结果

在新变换器的 PSpice 仿真模中使用了理想的开关和二极管。仿真波形如图 5、图 6 所示。

仿真条件总结如下：

$R_L = 50\Omega, C_f = 4.7\mu F, L_1 = L_2 = 120\mu H,$
$k = 0.91, V_i = 30\text{V}, f = 50kHz$

在图 5 中 $D_1 = D_2 = 0.25$ ，在图 6 中 $D_1 = 0.25, D_2 = 0.35$

仿真结果如下：

图 5 中，i_{L1}(peak)=i_{L2}(peak)=2.687A，I_1 =I_2 =1.05A，V_o=55.70V，在图 6 中，i_{L1}(peak)=3.76A, i_{L2}(peak)=3.81A，I_1 = 1.52A，I_2 = 1.54A，V_o = 67.30A

值得注意的是：即使有 40%的中不可比不匹配（D1 = 0.25，D2=0.035)，平均电感电流之差只有 1.3%（分别为 1.52 和 1.54A）

6、 实验结果

如图 1 所示的实验原型电路被搭建起来，原件的参数和上一节图 7 的仿真电路一致，实验测量了占空比 D1 = D2 =0.35 的电感电流波形。两个电感电流波形实际上是一样的。图 8 占空比 D1 = 0.25 和 D2=0.35 的电感电流波形。这些电感的平均电流之分别为 1.46A 和 1.50A。他们之间只有 3%的差别。基于式 14、15、18 的计算差别也只有与 3%。

7、 结论

一种补偿并联升压变换器电流不均衡问题的方法在文中提出。即一种由两个耦合且交错并联的升压变换器单元组成变换器。该新提出的变换器有如下优点：

- 电路即使存在较大的占空比不匹配，耦合单元只有很小的电流不均衡。
- 该变换器可以设计出小输入波纹和零升压整流二极管反向恢复损失。
- 不需要电流传感器
- 两个变换器共用一个铁芯，价格便宜

变换器的稳态分析证明了其出色的电流均衡特性。仿真和实验结果同样验证了其出色的表现。

附录 耦合交错并联升压变换器直流分析

从图 4 中i_{L1}的稳态电流波形可以看出：

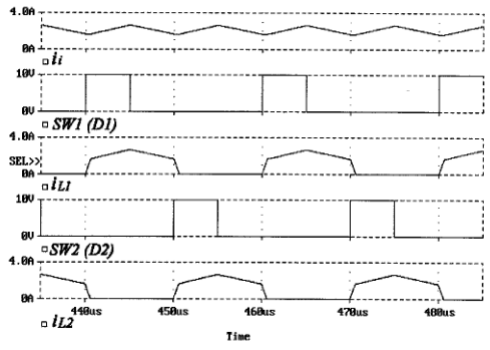


图 5 仿真电流波形

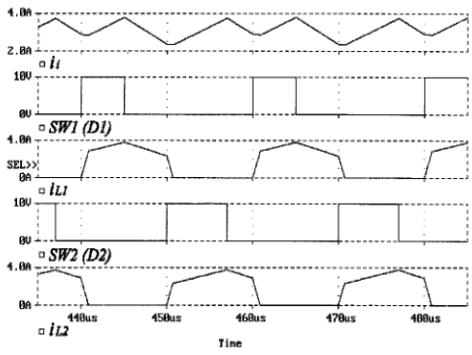


图 6 占空比不匹配电流波形

$$\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T+\frac{V_i}{L_1}(D_1-D_{11})T$$
$$=\frac{V_o-V_i}{L_1}(0.5-D_1)T+\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T$$

（A1）

从图 4 中i_{L1}波形可看出：

$$\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T+\frac{V_i}{L_2}(D_2-D_{21})T$$
$$=\frac{V_o-V_i}{L_2}(0.5-D_2)T+\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T$$

（A2）

由（A1)、(A2）有，D_1、D_2可整理成（A3)、(A4)。由图 4，i_{L1}、i_{L2}的平均值 I_1、I_2可分别表示成：

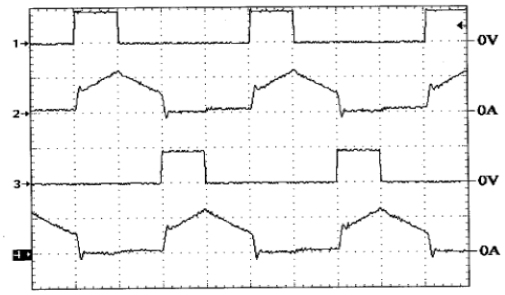


图 7

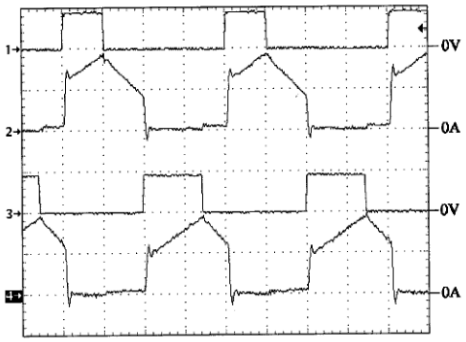


图 8

$$I_1=\frac{1}{T}\left\{\begin{array}{l}\frac{1}{2}D_{11}T\,\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T\\+\frac{1}{2}(D_1-D_{11})T*[\frac{2V_o}{L_1^{'}+L_2^{'}}D_{11}T\\+\frac{V_i}{L_1}(D_1-D_{11})T]\\+\frac{1}{2}(0.5-D_1)T\\*[\frac{V_o}{L_1^{'}+L_2^{'}}(D_{11}+D_{21})T\\+\frac{V_i}{L_1}*(D_1-D_{11})]T\\+\frac{1}{2}D_{21}T\,\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T\end{array}\right\}$$

（A5）

$$I_2=\frac{1}{T}\left\{\begin{array}{l}\frac{1}{2}D_{21}T\frac{V_o}{L_1^{'}+L_2^{'}}D_{21}T+\frac{1}{2}(D_2-D_{21})T\\ *[\frac{2V_o}{L_1^{'}+L_2^{'}}D_{21}T\\ +\frac{V_i}{L_2}(D_2-D_{21})T]\\ +\frac{1}{2}(0.5-D_2)T\\ *[\frac{V_o}{L_1^{'}+L_2^{'}}(D_{11}+D_{21})T\\ +\frac{V_i}{L_2}*(D_2-D_{21})]T\\ +\frac{1}{2}D_{11}T\frac{V_o}{L_1^{'}+L_2^{'}}D_{11}T\end{array}\right\} \quad (A6)$$

联立（A5)、(A6）得：

$$I_1=\frac{T}{2}\{\frac{V_o}{L_1^{'}+L_2^{'}}[D_{11}(0.5+D_1-D_{11})+D_{21}*(0.5-D_1+D_{21})]+\frac{V_i}{L_1}[(0.5-D_{11})(D_1-D_{11})]\} \quad (A7)$$

$$I_2=\frac{T}{2}\{\frac{V_o}{L_1^{'}+L_2^{'}}[D_{21}(0.5+D_2-D_{21})+D_{11}*(0.5-D_2+D_{11})]+\frac{V_i}{L_1}[(0.5-D_{21})(D_2-D_{21})]\} \quad (A8)$$

假设变换器是理想的，输入功率 P_i 与输出功率 P_o 相等，则有：

$$P_i=P_o \quad (A9)$$

$$V_i(I_1+I_2)=\frac{V_o^2}{R_L} \quad (A10)$$

$$I_i=I_1+I_2 \quad (A11)$$

$$V_i(I_1+I_2)=\frac{V_o^2}{R_L} \quad (A12)$$

其中：

I_i　　输入电流平均值

I_1　　L 电流平均值

I_2　　L 电流平均值

I_o　　负载电流

R_L　　负载电阻

将（A7）、（A8）代入（A12）有：

$$\frac{V_i T}{2}\left\{\begin{array}{l}\dfrac{V_o}{L_1^{'}+L_2^{'}}[(D_{11}+D_{21}) \\ +(D_1-D_2)(D_{11}-D_{21})] \\ +\dfrac{V_i}{L_1}[(0.5-D_{11})(D_1-D_{11})] \\ +\dfrac{V_i}{L_2}[(0.5-D_{21})(D_2-D_{21})]\end{array}\right\} = \frac{V_o^2}{R_L} \tag{A14}$$

由于 D_{11}、D_{21} 和 δD 很小，我们进一步假设 $\delta D(D_{11}-D_{21})$ 、$D_{11}^2, D_{21}^2, \delta D D_{21}$ 可忽略，则（A14）变成：

$$\frac{V_i T}{2}\left\{\begin{array}{l}\dfrac{V_o}{2(1-k)L}(D_{11}+D_{21})+ \\ \dfrac{V_i}{L}*[0.5(2D+\delta D)-(0.5+D)(D_{11}+D_{21})]\end{array}\right\} \cong \frac{V_o^2}{R_L} \tag{A15}$$

由（A3）、（A4）可得（A16）-（A19），将（A19）代入（A15）得（A20）和（A21）。另外，二次方程（A20）的另一个解有 V_o 小于 V_i，不是变换器的有效解。

此外，只有当在 R_L 足够大以至于能维持图 4 所示波形时，（A21）才有效。

当 R_L 比（A22）给点值小时，输出电压会趋向于：

$$V_o = \frac{V_i}{1-(2D+\delta D)}$$

或 $$V_o = \frac{V_i}{1-(D_1+D_2)}$$

这个值正好与占空比为（D_1+D_2）且工作在 CICM 模式下的传统变换器输出电压一致。

通过将 $\begin{matrix} D_1 = D, D_2 = D+\delta D, L_1 = L_2 = L, \\ L_1^{'} = L_2^{'} = (1-k)L \end{matrix}$ 代入（A7）、（A8），I_1和 I_2之差为：

$$I_1 - I_2 = \frac{T}{2}\left\{\begin{matrix} \frac{V_o}{2L(1-k)}[(2D+\delta D)(D_{11}-D_{21}) \\ -2(D_{11}^2 - D_{21}^2)] \\ +\frac{V_i}{L}[-(0.5+D)(D_{11}-D_{21}) - 0.5\delta D \\ +D_{11}^2 - D_{21}^2 + \delta D D_{21}] \end{matrix}\right\} \quad \text{（A24）}$$

假设 $D_{11}^2, D_{21}^2, \delta D D_{21}$ 很小可忽略，则

$$I_1 - I_2 \cong \frac{T}{2}\left\{\begin{matrix} \frac{V_o}{2L(1-k)}[(2D+\delta D)(D_{11}-D_{21}) \\ +\frac{V_i}{L}[-(0.5+D)(D_{11}-D_{21}) - 0.5\delta D] \end{matrix}\right\} \quad \text{（A25）}$$

将（A18）代入（A25）得：

$$\begin{matrix} I_1 - I_2 = \frac{T\delta D}{4L(V_o - V_i(1-k))}\{V_o^2(2D+\delta D) \\ -V_o V_i * [2(1-k)(0.5+D)+1] + V_i^2(1-k)\} \end{matrix} \quad \text{（A26）}$$

文中提出的变换器中，（1-k）很小，因此电感的平均电流之差可以简化成下面的等式：

$$I_1 - I_2 \cong \frac{T\delta D}{4L}[V_o(2D+\delta D) - V_i] \quad \text{（A27）}$$

Steady-State Analysis of an Interleaved Boost Converter with Coupled Inductors

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***Abstract*—Boost converters are widely used as power-factor corrected preregulators. In high-power applications, interleaved operation of two or more boost converters has been proposed to increase the output power and to reduce the output ripple. A major design criterion then is to ensure equal current sharing among the parallel converters. In this paper, a converter consisting of two interleaved and intercoupled boost converter cells is proposed and investigated. The boost converter cells have very good current sharing characteristics even in the presence of relatively large duty cycle mismatch. In addition, it can be designed to have small input current ripple and zero boost-rectifier reverse-recovery loss. The operating principle, steady-state analysis, and comparison with the conventional boost converter are presented. Simulation and experimental results are also given.**

***Index Terms*—Coupled inductors, current sharing, interleaved boost converters.**

I. INTRODUCTION

WITH the tightening requirements of power quality, offline power supplies are required to operate at high power factor and to draw low harmonic currents from the ac mains. The conventional method of reducing input current harmonics using an *LC* input filter is no longer practically sufficient to meet the requirements in many high-power applications. Active power-factor correction using buck, boost, buck–boost, Cuk and Sepic converters has been proposed. Among these converters, the single-ended boost converter has been widely adopted as a front-end power-factor-corrected(PFC) regulator. The reasons for using boost converter are the simplicity in circuit and system design, reduced voltage stress on devices, and high conversion efficiency compared to the other topologies. Further, the step-up conversion makes it suitable for universal input voltage application (90 264 V).

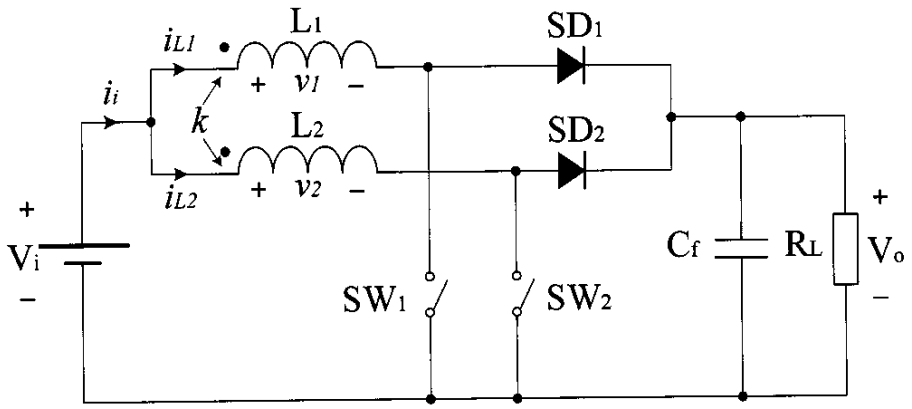


Fig. 1. Converter consisting of two interleaved and intercoupled boost converter cells.

PFC boost converters operating in continuous inductor current mode (CICM) have better utilization of power devices, lower conduction loss, and lower input current ripple. On the other hand, boost converters in discontinuous inductor current mode (DICM) have lower boost-rectifier reverse-recovery. loss and lower transistor switching-on loss [1], [2]. In order to reduce the input current ripple, modified boost converter topologies have been proposed in [3]–[5].

In high-power applications (greater than 1.5 kW), boost converters are often paralleled in an interleaved manner to increase the output current and reduce the input current ripple. However, current sharing among the parallel paths is a major design problem. It can be shown that, when two similar but independently controlled boost converters are connected in parallel(with the same input and output voltages), the converter with a larger duty cycle may operate in CICM, while the other will then automatically operate in DICM. Under this condition, any further additional loading current will be taken up by the converter in CICM operation. Thus, current sharing is very sensitive to the mismatch in duty cycle. The design of current-sharing control circuits has been discussed in [1], [6], [7]. A method of using hysteresis current control in a pair of boost converters with coupled inductors has also been suggested in [8].

In this paper, a converter consisting of two interleaved and intercoupled boost converter cells is proposed and studied. The converter can be designed to have a simple circuit, excellent current sharing characteristics, low input current ripple, and zero boost-rectifier reverse-recovery loss. The operating principle, steady-state analysis, and comparison with the conventional boost converter are described. The concept is demonstrated by simulation and experimental results.

II. OPERATING PRINCIPLE

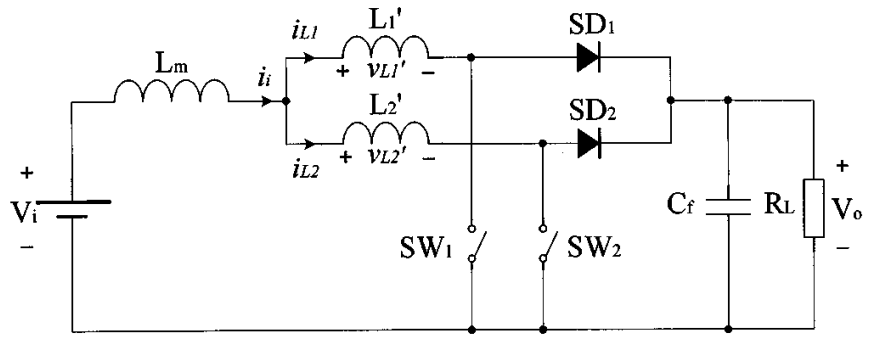


Fig. 2. Equivalent circuit of the converter.

Fig. 1 shows the schematic diagram of the proposed converter, consisting of two interleaved and intercoupled boost converter cells. The inductors and are closely coupled and with the same winding orientation. The coupled inductors can be represented by an equivalent circuit with three uncoupled inductors as illustrated in Fig. 2. The relationships of the inductors are related by the following equations:

$$L_1^{'} = L_1 - L_m \qquad (1)$$

$$L_2^{'} = L_2 - L_m \qquad (2)$$

$$L_m = k\sqrt{L_1 L_2} \qquad (3)$$

where ,

L1、L2 inductances of the two inductors;

K coupling coefficient; ,

L1`、L2` leakage inductances of the two inductors in the equivalent circuit;

Lm mutual inductance.

Referring to the equivalent circuits for the different switching states shown in Fig. 3 and the waveforms in Fig. 4, the operation of the converter can be explained as follows.

1) *State a [Fig. 3(a)]:*

At time , SW is closed. The current in the inductor starts to rise while continues to discharge. (The current in was acquired in the last switching cycle.) The rate of change of is approximately given by

$$\frac{di_{L2}}{dt} = \frac{-V_o}{L_1^{'} + L_2^{'}} \qquad (4)$$

2) *State b [Fig. 3(b)]:* At time , falls to zero. continues to rise and the rate of change of is

$$\frac{di_{L1}}{dt} = \frac{V_i}{L_1} \qquad (5)$$

where .

3) *State c [Fig. 3(c)]:*

At time , SW is opened. The energy stored in the inductor is transferred to the load via the boost rectifier SD . The rate of change of is

$$\frac{di_{L1}}{dt} = \frac{-(V_o - V_i)}{L_1} \qquad (6)$$

4) *State d [Fig. 3(d)]:*

The switch SW is closed at time . The current in inductor starts to rise. continues to discharge. The rate of change of is approximately given by

$$\frac{di_{L1}}{dt} = \frac{-V_o}{L_1' + L_2'} \qquad (7)$$

5) *State e [Fig. 3(e)]:*

At time , the inductor current rises at the rate of

$$\frac{di_{L2}}{dt} = \frac{V_i}{L_2} \qquad (8)$$

where .

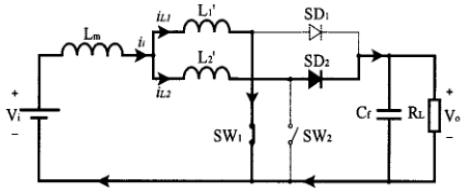
6) *State f [Fig. 3(f)]:*

At time , SW is opened. discharges through the output circuit. The rate of change of is

$$\frac{di_{L2}}{dt} = \frac{-(V_o - V_i)}{L_2} \qquad (9)$$

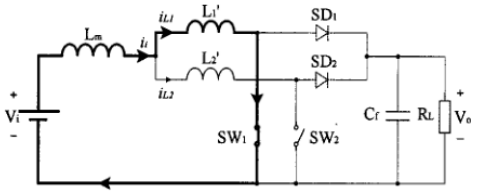
The switching cycle will be repeated when SW is turned on again at t0.

A careful study of the waveforms shown in Fig. 4 will reveal the following interesting facts. 1) As far as the input current is concerned, the converter appears to operate in CICM (because is continuous). Thus, the peak current stress of the inductors/switches and the input current ripple can be maintained relatively low. 2) However, as far as the individual boost converter cells are concerned, since and are discontinuous, these converter cells are actually operating in DICM. This helps solve the problem of uneven current sharing. Also, since the boost rectifier SD /SD is turned off before SW /SW is turned on, the reverse-recovery loss of the boost rectifiers is eliminated. In the waveforms shown in Fig. 4, it has been purposely assumed that the duty cycle of SW (denoted as) is significantly larger than that of SW (denoted as). However, this results in only a small change in the sharing of currents between the two inductors (and as shown in Fig. 1). This is because of the fact that, for one half of the switching cycle flows through , and for the other half of the switching cycle flows through . If is made relatively constant, and will be approximately equal.



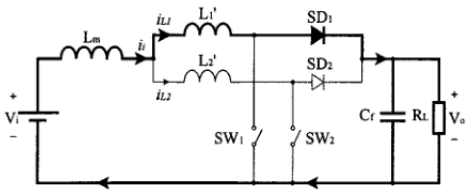
Time t_0–t_1

(a)



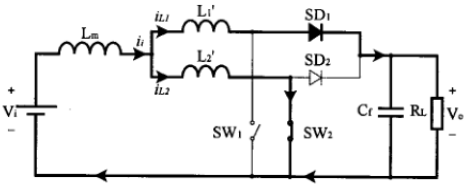
Time t_1–t_2

(b)



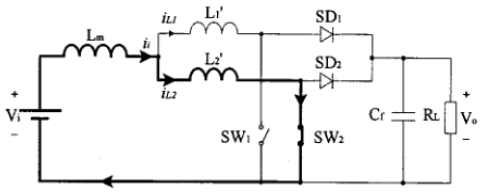
Time t_2–t_3

(c)



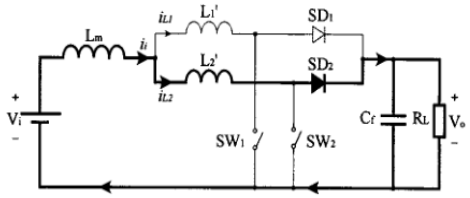
Time t_3–t_4

(d)



Time t_4–t_5

(e)



Time t_5–t_6

(f)

III. STEADY-STATE ANALYSIS

Assume that the current waveforms shown in Fig. 4 have reached a steady state. From the waveform of shown in Fig. 4, it can be found that From the waveform of shown in Fig. 4, it can be found that Also from Fig. 4, the average values of and , denoted as and , respectively, are found as Assume that the converter is lossless, i.e., the input power is equal to the output power where is the load resistance. In principle, (10)–(14) can be solved to find . However, in order to simplify the calculation, it is assumed that , some algebraic manipulations and solving a quadratic equation derived from (14), the expression for the output voltage is obtained as shown in (15) at the bottom of the page. [The detailed derivation is given in the Appendix, where the expression for is derived as (A21).] It should be noted that (15) is valid only if is real (having no imaginary part). Physically what it means is shown in (16) at the bottom of the page. When is smaller than the value given by (16), the output voltage will tend to approach the value of which is the output voltage of a conventional boost converter in CICM of operation with a duty cycle of ( ). In the Appendix, it is also found [from (A27)] that the difference between and (which are the average values of and , respectively) is given by It is interesting to note the following. 1) The difference between and is (approximately) proportional to , and this difference can be reduced by increasing the inductance . 2) When , we have (approximately) Therefore, as far as current sharing is concerned, (for each switching transistor) is the best operating point.

$$V_o = \frac{[1+2(1-k)(0.5+D)(1-2D-\delta D)] + \sqrt{[1+2(1-k)(0.5+D)(1-2D-\delta D)]^2 - 4(1-k)(1-\delta D)\left[\frac{4L(1-k)}{R_L T} + (1-2D-\delta D)\right]}}{2\left[\frac{4L(1-k)}{R_L T} + (1-2D-\delta D)\right]} V_i \quad (15)$$

$$R_L \geq \frac{16L(1-k)^2(1-\delta D)}{T\{[1+2(1-k)(0.5+D)(1-2D-\delta D)]^2 - 4(1-k)(1-\delta D)(1-2D-\delta D)\}} \quad (16)$$

IV. COMPARISON WITH CONVENTIONAL BOOST CONVERTER AND DESIGN CONSIDERATIONS

In this section, the characteristics of the proposed converter will first be compared with those of the conventional boost converter (for both CICM and DICM operations). Some special design features of the proposed converter will then be briefly discussed. *A. Comparison with Conventional Boost Converter* A comparison of the characteristics between the conventional converter and the proposed converter is given in Table I. *B. Magnetic Design* In the proposed converter, if the

two inductors are more tightly coupled, i.e., and are small compared with , the current waveforms become more rectangular. However, if and are too small, there is a tendency for SD and SD to conduct simultaneously at *states c* and *f* [Fig. 3(c) and (f)]. The proposed converter will then behave like a single boost converter with two active switches in parallel. In order to prevent this from happening, we need to keep or larger than about 1 V, so that the conducting inductor (either and) will have a sufficiently large back EMF to reverse biase the diode rectifier connected to the other inductor. The practical coupling coefficient can be chosen in the range of 0.9 0.98. In the practical construction of the intercoupled inductors, a lower value of can be achieved by physically separating the two windings and possibly also introducing an air gap between them, thus resulting in a larger leakage magnetic flux. *C. Feedback Design* In the design of the feedback control circuit, the proposed converter could be treated as a single boost converter with a duty cycle of (assuming). The design procedures are then much the same as those of conventional boost converters.

	Conventional Converter in CICM (Assuming a smooth input current i_i)	Conventional Converter in DICM (Assuming a triangular i_i, i.e.,critical mode operation)	Proposed Converter (Assuming a smooth input current i_i, and therefore rectangular i_{L1} and i_{L2})
RMS current in input inductor	Normalised to 1 (1 winding)	1.414 (1 winding)	0.707 (2 windings)
Suitability for parallel operation	Not Suitable	Suitable	Suitable
Reverse-recovery loss of rectifier	Large	Small	Small
Output ripple	Large	Large	Small
No. of rectifiers required	1	1	2
Average rectifier current	Normalised to 1	1	0.5
Max peak current stress of rectifier	Normalised to 1	2	1
No. of transistor switches required	1	1	2
Average transistor switch current	Normalised to 1	1	0.5
Max peak current stress of transistor switch	Normalised to 1	2	1

V. SIMULATION RESULTS

A PSpice simulation model of the proposed converter has been developed. Ideal switches and diodes are used in the model. The simulated waveforms are shown in Figs. 5 and 6. The simulation conditions are summarized as follows: , F, H, , V, and kHz. In Fig. 5, . In Fig. 6, , . The simulation results are as follows. In Fig. 5, (peak) (peak) A, (average value of) (average value of) A, and V. In Fig. 6, (peak) A, (peak) A, (average value of) A, (average value of) A, and V. It is interesting to note that, even in the presence of 40% mismatch in duty cycles (and), the difference between the average inductor currents (and) is only 1.3% (1.52 and 1.54 A, respectively).

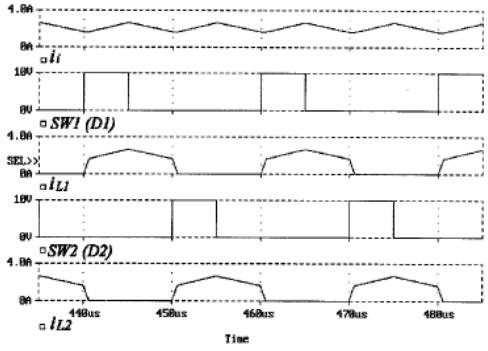


Fig. 5. Simulated current waveforms with matched duty cycles.

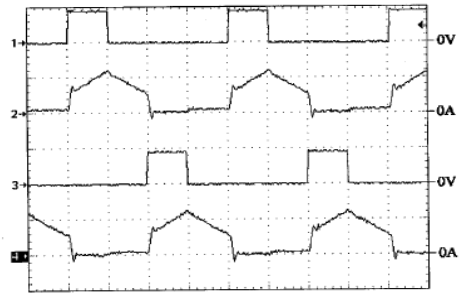


Fig. 7. Experimental waveforms with matched duty cycles. Vertical: trace 1, trigger signal of SW_1 (10 V/div); trace 2, inductor current i_{L_1} (2 A/div); trace 3, trigger signal of SW_2 (10 V/div); trace 4, inductor current i_{L_2} (2 A/div). Horizontal: time, 5 μs/div.

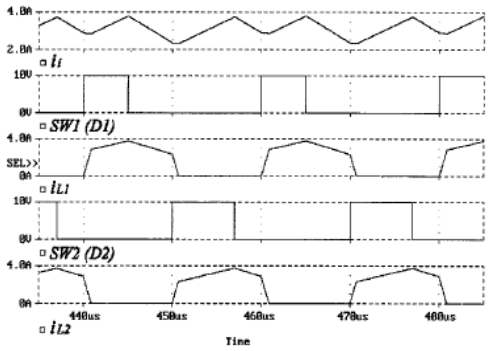


Fig. 6. Simulated current waveforms with mismatched duty cycles.

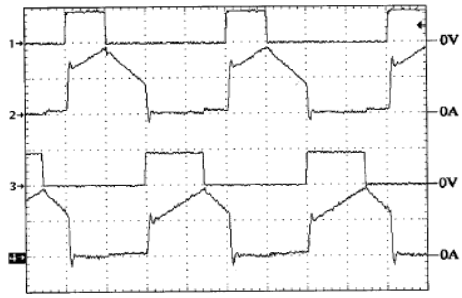


Fig. 8. Experimental waveforms with mismatched duty cycles. Vertical: trace 1, trigger signal of SW_1 (10 V/div); trace 2, inductor current i_{L_1} (2 A/div); trace 3, trigger signal of SW_2 (10 V/div); trace 4, inductor current i_{L_2} (2 A/div). Horizontal: time, 5 μs/div.

VI. EXPERIMENTAL RESULTS

An experimental prototype circuit, as shown in Fig. 1, has been built. The component values used are the same as those for the simulation described in Section V. Fig. 7 shows the experimentally measured inductor current waveforms for duty cycles . The two inductor currents are practically the same. Fig. 8 shows the measured inductor current waveforms for and . The average values of these inductor currents are 1.46 A and 1.50 A, respectively. They differ by only 3%. The calculated difference based on (14), (15), and (18) is also approximately 3%.

VII. CONCLUSION

A method to equalize the current sharing between two parallel- connected boost converters has been proposed. This results in a converter comprised of two interleaved and intercoupled boost converter cells. The proposed circuit has the following advantages.

- Even in the presence of large duty cycle mismatch, the intercoupled cells have only small unbalance in current sharing.
- It can be designed to have a small input current ripple and zero boost-rectifier reverse-recovery loss.
- It does not require any current sensor.
- It is less costly because the two boost converter cells share the same magnetic core.

Analytical expressions for steady-state operation have been derived to illustrate the excellent current sharing characteristics. The performance of the converter has also been demonstrated by simulation and experiments.

APPENDIX

DC ANALYSIS OF INTERLEAVED BOOST CONVERTER WITH COUPLED INDUCTORS

From the steady-state waveform of shown in Fig. 4, it can be found that From the waveform of in Fig. 4, it can also be found that From (A1) and (A2), and can be expressed as (A3) and (A4), which are shown at the bottom of the page. Also from Fig. 4, the average values of and , denoted as and respectively, are found as Assume that the converter is lossless, i.e., the input power is equal to the output power . We have (A9) (A10) (A11) (A12) where average input current; average current in (or); average current in (or); load current; load resistance. Substitution of (A7) and (A8) into (A12) gives The value of can be obtained by substituting (A3) and (A4) into (A13), and solving the resulting quadratic equation. To simplify the calculation, assume , , , and . Equation (A13) then becomes (A14) Since , , and are small, we further assume that , , , and are negligible. Equation (A14) then becomes From (A3) and (A4), (A16)–(A19) can be found, as shown at the bottom of the page. Substituting (A19) into (A15) and then rearranging, we have (A20) and (A21), shown at the bottom of the page. Note that the other root of the quadratic equation (A20) gives a less than , which is not a valid solution to a boost converter. It should also be noted that (A21) is valid only when is sufficiently large so as to maintain the current waveforms shown in Fig. 4, i.e., (A22), shown at the bottom of the page. When is smaller than the value given by (A22), the output voltage will tend to approach the value of or (A23) which is the output voltage of a conventional boost converter in CICM operation with a duty cycle of ( ). By substituting , , and into (A7) and (A8), the difference between and (which are the

average values of and respectively) is found as Applying the assumptions that , , and are small and negligible, (A25) Substitution of (A18) into (A25) gives (A26) In the proposed converter, the term ( ) is small. Equation (A25) can, therefore, be further reduced to give the following expression for the difference between the two average inductor currents:

$$I_1 - I_2 \cong \frac{T\delta D}{4L}\left[V_o(2D+\delta D) - V_i\right]. \qquad \text{(A27)}$$

$$D_{11} = \frac{V_o V_i\left[1+2(1-k)(0.5-D)\right] - V_i^2(1-k) - V_o^2(1-2D-\delta D)}{2V_i\left[V_o - V_i(1-k)\right]} \qquad \text{(A16)}$$

$$D_{21} = \frac{V_o V_i\left[1+2(1-k)(0.5-D-\delta D)\right] - V_i^2(1-k) - V_o^2(1-2D-\delta D)}{2V_i\left[V_o - V_i(1-k)\right]} \qquad \text{(A17)}$$

$$D_{11} - D_{21} = \frac{V_o(1-k)}{V_o - V_i(1-k)}\delta D \qquad \text{(A18)}$$

$$D_{11} + D_{21} = 1 - \frac{V_o}{V_i}(1-2D-\delta D) \qquad \text{(A19)}$$

$$\left[\frac{4(1-k)L}{R_L T} + (1-2D-\delta D)\right]\left(\frac{V_o}{V_i}\right)^2 - \left[1+2(1-k)(0.5+D)(1-2D-\delta D)\right]\left(\frac{V_o}{V_i}\right) + (1-k)(1-\delta D) = 0 \qquad \text{(A20)}$$

$$V_o = \frac{\left[1+2(1-k)(0.5+D)(1-2D-\delta D)\right] + \sqrt{\begin{array}{l}\left[1+2(1-k)(0.5+D)(1-2D-\delta D)\right]^2 \\ -4(1-k)(1-\delta D)\left[\frac{4L(1-k)}{R_L T} + (1-2D-\delta D)\right]\end{array}}}{2\left[\frac{4L(1-k)}{R_L T} + (1-2D-\delta D)\right]} V_i \qquad \text{(A21)}$$

$$R_L \geq \frac{16L(1-k)^2(1-\delta D)}{T\left\{\left[1+2(1-k)(0.5+D)(1-2D-\delta D)\right]^2 - 4(1-k)(1-\delta D)(1-2D-\delta D)\right\}} \qquad \text{(A22)}$$