2 JDEL022

DIPLOMA IN ELECTRONICS ENGG. VI- SEMESTER

I- SESSIONAL TEST

M M:=15

VLSI Design - DEL -605

Q 1. State Moore's Law. Highlight its significance in predicting IC size in different generations Of IC technology.

(6)

OR

Explain what is meant by channel length modulation. What effect does it have on the I-V characteristics of MOSFETs?

Q2. Derive the current equation for the n-channel MOS transistor operating in the Linear region.

(9)

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(Q1) Why do we need MOSFET scaling ? What are the effects of MOSFET scaling on its operational characteristics ?

OR

(8)

Explain with suitable diagrams the oxide related capacitance between gate to Source,Cgs (total), for all the three operating modes of the MOS transistor. How Cgs varies with gate to source Voltage Vgs ?

(Q2) For N-MOS devices why resistance is not used as lead element. Discuss in detail N-MOS Depletion Mode pull up .

OR

(7)

Draw the circuit of NAND gate and NOR gate by using n-MOS.

Diploma in Electronics Engineering, Semester –VI, Examination, 2024

VLSI Design

Paper No. : DEL -605

Time : 3 Hours **Max Marks : 60**

(Write your Roll no. On the top immediately on receipt of this question paper)

Note: Attempt any two parts from each question. Each question carries equal marks.

Q1.(a) Derive the current equation for n-channel MOS transistor operating in Linear and Saturation region. **(06)**

(b) Define Threshold voltage. Explain the effect of body effect on threshold voltage. **(06)**

(c) Write short notes on

(i) Mobility variation effect. **(06)**

(ii) Hot electron effect

Q2. (a) Explain the Capacitance estimation of MOSFET. **(06)**

(b) Why do we need MOSFET scaling ? Explain the constant field scaling method. **(06)**

(c) Explain with suitable diagram the Junction capacitances of MOS transistor. **(06)**

Q3.(a) With the help of suitable diagrams, discuss different steps in fabrication of CMOS transistor process . **(06)**

(b) what is oxidation? Why is it needed? **(06)**

(c) What is ion implantation? What are its advantages over diffusion process? **(06)**

Q4.(a) For a CMOS inverter, discuss in detail about voltage transfer characteristics. **(06)**

(b) For NMOS devices why resistance is not used as lead element. Discuss NMOS Inverter with EMD load. **(06)**

(c) Draw the circuit of NAND gate and NOR gate by using n-MOS. **(06)**

Q5.(a) What is VHDL ? Explain its features. **(06)**

(b) Explain Entity in Hardware Description language. Give an example. **(06)**

(c) Write a HDL program for a 2-to-4 Decoder circuit using Behavioral style of Modeling. **(06)**

Code No.:DEL-605 Roll No. 20DE10

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VLSI Design

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Time : 3 Hours Max Marks : 60

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Note: Attempt any two parts from each question. Each question carries equal marks.

Q1.(a) Derive the current equation for n-channel MOS transistor operating in Saturation region. (06)

(b) Explain what is meant by channel length modulation. What effect does it have on the I-V characteristics of MOSFETs ? (06)

(c) Define Threshold voltage. Explain the effect of body effect on threshold voltage. (06)

Q2. (a)Explain the Resistance estimation of MOSFET. (06)

(b) Explain with suitable diagrams the oxide related capacitance between gate to Source,Cgs (total), for all the three operating modes of the MOS transistor. How Cgs varies with gate to source Voltage Vgs ? (06)

(c) Why do we need MOSFET scaling ? Explain the constant field scaling method. (06)

Q3.(a) With the help of suitable diagrams, discuss different steps in fabrication of NMOS transistor. (06)

(b)Discuss the mechanism of latch- up in CMOS circuits. Also give various methods to reduce the problem of latch-up in CMOS circuits. (06)

(c) Write short notes on the following Fabrication steps. (06)

(i) Oxidation.

(ii) Metallization.

Q4.(a) For N-MOS devices why resistance is not used as lead element. Discuss in detail N-MOS Depletion Mode pull up . **(06)**

(b) Realize two inputs NAND and NOR gates using CMOS. **(06)**

(c) Realize following function using CMOS logic gate circuit.

$$Y = \overline{A.B.C.D}$$

(06)

Q5.(a) What is VHDL ? Explain its features. **(06)**

(b) Explain Entity in Hardware Description language. Give an example. **(06)**

(c) Write a HDL program for a 2-to-4 Decoder circuit using Structural style of Modeling. **(06)**