1484/III

B. C. A. (Part-II) Examination, 2021-22

(Third Semester)

BCA-304 : COMPUTER ORGANIZATION AND ARCHITECTURE

Paper : IV

Time : Three Hours] [Maximum Marks : 70

Note: (i) Answer **Five** questions in all.

(ii) Question No. **1** is **compulsory.**

(iii) Answer remaining four questions, selecting **two** from each Section **A** and **B.**

(iv) All questions carry equal marks.

1. Answer all parts of the following:

(a) Differentiate between the term computer organization and computer architecture.

(b) List down the logic family with name of components used in it.

(c) Briefly describe about MUX.

(d) Perform the following operation using 2's complement arithmetic: $(110)_2 - (011)_2$

SECTION – A

SECTION – A

2. Draw the logic diagram of SR flip-flop also give its function table.

3. Perform summation between following numbers.

   (a) $(+1011)_2$ and $(-0101)_2$

   (b) $(10110)_2$ and $(-11010)_2$

   (c) (0011) and $(-0101)_2$

4. What is binary addition? Explain the role of full adder with suitable truth table and logic circuit for the purpose of addition of binary numbers.

5. Explain the memory hierarchy. What is cache memory? Why is it used?

SECTION – B

6. (a) Implement 16×1 MUX using 4×1 MUX es.

   (b) What is instruction set? Write a brief note on instruction cycle.

7. (a) Explain the basic addressing modes with suitable example.

   (b) Differentiate between Programmed I/ data transfer and DMA data transfer scheme.

8. (a) Give the implementation of arithmetic

SECTION – B

6. (a) Implement 16×1 MUX using 4×1 MUX es.

(b) What is instruction set? Write a brief note on instruction cycle.

7. (a) Explain the basic addressing modes with suitable example.

(b) Differentiate between Programmed I/ data transfer and DMA data transfer scheme.

8. (a) Give the implementation of arithmetic operations in computer system.

(b) Explain the operation of parallel adder/subtractor with suitable diagram.

9. Write notes on any two of the following:

(i) DMA

(ii) I/O module

(iii) Memory Management

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B.C.A. (PART-II) EXAMINATION, 2022-23

(Third Semester)

9237

(BCA 304 : COMPUTER ORGANIZATION AND ARCHITECTURE)

Paper : IV

Time : Three Hours] [Maximum Marks : 70

Note: (i) Answer **Five** Questions in all.

(ii) Question No.**1** is **Compulsory**.

(iii) Answer remaining **Four** questions, selecting **Two** from each Section **A** and **B**.

(iv) All questions carry equal marks.

1. Answer **all** parts of the following:

(a) Find 2's and 1's complement of the number -17 and 18

(b) How computer organization and architecture effects the performance of a computer?

(c) Explain working of D-Flip flop.

(d) Design a digital circuit that perform two logic operations of exclusive- OR and exclusive-NOR. Show logic diagram

SECTION-A

2. Represent $(-456.1234)_{10}$ in single precision and double precision format.

3. Explain the bus architecture with its types. Discuss also the I/O bus architecture with block diagram.

4. Solve the following:

   (a) $(734)_8 + (325)_8$

   (b) $(810) + (-417)$ Using 2's compliment

   (c) $(10000111)_2 - (1111100)_2$

   (d) $(-9764)_{10} + (-3778)_{10}$

5. What are half adder and full adder? Design a logic circuit diagram of full adder using truth table and K-map?

SECTION-B

6. (a) Draw the instruction word format. Indicate and explain number of bits required with its meaning on each part.

   (b) What do you mean by CPU organization? Explain various types of processor organization.

7. (a) Draw a diagram of bus system using MUX which has four registers of size 4 bits each.

(b) Draw the flowchart for instruction cycle with neat diagram and explain.

8. (a) Explain in detail the principle of carry look ahead adder and design 4-bit CLA adder

(b) Describe in detail immediate, direct, indirect and Register indirect addressing modes with suitable example and diagram if necessary.

9. Write notes on any of two of the following:

(a) Memory hierarchy

(b) DMA controller

(c) Interrupts

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B.C.A. (Part-II) EXAMINATION, 2023-24

[III[rd] SEMESTER]

1525

(BCA 304: Computer Organization and Architecture)

Paper : IV

Time : Three Hours] [Maximum Marks : 70

Note: (i) Answer **five** questions in all.

(ii) Question No. **1** is **compulsory**.

(iii) Answer remaining **four** questions, selecting **two** from each Section **A** and **B**.

(iv) All questions carry equal marks.

1. Answer all parts of the following :

(a) Give the difference between RAM and ROM.

(b) Find 2's and 1's complement of the number-18 and 17

(c) Explain working of encoder.

(d) Explain the concept of cache memory.

Section-A

2. Explain the bus architecture with its types. Also, discuss the I/O bus architecture with block diagram.

3. Solve the following :

   (a) $(721)_8 + (325)_8$

   (b) $(1000011)_2 - (111110)_2$

   (c) $(-976)_{10} + (-377)_{10}$

4. Give the generalized architecture of CPU and explain the function of different units therein.

5. What do you mean by addressing modes? Explain various types of addressing modes.

Section-B

6. (a) Explain the floating point representation with example.

   (b) Draw the flowchart for instruction cycle with neat diagram and explain.

7. (a) What do you mean by synchronous and asynchronous communication ?

(b) Draw a diagram of bus system using MUX which has four registers of size 4 bits each.

8. (a) Explain memory hierarchy in detail.

(b) Draw the logic diagram of a 3×8 decoder.

9. Write notes on any **two** of the following :

(a) ALU

(b) Division algorithm

(c) DMA

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