

Unit-1 Number System

The process of assigning zeros and ones to the voltage level is known as logic levels and it's of 2 types :-

- (a) +ve logic level < Here ON = 1 ; OFF = 0 >
- (b) -ve logic level < Here ON = 0 ; OFF = 1 >

Decimal Numbers :- (0 - 9) (Base 10)

(a) Decimal to Binary :-

$$(76)_{10} = (1001100)_2$$

(b) Decimal to Octal

$$(76)_{10} = (114)_8$$

2	76	LSB (Least sig. bit.)
2	38 - 0	
2	19 0	
2	9 - 1	
2	4 - 1	
2	2 - 0	
1	1 = 0	

MSB (Most significant Bit)

(c) Decimal to octal Hexadecimal

$$(76)_{10} = (4C)_{16}$$

A - 10
B - 11
C - 12
D - 13
E - 14
F - 15

Binary (Base 2) ; Octal (Base 8) ;

Hexadecimal (Base 16)

Conversion from other no. system to decimal

(a) Binary to decimal

$$(1 \ 0 \ 0 \ 1 \ 1 \ 1)_{\text{2}} = (39)_{10}$$

$$\begin{aligned} (1 \times 2^0) + (1 \times 2^1) + (1 \times 2^2) + (0 \times 2^3) + (0 \times 2^4) + (1 \times 2^5) \\ = 1 + 2 + 4 + 32 = 39 \end{aligned}$$

(b) Octal to decimal :-

$$(46)_{10} \rightarrow (38)_{10}$$

$$(6 \times 8^0) + (4 \times 8^1) = 6 + 32 = 38$$

Hexadecimal to decimal :-

$$(70)_{16} \rightarrow (112)_{10}$$

$$(0 \times 16^0) + (7 \times 16^1) = 0 + 112 = 112$$

Binary to octal

$$\begin{array}{r} 4 \\ | \\ 1001111 \\ | \\ 7 \end{array} \rightarrow (47)_8$$

Binary to Hexadecimal

$$\begin{array}{r} 00100111 \\ | \\ 2 \quad 7 \end{array} \rightarrow (27)_{16}$$

Binary

$$0 \rightarrow 0$$

$$1 \rightarrow 1$$

$$2 \rightarrow 10$$

$$3 \rightarrow 11$$

$$4 \rightarrow 100$$

$$5 \rightarrow 101$$

$$6 \rightarrow 110$$

$$7 \rightarrow 111$$

$$8 \rightarrow 1000$$

$$9 \rightarrow 1001$$

Signed Numbers :-

- In this, we need kept 4-bits upto 7
- In signed magnitude no., an extra bit is added in MSBS (most significant bit side)

zero is added for +ve nos

1 is added for -ve nos

A	10	$\rightarrow 1010$
B	11	$\rightarrow 1011$
C	12	$\rightarrow 1100$
D	13	$\rightarrow 1101$
E	14	$\rightarrow 1110$
F	15	$\rightarrow -1111$

- Another method to represent -ve decimal nos is ones compliment method.

e.g. 3 is 0011 but in ones compliment its 1100

→ Because its reverse.

→ Another method is Two's compliment.

Here we add 1 in ones compliment of a no. to get two's compliment.

$$\text{e.g.: } 1+1=10$$

$$1+1+1=11$$

$$n! = n \times (n-1) \times (n-2) \dots$$

$$5! = 5 \times 4 \times 3 \times 2 \times 1$$

Logic gates :- divided into two categories
 (a) Basic gates ; (b) Universal gates

1-august-2018

- Boolean Algebra :- It contains boolean functions which have expressions having boolean variables.
1. It is used for analysing a logic circuit.
 2. It is used to give its mathematical operations.
 3. It is used to simplify logic circuits and logic expression.

Boolean laws :-

Law

1. Identity law
2. Null Element law
3. Idempotent law
4. Commutative law
5. Associative law
6. Distributive law
7. Absorption law
8. Double Inversion / Involution law
9. Consensus law
10. De Morgan's Theorem :-

AND law

$$A \cdot 1 = A$$

$$A \cdot 0 = 0$$

$$A \cdot A = A$$

$$A \cdot B = B \cdot A$$

$$A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

$$A + (B \cdot C) = (A + B) \cdot (A + C)$$

OR law

$$A + 0 = A$$

$$A + 1 = 1$$

$$A + A = A$$

$$A + B = B + A$$

$$A + (B + C) = (A + B) + (A + C)$$

$$A + A \cdot B = A$$

$$A \cdot (A + B) = A$$

$$\bar{\bar{A}} = A$$

$$AB + \bar{A}C + BC = AB + \bar{A}C$$

$$\overline{A+B} = \bar{A} \cdot \bar{B} ; \quad \overline{A \cdot B} = \bar{A} + \bar{B}$$

Some other laws :-

$$1. A + \bar{A}B = A + B$$

$$2. \bar{A} + AB = \bar{A} + B$$

$$3. A + \bar{B} \cdot \bar{A} = A + \bar{B}$$

Proof and Verification of Boolean's Law :

$$1. A + (B \cdot C) = (A+B) \cdot (A+C)$$

Proof. R.H.S = $(A+B) \cdot (A+C)$

$$= A \cdot A + A \cdot C + B \cdot A + B \cdot C$$

Acc. to Idempotent law $A \cdot A = A$

$$\therefore = A + A \cdot C + B \cdot A + B \cdot C$$

$$= A(1+C) + A \cdot B + B \cdot C$$

Acc. to Null element law

$$A+1 = 1 \quad ; \quad 1+C = 1$$

$$\therefore = A \cdot 1 + A \cdot B + B \cdot C$$

$$= A(1+B) + B \cdot C$$

$$= A(1) + B \cdot C$$

$$= A + B \cdot C = L.H.S \quad \text{Hence Proved}$$

3-August

$$2. AB + \bar{A} \cdot C + B \cdot C = AB + \bar{A} \cdot C$$

$$= L.H.S = AB + BC + \bar{A} \cdot C$$

$$= A \cdot B + B \cdot C \cdot (1) + \bar{A} \cdot C$$

$$= AB + BC(A + \bar{A}) + \bar{A} \cdot C$$

$$= AB + BCA + \bar{A}BC + \bar{A}C$$

$$= AB(1+C) + \bar{A}C(B+1)$$

$$= AB \cdot 1 + \bar{A}C \cdot 1$$

$$= AB + \bar{A}C = R.H.S$$

$$3. \text{ Show that } A + AB = A$$

$$= L.H.S = A + AB$$

$$= A(1+B)$$

$$= A \cdot 1 = A = R.H.S$$

De- Morgan's Theorem

$$(a) \overline{A+B} = \overline{A} \cdot \overline{B}$$

It means that $\overline{A} \cdot \overline{B}$ is equal to the complement of $A+B$

∴ We can write,

$$(A+B) + (\overline{A} \cdot \overline{B}) = 1$$

On applying distributive law, we get

$$(A+B+\overline{A}) \cdot (A+B+\overline{B}) = 1$$

$$(1+B) \cdot (1+A) = 1$$

$$1 \cdot 1 = 1.$$

$$(b) \overline{A \cdot B} = \overline{A} + \overline{B}$$

L.H.S.

$$(A \cdot B) \cdot (\overline{A} + \overline{B}) = 0$$

$$A \cdot \overline{A} \cdot B + A \cdot B \cdot \overline{B}$$

$$= 0 \cdot B + A \cdot 0 = 0$$

Proved.

2nd method: By substituting various values

Sum of Product (SOP); Product of Sum (POS)

SOP: Product term of a funct. are added in this form also known as MinTerm & denoted by 'm'

POS: Sum terms of a funct. are multiplied with each other in this form. also known as Max terms, denoted by 'M'.

Ig.	A	B	C	SOP	POS
	0	0	0	$\overline{A} \cdot \overline{B} \cdot \overline{C}$	$A+B+C$
	0	0	1	$\overline{A} \cdot \overline{B} \cdot C$	$A+B+\overline{C}$
				!	!
				!	!

$$\text{Net } \sum m = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{\overline{A} \cdot \overline{B} \cdot C}$$

$$\bar{M} = (A+B+C)(A+B+\overline{C})$$

And Gate :-		SOP		POS	
A	B	$A \cdot B = Y$		$A+B$	only $Y=1$ terms will be included
0	0	0		$A+\bar{B}$	
0	1	0		$\bar{A}+B$	
1	0	0			
1	1	1	$A \cdot B$		
<u>Note :-</u>		$A \cdot B$		$(A+B)(A+\bar{B})(\bar{A}+B)$	

7-August-2018

→ Standard and Non-standard for POS & SOP forms.
Standard form is also known as canonical form.

Eg:- $y = AB + A\bar{B}\bar{C} + \bar{A}BC \rightarrow$ Non-stand-form SOP
 $y = AB + \bar{A}B + \bar{A}\bar{B} \rightarrow$ stand-form SOP
 $y = (\bar{A}+B) \cdot (A+B) \cdot (A+\bar{B}) \rightarrow$ stand-form POS
 $y = (\bar{A}+B) \cdot (A+B+C) \rightarrow$ Non-stand-form POS.

→ Conversion from Non-stand POS & SOP to canonical/standard form.

1. SOP :-

- Rules:-
- For each term find the missing literal
 - ANDing the terms with the term formed by ORing the missing literal + its complement.

Eg:- $y = \frac{AB}{C} + \frac{A\bar{C}}{\bar{B}} + \frac{BC}{A} \leftarrow$ missing.

$$\begin{aligned} y &= AB(C+\bar{C}) + A\bar{C}(B+\bar{B}) + BC(A+\bar{A}) \\ &= ABC + ABC + A\bar{B}\bar{C} + A\bar{B}C + ABC + \bar{A}BC \end{aligned}$$

2. POS :-

- Rules:-
- For each term find the missing literal
 - ORing the each term by the term formed by ANDing the missing literal with its complement.

$$\text{eg. } Y = \overbrace{(A+B)}^C \cdot \overbrace{(A+C)}^B \cdot \overbrace{(B+\bar{C})}^A \leftarrow \text{minterms}$$

$$= (A+B+C \cdot \bar{C}) (A+C+B \cdot \bar{B}) (A \bar{A} + B + \bar{C})$$

A	B	C	Y	(m ₀) SOP (minterm) (Σm)	(M ₀) POS (Maxterm) (ΠM)
0	0	0	0	m ₀ $\bar{A} \bar{B} \bar{C}$	M ₀ A + B + C
1	0	1	1	m ₁ $\bar{A} \bar{B} C$	M ₁ A + B + \bar{C}
2	0	1	0	m ₂ $\bar{A} B \bar{C}$	M ₂ A + \bar{B} + C
3	0	1	1	m ₃ $\bar{A} B C$	M ₃ A + \bar{B} + \bar{C}
4	1	0	0	m ₄ $A \bar{B} \bar{C}$	M ₄ $\bar{A} + B + C$
5	1	0	1	m ₅ $A \bar{B} C$	M ₅ $\bar{A} + B + \bar{C}$
6	1	1	0	m ₆ $A B \bar{C}$	M ₆ $\bar{A} + \bar{B} + C$
7	1	1	1	m ₇ $A B C$	M ₇ $\bar{A} + \bar{B} + \bar{C}$

$$\Phi(Y) = \sum m (1, 2, 5, 6) ; Y = \prod m (0, 3, 4, 7)$$

$2^n = x$, n - no of inputs, x - no. of comb.

Karnaugh - Map (K-Map) :- It is the simplification technique used to reduce the Boolean equation. This technique can be used upto 6 variables & disadvantage of this tech is that this tech. cannot be automated.

Step 1: Filling in SOP

For 2 variables

A	B	0	1
\bar{A}	0	0	1
1	1	1	1

no need to mention

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

In case of 3 variables,

the comb. is 00,01,11,10.

Acc to grey code. i.e

00 → 01 → 11 → 10

01 After 01 u can't change to 10
 ↓ b' because it needs replacement of 2 bits where
 as 01 → 11 can be changed easily as it needs 1 bit only

For 3 variables

BC		AB			
		00	01	11	10
A	\bar{A}	0	1	3	2
\bar{A}	0	0	1	3	2
A	1	4	5	7	6

For 4 variables

CD		AB				BC			
		00	01	11	10	00	01	11	10
AB		00	01	11	10	00	01	11	10
00	01	11	10	00	01	11	10	00	01
01	11	10	00	01	11	10	00	01	11
11	10	00	01	11	10	00	01	11	10
10	00	01	11	10	00	01	11	10	00

Step 2: GROUPING:

- * single (1) ; pair (2) ; quad (4), octa (8), hexa (16) group

RULES FOR GROUPING:

1. NO diagonal grouping at any stage can take place.
2. Only adjacent sides or adj. 1's can be grouped together.
3. A single 1 can be shared by any no. of groups.
4. Top side with last side and left side with right side can be grouped together.

Note: 5. The size of the group should be as

Note: 6. Large as possible.

6. The number of groups should be as least as possible.



Make: Doesn't go for single grouping until or unless you have
single 1 remaining

Step 3:

HAVE UR ANS:-

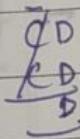
AB		$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$		00	01	11	10
$\bar{A}\bar{B}$	00	I			
$\bar{A}\bar{B}$	01		I		
$A\bar{B}$	11			I	
$A\bar{B}$	10	I			

$$\begin{aligned} I &:: \bar{C}D \\ &= D \end{aligned}$$

and $\bar{A}B$ AB

$$= B$$

Ans (I) BD



(IV) :- $CD \cdot C\bar{D}$
= C .

and $\bar{A}B$

Ans II = $\bar{A}BC$

(V) :- $A\bar{C}\bar{D}$

and $A\bar{B}$

Ans III = $\bar{C}\bar{D} \cdot A\bar{B}$

Hence, final Ans. :- $BD + \bar{A}BC + A\bar{B}\bar{C}\bar{D}$ Ans.

8-August-2018

Ques. $F(A, B, C) = \sum m(1, 3, 5, 6, 7)$

0-3 → 2

0-7 → 3

0-15 → 4

0-31 → 5

	A	B	C	Y
m_0	0	0	0	0
m_1	0	0	1	1
m_2	0	1	0	0
m_3	0	1	1	1
m_4	1	0	0	0
m_5	1	0	1	1
m_6	1	1	0	1
m_7	1	1	1	1

A	$\bar{B}C$	$\bar{B}C$	BC	$B\bar{C}$
0	00	01	11	10
1	10	11	01	00
0	01	11	10	02
1	10	01	00	01

000 → 0

001 → G1

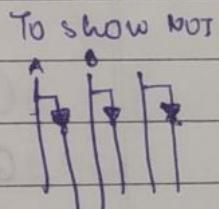
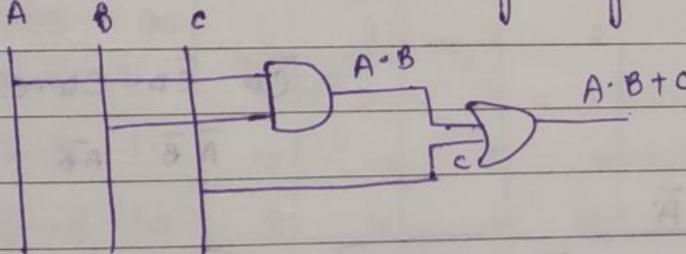
$G_1 \rightarrow (\bar{B}C + BC)$

$G_1 \rightarrow C$

$G_2 \rightarrow B \cdot A$

Total = $G_1 + G_2 = C + AB = Y$

Realisation into logic gates:-

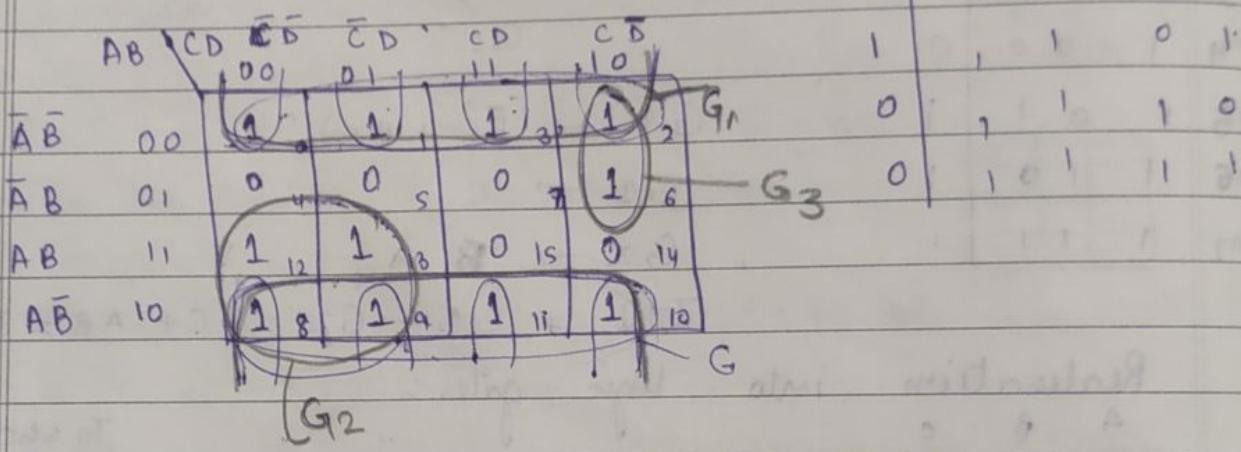


Ques. $f(Y) = \sum m(0, 1, 2, 3, 6, 8, 9, 10, 11, 12, 13)$

2, 3, 8, 5, 6

A	B	C	D	y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	1	0	0	0
1	0	0	0	0
0	0	1	1	1
0	1	1	0	0
1	1	0	0	0
1	0	1	0	1
1	0	0	1	1
0	1	0	1	1

R	Y	S	A	B	C	D
01	0	0	0	0	0	0
1	0	0	0	1	0	0
1	0	0	1	0	0	0
1	0	0	1	1	0	0
0	0	1	0	0	0	1
0	0	1	0	1	0	0
1	0	1	1	0	0	0
0	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	1	1	0
1	1	1	0	0	0	0



$$G_1 \rightarrow \bar{B}$$

$$G_2 \rightarrow \bar{C} \cdot A$$

$$G_3 \rightarrow \bar{C}\bar{D} \cdot \bar{A}$$

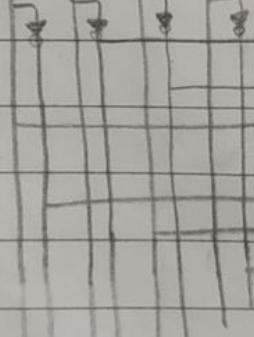
$$\text{Total} = [\bar{B} + \bar{C} \cdot A + \bar{C}\bar{D} \cdot \bar{A}] = Y$$

$$\bar{C}\bar{D} \quad \bar{C}D \quad CD \cdot \bar{C}\bar{D} =$$

$$\bar{A}\bar{B} \quad \bar{A}B$$

key gate:-

A B C D



C.A

A.B.C

$$\bar{A}\bar{D}C + A\bar{C} + \bar{B} = Y$$

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Page No. 11
Date:

SOP:

$AB\backslash CD$	$\bar{C}\bar{D}$	G_1	G_2
$\bar{A}\bar{B} \ 00$	1	1	3
$\bar{A}B \ 01$	4	5	7
$AB \ 11$	12	13	15
$A\bar{B} \ 10$	8	9	14
		G_3	G_4

SOP:

$$G_1 \rightarrow \bar{A}\bar{B} \ \bar{A}B \ AB \ A\bar{B}, \ \bar{C}\bar{D} \Rightarrow \bar{C}\bar{D}$$

$$G_2 \rightarrow \bar{C} \bar{A} \bar{B}$$

$$G_3 \rightarrow D \ A B$$

$$G_4 \rightarrow A C D$$

$$G_5 \rightarrow \bar{D} \ \bar{A} \ B$$

$$Y = G_1 + G_2 + G_3 + G_4 + G_5$$

$$Y = \bar{C}\bar{D} + \bar{A}\bar{B} \bar{C} + ABD + ACD + \bar{A}B\bar{D}$$

Ans

POS :-

TM (2, 5, 7, 10, 14)

$A+B$	$C+D$	$C+\bar{D}$	$\bar{C}+\bar{D}$	$\bar{C}+D$
$A+B \ 00$	0	1	3	2
$A+\bar{B} \ 01$	4	5	7	6
$\bar{A}+\bar{B} \ 11$	12	13	15	14
$\bar{A}+B \ 10$	8	9	11	10

$$C+\bar{D} + \bar{C}+\bar{D} = \bar{D}$$

$$A+\bar{B} + \bar{A}+\bar{B} = \bar{B}$$

$$G_1 = \bar{B} + \bar{D}$$

(d) Don't Care Conditions :

$$Y = \Sigma m(0, 1, 4, 6, 8, 11, 12, 13, 15) + d(2, 3, 7)$$

$AB\backslash CD$	00	01	11	10
00	1	1	3	X_2
01	1	X_5	X_7	1
11	1	1	15	14
10	1	2	11	10

either 0 or 1
take it 0 or 1 acc.
to the need.

Special Case of K-Map :

AB	CD	$\bar{C}\bar{D}$	CD	$C\bar{D}$	$\bar{C}\bar{D}$
$\bar{A}\bar{B}$	1				1
$\bar{A}B$					
AB					
$A\bar{B}$	1			1	

$$\bar{E}\bar{D} \cdot C\bar{D} = \bar{D}$$

$$A\bar{B} \cdot A\bar{B} = \bar{B}$$

$$Y = \bar{B}\bar{D}$$

Ques:- $Y = \sum m (0, 2, 5, 7, 8, 10, 13, 15)$

AB	CD	$\bar{C}\bar{D}$	CD	$C\bar{D}$	$\bar{C}\bar{D}$
$\bar{A}\bar{B}$	1				
$\bar{A}B$	1	1	1	1	1
AB	1	1	1	1	1
$A\bar{B}$	1	1	1	1	1

 G_1

$$Y = BD + \bar{B}\bar{D}$$

$$G_1 = \bar{C}D, CD = D$$

$$\bar{A}B, AB = B$$

$$G_F = BD$$

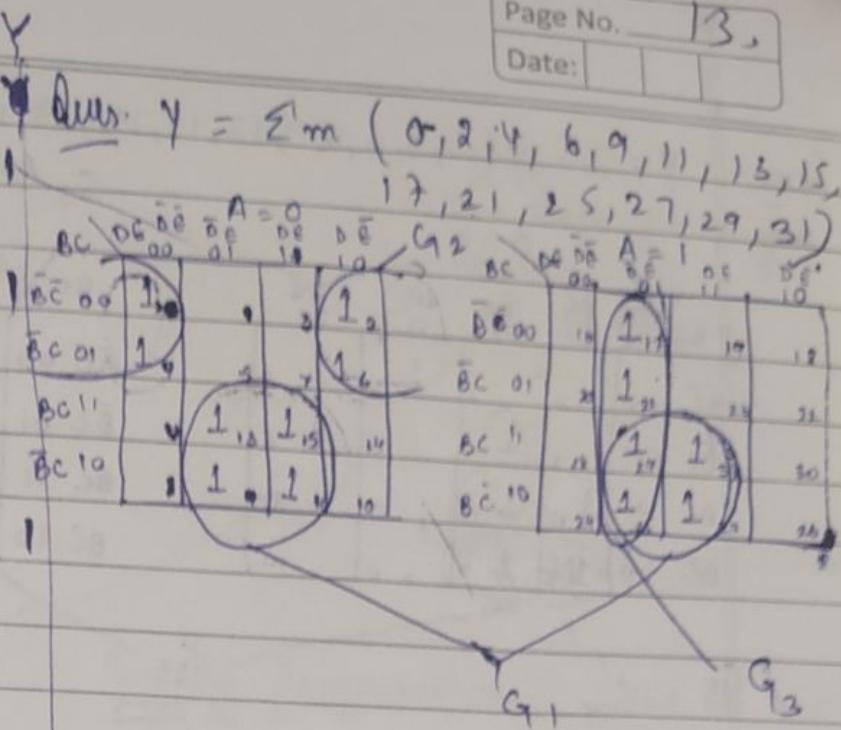
$$G_2 = \bar{B}\bar{D}$$

5-Variable K-Map :-

	A	B	C	D	E	Y	BC'D'E'	A=0	BC'D'E'	A=1
m_0	0	0	0	0	0	1		0	1	3
m_1	0	0	0	0	1	0		4	5	6
m_2	0	0	0	1	0	1		12	13	15
m_3	0	0	0	1	1	1		8	9	10
m_4	0	0	1	0	0	1				
m_5	0	0	1	0	1	1				
m_6	0	0	1	1	0	1				
m_7	0	0	1	1	1	1				
m_8	0	1	0	0	0					
m_9	0	1	0	0	0	1				
m_{10}	0	1	0	1	0	0				
m_{11}	0	1	0	1	1	1				
m_{12}	0	1	1	0	0	0				
m_{13}	0	1	1	0	1	1				

only adjacent larger group of
 $13 \rightarrow 29. yl$

m ₁₄	0	1	1	0
m ₁₅	0	1	1	1
m ₁₆	1	0	0	0
m ₁₇	0	0	0	1
m ₁₈	0	0	1	0
m ₁₉	0	0	1	1
m ₂₀	0	1	0	0
m ₂₁	0	1	0	1
m ₂₂	0	1	1	0
m ₂₃	0	0	0	0
m ₂₄	0	0	0	1
m ₂₅	1	0	1	0
m ₂₆	0	1	0	0
m ₂₇	0	0	1	1
m ₂₈	0	1	0	0
m ₂₉	0	1	0	1
m ₃₀	0	1	1	0
m ₃₁	0	1	1	1

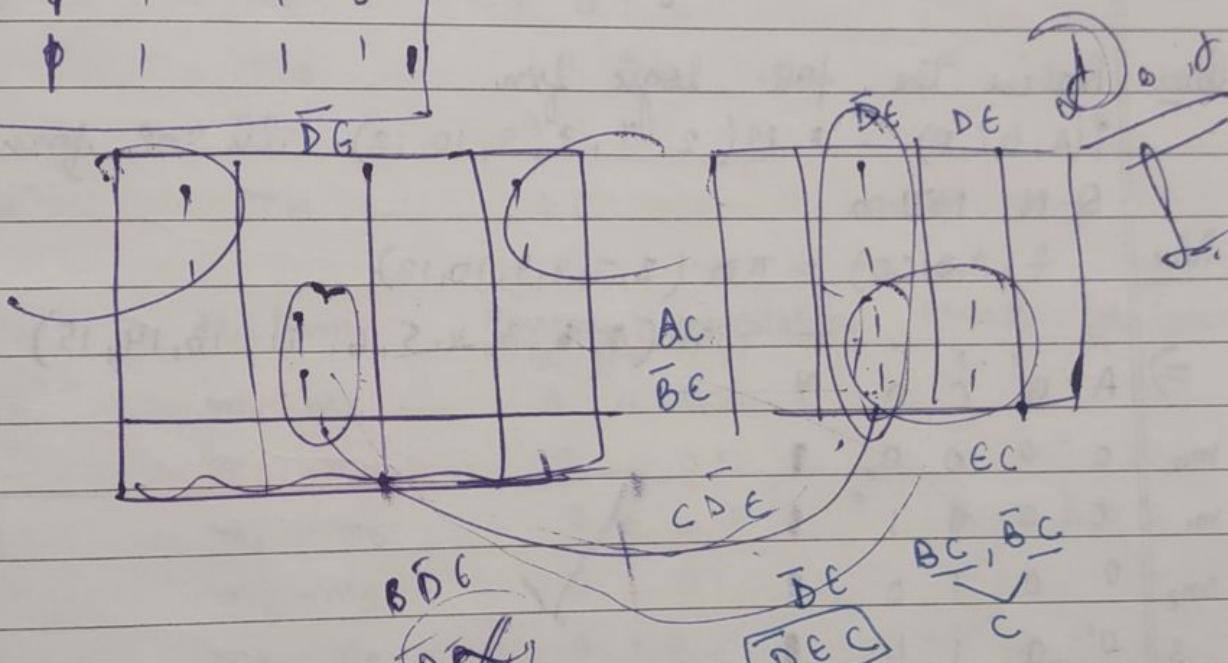


$$G_1 = BE$$

$$G_2 = \bar{A}\bar{B}\bar{E}$$

$$G_3 = A\bar{D}G$$

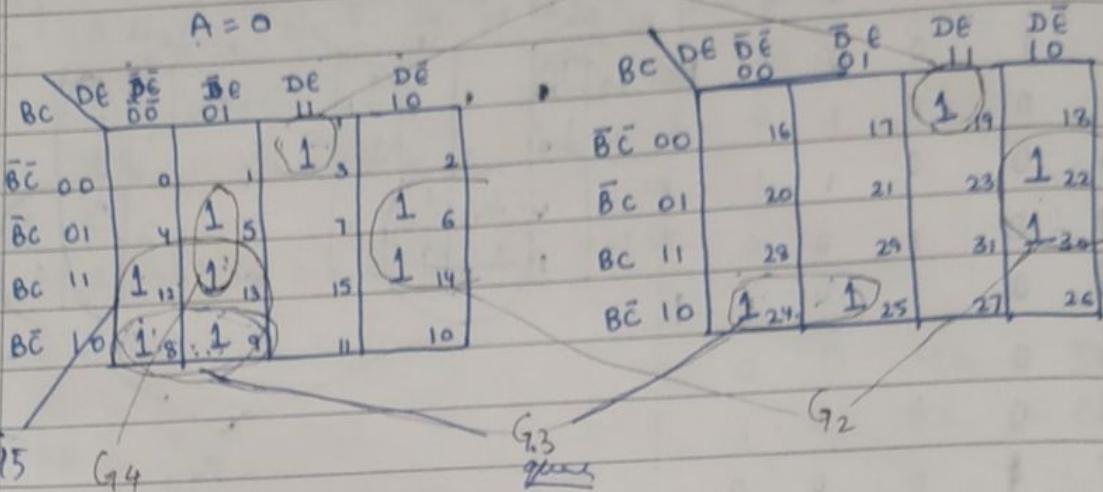
$$Y = BG + \bar{A}\bar{B}\bar{E} + A\bar{D}E$$



$$Y = \sum m (3, 5, 6, 8, 9, 12, 13, 14, 19, 22, 24, 25, 30)$$

Ques.
Ans.

$$Y = \sum m(3, 5, 6, 8, 9, 12, 13, 14, 19, 22, 24, 25, 30)$$



$$G_1 = DE \cdot \bar{BC} ; G_2 = CD \cdot \bar{E} ; G_4 = \bar{A} C \bar{D} \bar{E}$$

$$G_3 = \bar{D} B \bar{C} , G_5 = \bar{A} \bar{B} \bar{D}$$

01-August-2018

Simpl

Quine - Mc - Cluskey (QM) Method

Ques. Realise the foll. logic fxn

$f(A, B, C, D) = \sum m(2, 7, 8, 9, 10, 12)$ in SOP form using Q-M Method

$$f(A, B, C, D) = \sum m(2, 7, 8, 9, 10, 12)$$

$$\Rightarrow \begin{array}{cccc} A & B & C & D \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 2 & 0 & 0 & 1 & 0 \\ 3 & 0 & 0 & 1 & 1 \\ 4 & 0 & 1 & 0 & 0 \\ 5 & 0 & 1 & 0 & 1 \\ 6 & 0 & 1 & 1 & 0 \\ 7 & 0 & 1 & 1 & 1 \end{array} = \sum m(0, 1, 3, 4, 5, 6, 11, 13, 14, 15)$$

m ₀	0	0	0	0	1
m ₁	0	0	0	1	1
m ₂	0	0	1	0	0
m ₃	0	0	1	1	1
m ₄	0	1	0	0	1
m ₅	0	1	0	1	1
m ₆	0	1	1	0	1
m ₇	0	1	1	1	0

8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

Change of 1 bit only
can make grouping possible.

Group	Minterm	Binary Representation	Check for Group.
0	m_0	A B C D 0 0 0 0	✓
1	m_1	0 0 0 1	✓
	m_4	0 1 0 0	✓
2	m_3	0 0 1 1	✓
	m_5	0 1 0 1	✓
	m_6	0 1 1 0	✓
3	m_{11}	1 0 1 1	✓
	m_{13}	1 1 0 1	✓
	m_{14}	1 1 1 0	✓
4	m_{15}	1 1 1 1	✓

Group	Minterm	Binary Representation	Check for Group.
0	$m_0 - m_1$	A B C D 0 0 0 -	✓
	$m_0 - m_4$	0 - 0 1	✓
1	$m_1 - m_3$	0 0 - 1	* $\bar{A} \bar{B} D$
	$m_1 - m_5$	0 - 0 1	✓
	$m_4 - m_5$	0 1 0 -	✓
	$m_4 - m_6$	0 1 - 0	* $\bar{A} \bar{B} \bar{D}$
2	$m_3 - m_{11}$	- 0 1 1	* $\bar{B} C D$
	$m_5 - m_{13}$	- 1 0 1	* $\bar{B} \bar{C} D$
	$m_6 - m_{14}$	- 1 1 0	* $B C \bar{D}$

3	$m_{11} - m_{15}$	1 - 11	*	ACD
	$m_{13} - m_{15}$	1 1 - 1	*	ABD
	$m_{14} - m_{15}$	1 1 1 -	*	ABC

⇒ Group	Minterm	Binary Representation				check for gp.
		A	B	C	D	
0	$m_0 - m_1 - m_4 - m_5$	0 - 0 -				
	$m_0 - m_4 - m_1 - m_5$	0 - 0 -				$\bar{A} \bar{C}$

Prime implicants - all those m- which were no gp. in 3rd last table & last tableⁱⁿ which no further grouping is possible - all these values are known together give prime implicants

$$\Rightarrow Y = \bar{A}\bar{B}D + \bar{A}B\bar{D} + \bar{B}CD + B\bar{C}D + BCD + ACD + ABD + ABC \\ + \bar{A}\bar{C}$$

⇒ Prime Implicant Table - To have Essential Prime Implicant we need to draw it - make it

PI	Minterm No	Given Minterm							
		0	1	3	4	5	11	13	14
$\bar{A}\bar{B}D$	1, 3	X	X						
$\bar{A}\bar{B}\bar{D}$	4, 6			X	X				
$\bar{B}CD$	3, 11		X			X			
$B\bar{C}D$	5, 13			X			X		
$B\bar{C}\bar{D}$	8, 14				X		X		
ACD	11, 15				X			X	
ABD	13, 15					X			X
ABC	14, 15					X		X	
$\bar{A}\bar{C}$	0, 1, 4, 5	X	X		X	X		X	X
EPI							↑	↑	↑

$$Y = \overline{B}(\overline{CD} + B\overline{C}\overline{D} + ABD + \overline{A}\overline{C})$$

representation

Ans. Using K map. solve.

$$f(A, B, C, D) = \sum m(0, 1, 3, 4, 5, 6, 11, 13, 14, 15)$$

Solve:

		CD		CD		CD		CD	
		AB		00	01	11	10		
$\bar{A}\bar{B}$	00	1	0	1	1	1	0		
$\bar{A}\bar{B}$	01	1	1	1	0	1	1		
AB	10	1	1	1	1	1	1	1	1
AB	11	1	0	1	0	1	0	1	0

G_1 , G_2 , G_3 , G_4

$$G_1 = \bar{A}\bar{C}, G_2 = \bar{B}CD, G_3 = \bar{C}\bar{D}B,$$

$$G_4 = ABD; G_5 =$$

$$Y = \bar{A}\bar{C} + \bar{B}CD + BC\bar{D} + ABD$$

Why QM-map? Coding is possible in case of QM Map whereas it is not so possible in case of K-Map.

Ques. = $\sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 11, 14)$ Solve using QM Method

Solve. $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

	A	B	C	D	Y	A	B	C	D	Y	
m_0	0	0	0	0	1	m_9	1	0	0	1	1
m_1	0	0	0	1	1	m_{10}	1	0	1	0	0
m_2	0	0	1	0	1	m_{11}	1	0	1	1	1
m_3	0	0	1	1	1	m_{12}	1	1	0	0	0
m_4	0	1	0	0	0	m_{13}	1	1	0	1	0
m_5	0	1	0	1	1	m_{14}	1	1	1	0	1
m_6	0	1	1	0	0	m_{15}	1	1	1	1	0
m_7	0	1	1	1	1						
m_8	1	0	0	0	1						

\Rightarrow Group		Minterm	Binary Rep.	checks for Gp.
			A B C D	
0	m_0		0 0 0 0	✓
1	m_1		0 0 0 1	✓
	m_2		0 0 1 0	✓
	m_8		1 0 0 0	✓
2	m_9		0 0 1 1	✓
	m_{10}		0 1 0 1	✓
	m_9		1 0 0 1	✓
3	m_7		0 1 1 1	✓
	m_{11}		1 0 1 1	✓
	m_{14}		1 1 1 0	✗ ABCD

\Rightarrow Group		Minterm	(B.R)(A B C D)	check for Gp.
0	$m_0 - m_1$		0 0 0 +	✗ ✓
	$m_0 - m_2$		0 0 - 0	✗ ✓
	$m_0 - m_8$		- 0 0 0	✗ ✓
1	$m_1 - m_3$		0 0 - 1	✗ ✓
	$m_1 - m_5$		0 - 0 1	✗ ✓
	$m_1 - m_9$		- 0 0 1	✗ ✓
2	$m_2 - m_3$		0 0 1 -	✗ ✓
	$m_8 - m_9$		1 0 0 -	✗ ✓
3	$m_0 - m_7$		0 - 1 1	✗ ✓
	$m_3 - m_{11}$		- 0 1 1	✗ ✓
	$m_5 - m_9$		0 1 - 1	✗ ✓
	$m_9 - m_{11}$		1 0 - 1	✗ ✓

\Rightarrow Group.		Minterms	A B C D	Check for Gp.
0	$m_0 - m_2 - m_1 - m_3$		0 0 - -	✓
	$m_0 - m_8 - m_1 - m_9$		- 0 0 -	✓
1	$m_1 - m_3 - m_5 - m_7$		0 0 - -	✓
	$m_1 - m_3 - m_9 - m_{11}$		- 0 - 1	✓

$$\begin{array}{c|cc} 0 & 0 \\ \hline m_1 - m_5 - m_3 - m_{17} & 0 \\ m_1 - m_9 - m_3 - m_{11} & 0 \\ \hline m_2 - m_{12} & 1 \end{array}$$

\Rightarrow Group

Minterum

A B C D

Check for Gp.

$$\begin{array}{l}
 m_0 - m_1 - m_2 - m_3 \quad 00-- \\
 m_0 - m_1 - m_8 - m_9 \quad -00- \\
 m_0 - m_2 - m_1 - m_3 \quad 00-- \\
 m_0 - m_8 - m_1 - m_9 \quad -00-
 \end{array}
 \left. \begin{array}{l} \\
 \\ \\
 \end{array} \right\} \bar{A}\bar{B} \quad \left. \begin{array}{l} \\
 \\ \\
 \end{array} \right\} \bar{B}\bar{C}$$

1

$$m_1 - m_3 - m_5 - m_7$$

0 - - 1

$$m_1 - m_3 - m_9 - m_{11}$$

二〇一

~~m m m m~~

1

$$m_1 - m_9 = m_3 - m_1$$

- 0 - 1

$$m_1 - m_2 - m_3 - m$$

0 - 1

$$Y = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}D + \bar{B}D + ABC\bar{D}$$

Do it again

\Rightarrow Prime implicant Table

Using K-map solve $\Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

AB \ CD	$\bar{A}\bar{D}$	$\bar{A}D$	$A\bar{D}$	AD
$\bar{A}\bar{B}$	00	01	11	10
$\bar{A}B$	01	11	10	00
AB	11	10	01	00
$A\bar{B}$	10	01	00	11
G ₁	1	1	0	0
G ₂	1	0	1	1
G ₃	0	1	1	1
G ₄	1	1	1	0
G ₅	1	0	0	1

$$\bullet 1 - 2 \rightarrow 10,$$

$$1+1 = \bar{A}\bar{B},$$

$$= 0 \bar{B}\bar{C}$$

$$= \bar{A}\bar{B}$$

$$= \bar{B}\bar{D}$$

$$G_1 \rightarrow \bar{A}\bar{D}; G_2 \rightarrow \bar{A}\bar{B}; G_3 \rightarrow A\bar{B}D; G_4 \rightarrow \bar{B}\bar{C}\bar{D}$$

$$G_5 \rightarrow AB\bar{C}\bar{D}$$

$$Y = \bar{A}\bar{D} + \bar{A}\bar{B} + A\bar{B}D + \bar{B}\bar{C}\bar{D} + ABC\bar{D}$$

28-Aug-2018

Code Conversion

Gray code				Binary				(Not to conv. about carry)			
A	B	C	D	E	F	G	H	1001	1001	00	00
0	0	0	0	0	0	0	0	1001	1001	01	01
1	0	0	1	0	0	0	1	1111	1111	11	10
2	0	0	1	0	0	1	1	1010	1010	10	11
3	0	0	1	1	0	0	10	0101	0101	01	00
4	0	1	0	0	1	1	0	1110	1110	11	10
5	0	1	0	1	1	1	1	1011	1011	10	11
6	0	1	1	0	1	0	1	1011	1011	11	01
7	0	1	1	1	0	0	1	1100	1100	01	00
8	1	0	0	0	1	0	0	1011	1011	11	00
9	1	0	0	1	0	1	0	1101	1101	11	11
10	1	0	1	0	1	1	1	1111	1111	00	00
11	1	0	1	1	1	1	0	1110	1110	11	11
12	1	1	0	0	1	0	1	1010	1010	10	00
13	1	1	0	1	1	0	1	1011	1011	11	00

Binary to Gray

$\begin{array}{c} \swarrow \searrow \\ 1001 \\ \downarrow \\ 1001 \end{array}$

Page No. 21

Date:

14 1 1 1 0 1 0 0 1
15 1 1 1 1 1 0 0 0

gray to

Binary

$(\text{sum of } q_1 + q_2)/2$

for F

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	00	0	0	2	0
$\bar{A}B$	01	0	4	0	5
AB	11	1	12	1	13
A \bar{B}	10	1	8	1	9

G₁

for F

AB	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	00	0	0	2
$\bar{A}B$	01	1	4	5
AB	11	0	15	1
A \bar{B}	10	1	3	1

G₂

for G

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	1	3
$\bar{A}B$	1	4	1	5	0
AB	1	12	1	13	0
A \bar{B}	0	8	0	9	1

G₁

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	1	1	3
$\bar{A}B$	0	4	1	5	0
AB	0	12	1	13	0
A \bar{B}	0	8	1	9	0

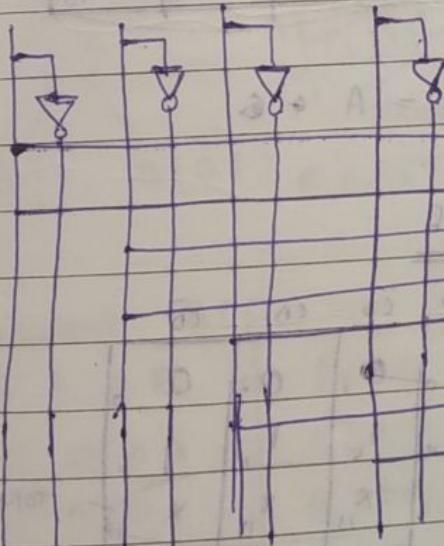
G₁

G₂

$$\text{for E} = A \cdot 0 ; \text{ for F} = \bar{A}B + A\bar{B} = A \oplus B \text{ EXOR}$$

$$\text{for G} = \bar{B}\bar{C} + \bar{B}C ; \text{ for H} = \bar{C}D + C\bar{D} = C \oplus D \text{ EXOR}$$

A B C D



$$O_E = A \cdot 0$$

$$O_F = A \oplus B$$

$$O_G = B \oplus C$$

$$H = C \oplus D$$

$$D/P = A + (A \oplus B) + (B \oplus C) + (C \oplus D)$$

10110
11010
10110
10110

24-august - 2018

RENAULT

Date:

22

Binary Coded Decimal (BCD) Code / 8421 Code

0 0000

1 0001

2 0010

3 0011

4 0100

5 0101

6 0110

7 0111

8 1000

9 1001

$$(a) (23)_{10} \rightarrow (10110)_2$$

(BCD) — 23

2 / 3
0010 0011

$$(23)_{10} = (0010, 0011)_{BCD}$$

BCD

Decimal to Bin

$$(b) 146$$

0001 0100 0110

$$(146)_{10} = (0001, 0100, 0110)_{BCD}$$

Convert decimal no \rightarrow 4-bit BCD code

Ques. Design a four-bit binary to 4-bit BCD code

A	B	C	D	BCD
E	F	G	H	
0	0	0	0	0, 0 00
1	0	0	0	1 0001
2	0	0	1	0 010
3	0	0	1	0 011
4	0	1	0	0 100
5	0	1	0	0 101
6	0	1	1	0 110
7	0	1	1	0 111
8	1	0	0	1 000
9	1	0	0	1 001
10	1	0	1	X X X X
11	1	0	1	X X X X
12	1	1	0	X X X X
13	1	1	0	X X X X
14	1	1	1	X X X X
15	1	1	1	X X X X

K-Map

AB	GH	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
00	00	0	0	0	0
00	01	0	0	0	1
01	00	0	1	1	0
01	01	0	1	1	1
10	00	1	0	0	0
10	01	1	0	0	1
11	00	1	1	1	0
11	01	1	1	1	1

$$E = A + G$$

FonF

AB	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
AB	0, 0	0, 1	0, 1	0
$\bar{A}\bar{B}$	1, 0	1, 1	1, 1	1
AB	X, 0	X, 1	X, 1	X
$\bar{A}\bar{B}$	0, 0	0, 1	1, 1	X

Take as

$$F = B$$

For G

	$\bar{A} \bar{B}$	$A \bar{B}$	AB	$\bar{C} \bar{D}$	$C \bar{D}$	CD	$C \bar{B}$
0	0 0	0 1	1 0	1 3	1 2	1 3	1 2
1	0 1	1 0	1 1	0 5	1 7	1 7	1 6
2	1 0	X	X	1 2	X	X	1 5
3	1 1	X	X	1 3	X	X	1 4
4	0 0	0 1	0 1	0 8	X	X	1 0
5	0 1	1 0	1 1	0 9	X	X	1 1
6	1 0	X	X	1 0	X	X	1 0
7	1 1	X	X	1 1	X	X	1 1

For H

	0	1	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
2	X	X	X	X	X
3	0	1	1	1	0
4	0	1	1	1	0
5	X	X	X	X	X
6	0	1	1	1	0
7	0	1	1	1	0

$$G = C$$

$$H = D$$

Ex - 3 Code } derived from BCD code

(No.) \rightarrow BCD \rightarrow Ex-3 code

$$\text{eg. } (8)_{10} \rightarrow 1000 \xrightarrow{\text{every bit}} + 0011 \\ \underline{(1011)}$$

$$(42)_{10}.$$

$$\begin{array}{r} 0100 \quad 0010 \\ + 0010 \quad + 0010 \\ \hline 0110 \quad 0101 \end{array}$$

$$(42)_{10} = (0111\ 0101)_{\text{Ex-3}}$$

$$+ 3 + 3 \\ \hline 7 5$$

$$(0111\ 0101)_{\text{Ex-3}}$$

P̄S

$$(62)_{10} \\ + 3 + 3 \\ \hline 9 5 \\ / \\ (001\ 0101)_{\text{Ex-3}}$$

P̄Q R

P̄Q (P̄S)

P̄Q R

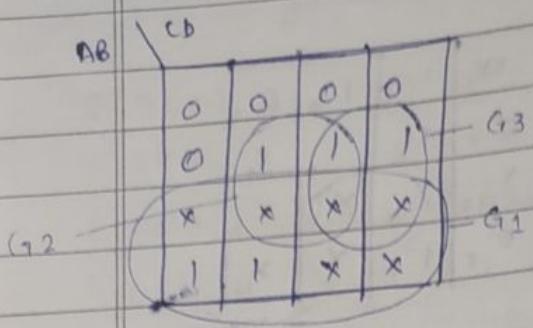
P̄Q (P̄S) X P̄Q R

P̄Q R X P̄Q (P̄S)

P̄Q R X P̄Q R

for G

for F



$$E = A + B \cdot C + B \cdot D$$

for G

for H

28/Aug/18. Magnitude comparative

input \rightarrow van - K-map
 output \rightarrow how many
 K-map

Two-bit magnitude comparative

	X	Y	$x > y / y > x$	$x > y / y \geq x$	$x = y$
m ₀	00	00	0	0	1
m ₁	00	01	0	0	0
m ₂	00	10	1	0	0
m ₃	00	11	1	0	0
u	01	00	0	1	0
s	01	01	0	0	1
g	01	10	1	0	0
y	01	11	1	0	0
g	10	00	0	1	0
g	10	01	0	1	0
g	10	10	0	0	1
g	10	11	1	0	0

	$y > x$	$x > y$	$x = y$
11 00	0	1	0
11 01	0	1	0
11 10	0	1	0
11 11	0	0	1

F0H $x \leftarrow y$

AB	CD	$\bar{C}D$	$\bar{C}\bar{D}$	$C\bar{D}$	CD
$\bar{A}\bar{B}00$	0	1	1	1	0
$\bar{A}\bar{B}01$	4	5	1	7	1
$A\bar{B}11$	12	13	15	14	
$AB10$	8	9	11	10	

F0H $x > y$

AB	CD	$\bar{C}D$	$\bar{C}\bar{D}$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	-	-	0	1	2
$\bar{A}B$	1	1	1	5	
AB	12	13	1	15	14
$A\bar{B}$	8	9	11	10	

$$y = C \cdot \bar{A} + \bar{A}\bar{B}D + \bar{B}CD$$

3 AND, 7 OR gates

$$Y = A\bar{C} + B\bar{C}\bar{D} + AB\bar{D}$$

3 AND, 4 OR Gates

F0H $x = y$

AB	CD	$\bar{C}D$	$\bar{C}\bar{D}$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	1	0	1	3	2
$\bar{A}B$	4	1	1	7	6
AB	12	9	3	15	14
$A\bar{B}$	8	9	11	10	

diagonal direction

EX-OR

EX-NOR

$$\oplus \bar{A}B + A\bar{B} = X - OR$$

$$\ominus AB + \bar{A}\bar{B} = X - NOR$$

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} + A\bar{B}CD$$

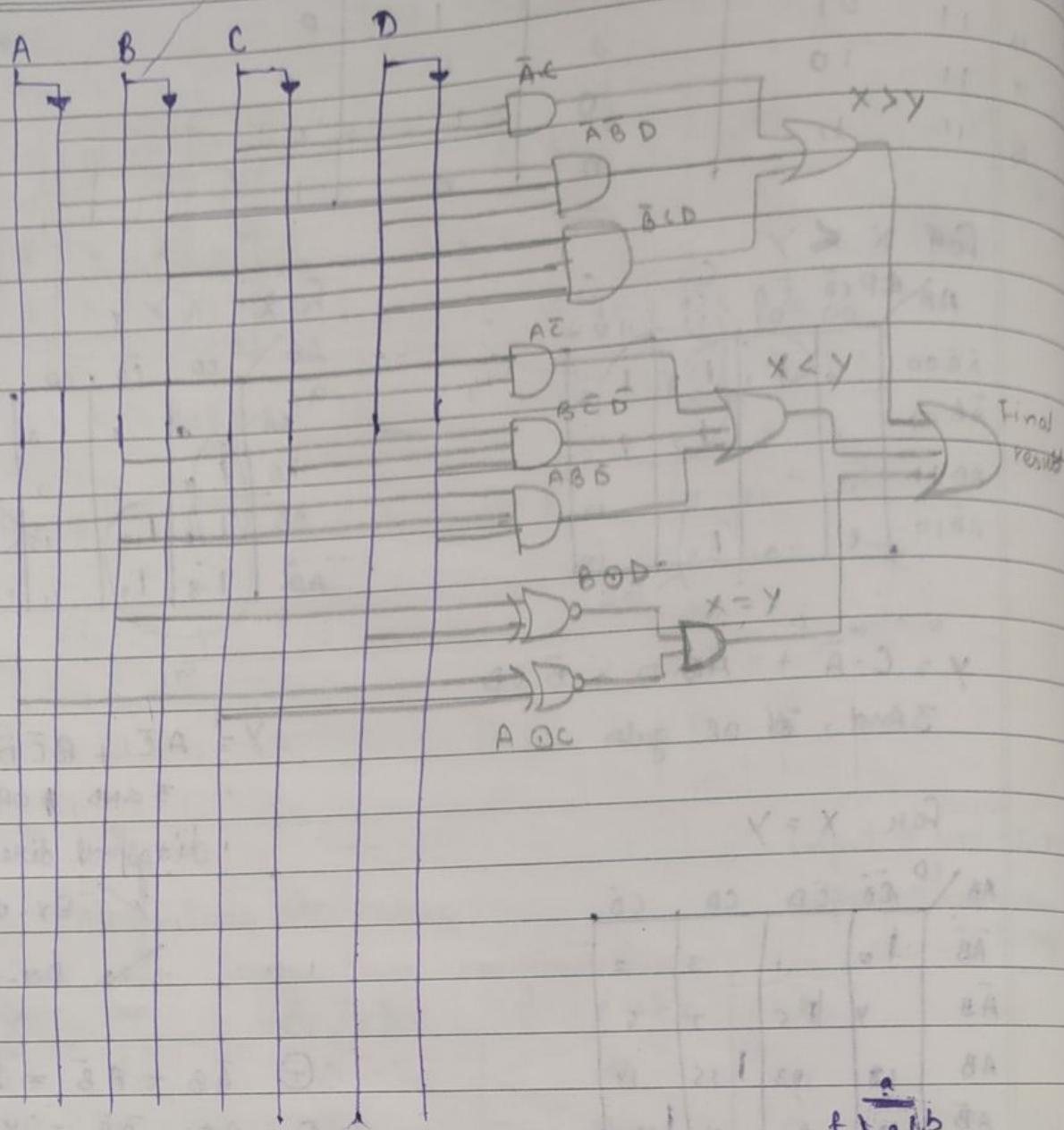
$$= \bar{A}\bar{C}(\bar{B}\bar{D} + B\bar{D}) + AC(BD + \bar{B}\bar{D})$$

$$= (\bar{B}\bar{D} + BD) + (AC + \bar{A}\bar{C})$$

$$= (B \oplus D)(A \odot C)$$

$$= 2 EX-NOR, 1 AND gate$$

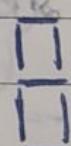
$$\text{Final Result : } (\bar{A}C + \bar{A}\bar{B}D + \bar{B}CD) + (\bar{A}\bar{C} + B\bar{C}\bar{D} + AB\bar{D}) + [(B \oplus D)(A \odot C)]$$



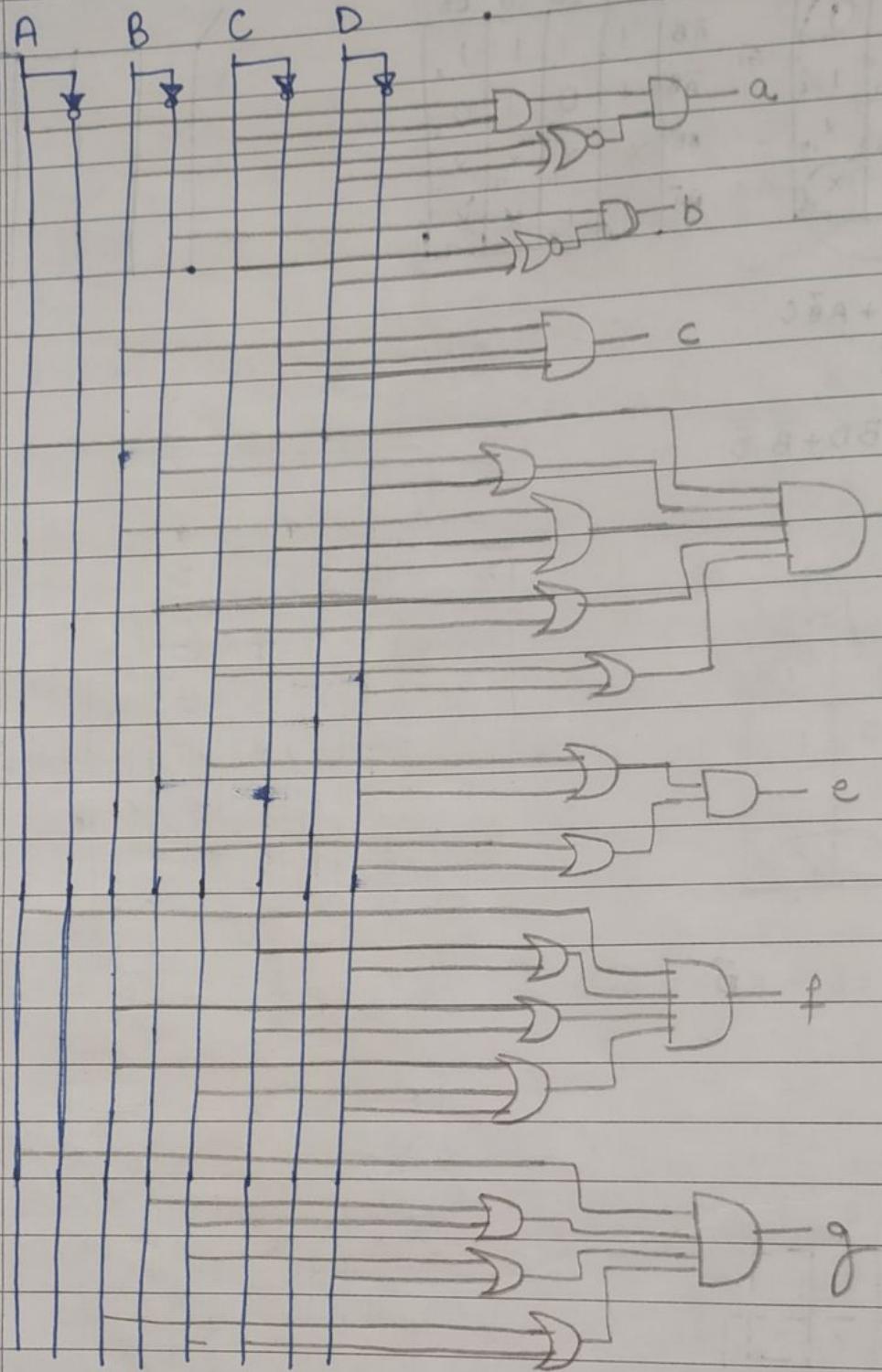
BCD to Seven segment display encoder

	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	0
3	0	0	1	1	1	1	1	1	1	0	0
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	0	1	0	1	1	0	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	1	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	1	0	1

+ $\frac{a}{e}$ $\frac{b}{f}$ $\frac{c}{g}$ $\frac{d}{h}$



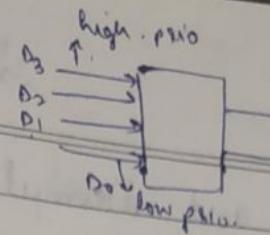
Z



with Priority Encoder :-

A B C D₁ MSB LSB

	D ₃	D ₂	D ₁	D ₀	Y ₁	Y ₀	Y ₁	Y ₀
0	0	0	0	0	X	X	0	0
1	0	0	0	1	0	0	X	X
2	0	0	1	0	0	1	0	0
3	0	0	1	1	0	1	X ₁	0
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	0	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	0
10	1	0	1	0	1	1	0	0
11	1	0	1	1	1	1	0	0
12	1	1	0	0	1	1	0	0
13	1	1	0	1	1	1	0	0
14	1	1	1	0	1	1	0	0
15	1	1	1	1	1	1	0	0



for Y₁

AB	CD	$\bar{A}\bar{B}$	$\bar{A}D$	$\bar{C}D$	$C\bar{D}$	
$\bar{A}\bar{B}$	X	0	0	3	0	G ₂
$\bar{A}B$	1	4	1	5	1	6
AB	1	2	1	3	1	4
A \bar{B}	1	8	1	9	1	10

for Y₀

AB	CD	$\bar{A}\bar{B}$	$\bar{C}D$	$C\bar{D}$	
$\bar{A}\bar{B}$	X	0	1	3	2
$\bar{A}B$	0	4	0	7	0
AB	1	2	1	10	14
A \bar{B}	1	8	1	11	10

$$G_{K1} = A, G_2 = \bar{B}C$$

$$Y_1 = D_3 + D_2$$

$$G_1 = A, G_2 = \bar{B}C$$

$$Y_0 = D_3 + \bar{D}_2 D_1$$

$$2^m = n$$

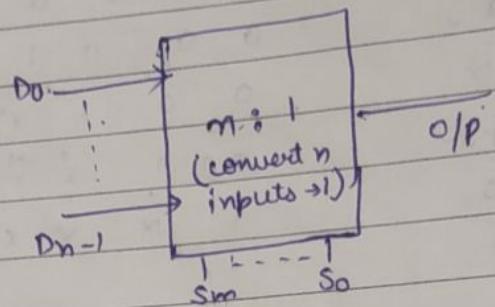
~~1:b:1~~

4.16

2 - Multiplexers and Demultiplexers 3

? Multiplexers :-

to control OLP data or to tell command which data line to transfer - Select line

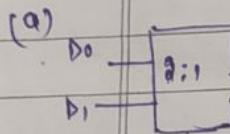


$$g^m = m$$

no of
impost

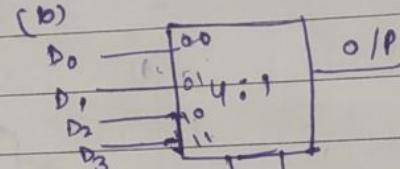
Types of Multiplexers:

- (a) 2 : 1
- (b) 4 : 1
- (c) 8 : 1
- (d) 16 : 1



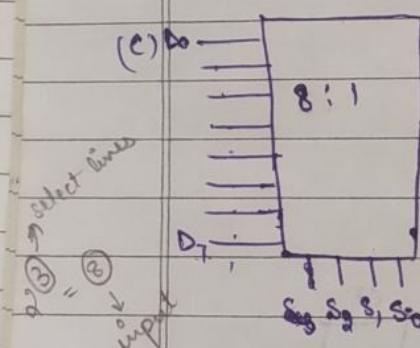
$$S_0 = 0 \quad O/P = D_0$$

$$S_1 = 1 \quad O/P = D,$$

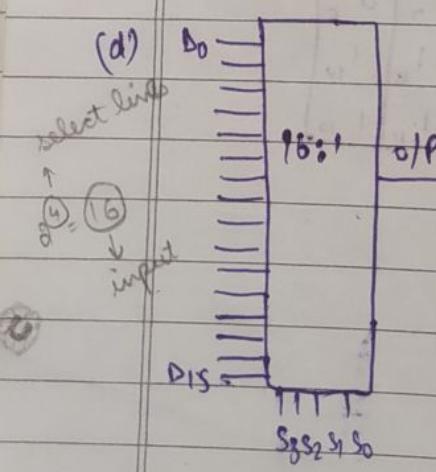
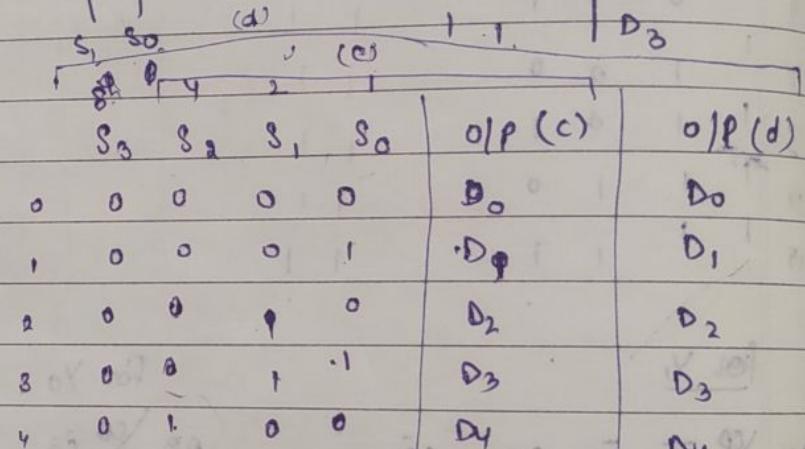


$$= \frac{D_D}{D_1}$$

S_1	S_0	D_1/D_0
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



select lines



Select line
④ = ⑯

S	0	1	0	1	D5
G	0	1	1	0	D6
B	0	1	1	1	D7
D	1	0	0	0	D8
F	1	0	0	1	D9
A	1	0	1	0	D10
C	1	0	1	1	D11
E	1	1	0	0	D12
H	1	1	0	1	D13
J	1	1	1	0	D14
K	1	1	1	1	A5

74150

16:1(MUX)

DM74150N

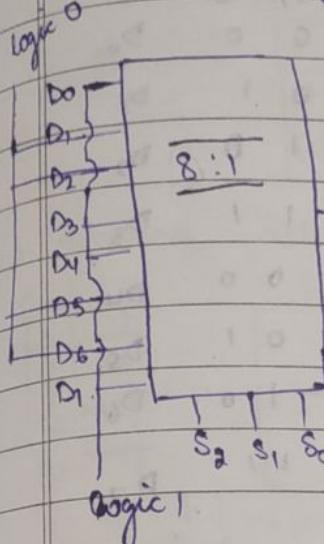
Page No. 31

Date: 31 08 18

Implementation of Multiplexers :-

Q. Implement using Multiplexers.

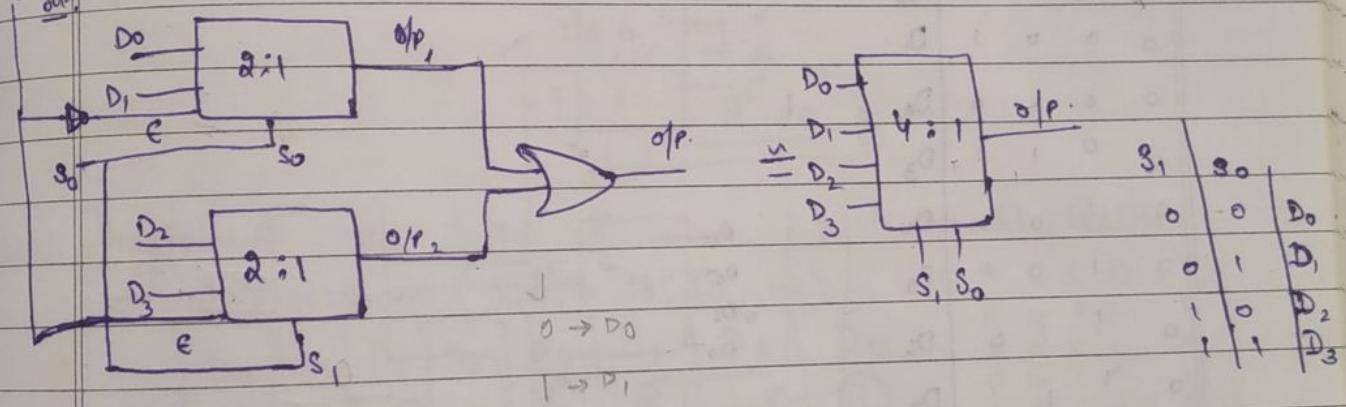
S. m (0, 3, 4, 7)



S_2	S_1	S_0	Sum	Carry	o/p.
✓ 0	0	0	0	0	0
✓ 1	0	1	1	0	1
✓ 2	0	0	0	1	0
✓ 3	0	1	1	0	1
✓ 4	1	0	0	1	0
✓ 5	1	0	1	0	1
✓ 6	1	1	0	0	1
✓ 7	1	1	1	1	1

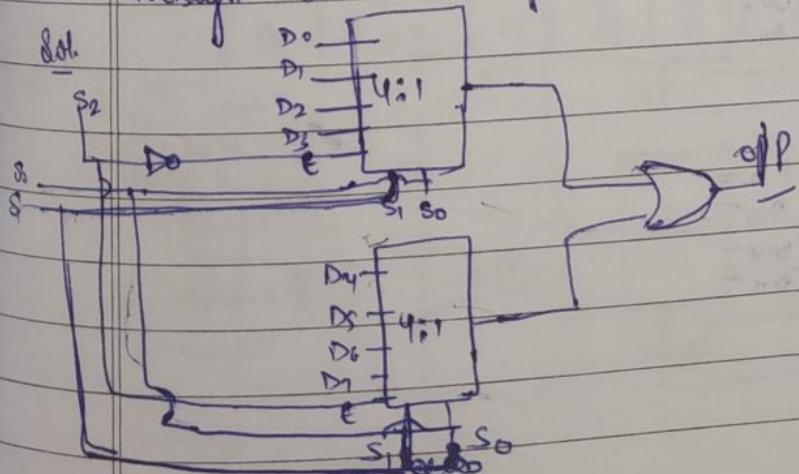
⇒ MULTIPLEXER - TREE

Ques. Implement 4:1 multiplexer using ^{two} 2:1 multiplexer



Sept

Design 8:1 multiplexer using two 4:1 multiplexers



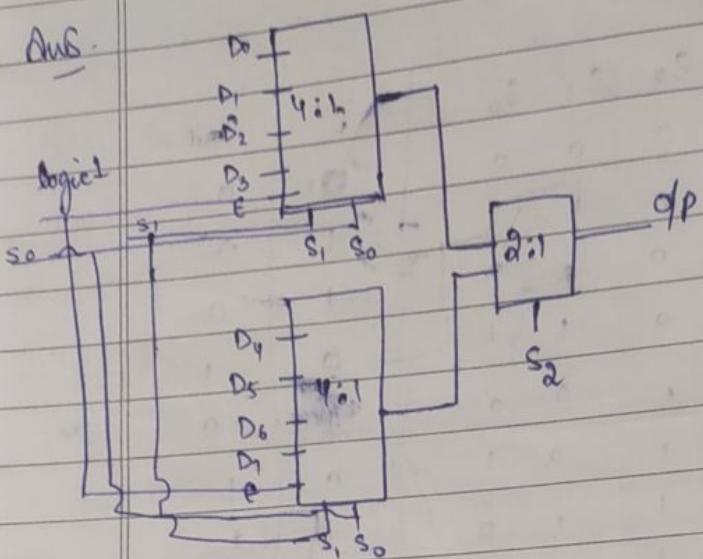
S_2	S_1	S_0	D_0
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

4/Sept
Ques.

Ques.

Using only multiplexers i.e. without any basic gates
 derive 8:1 multiplexer.

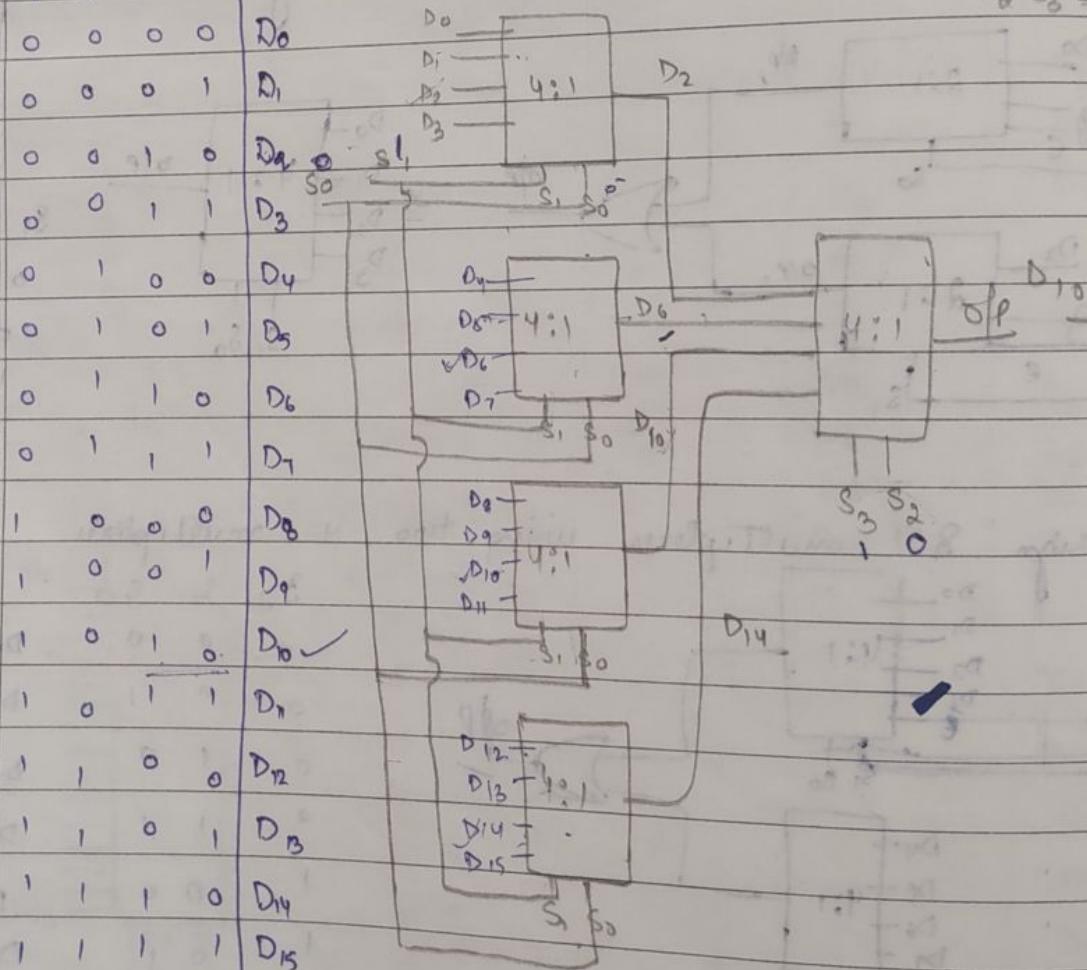
Ans.



S_2	S_1	S_0	D_P
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Ques.

Draw / Implement the 16:1 multiplexer using only 4:1 multiplexers.

 $S_3 \ S_2 \ S_1 \ S_0$ $S_2 \ S_3 \Rightarrow 10$ 

If both are included $\rightarrow 1$
 If none is included $\rightarrow 0$
 Other corresponding $\rightarrow \square$

left MSB.

Page No. 33

Date:

Ques:
Ans:

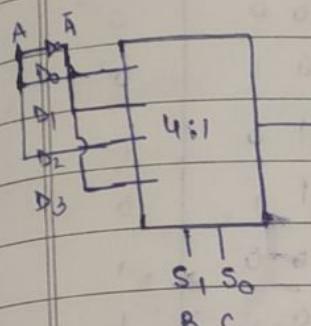
Implement the logic function using 4:1 multiplexer
 $y = \sum m(1, 3, 4, 6)$

- Sol:
 1. Apply two variables B and C to the select lines
 2. Write a design table for leftover Most significant

A.

	D ₀	D ₁	D ₂	D ₃
0 (\bar{A})	0	1	2	3
(1) A	4	5	6	7

3. Encircle all the given terms in table.



	D ₀	D ₁	D ₂	D ₃
(0) \bar{A}	0	1	2	3
(1) A	4	5	6	7
A	8	9	10	11
B, C	0	1	0	1
O/P	0	1	0	1
A B C Y	0 0 0 0	0 0 1 1	0 1 0 1	0 1 1 0
0 0 1 1	1 0 0 0	1 0 1 1	1 1 0 0	1 1 1 1
0 1 0 0	0 0 0 0	0 0 1 1	0 1 0 1	0 1 1 0
0 1 1 1	0 0 0 1	0 0 1 0	0 1 0 0	0 1 1 1
0 0 0 1	0 0 0 0	0 0 1 0	0 1 0 1	0 1 1 0
0 0 1 0	0 0 0 0	0 0 1 1	0 1 0 0	0 1 1 1
0 1 0 1	0 0 0 1	0 0 1 0	0 1 0 1	0 1 1 0
0 1 1 0	0 0 1 0	0 0 1 1	0 1 1 0	0 1 1 1
0 1 1 1	0 0 1 1	0 0 0 1	0 1 1 1	0 1 1 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

- Ques: Implement the foll. function 8:1 multiplexer

$$y = \sum m(2, 4, 5, 7, 10, 14)$$

\bar{A}	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	1	2	3	4	5	6	7	14
1	8	9	10	11	12	13	15	
0	0	1	0	\bar{A}	\bar{A}	A	\bar{A}	

A B C D Y

0 0 0 0 0

0 0 0 1 0

0 0 1 0 1

0 0 1 1 0

0 1 0 0 1

0 1 0 1 1

0 1 1 0 0

0 1 1 1 1

1 0 0 0 0

1 0 0 1 0

1 0 1 0 0

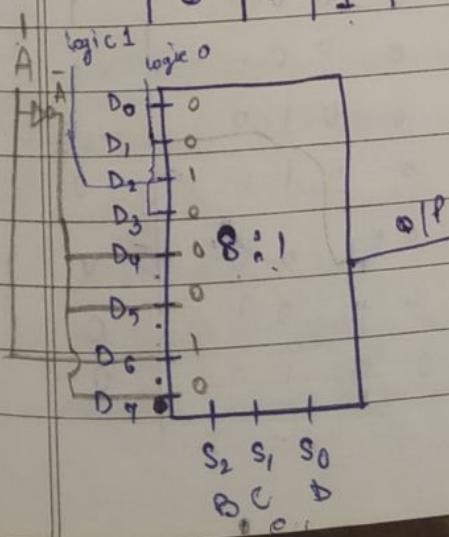
1 0 1 1 0

1 1 0 0 0

1 1 0 1 0

1 1 1 0 1

1 1 1 1 0



(2) Minimization of logic fn. OR, AND, NOT, NOR, NAND, EX-OR, EX-NOR, Basic theorem of Boolean Algebra, SOP & POS, Canonical form, Karnaugh Map, Q-M Map.

(3) (C) Combinational Circuits - Intro, CC Design, Encoders, decoders, Adders, Subtractors & Code Converters, Parity checker, Seven segment display, Mag. comparators, MUX, DEMUX, Implementation of C.C's using MUX

(SC) Sequential Circuits :- Intro, flip flops, clocked flip flops, SR, JK, D, T and edge triggered flip flop, Excitation tables of F.t., Shift Registers, Type of Shift Reg.; Counter - types, design with state eq. & state diag.

(4) D/A & A/D converters - Intro, weighted D/A converter, Binary ladder D/A converter, steady state accuracy test, D/A accuracy & resolution, I/A/D converter, counter type A/D converter Successive approx. A/D converter, Single & dual slope A/D converter, A/D accuracy & resolution

Logic Families :- RTL, DCTL, DTL, TTL, ECL, CMOS & its various types, Comp. of logic families.

Combinational logic switching circuits are those whose output levels at any instant of time are depended only on the levels present at the inputs at that time. Any prior IP level conditions have no effect on the present output because they have no memory. A circuit consisting of only logic gates is a combinational circuit.

Maxterms are known as False minterms.
 PI obtained by using the maxterms - False PI
 The FPI which contains atleast one 0 which cannot be covered
 by any other FPI is called Essential FPI (EFP I)

- A Non-PI is a minterm which does not have any adjacent minterms i.e. can form a part of a bigger Eq.
- A Non-EPI is a selective PI. It is neither essential nor redundant. It may or may not appear in the minimal expression.

Limitations of K-Map

- This method is convenient as long as the no. of variables doesn't exceed 6. As no. of variables exceed it is impossible difficult to make judgements about the combination form.
- It is a manual technique and simplification process is heavily dependent on the human abilities. It is
- It cannot be programmed.

Syllabus

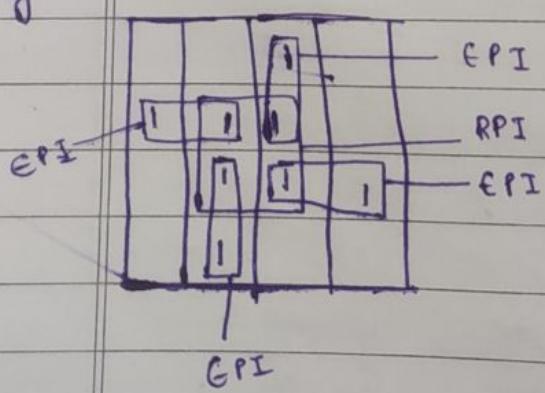
- ① Number System & Binary Code :-
 Intro ; Binary, Octal & Hexadecimal No. system Conversion,
 Addition & subtraction ; Signed & Unsigned no., Binary
 Sub. using 1's & 2's complement, ASCII code, Excess 3
 Code, Grey code, BCD code & BCD addition.

K-Map

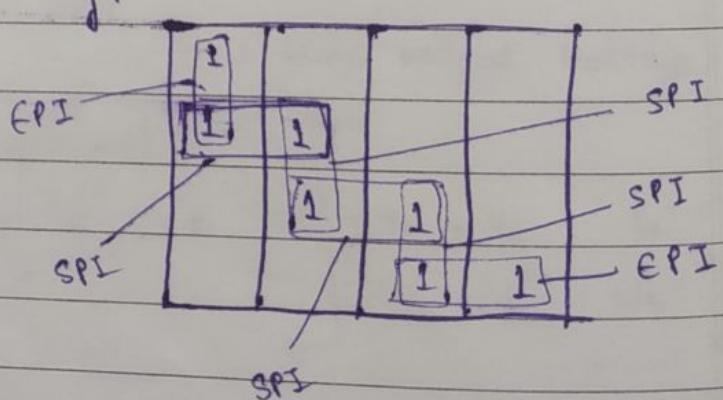
Prime Implicants, Essential P.I, Redundant P.I, Selective P.I

- Each sq. or rect. made up of the bunch of adjacent minterms is called a subcube.
- Each of these subcubes is called a prime implicant (PI).
- The PI which contains atleast one 1 which cannot be covered by any other prime implicant is called an essential prime implicant (EPI).
- The PI whose each 1 is covered by one EPI is called a redundant prime implicant (RPI).
- A PI which is neither a EPI nor a RPI is called a Selective Prime Implicant (SPI).

eg:-



eg.



$$\text{No. of step} = \frac{V_{in}}{\text{Resolution}}$$

A-D Convertors.

2-Nov

Types :-

ii) Parallel comparator ADC

$$2^{2^n} - 1 = \text{No. of comp. no.}$$

- ج

Now. If ddd. another data is 011

$$V_2 V_1 V_0 = 011$$

we have logic 0 = 0V

logic 1 = +7V

$$V_A = \frac{V_0/R_0 + V_1/(R_0/2) + V_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)}$$

$$= \frac{0/R_0 + 1/(R_0/2) + 0}{1/R_0 + 2/R_0 + 4/R_0}$$

$$= \frac{0/R_0 + 1^4/R_0}{7/R_0} = \frac{7+14}{7} = \frac{21}{7} = 3 \text{ Volts}$$

So analog O/P is analog +3V

Drawbacks :- 1. Each resistor in the network has different values.

2. More resistors are used thus much greater currents are needed.

We R-2R ladder.

Parameters

$$\rightarrow \text{Resolution} = \text{step size} = \frac{V_R}{2^n} \leftarrow \text{bit}$$

$$\rightarrow \text{Resistance Resolution} = \frac{\text{step size} \times 100}{f_{SO}}$$

$$f_{SO} \Rightarrow \text{step size} \times (2^N - 1)$$

$$\Rightarrow V_R = \text{Weight of LSB}$$

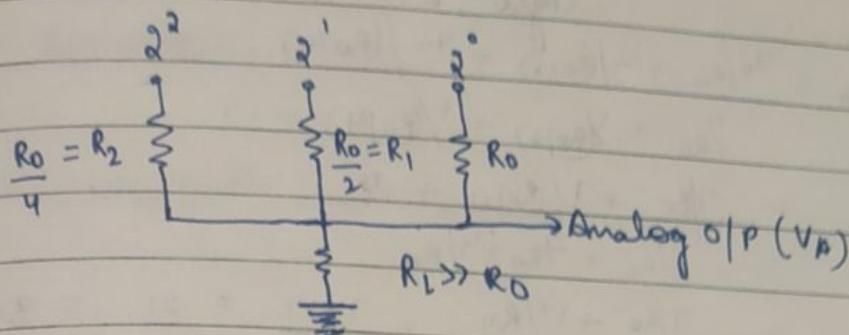
full scale output voltage

$$\frac{\text{Stepsize}}{(2^n - 1)} \times \frac{100}{\text{Step size}} = \frac{100}{2^N - 1}$$

$$\text{eg. } N = 2 \\ \frac{100}{2^2 - 1} = \frac{100}{3} = 33.3$$

$$V_R = \frac{V_R}{2^n} \quad \text{let } n=3 \\ V_R = \frac{V_R}{2^3} \\ = \frac{7VA}{8}$$

2. These three voltages represent the digital bits of they must be summed together to form the analog voltage.



This circuit can be solved using Millman theorem.

Acc. to Millman theorem

$$V = \frac{V_0/R_0 + V_1/(R_0/2) + V_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)}$$

$V = IR$ here All resistances are in Parallel

$$\therefore V = \frac{I}{R}$$

As in general $I = V/R$

\therefore Req. eq. of Millman's Theorem.

Eg. If digital I/P is 001 i.e. $V_2 V_1 V_0 = 001$

Let us assume that logic 0 = 0 V

Logic 1 = +7 V

Acc. to Millman's Theorem

$$V_A = \frac{V_0/R_0 + V_1/(R_0/2) + V_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)}$$

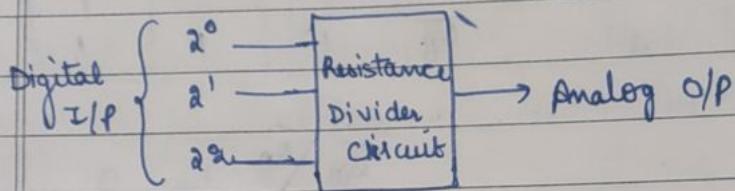
$$= \frac{0/R_0 + 0 + 0}{1/R_0 + 2/R_0 + 4/R_0} = \frac{0}{7/R_0} = 0 V$$

So the analog o/p is analog +1 V.

Comparison of logic families

Propagation delay time (ns)	Power dissipation per gate (mw)	Noise Margin (%)	Fan in	Fan out	Cost
TTL	10	422 0.4	8	10	low
ECL	50	0.25	5	10	High
MOS	0.1	1.5	1	10	low
CMOS	0.01	5	10	50	low
III	0.1	0.34	5	8	Very low

Binary Weighted Register D-A converter



Digital I/P	Analog O/P
000	0V
001	+1V
010	+2V
011	+3V
100	+4V
101	+5V
110	+6V
111	+7V

Resistive divider ckt do two things to change digital input into an equivalent analog o/p.

1. The \$2^0\$ bit must be changed to +1 volts &
2. \$2^1\$ bit must be changed to +2V &
3. \$2^2\$ bit must be changed to +4V ..

for Test - 3.

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Date: 29/10/18

Counters & design logic families, there different logic families parameters & comparison

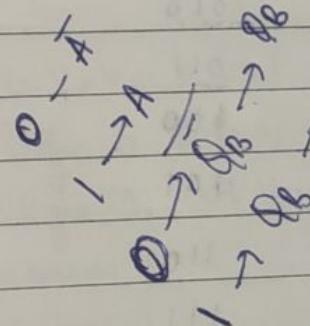
S

		Q _B Q̄ _A		Q̄ _B Q _A		S	
Q _B Q̄ _A		0 0	1 1	0 0	1 1	0 0	1 1
0	0	1	1	1	1	1	1
0	1	1	0	1	0	1	0
1	0	0	1	1	0	0	1
1	1	0	0	0	1	1	1

on 2-bit store

Q _B	Q̄ _B	Q _A	Q̄ _A	S
0	1	0	1	X
1	0	1	0	1
0	1	1	0	1
1	1	0	1	1

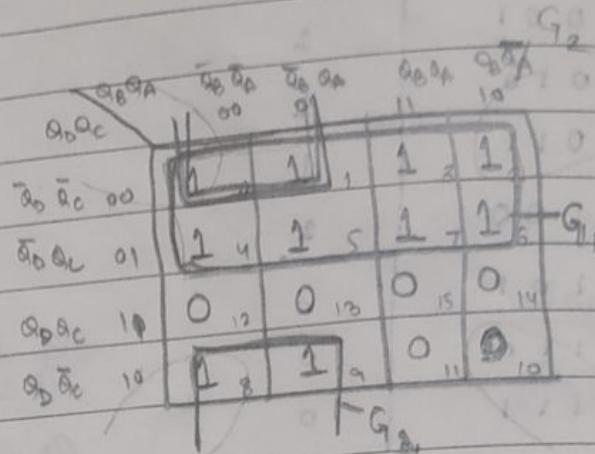
Q _B	Q̄ _B	Q _A	Q̄ _A	S
0	1	0	1	0
1	0	1	0	1
0	1	1	0	1
1	1	0	1	1



HW Make Mode -10 counter. (Decade Counter)

bitside

Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	1
1	0	0	1	1
2	0	0	1	2
3	0	0	1	1
4	0	1	0	1
5	0	1	0	1
6	0	1	0	1
7	0	1	1	1
8	1	0	0	1
9	1	0	0	1
10	1	0	1	0
11	1	0	1	0
12	1	1	0	0
13	1	1	0	0
14	1	1	0	0
15	1	1	1	0

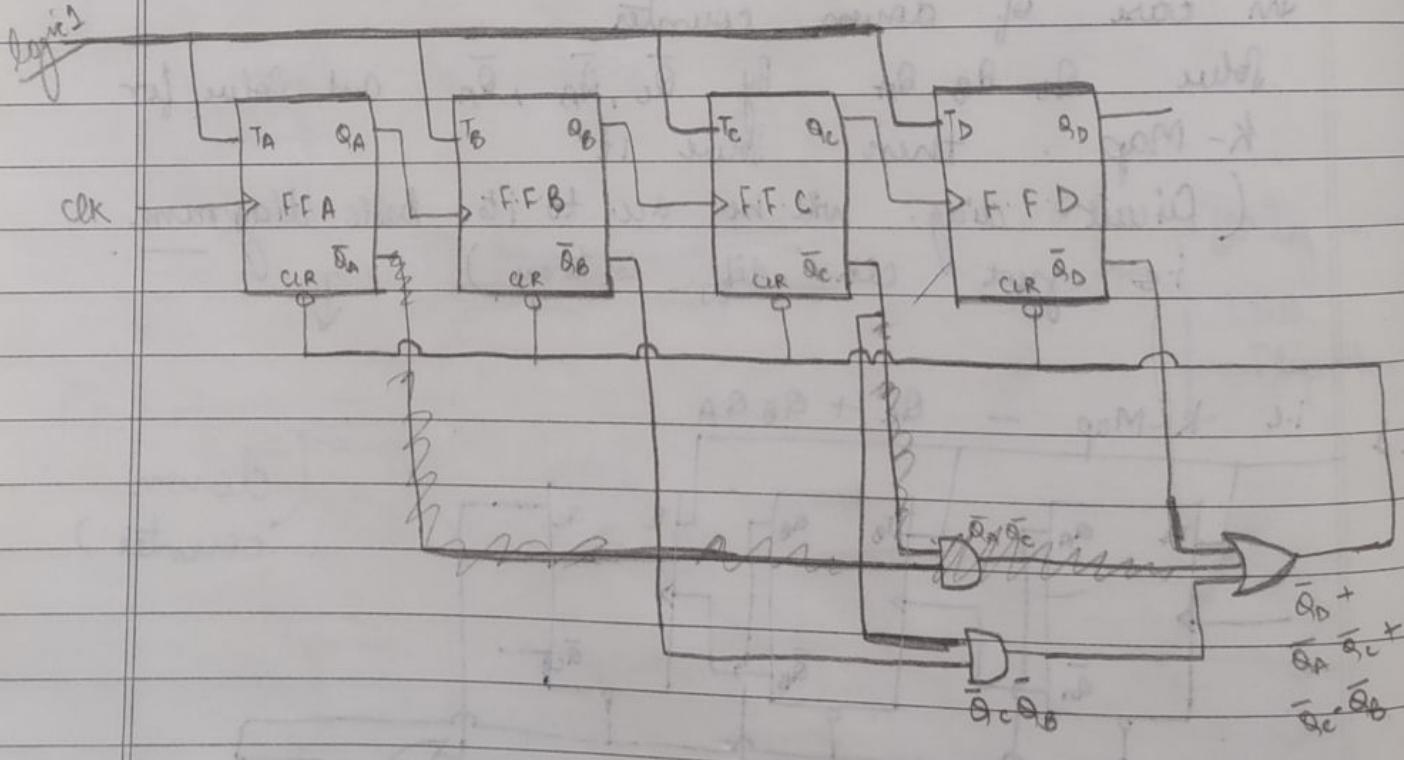


$$G_1 := \bar{Q}_D$$

$$G_2 := \bar{Q}_C * \bar{Q}_A$$

$$G_2 := \bar{Q}_C * \bar{Q}_B$$

$$Y = \bar{Q}_D + \bar{Q}_C * \bar{Q}_A + \bar{Q}_C * \bar{Q}_B$$



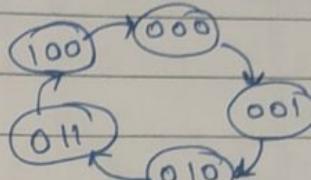
Asynchronous Mode 5

	$Q_C Q_B Q_A$	y (Bubble)
0	0 0 0	1
1	0 0 1	1
2	0 1 0	1
3	0 1 1	1
4	1 0 0	1
5	1 0 1	0
6	1 1 0	0
7	1 1 1	0

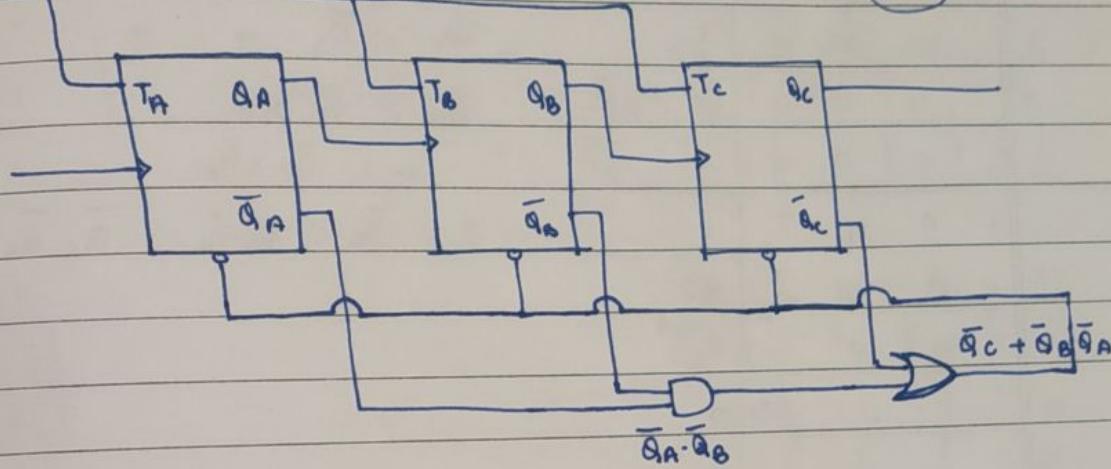
\bar{Q}_C	$\bar{Q}_B \bar{Q}_A$	00	01	11	10
0	1	1	1	1	1
1	1	1	0	0	0

$$\bar{Q}_C + \bar{Q}_B \bar{Q}_A$$

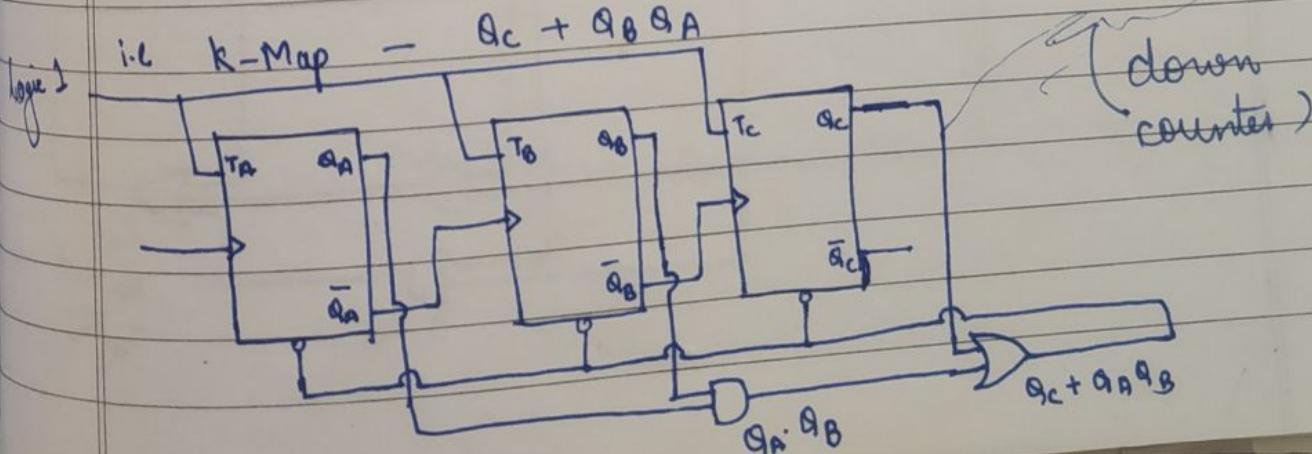
State diagram



Logic 2.



In case of down counter

Solve Q_C , Q_B , Q_A by \bar{Q}_C , \bar{Q}_B , \bar{Q}_A and solve for K-Map. then solve it.(Circuit diag. will be acc. to its basic diagram.
i.e just CLK diff. is there). i.e ↓

Mode

eg. in a bit.

in 3 bit

2 (no. of flip-flops)

 $2^2 = 4$ Mode (0-3) $2^3 = 8$ Mode (0-7) $2^4 = 16$ Mode (0-15)
$$\begin{matrix} & 2 & 2 & 2 \\ 2 & 2 & 2 & 2 \\ 8 & 4 & 2 & 1 \end{matrix}$$

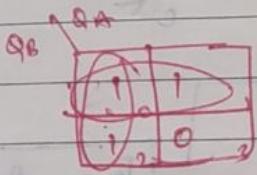
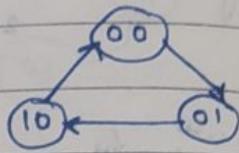
Ques. Design a mode 3 - asynchronous 2 bit ripple counter.

using Bubble preferred.

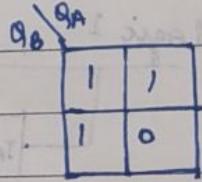
state diagram

	Q _B	Q _A	Y	Y
0	0	0	0	1
1	0	1	0	1
2	1	0	0	1
3	1	1	1	0

$$= Q_A \cdot Q_B \cdot (\text{AND})$$



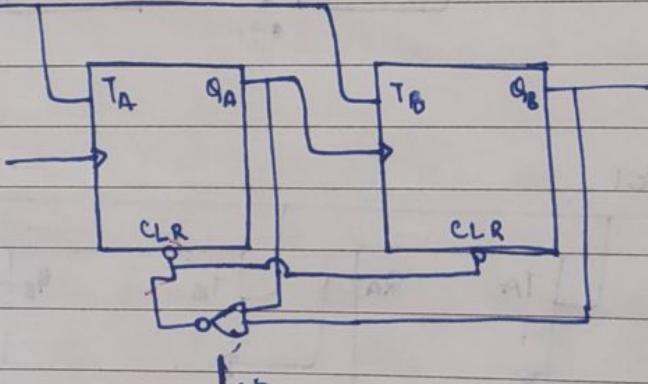
$$Q_A + \bar{Q}_B$$



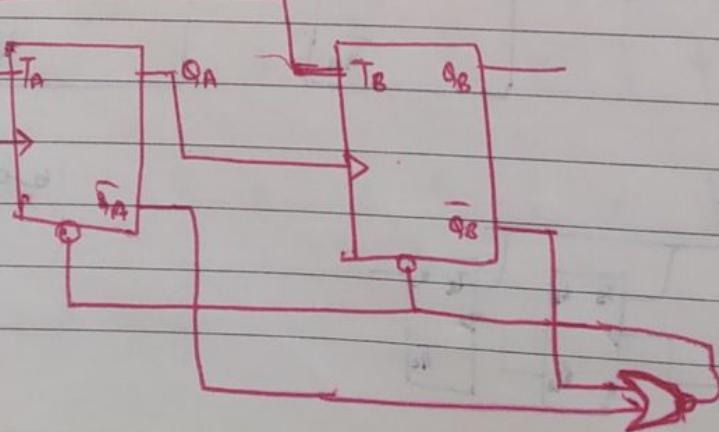
$$= \bar{Q}_A + \bar{Q}_B \cdot (\text{NAND})$$

give to CLR

bubble
reverse
the
result
input

Logic 1

get by use
LSB
Flip flop

Logic

$$Q_B \quad Q_A = 00$$

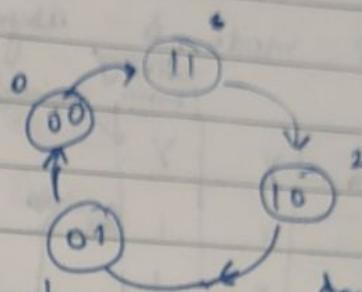
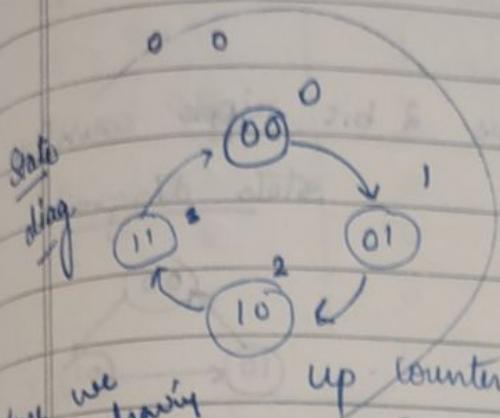
0 0

0 1

1 0

1 1

0 0



23 - Oct - 2012

down counter.

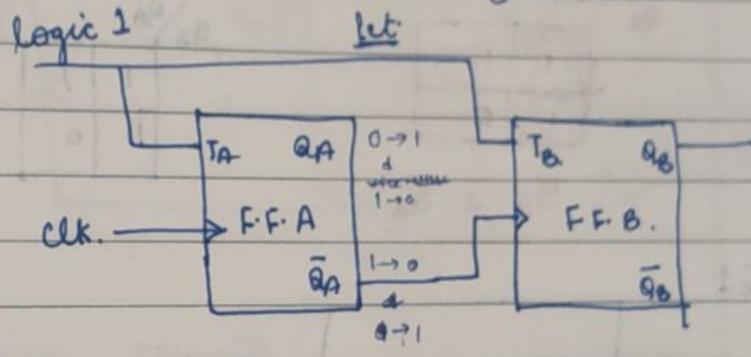
$$Q_B \quad Q_A$$

1 1

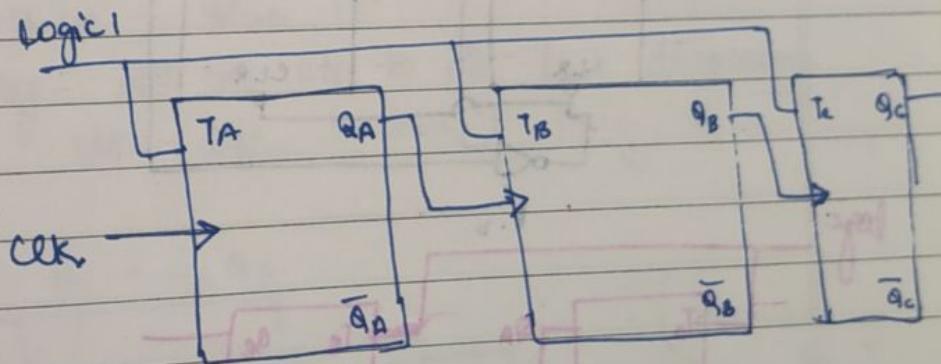
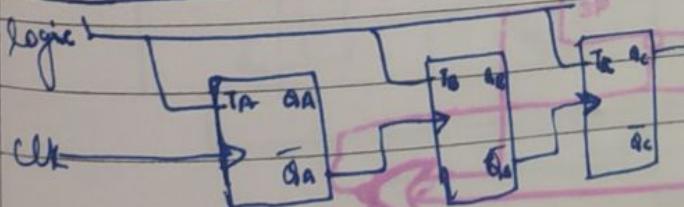
1 0

0 1

0 0

For 3-bit.

upcounter.

down counter

16/01/18

Counters: The digital circuit used for counting pulses is called Counter. It is sequential circuit and made up of group of flip-flops. It is the widest application of flip-flops. Mostly the counters are used for counting pulses but with some modification they are often used to measure frequency or time period.

Types of Counter:

- Basically, 2 types of counter

1. Asynchronous Counter

— don't provide CLK together, need work sequentially

2. Synchronous Counter

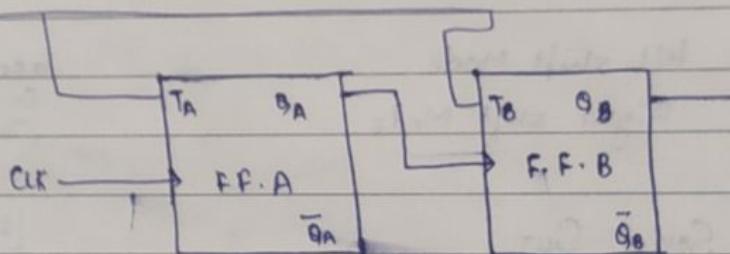
— provide CLK equally at a same time

↳ Ring Counter ↳ Johnson Counter.

- Asynchronous Counter (Ripple Counter)

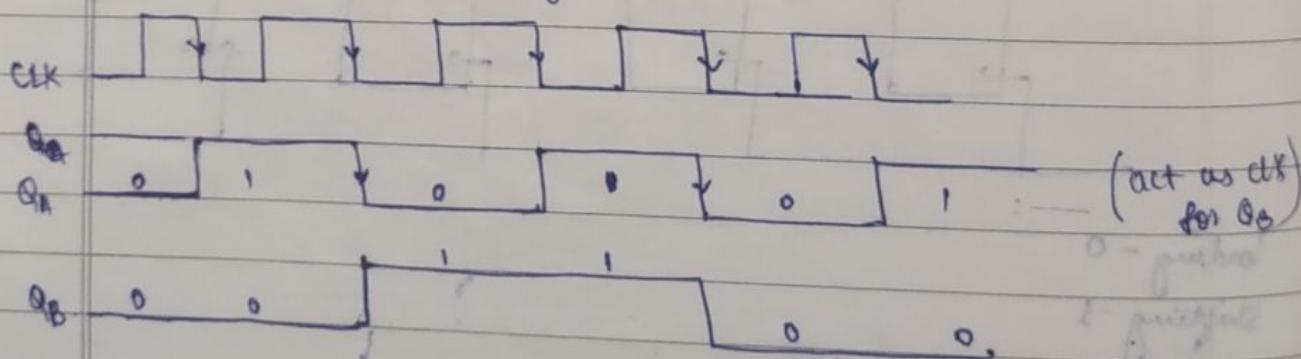
8-Bit Asynchronous Counter (Ripple Counter)

logic 1



Let initially both the F.F are at rest state. Set the outputs Q_B , Q_A be 0,0 and also assume that both the F.F work on -ve edge triggering.

On the 1st -ve edge



~~for Test 3 :-~~

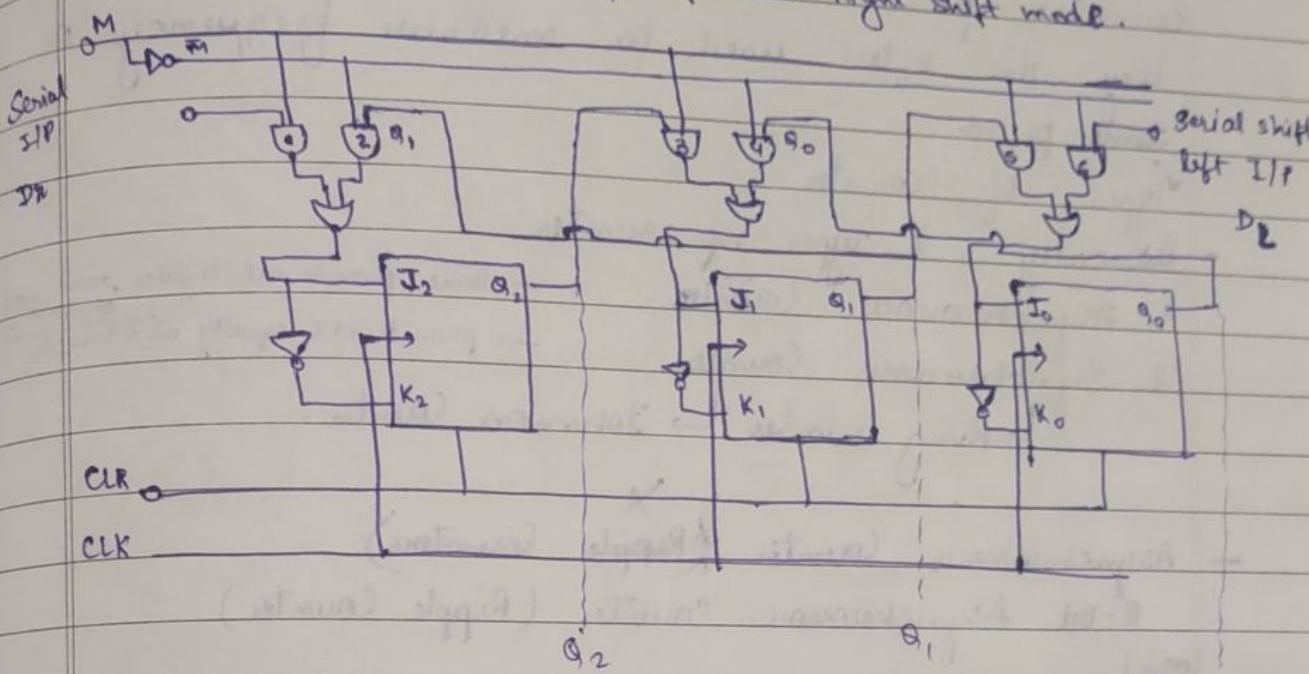
Counters

Part 4. A-D, D-A Convector ; logic families ;

10-oct-2018.

Serial In Parallel Out (Bi-directional shift register)

Left shift mode Right shift mode



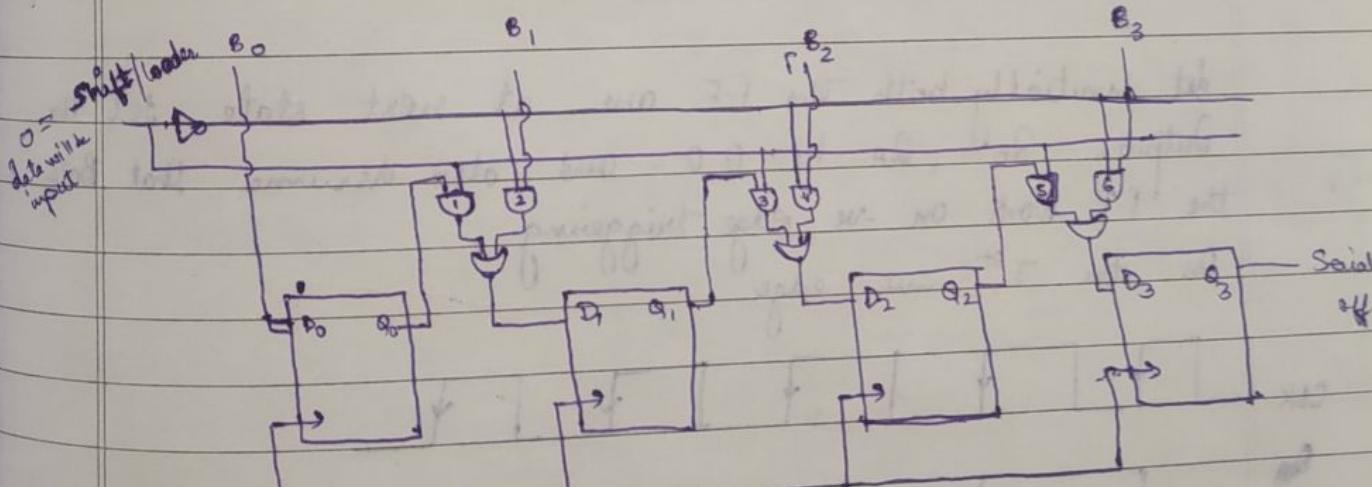
When $M = 0$ left shift mode

when $M=1$ Right shift Mode.

Take previous value
for determination
(To give)

Parallel In Serial Out

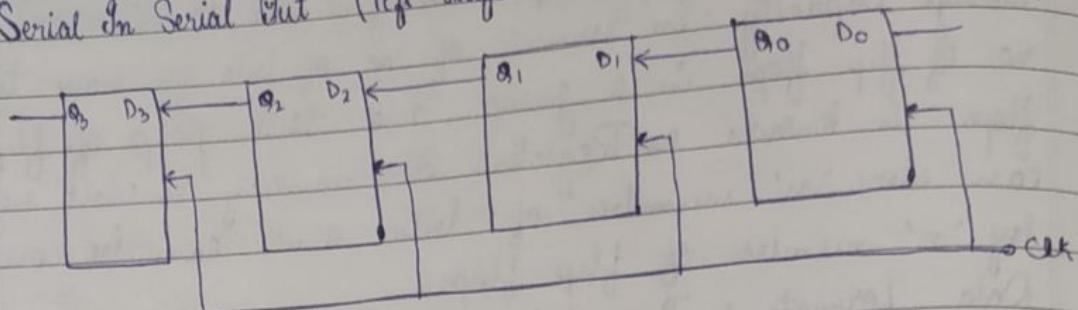
12-oct-2018



Leading - 0

Shifting - I

Serial In Serial Out (left shift mode)



Before applying a clk set the o/p of Q_3, Q_2, Q_1, Q_0 be 0000

Firstly apply MSB to it

So at the first clk $Q_3 Q_2 Q_1 Q_0 \rightarrow 0001$

1st CLK

2nd CLK

3rd CLK

4th CLK

Q3

CLK. $Q_3 Q_2 Q_1 Q_0$.

Ist clk. x 0 0 0.0

IInd clk. ↓ 0 0 1.0

IIIrd clk. ↓ 0 1 0.1

IVth clk. ↓ 1.0 1.1

clk.

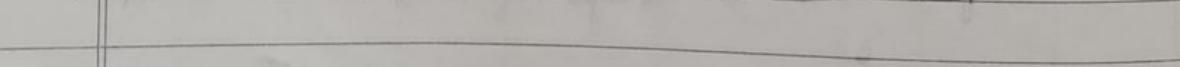
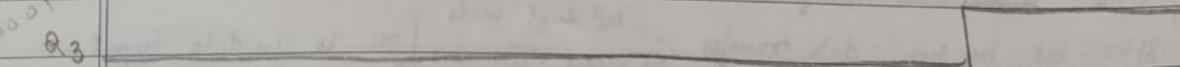
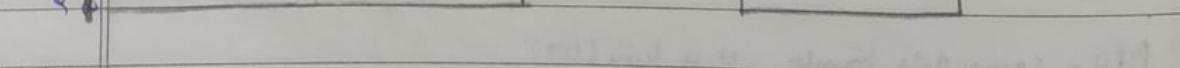
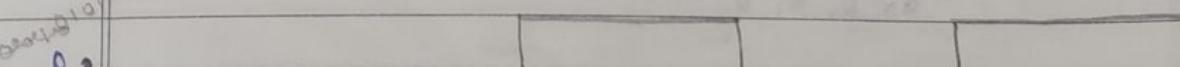
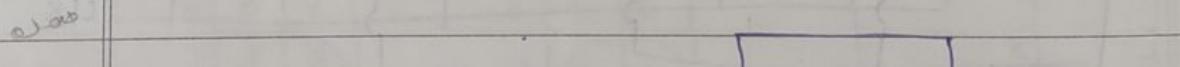
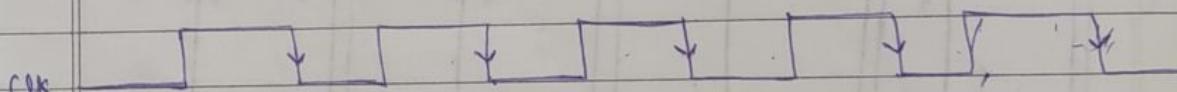
x

↓

↓

↓

↓



0 = ~~gnd~~
Data will be
input

load
shift

Parity Encoder

In syllabus.

Page No. _____

Date: 5 10 18

Registers :-

flip flop can store 1 bit of memory and to increase the storage capacity in terms of no. of bits we have to use no. of flip-flops in a group and this group of flip-flops is known as Register. So, namely 'n' bit register can store 'n' numbers of bits and can be constructed by 'n' number of flip-flops.

Data formats :- The data can be loaded serially or in parallel (all the bits at a time)

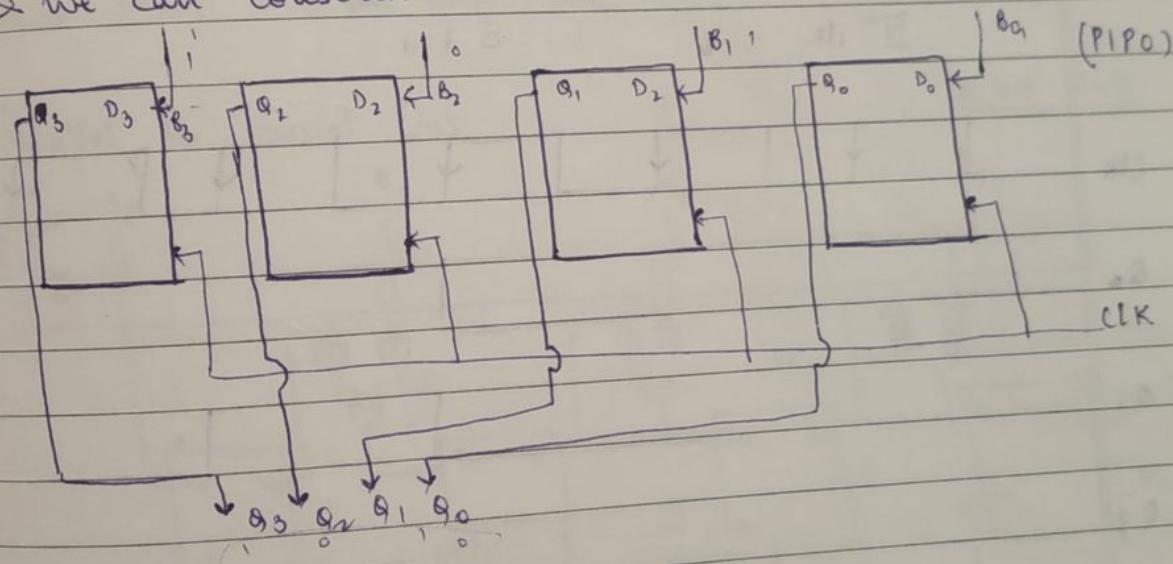
Classification :- Classified on the basis of mode of operation

1. Serial In and Serial Out (SISO)
2. Serial In and Parallel Out (SIPO)
3. Parallel In and Serial Out (PISO)
4. Parallel In and Parallel Out (PIPO)

Buffer Register :- (a) 4 Bit BR :-

'D'

simplest type of register & constructed by using 4 flip flops & we can construct 'n' Bit BR.



- PIPo - same data transfer at a time (WR)
- SISO - bit by bit data transfer
 - left shift mode acc to the data input.
 - Right shift mode

- Convert SR flip flop to D flip flop

D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
1	0	1	1	0
0	1	0	0	1
1	1	1	X	0

for S

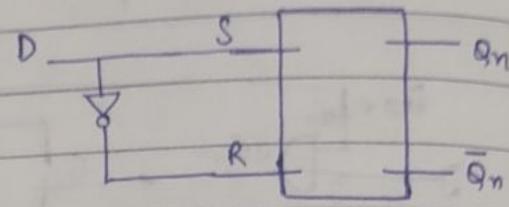
for R

D	Q_n	0	1
0	0	0	
1	1	X	

= 0

D	Q_n	0	1
0	0	X	1
1	0	0	

= 1



- Convert JK flip flop to T flip flop.

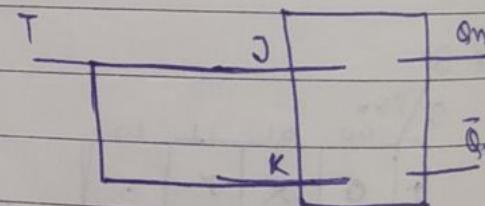
T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
1	0	1	1	X
1	1	0	X	1
0	1	1	X	0

T	Q_n	0	1
0	0	X	
1	1	X	

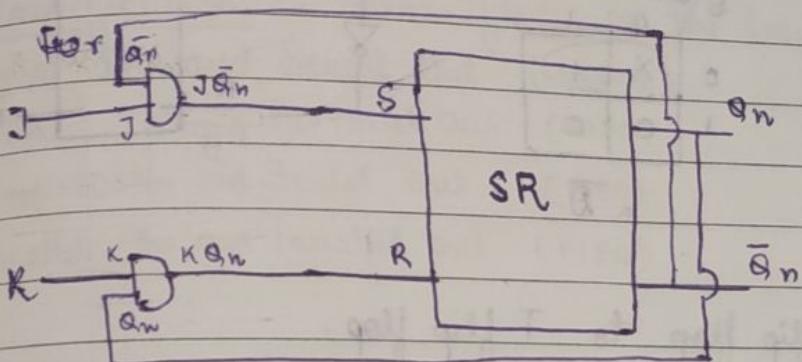
T

T	Q_n	0	1
0	0	X	0
1	0	X	1

T



J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	x
0	1	0	0	0	x
1	0	0	1	1	0
1	1	0	1	1	0
0	1	1	0	0	1
1	1	1	0	0	1
0	0	1	1	x	0
1	0	1	1	x	0



- Convert JK flip flop to SR flip flop.

JK Q_n Q_{n+1} JK

0x 0 0 0x

10 0 1 1x

01 1 0 x1

x0 1 1 xo

SR Q_n Q_{n+1} JK

00 0 0 0x

01 0 0 x0

10 0 1 1x

x* 0 1 1x

01 1 0 x1

x* 1 0 x1

00 1 1 x0

10 1 1 xo

for J

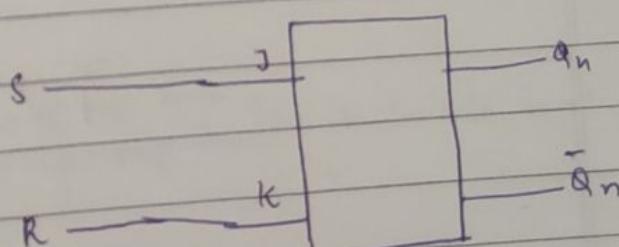
S	R	Q_n	00	01	11	10
0	0	x	x	0		
1	1	x	x	x		

$$= S$$

for K

S	R	Q_n	00	01	11	10
0	x	0	1	x		
1	x	0	x	x		

$$= R$$



- Conversion of J-K-Flip-flop to T-Flip-flop

T	Q_n	Anti	J	K
0	0	0	0	X
1	0	1	1	X
1	1	0	X	1
0	1	1	X	0

for J

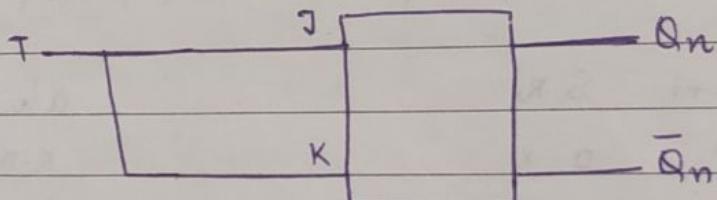
T	Q_n	0	1
0	0	X	
1	(1)	(X)	

$$= T$$

for K

T	Q_n	0	1
0	X	0	
1	(X)	1	

$$= T$$



- Convert SR flip flop to JK flip flop.

J	K	Q_n	Q_{n+1}	S	R
0	X	0	0	0	X
1	X	0	1	1	0
X	1	1	0	0	1
X	0	1	1	X	0

For S

J	Q_n	\bar{Q}_n	\bar{K}_n	K_n	\bar{K}_n	K_n	\bar{K}_n
0	0	X	0	0			
1	(1)	X	0	1			

$$= J \bar{Q}_n$$

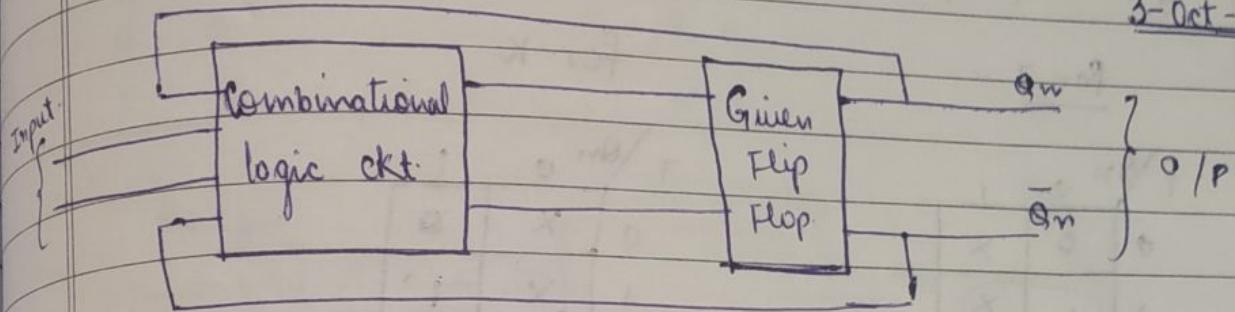
For R

J	\bar{K}_n	K_n	\bar{K}_n	K_n	\bar{K}_n	K_n	\bar{K}_n
0	0	X	0	0			
1	0	0	0	1	(1)	X	0

$$= \bar{S}R + K\bar{Q}_n$$

Q_n	Q_{n+1}	S	R	D	J	K	T
0	0	0	X	0	0	X	0
0	1	1	0	1	1	X	1
1	0	0	1	0	X	1	1
1	1	X	1	1	X	0	0

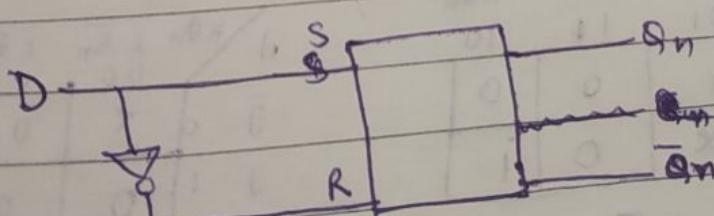
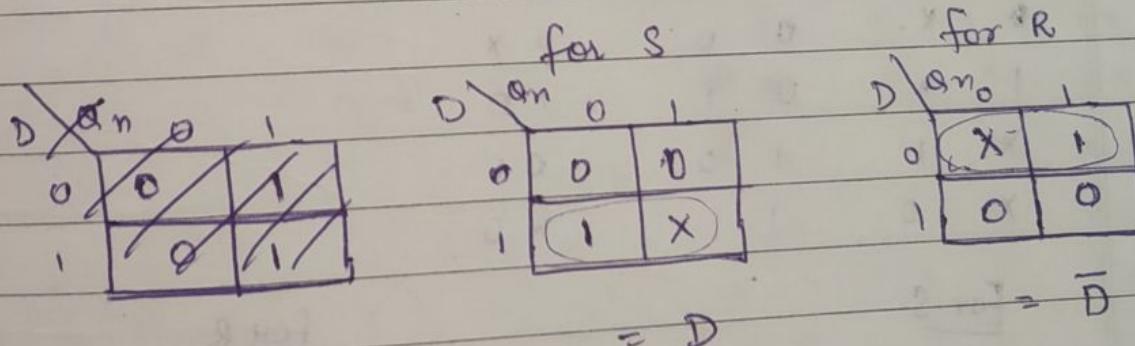
3-Oct-2018



Conversion from S-R flip flop to D-flip flop

D	Q_n	Q_{n+1}	S R
0	0	0	0 X
1	-Q	1	1 0
0	1	0	0 1
1	1	1	X 0

always made
K-Map with Q_n
 $Input 1 + Q_n = Q_{n+1}$
 $Input 2 + Q_n = \bar{Q}_{n+1}$
and so on



Jk flip flop

characteristics

J	K	Q_n	Q_{n+1}
0	0	0	0

No change

J	K	Q_n	Q_{n+1}
0	0	1	1

Reset

J	K	Q_n	Q_{n+1}
0	1	0	0

Reset

J	K	Q_n	Q_{n+1}
0	1	1	0

Set

J	K	Q_n	Q_{n+1}
1	0	0	1

Set

J	K	Q_n	Q_{n+1}
1	0	1	1

Toggle

J	K
0	0

N.C

J	K
0	1

Reset

J	K
1	0

Set

J	K
1	1

Toggle

Take care :- α & β] Toggle

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X

Q_n	Q_{n+1}	J	K
0	1	1	X

Q_n	Q_{n+1}	J	K
1	0	X	1

Q_n	Q_{n+1}	J	K
1	1	X	0

gall gall - 0

T- flip flop.

characteristics

T	Q_n	Q_{n+1}
0	0	0

No change

T	Q_n	Q_{n+1}
0	1	1

Toggle

T	Q_n	Q_{n+1}
1	0	1

Toggle

T	Q_n	Q_{n+1}
1	1	0

Toggle

T	Q_n	Q_{n+1}
0	0	N.C

T	Q_n	Q_{n+1}
0	1	1

T	Q_n	Q_{n+1}
1	0	1

T	Q_n	Q_{n+1}
1	1	1

Excitation Table

Q_n	Q_{n+1}	T
0	0	0

T	Q_n	Q_{n+1}
0	0	0

Q_n	Q_{n+1}	T
0	1	1

T	Q_n	Q_{n+1}
1	1	0

Q_n	Q_{n+1}	T
1	0	1

T	Q_n	Q_{n+1}
0	0	1

Q_n	Q_{n+1}	T
1	1	0

T	Q_n	Q_{n+1}
1	1	1

Characteristics of S-R flip flop.

S	R	Q_n	Q_{n+1}
0	0	0	0
0	D	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	X	X

Previous
Present
 $Q_n, \bar{Q}_n \rightarrow Q_{n+1}, \bar{Q}_{n+1}$
Next

Truth Table

S	R
0	0
0	1
1	0
1	1

Excitation Table :

Present	Next	S	R
Q_n	Q_{n+1}		.
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D - flip flop.

Characteristics

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Truth Table

Present	Next	D	Q_n
0	0	0	0
1	1	1	0

Excitation Table :

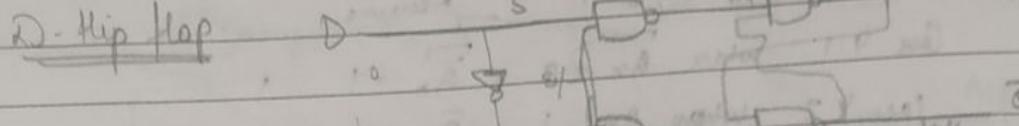
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

oldst wait state

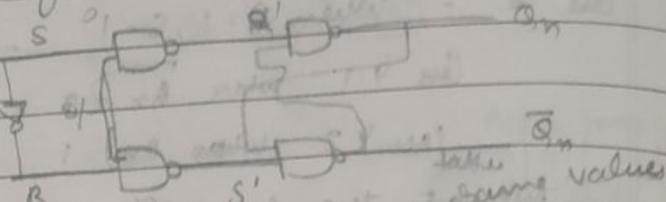
-ve level triggering gate D flip flop

Delay flip flop

D-Hip Hop



D	Q_n	Q_{n+1}
0	Q_n	0
1	Q_n	1



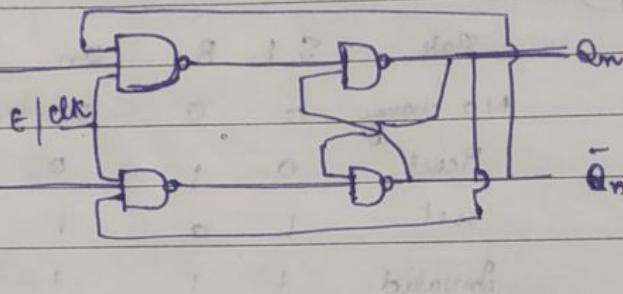
[Race cond - unavoidable]

Race around - discuss later

26/Sept/2018

⇒ JK- flip flop.

Discuss all the cases in detail with diff. diagram.

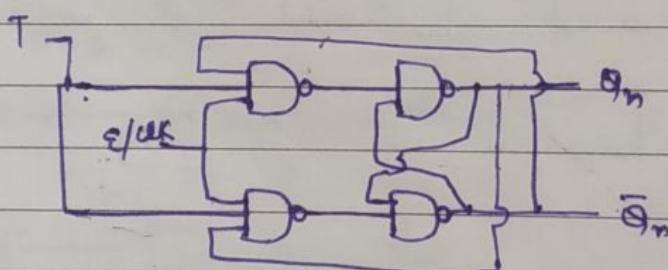


Toggle

G	J	X	Q_{n+1}
0	x	x	N.C(Q_n)
1	0	0	N.C. (Q_n)
1	0	1	Reset $Q_{n+1} = 0$
1	.1	0	Set $Q_{n+1} = 1$
1	1	1	Toggle (Q_n)

(Race-around cond.) $Q_n \rightarrow Q_{n+1}$
 $0 \rightarrow 1$
 $1 \rightarrow 0$

⇒ T- flip - flop.



E	T	Q_{n+1}
0	x	N.C.
1	0	N.C.
1	1	Toggle

28/Sept/2018

Conversion of flip flops.

Case 3 :- When $R=1, S=0$

$$Q_n = 0, \bar{Q}_n = 1$$

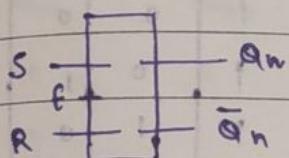
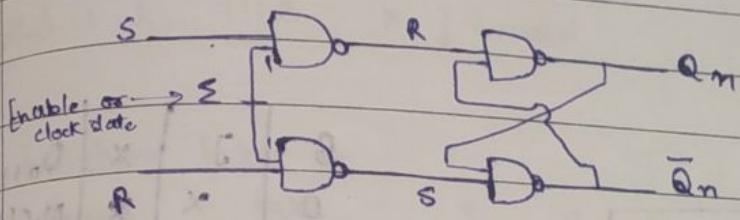
Case 4 :- When $R=1, S=1$ Reset state

Case 4.1 when $Q_n = 0, \bar{Q}_n = 1$ Assume

Case 4.2 when $Q_n = 1, \bar{Q}_n = 0$

We get two Ans which we assume to be No change state

Gated S-R latch



S R Qn bar{Q}n

00 Qn bar{Q}n Qn Qn

01 Qn bar{Q}n 0 1

10 bar{Q}n bar{Q}n 1 0

11 Qn bar{Q}n X X

State S R Qn bar{Q}n

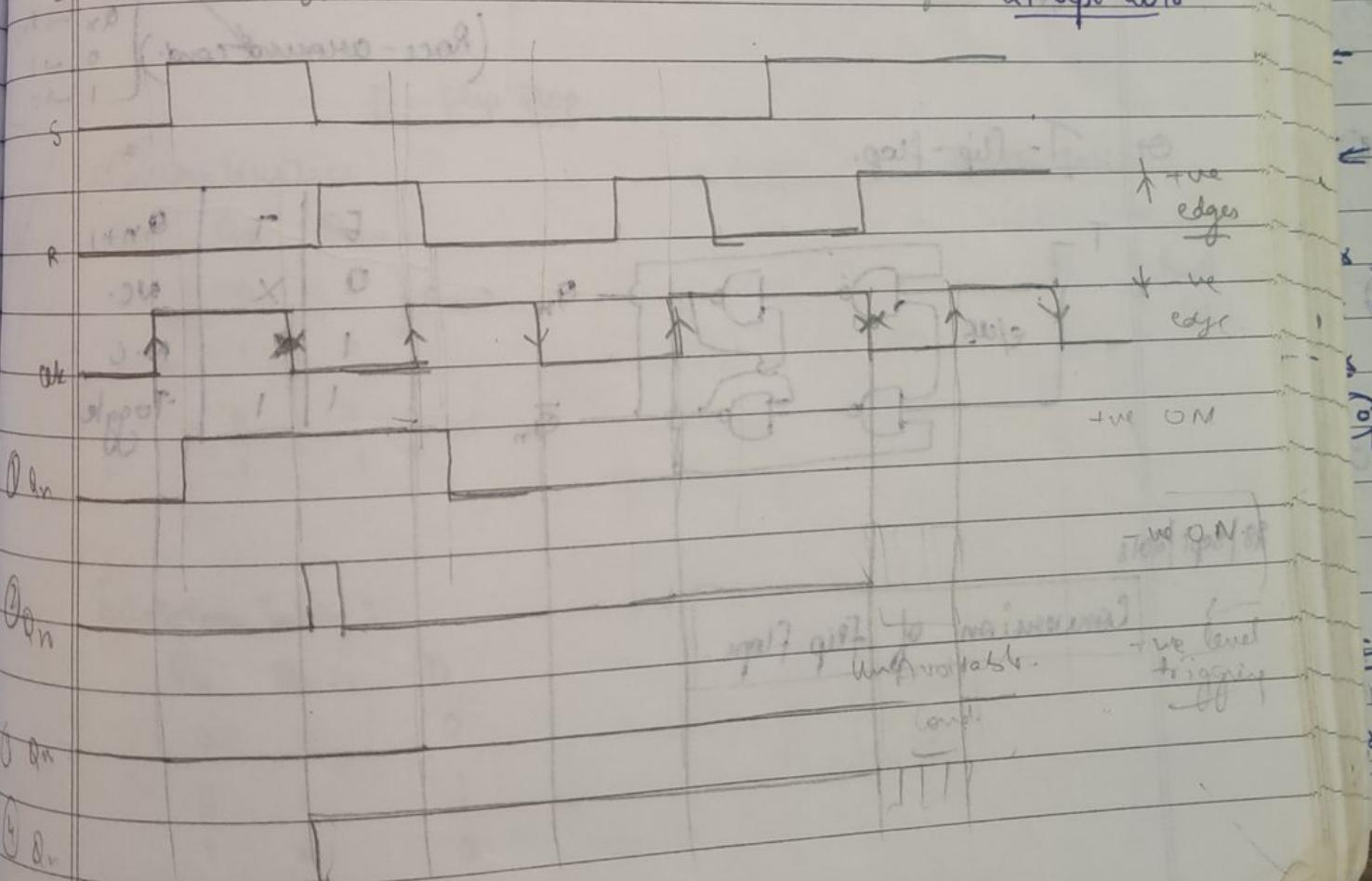
No change 0 0 Qn = Qn+1

Reset 0 1 0 1

Set 1 0 1 0

Invalid 1 1 1 1

- ① +ve level triggering ② -ve level ③ +ve edge triggering 21-Sept-2018

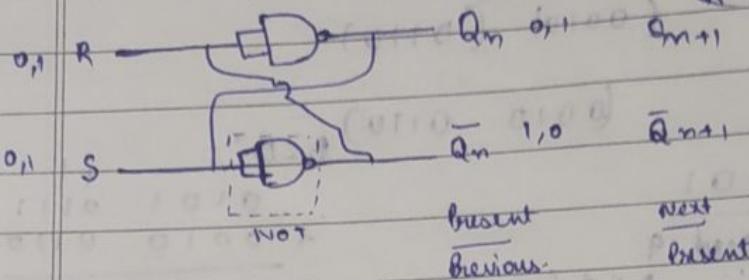


18-Sept-2018

Combinations
not depend on
previous QP.

Sequential Circuits

Gross-Coupled Nand Gate



- 1 bit memory cell.

(R-S latch)

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Cases:-

(i) When $R=0, S=0$

invalid state

$$Q_n = 1, \bar{Q}_n = 1$$

Prohibited state

latch - no clock pulse
is provided

(ii) When $R=0, S=1$

$$Q_n = 1, \bar{Q}_n = 0$$

flip-flops - clock pulse
is provided

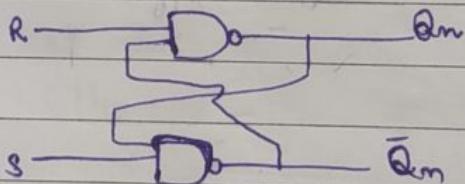
(iii) When $R=1, S=0$

$$Q_n = 0, \bar{Q}_n = 1$$

(iv) When $R=1, S=1$

$$Q_n = 0, \bar{Q}_n = 0$$

R-S latch.



state R S Q_n \bar{Q}_n

Invalid 0 0 1 1

Set 0 1 1 0

Reset 1 0 0 1

No change 1 1 $Q_n = Q_{n+1}$

Invalid
cond.

Case I. When $R, S = 0$

$$Q_n = 1, \bar{Q}_n = 1$$

invalid state / Prohibited state

Case II

When $R = 0, S = 1$

$$Q_n = 1, \bar{Q}_n = 0$$

Set state.

g. Add $(57)_{10}$ & $(26)_{10}$ using BCD addition

$$\begin{array}{r}
 (57)_{10} \\
 / \\
 (0101) \quad (0111)
 \end{array}
 \quad
 \begin{array}{r}
 (26)_{10} \\
 / \\
 (0010) \quad (0110)
 \end{array}$$

$$\begin{array}{l}
 (01010111)_{BCD} \quad (0010 \quad 0110)_{BCD} \\
 \begin{array}{r}
 0111 \quad 1101 \\
 \hline
 \text{Exceed 9} \\
 \therefore \text{Add 6} \\
 \begin{array}{r}
 0111 \quad 1101 \\
 + 0000 \quad 0110 \\
 \hline
 1000 \quad 0010
 \end{array}
 \end{array}
 \end{array}$$

$$\begin{array}{r}
 0101 \quad 0111 \\
 + 0010 \quad 0110 \\
 \hline
 0111 \quad 1101
 \end{array}$$

$$\begin{array}{l}
 (1000 \quad 0010)_{BCD} \\
 (83)_{10}.
 \end{array}$$

y. Perform $(51)_{10} + (46)_{10}$ using BCD addition

$$\begin{array}{r}
 (51)_{10} \\
 / \\
 (0101 \quad 0111)_{BCD}
 \end{array}
 \quad
 \begin{array}{r}
 (46)_{10} \\
 / \\
 (0100 \quad 0110)_{BCD}
 \end{array}$$

$$\begin{array}{r}
 0101 \quad 0111 \\
 + 0100 \quad 0110 \\
 \hline
 1001 \quad 1101
 \end{array}$$

$$\begin{array}{r}
 \text{Carry} \\
 \text{i.e. result is} \\
 \text{now } > 9 \\
 \text{Add 6 to it}
 \end{array}
 + \begin{array}{r}
 0110 \quad 0110 \\
 \hline
 1000 \quad 0011
 \end{array}
 = [0001 \quad 0000 \quad 0010]_{BCD}$$

$$(103)_{10}.$$

12-Sept-2018

BCD addition

e.g. Add $(2)_{10} + (6)_{10}$ using BCD addition

$$\begin{array}{r}
 (2)_{10} = 0010 \\
 + (6)_{10} = 0110 \\
 \hline
 b = 1000 = (8)_{10}
 \end{array}$$

$$(2)_{10} + (6)_{10} = (8)_{10}$$

e.g. Add $(7)_{10} + (6)_{10}$

$$(7)_{10} = (0111)$$

$$(7)_{10} + (6)_{10} = (1101) = (13)_{10}$$

$$\begin{array}{r}
 0111 \\
 + 0110 \\
 \hline
 1101
 \end{array}$$

10_{base}

Rule Whenever the result is greater than 9 then add 6 to the result always.

Now in above eg. we will have

$$\begin{array}{r}
 1101 \\
 + 0110 \\
 \hline
 1001
 \end{array}$$

↑ carry

$$\begin{array}{r}
 1001 \\
 + 0011 \\
 \hline
 1100
 \end{array}$$

\rightarrow BCD

$$\begin{array}{r}
 1 \\
 1 \\
 0 \\
 0 \\
 \hline
 1 \\
 1 \\
 0 \\
 1
 \end{array}$$

\rightarrow BCD

$$\begin{aligned} (4)_{10} &= (0100)_2 \\ &+ (0111)_2 \\ &\underline{(1011)_2} \end{aligned}$$

As the final carry is zero, so the result is in -ve form or in 2's complement representation.

$$\boxed{0} (1011)_2$$

$$\underline{-11} \\ (1010)_2 - 1's \text{ complement}$$

$$(0101)_2 - (\text{again compl.}) - \text{neg. ans.} \\ = (5)_{10}$$

$$\text{Hence. } (4)_{10} - (9)_{10} = (5)_{10}$$

$$\begin{array}{r} 1010 \\ 0101 \\ \hline 1010 \end{array}$$

(iii) when A & B both are -ve

g. Perform $(-4)_{10} - (-6)_{10}$ using 2's complement

Step 1. obtain 2's complement of $(6)_{10}$

$$(6)_{10} = (0110)_2$$

$$= (1001)_2 - 1's \text{ complement}$$

$$+1 = (1010)_2 - \text{and complement}$$

Step 2.

$$(-4)_{10} = (4)_{10} = (0100)_2 \quad (-4)_{10} = (1011)_2 -$$

Add $(-4)_{10}$ to 2's complement of $(6)_{10}$.

$$(6)_{10} = (0110)_2 \rightarrow (1001)_2 - 1^{\text{st}} \text{ carry}$$

$$(1010)_2 - 2^{\text{nd}} \text{ complement}$$

$$(4)_{10} = (0100)_2 \rightarrow (1011)_2 - 1^{\text{st}} \text{ carry}$$

$$+1 = (1010)_2 - 2^{\text{nd}} \text{ complement}$$

$$\text{next } (1010)_2 + (1100)_2 \rightarrow \text{True form}$$

$$1010$$

$$1100$$

$$\underline{0110}$$

$$1010$$

$$1100$$

$$\underline{0110}$$

$$1010$$

$$1100$$

$$\underline{0110}$$

$$1010$$

General rules for 2's complement

STEP 1.

Add $(A)_2$ to 2's complement of $(B)_2$

STEP 2. If final carry is generated then the result is +ve and is in true form.

If the carry generated is zero or no carry then the result is in its -ve form and in 2's complement representation

Cases:-

- (i) When $A > B$
- (ii) When $A < B$
- (iii) $A + B = -ve$
- (iv) $A = B$.

Case (i) When $A > B$ & $A + B$ are +ve

eg. Perform $(9)_{10} - (5)_{10}$ using 2's complement

STEP 1. Obtain 2's comp. of $(5)_{10}$

$$\begin{aligned} (5)_{10} &= (0101)_2 \\ &= (1010)_2 - 1's \text{ complement} \\ &\quad +1 \end{aligned}$$

$(1011)_2$ - 2's complement

STEP 2. Add $(9)_{10}$ to 2's complement of $(5)_{10}$

$$(9)_{10} = (1001)_2$$

$$(5)_{10} = (1011)_2 - 2's \text{ comp.}$$

$$\boxed{1} \underline{0100}$$

- True form.

$$\text{Hence } (9)_{10} - (5)_{10} = (0100)_2 - \underline{\text{Ans.}}$$

Case (ii) When $A < B$ & $A + B$ are +ve

eg. Perform $(4)_{10} - (9)_{10}$ using 2's complement form.

STEP 1. Obtain 2's complement of $(9)_{10}$

$$(9)_{10} = (1001)_2$$

$$(0110)_2 - 1's \text{ comp.}$$

$$\underline{+1} \quad \underline{(0111)}_2 - 2's \text{ comp}$$

STEP 2. Add $(4)_{10}$ to 2's comp. of $(9)_{10}$