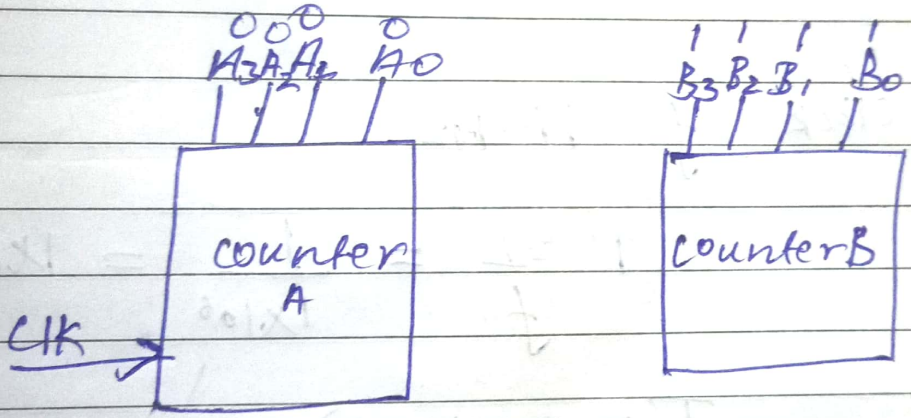
Assignment ⇒ (Md. Danish GIS - VLSI)

Q. There are 2 counters "counter A" being asynchronous up counter and "counter B" is an asynchronous down counter and at T=0, 0000 & 1111 are loaded respectively as shown. Clock source (CLK) available is 1MHz.



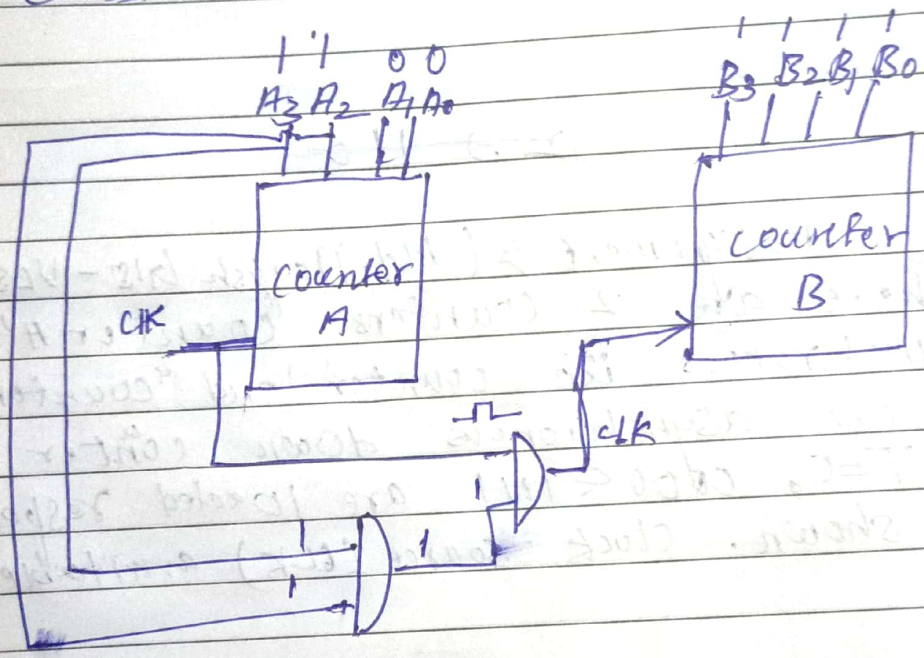
(1) complete the design such that counter B decrements by one value each time when decimal "12" appears at output of counter A (A0 being LSB)?

(2) What is the decimal value at outputs of both counter A & counter B at T=0.2 milli seconds ?

(3) What is the frequency of B_0 with respect to clock (1 MHz) ?

Soln

(1) Ans $12 \rightarrow 1100$



(2) Ans Clock $f = 1\,MHz$

$$T = \frac{1}{f} = \frac{1}{1\times10^6} = 1\times10^{-6}\ sec$$

$$T = 0.001\times10^{-3}\ sec$$

$$T = 0.001\ m sec$$

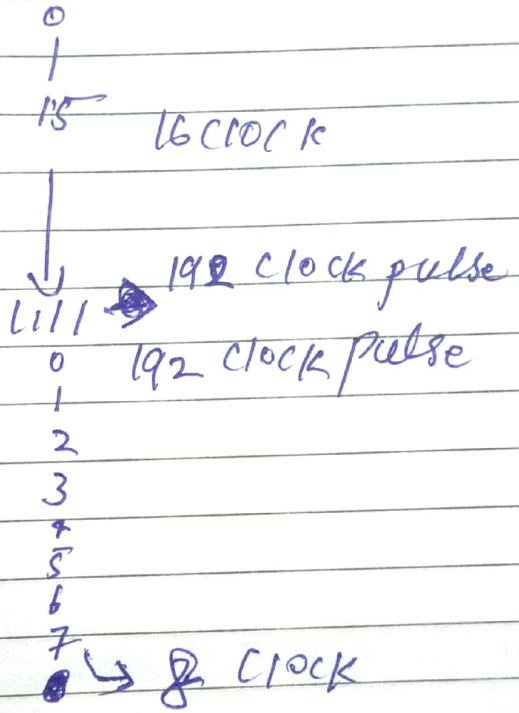
No of clocks = $\frac{0.2}{0.001}$ = 200 clocks

Output of counter A after 200 clocks

4 bit

no of states = 2^4 = 16 States

0 ⟶ 15



$$16 \overline{)200}\ (12,\ 16,\ 40,\ 32,\ 8$$

192

Scan output of counter A after T = 0.2 ms

i.e 7 ⇒ 0111

Now for counter B

1111 → 15

12 times 192 clocks of counter B

3

12 clocks

Time = 12 × 0.001 msec

⇒ 0.012 Sec

So the value at counter B is 3 after T = 0.2m sec

↓

0011

(B) Ans

clk = 1MHz

for LSB (B_0) = $\frac{f}{2}$

= $\frac{1}{2}$ = 0.5MHz

= 0.5MHz