

31. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add two registers	$Rd \leftarrow Rd + Rr$	Z,C,N,VH	1
ADC	Rd, Rr	Add with carry two registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl, K	Add immediate to word	Rdh: Rdl \leftarrow Rdh: Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract constant from register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with carry two registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with carry constant from reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl, K	Subtract immediate from word	Rdh: Rdl \leftarrow Rdh: Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND registers	$Rd \leftarrow Rd \times Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND register and constant	$Rd \leftarrow Rd \times K$	Z,N,V	1
OR	Rd, Rr	Logical OR registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR register and constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd, K	Set bit(s) in register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd, K	Clear bit(s) in register	$Rd \leftarrow Rd \times (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for zero or minus	$Rd \leftarrow Rd \times Rd$	Z,N,V	1
CLR	Rd	Clear register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply unsigned	R1:R0 \leftarrow Rd \times Rr	Z,C	2
MULS	Rd, Rr	Multiply signed	R1:R0 \leftarrow Rd \times Rr	Z,C	2
MULSU	Rd, Rr	Multiply signed with unsigned	R1:R0 \leftarrow Rd \times Rr	Z,C	2
FMUL	Rd, Rr	Fractional multiply unsigned	R1:R0 \leftarrow (Rd \times Rr) \ll 1	Z,C	2
FMULS	Rd, Rr	Fractional multiply signed	R1:R0 \leftarrow (Rd \times Rr) \ll 1	Z,C	2
FMULSU	Rd, Rr	Fractional multiply signed with unsigned	R1:R0 \leftarrow (Rd \times Rr) \ll 1	Z,C	2
Branch Instructions					
RJMP	k	Relative jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct jump	$PC \leftarrow k$	None	3
RCALL	k	Relative subroutine call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct subroutine call	$PC \leftarrow k$	None	4
RET		Subroutine return	$PC \leftarrow \text{STACK}$	None	4
RETI		Interrupt return	$PC \leftarrow \text{STACK}$	I	4
CPSE	Rd, Rr	Compare, skip if equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd, Rr	Compare	$Rd - Rr$	Z,N,V,C,H	1

31. Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CPC	Rd, Rr	Compare with carry	$Rd - Rr - C$	Z, N, V, C, H	1
CPI	Rd, K	Compare register with immediate	$Rd - K$	Z, N, V, C, H	1
SBRC	Rr, b	Skip if bit in register cleared	if $(Rr(b) = 0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRs	Rr, b	Skip if bit in register is set	if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if bit in I/O register cleared	if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if bit in I/O register is set	if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if status flag set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if status flag cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if not equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if carry set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if carry cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if same or higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if greater or equal, signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if less than zero, signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if half carry flag set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if half carry flag cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T flag set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T flag cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if overflow flag is set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if overflow flag is cleared	if $(V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if interrupt enabled	if $(I = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if interrupt disabled	if $(I = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
Bit and Bit-Test Instructions					
SBI	P, b	Set bit in I/O register	$I/O(P, b) \leftarrow 1$	None	2
CBI	P, b	Clear bit in I/O register	$I/O(P, b) \leftarrow 0$	None	2
LSL	Rd	Logical shift left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z, C, N, V	1
LSR	Rd	Logical shift right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z, C, N, V	1
ROL	Rd	Rotate left through carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z, C, N, V	1
ROR	Rd	Rotate right through carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z, C, N, V	1
ASR	Rd	Arithmetic shift right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z, C, N, V	1
SWAP	Rd	Swap nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit store from register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to register	$Rd(b) \leftarrow T$	None	1
SEC		Set carry	$C \leftarrow 1$	C	1
CLC		Clear carry	$C \leftarrow 0$	C	1
SEN		Set negative flag	$N \leftarrow 1$	N	1

31. Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CLN		Clear negative flag	$N \leftarrow 0$	N	1
SEZ		Set zero flag	$Z \leftarrow 1$	Z	1
CLZ		Clear zero flag	$Z \leftarrow 0$	Z	1
SEI		Global interrupt enable	$I \leftarrow 1$	I	1
CLI		Global interrupt disable	$I \leftarrow 0$	I	1
SES		Set signed test flag	$S \leftarrow 1$	S	1
CLS		Clear signed test flag	$S \leftarrow 0$	S	1
SEV		Set twos complement overflow.	$V \leftarrow 1$	V	1
CLV		Clear twos complement overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set half carry flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear half carry flag in SREG	$H \leftarrow 0$	H	1
Data Transfer Instructions					
MOV	Rd, Rr	Move between registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy register word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load indirect and post-inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load indirect and pre-dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load indirect and post-inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load indirect and pre-dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load indirect with displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load indirect and post-inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load indirect and pre-dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load indirect with displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store indirect and post-inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store indirect and pre-dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store indirect and post-inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store indirect and pre-dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store indirect with displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store indirect and post-inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store indirect and pre-dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store indirect with displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load program memory	$R0 \leftarrow (Z)$	None	3

31. Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
LPM	Rd, Z	Load program memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load program memory and post-inc	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	3
SPM		Store program memory	$(Z) \leftarrow R1:R0$	None	–
IN	Rd, P	In port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push register on stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop register from stack	$Rd \leftarrow STACK$	None	2
MCU Control Instructions					
NOP		No operation		None	1
SLEEP		Sleep	(see specific descr. for sleep function)	None	1
WDR		Watchdog reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For on-chip debug only	None	N/A