16.30 From Eq. (16.14) or (16.15), we have

$$\triangle V \simeq \frac{C_S}{C_B}\left(\frac{V_{DD}}{2}\right)$$

$$25 \times 10^{-3} = \frac{35}{C_B} \times \frac{1.2}{2}$$

$$\Rightarrow C_B = 840 \text{ fF}$$

This is the maximum allowable value for C_B.

Capacitive load due to cells $= 840 - 20 = 820$ fF

$$\text{Maximum number of cells} = \frac{820}{0.8}$$

$= 1025$ or likely 1024.

Number of row address bits requiring

$$= \log_2 1024 = 10$$

If the sense amplifier gain is increased by a factor of 4, $\triangle V$ is reduced by a factor of 4, and the maximum C_B increases by a factor of 4. Thus, the number of cells can be increased approximately by a factor of 4 to 4096 bits, requiring two more bits for the word address, for a total of 12 bits.

16.31 If the memory array has n columns, it has $2n$ rows and $2n^2$ cells. Refresh time is

$$2n \times 10 \times 10^{-9} = (1 - 0.98) \times 10 \times 10^{-3}$$

$$\Rightarrow n = 10^4 \simeq 8 \text{ kbits}$$

(Recall that 1 kbit = 1024 bits)

Thus the cell array is 8 kbits × 16 kbits or 128 Mbits.

16.32 A 1-Mbit-square array has 1024 words × 1024 bits. Thus the capacitance of the bit line, C_B, is

$$C_B = 1024 \times 0.5 + 12$$

$$= 524 \text{ fF}$$

$$\triangle V(1) \simeq \frac{C_S}{C_B}\left(\frac{V_{DD}}{2}\right)$$

$$= \frac{30}{524}\left(\frac{1.2}{2}\right) = 34.4 \text{ mV}$$

$$\triangle V(0) \simeq -\frac{C_S}{C_B}\left(\frac{V_{DD}}{2}\right) = -34.4 \text{ mV}$$

16.33 The storage capacitor C_S loses 0.2 V in 12 ms as a result of the leakage current I, thus

$$I \times 12 \text{ ms} = C_S \times 0.2 \text{ V}$$

$$\Rightarrow I = \frac{30 \times 10^{-15} \times 0.2}{12 \times 10^{-3}}$$

$$= 0.5 \text{ pA}$$

16.34 From Eq. (16.16), we have

$$v_B = \frac{V_{DD}}{2} + \triangle V(1) e^{(G_m/C_B)t} \qquad (1)$$

$$0.9V_{DD} = 0.5V_{DD} + 0.05e^{(G_m/C_B)\times 2\times 10^{-9}}$$

$$\frac{G_m}{C_B} \times 2 \times 10^{-9} = \ln\left(\frac{0.4\ V_{DD}}{0.05}\right)$$

$$G_m = \frac{C_B}{2 \times 10^{-9}} \times \ln\left(\frac{0.4 \times 1.2}{0.05}\right)$$

$$= \frac{1 \times 10^{-12}}{2 \times 10^{-9}} \times 2.26 = 1.13 \text{ mA/V}$$

$$G_m = g_{mn} + g_{mp}$$

Since the inverters are matched, we have

$$g_{mn} = g_{mp} = \frac{G_m}{2} = \frac{1.13}{2} = 0.565 \text{ mA/V}$$

But,

$$g_{mn} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(\frac{V_{DD}}{2} - V_{tn}\right)$$

$$0.565 \times 10^{-3} = 500 \times 10^{-6}\left(\frac{W}{L}\right)_n (0.6 - 0.4)$$

$$\Rightarrow \left(\frac{W}{L}\right)_n = 5.65$$

$$W_n = 5.65 \times 0.13 = 0.73 \ \mu\text{m}$$

$$W_p = 4W_n = 2.94 \ \mu\text{m}$$

If the input signal is doubled, we can use Eq. (1) to determine t as follows:

$$0.9V_{DD} = 0.5V_{DD} + 0.1e^{(G_m/C_B)t}$$

$$\frac{G_m}{C_B}t = \ln\left(\frac{0.4\ V_{DD}}{0.1}\right)$$

$$t = \frac{1 \times 10^{-12}}{1.13 \times 10^{-3}} \ln(4 \times 1.2)$$

$$= 1.4 \text{ ns}$$

16.35 The value of G_m is given by

$$G_m = g_{mn} + g_{mp}$$

Since the inverters have a matched design, then

$$g_{mn} = g_{mp}$$

and

$$g_{mn} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(\frac{V_{DD}}{2} - V_{tn}\right)$$

$$= 500\left(\frac{0.26}{0.13}\right)\left(\frac{1.2}{2} - 0.4\right)$$

$$= 200 \ \mu\text{A/V} = 0.2 \text{ mA/V}$$

Thus,

$$G_m = 0.4 \text{ mA/V}$$

Assume a read 1 operation,

$$v_B = 0.5V_{DD} + \triangle V(1)e^{(G_m/C_B)t}$$

Thus,

$$0.9V_{DD} = 0.5V_{DD} + \triangle V(1)e^{(G_m/C_B)t}$$

$$\frac{0.4V_{DD}}{\triangle V(1)} = e^{(G_m/C_B)t_1}$$

$$\Rightarrow \triangle V(1) = 0.4V_{DD}e^{-(G_m/C_B)t_d} \qquad (1)$$

Substituting $V_{DD} = 1.2$ V, $G_m = 0.4$ mA/V, $C_B = 0.4$ pF, and $t_d = 1$ ns, we obtain

$$\triangle V(1) = 0.177 \text{ V}$$

Thus the signal between the B and $\overline{B}$ lines is

$$2\triangle V(1) = 0.353 \text{ V} = 353 \text{ mV}$$

If the time can be relaxed by 1 ns, then $t_1 = 2$ ns and

$$\triangle V(1) = 0.065 \text{ V}$$

and the required signal between the B and $\overline{B}$ becomes

$$2\triangle V(1) = 130 \text{ mV}$$

If instead we have $\triangle V(1) = 0.177$ V and $t_1 = 2$ ns, we can see from Eq. (1) that C_B can be increased by the same factor t_1 is increased, that is, by a factor of 2. Thus C_B can become

$$C_B = 2 \times 0.4 = 0.8 \text{ pF}$$

Thus the bit line length can be increased by 100%, i.e., doubled. Doubling the length of the bit line will double the delay time required to charge the bit-line capacitance to 4 ns.

16.36 (a) Using Eq. (16.16)), we write

$$v_B = 0.5V_{DD} + \triangle V(1)e^{(G_m/C_B)t}$$

$$0.9V_{DD} = 0.5V_{DD} + \left(\frac{\triangle V}{2}\right)e^{(G_m/C_B)t_d}$$

$$\Rightarrow t_d = \frac{C_B}{G_m}\ln\left(\frac{0.8V_{DD}}{\triangle V}\right) \qquad \text{Q.E.D.} \qquad (1)$$

An identical expression can be obtained for the case a 0 is being read.

(b) If t_d is to be reduced to one-half its original value, G_m must be increased by a factor of 2. This can be achieved by doubling the width of all transistors (because g_{mn} and g_{mb} are proportional to $(W/L)_n$ and $(W/L)_p$, respectively).

(c) Consider Eq. (1) in two situations: (1) $\triangle V = 0.2$ V and $G_m = G_{m1}$, (2) $\triangle V = 0.1$ V and $G_m = G_{m2}$. If in both cases the same value of t_d results, then

$$\frac{1}{G_{m1}}\ln\left(\frac{0.8 \times 1.2}{0.2}\right) = \frac{1}{G_{m2}}\ln\left(\frac{0.8 \times 1.2}{0.1}\right)$$

$$\Rightarrow \frac{G_{m2}}{G_{m1}} = 1.44$$

To increase G_m by a factor of 1.44, the widths of all transistors must be increased by a factor of 1.44.

16.37 To meet the delay specification in both cases of a stored 1 and a stored 0, we must design for the worst case, which is the case of a stored 1. The initial voltage that develops on the half-bit line is +40 mV. Thus the voltage of the half-bit line will rise exponentially from $(V_{DD}/2)$, as

$$v_B = \frac{V_{DD}}{2} + \triangle V(1)e^{(G_m/C_B)t}$$

To develop a differential output voltage of 1 V and recalling that the bit-line on the dummy-cell side remains at a constant voltage of $(V_{DD}/2)$, we required v_B to rise to $(V_{DD}/2) + 1$, thus

$$1 \text{ V} = 0.04e^{(G_m/C_B)t_d}$$

where $t_d = 2$ ns and $C_B = 0.5$ pF. The value of G_m can be found from

$$\frac{G_m}{0.5 \times 10^{-12}} \times 2 \times 10^{-9} = \ln\left(\frac{1}{0.04}\right)$$

$$\Rightarrow G_m = 0.8 \text{ mA/V}$$

Now,

$$G_m = g_{mn} + g_{mp}$$

Since the inverters have a matched design,

$$g_{mn} = g_{mp} = 0.4 \text{ mA/V}$$

and

$$g_{mn} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n\left(\frac{V_{DD}}{2} - V_t\right)$$

$$0.4 = 0.3 \times \left(\frac{W}{L}\right)_n (0.9 - 0.5)$$

$$\Rightarrow \left(\frac{W}{L}\right)_n = 3.33$$

and

$$\left(\frac{W}{L}\right)_p = 4\left(\frac{W}{L}\right)_n = 13.32$$

Now, if a 0 is read, then

$$v_B = \frac{V_{DD}}{2} - \triangle V(0)e^{(G_m/C_B)t_d}$$

$$\frac{V_{DD}}{2} - 1 = \frac{V_{DD}}{2} - 0.1e^{(G_m/C_B)t_d}$$

$$\Rightarrow t_d = \frac{C_B}{G_m} \ln 10$$

$$= \frac{0.5 \times 10^{-12}}{0.8 \times 10^{-3}} \times 2.3 = 1.44 \text{ ns}$$

which, as expected, is less than the worst-case value of 2 ns (because of the larger $\triangle V$). If a 1 is read, then

$$v_B = \frac{V_{DD}}{2} + \triangle V(1)e^{(G_m/C_B)t_d}$$

$$\frac{V_{DD}}{2} + 1 = \frac{V_{DD}}{2} + 0.04e^{(G_m/C_B)t_d}$$

$$\Rightarrow t_d = \frac{C_B}{G_m} \ln 25$$

$$= \frac{0.5 \times 10^{-12}}{0.8 \times 10^{-3}} \times 3.2 = 2 \text{ ns}$$

as expected.

16.38 Using Eq. (16.18), we have

$$\triangle t = \frac{CV_{DD}}{I}$$

$$0.5 \times 10^{-9} = \frac{50 \times 10^{-15} \times 1.2}{I}$$

$$\Rightarrow I = 120 \ \mu\text{A}$$

$$P_D = V_{DD}I$$

$$= 1.2 \times 120 = 144 \ \mu\text{W}$$

16.39

(a) $V_{D1} = V_{D2} = V_{DD} - V_t - V_t = V_{DD} - 2V_t$

$$= 1.2 - 0.8 = 0.4 \text{ V}$$

(b) $\triangle V = \sqrt{2}\, V_{OV}$

$$140 = \sqrt{2}\, V_{OV}$$

$$\Rightarrow V_{OV} \simeq 100 \text{ mV} = 0.1 \text{ V}$$

$$V_{S1,2} = V_{DD} - V_t - V_{GS}$$

$$= V_{DD} - V_t - V_t - V_{OV}$$

$$= 1.2 - 0.4 - 0.4 - 0.1 = 0.3 \text{ V}$$

(c) $\triangle t = \frac{CV_{DD}}{I}$

$$0.5 \times 10^{-9} = \frac{55 \times 10^{-15} \times 1.2}{I}$$

$$\Rightarrow I = 132 \ \mu\text{A}$$

(d) $\frac{I}{2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2} V_{OV}^2$

$$\frac{0.132}{2} = \frac{1}{2} \times 0.5 \times \left(\frac{W}{L}\right)_{1,2} \times 0.1^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_{1,2} = 26.4$$

For Q_3 and Q_4,

$$\frac{132}{2} = \frac{1}{2} \times 125 \left(\frac{W}{L}\right)_{3,4} (1.2 - 0.4 - 0.4)^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_{3,4} = 6.6$$

(e) $0.132 = \frac{1}{2} \times 0.5 \times \left(\frac{W}{L}\right)_5 \times 0.1^2$

$$\left(\frac{W}{L}\right)_5 = 52.8$$

$$V_R = V_t + V_{OV} = 0.5 \text{ V}$$

16.40 Since $2^{10} = 1024$, there are 10 address bits.

The decoder has 1024 output lines. The NOR array requires 20 input lines (for the 10 address bits and their complements).

Each output line has one PMOS transistor; for a total of 1024 PMOS transistors.

Each output line has 10 NMOS transistors for a total of $1024 \times 10 = 10,240$ NMOS transistors.

The total number of NMOS and PMOS transistors is 11,264.

16.41 In a 1-Mbit-square array, there are 1024 columns, requiring 10 address bits.

1024 NMOS pass transistors are needed in the multiplexer. The NOR decoder has 1024 output lines; each output line has one PMOS transistor, for a total of 1024 PMOS transistors. Each output line has 10 NMOS transistors, for a total 10,240 NMOS transistors. Total number of transistors

$$= 1024 + 1024 + 10,240 = 12,288$$

16.42 A square 1-Mbit array has 1024 columns, requiring 10 address bits. Ten levels of pass gates are required.

Using the expression given to the answer of Exercise 16.13, we have

Total number of transistors $= 2(2^N - 1)$

$$= 2(2^{10} - 1) = 2046$$

16.43 Refer to Fig. 1.

$$T = (3t_{PHL} + 2t_{PLH}) + (2t_{PHL} + 3t_{PLH})$$

$$= (3 \times 2 + 2 \times 3) + (2 \times 2 + 3 \times 3)$$

$$= 12 + 13 = 25 \text{ ns}$$

$$f = \frac{1}{T} = \frac{1}{25 \times 10^{-9}} = 40 \text{ MHz}$$

The output is high for 12 of the 25-ns period = 48% of the cycle. Note that

$$t_P = \frac{1}{2}(t_{PLH}) + (t_{PHL})$$

$$= \frac{1}{2}(3 + 2) = 2.5 \text{ ns}$$

$$T = 2Nt_P = 2 \times 5 \times 2.5 = 25 \text{ ns}$$

as found graphically.

This figure belongs to Problem 16.43.

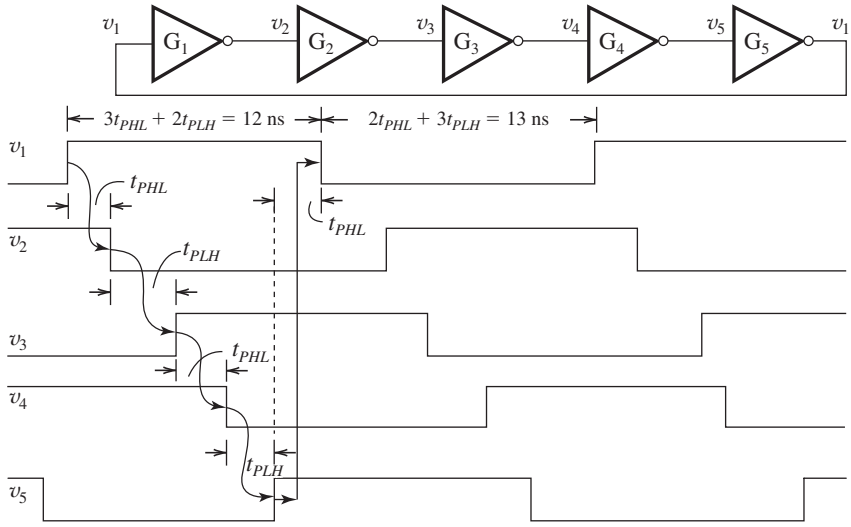

Figure 1

16.44 $f = \dfrac{1}{2Nt_P}$

$20 \times 10^6 = \dfrac{1}{2 \times 9t_P}$

$\Rightarrow t_P = 2.78$ ns

16.45 We need four inverters to implement the 10-ns delay block.

16.46 Refer to Fig. 16.30 and recall that a cell without a transistor is storing a logic 1 while a cell with a transistor is storing a logic 0. Thus the eight words, W_1 to W_8, are:

1101, 1111, 1110, 0110, 0101, 0111, 1001, 1011

16.47 Need $z = xy$

W	X	Y	Z
0	00	00	0000
1	00	01	0000
2	00	10	0000
3	00	11	0000
4	01	00	0000
5	01	01	0001
6	01	10	0010
7	01	11	0011
8	10	00	0000
9	10	01	0010
10	10	10	0100
11	10	11	0110
12	11	00	0000
13	11	01	0011
14	11	10	0110
15	11	11	1001

See Figure on next page.

16.48

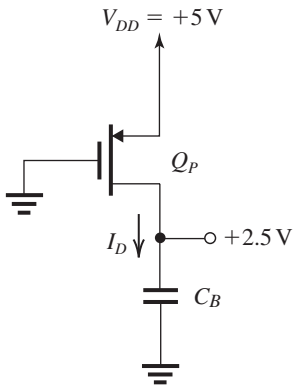

Figure 1

(a) Figure 1 shows the relevant part of the circuit during the precharge phase. Note that Q_P is operating in the triode region, thus

$$I_D = 30 \times \frac{12}{1.2}\left[(5-1)2.5 - \frac{1}{2}(2.5)^2\right]$$

$= 2.06$ mA

$$\triangle t = \frac{C_B V_{DD}}{I_D}$$

$$= \frac{1 \times 10^{-12} \times 5}{2.06 \times 10^{-3}} = 2.4 \text{ ns}$$

(b) $t_r = 2.2\tau$

$= 2.2CR$

$= 2.2 \times 2 \times 10^{-12} \times 5 \times 10^3$

$= 22$ ns

$v_W(t = \tau) = V_{DD}(1 - e^{-1})$

$= 3.16$ V

This figure belongs to Problem 16.47.