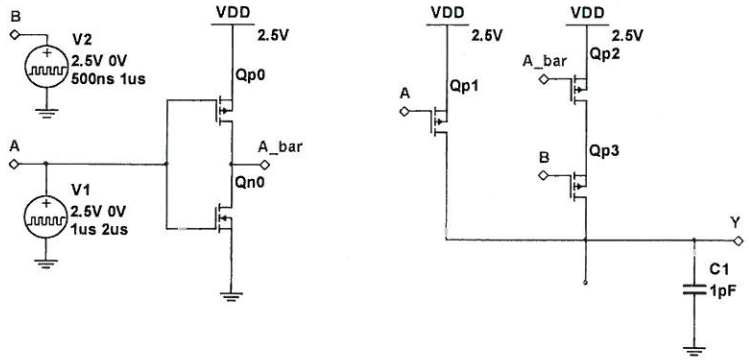
ECE 321, Electronics I

Quiz 5 (Fall 2016), CMOS Logic

Name _____

Section _____

1. (100 points) The figure below shows the pull-up network (PUN) for a logic function Y with 3 inputs.



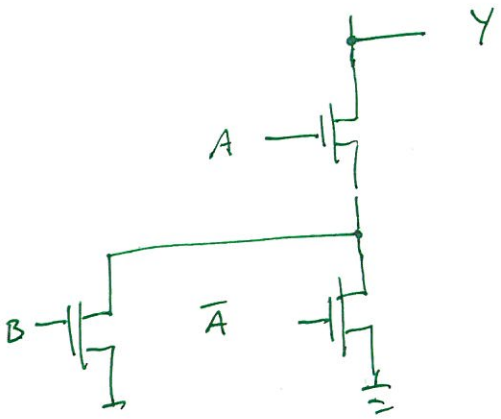
a. (25 points) Fill in the truth table below.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

b. (25 points) Determine the logic function for Y, either by inspection or reducing the truth table.

$$Y = \bar{A} + A\bar{B} = \bar{A} + \bar{B} = \overline{AB}$$

c. (25 points) Draw the pull-down network (PDN).



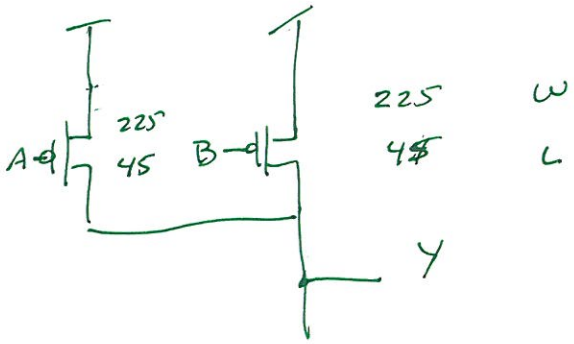
d. (25 points) If an inverter with $\left(\frac{W}{L}\right)_n = \frac{90\text{ nm}}{45\text{ nm}}$ and $\left(\frac{W}{L}\right)_p = \frac{225\text{ nm}}{45\text{ nm}}$ produces equal t_{PHL} and t_{PLH}, and we want to match those delays with our gate, size the transistors in the pull-up network. The minimum-length transistors have channel length, L, of 45 nm.

$\left(\frac{W}{L}\right)_{QP1} = \frac{225\text{nm}}{45\text{nm}}$ $\left(\frac{W}{L}\right)_{QP2} = \frac{450}{45}$ $\left(\frac{W}{L}\right)_{QP3} = \frac{450}{45}$

Bonus. (Up to 25 points) Minimize the expression for $\overline{Y}$ and draw the pull-up network to implement the minimized expression. Size the transistors for worst-case delay to match the delay of the reference inverter.

$Y = \overline{A} + \overline{B}$

$\overline{Y} = \overline{\overline{A} + \overline{B}} = AB$



2. (100 points) Figures 2 and 3 below show two different options to implement the PDN from Part I whose logic function Y was $Y = \overline{A} + A\overline{B}$, with PUN shown in Figure 1.

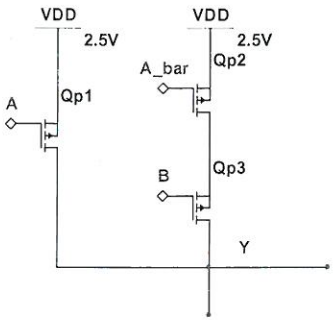


Figure 1 PUN

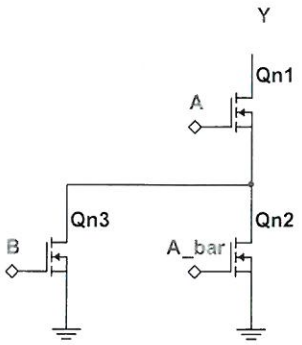


Figure 2 PDN option 1

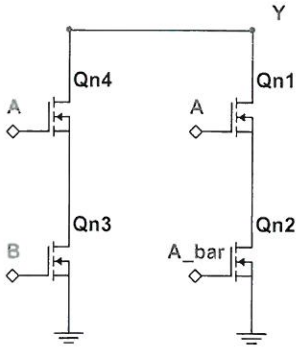


Figure 3 PDN option 2

(10 points) Write the logic function $\overline{Y}$ for PDN option 1. Do not reduce.

$\overline{Y} = A(B + \overline{A})$

(10 points) Write the logic function $\overline{Y}$ for PDN option 2. Do not reduce.

$\overline{Y} = AB + A\overline{A}$

(10 points) Write the minimized logic function of $\overline{Y}$ and draw the PDN to the right.

$\overline{Y} = AB$

(25 points) What is the sizing requirement $n=x(W/L)$ for each PDN transistor in options 1 and 2 and in the minimized PDN. x is the factor by which the basic inverter is scaled.

3x each

x-option 1 = 2

4x each

x-option 2 = 2

2x each

x-minimized = 2

(45 points) Using your results above, explain why using reduced logic functions reduces the area required to synthesize a logic function, while optimizing delays.

we gain nothing in sizing (per transistor) by using a non-minimized implementation and it takes more transistors