$t_{PLH} = 0.69CR_P$

$= 0.69 \times 20 \times 10^{-15} \times 30 \times 10^3$

$= 414$ ps

$t_P = \frac{1}{2}(172.5 + 414)$

$= 293.3$ ps

14.49 For

$t_{PHL} = t_{PLH} = t_P \leq 50$ ps

we use

$t_{PHL} = 0.69CR_N$

$= 0.69C \times \frac{12.5}{(W/L)_n} \times 10^3$

and thus obtain

$0.69 \times 10 \times 10^{-15} \times \frac{12.5}{(W/L)_n} \times 10^3 \leq 50 \times 10^{-12}$

$\Rightarrow \left(\frac{W}{L}\right)_n \geq 1.725$

Similarly,

$t_{PLH} = 0.69\ C\ R_P$

$= 0.69\ C \times \frac{30}{(W/L)_p} \times 10^3$

Thus,

$0.69 \times 10 \times 10^{-15} \times \frac{30}{(W/L)_p} \times 10^3 \leq 50 \times 10^{-12}$

$\Rightarrow (W/L)_p \geq 4.14$

14.50 Refer to Example 14.6.

The method of average currents yields

$t_{PHL} = 41.2$ ps

The method of equivalent resistance yields

$t_{PHL} = 57.5$ ps

If the discrepancy is entirely due to the reduction in current due to velocity saturation in the NMOS transistor, then the factor by which the current decreases is $41.2/57.5 = 0.716$.

The value of t_{PLH} does not change (in fact there is a slight decrease due to various approximations). We may therefore conclude that the effect of velocity saturation is minimal in the PMOS transistor.

14.51 $\alpha_n = 2\Big/\left[\frac{7}{4} - \frac{3\ V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$

$= 2\Big/\left[\frac{7}{4} - \frac{3 \times 0.35}{1} + \left(\frac{0.35}{1}\right)^2\right]$

$= 2.43$

$t_{PHL} = \frac{\alpha_n C}{k_n'(W/L)_n V_{DD}}$

$= \frac{2.43 \times 10 \times 10^{-15}}{470 \times 10^{-6} \times 1.5 \times 1}$

$= 34.4$ ps

$t_{PLH} = \frac{\alpha_p C}{k_p'(W/L)_p V_{DD}}$

Since $|V_{tp}| = V_{tn}$, we have

$\alpha_p = \alpha_n = 2.43$

Thus,

$t_{PLH} = \frac{2.43 \times 10 \times 10^{-15}}{190 \times 10^{-6} \times 3 \times 1}$

$= 42.6$ ps

$t_P = \frac{1}{2}(34.4 + 42.6) = 38.5$ ps

The theoretical maximum switching frequency is

$f_{\max} = \frac{1}{2t_P} = \frac{1}{2 \times 38.5 \times 10^{-12}} \simeq 13$ GHz

14.52 $C = 4 \times 0.27 + 4 \times 0.27 + 2 + 2 + 5$

$= 11.16$ fF

$\alpha_n = 2\Big/\left[\frac{7}{4} - \frac{3\ V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$

$= 2\Big/\left[\frac{7}{4} - \frac{3 \times 0.5}{1.8} + \left(\frac{0.5}{1.8}\right)^2\right]$

$= 2.01$

$t_{PHL} = \frac{\alpha_n C}{k_n'\left(\frac{W}{L}\right)_n V_{DD}}$

$= \frac{2.01 \times 11.16 \times 10^{-15}}{380 \times 10^{-6} \times \frac{0.27}{0.18} \times 1.8}$

$= 21.9$ ps

$\alpha_p = \alpha_n = 2.01$

$t_{PLH} = \frac{\alpha_p C}{k_p'\left(\frac{W}{L}\right)_p V_{DD}}$

$= \frac{2.01 \times 11.16 \times 10^{-15}}{\frac{380}{4} \times 10^{-6} \times \frac{0.27}{0.18} \times 1.8}$

$= 87.6$ ps

$$t_P = \frac{1}{2}(21.9 + 87.6) = 54.8 \text{ ps}$$

If the design is changed to a matched one, then

$$W_p = 4W_n = 4 \times 0.27 = 1.08 \ \mu\text{m}$$

$$C = 4 \times 0.27 + 4 \times 1.08 + 2 + 2 + 5$$

$$= 14.4 \text{ fF}$$

$$\alpha_n = \alpha_p = 2.01$$

$$t_{PHL} = \frac{2.01 \times 14.4 \times 10^{-15}}{380 \times 10^{-6} \times \dfrac{0.27}{0.18} \times 1.8}$$

$$= 28.2 \text{ ps}$$

$$t_{PLH} = \frac{2.01 \times 14.4 \times 10^{-15}}{\dfrac{380}{4} \times 10^{-6} \times \dfrac{1.08}{0.18} \times 1.8}$$

$$= 28.2 \text{ ps}$$

$$t_P = \frac{1}{2}(28.2 + 28.2) = 28.2 \text{ ps}$$

14.53 $W_n = 0.75 \ \mu\text{m}$

$$W_p = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} \times W_n$$

$$= \frac{180}{45} \times 0.75 = 3.0 \ \mu\text{m}$$

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$

where

$$C_{gd1} = 0.4 \times W_n = 0.4 \times 0.75 = 0.3 \text{ fF}$$

$$C_{gd2} = 0.4 \times W_p = 0.4 \times 3 = 1.2 \text{ fF}$$

$$C_{db1} = 1 \times W_n = 1 \times 0.75 = 0.75 \text{ fF}$$

$$C_{db2} = 1 \times W_p = 1 \times 3 = 3 \text{ fF}$$

$$C_{g3} = 0.75 \times 0.5 \times 3.7 + 2 \times 0.4 \times 0.75 = 1.9875 \text{ fF}$$

$$C_{g4} = 3 \times 0.5 \times 3.7 + 2 \times 0.4 \times 3 = 7.95 \text{ fF}$$

Thus,

$$C = 2 \times 0.3 + 2 \times 1.2 + 0.75 + 3 + 1.9875 + 7.95 + 2$$

$$= 18.7 \text{ fF}$$

$$\alpha_n = 2 \Big/ \left[\frac{7}{4} - \frac{3\ V_t}{V_{DD}} + \left(\frac{V_t}{V_{DD}} \right)^2 \right]$$

$$= 2 \Big/ \left[\frac{7}{4} - \frac{3 \times 0.7}{3.3} + \left(\frac{0.7}{3.3} \right)^2 \right]$$

$$= 1.73$$

$$t_{PHL} = \frac{\alpha_n C}{k'_n \left(\dfrac{W}{L} \right)_n V_{DD}}$$

$$= \frac{1.73 \times 18.7 \times 10^{-15}}{180 \times 10^{-6} \times \left(\dfrac{0.75}{0.5} \right) \times 3.3}$$

$$= 36.3 \text{ ps}$$

Since the inverter is matched,

$$t_{PLH} = t_{PHL} = 36.3 \text{ ps}$$

and

$$t_P = 36.3 \text{ ps}$$

The propagation delay increases by 50% if C is increased by 50%, that is, by $18.7/2 = 9.35$ fF.

14.54 To reduce t_P by 40 ps, we need to reduce the extrinsic part by 40 ps. Now the original value of the extrinsic part is

$$t_P = 80 \times \frac{45}{45 + 15} = 60 \text{ ps}$$

A reduction by 40 ps requires the use of a scale factor S,

$$S = 3$$

This is the factor by which $(W/L)_n$ and $(W/L)_p$ must be scaled. The inverter area will be increased by the same ratio, that is, 3.

14.55 (a) Examination of Eq. (14.59) reveals that the NMOS transistors Q_1 and Q_3 contribute

$$C_n = 2\ C_{gd1} + C_{db1} + C_{g3} \tag{1}$$

and the PMOS transistors Q_2 and Q_4 contribute

$$C_p = 2\ C_{gd2} + C_{db2} + C_{g4} \tag{2}$$

The only difference in determining the corresponding capacitances in Eqs. (1) and (2) is the transistor width W. Thus each of the components in Eq. (2) can be written as the corresponding component in Eq. (1) multiplied by (W_p/W_n). Overall, we can write

$$C_p = C_n \frac{W_p}{W_n}$$

and the total capacitance C can be expressed as

$$C = C_n + C_p + C_w$$

$$= C_n + C_n \frac{W_p}{W_n} + C_w$$

Thus,

$$C = C_n \left(1 + \frac{W_p}{W_n} \right) + C_w \qquad \text{Q.E.D.}$$

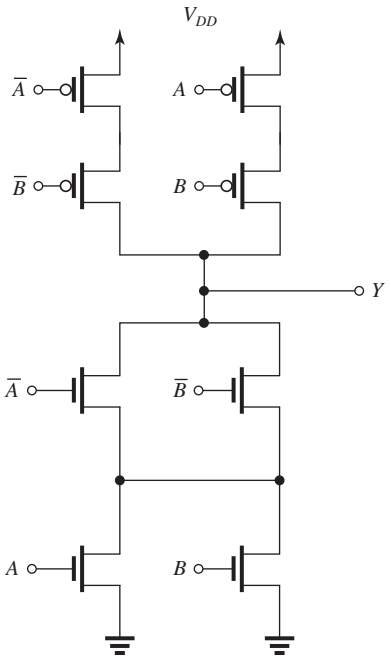

Figure 1

14.12 Direct realization of the given expression results in the PUN portion of the circuit shown in Fig. 1. The PDN is obtained as the dual of the PUN. Not shown are the three inverters needed to obtain $\overline{A}$, $\overline{B}$ and $\overline{C}$.

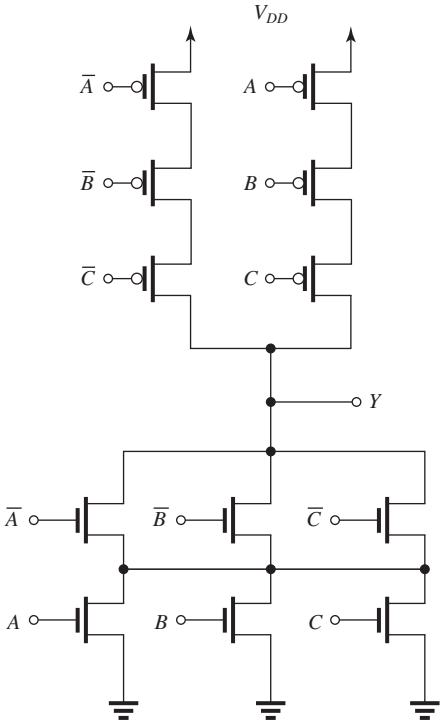

Figure 1

14.13 (a) Even-parity checker:

$$\overline{Y} = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}BC + A\overline{B}C + AB\overline{C}$$

See Fig. 1 on next page.

(b) This expression can be directly realized with the PDN shown in Fig. 1. Note that the circuit requires 12 transistors in addition to the three inverters needed to generate $\overline{A}$, $\overline{B}$, and $\overline{C}$.

(c) From inspection of the PDN in Fig. 1 we see that we can combine the two transistors controlled by $\overline{A}$ and the two transistors controlled by A. This results in the PDN realization shown in Fig. 2 which requires 10 transistors, not counting those in the inverters. See Fig. 2 on next page.

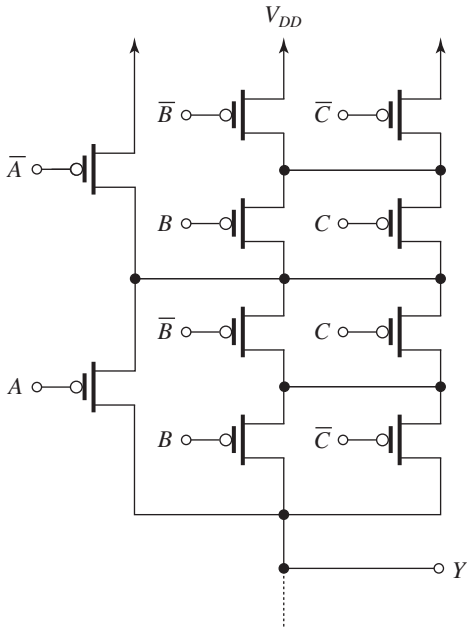

Figure 3

(d) The PUN in Fig. 3 can be obtained as the dual of the PDN in Fig. 2. Combining the PDN and the PUN gives the complete realization of the even-parity checker.

Note: The number of transistors in the PDN of Fig. 2 can be reduced by 2 by combining the two transistors in the bottom row that are controlled by C, and the two transistors that are controlled by $\overline{C}$. The resulting 8-transistor realization is shown in Fig. 4. However, it is not easy to obtain a PUN as a dual of this circuit. See Fig. 4 on next page.

This figure belongs to Problem 14.13, part (a).

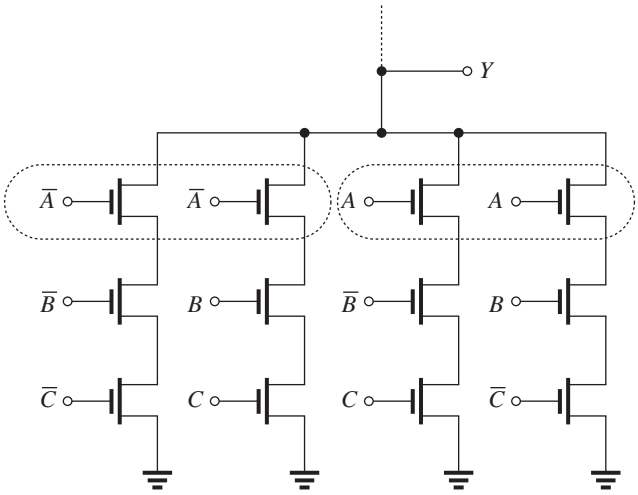

Figure 1

This figure belongs to Problem 14.13, part (c).

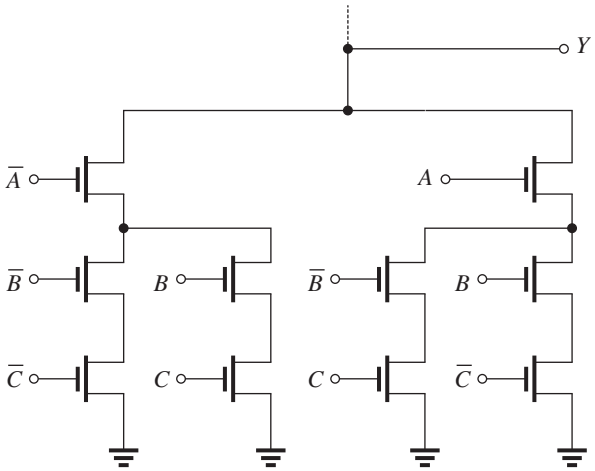

Figure 2

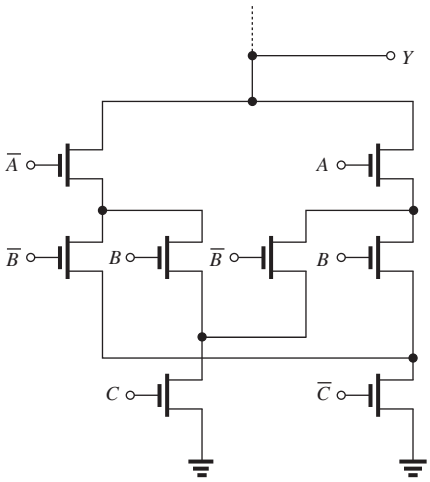

Figure 4

14.14 Odd-parity checker:

$$Y = \overline{A}B\,\overline{C} + \overline{A}\,\overline{B}C + A\overline{B}\,\overline{C} + ABC$$

$$= \overline{A}\,(B\overline{C} + \overline{B}C) + A(BC + \overline{B}\,\overline{C}) \qquad (1)$$

The Boolean expression in Eq. (1) can be directly realized by the PUN in Fig. 1. Recall that we use for the switch control variables the complements of the variables in the equation. It requires 10 transistors in addition to the three inverters needed to provide $\overline{A}$, $\overline{B}$ and $\overline{C}$. The dual of the PUN can be obtained and results in the PDN shown in Fig. 1.

be equal to $3n$. Finally, for the discharge path (Q_{NA}, Q_{NB}) to have an equivalent W/L equal to n, we selected W/L of Q_{NB} equal to $1.5n$.

For the PUN, the worst-case charging path is that through Q_{PB} and one of Q_{PC} or Q_{PD}. Thus we select each of these three transistors to have $W/L = 2p$. Finally, we selected W/L of Q_{PA} equal to p.

14.57

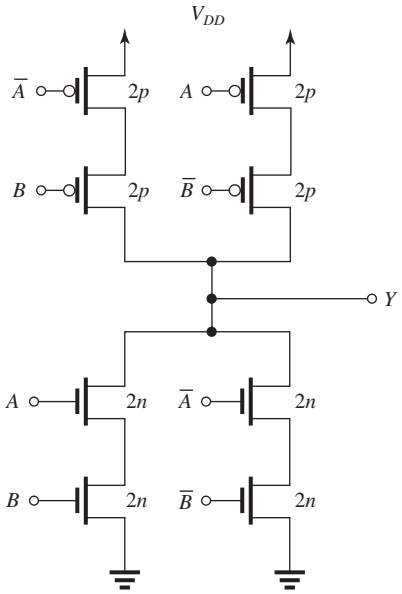

Figure 1

$$n = \frac{0.20}{0.13}\ ,\ p = \frac{0.40}{0.13}$$

Figure 1 shows the circuit with the W/L ratio of each of the eight transistors indicated. Observe that the worst-case situation for both charging and discharging is two transistors in series. To achieve an equivalent W/L ratio for each path equal to that of the corresponding transistor in the basic inverter, each transistor is sized at twice that of the inverter. Including the two inverters required to obtain the complemented variable, the area is

$$A = 2W_nL + 2W_pL + 4 \times 2W_nL + 4 \times 2W_pL$$

$$= 10L(W_n + W_p)$$

$$= 10 \times 0.13(0.2 + 0.4)$$

$$= 0.78\ \mu\text{m}^2$$

14.58 When the devices are sized as in Fig. 14.35, t_{PLH} that results when one PMOS transistor is conducting (worst case) is

$$t_{PLH} = 0.69R_PC$$

$$= 0.69 \times \frac{30 \times 10^3}{p} \times C$$

and t_{PHL} is obtained by noting that the equivalent W/L of the discharge path is $4n/4 = n$ and thus

$$t_{PHL} = 0.69\ R_NC$$

$$= 0.69 \times \frac{12.5 \times 10^3}{n} \times C$$

For the case in which all p-channel devices have $W/L = p$ and all n-channel devices have $W/L = n$, we have

$$t_{PLH} = 0.69 \times \frac{30 \times 10^3}{p} \times C$$

which is the same as in the first case. However,

$$t_{PHL} = 0.69 \times \frac{12.5 \times 10^3}{n/4} \times C$$

$$= 0.69 \times \frac{4 \times 12.5 \times 10^3}{n} \times C$$

which is four times the value obtained in the first case.

14.59

$L = 0.13\ \mu\text{m},\ W_n = 0.2\ \mu\text{m},\ W_p = 0.4\ \mu\text{m},$

$n = 0.2/0.13,\ p = 0.4/0.13$

(a) Circuit (a) uses a six-input NOR gate and one inverter.

The six-input NOR requires:

6 NMOS transistors each with $W/L = n$

and

6 PMOS transistors each with $W/L = 6p$

The inverter requires

1 NMOS transistor with $W/L = n$

and

1 PMOS transistor with $W/L = p$

Thus,

$$\text{Area} = 6W_nL + 6 \times 6W_pL + W_nL + W_pL$$

$$= L(7\ W_n + 37\ W_p)$$

$$= 0.13(7 \times 0.2 + 37 \times 0.4)$$

$$= 0.13 \times 16.2 = 2.1\ \mu\text{m}^2$$

(b) Circuit (b) uses two three-input NOR gates and one two-input NAND gate.

Each three-input NOR gate requires

3 NMOS transistors, each with $W/L = n$

3 PMOS transistors, each with $W/L = 3p$

The two-input NAND gate requires

2 NMOS transistors, each with $W/L = 2n$

2 PMOS transistors, each with $W/L = p$

Thus,

$$\text{Area} = 2 \times 3 \times W_n L + 2 \times 3 \times 3 \times W_p L + 2 \times 2 \times W_n L + 2 \times W_p L$$

$$= L(10\ W_n + 20\ W_p)$$

$$= 0.13(10 \times 0.2 + 20 \times 0.4)$$

$$= 0.13 \times 10$$

$$= 1.3\ \mu\text{m}^2$$

Thus circuit (a) required $2.1/1.3 = 1.62$ times the area of circuit (b).

14.60

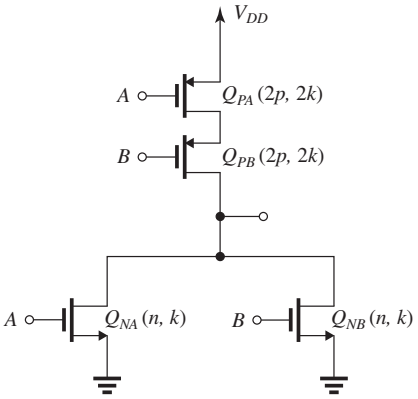

Figure 1

Refer to the circuit in Fig. 1. For Q_{NA} and Q_{NB}, (W/L) is equal to that of the NMOS transistor in the basic matched inverter. Thus,

$$k_{NA} = k_{NB} = k$$

For Q_{PA} and Q_{PB}, (W/L) is equal to twice the value of the PMOS transistor of the basic matched inverter. Since for the matched inverter $k_p = k_n = k$, here we have

$$k_{PA} = k_{PB} = 2k$$

(a)

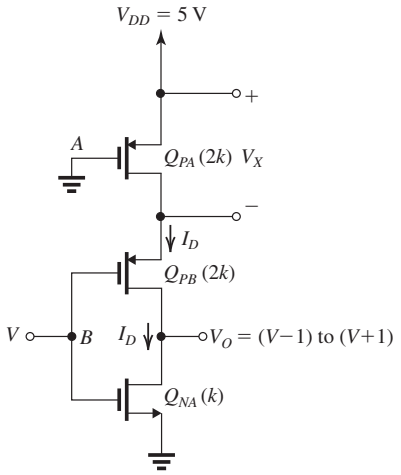

Figure 2

Figure 2 shows the circuit for the case input A is grounded. Note that Q_{NA} will be cut-off and has been eliminated. Switching will occur at $v_I = V$ which will be near $V_{DD}/2$. At this point, Q_{NB} and Q_{PB} will be in saturation and Q_{PA} will be in the triode region with a very small voltage V_X across it. All transistors will be conducting the same current I_D. For Q_{PA} we can write

$$I_D = 2k\left[(5-1)V_X - \frac{1}{2}V_X^2\right]$$

or

$$I_D = k(8\ V_X - V_X^2) \tag{1}$$

For Q_{PB} we can write

$$I_D = \frac{1}{2} \times 2k(5 - V_X - V - 1)^2$$

or

$$I_D = k(4 - V_X - V)^2 \tag{2}$$

Finally, for Q_{NB} we can write

$$I_D = \frac{1}{2}k(V-1)^2 \tag{3}$$

Next, we solve Eqs. (2) and (3) together to obtain V_X in terms of V. Equating Eqs. (2) and (3) gives

$$\pm\frac{1}{\sqrt{2}}(V-1) = 4 - V_X - V$$

$$\pm 0.707(V-1) = 4 - V_X - V \tag{4}$$

First try the solution corresponding to the + sign on the left-hand side of (4):

$$0.707(V-1) = 4 - V_X - V$$

$$\Rightarrow V_X = 4.707 - 1.707\ \text{V} \tag{5}$$

Since $V_X \simeq 0$, this equation gives

$$V = 2.75\ \text{V}$$

which is reasonable. The other solution gives

$$-0.707(V-1) = 4 - V_X - V$$

$$\Rightarrow V_X = 3.293 - 0.293\ \text{V}$$

For $V_X \simeq 0$, this equation gives

$$V = 11.2\ \text{V}$$

which is obviously impossible! Thus Eq. (5) is the solution that is physically meaningful. Next we substitute for V_X. From Eq. (5) into Eq. (1) to obtain

$$I_D = k\ 8(4.707 - 1.707\ \text{V}) - k(4.707 - 1.707\ \text{V})^2$$

$$= k(15.5 + 2.414\ \text{V} - 2.914\ \text{V}^2) \tag{6}$$

Equating this value of I_D to that in Eq. (3) gives

$$(V-1)^2 = 2(15.5 + 2.414\ \text{V} - 2.914\ \text{V}^2)$$

$$\Rightarrow 6.83\ \text{V}^2 - 6.83\ \text{V} - 30 = 0$$

$$\Rightarrow V = 2.65\ \text{V}$$

$$n = \frac{\ln 1200}{\ln e} = 7.09 \simeq 7$$

Thus, we use 7 inverters. The actual scaling factor required can be found from

$$x^7 = 1200$$

$$\Rightarrow x = (1200)^{1/7} = 2.75$$

The value of t_P realized will be

$$t_P = 7 \times 2.75CR$$

$$= 19.25CR$$

which represents a reduction in t_P by about 17.4%. Thus adding three inverters reduces the delay by 17.4%.

14.62 (a) Refer to Fig. 14.37(c). By inspection we see that

$$t_P = \tau_1 + \tau_2 + ... + \tau_{n-1} + \tau_n$$

But,

$$\tau_1 = \tau_2 = ... = \tau_{n-1} = xCR$$

and

$$\tau_n = \frac{R}{x^{n-1}} C_L$$

Thus,

$$t_P = (n-1)xRC + \frac{1}{x^{n-1}} RC_L \qquad \text{Q.E.D.} \qquad (1)$$

(b) Differenting t_P in Eq. (1) relative to x gives

$$\frac{\partial t_P}{\partial x} = (n-1)RC - \frac{(n-1)}{x^n} RC_L$$

Equating $\frac{\partial t_P}{\partial x}$ to zero gives

$$x^n = \frac{C_L}{C} \qquad \text{Q.E.D.} \qquad (2)$$

(c) Differenting t_P in Eq. (1) relative to n gives

$$\frac{\partial t_P}{\partial n} = xRC - \frac{1}{x^{n-1}} (\ln x) RC_L$$

Equating $\frac{\partial t_P}{\partial n}$ to zero gives

$$x^n \left(\frac{C}{C_L} \right) = \ln x \qquad \text{Q.E.D.} \qquad (3)$$

To obtain the value of x for optimum performance, we combine the two optimality conditions in (2) and (3). Thus

$$\ln x = 1$$

$$\Rightarrow x = e \qquad \text{Q.E.D.}$$

14.63 $E = CV_{DD}^2$

$$= 10 \times 10^{-15} \times 1.8^2 = 32.4 \text{ fJ}$$

For 2×10^6 inverters switched at $f = 1$ GHz,

$$P_D = 2 \times 10^6 \times 1 \times 10^9 \times 32.4 \times 10^{-15} \text{ x VDD^2}$$

$$= 64.8 \text{ W}$$

$$I_{DD} = \frac{P_D}{V_{DD}} = \frac{64.8}{1.8} = 36 \text{ A}$$

14.64 $P_{\text{dyn}} = fCV_{DD}^2$

$$= 2 \times 10^9 \times 5 \times 10^{-15} \times 1$$

$$= 10 \ \mu\text{W}$$

$$I_{DD} = \frac{10 \times 10^{-6}}{1} = 10 \ \mu\text{A}$$

14.65 Each cycle, the inverter draws an average current of

$$I_{\text{av}} = \frac{60 + 0}{2} = 30 \ \mu\text{A}$$

Since $I_{\text{av}} = 150 \ \mu$A, then the average current corresponding to the dynamic power dissipation is 120 μA. Thus,

$$P_{\text{dyn}} = 3.3 \times 120 \times 10^{-6} = 396 \ \mu\text{W}$$

But,

$$P_{\text{dyn}} = fCV_{DD}^2$$

Thus,

$$396 \times 10^{-6} = 100 \times 10^6 \times 3.3^2 \times C$$

$$\Rightarrow C = 0.36 \text{ pF}$$

14.66 Since P_{dyn} is proportional to V_{DD}^2, reducing the power supply from 5 V to 3.3 V reduces the power dissipation by a factor of $\left(\frac{3.3}{5} \right)^2 = 0.436$. The power dissipation now becomes $0.436 \times 10 = 4.36$ mW. Since P_{dyn} is proportional to f, reducing f by the same factor as the supply voltage (0.66) results in reducing the power dissipation *further* by a factor of 0.66, i.e.

Additional savings in power $= (1 - 0.66) \times 4.36$

$$= 1.48 \text{ mW}$$

14.67 $t_{PLH} = 30$ ns, $t_{PHL} = 50$ ns

$$t_P = \frac{1}{2}(30 + 50) = 40 \text{ ns}$$

$$P_{D\text{av}} = \frac{1}{2}(1 + 0.6) = 0.8 \text{ mW}$$

$$PDP = 0.8 \times 10^{-3} \times 40 \times 10^{-9} = 32 \text{ pJ}$$

Thus,

$$\text{Area} = 2 \times 3 \times W_n L + 2 \times 3 \times 3 \times W_p L + 2 \times 2 \times W_n L + 2 \times W_p L$$

$$= L(10\ W_n + 20\ W_p)$$

$$= 0.13(10 \times 0.2 + 20 \times 0.4)$$

$$= 0.13 \times 10$$

$$= 1.3\ \mu\text{m}^2$$

Thus circuit (a) required $2.1/1.3 = 1.62$ times the area of circuit (b).

14.60

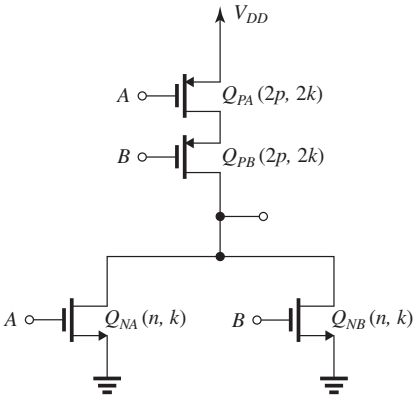

Figure 1

Refer to the circuit in Fig. 1. For Q_{NA} and Q_{NB}, (W/L) is equal to that of the NMOS transistor in the basic matched inverter. Thus,

$$k_{NA} = k_{NB} = k$$

For Q_{PA} and Q_{PB}, (W/L) is equal to twice the value of the PMOS transistor of the basic matched inverter. Since for the matched inverter $k_p = k_n = k$, here we have

$$k_{PA} = k_{PB} = 2k$$

(a)

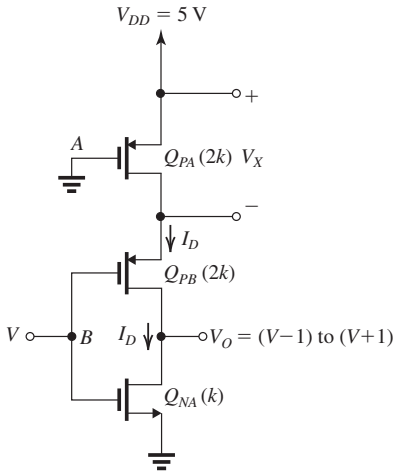

Figure 2

Figure 2 shows the circuit for the case input A is grounded. Note that Q_{NA} will be cut-off and has been eliminated. Switching will occur at $v_I = V$ which will be near $V_{DD}/2$. At this point, Q_{NB} and Q_{PB} will be in saturation and Q_{PA} will be in the triode region with a very small voltage V_X across it. All transistors will be conducting the same current I_D. For Q_{PA} we can write

$$I_D = 2k\left[(5-1)V_X - \frac{1}{2}V_X^2\right]$$

or

$$I_D = k(8\ V_X - V_X^2) \tag{1}$$

For Q_{PB} we can write

$$I_D = \frac{1}{2} \times 2k(5 - V_X - V - 1)^2$$

or

$$I_D = k(4 - V_X - V)^2 \tag{2}$$

Finally, for Q_{NB} we can write

$$I_D = \frac{1}{2}k(V-1)^2 \tag{3}$$

Next, we solve Eqs. (2) and (3) together to obtain V_X in terms of V. Equating Eqs. (2) and (3) gives

$$\pm\frac{1}{\sqrt{2}}(V-1) = 4 - V_X - V$$

$$\pm 0.707(V-1) = 4 - V_X - V \tag{4}$$

First try the solution corresponding to the + sign on the left-hand side of (4):

$$0.707(V-1) = 4 - V_X - V$$

$$\Rightarrow V_X = 4.707 - 1.707\ \text{V} \tag{5}$$

Since $V_X \simeq 0$, this equation gives

$$V = 2.75\ \text{V}$$

which is reasonable. The other solution gives

$$-0.707(V-1) = 4 - V_X - V$$

$$\Rightarrow V_X = 3.293 - 0.293\ \text{V}$$

For $V_X \simeq 0$, this equation gives

$$V = 11.2\ \text{V}$$

which is obviously impossible! Thus Eq. (5) is the solution that is physically meaningful. Next we substitute for V_X. From Eq. (5) into Eq. (1) to obtain

$$I_D = k\ 8(4.707 - 1.707\ \text{V}) - k(4.707 - 1.707\ \text{V})^2$$

$$= k(15.5 + 2.414\ \text{V} - 2.914\ \text{V}^2) \tag{6}$$

Equating this value of I_D to that in Eq. (3) gives

$$(V-1)^2 = 2(15.5 + 2.414\ \text{V} - 2.914\ \text{V}^2)$$

$$\Rightarrow 6.83\ \text{V}^2 - 6.83\ \text{V} - 30 = 0$$

$$\Rightarrow V = 2.65\ \text{V}$$