USAF Academy
Department of Electrical and Computer Engineering
ECE 321 – Electronics I

The Digital Lab - Part B

Objective: To illustrate and reinforce operational and modeling concepts of the CMOS used as digital inverters, logic gates, and SR Latches.

Authorized Resources: 1) ECE321 class handouts, 2) course texts, 3) lab and equipment manuals, and 4) simulation handouts.

Collaboration Policy: Cadets may collaborate regarding the theory relevant to this experiment and on the operation/use of software and hardware. Cadets must design and develop their own experiments, take their own data and measurements, and perform their own analysis and conclusions. Proper documentation is required per USAFA policy.

Due date: Your completed Lab Notebook for this exercise is due IAW the syllabus.

Grading: This lab is a significant component of overall lab grade for the course. See the syllabus for weightings.

Lab Notebook Format: Your final lab submission will be a "**Design Exercise**" format. However, the "Inverter Lab" will follow the "**Traditional Experiment**" format since we give you the schematic/design up front.

Part A. Inverter. This lab consists of three parts. In Part A, you built and tested CMOS inverters.

Part B. Logic Gates. In this Part B, you will design, simulate, and build a simple CMOS logic gate to perform a particular function.

Part C. SR Latch. This Part C adds an SR-Latch to the circuit to demonstrate the basic operation of memory. Reference handout on course website when available.

Important: Each part requires a graded Prelab. You will turn this in at the start of each lesson for a grade so be sure to keep a copy for your use in lab.

Part B. Logic Gate

Design a CMOS logic circuit that will accept three digital signals (call them A, B, and C) from a counter chip. Signal A is the most significant bit of the three-bit counter and signal C is the least significant bit. Another way to think about this is that signal B is twice as fast as signal A and signal C is twice as fast as signal B. The input to the counter is a pulsed clock signal from a function generator (or other source). The counter will give you a three bit cycling binary set of bits from 0 to 7 and repeating.

Your circuit must use these three signals and produce two logical outputs (call them F1 and F2). You will use these outputs in Part C.

The two outputs F_1 and F_2, are "bit-streams" and must look like:

F_1 = …000100000001000000010000000010000…
F_2 = …000000010000000100000001000000001…

or

F_1 = …111011111110111111101111111011111…
F_2 = …111111101111111011111110111111110…

This particular logic family uses LOGIC HIGH = 6 V and LOGIC LOW = 0 V. The load to your logic circuit will be capacitive and should be 1.0 nF.

Use BS170 and BS250 transistors and an SGS-Thompson HCF40161B CMOS binary counter or a 74LS161. The HCF40161B counter data sheet is on the Course Website or online at

http://pdf1.alldatasheet.com/datasheetpdf/view/22315/STMICROELECTRONICS/HCF40161B.html.

Some things that you should do are:

Simulate and measure the worst-case propagation delay times (t_{PLH} and t_{PHL}) for your logic gates. Make sure you clearly indicate, in your notebook, how you are obtaining your data. Note you do not have the ability to modify either W or L for your circuit. How do these values compare with those of the basic inverter you created?

You do not need to measure V_{IH}, V_{OH}, N_{MH}, N_{ML}, V_{IL}, V_{OL} and you do not need to create a VTC. Explain why a VTC would not make sense?

Predict/Simulate/Measure timing diagrams that show all inputs and outputs. Use pictures/graphs to indicate things like worst-case propagation paths.

Simulation Hints:

- Use PSPICE (or Multisim) to simulate the behavior of your gate(s). Verify your circuit executes the logical function for which it was designed. You can either get a part similar to the 161 counter used in hardware, or you may use several VPULSE sources to "create" the counter outputs for the simulation. If you use a real 161, you will need to make the power pins visible in the schematic and connect them to the higher than normal supply levels. (6 V instead of 5 V or 3 V)

- Make sure your plots show both inputs and outputs. Include in your notebook sufficient information so all recorded data could be taken again, if needed.

Hardware Hints:

- Know exactly what you need to measure before you start building your circuit.
- Use a SGS Thompson HCF40161B CMOS binary counter to generate your logic gate inputs. The function generator will provide the input to the counter chip.
- You will need to build/use one or more inverters in addition to your logic circuit.
- Build your circuit incrementally. Get your counter working first. Verify the outputs are doing what you expect. Then, add your logic one piece at a time and verify that it works as desired and predicted.
- Be neat with your wiring. Many cadets build everything at once and then typically will spend many hours trying to figure out why their circuit doesn't work.
- Lay out your circuit in your notebook first so you have an idea of physically what your board will look like.
- Do not leave a transistor's gate input unconnected. Results will be unpredictable.
- Ensure the drain and source pins are correct. Remember that discrete devices have the "back diode" and are not symmetrical.

Limit the speed of operation (frequency) of your complete circuit to prevent the power supply's ammeter from exceeding 200 mA. Why is this a concern? Recall information from the Part A.