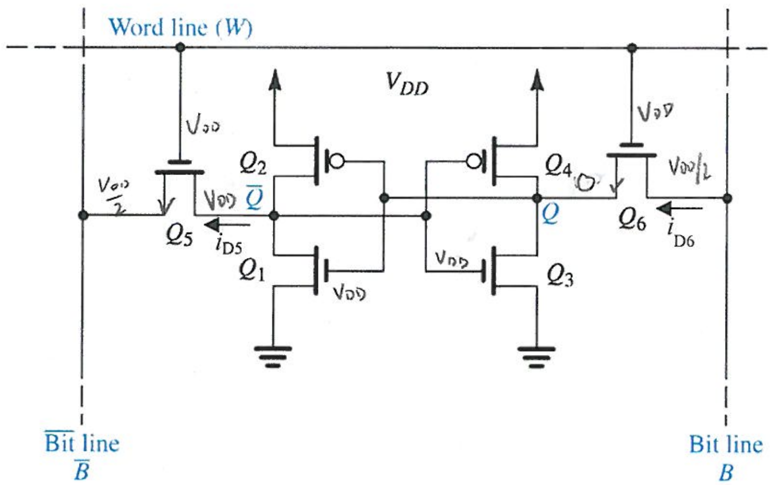
Name Solution

Section ________

1. In the figure below the voltage at Q represents the value stored in the cell and the voltage at $\bar{Q}$ represents the complement of the stored value. Suppose that the cell stores a '0'. Consequently, $v_Q = 0\ V$ and $v_{\bar{Q}} = V_{DD}$. Prior to the word line being raised to V_{DD}, both Bit and $\overline{Bit}$ are pre-charged to $\frac{V_{DD}}{2}$. Note that this is different from the text where they are pre-charged to V_{DD}. As is common, $V_{tn} = -V_{tp} = 0.2\ V_{DD}$.



a. Determine the voltages and currents for the table below ***immediately*** after the word line is raised to V_{DD}. Also determine the condition of the transistor (Off, On-Triode, On-Saturation) for each. If $|v_{GS}| > |V_t|$, but $|v_{DS}| = 0$, record the condition as On-No current. Remember that for NMOS transistors, $v_S < v_D$.

Transistor	$\lvert v_{GS}\rvert$	$\lvert v_{GS}\rvert - \lvert V_t\rvert$	$\lvert v_{DS}\rvert$	Condition
Q_3	V_{DD}	$V_{DD} - V_t$	0	On-No current
Q_5	$V_{DD}/2$	$V_{DD}/2 - V_t$	$V_{DD}/2$	On-Sat
Q_6	V_{DD}	$V_{DD} - V_t$	$V_{DD}/2$	On-Triode

b. Solve for i_{D5} and i_{D6} as a function of k for the access transistors, $k_a = k_n'\left(\frac{W}{L}\right)_a$, and V_{DD}. (Ignore channel-length modulation.) Simplify your answer.

$$i_{D5} = \frac{1}{2} K_a \left(\frac{V_{DD}}{2} - V_t\right)^2 = \frac{1}{2} K_a (0.5 V_{DD} - 0.2 V_{DD})^2 = \frac{1}{2} K_a V_{DD}^2 \cdot 0.09$$

$$= K_a V_{DD}^2 \cdot 0.045$$

$$i_{D6} = K_a\left[(V_{DD} - V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

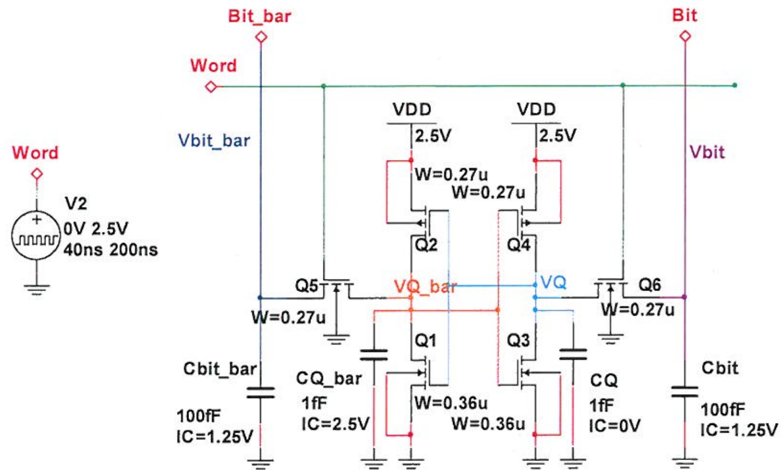
$$= K_a\left[(0.8 V_{DD})(0.5 V_{DD}) - 0.125\ V_{DD}^2\right]$$

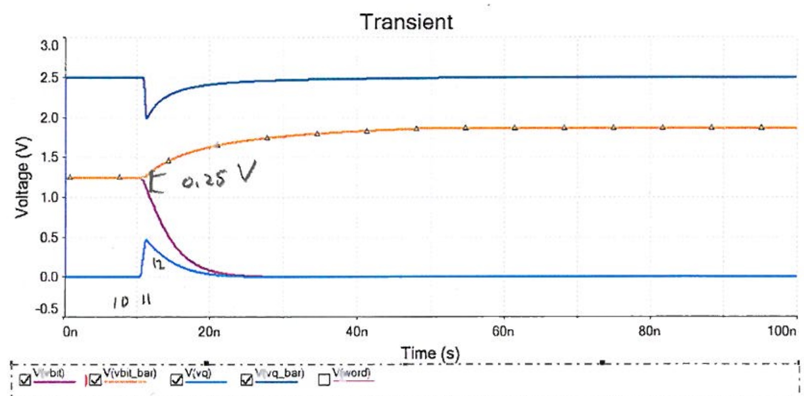
$$= K_a (0.4 - 0.125) V_{DD}^2$$

$$= K_a V_{DD}^2\ 0.275$$

On: $|v_{GS}| > |V_t|$; Triode: $|v_{DS}| \le |v_{GS}| - |V_t|$ or $|v_{GD}| > |V_t|$; $i_D = k\left[(|v_{GS}| - |V_t|)|v_{DS}| - \frac{1}{2}v_{DS}^2\right]$;
Saturation: $|v_{DS}| \ge |v_{GS}| - |V_t|$ or $|v_{GD}| < |V_t|$; $i_D = \frac{k}{2}(|v_{GS}| - |V_t|)^2(1 + \lambda|v_{DS}|)$

2. The figures below show the same circuit in Multisim performing the read operation. Four voltages are shown in the waveform diagram. The Word line is raised to V_{DD} at t=10 ns, with a 1-ns rise time. The magnitude of the threshold voltages for all transistors is 0.2 V_{DD}. $\mu_n = 2.5\,\mu_p$





a. Explain why V(vbit) falls faster than V(vbit_bar) rises. (if your answers to part b are correct these equations give you the answer, but you could think it through without the equations too).

The drive on Q_5 is much smaller so even though it is in saturation its current is smaller than that of Q_6 => V_{bit} falls faster

Current is about 6x bigger in Q_6

b. Briefly explain why V(vbit) falls all the way to 0 V, while V(vbit_bar) only rises to 1.9 V.

– Degraded level Q_5 turns off when $V_{bit\_bar} = V_{DD} - V_t$

c. If the sense amplifier has a differential gain of 10 V/V, estimate the time required for a read from this memory. Hint: the outputs of the sense amplifier should be at the supply rails which implies $v_{bit} - v_{\text{bit\_bar}} = 0.25$ V

looks like about 2ns after word starts to rise

1ns after word reaches V_{DD}

$$\frac{(W/L)_a}{(W/L)_n} \le \frac{1}{\left(1 - \frac{V_{tn}}{V_{DD} - V_{tn}}\right)^2} - 1 \qquad \frac{(W/L)_p}{(W/L)_a} \le \left(\frac{\mu_n}{\mu_p}\right)\left[1 - \left(1 - \frac{V_{tn}}{V_{DD} - V_{tn}}\right)^2\right]$$