USAF Academy
Department of Electrical and Computer Engineering
ECE 321 – Electronics I

The Amplifier

Objective: To illustrate and reinforce operational and modeling concepts of metal-oxide-semiconductor field-effect transistors (MOSFETs) used as analog amplifiers.

Authorized Resources: 1) ECE 321 class handouts, 2) course texts, 3) lab and equipment manuals, and 4) simulation handouts.

Collaboration Policy: Cadets may collaborate regarding the theory relevant to this experiment and on the operation/use of software and hardware. Pre-labs 1 and 3 will be completed as individual effort. You may consult either course instructor for assistance as needed. Pre-lab 2, demonstration of the Part A circuit, will be completed as a group. Your final submission, notebook and formal report, with all sections of the Design Laboratory Report, will be done in your two- or three-person group. Proper documentation is required per USAFA policy.

Due Date: Your Lab Notebooks and final report for this exercise is due IAW the syllabus.

Grading: This lab is a significant component of overall lab grade for the course. See the syllabus for weightings.

Overview: In this lab you will demonstrate the concepts of the field-effect transistor with application as an amplifier. Your overall task will be to design, build, and test the circuit(s) described on the following pages.

Start this lab (and all others) by reading over the entire lab before you do anything else. You must have a good idea of what you'll be doing before you start. Keep your lab notebook in the "**Design Exercise**" format. See the lab notebook handout to find out what should be included in this lab. Missing sections because of ignorance is not an excuse. Notebook details will also be given for each of the parts to this lab.

Part A. Single-Stage Amplifier. Design a Common Source amplifier with Source Resistor to meet specifications.

Part B. Cascaded Amplifiers. Design a Common Source amplifier with Source Resistor cascaded with a Common Drain amplifier to meet specifications.

Important: Each part requires a graded Pre-lab. You will turn this in at the start of lab days 1 and 3 for a grade so be sure to keep a copy for your use in lab.

Part A. Single Stage Amplifier

Specifications and Limitations

- Circuit Topology: Common-source with source resistor (See Figure 1 for topology)
- Transistor: BS-170 MOSFET
- V_{DD} from 10 to 20 V ($10V \leq V_{DD} \leq 20V$)
- Maximum drain current: 75% of the max transistor DC current (from data sheet)
- Input Resistance (R_i): $\geq$ 100 kΩ
- Output Resistance (R_{out}): $\leq$ 5 kΩ
- Load Resistance (R_L): 100 kΩ (AC-coupled using 10 µF - 47µF electrolytic capacitor)
- v_{in}: 1kHz sine wave – AC-coupled (10µF - 47µF electrolytic capacitor)
- Voltage Gain (A_v): -3 V/V $\geq A_V \geq -30$ V/V (no visible signal distortion)
- v_{out}: Should achieve at least 3 $V_{p\text{-}p}$ with no visible distortion
- Instantaneous power dissipation in any part not to exceed 75% of max power dissipation
- Potentiometers may not be used for any part of the design

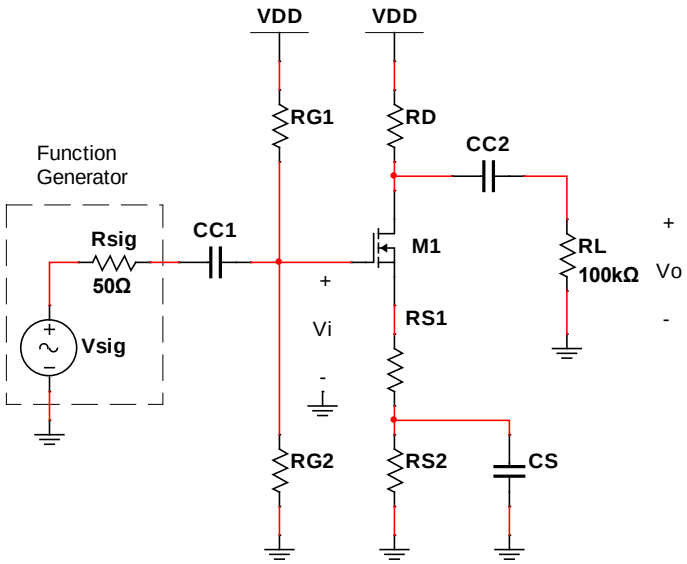

Figure 1. Common-source amplifier with source resistor using NMOS FET biased with the classical 4-resistor scheme.

Question – What does C_S do? Explain in your notebook what it does.

General lab process

- Objective in notebook
- Circuit specifications in notebook, as you understand them
- Develop your approach to the design and your testing approach
  The design approach should be based on the specifications, preferrably symbolically. It should not include numerical values of any component or signal descriptor, like voltages and currents. Once complete, you should be able to follow the design process by substituting numerical values from specifications and standard component values adopted from calculations of non-standard values. The process of determining actual component values is separate from creation of the design approach. Similarly, the design of the test is a separate activity from the actual testing and collection of measurement data. Keep approaches separate from design and test results.
- Apply your approach to determine component values. This is the first part of designing your circuit.
- Simulate your circuit(s) and re-design, if needed. Simulation is second part of the design.
- Determine actual transistor properties via curve tracer
- Build your circuit(s)
- Measure operating point
- Re-design or repair circuit as needed
- Follow testing approach taking data for analysis and confirmation of success
- Analyze data. Compare hand calculations, simulations and test results. Include tables with percent errors. Quantify error analysis.
- Write conclusion

Modifications to your working design

- Change the load resistance from very large to small (starting point of 100 kΩ to 10 kΩ then 1 kΩ then 100 Ω) and observe the effect on the gain. How is the gain affected by the size of the load resistance? Can you explain why? Make sure you replace the load with the original load resistor when finished.

- What happens if you eliminate one or both of the coupling capacitors, C_{C1} and C_{C2}?

- What happens to gain if you double (or halve) the value of R_S (or R_{S1}) and R_D?

- Answer the questions above and demonstrate that your circuit meets all specifications in your validation-testing notebook section. Also discuss these topics in the analysis/conclusion of the report.

Curve Tracer Notes

GOAL: Obtain a family of V_{DS}, I_D, and V_{GS} curves for your transistor.

1. Determine the threshold voltage V_t. You will probably have to adjust the curve tracer settings to accurately estimate this value. When drain currents is below 100 μA, the transistor can reasonably be considered off.
2. Determine the transistor output resistance (r_o) and the Early Voltage (V_A) at your target design DC bias point. One method is to find two points on a V_{GS} trace, and then find the slope and determine where that line crosses the 0-current point.
3. Determine a value for g_m.
4. Curve tracer graphs can be saved to floppy disk and transferred to your computer via the USB floppy drives provided in the lab.
5. For the transistor you are using, W and L are constant. k_n' is a function of several things including mobility which is a function of I_D and the carrier concentration which is a function of V_{GS}. Use appropriate equations to determine/estimate $k_n' W/L$.

Hardware protoboard notes

- Use your protoboard to build and test your circuit. As you build and verify, include a schematic of the actual circuit you build. You should be able to re-create any circuit and test based solely on your notebook.

Simulation notes

- Review your Testing Approach section. Make sure that you include in your notebook sufficient information to demonstrate/verify your circuit works correctly and meets all specifications. Many people use the top of a notebook page for schematics and explanations while saving the bottom part of the page for pictures/graphs. You **must** simulate your design to verify your circuit meets specs before attempting to build your circuit.

- If you would like to use the values from the curve tracer in simulation, you will have to modify the model parameters as discussed in class.

- **Using MultiSim for simulation**. In MultiSim, enter the values for k_n', V_{tn} and λ you developed on Day 1. To do this, right click on the part and select Properties > Edit Model from the "Value" tab. Note: MultiSim uses the variable name KP for k', the process transconductance parameter for both NMOS and PMOS device statements. KP does not mean the "k" for a PMOS; it means "k"-prime. The units of KP are in Amps/Volt^2. MultiSim uses VTO for the threshold voltage of both NMOS and PMOS devices. Multisim uses LAMBDA for channel λ or channel length modulation. You can set the ratio Width/Length on the "Value" tab, but since you don't know this first-hand you can elect to use 1/1.

- **Using PSpice for simulation**. In PSPICE, add the following line to your existing SPICE library (Or create an entirely new library file). Enter the values for k_n', V_{tn} and λ you developed on Day 1. Note: PSPICE uses the variable name Kp (or KP, or kp; PSPICE does not care about case) for k', the process transconductance parameter for both NMOS and PMOS device statements. Kp does not mean the "k" for a PMOS; it means "k" prime. The units of KP are in Amps/Volt^2. SPICE uses VTO for the threshold voltage of both NMOS and PMOS devices. PSPICE uses LAMBDA for channel λ or channel length modulation.

Example Model Statement (PSpice only)

.model my_nmos NMOS (KP=25m W=1 L=1 VTO=2.1 LAMBDA=2m)
*$

Next, create your schematic, using the MbreakN, (or MBreakP), symbol from the BREAKOUT library to represent your FET. Connect the body terminal to the source if using the 4 terminal device. You could also use MbreakN3 if you want the body source connection to already be done for you. Use the Property Editor to change *both* the VALUE and IMPLEMENTATION of the transistor model to whatever you named your part. Finally, make sure your simulation "Sees" your library by adding, if needed, the library file to your library list.

If your simulations show excessive power dissipation in any component, you must re-design your circuit.

Part B. Cascaded Amplifiers

Specifications & Limitations

- Circuit Topology: Common-source with source resistor cascaded with a common-drain (See Figure 2 for topology). Make sure they are AC coupled – C3!
- Transistor: BS-170 and BS-250
- V_{DD} from 10 to 20 V ($10V \leq V_{DD} < 20V$)
- Maximum drain current: 75% of the max transistor DC current (from data sheet)
- Input Resistance (R_i): $R_i \geq 100\ k\Omega$
- R_i of the PMOS $\geq 100\ k\Omega$
- Output Resistance (R_{out}): $R_{out} \leq 5\ k\Omega$
- Load Resistance (R_L): 50 Ω (AC coupled using 10 µF–47µF electrolytic caps)
- v_{in} : 1kHz sine wave -- AC coupled (10µF – 47µF Electrolytic cap)
- Voltage Gain (A_V): -3 V/V ≥ A_V > -30 V/V (no visible signal distortion)
- v_{out}: The amplifier should be able to supply at least 3 V_{p-p} with no visible distortion
- Instantaneous power dissipation in any part may not exceed 75% of max power dissipation specified for the part
- Potentiometers may not be used for any part of the design.
- V_{SD} of PMOS ~7 Volts (or roughly ½ the supply voltage)
- I_D of PMOS ~60 mA

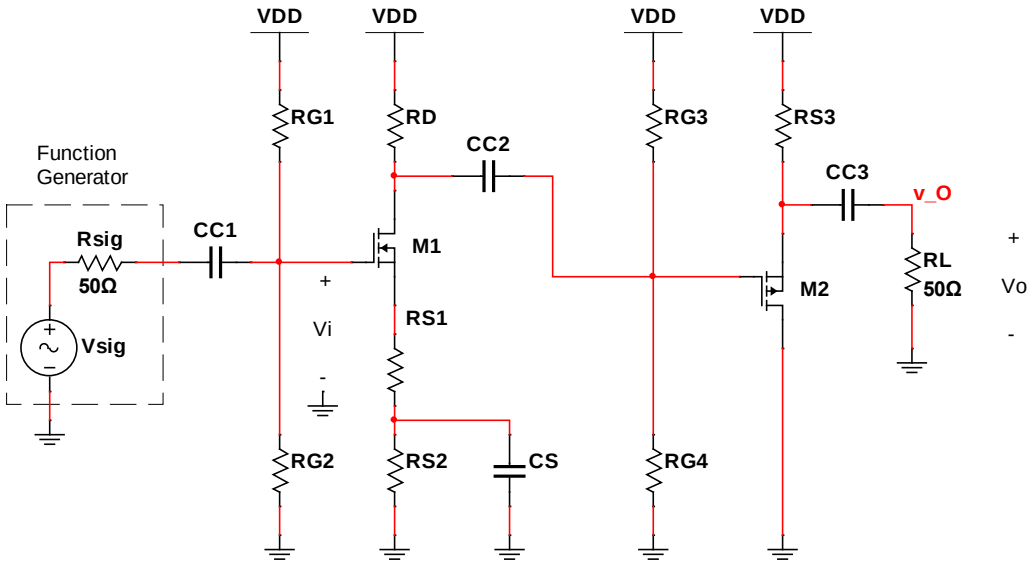

Figure 2. Common-source amplifier with source resistor using NMOS FET biased with the classical 4-resistor scheme, cascaded with common-drain using PMOS FET biased with classical 4(3+1wire)-resistor scheme.

You must size R_{G3}, R_{G4}, R_{S3} to achieve the PMOS bias point and to achieve a total circuit A_V as specified above. Demonstrate that your new circuit meets all the specifications.

Questions to answer in your analysis:

1) Why can the new configuration achieve the desired A_v into the 50 Ω load when the common-source amplifier of Part A by itself cannot?
2) How low can R_L get and still have a non-distorted output (symmetrical about zero volts and/or not clipped)?
3) What could you change in the new circuit to achieve the correct output into a smaller R_L? Note: Don't actually do this on the real circuit as you might exceed wattage rating. Just simulate results in Multisim.
4) What would happen to the total circuit gain if the R_{in} of the pMOS (Source Follower) was $\leq$ 100 kΩ

Bonus:

Discuss techniques and determine harmonic distortion/measure of non-linearity for your amplifier circuit.

Need to update this part.
Grading Rubric

(See Course Webpage for tips to getting better lab grades)

Notebook: Objectives / Specifications / Limitations _____ **/10**

Notebook: Approach and Design _____ **/30**

Notebook: Simulations _____ **/20**

Prelab A: Design, Simulation, and Test Plan of Part A _____ **/30**

Prelab B: Demonstration of Part A in lab _____ **/30**

Prelab C: Design, Simulation, and Test Plan of Part B _____ **/30**

Notebook: Implementation and Testing _____ **/20**

FORMAL: (130 pts)

Analysis _____ **/80**

Conclusion _____ **/30**

Peer Reviewed Version included and used _____ **/20**

Peer Reviewed by:_____

BONUS: (15) _____

Total Points Awarded: _____ **/300**