USAF ACADEMY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ECE 321
Electronics I
Fall 2016
Graded Review #2

ACADEMIC TESTING MATERIAL

ACADEMIC SECURITY: This examination is not released from academic security until 1630 on Tuesday, 8 Nov 2016. Until this time, you may not discuss the examination contents or the course material with anyone other than your instructor.

INTEGRITY: Your honor is extremely important. This academic security policy is designed to help you succeed in meeting academic requirements while practicing the honorable behavior our country rightfully demands of its military. Do not compromise your integrity by violating academic security or by taking unfair advantage of your classmates.

AUTHORIZED RESOURCES: One 8 ½" x 11" sheet of paper with writing on both sides; any calculator.

- You have 90 minutes.
- Box your final answer where appropriate.
- Show all work to qualify for partial credit.
- Organize your work. Your instructor must be able to follow your solution process.
- Use engineering notation with three significant figures.

PROBLEM	VALUE	EARNED
1 Knowledge/Comprehension	40	
2 Comprehension/Application	40	
3 Analysis	40	
4 Analysis	40	
5 Design	40	
Total	200	

NAME Solution SECTION_____

Multiple Choice General Knowledge

1. (40 points - 8 points each)

1.1 A pMOS transistor ($V_t = -2.7$ V) is biased with $V_{GS} = -4.1$ V and $V_{DS} = -10.0$ V is in

a) cutoff
b) triode
c) saturation
d) active
e) none of the above

$|V_{GS}| > |V_t|$ and $|V_{GS} - V_t| < |V_{DS}|$
on sat.

1.2 An nMOS transistor ($V_t = 2$ V) biased with $V_{GS} = 3.5$ V and $V_{DS} = 1.5$ V is

a) at the boundary between cutoff and saturation regions
b) at the boundary between triode and saturation regions
c) at the boundary between cutoff and triode regions
d) correctly biased as an amplifier, in the middle of the saturation region
e) biased in triode region, far from saturation

$V_{GS} > V_t$ $V_{GS} - V_t = V_{DS}$

1.3 A high input resistance, low output resistance, and a voltage gain slightly less than 1 best describes a

a) common gate amplifier.
b) common drain amplifier
c) common source amplifier
d) common collector amplifier
e) none of the above

1.4 You couple a 100 kHz signal to your common-source amplifier with input resistance $R_{in} = 1$ MΩ. An appropriately sized coupling capacitor ($|Z_C| \ll R_{in}$) is

a) 1.5 pF ($1.59 \cdot 10^{-12}$ F)
b) 50 pF ($50.0 \cdot 10^{-12}$ F)
c) 1.5 fF ($1.59 \cdot 10^{-15}$ F)
d) 10 fF ($10.0 \cdot 10^{-15}$ F)
e) none of the above

$Z_{c\ 1.5pf} = \frac{-j}{2\pi \cdot 100k \cdot 1.5pF} = -j\,1.06\,M\Omega$ too big

1.5 The small signal approximation below ensures mostly linear operation in saturation. **Hint:** from the saturation equation, the small signal can be expressed as $i_d = k(V_{OV})v_{gs} + \frac{1}{2}kv_{gs}^2$

a) $v_{gs} \ll \frac{1}{2}V_{OV}$
b) $v_{gs} \ll V_{OV}$
c) $v_{gs} \ll 2V_{OV}$
d) $v_{gs} \ll 4V_{OV}$
e) none of the above

$g_m = \frac{\partial i_d}{\partial v_{gs}} = kV_{OV} + kv_{gs} \simeq kV_{OV}$

$kV_{OV}v_{gs} >> \frac{1}{2}kv_{gs}^2 \Rightarrow v_{gs} << 2V_{OV}$

MOSFET Descriptors - Short Answer

2. (40 pts - 10 points each)

2.1 The transconductance parameter, k, is given by $\mu C_{ox}\left(\frac{W}{L}\right)$. Choose the width of the **pMOS, W_p,** given a width W_n for the nMOS, to achieve the same drain current if the electron and hole mobilities, μ_n and μ_p, are 1000 and 400 cm²/V-s respectively. Assume the same L, C_{ox}, and $|V_t|$ for each. Your answer should be in terms of W_n.

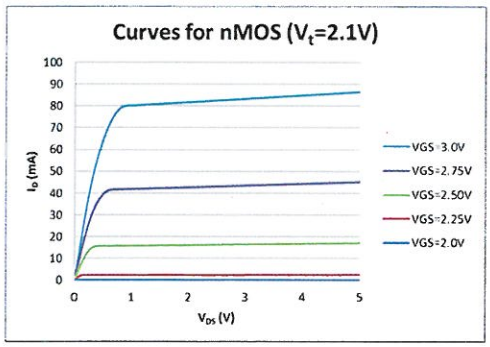
$$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p \Rightarrow 1000\, W_n = 400\, W_p$$

$$W_p = 2.5\, W_n$$

2.2 The oxide capacitance C_{ox} describes the capacitance per unit area between the gate and the semiconductor body in the MOS structure. Knowing that $C = \frac{\Delta Q}{\Delta V}$ describes the change in charge Q due to a change in voltage V, **describe why** increasing capacitance increases drain current in the MOSFET. **Hint**: think about carriers and charge in the channel.

$\Delta Q = C\Delta V \Rightarrow$ Therefore increasing C increases charge (concentration) for the same voltage. As charge concentration increases current increases (for same electric field).

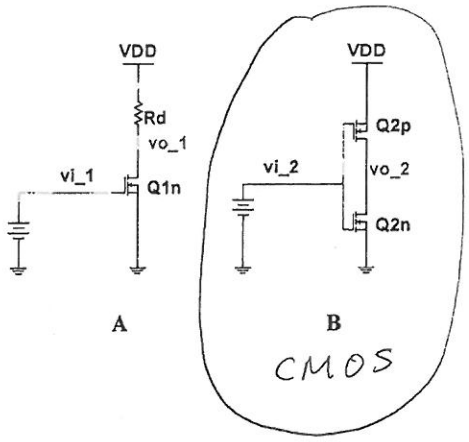
2.3 The transconductance gain, g_m, is defined as $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}}$. Using the family of curves below **conceptually describe** the meaning of g_m.



g_m describes how current changes as v_{gs} changes (and v_{DS} is held constant)

To evaluate g_m at a point start with v_{gs} and i_d at some values say $v_{DS} = 2.5V$ and $v_{GS} = 2.75\ V \Rightarrow i_D \cong 42$ mA. Increasing v_{GS} to 3.0 V gives $i_D = 82$mA. Decreasing v_{GS} to 2.5V gives $i_D = 17$ mA $\Rightarrow$ $g_m = \frac{82mA - 17mA}{3.0V - 2.5V} = \frac{65mA}{0.5V}$ or 130mA/V

2.4 The figures below show a "resistively loaded inverter" and a "CMOS inverter". **Circle** the "CMOS inverter". V_{DD} = 2.5 V; R_d = 48 kΩ; for both types of transistors, $r_{ds} \cong$ 2 kΩ when $|V_{GS}| = V_{DD}$ and $V_{DS} \leq$ 0.5 V. **Calculate** static power dissipation for each type inverter when the output is low, and, when the output is high. **Contrast** static power dissipation P_D for the two inverters.



Power Dissipation		
	Resistive Load	**CMOS**
$V_O=V_{OL}$	125 μW	0
$V_O=V_{OH}$	0	0

For CMOS $I_D = 0$ under both conditions

$\Rightarrow P_{static} = 0W$

For resistive load $I_D = 0$ when nMOS is off or $V_O = V_{OH}$. But when nMOS is on $r_{ds} = 2k\Omega \Rightarrow I_D = \frac{V_{DD}}{48K+2K} = \frac{2.5}{50K} = 50\mu A$

$P_D = V_{DD} I_D = 2.5V \cdot 50\mu A = 125\mu W$

$\Rightarrow$ CMOS has no static power dissipation

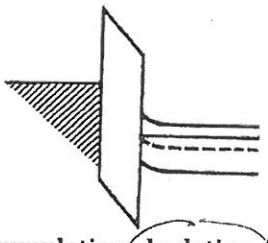
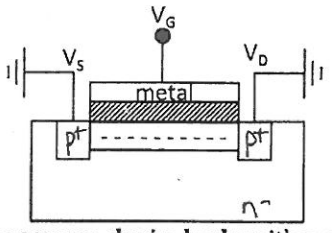
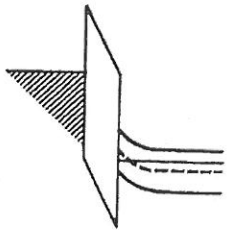
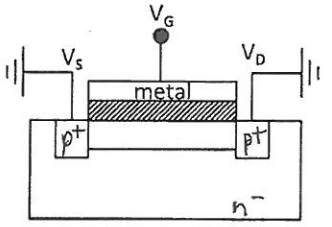
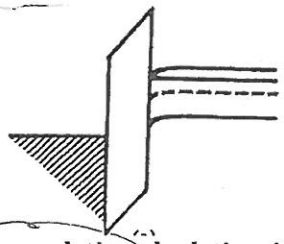
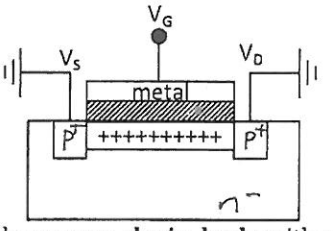
Resistive load has no static power 1/2 of the time but 125μW when $V_O = V_{OL}$. Assuming inverters have $V_O = V_{OL}$ 1/2 of the time. The average power dissipation of resistively loaded inverters in 62.5μW each.

MOSFET Physics - Analysis

3. (40 pts) The figure below shows **energy band diagrams** on the left for an MOS and concept of a different **channel types** that form under the oxide on the right.

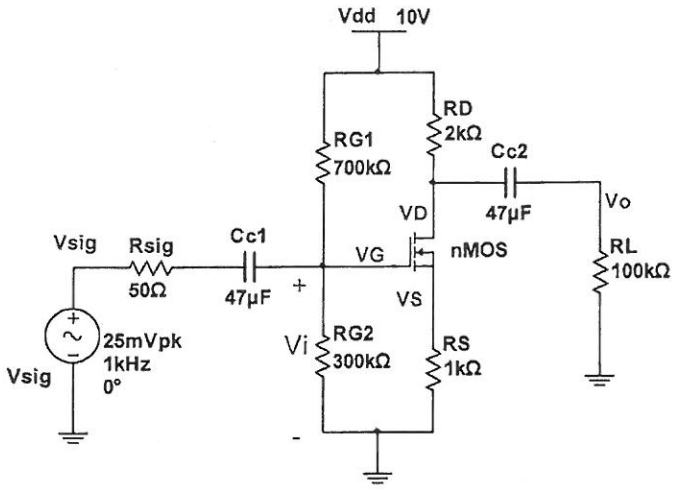
- 3.1. (15 pts, 5 each) Match the **energy band diagram** (letter) with **channel type** (#) of the MOS structure using the spaces provided. Positive symbols (+) indicate holes while negative (-) indicate electrons. Use the labeled spaces in the diagrams to match them.
- 3.2. (9 pts, 3 each) In each circle whether the energy band diagram shows **accumulation**, **depletion**, or **inversion**.
- 3.3. (6 pts, 2 each) In each indicate the type (**n** or **p**) for the **drain** and **source** regions.
- 3.4. (6 pts, 2 each) In each indicate the type (**n** or **p**) for the **body**.
- 3.5. (4 pts) Circle the polarity of the **threshold voltage** for this structure.

$V_t < 0$ **$V_t > 0$**

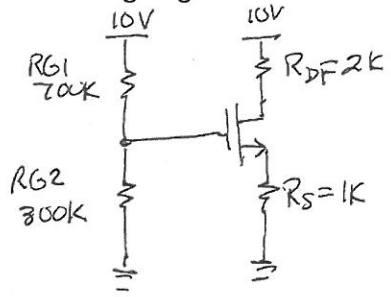
Energy Band Diagram	MOS Channel
A.  2 Channel Circle: **accumulation** **depletion** **inversion**	1.  Label the **source**, **drain**, **body** with n or p.
B.  3 Channel Circle: **accumulation** **depletion** **inversion**	2. A  Label the **source**, **drain**, **body** with n or p.
C.  Channel Circle: **accumulation** **depletion** **inversion**	3. B  Label the **source**, **drain**, **body** with n or p.

MOSFET Amplifier Analysis – Large and Small Signal

4. (40 pts) The nMOSFET below uses a classical, four-resistor biasing. The transistor has the following parameters: k= 20.0 mA/V², λ = 0.01 V⁻¹, V_t = 1.0 V. Answer the following questions.



4.1 (10 pts) **Draw** the large signal model circuit.



4.2 (10 pts) **Find** the bias point, i.e. find V_G, V_S, V_D, and I_D. Ignore the effect of λ. **Circle** if the transistor is 1) **on** and 2) **in saturation**. Workspace continued on next page.

$I_D = \frac{1}{2} k (V_G - V_S - V_t)^2$ $\quad V_S = I_D R_S$ $\quad V_G = 3V$

$I_D = \frac{1}{2} 20 (3 - 1 - I_D \cdot 1)^2$

$\frac{I_D}{10} = (2 - I_D)^2 = 4 - 4I_D + I_D^2$

$I_D^2 - 4.1 I_D + 4 = 0$

$I_D = 2.05 \pm \sqrt{2.05^2 - 4}$

$= 2.5, 1.6$ mA

2.5 results in $V_{GS} < V_t$

$I_D = 1.6$mA

$V_D = 10 - (2)(1.6) = 6.8V$

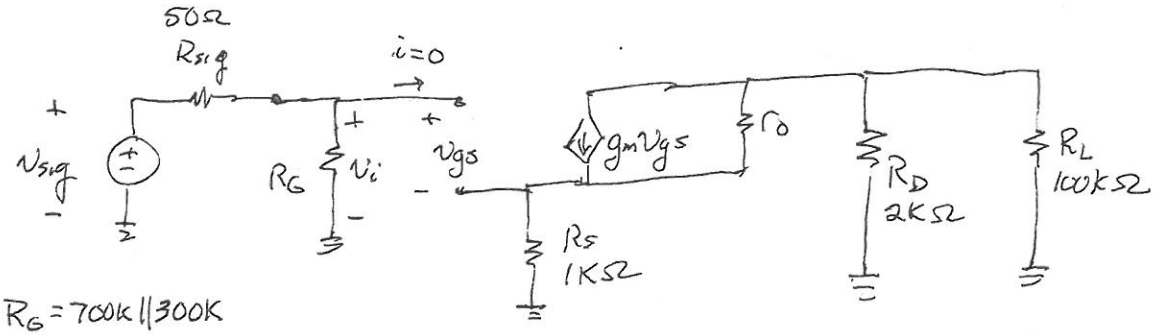
$V_S = 1 \cdot 1.6 = 1.6V$ $\quad V_{GS} > V_t \Rightarrow$ on

$V_{GS} = 3 - 1.6 = 1.4V$ $\quad V_{GS} - V_t = 0.4V < V_{DS}$

$V_{DS} = 6.8 - 1.6V = 5.2V$ $\quad \Rightarrow$ sat

Circle: (On) Off Mode: Cutoff (Saturation) Triode

4.3 (10 pts) **Draw** the small signal model circuit; use either the **hybrid-π or T-model. Include r_o. Label all components; label any dependent sources; label the control variable for any dependent sources; label any branches with zero current; label the following voltages: v_{sig}, v_i, v_{gs}, and v_o. Do not** develop, nor numerically solve, for any small signal parameters.



$R_G = 700k \| 300K$
$= 210K\Omega$

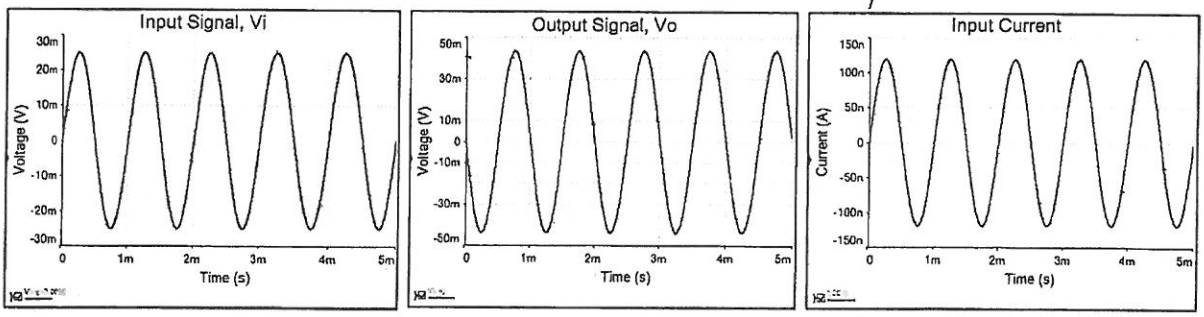
4.4 (5 pts) You test the amplifier and generate the signals below on your oscilloscope.

- **Approximate** the small signal gain A_v and input resistance R_i.

$A_v = \frac{v_o}{v_i} = -\frac{42mV}{25mV} = -1.68\ V/V$ $\quad R_{in} = \frac{v_{in}}{i_{in}} = \frac{25mV}{120nA} = 208K\Omega$

- Is this amplifier **inverting** or **noninverting?**

inverting v_o is 180° out of phase with v_{in}



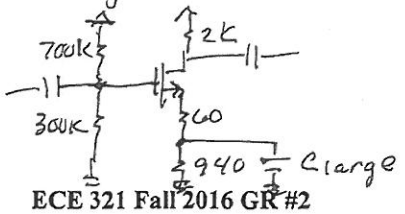
4.5 (5 pts) What could you do to increase the magnitude of the gain of the amplifier to 8 V/V, without changing the Q-point? Draw a schematic showing component values with your proposed change.

The easiest thing would be to bypass part of R_S

$\frac{R_D}{\frac{1}{g_m} + R_S} = |A_v|$ $\quad \frac{2K}{\frac{1}{g_m} + 1K} \simeq 1.68$ $\quad \frac{2K}{1.68} \simeq \frac{1}{g_m} + 1K$ $\quad \frac{1}{g_m} \sim 190\Omega$

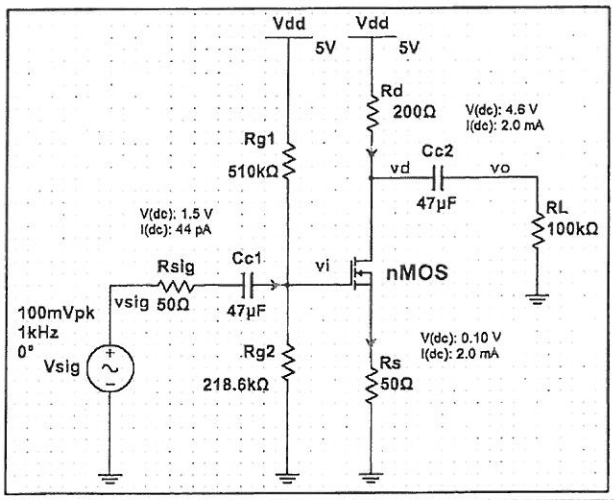
to get a gain of $R_S + \frac{1}{g_m} = \frac{2K}{8} = 250$ $\Rightarrow$ bypass all but 60Ω of R_S

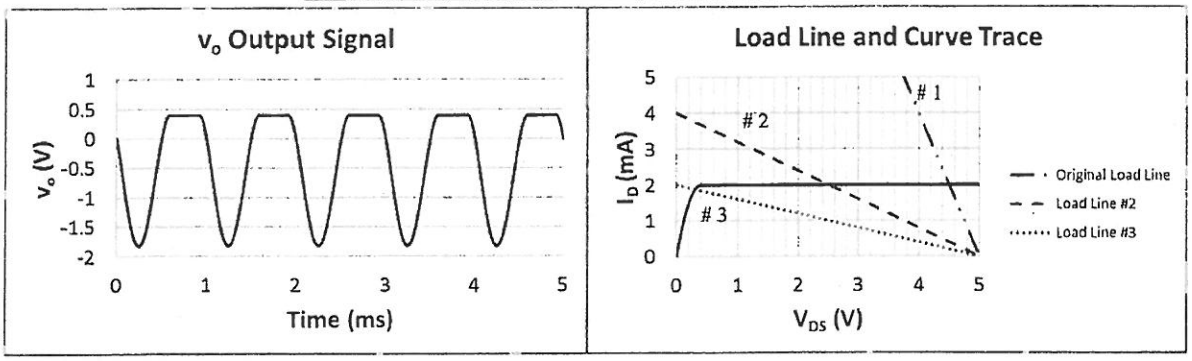
Not the best because now gain depends heavily on K and V_t



MOSFET Amplifier Design

5 (40 pts) You designed the amplifier below (V_t=1 V, k=25 mA/V², λ=0) and obtained the output signal shown. You don't know why the signal is distorted ("clipping") and decide to plot the load-line, labeled #1. You plot to additional load-lines, 2 and 3.





5.1 (10 pts) Write a general expression for the load -line. In other words, express I_D as a function of V_{DD}, V_{DS}, R_D, and R_S.

$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$$

5.2 (5 pts) Determine a numerical value for the slope of the original load-line.

$$m = \frac{-1}{R_D + R_S} = \frac{-1}{200\Omega + 50\Omega} = -0.004\,S \text{ or } -4\,mA/V$$

5.3. (15 pts) Assume you found the original load-line slope to be –4 mA/V. The slope of load-line #2 is one fifth (1/5) the slope of load-line #1. If you want to keep **the same I_D**, determine new values for R_D and R_S. Hint: You still are using the same V_{GS} curve and V_G has not changed.

$\Rightarrow R_D' + R_S' = 5(R_D + R_S) = 5 \cdot 1250 = 1250\,\Omega$

to keep I_D the same V_{GS} the same $\Rightarrow$ V_S the same

$\Rightarrow R_S$ unchanged so $R_D = 1200\,\Omega$ $R_S = 50\,\Omega$

5.4. (10 pts) Would you choose Load Line #2 or #3? Why?

The change above puts you on load-line #2 ~~This~~ at the intersection with V_{GS} curve. This is a good Q-point, enough leg room and head room.

Load Line 3 is too close to triode

$\Rightarrow$ no leg room

Use load line #2