

UNIVERSITY OF CALIFORNIA, BERKELEY  
**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**

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**Homework #2**

**EECS141**

*Due Thursday, September 9, 5pm, box in 240 Cory*

**PROBLEM 1: VTC**

In this problem we will analyze the noise margins for a chain of identical gates, Figure 1(a). The VTC for these gates is piece-wise linear with six segments, where each segment is a straight line, as shown in Figure 1(b).

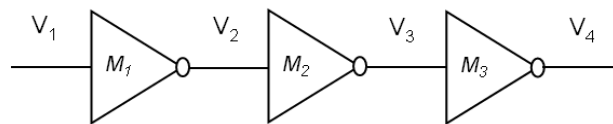


Figure 1(a)

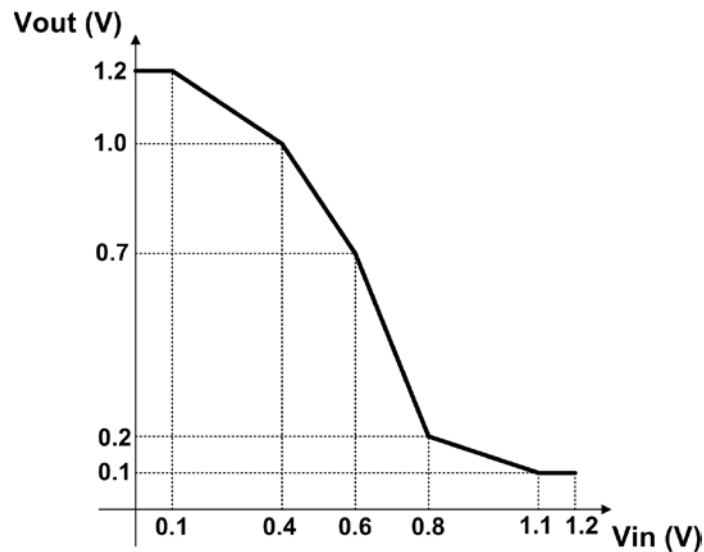


Figure 1(b)

- a) Add the DC voltage sources to Figure 1(a) that you would use for modeling noise coupling to the input and output of gate  $M_2$ . You should arrange these voltage sources so that they would both impact the noise margin in the same way (i.e., if the voltage source at the input decreases the noise margin, the voltage source at the output should also decrease the noise margin).

**Solution:**

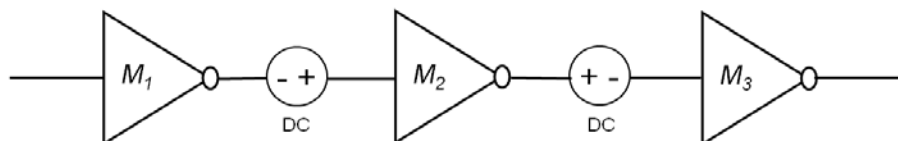


Figure S1(a)

- b) Determine the noise margins (as defined in lecture) for gate  $M_2$  when noise couples only to its input. We want a numerical answer in Volts, not one based on just looking at the VTC.

**Solution:**

To find the noise margin, we need to know  $V_{IL}$ ,  $V_{IH}$ ,  $V_{OL}$ , and  $V_{OH}$  for the inverters. As a reminder, if the VTC is represented as a function,  $f(\cdot)$ , then  $V_{OH} = f(V_{OL})$  and  $V_{OL} = f(V_{OH})$ . In this case, the only output levels that obey this definition (this can be found from the butterfly plot as well) are:

$$V_{OH} = 1.2\text{V}, V_{OL} = 0.1\text{V}$$

To find  $V_{IL}$  and  $V_{IH}$ , we need to find the unity-gain points on the VTC. Since the VTC is piece-wise linear, we first need to compute the slopes of each segment, and then determine the points at which the slope of the curve crosses unity gain.

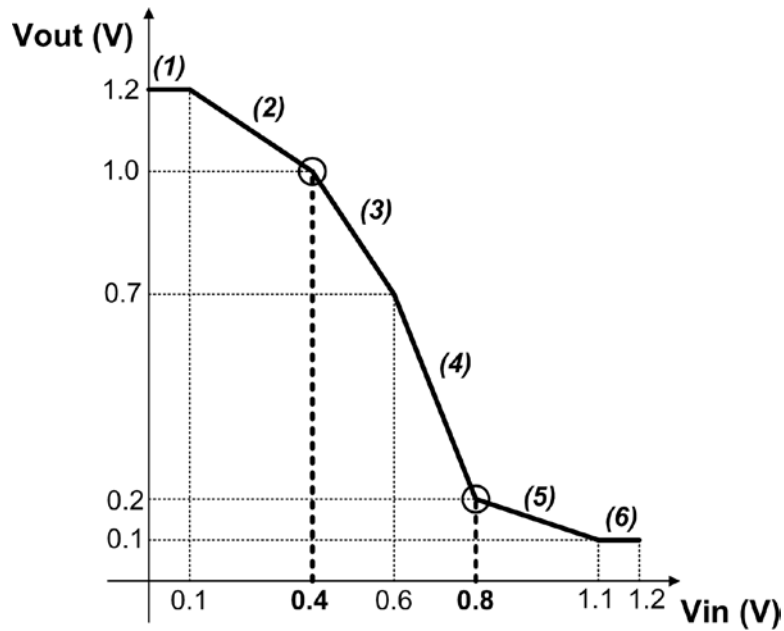


Figure S1(b)

If the segments are labeled as in Figure S1(b) above, then the magnitudes of the slopes of the segments can be computed as below:

$$|Slope(1)| = 0$$

$$|Slope(2)| = \left| \frac{1.0 - 1.2}{0.4 - 0.1} \right| = \frac{2}{3} < 1$$

$$|Slope(3)| = \left| \frac{0.7 - 1.0}{0.6 - 0.4} \right| = \frac{3}{2} > 1$$

$$|Slope(4)| = \left| \frac{0.2 - 0.7}{0.8 - 0.6} \right| = \frac{5}{2} > 1$$

$$|Slope(5)| = \left| \frac{0.1 - 0.2}{1.1 - 0.8} \right| = \frac{1}{3} < 1$$

$$|Slope(6)| = 0$$

Therefore:

$$V_{IL} = 0.4V$$

$$V_{IH} = 0.8V$$

Finally:

$$NM_H = V_{OH} - V_{IH} = 1.2V - 0.8V = \underline{\underline{0.4V}}$$

$$NM_L = V_{IL} - V_{OL} = 0.4V - 0.1V = \underline{\underline{0.3V}}$$

- c) Consider a gate  $M_4$  that has a VTC as shown in Figure 1(c). Assuming that  $V_A < V_B$  and  $V_C < V_D$ , define the relationships between  $V_A$ ,  $V_B$ ,  $V_C$  &  $V_D$  that would make  $M_4$  digital.

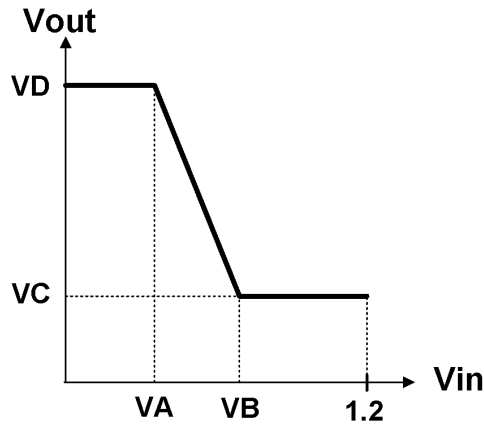


Figure 1(c)

### **Solution:**

In order for a gate to be digital, it must have positive noise margins,  $NM_H$  and  $NM_L$ . To have well-defined  $V_{IL}$  and  $V_{IH}$ , the VTC must have a region where its slope  $> 1$ . This leads to the first relationship:

$$\frac{V_D - V_C}{V_B - V_A} > 1$$

Assuming this first constraint is met, it is now easy to see that:

$$\begin{aligned}
 V_{IL} &= V_A \\
 V_{IH} &= V_B \\
 V_{OH} &= V_D \\
 V_{OL} &= V_C
 \end{aligned}$$

Therefore, enforcing positive noise margins leads us to the second set of relationships:

$$\begin{aligned}
 NM_H &= V_{OH} - V_{IH} = V_D - V_B > 0 \\
 NM_L &= V_{IL} - V_{OL} = V_A - V_C > 0
 \end{aligned}$$

Note that the more stringent requirement is actually the second set of relationships, since if those are satisfied then the slope requirement will automatically be met as well.

- d) Consider the cascade of gates  $M_3$  and  $M_4$ , as shown in Figure 1(d), where  $M_3$  is the gate from parts (a) & (b), and  $M_4$  is the gate from part (c). If  $V_A = 0.2V$ ,  $V_B = 0.7V$  and  $V_D = 1.2V$  (as shown in the figure), what is the range of values of  $V_C$  for which the cascade is digital? As a part of your answer, sketch out the VTC of the cascade of  $M_3$  and  $M_4$ .

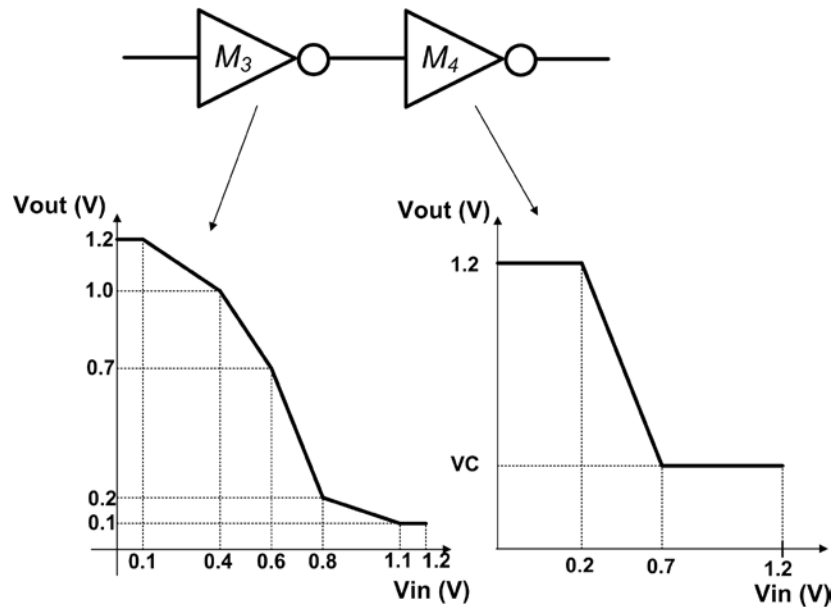


Figure 1(d)

### **Solution:**

Let us first sketch the VTC of the cascade of gates  $M_3$  and  $M_4$  with a variable  $V_C$  as shown in Figure S1(d). For estimating the VTC, it is convenient to traverse the VTCs of  $M_3$  and  $M_4$  segment by segment.

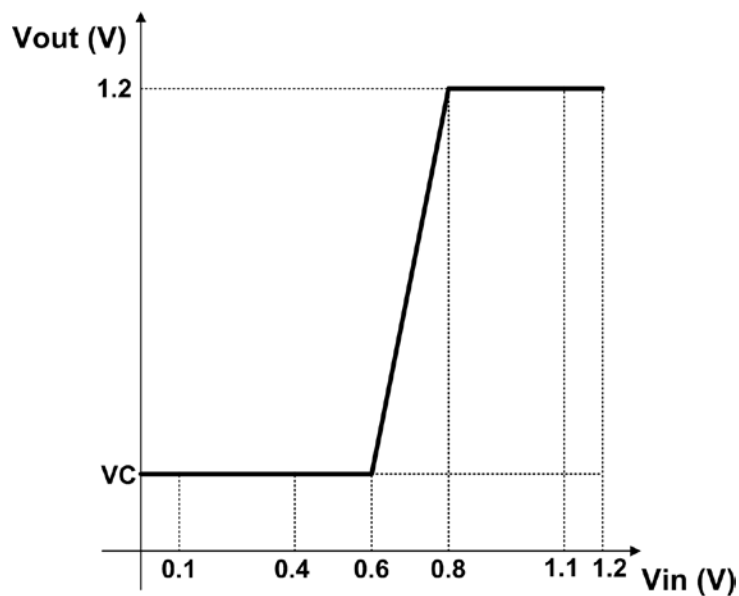


Figure S1(d)

The cascade is digital if the VTC in Figure S1(d) has positive noise margins. As can be seen,

$$V_{IL} = 0.6V, V_{IH} = 0.8V, V_{OL} = VC, V_{OH} = 1.2V$$

$$NM_H = 1.2 - 0.8 = 0.4 > 0.$$

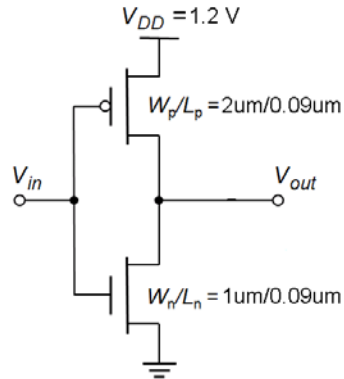
$$NM_L = 0.6 - VC > 0.$$

Therefore, the cascade is digital for:

$$\underline{0V < VC < 0.6V}$$

## PROBLEM 2: DELAY

Recall that we have defined the propagation delay  $t_p$  as the time between the 50% transition points of the input and output waveforms. In this problem, we will explore how the way you set up a simulation can affect the results you measure. Please turn in a single spice deck that performs the simulations for parts b) through d). You can measure the delays either by using .MEASURE statements in SPICE, or using WaveView. However, if you use WaveView you should include plots of your waveforms.



- a) Create a SPICE subcircuit for the inverter shown above. Use the following line in your SPICE deck to obtain the correct NMOS and PMOS transistor models:

*.LIB '/home/ff/ee141/MODELS/gpdk090\_mos.sp' TT\_s1v*

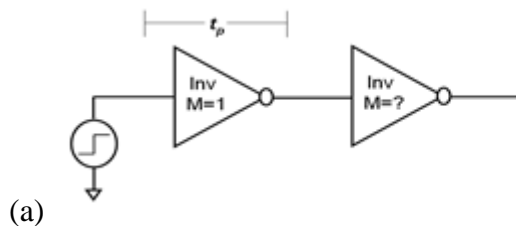
To help get you started, we have provided the following example which demonstrates the creation and usage of subcircuits in SPICE. The following input creates an instance named X1 of the MYRC subcircuit, which consists of a 5k $\Omega$  resistor and 10fF capacitor in parallel.

*X1 TOP BOTTOM MYRC*

*.SUBCKT MYRC A B*  
*R1 A B 5k*  
*C1 A B 10f*  
*.ENDS*

### Solution:

\* Inverter SUBCKT Definition  
 .SUBCKT inv vdd gnd in out  
 Mp out in vdd vdd gpdk090\_pmos1v W=2u L=0.09u  
 Mn out in gnd gnd gpdk090\_nmos1v W=1u L=0.09u  
 .ENDS



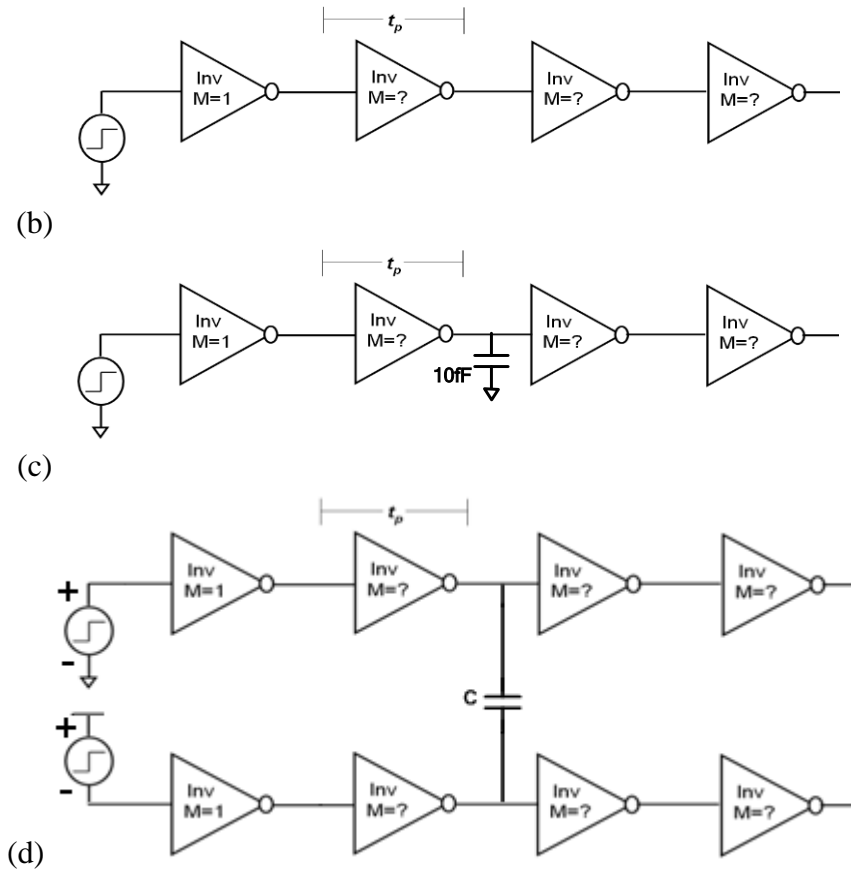


Figure 2

- b) Measure the average propagation delay of an inverter driving four copies of itself (Fig. 2a). First apply a step input with a rise/fall time of 1 ns to the first inverter. Then, repeat this measurement with a rise/fall time of 1 ps. *Note: Use the M (Multiply) parameter in the subcircuit instantiation to replicate the inverter.*

**Solution:**

(See part e) for the spice deck)

1 ns:  $t_{pHL} = 45.8\text{ps}$ ,  $t_{pLH} = 95.9\text{ps}$ ,  $t_{pavg} = 70.9\text{ps}$

1 ps:  $t_{pHL} = 18.2\text{ps}$ ,  $t_{pLH} = 18.9\text{ps}$ ,  $t_{pavg} = 18.6\text{ps}$

- c) Now create a chain of four inverters, each with a fanout of 4 (Fig. 2b). Measure the average propagation delay of the second inverter in the chain when applying a step input to the first inverter. Is the delay from part b) or part c) more realistic in terms of what you might see on an actual IC? Explain the role of the first inverter in the chain.

(See part e) for the spice deck)

$t_{pHL} = 23.5\text{ps}$ ,  $t_{pLH} = 25.2\text{ps}$ ,  $t_{pavg} = 24.4\text{ps}$

The delay from part c) is more realistic because the input is provided by the output of the previous gate (first inverter in the chain) instead of a step function with an arbitrary (i.e., unrealistic) rise/fall time.

- d) Repeat part c) with the chain of four inverters, each with the fanout of 4 (Fig. 2c), but this time add a 10 fF capacitor (which could be from a wire) between the second and the third inverter. Compare this delay with the result from part c).

**Solution:**

(See part e) for the spice deck)

$t_{pHL} = 25.2\text{ps}$ ,  $t_{pLH} = 27.1\text{ps}$ ,  $t_{pavg} = 26.2\text{ps}$

- e) Now let's use the circuit from Fig. 2d to see how connecting the capacitor in a different way may have more or less impact on the delay. Notice that the input to the lower inverter chain in the figure is complementary to the input given to the upper chain. In other words, when the input to the upper chain rises, the input to the lower chain falls (and vice versa).

What value of C do you need to use to make the delay of the circuit from Fig. 2d match the delay you measured in part d)? Why might this capacitor be larger or smaller than the 10fF used in part d)?

**Solution:**

To match the average delay of the two chains,  $C = \sim 5\text{fF}$ . This capacitor is smaller (and, in fact, almost exactly half) than the one in part d) because the two nodes that the capacitor is tied to are switching in opposite directions at the same time. This means that the total voltage swing across the capacitor is approximately twice what was in part d) – i.e., the “Miller effect” is making this C look larger than it would if one of the terminals was grounded (i.e., not moving).

$t_{pHL} = 25.2\text{ps}$ ,  $t_{pLH} = 27.1\text{ps}$ ,  $t_{pavg} = 26.3\text{ps}$

**SPICE Deck:**

\*\*\* HW2 Problem 2 \*\*\*

```
.LIB '/home/ff/ee141/MODELS/gpdk090_mos.sp' TT_s1v
.PARAM vddval=1.2

* Inverter SUBCKT Definition
.SUBCKT inv vdd gnd in out
Mp out in vdd vdd gpdk090_pmos1v W=2u L=0.09u
Mn out in gnd gnd gpdk090_nmos1v W=1u L=0.09u
.ENDS

* Voltage Sources
V1 vdd 0 'vddval'
V2 vstep 0 PWL 0 0V 10p 0V 1010p 'vddval' 1210p 'vddval' 2210p 0V
V3 vstep2 0 PWL 0 0V 10p 0V 11p 'vddval' 211p 'vddval' 212p 0V
V4 vstep3 0 PWL 0 'vddval' 10p 'vddval' 11p 0V 211p 0V 212p 'vddval'
```



\* Part B

```
Xinv1b vdd 0 vstep vout1b inv M=1
Xinv2b vdd 0 vout1b vout2b inv M=4
Xinv1b2 vdd 0 vstep2 vout1b2 inv M=1
Xinv2b2 vdd 0 vout1b2 vout2b2 inv M=4
```

\* Part C

```
Xinv1c vdd 0 vstep2 vout1c inv M=1
Xinv2c vdd 0 vout1c vout2c inv M=4
Xinv3c vdd 0 vout2c vout3c inv M=16
Xinv4c vdd 0 vout3c vout4c inv M=64
```

\* Part D

```
Xinv1d vdd 0 vstep2 vout1d inv M=1
Xinv2d vdd 0 vout1d vout2d inv M=4
Xinv3d vdd 0 vout2d vout3d inv M=16
Xinv4d vdd 0 vout3d vout4d inv M=64
C_d vout2d 0 10f
```

\* Part E

```
Xinv1e1 vdd 0 vstep2 vout1e1 inv M=1
Xinv2e1 vdd 0 vout1e1 vout2e1 inv M=4
Xinv3e1 vdd 0 vout2e1 vout3e1 inv M=16
Xinv4e1 vdd 0 vout3e1 vout4e1 inv M=64
```

```
Xinv1e2 vdd 0 vstep3 vout1e2 inv M=1
Xinv2e2 vdd 0 vout1e2 vout2e2 inv M=4
Xinv3e2 vdd 0 vout2e2 vout3e2 inv M=16
Xinv4e2 vdd 0 vout3e2 vout4e2 inv M=64
C_f vout2e1 vout2e2 5f
```

\* options

```
.option post=2 nomod
```

\* analysis

```
.TRAN 0.1PS 5NS
```

\* Part B Measurement

```
.MEASURE TRAN tpHLb TRIG V(vstep) VAL='vddval/2' RISE=1 TARG V(vout1b) VAL='vddval/2' FALL=1
.MEASURE TRAN tpLHb TRIG V(vstep) VAL='vddval/2' FALL=1 TARG V(vout1b) VAL='vddval/2' RISE=1
.MEASURE TRAN tpavgb PARAM='(tpHLb+tpLHb)/2'
```

```
.MEASURE TRAN tpHLb2 TRIG V(vstep2) VAL='vddval/2' RISE=1 TARG V(vout1b2) VAL='vddval/2' FALL=1
.MEASURE TRAN tpLHb2 TRIG V(vstep2) VAL='vddval/2' FALL=1 TARG V(vout1b2) VAL='vddval/2' RISE=1
.MEASURE TRAN tpavgb2 PARAM='(tpHLb2+tpLHb2)/2'
```

\* Part C measurement

```
.MEASURE TRAN tpHLc TRIG V(vout1c) VAL='vddval/2' RISE=1 TARG V(vout2c) VAL='vddval/2' FALL=1
.MEASURE TRAN tpLHc TRIG V(vout1c) VAL='vddval/2' FALL=1 TARG V(vout2c) VAL='vddval/2' RISE=1
.MEASURE TRAN tpavgc PARAM='(tpHLc+tpLHc)/2'
```

\* Part D measurement

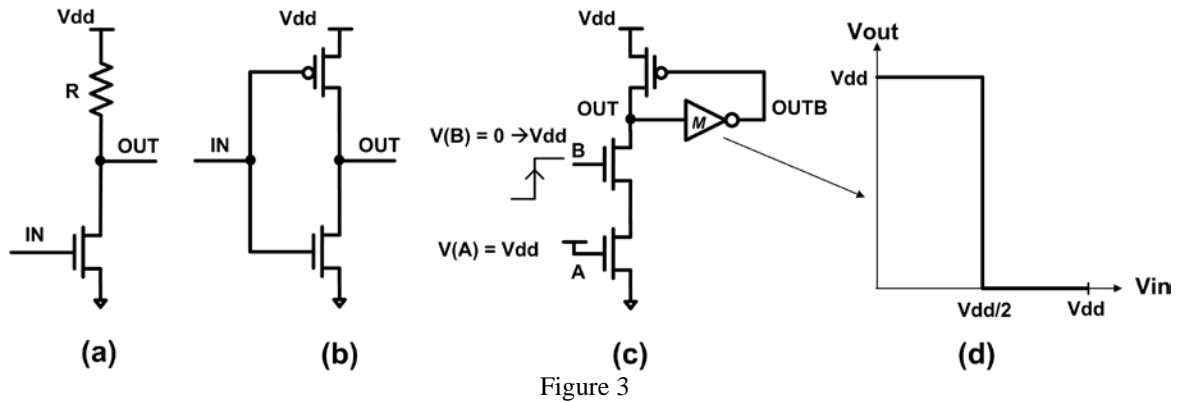
```
.MEASURE TRAN tpHLd TRIG V(vout1d) VAL='vddval/2' RISE=1 TARG V(vout2d) VAL='vddval/2' FALL=1
.MEASURE TRAN tpLHd TRIG V(vout1d) VAL='vddval/2' FALL=1 TARG V(vout2d) VAL='vddval/2' RISE=1
.MEASURE TRAN tpavgd PARAM='(tpHLd+tpLHd)/2'
```

\* Part E measurement

```
.MEASURE TRAN tpHLe TRIG V(vout1e1) VAL='vddval/2' RISE=1 TARG V(vout2e1) VAL='vddval/2' FALL=1
.MEASURE TRAN tpLHe TRIG V(vout1e1) VAL='vddval/2' FALL=1 TARG V(vout2e1) VAL='vddval/2' RISE=1
.MEASURE TRAN tpavge PARAM='(tpHLe+tpLHe)/2'
```

```
.END
```

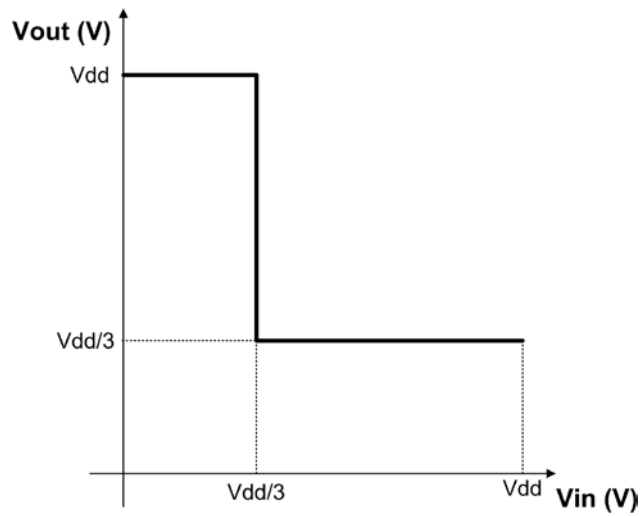
### PROBLEM 3: SWITCH MODEL



In this problem, you should use the simple switch model for MOSFETs with the following characteristics:  $|V_{TP}| = V_{dd}/3$ ,  $V_{TN} = V_{dd}/3$

- a) Sketch the VTC of the circuit shown in Figure 3(a) when  $R = 2 \cdot R_{NMOS}$ .

**Solution:**



- b) Sketch the VTC of the circuit shown in Figure 3(b) when  $R_{PMOS} = 2 \cdot R_{NMOS}$ .

**Solution:**

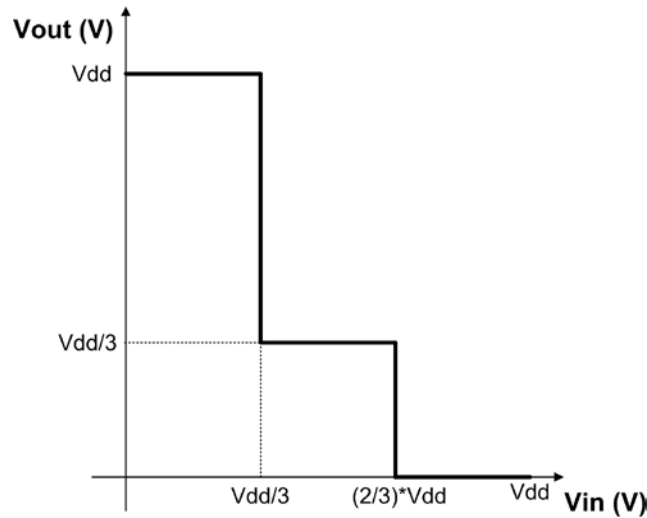


Figure S3(b)

- c) For the circuit shown in Figure 3(c), consider the following scenario.  $R_{PMOS} = 10 \cdot R_{NMOS}$ . The inverter  $M$  has an ideal VTC as shown in Fig. 3(d).  $V(A)$  is held constant at  $V_{dd}$ ,  $V(OUT)$  is initially equal to  $V_{dd}$ , and  $V(B)$  is initially equal to  $0V$ . Sketch  $V(OUT)$  vs.  $V(B)$  with  $V(B)$  swept from  $0V$  to  $V_{dd}$ . In other words, you should assume that  $V(B)$  starts at  $0V$  and then plot what happens to  $V(OUT)$  as you increase  $V(B)$  up to  $V_{dd}$ . (The curve you are drawing is very much like a VTC, but is only valid when the input and output start in the given states.)

**Solution:**

This part is a little tricky because not only does the output of gate  $M$  determine the gate voltage of the PMOS, but the source of the top NMOS transistor is not connected to a supply voltage (and hence can vary). Let's call the node between the two NMOS transistor  $S$  (as shown in Figure S3(c) below).

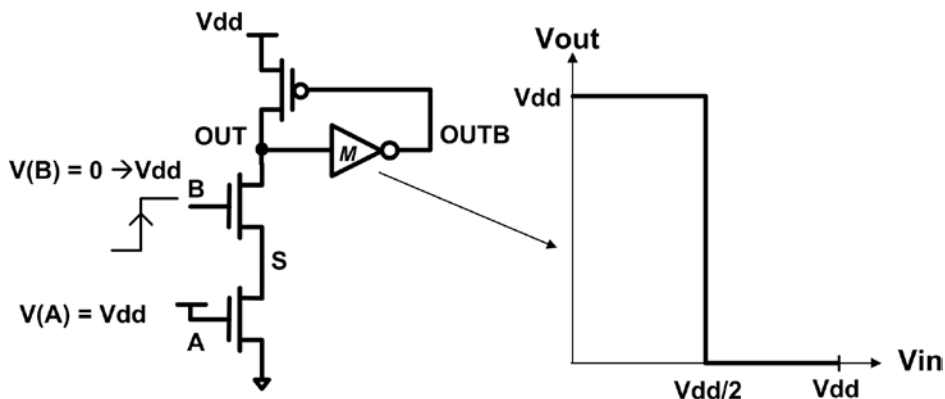


Figure S3(c)

- i. First, when  $V(B)$  is less than  $V_{TN}$  – i.e., when  $V(B) < V_{dd}/3$ , the top NMOS transistor is definitely off and therefore  $V(OUT) = V_{dd}$ . The output of gate  $M$   $V(OUTB) = 0V$ , which means that the PMOS transistor is on and is maintaining  $V(OUT) = V_{dd}$ . (In other words, we have a self-consistent solution). Meanwhile,  $V(S) = 0$ .
- ii. Once  $V(B)$  gets ever so slightly higher than  $V_{dd}/3$  (i.e., larger than  $V_{TN}$ ) is when the most interesting behavior occurs. When  $V(B)$  is slightly bigger than  $V_{dd}/3$ , the upper NMOS transistor (whose gate is connected to  $B$ ) should turn on. However, as soon as the transistor turns on and starts drawing some current,  $V(S)$  will rise above  $0V$ . In fact, if all three transistors were on,  $V(OUT)$  would be  $V_{dd}/6$ , and  $V(S)$  would be  $V_{dd}/12$ . This is problematic because in order for the top NMOS to stay on with  $V(S) = V_{dd}/12$ ,  $V(B)$  has to be greater than  $V_{TN} + V_{dd}/12$ , which implies that for  $V(B)$  only ever so slightly above  $V_{TN}$  the top NMOS transistor can't be on.

Even though we've just found that the top NMOS transistor can't be on, it turns out it can't be off either. This is because as soon as this transistor turns off, the bottom NMOS transistor pulls  $V(S)$  back to  $0V$ , which would turn the top NMOS transistor right back on.

Neither the on nor the off state is self-consistent, but we can imagine that this sequence of turning on and turning off will repeat itself over and over in a way that causes  $V(S)$  to stay at the boundary between the two states. This boundary is  $V(S) = V(B) - V_{TN} = V(B) - V_{dd}/3$ . The current flowing through the bottom NMOS transistor will therefore be:

$$I_{bot} = (V(B) - V_{dd}/3) / R_{NMOS}$$

and since  $R_{PMOS} = 10 * R_{NMOS}$ , this means that:

$$V(OUT) = V_{dd} - I_{bot} * 10 * R_{NMOS} = V_{dd} - 10 * (V(B) - V_{dd}/3)$$

In other words, as  $V(B)$  increases,  $V(OUT)$  falls with a slope of  $-10$ .

- iii. When  $V(B)$  is slightly greater than  $V_{dd}/3 + V_{dd}/20$ ,  $V(OUT)$  drops below  $V_{dd}/2$ , which causes the output of gate  $M$  to flip to  $V(OUTB) = V_{dd}$ . This causes the PMOS transistor to turn off, allowing both  $V(S)$  and  $V(OUT)$  drop to  $0V$ . Since  $V(S)$  is now at  $0V$ , we can be sure that the top NMOS transistor is on – i.e., we once again have a (simple) self-consistent solution.

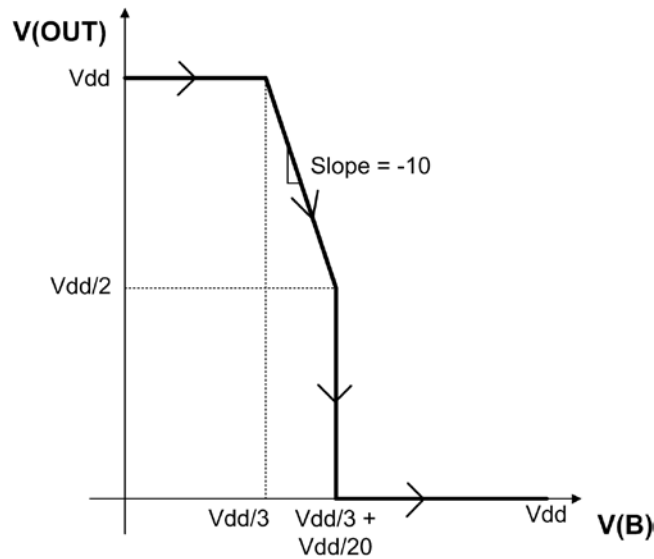


Figure S3(d): Solution for Question 3.c)

Note that if you correctly identified that the gate essentially begins to transition from  $V_{dd}$  to  $Gnd$  at  $V(B) = V_{dd}/3$ , and that the final state will indeed be  $V(OUT) = 0V$ , you will receive full credit for this part of the problem. If you correctly explained the full behavior, you will receive bonus credit.

- d) For part 3(c) if  $R_{PMOS} = R_{NMOS}$ , with all other conditions remaining the same, redraw  $V(OUT)$  vs.  $V(B)$  with  $V(B)$  swept from  $0V$  to  $V_{dd}$ .

**Solution:**

- i. For  $V(B) < V_{dd}/3$  the upper NMOS transistor is definitely off and  $V(OUT) = V_{dd}$ . Therefore, as in part (c), in this region the output of gate  $M$   $V(OUT_B) = 0V$ .
- ii. When  $V(B)$  is slightly larger than  $V_{dd}/3$ , we have a similar situation as in part c), and transistor B is neither on nor off. Now since  $R_{PMOS} = R_{NMOS}$ , we have

$$V(OUT) = V_{DD} - (V(B) - V_{dd}/3).$$

Therefore, as  $V(B)$  increases,  $V(OUT)$  decreases with a slope of  $-1$ , until  $V(B)$  reaches  $(2/3)*V_{dd}$ .

- iii. For  $V(B) > (2/3)*V_{dd}$ , transistor B is fully on and  $V(S)$  stays put at  $V_{dd}/3$ . Therefore,  $V(OUT) = (2/3)*V_{dd}$ . Notice that gate  $M$  maintains  $V(OUT_B) = 0V$ , thus leaving the PMOS transistor on.

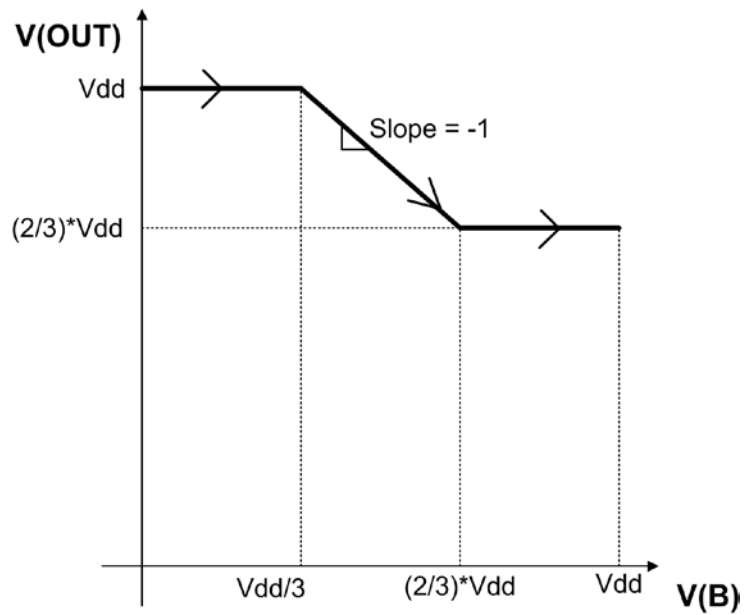


Figure S3(e): Solution for Question 3.d)

As with part (c), if you correctly identified the point at which the circuit transitions and the final value (i.e.,  $2/3 \cdot V_{\text{dd}}$ ), you will receive full credit on this part of the problem. If you also correctly the full behavior of the transition region, you will receive bonus credit.