The Amplifier

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Objective

The purpose of this lab is to illustrate and reinforce the modeling and operational concepts of metal-oxide-semiconductor field-effect transistors (MOSFETs) used as amplifiers. The first portion of the lab involved using a nMOS transitor set up in a common source amplifier layout in order to induce a -3 V/V to -30 V/V gain from a small signal input. The second portion of the lab included creating a buffering amplifier from a transistor in a common drain set up.

Specifications and Limitations

Single Stage Amplifier:

- Circuit Topology: Common Source with Source Resistor (See Fig. 1 for topology)
- Transistor: BS-170 MOSFET
- V_{DD} from 10 to 20 V ($10V \leq V_{DD} \leq 20V$)
- Maximum drain current: 75% of the max transistor DC current
- Input Resistance (R_i): > 100 kΩ
- Output Resistance (R_{out}): ≤ 5 kΩ
- Load Resistance (R_L): 100 kΩ (AC coupled using 10 µF - 47µF electrolytic caps)
- V_{in}: 1kHz sine wave -- AC coupled (10µF - 47µF Electrolytic cap)
- Voltage Gain (A_V): -3 V/V ≥ A_V ≥ -30 V/V (no visible signal distortion)
- V_{out}: Should achieve at least 3 V_{p-p} with no visible distortion
- Instantaneous Power Dissipation in any part NOT to exceed 75% of max power
- Potentiometers can't be used for any part of the design

Cascaded Amplifiers:

- Circuit Topology: Common Source with Source Resistor cascaded with a Common Drain (See Fig. 2 for topology).
- Transistor: BS -170 and BS-250
- V_{DD} from 10 to 20 V ($10V \leq V_{DD} < 20V$)
- Maximum drain current: 75% of the max transistor DC current
- Input Resistance (R_i): R_i > 100 kΩ
- R_i of the PMOS > 100 kΩ
- Output Resistance (R_{out}): $R_{out} \leq 5$ kΩ
- Load Resistance (R_L): 50 Ω (AC coupled using 10 µF–47µF electrolytic caps)
- V_{in} : 1kHz sine wave -- AC coupled (10µF – 47µF Electrolytic cap)
- Voltage Gain (A_V): -3 V/V ≥ A_V > -30 V/V (no visible signal distortion)
- V_{out}: The amplifier should be able to supply at least 3 V_{p-p} with no visible distortion
- Instantaneous power dissipation in any part may not exceed 75% of max power dissipation specified for the part
- Potentiometers can't be used for any part of the design.
- VSD of PMOS ~7 Volts (or roughly ½ the supply voltage)
- ID of PMOS ~60 mA

General Approach

The laboratory exercise begins with the creation of an amplification circuit that produces a negative gain between 3 V/V and 30 V/V. The lab concludes with connecting the first circuit to a buffering circuit that produces a gain of nearly 1 V/V. When approaching the construction of this circuit, it is best to create the two circuits separately and ensure they are working as expected before combining them. The best way to create these circuits is to first design the circuits and simulate them before actually constructing them on a breadboard.

Beginning with the circuit producing a negative gain between 3 V/V and 30 V/V, it is best to compile a list of the circuits governing equations before attempting to determine the values of the circuit's components. The lab handout specifies that a common-source amplifier with a source resistor using a NMOS FET should be used in order to produce this gain, which is demonstrated below in Figure 1.

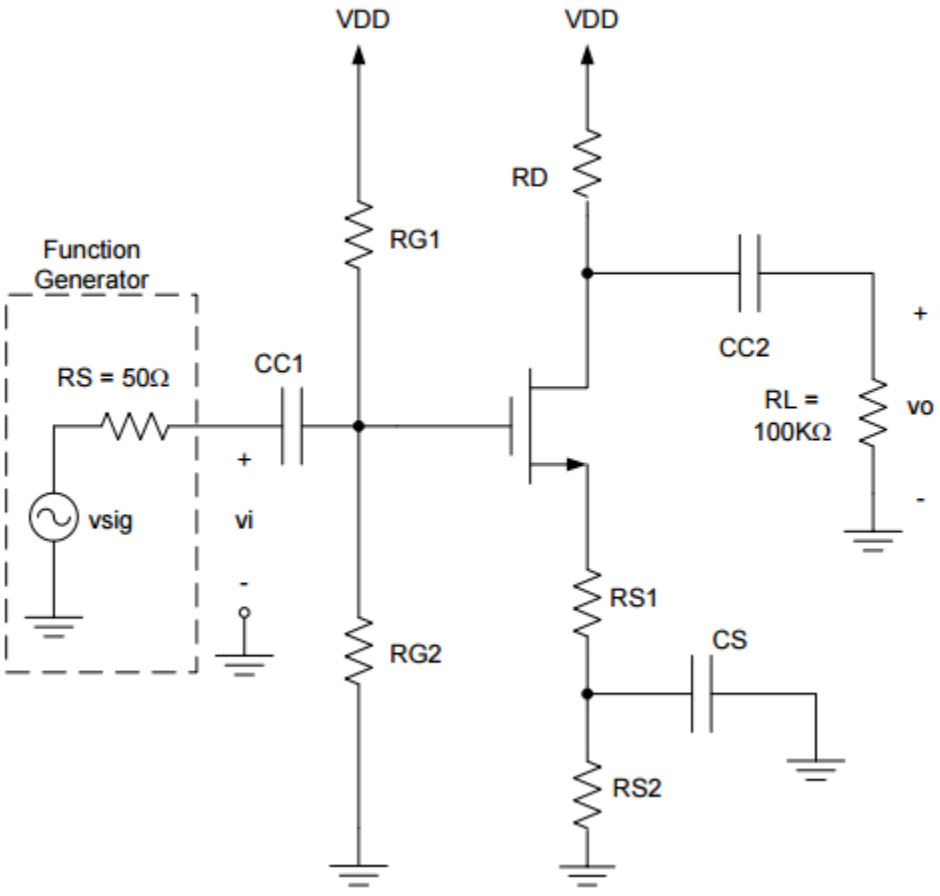

Figure 1. Common-source amplifier with source resistor using NMOS FET biased with the classical 4-resistor scheme.

Because the general schematic for the circuit was provided, the next step is to produce the governing equations in order to determine the values of the circuit components. The design of the circuit begins with using the large voltage V_{DD} to correctly bias the nodes of the transistor so that

it is in the saturation region, also known as “turned on”. In order to correctly handle the large signal circuit, it is important to isolate the components of the circuit that are affected by that signal. Considering that the capacitors on the circuit in Figure 1 cause an open circuit from the perspective of the large signal input, the resulting large signal circuit can be seen in Figure 2. Next a biasing scheme should be created to determine how V_{DD} will be dispersed across R_D, the V_{DS} channel, and R_S. A common biasing scheme that tends to work is a drop of 2/5 of V_{DD} across R_D, a drop of 1/5 of V_{DD} across the V_{DS} channel, and finally 2/5 of V_{DD} across R_S. Using the biasing scheme, both V_D and V_S can be set, which will be used in determining V_G.

Large Signal Equations:

1) $V_G = \left(\frac{RG2}{RG1+RG2}\right) V_{DD}$

2) $V_S = I_D(RS1 + RS2)$

3) $V_D = V_{DD} - I_D R_D$

4) $I_D = \frac{1}{2}k(V_{ov})^2 = \frac{1}{2}k(V_{GS} - V_t)^2$

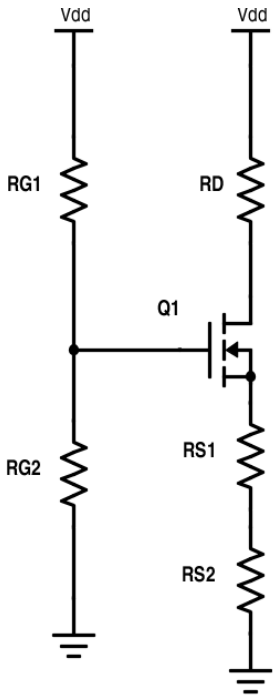

Figure 2. The Large Signal model circuit.

In order to determine V_G, consider Equation 4. The I_D is a characteristic that will be set by the designer, and will be proven true by the determination of the circuit component values. However, listed in the design Specifications and Limitations, the drain current must be less than 75% of the max transistor DC current, which is specified by the data sheet as 500 mA. If I_D is set and both k and V_t are characteristics of the transistor, which when designing will be assumed to be 250 mA/V^2 and 2 V respectively, then V_G is the only variable left to be solved for. Solving Equation 4 for the overdrive voltage (V_{OV}) will produce both a positive and negative answer because of V_{OV} being squared. Both V_{OV} values will need to be analyzed in order to find the value that will result in the transistor being in saturation mode, meaning that the V_{GS} voltage has a higher magnitude than that of the threshold voltage (V_t). After determining what V_{OV} causes the transistor to be in saturation, the V_G can be calculated. At this point, all of the resistance values need to be calculated in order to realize the desired biasing voltages. Equation 1 is used to calculate R_{G1} and R_{G2} values that can produce the calculated V_G value. Equation 2 is used to calculate the sum of R_{S1} and R_{S2}, the distinct values will be determined later in the analyzation of the small signal circuit. Finally, Equation 3 is used to determine the value of R_D. Now the entirety of the components in the large signal circuit have been determined that will ensure that the transistor is turned on and working correctly. The next step in designing the gain producing circuit is to analyze the small signal circuit.

When looking at the circuit from the small signal’s perspective, the capacitors can be considered shorts in the circuit and the large signal voltages can be disregarded, and so set as ground. The described small signal circuit can is demonstrated below in Figure 3. Analyzation of the small signal circuit produces the follow governing equations.

Small Signal Equations:

5) $g_m = kV_{ov} = \frac{2I_D}{V_{ov}}$

-Assuming $r_o >> R_L$ and R_D

6) $A_v = \frac{-g_m(R_D||R_L)}{1+ g_m R_{s1}}$

7) $A_{vo} = \frac{-g_m * R_D}{1+ g_m R_{s1}}$

8) $G_v = A_v(R_{sig}|| R_{in})$

9) $R_{in} = \frac{RG1*RG2}{RG1+RG2}$

10) $R_{out} = \frac{R_D * R_L}{R_D + R_L}$

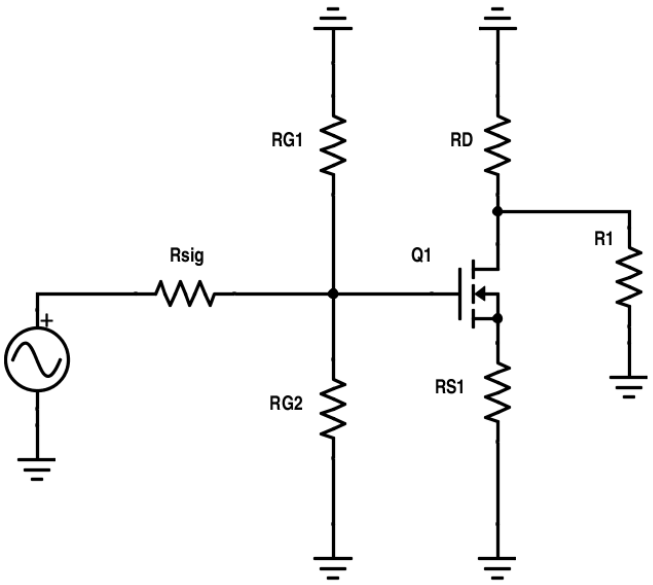

Figure 3. Small Signal Model circuit of the nMOS FET in the common-source configuration

Diving into the design of the circuit, solving Equation 5 produces a value for g_m, which will be used in the majority of the other equations. A quick analyzation of Equation 6 highlights two important factors. First that r_o can be disregarded considering that it is in parallel with and is of a much greater magnitude than both R_D and R_L, R_L set to 100KΩ as described by the lab handout. Second, Equation 6 highlights the importance of having R_{S1} in series with the CS capacitor as seen in Figure 1. Without the described configuration, the gain would be set when setting the circuit components based on the large signal circuit. The R_{S1} allows the designer to manipulate the gain of the circuit to some extent. At this point, the A_v can be set anywhere between the -3 V/V and -30 V/V described by the laboratory Specifications and Limitations and Equation 6 can be solved for the value of R_{S1}. Now that the value of R_{S1} has been determined, the value of R_{S2} can calculated based on the consideration of Equation 2 from the large signal circuit analyzation. At this point, both R_{in} and R_{out} can be calculated using Equations 9 and 10, respectively, in order to ensure they meet the values described by the Specification and Limitations. The R_{in} value is simple enough to adjust as the R_{G1} and R_{G2} values are simply used to create a ratio. If the R_{in} value is too low, the two resistance values can be scaled by the same scalar value in order to achieve a R_{in} value higher than 100 KΩ. Although the A_{vo} and G_v gains have no specifications, they are easily calculated using Equations 7 and 8, respectively.

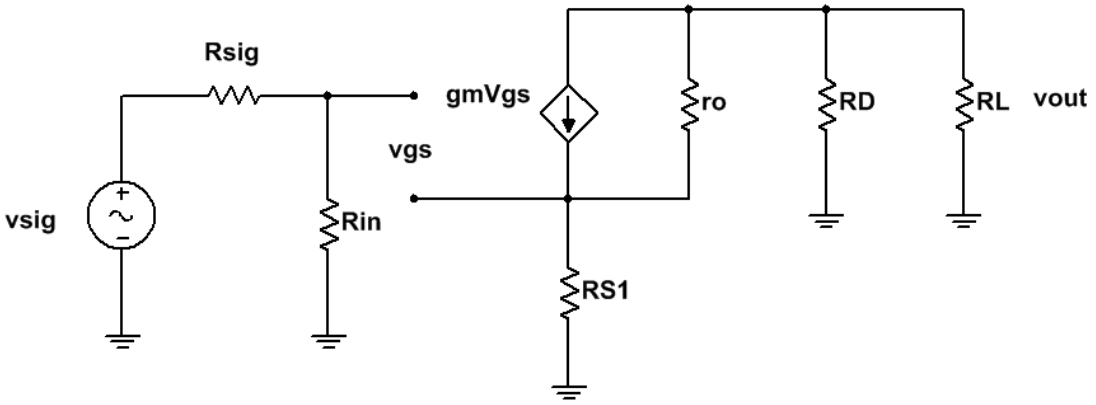

Figure 4. The hybrid-pi model of the Small Signal Operation of the nMOS FET in the common-drain configuration.

Now is the time to simulate the circuit in order to determine if the described circuit should theoretically meet the Specifications and Limitations given for the circuit. After constructing the circuit as shown in Figure 1, change the component values to those calculated as described in the paragraphs above. Additionally, the nMOS transistor in simulation needs to have its k' and V_t values need to be changed to those that were assumed for the design of the circuit. These values can be changed by right clicking the transistor, selecting the 'Properties', selecting 'Edit Model' under the 'Value' tab, and changing the values named VTO (V_t) to 2 V and KP (k) to 0.250 A/V^2. Now is the time to determine the small AC signal input, which needs to be large enough to produce a 3 V peak to peak output voltage but small enough that it will not cause any signal distortion for V_{out}. At this point, it is important to verify the drain, gate, and source voltages in order to verify that the transistor is turned on and that the biasing scheme worked correctly. In order to verify the drain, gate, and source voltages, place DC voltage and current nodes at the drain pin, the gate pin, and the source pin of the transistor. After verifying that these voltages and currents all match with those that we calculated, it is important to ensure that the circuit is producing the voltage gain that it was designed to produce. In order analyze the v_{in} against the v_{out}, use a transient analysis on the node going into the gate pin of the transistor against the node on the circuit side of the 100 KΩ load resistor. In order to order to be able to set these nodes as outputs for the transient analysis, name the nodes by right clicking on the node, choose 'Properties', then set an appropriate 'Preferred net name' for the node. Perform the transient analysis on the nodes, except remember to subtract out the large signal gate voltage, leaving only the small signal AC voltage. In order to select only the small signal gate voltage for transient analysis, under the 'Output' tab of 'Transient Analysis', select 'Add expression…' to the 'Selected variables for analysis' list and subtract the large signal gate voltage from the total gate voltage, leaving only the small signal gate voltage of interest. Now, compare the small signal input voltage to the output voltage on the transient analysis graph and ensure that the appropriate gain is achieved and that the output voltage is greater than 3 volts peak to peak.

Measuring the drain current is as simple as placing a DC current node next to either the source resistor or the drain resistor, the current should be the same either way. Additionally, the A_{vo} gain will be calculated very similarly as the A_v gain, only the load resistor will be taken off and

the output voltage will be taken from the negative node of the capacitor. Additionally, the G_v gain will be measured in a similar fashion to the A_v gain, only the input will be measured from the function generator input. Now comes the tricky task of measuring the R_{in} and R_{out} values. The R_{in} value is measured by placing a large resistor value between the small signal input and the coupling capacitor, measuring the voltage difference across the resistor using an oscilloscope, dividing that voltage by the test resistor value to obtain the test current, and finally dividing the voltage measured on the circuit side of the test resistor by the test current in order to obtain the resistance value. The R_{out} value is measured by doing the opposite of the R_{in} value. The load resistor is disconnected from the circuit and the small signal source is connected to where the output voltage would be read. A small test resistance is placed between the small signal source and the rest of the circuit. Using an oscilloscope, voltage readings are taken on either side of the resistor. The difference of these voltages is divided by the value of the resistor in order to obtain the test current. Then the measured voltage on the circuit side of the resistor is divided by the test current in order to calculate the value of the R_{in} resistance value.

At this point it is important to compare the simulated circuit values against those that were calculated in the circuit design. The table below allows the simulated values to easily be compared against the calculated values and ensure that the simulated values are all still within the Specifications and Limitations.

Parameter	Spec & Limits	Calcs	Sim	% Error
I_D (mA)	$\leq$ 75% max transistor DC current			
A_{vo} (V/V)	N/A			N/A
A_V (V/V)	-3 V/V $\geq A_v \geq$ -30 V/V			
G_V (V/V)	N/A			N/A
R_{in} (kΩ)	$\geq$ 100 kΩ			
R_{out} (kΩ)	$\leq$ 5 kΩ			
P_D (mW)	$\leq$ 75% of max power any part			

Table 1. Comparison of calculated circuit values to the simulated values.

Now it is important to implement the circuit on a breadboard, using component values that are as close to the calculated circuit values as possible! In many cases, components can be added in series or parallel in order to accomplish a value that is very close to what it was calculated to be. Additionally, it is important that the positive node of the capacitors is facing towards the large signal portion of the circuit in order for them to create an open circuit from the perspective of the large signal circuit. Additionally, the Power Supply will be used to produce the large signal voltage as well as the grounding node for the entire circuit. Because the V_{DD} will be used for many parts of the circuit, it is logical to connect the power supply to the red and blue power and grounding strips on the breadboard. Now the Function Generator will be connected to the negative pin of the ‘CC1’ capacitor. Before checking the circuit for a gain appropriately close to the simulated gain, it is important to use a Digital Multimeter to measure the voltages and currents at the drain, gate, and source nodes of the transistor and ensure that the values are closed to what was expected. If the values are vastly different, the transistor is likely not turned on, and the circuit will need to be trouble-shot.

Measuring the parameters of the circuit is performed exactly how it was done for the measuring of the parameters during the simulation. The one difference is in determining the drain current. If the digital Multimeter were to be hooked up in series with the drain current, it would affect the actual current. The method to get around this is to measure the voltage drop across either the source resistance or the drain resistance and then divide it by the resistor value to obtain the drain current.

It is important for the analysis of the circuit to consider how close the values from the circuit in the laboratory are to those that were simulated in Multisim. The table below will laboratory values first and foremost meet the Specifications and Limitations and then will easily allow the comparison of the two sets of values obtained.

Parameter	Spec & Limits	Sim	Lab	% Error
I_D (mA)	≤ 75% max transistor DC current			
A_{vo} (V/V)	N/A			N/A
A_V (V/V)	-3 V/V ≥ A_v ≥ -30 V/V			
G_V (V/V)	N/A			N/A
R_{in} (kΩ)	≥ 100 kΩ			
R_{out} (kΩ)	≤ 5 kΩ			
P_D (mW)	≤ 75% of max power any part			

Table 2. Comparison of the simulated circuit values with those obtained from the lab circuit.

The construction of the circuit on the breadboard marks the completion of the first portion of the laboratory exercise; however, there is still the design, simulation, and implementation of the buffering circuit- that will eventually be connected to the output of the first circuit- left to complete.

The buffering circuit theoretically produces a gain of 1 V/V and will be accomplished with a common drain amplifier in this laboratory exercise. Initially, this portion of the circuit may seem pointless, but after analyzing what value of resistors the output voltage can be read across, the application of the circuit will become much clearer. Essentially, the buffering amplifier allows for the load to occur with a lower load resistance, such as 50 Ω, which is much more common in applications than 100 KΩ.

The approach towards the common-drain buffer is very similar to the approach towards the common source amplifier. While designing the common drain buffer, it is beneficial to design it separate to ensure that it is working as expected and then connect it to the output of the common-source amplifier circuit.

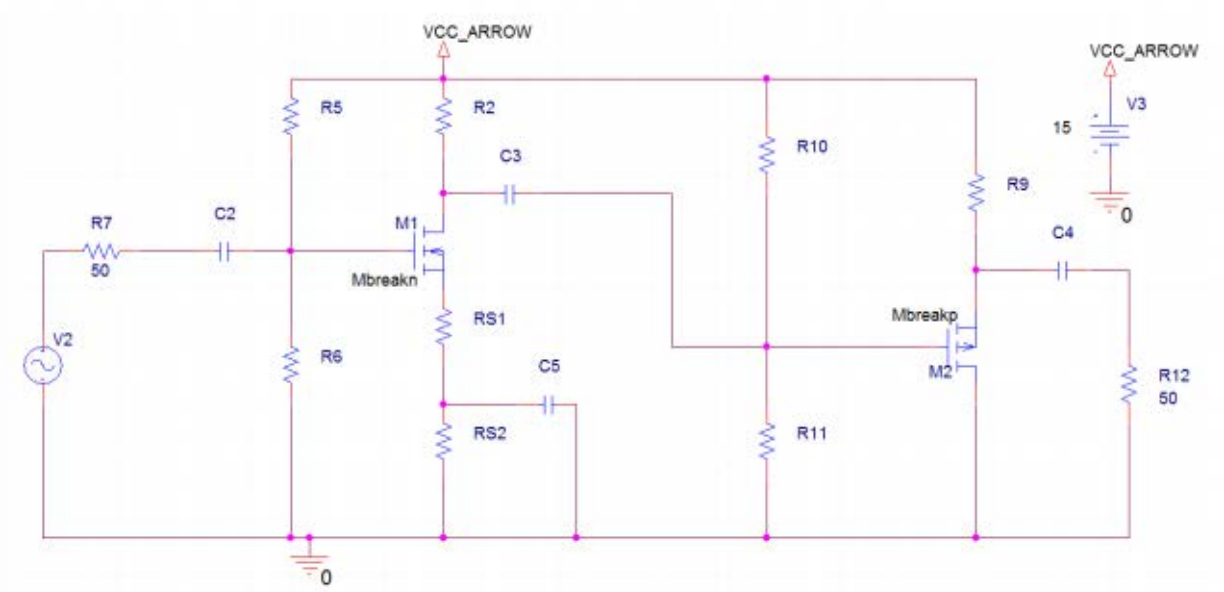

Figure 5. Common-source amplifier with source resistor cascaded with a common-drain buffer.

The figure above demonstrates how the pMOS FET with a common-drain configuration will be cascaded off the output of the nMOS FET with a common-source and source resistor configuration. The approach to the pMOS FET with a common-drain configuration circuit will begin with the analyzation of the large signal circuit. Similarly to the common-source amplifier circuit, the common-drain circuit results in the large signal circuit seen in Figure 5 because of the capacitors.

<u>Large Signal Equations:</u>

11) $V_G = \left(\frac{RG2}{RG1+RG2}\right) V_{DD}$

12) $V_S = V_{DD} - I_D R_S$

13) $V_D = 0$

14) $I_D = \frac{1}{2} k(V_{ov})^2 = \frac{1}{2} k(V_{GS} - V_t)^2$

A biasing scheme can now be determined using equations 11-15, which were derived from the large signal model circuit in Figure 5. Because the drain pin of the transistor is grounded, V_D can effectively be determined to be at 0 volts. Additionally, because the Specifications and Limitations specified that V_{SD} should be roughly half of the V_{DD}, V_S can be calculated to be half of V_{DD}. The Specifications and Limitations also request that the drain current of the pMOS FET be set to about 60 mA, meaning that because k and V_t have already been specified to 250 mA/V^2 and -2 V, respectively, the drain current will have to be set by V_{GS}. Equation 14 can be solved to achieve both a

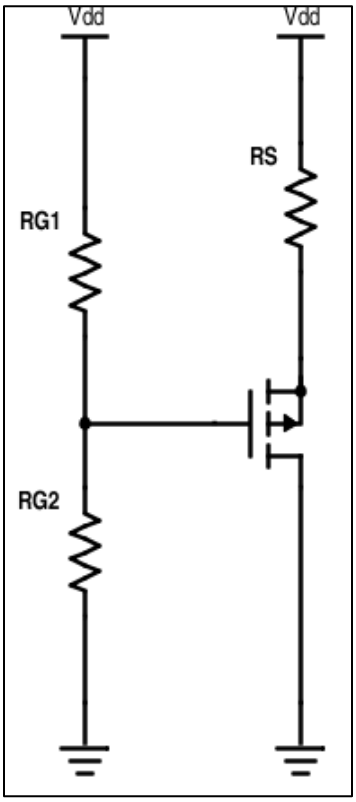

Figure 6. Large Signal Model circuit of the pMOS FET in the common-drain configuration.

positive and negative value for V_{OV}. Both values need to be analyzed in order to determine what value will result in the magnitude of V_{GS} being larger than that of V_t. Once the correct V_{OV} value is determined, the correct V_G can be determined and Equation 11 can be used in order to solve for resistors R_{G1} and R_{G2}. When choosing values for these resistors, values in the MΩ order of magnitude should be used in order to achieve a R_{in} value larger than 100 KΩ. Wrapping up the analysis of the large signal circuit, Equation 12 can be used to solve for the resistor R_S now that all other values are determined.

Moving on to the small signal model circuit, the figure below shows all the circuit components affected by the small signal input.

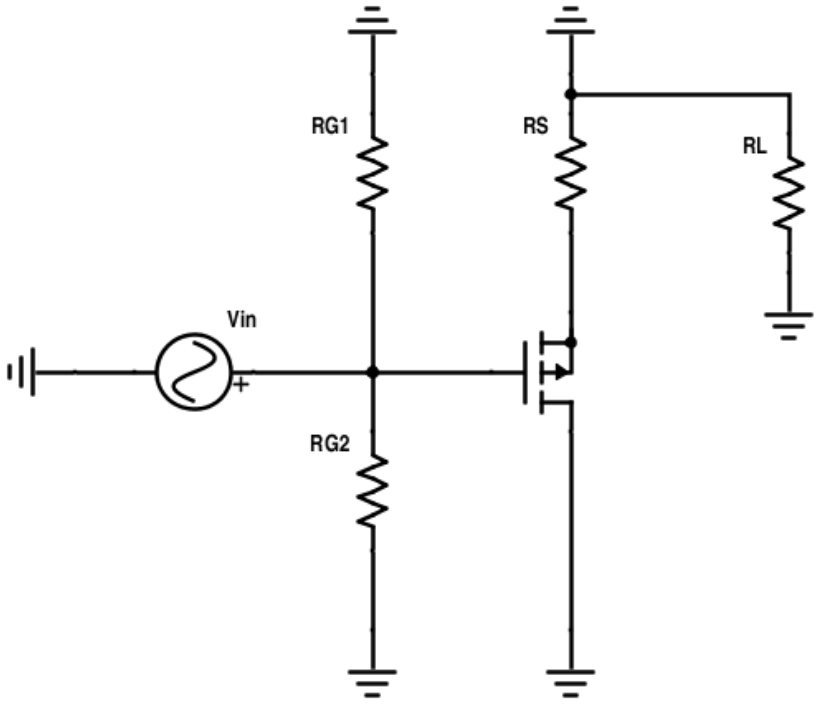

Figure 7. Smal Signal Model circuit of the pMOS FET in the common-drain configuration.

Although the figure above shows all the circuit components affected by the small signal input, a hybrid-pi model must be analyzed before the small signal circuit equations can affectively be derived.

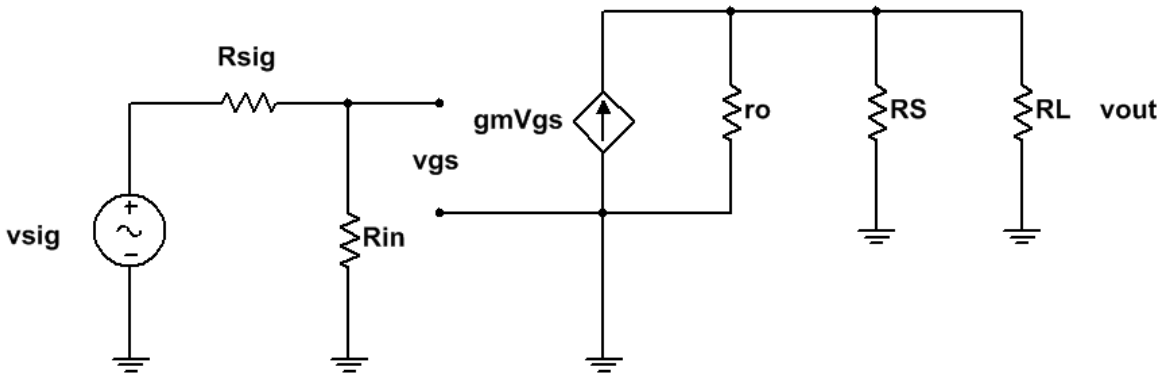

Figure 8. The hybrid-pi model of the Small Signal Operation of the pMOS FET in the common-drain configuration.

Using node voltage analysis, the following small signal equations can be derived from the hybrid-pi model. During the design process, because r_o and R_S will be much larger than R_L and all three resistors are in parallel, r_o and R_S can be taken out of the equations to simplify the design process. Assuming $r_o >> R_S >> R_L$, the following equations result:

Small Signal Equations:

15) $g_m = kV_{ov} = \frac{2I_D}{V_{ov}}$

16) $A_v = \frac{g_m R_L}{1+ g_m R_L}$

17) $A_{vo} = 1$

18) $G_v = A_v$

19) $R_{in} = \frac{RG1*RG2}{RG1+RG2}$

20) $R_{out} = \frac{1}{g_m}$

It is necessary to begin with Equation 15 to determine the g_m value. At this point it is now possible to calculate the A_v gain of the second stage amplifier using Equation 16. It is important that the second stage gain multiplied by the gain of the first stage amplifier is within -3V/V to -30V/V of gain. Now it is important to calculate the R_{in} and R_{out} using Equations 19 and 20 respectively in order to ensure that the R_{in} is greater than 100 KΩ and that the R_{out} is less than 5 KΩ as specified by the Specifications and Limitations. Now that the second stage of the circuit has been verified, it is time to connect the two circuits.

Connecting the two circuits is as simple as disconnecting the 100 KΩ load resistor from the first stage and connecting that output voltage to the input of the second stage of the circuit. Now it is

important to ensure that the two circuits work together in simulation to meet the Specifications and Limitations for the entire circuit. The A_v gain of the overall circuit should be between -3V/V and -30 V/V while the output voltage from the amplifiers should be greater than 3 volts peak to peak. Use the same techniques for measuring the circuits second stage as were used for measuring the circuits first stage.

After measuring all the parameters on the simulated circuit, it is important to compare those values with those that were calculated in order to analyze whether the simulated circuit still meets the Specifications and Limits.

Parameter	Spec & Limits	Calcs	Sim	% Error
I_D (mA)	≤ 75% max transistor DC current			
A_{vo} (V/V)	For the CD amp only			N/A
A_V (V/V)	For the CD amp only			
G_V (V/V)	For the CD amp only			N/A
R_{in} (kΩ)	≥ 100 kΩ			
R_{out} (kΩ)	≤ 5 kΩ			
P_D (mW)	≤ 75% of max power any part			

Table 3. Comparison of calculated circuit values to the simulated values.

Similar to connecting the first stage of the circuit, construct the second stage of the circuit being careful to use component values as close to those used in the simulation. Utilize the digital Multimeter in order to ensure that the values are what were expected. Connect the two circuits by removing the load resistor of the first circuit and connecting the output voltage of the first circuit to the input of the second circuit.

After connecting the two circuits to produce a single two gain stage amplifier circuit, begin measuring the circuit parameters much like the first circuit in order to analyze the circuit to ensure it meets the Specifications and Limitations. Populate the table below to compare how close the achieved values are to those that were set out to create!

Parameter	Spec & Limits	Sim	Lab	% Error
I_D (mA)	≤ 75% max transistor DC current			
A_{vo} (V/V)	For the CD amp only			N/A
A_V (V/V)	For the CD amp only			
G_V (V/V)	For the CD amp only			N/A
R_{in} (kΩ)	≥ 100 kΩ			
R_{out} (kΩ)	≤ 5 kΩ			
P_D (mW)	≤ 75% of max power any part			

Table 4.

Design

After covering the approach of the laboratory circuit design in great detail, the actual design of the circuit becomes much easier. The laboratory handout instructed that the circuit should be designed with k = 250 mA/V^2 and V_t = 2V. Although the estimated k and V_t values are not

entirely accurate to the BS – 170, the actual circuit will be slightly different than what is expected, but will get us moving in the right direction. Using the biasing scheme outlined in the approach and 15 V for V_{DD}, the following voltages are calculated.

Biasing Scheme:

$V_{DD} = 15\ V$

$\frac{2}{5}\ V_{DD}$ across R_D, $\frac{1}{5}\ V_{DD}$ across V_{DS} channel, $\frac{2}{5}\ V_{DD}$ across R_S

$V_D = 9\ V, V_S = 6\ V$

Now, choosing a drain current of 2 mA to avoid achieving too high of a power dissipation across any circuit element, the following possible over drive voltages are calculated.

Choose I_D = 2 mA:

$$I_D = \frac{1}{2}k(V_{ov})^2$$

$$2\ mA = \frac{1}{2}(250\ \frac{mA}{V^2})(V_{ov})^2$$

$$V_{ov} = \pm 0.126\ V$$

Analyzing both overdrive voltages, we find the correct voltage that results in the transistor correctly biased in saturation.

1) $V_{ov} = V_G - V_S - V_t = 0.126\ V$
$V_{ov} = V_G - 6V - 2V = 0.126\ V$
$V_G = 8.126\ V$
$V_{GS} = 2.126\ V$
$V_{GS} > V_t$
$|V_{DS}| > |V_{ov}|$
Transistor is on because $V_{GS} > V_t$

2) $V_{ov} = V_G - V_S - V_t = -0.126\ V$
$V_{ov} = V_G - 6V - 2V = -0.126\ V$
$V_G = 7.874\ V$
$V_{GS} = 1.874\ V$
$V_{GS} < V_t$
$|V_{DS}| > |V_{ov}|$
Transistor is off because $V_{GS} < V_t$

We can now begin calculating the resistor values that will cause the voltage biasing scheme to become true.

Choosing R_{G1} and R_{G2} values:

$$V_G = \left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right) V_{DD}$$

$$8.126\ V = \left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right) 15\ V$$

$$\left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right) = \frac{8.126\ V}{15\ V}$$

If R_{G2} = 1MΩ, then R_{G1} = 846kΩ

Calculating R_D:

$V_D = V_{DD} - I_D R_D$

9V = 15V – (2mA) R_D

R_D = 3kΩ

Calculating R_S:

$V_S = I_D(RS1 + RS2)$

6V = 2mA(R_{S1} + R_{S2})

R_{S1} + R_{S2} = 3kΩ

Using the calculated resistance values and those set by the circuit specifications; we can now calculate R_{in} and R_{out} to ensure that they are over 100 KΩ and under 5 KΩ, respectively.

Calculating R_{in}:

$$R_{in} = \frac{RG1*RG2}{RG1+RG2}$$

$$R_{in} = \frac{846k\Omega*1M\Omega}{846k\Omega+1M\Omega}$$

$$R_{in} = 458\ k\Omega$$

Calculating R_{out}:

$$R_{out} = \frac{R_D * R_L}{R_D + R_L}$$

$$R_{out} = \frac{3k\Omega * 100k\Omega}{3k\Omega + 100k\Omega}$$

$$R_{out} = 2.91\ k\Omega$$

Moving on to the small circuit model analysis, we can set an appropriate A_v gain that meets requirements, calculate the other gains with the given circuit values, and calculate the R_{S1} and R_{S2} values.

Calculating g_m:

$$g_m = kV_{ov}$$

$g_m = (250mA/V^2)(126\ mV)$

$g_m = 31.5mA/V$

Calculating A_v:

$$A_v = \frac{-g_m(R_D||R_L)}{1+g_mR_{s1}}$$

Choose A_v = -10V/V:

$$-10V/V = \frac{-\left(\frac{31.5mA}{V}\right)(3k\Omega||100k\Omega)}{1+\left(\frac{31.5mA}{V}\right)*R_{s1}}$$

$R_{S1} = 260\Omega$

So: $R_{S2} = 2.74k\Omega$

Calculating A_{vo}:

$$A_{vo} = \frac{-g_m*R_D}{1+g_mR_{s1}}$$

$$A_{vo} = \frac{-\left(\frac{31.5mA}{V}\right)*3k\Omega}{1+\left(\frac{31.5mA}{V}\right)*260\Omega}$$

A_{vo} = -10.28V/V

Calculating G_v:

$$G_v = A_v\left(\frac{R_{in}}{R_{in}+R_{sig}}\right)$$

$$G_v = -9.99\ V/V$$

It is important to simulate the designed circuit before constructing the circuit on the breadboard because the simulation will likely highlight any design flaws and will save time in the long run as you will know whether your design meets Specifications and Limitations before building the circuit. Additionally, ensure that the Multisim circuit's k and V_t values are changed to those specified in the circuit design.

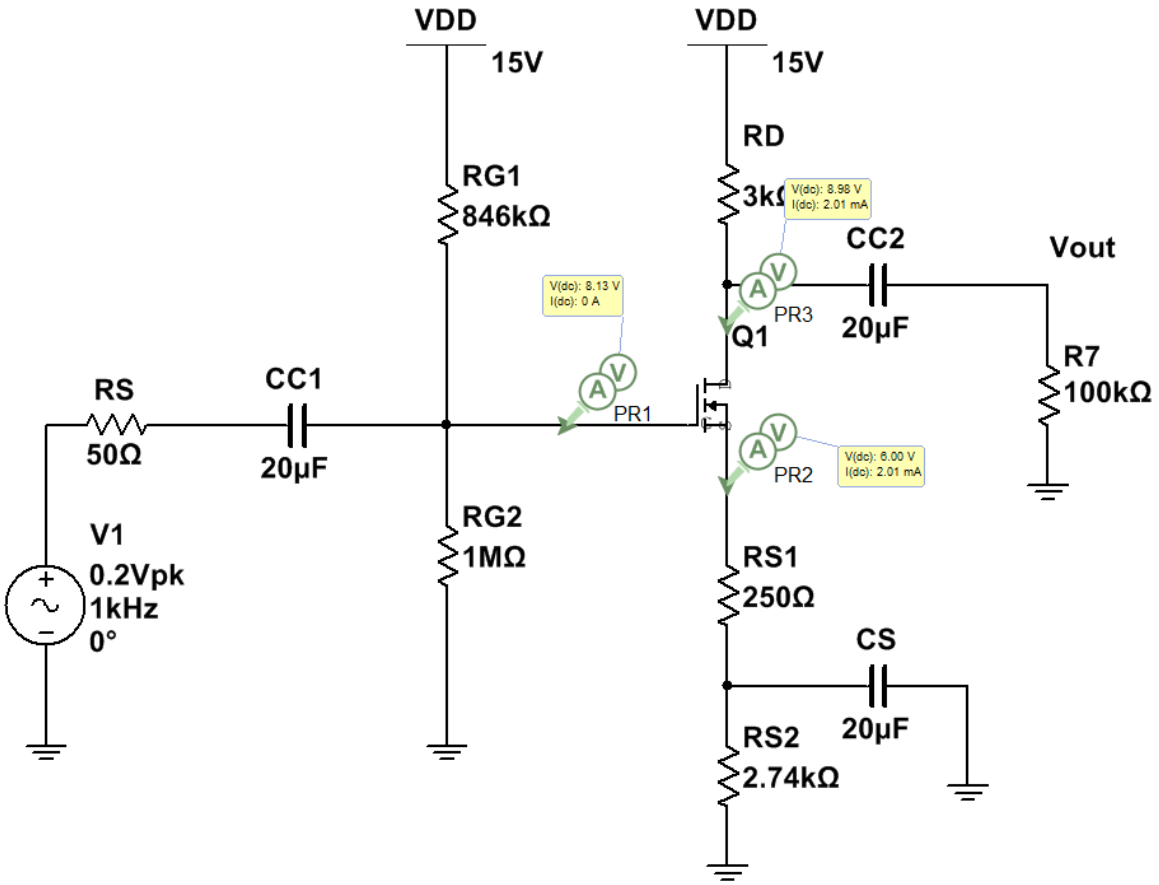

Figure 9. Multisim schematic of the first stage of the circuit.

In order to verify the circuit meets the Specifications and Limitations, a transient analysis needs to be performed as described in the Approach section. The analysis of the A_v gain below can serve as an example of how the other circuit parameters can be analyzed.

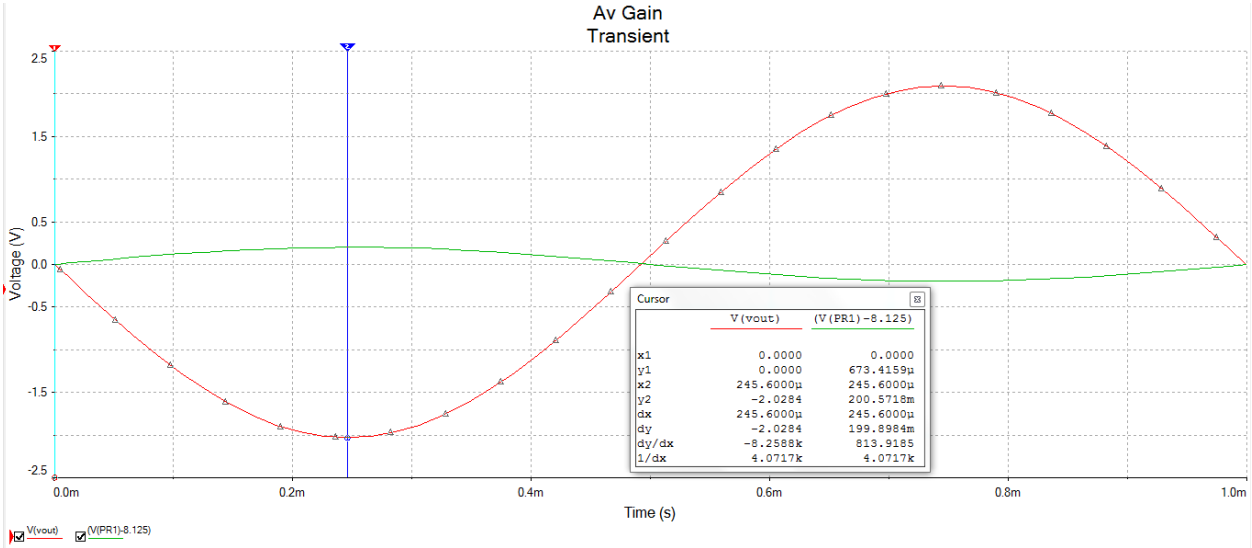

Figure 10. Transient analysis of the A_v gain for the first stage of the circuit.

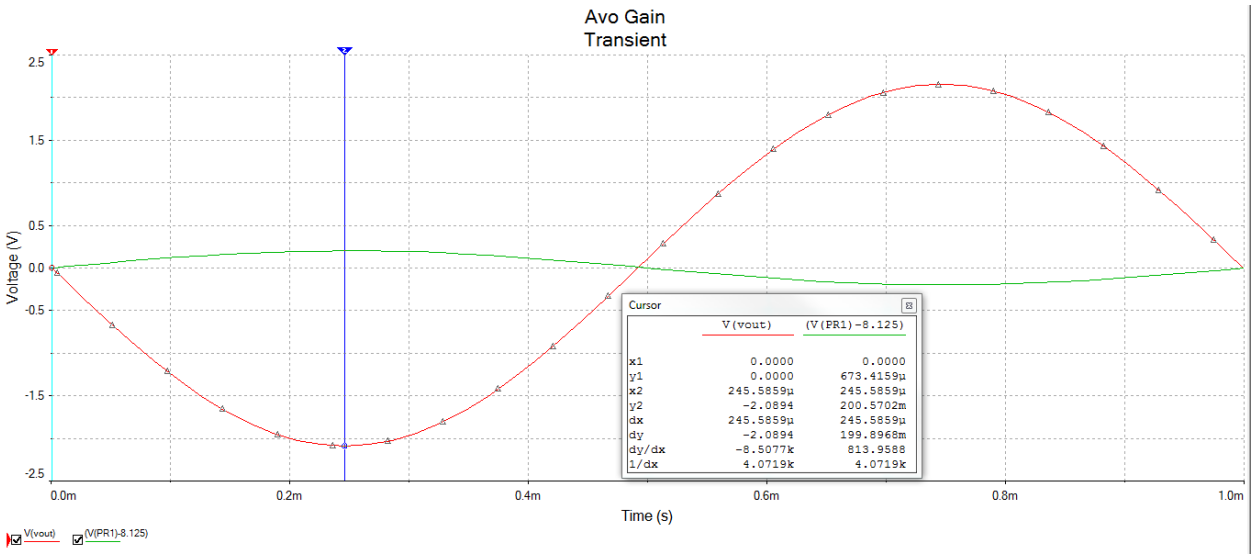

Figure 11. Transient analysis of the A_{vo} gain for the first stage of the circuit.

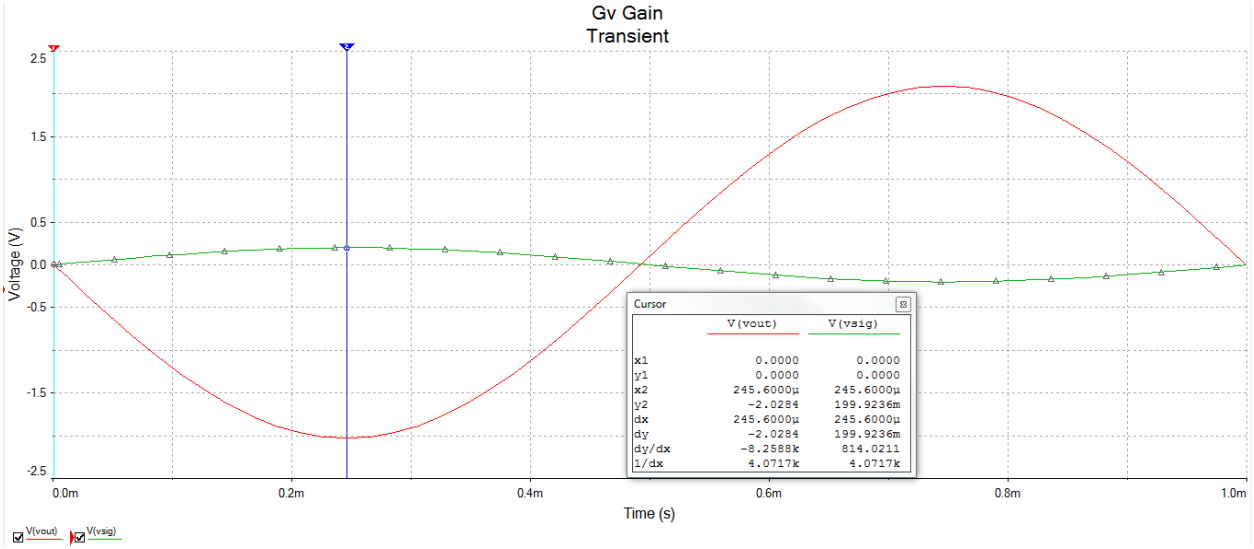

Figure 12. Transient analysis of the G_v gain for the first stage of the circuit.

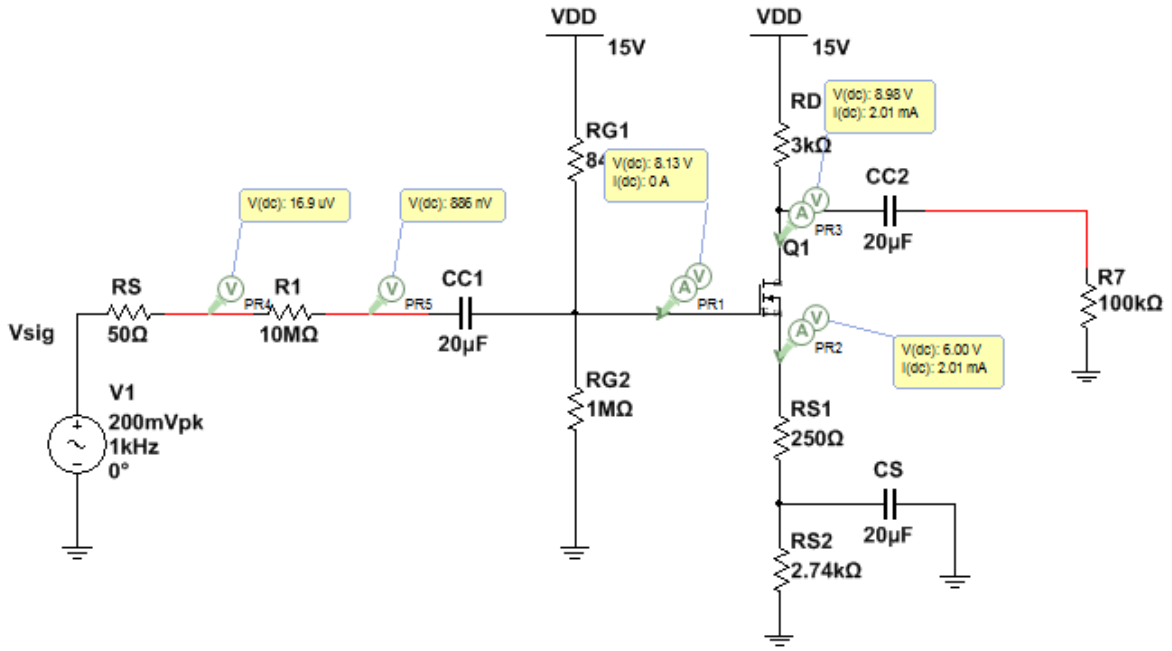

Figure 13. Circuit set up for Rin measurement of the first stage of the circuit.

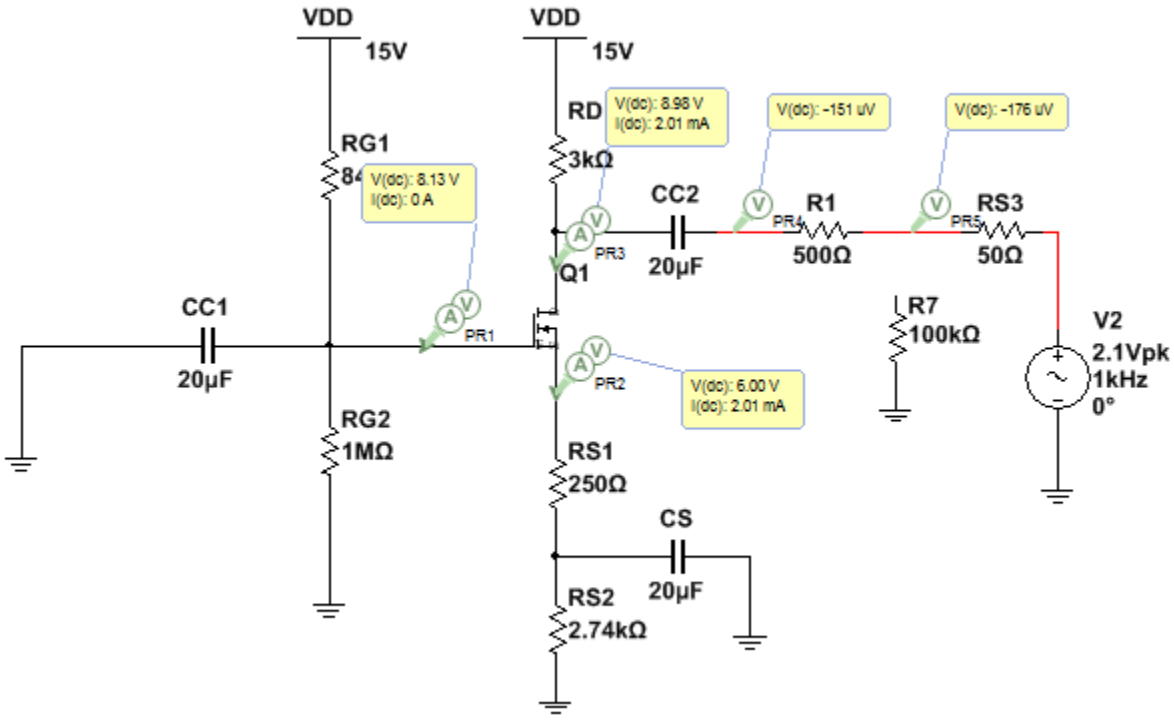

Figure 14. Circuit configuration for the Rout measurement for the first stage of the circuit.

Parameter	Spec & Limits	Calcs	Sim	% Error
I_D (mA)	≤ 75% max transistor DC current	2.00	2.01	0.5
A_{vo} (V/V)	N/A	-10.28	-10.41	N/A
A_V (V/V)	-3 V/V ≥ A_v ≥ -30 V/V	-10	-10.11	1.1
G_V (V/V)	N/A	-9.99	-10.15	N/A
R_{in} (kΩ)	≥ 100 kΩ	458	552	20.52
R_{out} (kΩ)	≤ 5 kΩ	2.91	3.00	3.09
P_D (mW)	≤ 75% of max power any part	X	X	X

Table 5. Comparison of calculated circuit values to the simulated values.

With the Multisim simulation using approximate values for k and V_t, it cannot be expected to produce values accurate to those in implementation. Using a device characterization machine, I characterized the transistor and found its actual values.

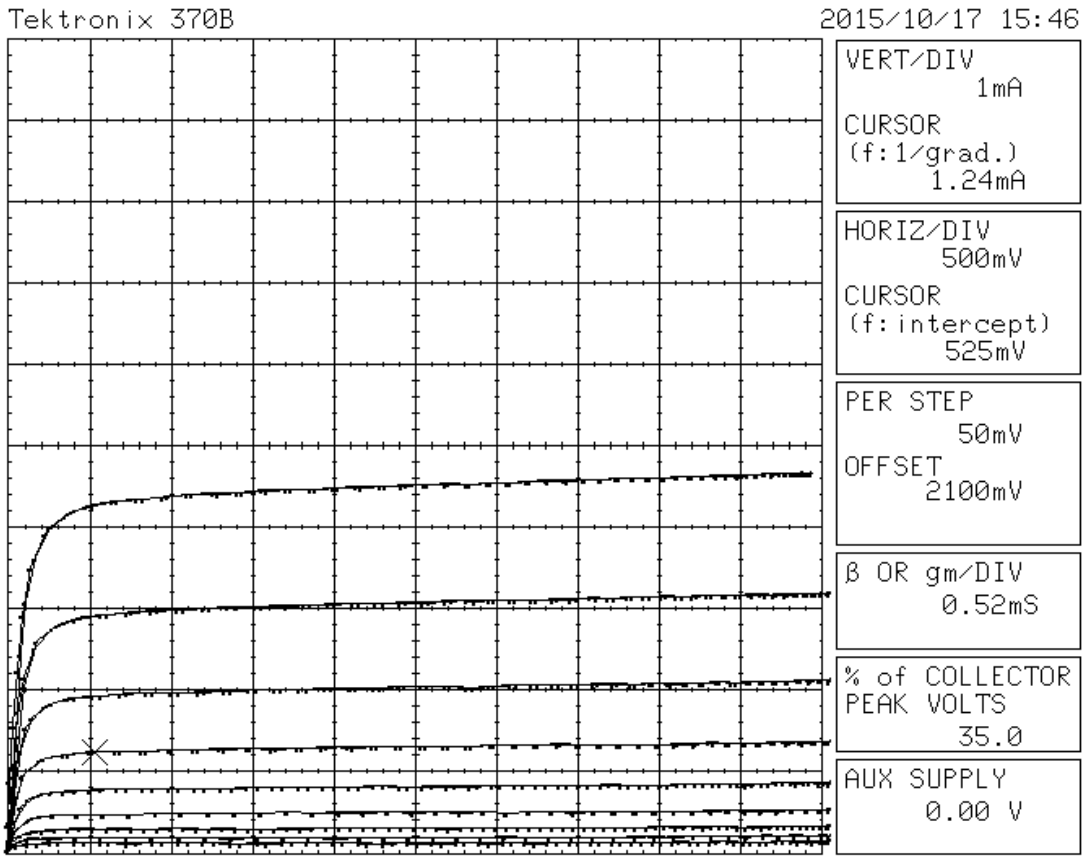

Figure 15. A screen shot of the device characterization machine.

Using the machine, I found the BS-170's actual values are:
V_t = 2.1 V
r_o = 27.857 kΩ
V_A = 55.7 V
g_m = 40 mA/V
k = 317 mA/V^2

With the first stage working according to the Specifications and Limitations, it is time to design and simulate the second stage to get it working as required. Following the design as outlined in the Approach section, we begin with setting the biasing scheme.

Given: $k = 250\ mA/V^2$ $V_t = -2V$ $R_L = 50\Omega$

Biasing Scheme:
$V_{DD} = 15\ V$
$V_D = 0\ V, V_S = 7.5\ V$

Now setting the drain current to 60 mA, we will calculate the over drive voltage that will produce this current.

Choose $I_D = 60\ mA$:

$$I_D = \frac{1}{2}k(V_{ov})^2$$
$$60\ mA = \frac{1}{2}(250\ \frac{mA}{V^2})(V_{ov})^2$$
$$V_{ov} = \pm 0.693\ V$$

Solving for V_{GS} using both values, we will be able to determine the overdrive voltage that results in a transistor in saturation.

1) $V_{ov} = V_G - V_S - V_t = 0.693\ V$
$V_{ov} = V_G - 7.5V + 2V = 0.693\ V$
$V_G = 6.193\ V$
$V_{GS} = -1.307\ V$
$|V_{GS}| > |V_t|?$
Transistor is off

2) $V_{ov} = V_G - V_S - V_t = -0.693\ V$
$V_{ov} = V_G - 7.5V + 2V = -0.693\ V$
$V_G = 4.807\ V$
$V_{GS} = -2.693\ V$
$|V_{GS}| > |V_t|?$
Transistor is on

Now that we have found biasing voltages that will produce a transistor in saturation, we can begin choosing resistor values that will produce these biasing voltages.

Choosing R_{G1} and R_{G2} values:

$$V_G = \left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right) V_{DD}$$
$$4.807\ V = \left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right) 15\ V$$
$$\left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right) = \frac{4.807\ V}{15\ V}$$

If $R_{G2} = 1M\Omega$, then $R_{G1} = 2.12M\Omega$

Calculating R_S:

$$V_S = V_{DD} - I_D R_S$$
$$7.5V = 15V - (60mA)R_S$$
$$R_S = 125\Omega$$

Now we will do a few quick calculations to ensure that the resistances are within Specifications and Limitations.

Calculating R_{in}:

$$R_{in} = \frac{RG1 * RG2}{RG1 + RG2}$$

$$R_{in} = \frac{2.12M\Omega * 1M\Omega}{2.12M\Omega + 1M\Omega}$$

$$R_{in} = 679\ k\Omega$$

Calculating R_{out}:

$$R_{out} = \frac{1}{g_m}$$

$$R_{out} = \frac{1}{173.25mA/V}$$

$$R_{out} = 5.77\ \Omega$$

At this point we can begin solving for the small circuit parameters, including all of the different types of gain.

Calculating g_m:

$$g_m = kV_{ov}$$

$g_m = (250mA/V^2)(-693\ mV)$

$g_m = -173.25mA/V$

Calculating A_v:

$$A_v = \frac{g_m R_L}{1 + g_m R_L}$$

$$A_v = \frac{\left(\frac{-173.25mA}{V}\right)50\Omega}{1 + \left(\frac{-173.25mA}{V}\right)50\Omega}$$

$$A_v = 1.13\ V/V$$

Calculating A_{vo}:

$$A_{vo} = 1$$

Calculating G_v:

$$G_v = A_v$$

$$G_v = 1.13\ V/V$$

At this point it is time to simulate our designed circuit to ensure that the values achieved are nearly what we calculated. Additionally, it is important to change the k and V_t values of the pMOS FET to those that we designed the circuit with.

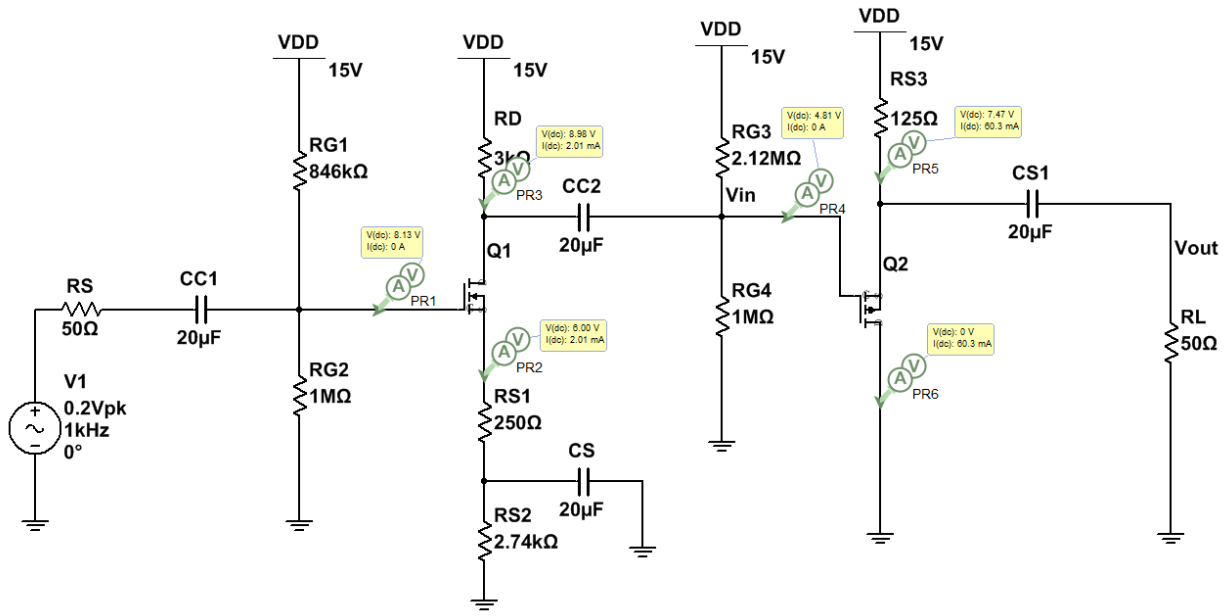

Figure 16. Fully designed circuit with second stage connected to the first stage.

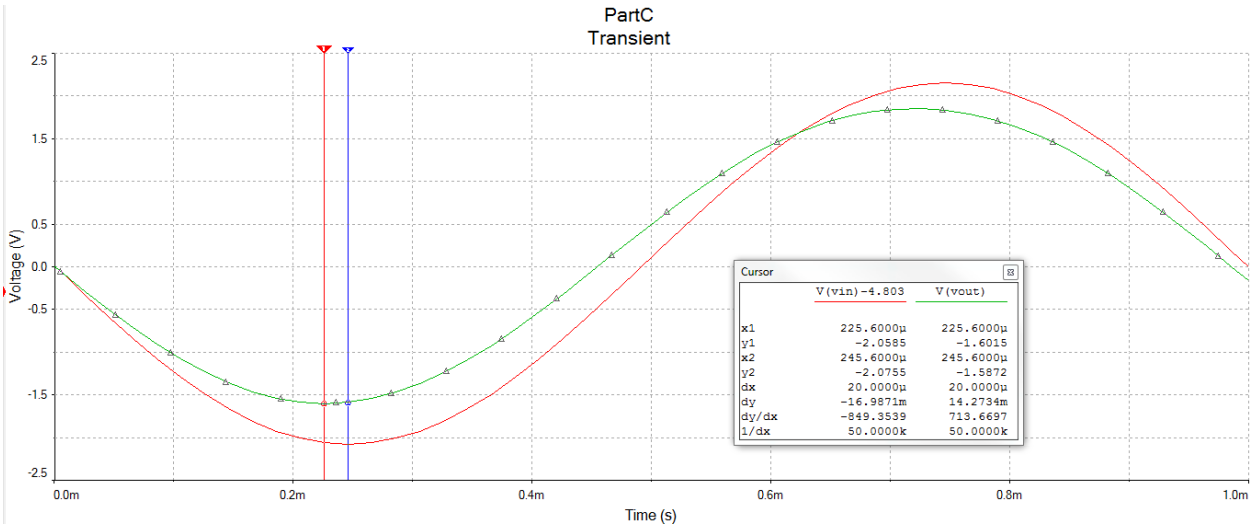

Figure 17. Simulated waveform for the A_v gain of the second stage of the circuit.

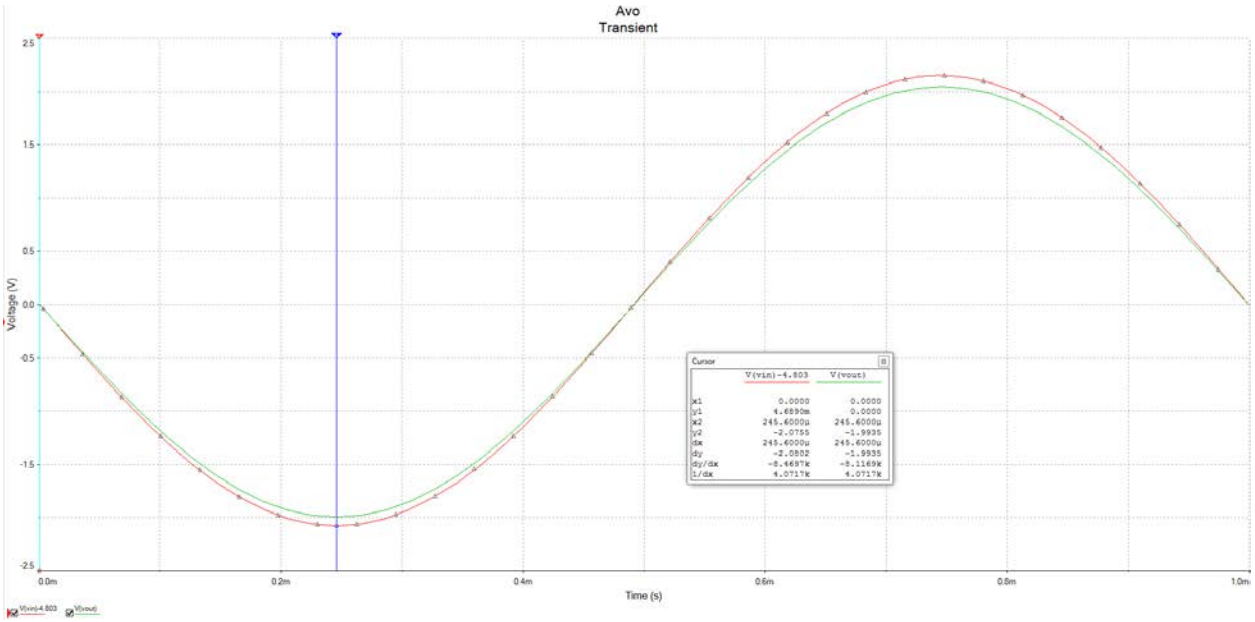

Figure 18. Simulated waveform for the A_{vo} gain of the second stage of the circuit.

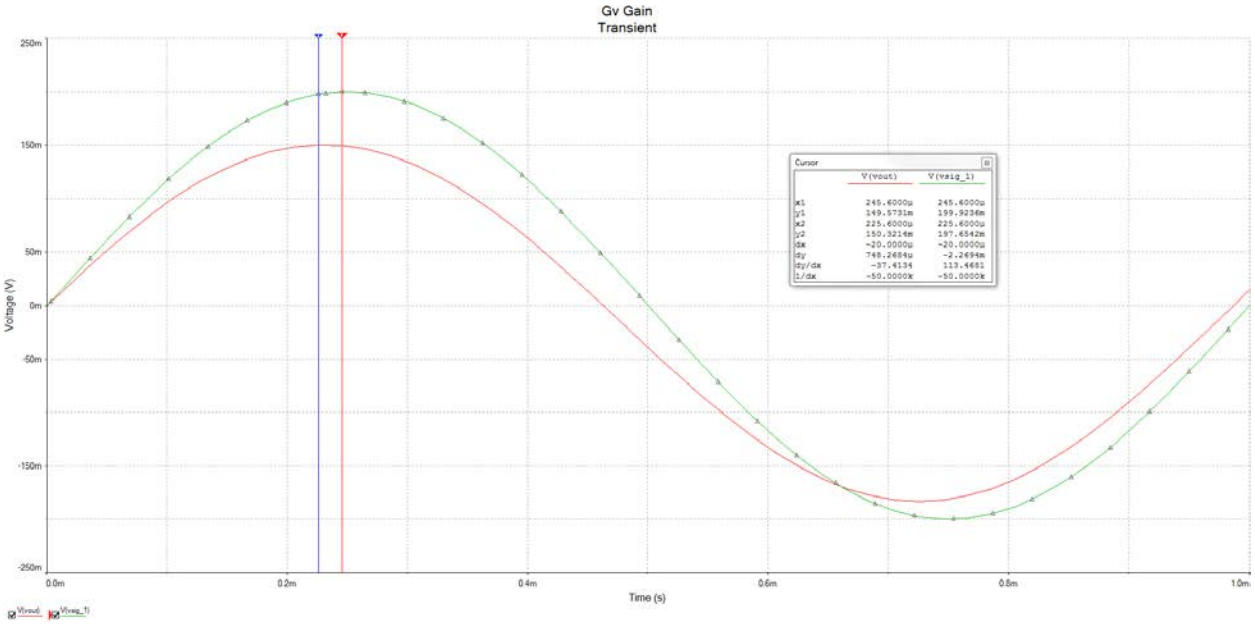

Figure 19. Simulated waveform for the G_v gain of the second stage of the circuit.

Parameter	Spec & Limits	Calcs	Sim	% Error
I_D (mA)	≤ 75% max transistor DC current	60	60.3	0.5
A_{vo} (V/V)	For the CD amp only	1	0.96	N/A
A_V (V/V)	For the CD amp only	1.13	0.77	31.8
G_V (V/V)	For the CD amp only	1.13	0.76	N/A
R_{in} (kΩ)	≥ 100 kΩ	679	588	13.4
R_{out} (Ω)	≤ 5 kΩ	5.77	7.81	35.35
P_D (mW)	≤ 75% of max power any part	X	X	X

Table 6. Simulated parameter values for the second stage of the circuit.

With the Multisim simulation using approximate values for k and V_t, it cannot be expected to produce values accurate to those in implementation. Using a device characterization machine, I characterized the transistor and found its actual values.

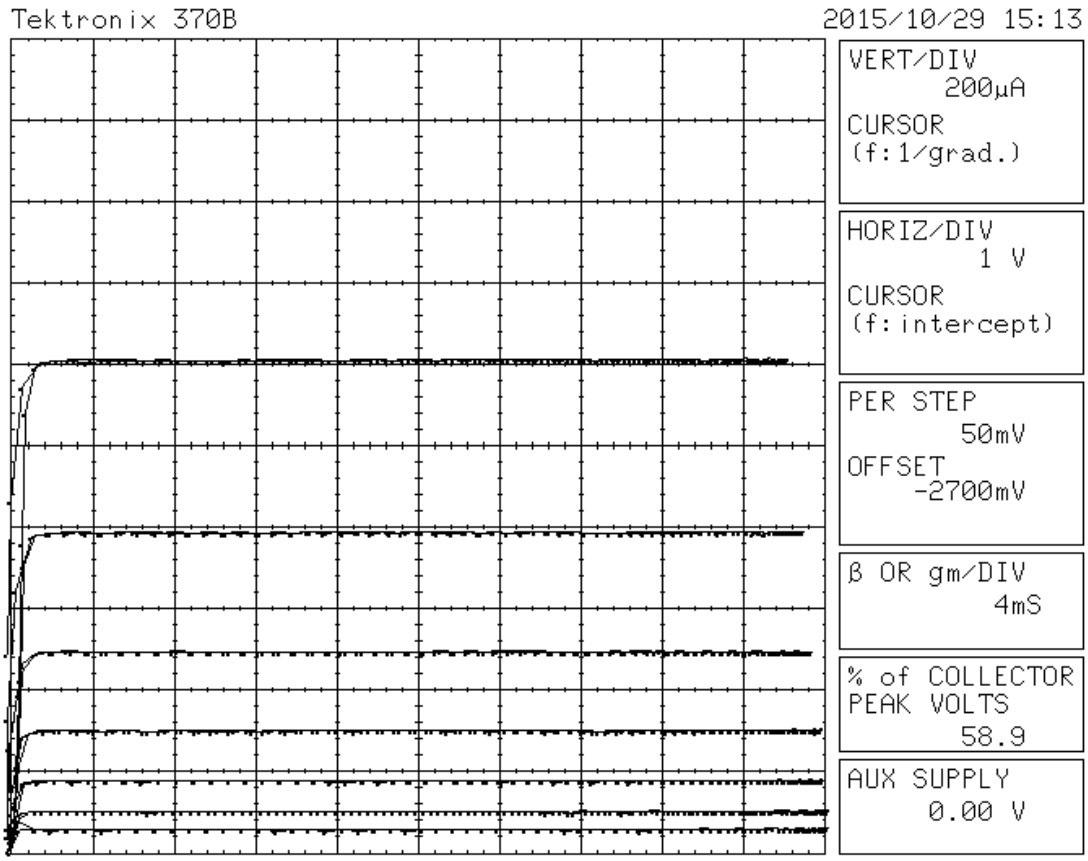

Figure 20. A screen shot of the device characterization machine characterizing the BS-250.

Using the machine, I found the BS-170's actual values are:
V_t = -2.7 V
r_o = 20.859 kΩ
V_A = 98.7 V
g_m = 400 mA/V
k = 577 mA/V^2

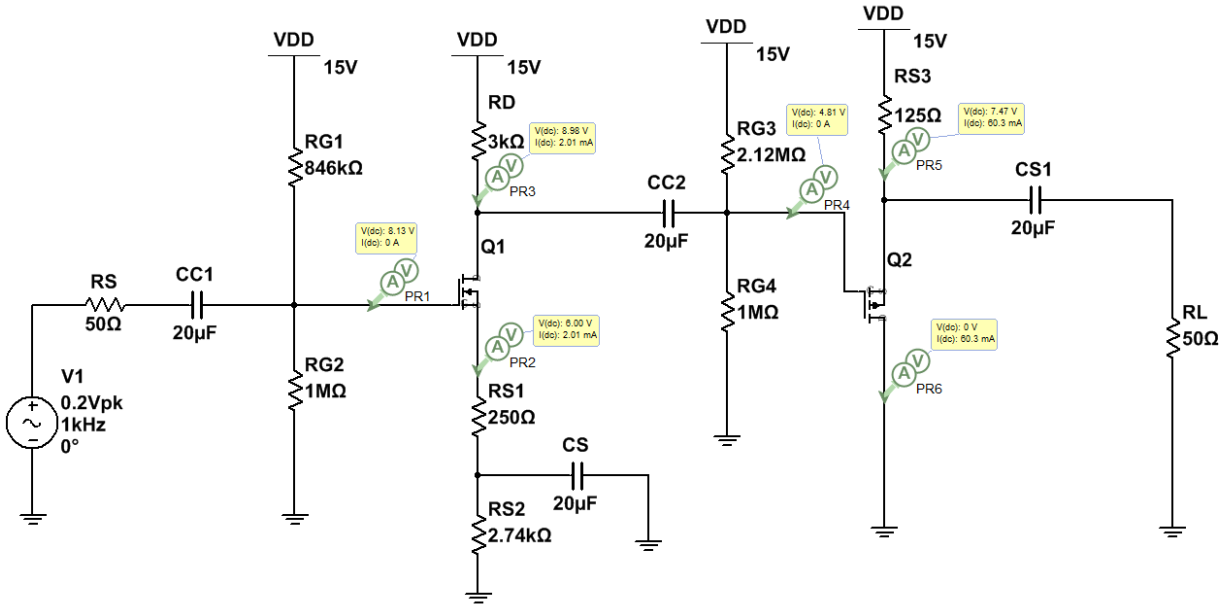

Figure 21. Final schematic with all of the component types and values.

Parameter	Spec & Limits	Calcs	Sim	% Error
I_D (mA)	≤ 75% max transistor DC current	60	60.3	0.5
I_D (mA)	≤ 75% max transistor DC current	2	2.01	0.5
A_{vo} (V/V)	N/A	-10.28	-9.94	N/A
A_V (V/V)	-3 V/V ≥ A_v ≥ -30 V/V	-11.3	-8.07	28.6
G_V (V/V)	N/A	-11.2	-8.10	N/A
R_{in} (kΩ)	≥ 100 kΩ	458	552	20.52
R_{out} (Ω)	≤ 5 kΩ	5.77	7.81	35.35
P_D (mW)	≤ 75% of max power any part	X	X	N/A

Table 7. Simulated parameter values for the entirety of the circuit.

The final schematic of the two amplifier stages put together with all circuit component values are demonstrated above in Figure 19. Additionally, Table 7 shows the parameter values for the entirety of the circuit. Although the simulated circuit parameters contain a percent error as high as 35%, the simulated parameters are still well within the circuit Specifications and Limitations! The next step is to build this circuit to verify that it performs according to our simulations.

Implementation

With the construction of the circuit, many complications arose. Beginning with the first portion of the circuit, the circuit was easily built using the Multisim schematic as a guide. During this portion, the physical component values were chosen as close to the design values as possible, in some cases, resistors were added in series to achieve the closest possible value. Below are images demonstrating how the circuit was constructed and tested.

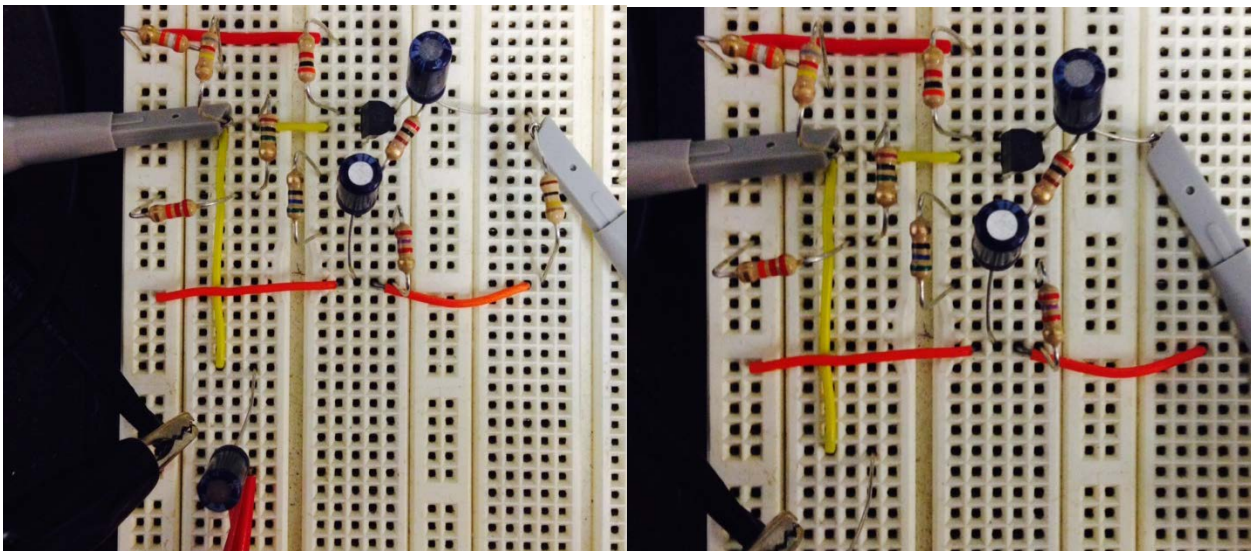

Figure 22. The breadboard construction and node connections for the measurement of the A_v gain shown on the left and the A_{vo} gain on the right.

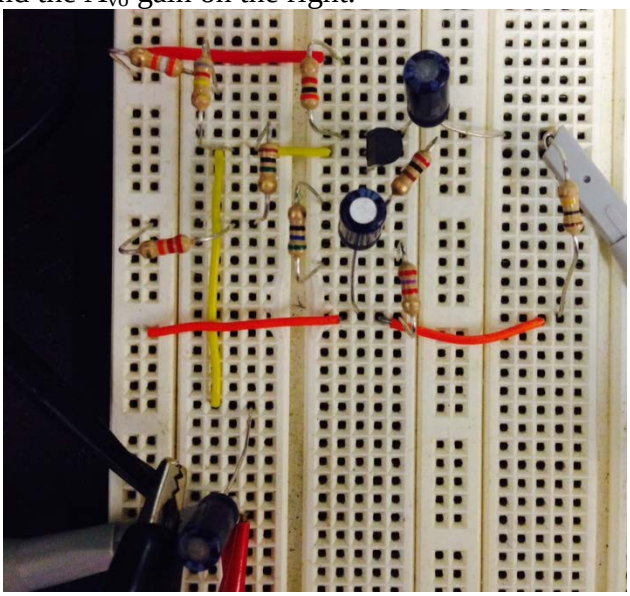

Figure 23. The breadboard construction and node connections G_v gain.

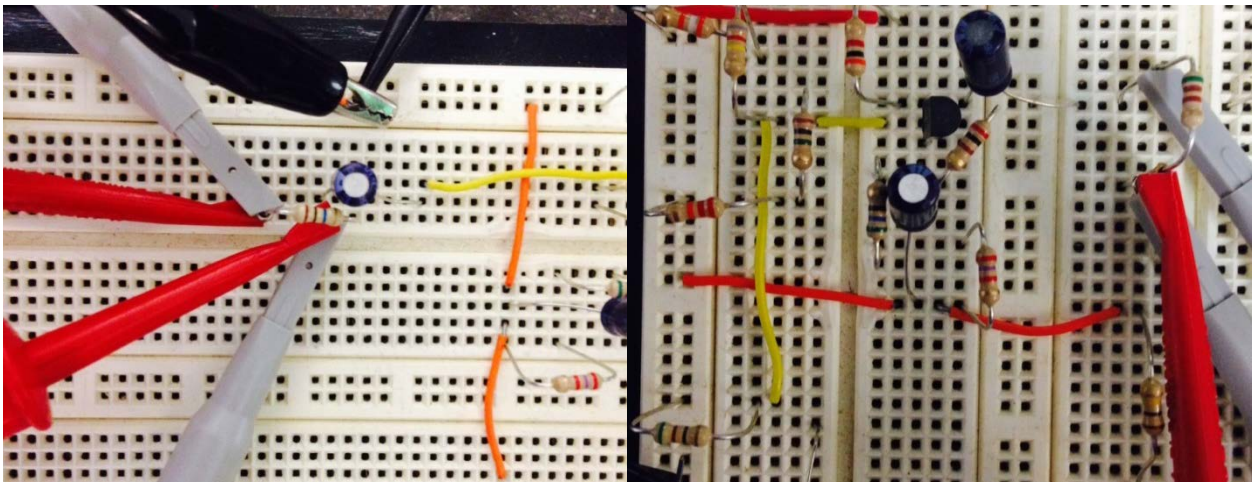

Figure 24. The breadboard construction and node connections for the measurement of the R_{in} shown on the left and the R_{out} on the right.

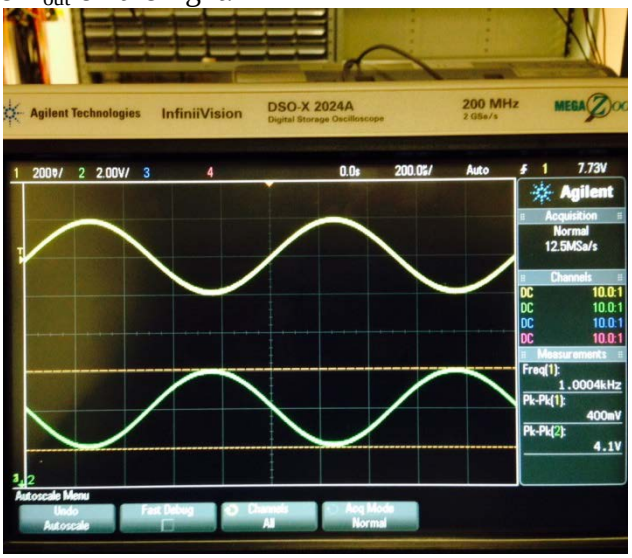

Figure 25. Oscilloscope screenshot demonstrating the A_v gain. This brief inspection suggests that the circuit performs as designed.

Because the first stage of the circuit appears to work as designed, we can now move on to the construction of the second stage of the design. The implementation of the second stage was a little more tricky first because the source resistance value had to be created out of parallel resistors so that the power dissipated did not exceed 250mW per resistor and the gate voltage had to be lowered by decreasing the R_{G1} of the second stage by 500 KΩ.

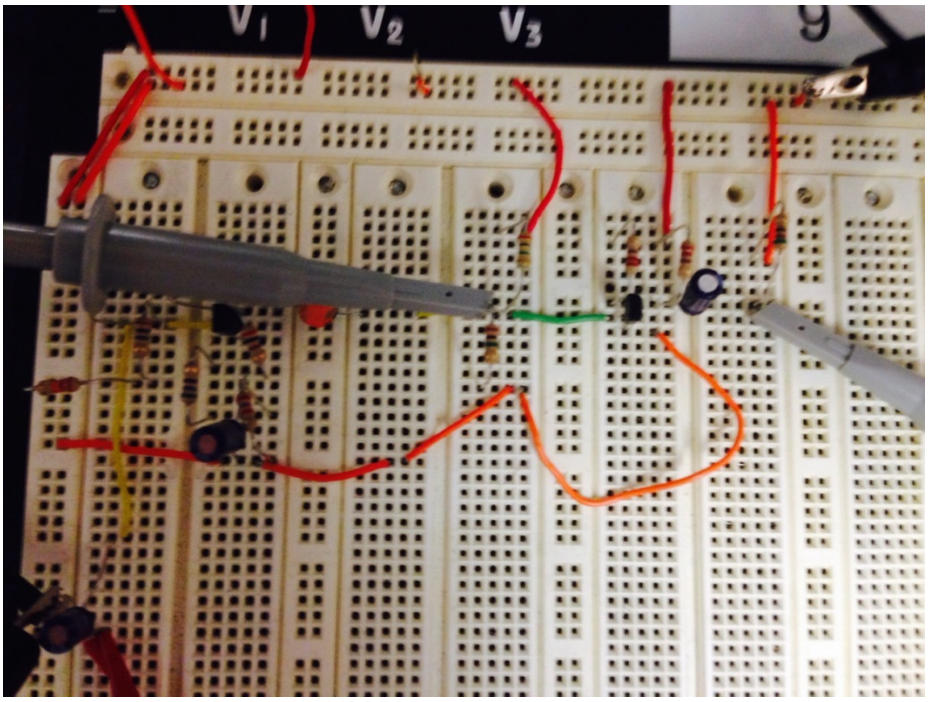

Figure 26. Second stage circuit construction and set-up showing nodes placed for measuring the second stage A_v gain.

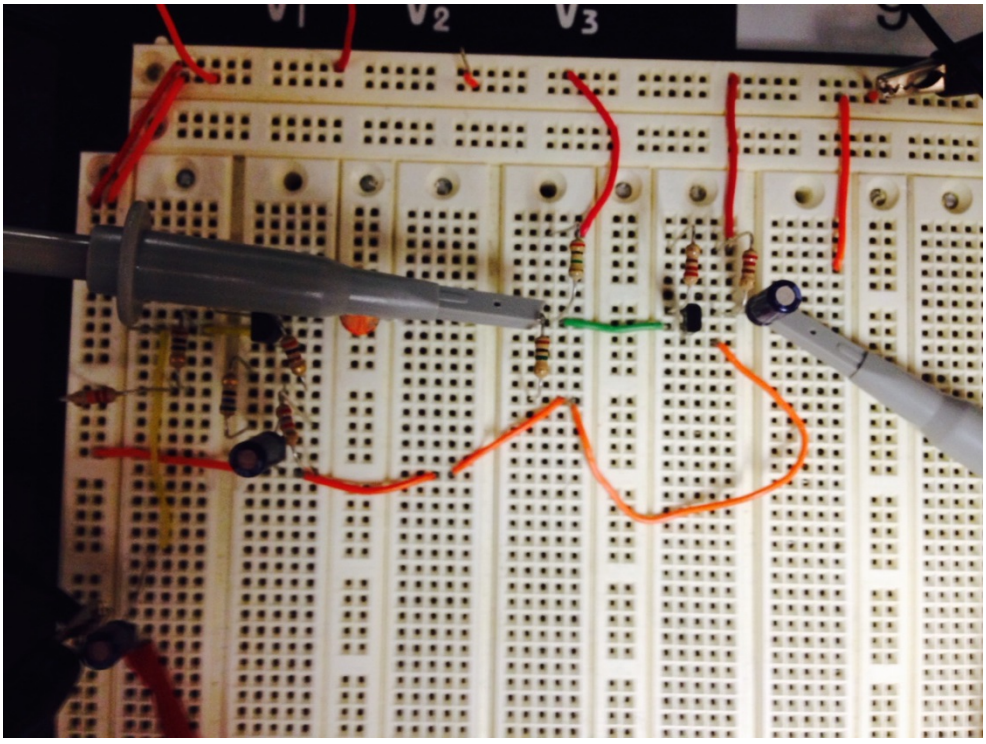

Figure 27. Second stage circuit construction and set-up showing nodes placed for measuring the second stage A_{vo} gain.

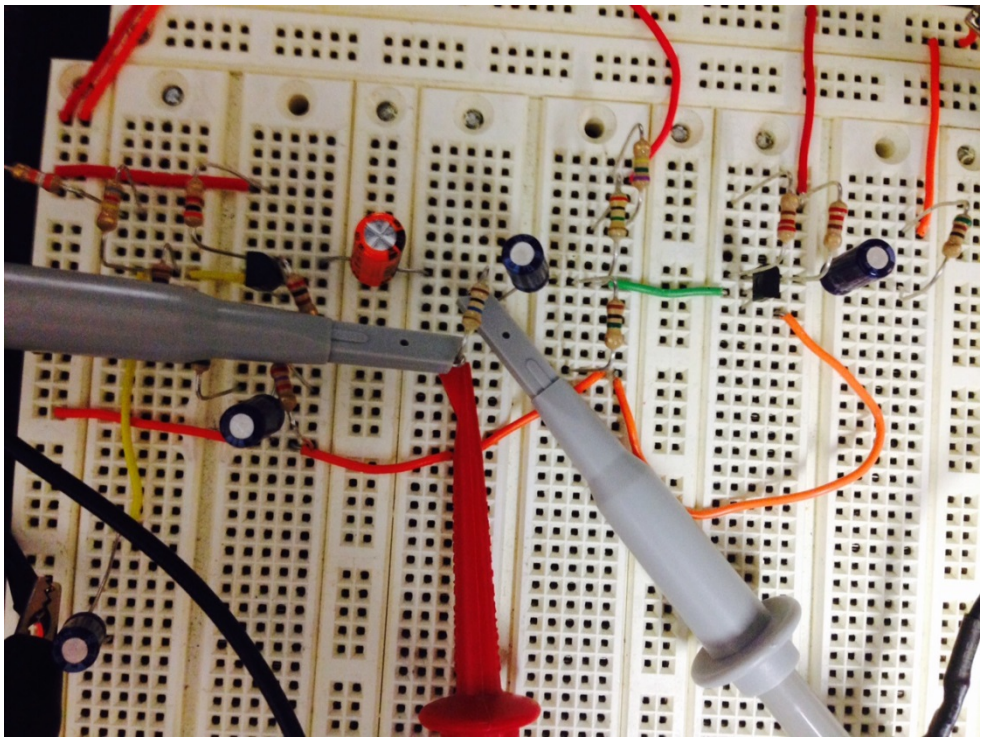

Figure 28. Oscilloscope nodes placed for the measuring of the R_{in} for the second stage of the circuit.

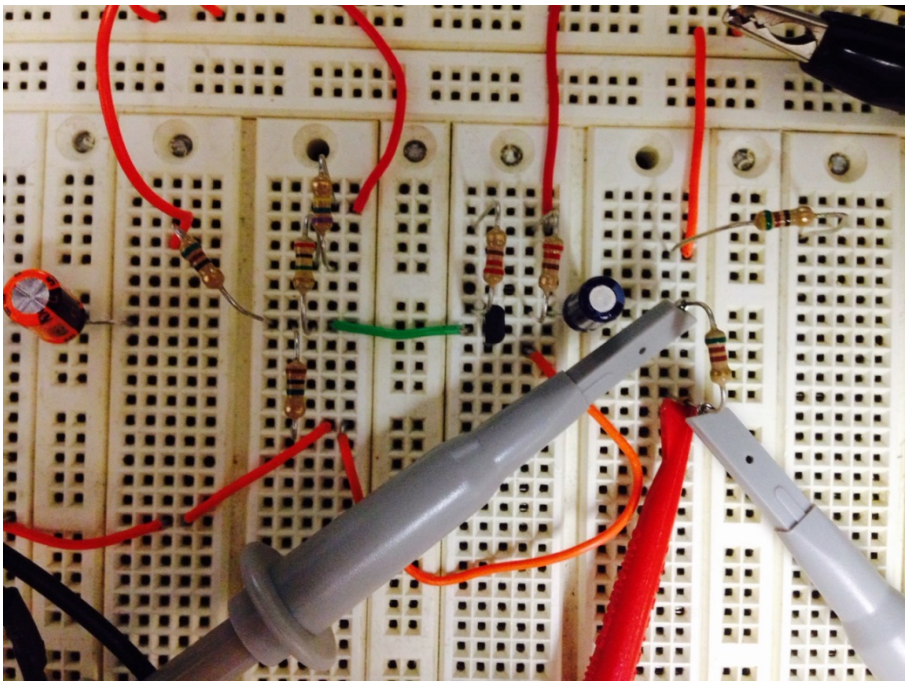

Figure 29. Oscilloscope nodes placed for the measuring of the R_{out} for the second stage of the circuit.

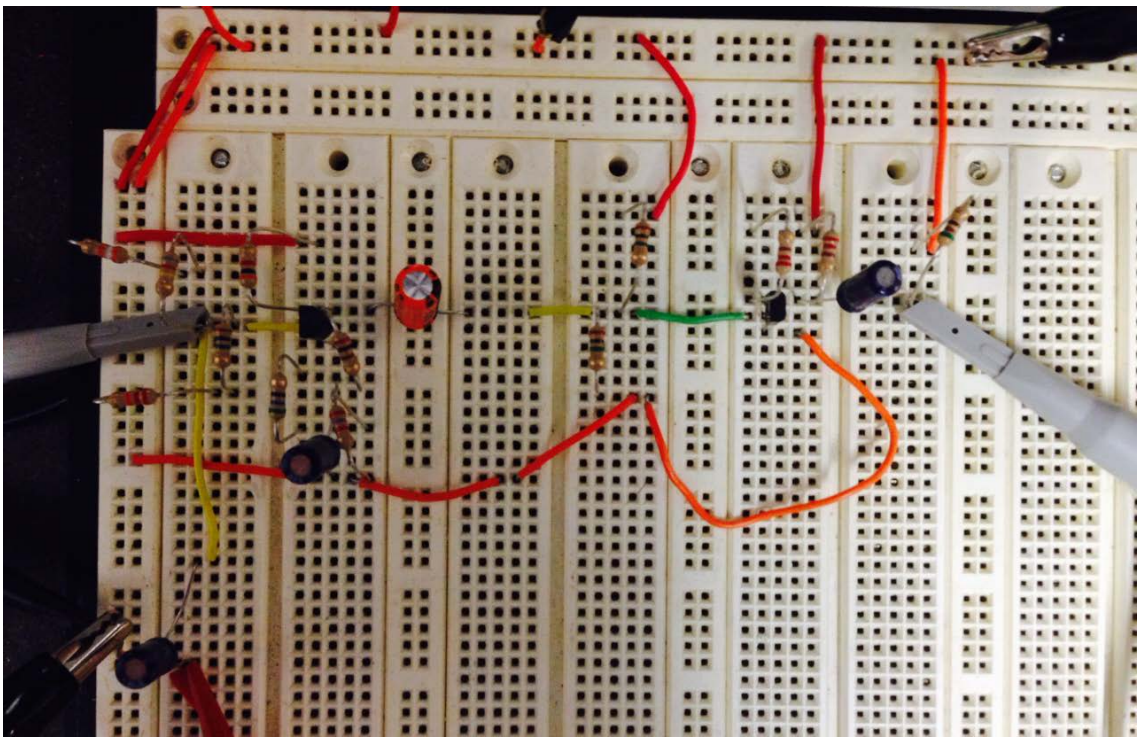

Figure 30. The complete construction of the entire circuit with the first and second stages connected and the gain being read across a 50 Ω load resistor.

Analysis and Testing

After combining the two stages of the circuit together, the construction of the total circuit is complete! Now comes the moment to analyze the results and see if the implemented circuit meets the Specifications and Limitations and how well the circuit compares to the designed and simulated circuits. We will begin with testing the first stage of the circuit, using the oscilloscope with the nodes connected to the circuit as shown in the Implementation section.

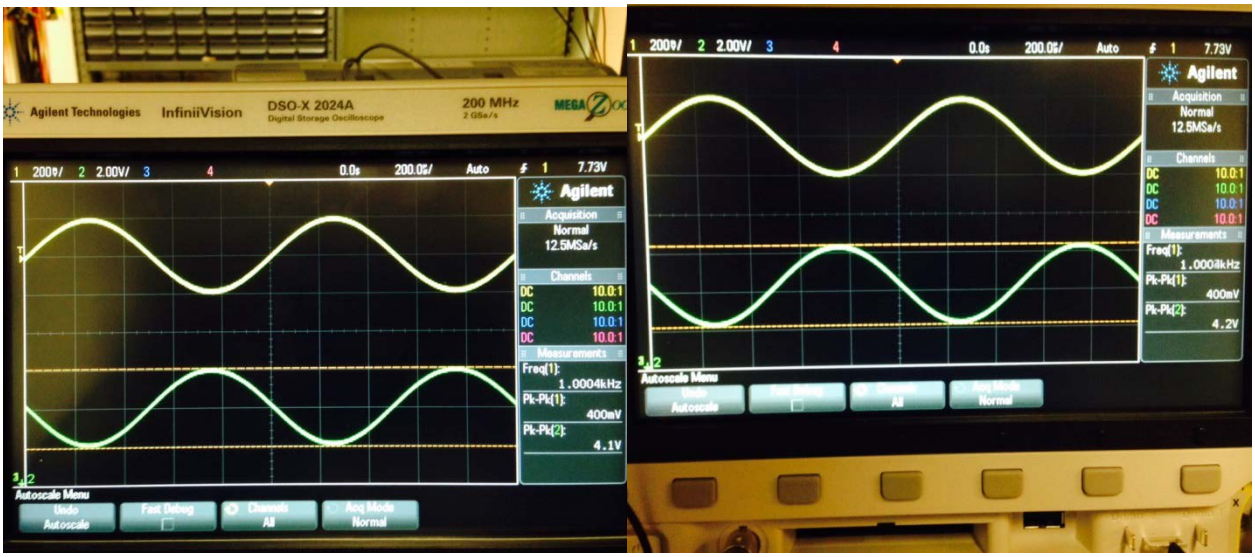

Figure 31. Oscilloscope screen shots of the measured A_v gain on the left and A_{vo} gain on the right for the first stage of the circuit.

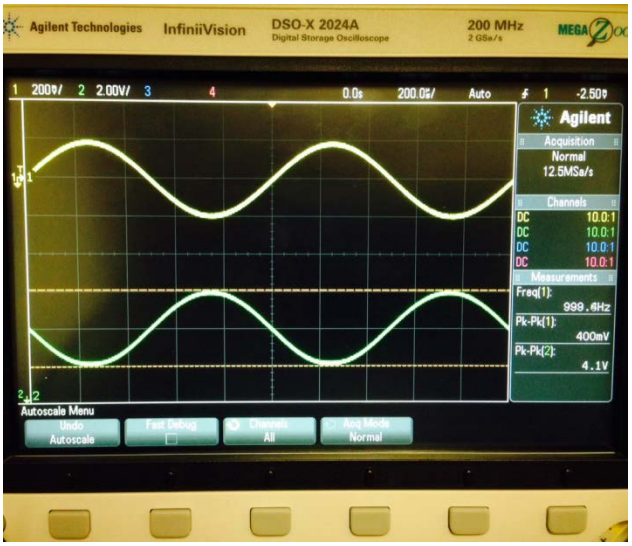

Figure 32. Oscilloscope screen shot of the measured G_v gain for the first stage of the circuit.

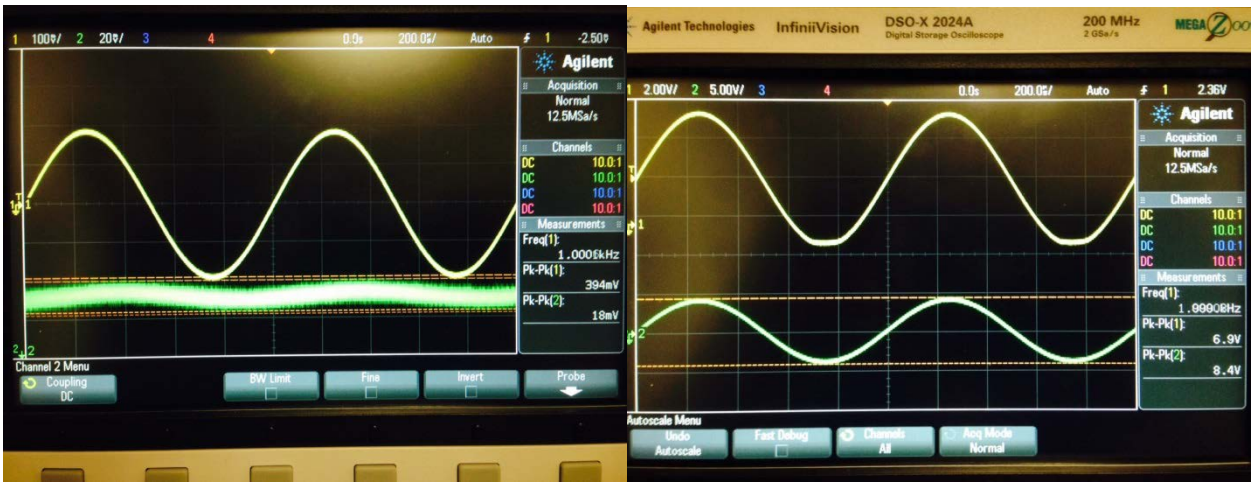

Figure 33. Oscilloscope screen shots used to measure the R_{in} and R_{out} values for the first stage circuit.

Using the values measured from the Oscilloscope and the methods described in the Approach section, the table below was completed comparing the values produced from the simulations and those measured from the constructed circuit.

Parameter	Spec & Limits	Sim	Lab	% Error
I_D (mA)	≤ 75% max transistor DC current	2.01	1.98	1.49
A_{vo} (V/V)	N/A	-10.28	-10.5	N/A
A_V (V/V)	-3 V/V ≥ A_v ≥ -30 V/V	-10	-10.25	2.5
G_V (V/V)	N/A	-10.15	-10.25	N/A
R_{in} (kΩ)	≥ 100 kΩ	458	546	19.2
R_{out} (kΩ)	≤ 5 kΩ	2.91	2.3	20.9
P_D (mW)	≤ 75% of max power any part	X	X	N/A

Table 8. Measured circuit parameters for the first stage of the circuit compared to the simulated parameters.

It is very apparent from Table 8 that the largest error in the laboratory implementation of the circuit comes from the R_{in} and R_{out} values. A percentage of these errors is due to the fact that it is impossible to implement a circuit with the exact component values that the circuit was simulated with. Additionally, another source of this error comes from the fact that the measured voltages from the Oscilloscope never settled on one value, so an estimation of the average value had to be used in order to measure the circuit R_{in} and R_{out} values.

Although the large error percentage coming from the R_{in} and R_{out} values is concerning, the first stage of the circuit meets all of the Specifications and Limitations as described. Additionally, the A_v gain is actually a little higher than what the first stage of the circuit was designed for and the output of the first stage is greater than 3 volts peak-to-peak.

Before moving on to testing and analyzing the second stage of the circuit, there are a few characteristics of the first stage of the circuit that are worth analyzing to gain a better understanding of the circuit in general.

The first of which is the coupling capacitor CS that can be seen in Figure 9. The purpose of this capacitor within the design is to add variables within the large signal circuit design that can be manipulated separately from the small signal circuit design. Because only R_{S1} and not R_{S2} is seen by the small signal circuit, R_{S1} can be manipulated to change the A_v gain, as seen by Equation 6. Without the capacitor placed in between the two source resistances, a single source resistance value would have to satisfy the large signal biasing scheme and then would set the gain that could be produced by the small signal.

Another characteristic of the circuit, which actually emphasizes the need for the second stage of the circuit, is the load resistance. The load resistance of the first stage of the circuit is 100 KΩ, which is pretty high if you are considering actually using the amplifier for day to day applications. There are not many appliances that contain a load resistance of 100 KΩ, so this parameter of the circuit is a little unrealistic. However, what happens if the load resistance is decreased to something much more realistic for a day to day appliance, such as headphones? When decreasing the load resistance for the first stage of the circuit, the gain of the circuit decreases in magnitude until it eventually drops below a gain of -1 V/V at a load resistance of 100 Ω. This characteristic of the circuit is due to a somewhat high current running through a small load resistance. Affectively, due to the current running through the load resistance, the 'Vout' node in Figure 9 does not see as high of a voltage. However, when the load resistance is increased, the current is almost completely stopped, which means that almost the full voltage is seen at the 'Vout' node.

Still another characteristic of the circuit that is worth exploring is the coupling capacitors. The coupling capacitors allow the small AC signals to be separated from the large DC signals. Without the coupling capacitors, the output voltage would simply be that of the drain voltage. The coupling capacitor allows the small signal to be used as the output voltage while unaffected by the large signal.

Finally, it is important to explore the effect on the gain from the manipulation of the drain resistors and the source resistors. If the resistor values are both doubled, the biasing voltages for the diode will be offset, causing the transistor to turn off and no gain will be produced from the circuit. Additionally, if the resistor values are halved, the transistor will allow a small signal through, but will not produce any gain.

Now we can begin to test and analyze the second stage of the circuit before combining the two stages to ensure the circuit works as expected.

Figure 34. Oscilloscope screen shots used to measure the A_v and the A_{vo} gains for the second stage of the circuit.

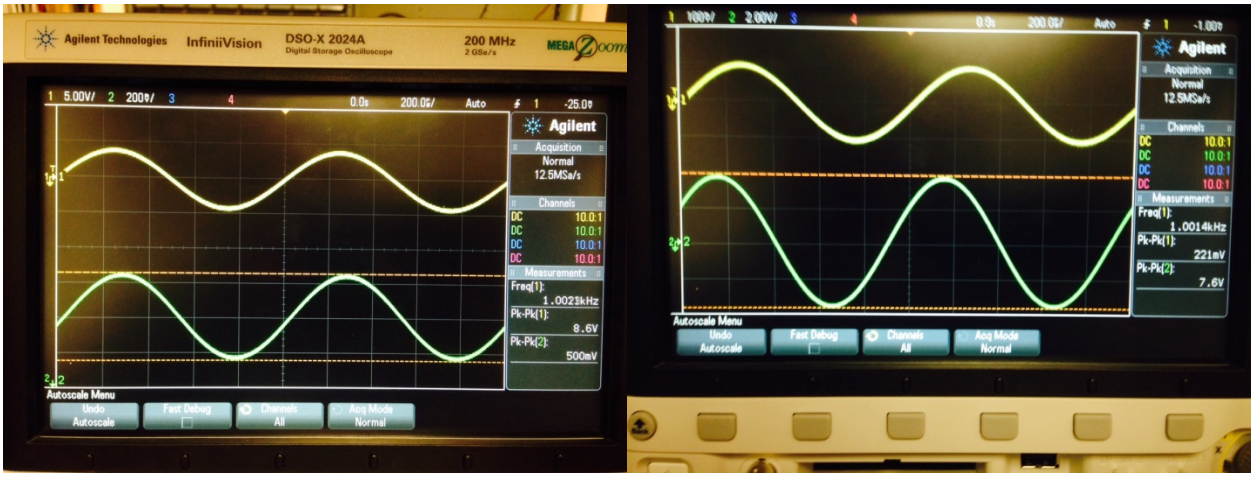

Figure 35. Oscilloscope screen shots used to measure the R_{in} and R_{out} values for the second stage of the circuit.

Parameter	Spec & Limits	Sim	Lab	% Error
I_D (mA)	≤ 75% max transistor DC current	60.3	57.3	4.98
A_{vo} (V/V)	For the CD amp only	0.96	0.88	N/A
A_V (V/V)	For the CD amp only	0.77	0.73	5.19
G_V (V/V)	For the CD amp only	0.76	0.73	N/A
R_{in} (kΩ)	≥ 100 kΩ	588	617	4.93
R_{out} (Ω)	≤ 5 kΩ	7.81	14.9	90.7
P_D (mW)	≤ 75% of max power any part	X	X	N/A

Table 9. Measured circuit parameters for the second stage of the circuit compared to the simulated parameters.

The majority of the values measured from the second stage of the circuit are very close to what they were simulated to be, however the measured R_{out} value is very far off from what it was simulated to be! This large difference is due to using an approximate g_m value for the simulated

circuit, while the actual g_m value of the transistor is somewhat different. The increased R_{out} value has caused an even further decrease in the voltage gains.

Even with the decrease in gain from the second stage of the circuit, combined with the first stage of the circuit, the resulting circuit should still meet the requirements set forth by the Specifications and Limitations.

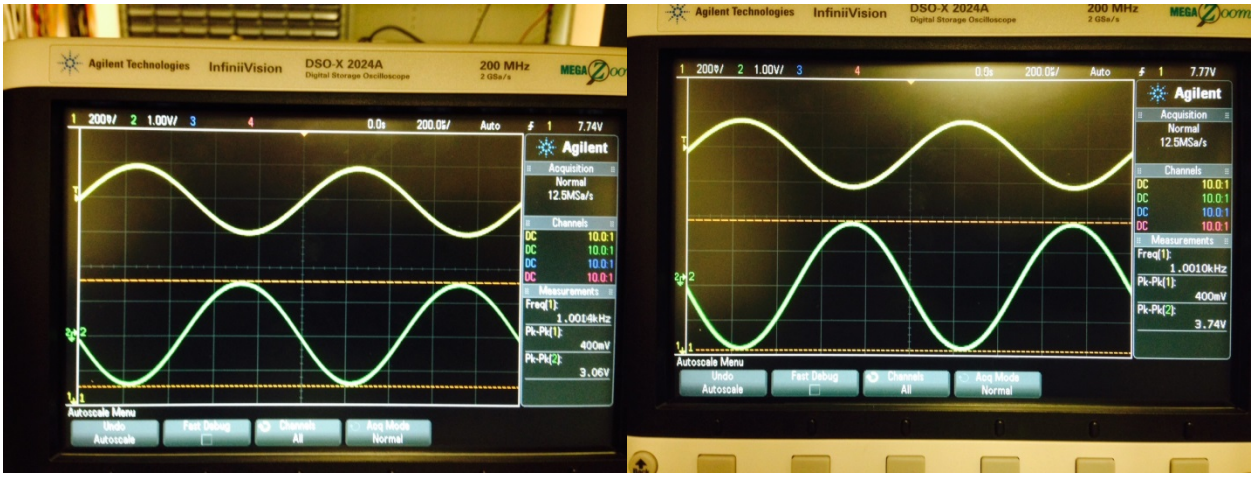

Figure 36. Oscilloscope screen shots used to measure the A_v and the A_{vo} gains for the entire circuit.

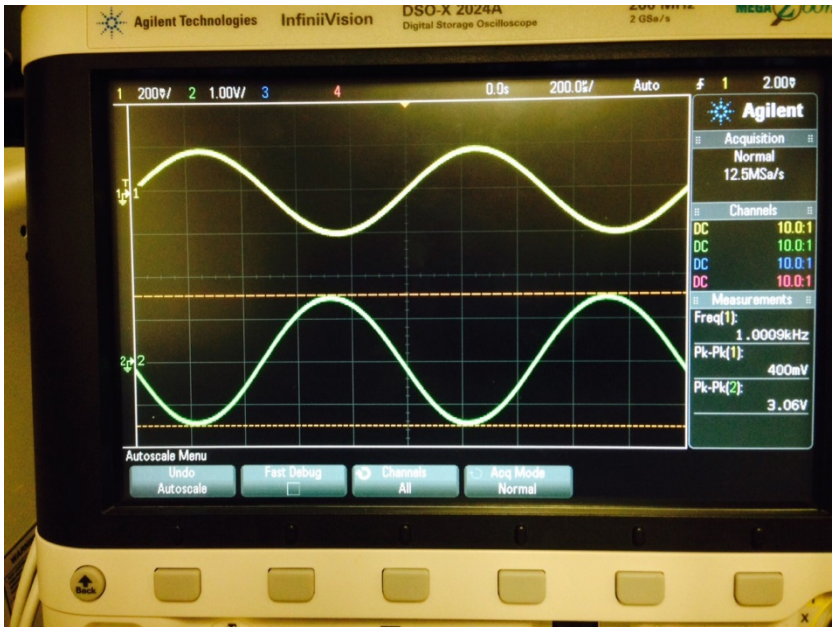

Figure 37. Oscilloscope screen shot used to measure the G_v gain for the entire circuit.

Parameter	Spec & Limits	Sim	Lab	% Error
I_D (mA)	≤ 75% max transistor DC current	60.3	57.3	4.98
I_D (mA)	≤ 75% max transistor DC current	2.01	1.98	1.49
A_{vo} (V/V)	N/A	-9.94	-9.35	N/A
A_V (V/V)	-3 V/V ≥ A_v ≥ -30 V/V	-8.07	-7.65	5.2
G_V (V/V)	N/A	-8.10	-7.65	N/A
R_{in} (kΩ)	≥ 100 kΩ	552	546	1.08
R_{out} (Ω)	≤ 5 kΩ	7.81	14.9	90.8
P_D (mW)	≤ 75% of max power any part	X	X	N/A

Table 10. Measured circuit parameters for the entirety of the circuit compared to the simulated parameters.

Parameter	Spec & Limits	Calc	Sim	Lab
I_D (mA)	≤ 75% max transistor DC current	60	60.3	57.3
I_D (mA)	≤ 75% max transistor DC current	2	2.01	1.98
A_{vo} (V/V)	N/A	-10.28	-9.94	-9.35
A_V (V/V)	-3 V/V ≥ A_v ≥ -30 V/V	-11.3	-8.07	-7.65
G_V (V/V)	N/A	-9.99	-8.10	-7.65
R_{in} (kΩ)	≥ 100 kΩ	548	552	546
R_{out} (Ω)	≤ 5 kΩ	5.77	7.81	14.9
P_D (mW)	≤ 75% of max power any part	X	X	X

Table 11. Comparison of the laboratory measured circuit parameters compared to those achieved during simulations and calculations.

Although the results from the implemented circuit vary from the results of the simulated circuit, the circuit's parameters still meet all the required Specifications and Limitations. The design calculations used many assumptions and shortcuts to provide a general direction for the design of the circuit. The simulation was useful in that it allowed us to have a good idea if the design would work before constructing the circuit on the breadboard. Simulating the circuit before constructing it saves time in the long run as it allows for easier testing to ensure that the circuit works before building it and possibly burning out circuit components.

Before wrapping up the analysis of the circuit, there are a few aspects of the circuit that should be considered in order to better understand the functioning of the circuit. The first aspect to consider is the purpose of the second stage of the circuit. What is beneficial about the amplifier that lowers the overall gain? The second stage of the circuit is a common drain pMOS FET, which in affect acts as a buffer. What this means is that produces the voltage gain across the load resistor with little to no current; meaning that the load resistance can be much lower without losing all of the gain voltage. This is important when considering the applications of amplifier circuits. Many times an amplification circuit does not connect to an interface, such as headphones or speakers, which has a 100 KΩ resistance! For this amplification circuit, I was able to get the load resistance down to 35 Ω before any before the output voltage experienced any clipping. If I were interested in achieving the correct output with this lower load resistance, I

could lower the source resistance. This technique works up to a certain point, but after a while you have to be concerned with exceeding the components power rating.

Finally, if the R_{in} of the pMOS FET circuit became lower than 100 kΩ, part of the small signal would be able to reach ground through the R_G resistors. In result, the output voltage would not be as large as it is supposed to be.

Conclusions

I can say without a doubt that my lab design did everything it was supposed to! My implemented circuit achieved an appropriate gain and produced an output voltage greater than 3 volts peak-to-peak. Additionally, all parts of the circuit had appropriate R_{in} and R_{out} values and the drain currents for each circuit was well under 75% of the max drain current rating, which was 500 mA. Finally, all components of the circuit dissipated less than 75% of its max power rating. The only adjustment that I had to make for the circuit was run two resistors in parallel for the source resistance of the second stage of the circuit. The source resistor was designed dissipate nearly 400mW while each resistor has a max power rating of 250mW. With the resistors in parallel, each resistor shares the burden and dissipates 200mW, which is well under their max power rating.

Even though the implemented circuit functioned somewhat differently from what I originally designed it to, this is nothing unexpected. I made many assumptions in the designing stage that made my design much simpler, but accounted for a slight difference in the actual result. Additionally, for the simulated circuits, I used approximate k and V_t values that were close enough to allow me to design a properly working circuit, however, the actual circuit did not function exactly how the simulation said it would.

Additionally, many of the perceived errors may have come from the lack of ability to appropriately analyze the circuit. For example, when measuring the R_{in} and R_{out} values, the wave on the Oscilloscope was very jumpy and inconsistent, meaning that the measured value was an approximate one, not the true value.

Finally, the big take away for me was realizing that the designed circuit is likely very similar to the inside of an amplifier chip. I have used amplifiers many times in the past few years, but have always taken its doings as a sort of magic, never understanding what is truly going on inside the amplifier chip. With the completion of this lab, I can now say that I have a very good idea of what is going on in the inside of an amplifier chip and I understand why the signal distorts when the circuit is biased for an unrealistically large gain.

Documentation: C2C Brett Griffith proof read my report.