USAF Academy
Department of Electrical and Computer Engineering
ECE 321 – Electronics I

The Digital Lab - Part A

Objective: To illustrate and reinforce operational and modeling concepts of the CMOS used as digital inverters, logic gates, and SR Latches.

Authorized Resources: 1) ECE 321 class handouts, 2) course texts, 3) lab and equipment manuals, and 4) simulation handouts.

Collaboration Policy: Cadets may collaborate regarding the theory relevant to this experiment and on the operation/use of software and hardware. Cadets must design and develop their own circuits and experiments, take their own data and measurements, and perform their own analysis and conclusions. Proper documentation is required per USAFA policy.

Due date: Your completed Lab Notebook for this exercise is due IAW the syllabus.

Grading: This lab is a significant component of overall lab grade for the course. See the syllabus for weightings.

Lab Notebook Format: Your final lab submission will be a "**Design Exercise**" format. However, the "Inverter Lab" will follow the "**Traditional Experiment**" format since we give you the schematic/design up front.

Part A. Inverter.

- Build an inverter circuit in the lab and repeat in simulation.
- Develop a voltage transfer curve (VTC) and propagation and delay models/simulations for the inverter.
- Use the test equipment to characterize the inverter in the lab.
- Vary the components in the circuit as instructed.
- Note how the circuit behavior changes.

Part B. Logic Gates. Reference handout on course website when available.

Part C. SR Latch. Reference handout on course website when available.

Important: Each part requires a graded pre-lab. You will turn this in at the start of each lesson for a grade. Be sure to keep a copy for your use in lab.

Part A. Inverter

Here you will simulate and build the inverter circuit shown in Figure 1**.**

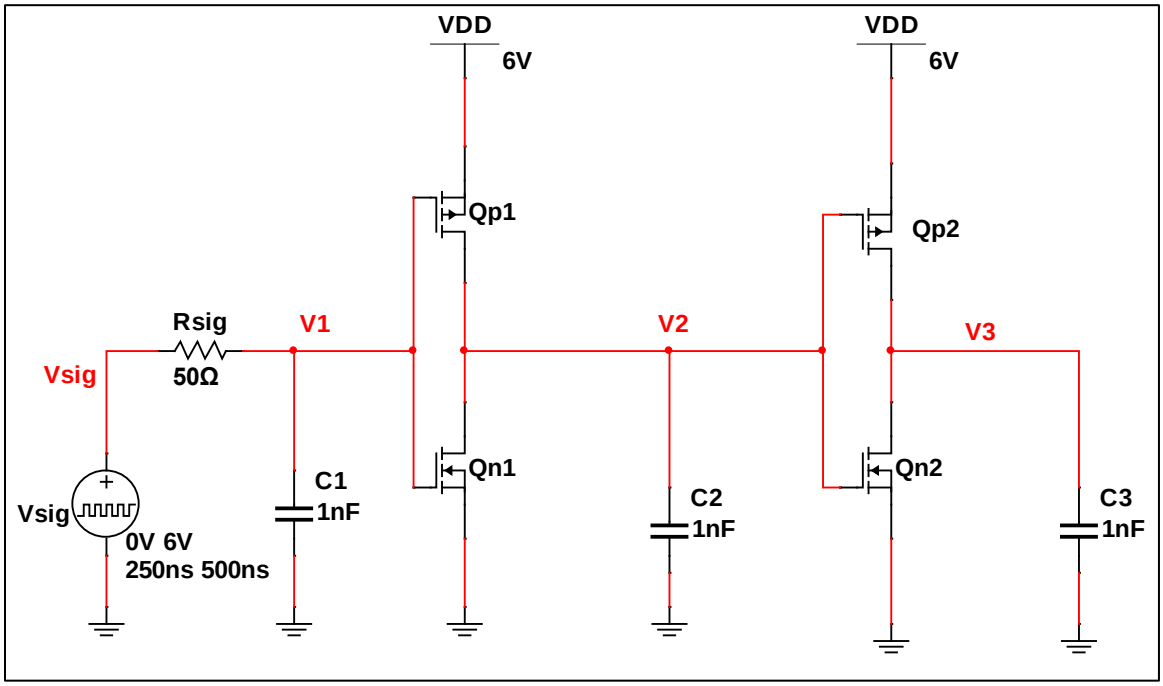

Figure 1. Inverter Circuit for Simulation and Testing

Simulation: Predict your results through simulation.

- You will need to use a PULSE_VOLTAGE to generate a square wave as the input signal. In PULSE_VOLTAGE, "Initial value" is 0 V and "Final value" is V_{DD}, "Rise time" and "Fall time" are self-explanatory, "Pulse width" is how long V_{sig} stays at V_{DD} during the "Period" (i.e. sets the duty cycle of the square wave – if "Pulse width" is ½ of "Period" then the square wave is a 50% duty cycle with time at V_{DD} equal to the time at ground), "Delay time" adds some delay/shift before the signal starts at time=0.
- Change the NMOS and PMOS model parameters to match $k'_{n,p}$, $V_{tn,p}$, and λ (KP, VTO, and LAMBDA) from your Amplifier Lab.
- To simulate the VTC you will need to use a "DC Sweep" analysis. An example is shown below in Figure 3. To complete this simulation, sweep the voltage of V_{sig} from 0 to 6 volts. A step size of 1 mV works well. "Add expression" as an output trace for "deriv(V_2)" to determine V_{IL} and V_{IH} where the slope changes to -1 V/V. For example Figure 2 shows V_{IL}=2.4 V and V_{IH}=2.8 V.
- To simulate the propagation delays and transition times you will need to use a time-domain simulation with V_2 and V_3 as the signals. MultiSim/Spice also refers to this type simulation as "Transient Analysis". An example of the propagation delay simulation is shown in Figure 3 with t_{PHL}=8.8 ns. The simulation was completed with a maximum time step of 100 ps, which is about 1 % of the measured propagation time from low to high.

Parts needed:

- 2 BS-170, nMOS transistors, 2 BS-250, pMOS transistors
- 1000 pF (1.0 nF, 0.001 µF) and 0.01 µF capacitors (non-electrolytic)

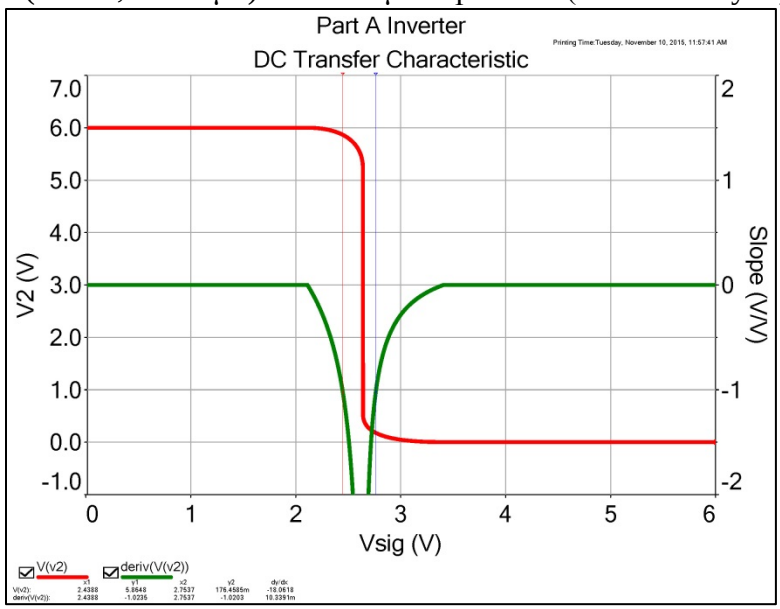

Figure 2. Voltage Transfer Curve Overlaid with Slope Trace for Determination of V_{IL} and V_{IH}, Simulation

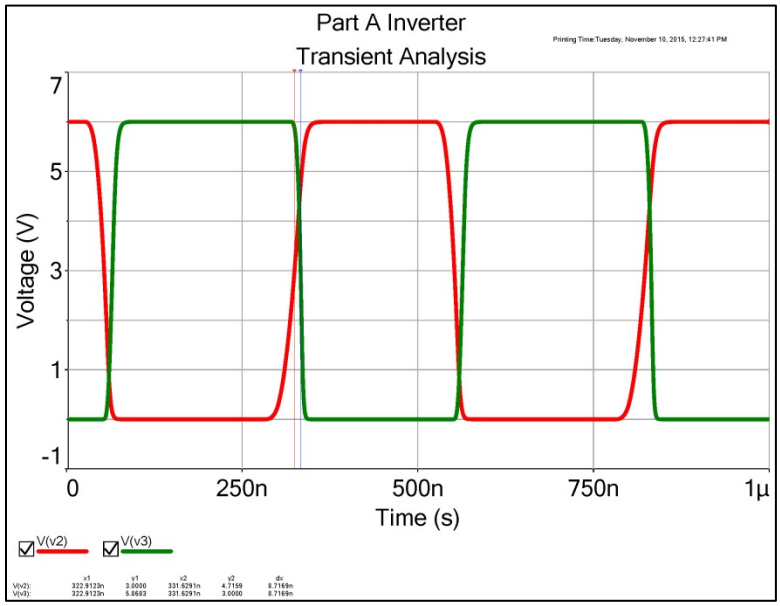

Figure 3. Propagation Delay t_{PHL}, High to Low, Simulation

Hardware: Determine the accuracy of your simulation in lab.

- Using the basic circuit shown above, build a **two-inverter** cascade with the output of one inverter driving the input of the other. **Set V_{DD} = +6 V**.

    - **Note:** Use cables with banana plugs at both ends to connect the power supply to the connectors at the top of the proto-board. From the banana plugs run wires for V_{DD} and ground to the horizontal runs at the top of the board area. Then, connect the long vertical runs to the horizontal runs at the top. Connect your circuit to the vertical runs.
- Connect the function generator to the first inverter's input.
- Verify, on the scope, you have the proper input signal, a 0 to 6 V square wave.
- Verify you are getting appropriate output data, inverted at the output of the first inverter and inverted twice (back to the same phase as the input) at the output of the second inverter.
- **Using the first inverter only**, measure as many of the values listed below as you can, and sketch and label a voltage transfer curve (VTC). You should get a result like Figure 14.25 on p. 1118 in *Sedra & Smith*. To get this result use either a sinusoid or triangle wave (do not use the square wave, as the input signal will not spend enough time in the transition to get a usable VTC) from 0 to 6 V, while setting the oscilloscope to "XY" mode.
    - If you have a large variation between traces as the load is charging and discharging (hysteresis), slow down the frequency of your function generator – give the inverter a slower signal so spends enough time in the transition region.
    - If you are not familiar with this mode, reference the manual for the Agilent 2000x oscilloscope on the course website.
    - Values to measure with oscilloscope cursors: (use the function generator as V_{in} and V_{C2} (across capacitor C_2) as V_{out})
        - V_{OH} and V_{OL}
        - V_{IH} and V_{IL}
        - V_M
- **Using the input and output of the second inverter only** (V_{in} is the output of the 1st inverter & V_{out} is the V_{C3} - across C_3)
    - Values to measure with O-scope cursors
        - t_{PLH}, t_{PHL}, and t_P
        - t_{THL} and t_{TLH}
- Estimate power dissipation. Hint: you need to know the frequency of the signal.
- Vary the capacitor load sizes. How does this affect things?
    - Only change C_2 and C_3. Keep C_1 at 1 nF
- Vary the frequency. Go really low…like 10 Hz or lower.
    - Watch the current meter on the power supply.

The following questions should be answered in your Notebook. Your Notebook will, however, also include additional appropriate sections and analysis.

Question #1 – What is the approximate maximum useable frequency when the load capacitance is 0.01 μF? Explain. Hint: you know the k_n, k_p, V_{tn} and V_{tp} values from the last lab.

Question #2 – What happens if you are not careful and try to create an X-Y plot using a sinusoidal +6 V and -6 V signal instead of +6 V to 0 V? What does the plot look like, and why?

Question #3 – Set up a square wave +6 V and 0 V and at about 2 kHz. Place a probe on ground or V_{DD} close to the circuit. Set the resolution to the smallest scale. Zoom in to V_{DD} or ground at the instant the transition occurs. Explain what is occurring.

Question #4 – Keeping the same connections as above, place a large capacitor between V_{DD} and ground. Use at least 1000 μF (remember electrolytic polarity matters). What differences do you observe from the conditions in Question #3? What implications does this observation have for large digital circuit design?