USAF Academy
Department of Electrical and Computer Engineering
ECE 321 – Electronics 1

Fall 2017

The Amplifier – Pre-lab

(Each Part due at beginning of class IAW syllabus. Make a copy for yourself.)

While you will build and test circuits in groups of two cadets, the pre-lab 1 and 3 are individual effort. It is recommended that you each keep a notebook which includes a copy of the pre-lab upon which you base the circuit you build and test.

Part A Pre-lab. Single Stage Amplifier

(25 pts) Theory

1. Describe the physics behind the p-type MOS-Capacitor using energy band diagrams and how this relates to threshold voltage for an nMOS transistor.

2. Using the "common source (CS) amplifier with source resistance" as shown in Figure 1 of the lab handout,
    a. Write down the governing equations for V_G, V_S, V_D and I_D. Assume $\lambda=0$. Draw the large signal model circuit.
    b. Write down the governing equations for g_m, A_V, A_{VO}, G_V, R_{in} and R_{out}. Assume $\lambda=0$. Draw the small signal model circuit (i.e. the hybrid-π or T-model).

(25 pts) Design

Through hand calculations using the governing equations, design your "CS amplifier with source resistance" to meet the "Specifications and Limitations" given in the lab handout. Since you have not characterized your transistor, yet use $k_n = 250\ \text{mA/V}^2$, $V_t = 2.0$ V, and $\lambda=0$. Also assume $R_{sig}=50\ \Omega$.

(25 pts) Simulation

Attach your simulation (circuit schematic and graph) and fill in the table below showing your simulated values for the "Specifications and Limitations". Note: A_{vo} and G_v are not specified, but you can easily simulate these.

Parameter	Spec & Limits	Calcs	Sim	% Error
I_D (mA)	≤ 75% max transistor DC current			
A_{vo} (V/V)	N/A	**N/A**		N/A
A_v (V/V)	-3 V/V ≥ A_V ≥ -30 V/V			

G_v (V/V)	N/A	**N/A**		N/A
R_{in} (kΩ)	≥ 100 kΩ			
R_{out} (kΩ)	≤ 5 kΩ			
P_D (mW)	≤ 75% of max power any part			

(25 pts) Procedure/Test Plan

Describe how will you measure, collect and analyze data. Describe the test equipment you will use. Draw a schematic showing how your test equipment is connected to your circuit.

Pre-lab B. Demonstration of Part A in lab

By the end of day 2 demonstrate the following.

(25 pts) Circuit build

Demonstrate you that you built your circuit on the protoboard with power supply and function generator appropriately connected.

(25 pts) Test Equipment setup

Demonstrate you appropriately connected your test equipment (o-scope, DMM, etc.) to perform the required measurements.

(25 pts) Demonstration

Demonstrate on the oscilloscope your input signal and amplified output signal.

(25 pts) Specs and Limitations

Fill in the table below indicating how well you did or did not meet specs and limits.

Parameter	Spec & Limits	Sim	Lab	% Error
I_D (mA)	$\leq$ 75% max transistor DC current			
A_{vo} (V/V)	N/A			
A_v (V/V)	-3 V/V $\geq A_V \geq$ -30 V/V			
G_v (V/V)	N/A			
R_{in} (kΩ)	$\geq$ 100 kΩ			
R_{out} (kΩ)	$\leq$ 5 kΩ			
P_D (mW)	$\leq$ 75% of max power any part			

Part C Pre-lab. Cascaded Amplifiers

(25 pts) Theory

1. Describe the physics behind the n-type MOS-Capacitor using energy band diagrams and how this relates to threshold voltage for a pMOS transistor.

2. Using only the "common drain (CD)" amplifier as shown in the 2nd stage of Figure 2 of the lab handout,
    a. Write down the governing equations for V_G, V_S, V_D and I_D. Assume $\lambda=0$. Draw the large signal model circuit.
    b. Write down the governing equations for g_m, A_V, A_{VO}, G_V, R_{in} and R_{out}. Assume $\lambda=0$. Draw the small signal model circuit (i.e. the hybrid-π or T-model).

(25 pts) Design

Through hand calculations using the governing equations, design your "common drain (CD)" amplifier to meet the "Specifications and Limitations" given in the lab handout. Since you have not characterized your transistor, yet use $k_p = 250\ \text{mA/V}^2$, $V_t = -2.0\ V$, and $\lambda=0$. Assume R_{out} from your CS amplifier (1st stage) is the effective R_{sig} value for the second, CD, stage.

(25 pts) Simulation

Attach your simulation (circuit schematic and graph) and fill in the table below showing your simulated values for the "Specifications and Limitations". Note: A_{vo} and G_v are not specified, but you can easily simulate these.

Parameter	Spec & Limits	Calcs	Sim	% Error
I_D (mA)	≤ 75% max transistor DC current			
A_{vo} (V/V)	For the CD amplifier only	**N/A**		**N/A**
A_v (V/V)	For the CD amplifier only			
G_v (V/V)	For the CD amplifier only	**N/A**		N/A
R_{in} (kΩ)	≥ 100 kΩ			
R_{out} (kΩ)	≤ 5 kΩ			
P_D (mW)	≤ 75% of max power any part			

(25 pts) Procedure/Test Plan

Describe how will you measure, collect and analyze data. Describe the test equipment you will use. Draw a schematic showing how your test equipment is connected to your circuit.