These figures belong to Problem 16.3.

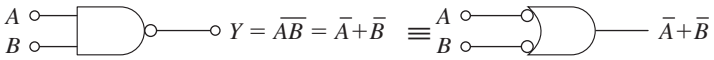


Figure 1

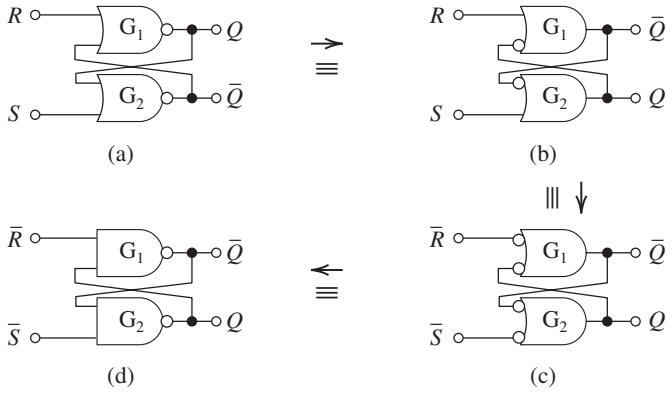


Figure 2

16.3 Figure 1 shows the equivalence of a NAND gate to an OR gate with inverters at the inputs. We can use this equivalence to derive an SR flip-flop utilizing two cross-coupled NAND gates starting from the one utilizing NOR gates in Fig. 15.3, as shown in Fig. 2.

The resulting circuit, shown in Fig. 2(d), can be described by the following truth table:

$\overline{R}$	$\overline{S}$	Q_{n+1}
0	0	not used
0	1	0
1	0	1
1	1	Q_n

Here, the rest state is when both trigger inputs $\overline{R}$ and $\overline{S}$ are high. To set the flip-flop we lower $\overline{S}$ to zero. This results in $Q_{n+1} = 1$. Conversely, to reset the flip-flop, $\overline{R}$ is lowered to zero, resulting in $Q_{n+1} = 0$. The situation with both $\overline{R}$ and $\overline{S}$ lowered to zero results in an undefined output and is thus avoided.

16.4 Following the procedure used in Example 16.1 and referring to Fig. 16.5(b), we can write

$$I_{D\text{eq}} = I_{D2}$$

$$k'_n \times \frac{1}{2}\left(\frac{W}{L}\right)_{5,6}\left[(V_{DD} - V_{tn})\left(\frac{V_{DD}}{2}\right) - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right] = k'_p\left(\frac{W}{L}\right)_p\left[(V_{DD} - |V_{tp}|)\left(\frac{V_{DD}}{2}\right) - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

Since $V_{tn} = |V_{tp}|$, this equation reduces to

$$\frac{1}{2}k'_n\left(\frac{W}{L}\right)_{5,6} = k'_p\left(\frac{W}{L}\right)_p \tag{1}$$

Since the inverter is matched, then

$$k'_p\left(\frac{W}{L}\right)_p = k'_n\left(\frac{W}{L}\right)_n \tag{2}$$

Substituting for $k'_p(W/L)_p$ from Eq. (2) into Eq. (1) gives

$$\left(\frac{W}{L}\right)_{5,6} = 2\left(\frac{W}{L}\right)_n \qquad \text{Q.E.D.}$$

Refer to Fig. 16.4. For Q_1 and Q_3,

$$\left(\frac{W}{L}\right)_{1,3} = \frac{0.13\ \mu\text{m}}{0.13\ \mu\text{m}}$$

$$\left(\frac{W}{L}\right)_{2,4} = \frac{0.52\ \mu\text{m}}{0.13\ \mu\text{m}}$$

$$\left(\frac{W}{L}\right)_{5-8} = \frac{0.26\ \mu\text{m}}{0.13\ \mu\text{m}}$$

16.5 From Table 14.2 on P. 1155 of the text we obtain for the inverter threshold voltage

$$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{1 + r}$$

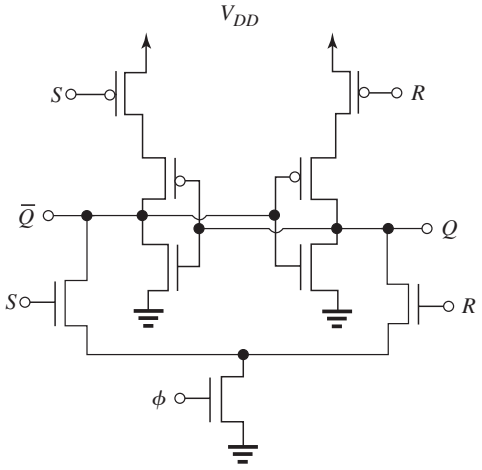
where

$$r = \sqrt{\frac{k'_p(W/L)_p}{k'_n(W/L)_n}}$$

For our case, we have

$$k'_n = 4k'_p = 300\ \mu\text{A/V}^2$$

$$\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n = \frac{0.27\ \mu\text{m}}{0.18\ \mu\text{m}}$$



This circuit suffers only from the fact that unclocked changes in S and R have a secondary input on $Q/\overline{Q}$ since raising S or R disconnects $Q/\overline{Q}$ from V_{DD}. In some applications this may lead to system noise sensitivity in which case one or the other or both of Q_{10}, Q_{12} (in the previous sketch) may be added.

16.9

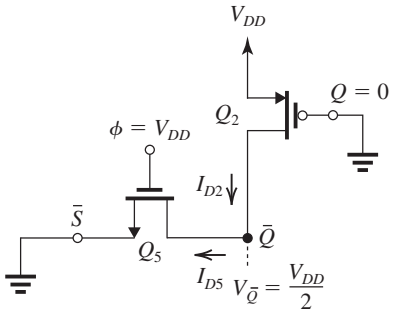


Figure 1

Figure 1 shows the relevant part of the circuit at the point of switching ($V_{\overline{Q}} = V_{DD}/2$). For this situation to be achieved, the current supplied by Q_5, I_{D5}, must at least be equal to that supplied by Q_2. Since both transistors are operating in the triode region, we can write

$$I_{D5} = I_{D2}$$

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_5\left[(V_{DD} - V_{tn})\left(\frac{V_{DD}}{2}\right) - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

$$=$$

$$\mu_p C_{ox}\left(\frac{W}{L}\right)_p\left[(V_{DD} - |V_{tp}|)\left(\frac{V_{DD}}{2}\right) - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

Since $V_{tn} = |V_{tp}|$, this equation yields

$$\left(\frac{W}{L}\right)_5 = \left(\frac{\mu_p}{\mu_n}\right)\left(\frac{W}{L}\right)_p$$

This is the minimum required value of $(W/L)_5$.

16.10 Refer to Fig. P16.10.

(a) When ϕ is high, the transmission gate is conducting (i.e., Q_5 and Q_6 are conducting) and the line D is connected to the input terminal of G_2. Thus $\overline{Q} = \overline{D}$ and $Q = D$. The two feedback loops around G_2 are open because although Q_1 or Q_4 can conduct (if $D = 1$ and thus $\overline{Q} = 0$, Q_1 can conduct while if $D = 0$ and thus $\overline{Q} = 1$, Q_4 can conduct) their conduction paths are blocked by Q_2 and Q_3 which remain cut off when ϕ is high.

(b) If D is high, then $\overline{Q}$ is low and Q is high. Now, if ϕ goes low, the transmission gate turns off, thus the input of G_2 is isolated from D. The high value at the gate of G_2 is maintained by the feedback loop around G_2 consisting of Q_1 and Q_2, both of which conduct, thus connecting the input node of G_2 to V_{DD}. Meanwhile, Q_3 and Q_4 are at cut off.

(c) If D is low, then the voltage at the input of G_2 will be low (0 V) and thus $\overline{Q}$ will be high and Q will be low. When ϕ goes low, the transmission gate turns off and the input node of G_2 is isolated from D. The low voltage at the input node of G_2 is maintained by the feedback loop around G_2 consisting of Q_3 and Q_4, both of which conduct. Meanwhile, Q_1 and Q_2 are cutoff.

(d) No. The circuit connects either V_{DD} or ground directly to the input of G_2 which establishes the value of Q and $\overline{Q}$. When ϕ goes low, a feedback loop closes around G_2, thus locking in the value of $\overline{Q}$ (equal to $\overline{D}$) and thus Q (equal to D).

16.11 A 4-Gbit RAM has 4G cells,

$= 4 \times 1024^3$

$= 4{,}294{,}967{,}296$ cells

16.12 The word address needs M bits where

$2^M = 256\text{M} = 256 \times 1024^2$

$M \log_2 2 = \log_2 256 + 2 \log_2 1024$

$\Rightarrow M = 8 + 2 \times 10 = 28$

16.13 The 1-Mbit square memory array has 1024 word lines and 1024 bit lines. Thus it requires 10 bits to address each of the 1024 words. If the 1024 bit lines are read in groups of 16 bits; there will be $1024/16 = 64$ groups, requiring 6 bits to address each group. Thus the total number of address bits needed is $10 + 6 = 16$. This should be compared to the 20 address bits needed if each of the 1 Mbits is to be individually read.

16.21

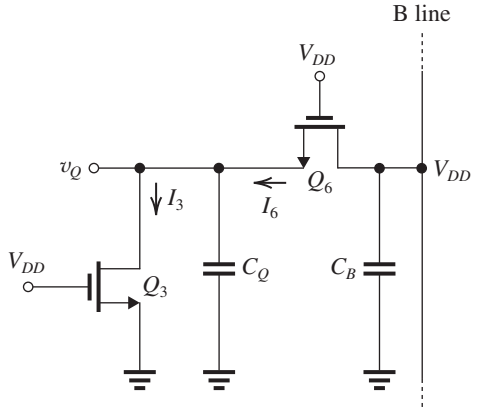


Figure 1

The relevant part of the circuit is shown in Fig. 1. It is assumed that $Q = 0$, that is, initially $v_Q = 0$ V. Also it is assumed that the B line voltage is V_{DD}. When the word line is selected and the gate of Q_6 is pulled to V_{DD} volts, Q_6 conducts and operates in the saturation region. Its current I_6 charges C_Q whose voltage v_Q rises from 0 V and thus Q_3 conducts and operates in the triode region. Current I_6, in addition to charging C_Q, also supplies a current equal to I_3. Equilibrium is reached at the value of V_Q that makes I_3 equal to I_6 and thus C_Q stops charging. The design is based on V_Q being sufficiently small to prevent the latch from changing state (nondestructive readout). Usually, one imposes the condition that $V_Q \leq V_{tn}$.

The operation of the circuit is described by equations identical to (16.1)–(16.4) except for $(W/L)_5$ replaced with $(W/L)_6$ and $(W/L)_1$ replaced with $(W/L)_3$. The graph in Fig. 16.14 applies here also with the same changes mentioned. Finally, Eq. (16.5) provides the constraint on the (W/L) ratios that results if V_Q is to be less or equal to V_{tn}.

16.22 Refer to Fig. 16.13. Since $V_{\overline{Q}} \leq V_t$, and $V_t = 0.5$ V $< V_{DSsat}$ which is 0.6 V, transistor Q_1 will be operating in the triode region and thus Eq. (16.2) still applies. Transistor Q_5, however, has $v_{GS} = v_{DS} = V_{DD} - v_{\overline{Q}}$ which ranges in value from 1.8 V to 1.3 V (as $v_{\overline{Q}}$ rises from 0 to 0.5 V). Thus, $v_{GS} \geq V_{DSsat}$ and $v_{DS} \geq V_{DSsat}$. Current I_5 will therefore be given by Eq. (15.11), namely,

$$I_{D5} = \mu_n C_{ox}\left(\frac{W}{L}\right)_5 V_{DSsat}\left(v_{GS} - V_t - \frac{1}{2}V_{DSsat}\right)$$

where we have neglected λ. Substituting

$$v_{GS} = V_{DD} - V_{\overline{Q}}$$

we obtain

$$I_{D5} = \mu_n C_{ox}\left(\frac{W}{L}\right)_5 V_{DSsat}\left(V_{DD} - V_{\overline{Q}} - V_t - \frac{1}{2}V_{DSsat}\right)$$

Equating I_{D5} to I_{D1} in Eq. (16.2), we obtain

$$\left(\frac{W}{L}\right)_5 V_{DSsat}\left(V_{DD} - V_{\overline{Q}} - V_t - \frac{1}{2}V_{DSsat}\right)$$

$$= \left(\frac{W}{L}\right)_1\left[(V_{DD} - V_t)V_{\overline{Q}} - \frac{1}{2}V_{\overline{Q}}^2\right]$$

Substituting $V_{DD} = 1.8$ V, $V_{\overline{Q}} = V_t = 0.5$ V, $V_{DSsat} = 0.6$ gives

$$\left(\frac{W}{L}\right)_5 \times 0.6 \times \left(1.8 - 0.5 - 0.5 - \frac{1}{2}\times 0.6\right)$$

$$= \left(\frac{W}{L}\right)_1\left[(1.8 - 0.5)0.5 - \frac{1}{2}(0.5)^2\right]$$

$$\Rightarrow \frac{(W/L)_5}{(W/L)_1} = 1.75$$

That is,

$$\frac{(W/L)_5}{(W/L)_1} \leq 1.75$$

In the absence of velocity saturation, we can find the maximum allowable value of this ratio using Eq. (16.5) as

$$\frac{(W/L)_5}{(W/L)_1} \leq 1.64$$

Thus, for a given $(W/L)_1$, velocity saturation allows a larger $(W/L)_5$, which is a result of the reduced current in the velocity-saturation region.

16.23 Without taking the body effect into account, Eq. (16.5) applies with $V_{tn} = V_{t0}$, thus

$$\frac{(W/L)_a}{(W/L)_n} \leq \frac{1}{\left(1 - \dfrac{0.4}{1.2 - 0.4}\right)^2} - 1$$

$$\Rightarrow \frac{(W/L)_a}{(W/L)_n} \leq 3$$

The body effect will affect the operation of Q_5 whose V_{tn} now will be given by

$$V_{tn} = V_{t0} + \gamma\left(\sqrt{V_{SB} + 2\phi_f} - \sqrt{2\phi_f}\right) \qquad (1)$$

In equilibrium

$$V_{\overline{Q}} = V_{tn}$$

thus

$$V_{SB} = V_{tn}$$

Equation (1) then becomes

$$V_{tn} = V_{t0} + \gamma\left(\sqrt{V_{tn} + 2\phi_f} - \sqrt{2\phi_f}\right)$$

Thus,

$$V_{tn} = 0.4 + 0.2\left(\sqrt{V_{tn} + 0.88} - \sqrt{0.88}\right)$$