**MIPS Exercise Name:\_\_Mark Demore II\_\_\_\_\_\_\_\_\_**

Given this assembly program

        addi    $a0, $0, 9      #a0 = number of values in array - 1

        la      $a1, array      #a1 = address (or pointer) to top of array

        lw      $a2, 0($a1)     #a2 = initial value

loop:   addiu   $a1, $a1, 4

        lw      $a3, 0($a1)

        add     $a2,$a3,$a2

        subiu   $a0, $a0, 1

        bne     $a0, $0, loop

\*done:  beq     $0,$0,done    #breakpoint at end

#   initialize data in the array

array:  .word 0x5, 0x4, 0x10, 0x3, 0x12, 0x1, 0x7, 0x4, 0x8, 0x2

1. How many total assembly instructions are executed by this program until it hits the breakpoint?

**49**

1. For the Single Cycle unpipelined RISC processor, every instruction executes in the same amount of time (during one long clock period).  If each instruction executes in 50 nsec, how long does it take the program to run?

**49 \* 50nsec = 2.45μs**

1. Now you will analyze this program’s execution on the H&P 5 stage RISC V pipeline using the attached spreadsheet file mips\_template.xlsx (tab “**with stalls and no forwarding**”). Assume this 5 stage pipeline has no support for forwarding but has hardware interlocks to stall when necessary, and branching delays similar to figure C.18 in your textbook. Add all the instructions executed by this program, and put the 5 stages (IF ID EX M WB) for each instruction with the proper stall cycles inserted to prevent any hazards from occurring.
2. How many total cycles did it take for this program to run?

**164**

1. If each cycle takes 11 ns, how long does it take the program to run?

**164 x 11ns = 1.804μs**

1. What is the speedup of this 5 cycle pipelined RISC V processor without forwarding versus the original single cycle RISC processor?

**2.45μs / 1.804μs = 1.358**

1. What is the average cycles per instruction (CPI) for this 5 cycle pipelined RISC V processor without forwarding?

**164 / 49 = 3.347**

1. Now you will analyze this program’s execution on the H&P 5 stage RISC V pipeline using the attached spreadsheet file mips\_template.xlsx (tab “**with forwarding & branch fix**”). Assume this 5 stage pipeline now has support for forwarding, but also has hardware interlocks to stall if necessary, and has improved branching, similar to figure C.25 in your textbook. Add all the instructions executed by this program, and put the 5 stages (IF ID EX M WB) for each instruction assuming forwarding, and add the proper stall cycles inserted to prevent any hazards from occurring if needed. Do not **reorder** any of the instructions.
2. How many total cycles did it take for this program to run?

**80**

1. If each cycle takes 11 ns, how long does it take the program to run?

**80 x 11ns = 0.88μs**

1. What is the speedup of this 5 cycle pipelined RISC V processor with forwarding versus the original single cycle RISC processor?

**2.45μs / 0.88μs = 2.784**

1. What is the average cycles per instruction (CPI) for this 5 cycle pipelined RISC V processor with forwarding?

**80 / 49 = 1.633**