CPE 301 Embedded Systems Design Lab Fall 2018

LAB #10 Week of December 3

Objective:

To become familiar with Verilog and the Altera Quartus-II FPGA compiler.

Procedure:

1. Read the "DE1_User_Manual.pdf" **before coming to Lab**. Specifically, read Chapters 1 and 2. Then, Read Sections 4.1, 4.2 and 4.3 carefully.

2. Follow the instructions in the "Altera_FPGA_Tutorial.pdf" and then implement and test the two-input logic gates.

3. Modify your code from #2 above and implement and test the following circuit. Build a 2 to 4 decoder circuit, with one enable input, (as shown below) and use the four outputs from the decoder to drive a seven segment display with the appropriate numbers from the decoder (0 through 4). Where not enabled = 0, y[0] = 1, y[1] = 2, y[2] = 3, and y[3] = 4.
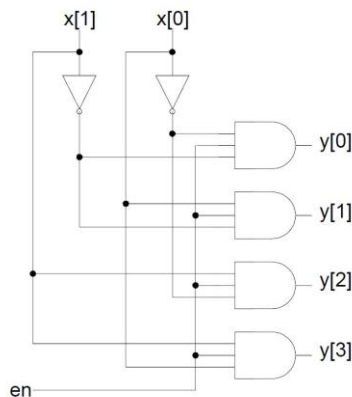
In addition to the standard lab report, include in your lab report's description:

1. Modified source code.
2. Truth table and Boolean equations for each LED segment.
3. Table reflecting the pin assignments from the source code variables to the LED segment identifiers.