Alexis Diaz
CPE 301-1001
Lab 02
September 22, 2017

Assignment Description:

In this lab, the objective was to utilize a decoder, an octal D-latch, and a shift register on a breadboard. We did this by reading a truth table of the decoder, and observing what the enable does. We also observed the activity of the shift register using a button to act as the clock cycle.

Problems Encountered:

This lab went smoothly except for some circuit troubleshooting. After repeatedly checking that the wiring was correct, I figured my decoder chip must be defective, but upon extracting the IC, I noticed what the issue was all along: The VCC pin on my 74LS138 was bent and was not inserted into the breadboard. I also did not know how to wire the resisters to be used effectively, but after help from the TA, I was able to do it. I did not have any issues besides this.

Lessons Learned:

In this lab, I learned that the LE (latch enable) is what allows the decoder IC to perform its functions, otherwise it will not perform its actions. I also learned that a shift register shifts a bit to the right every time the clock cycle happens, if the CLR is active low.

Description of Completed Lab:

Procedure:

1. First, I connected a wire to the 5V port on the power supply, then I assembled the circuit that was seen in the pdf file “Lab02-Fig1” (Figure 1). This part of the lab featured DIP Switches, 74LS138 (3-to-8 Decoder), 74LS373 (Octal D-Latch), a 320 ohm resistor, and SIP resistors, making sure all chips were grounded. After I was sure I had the circuit wired correctly, I connected the ciruit to power. An image of my circuit is included below:

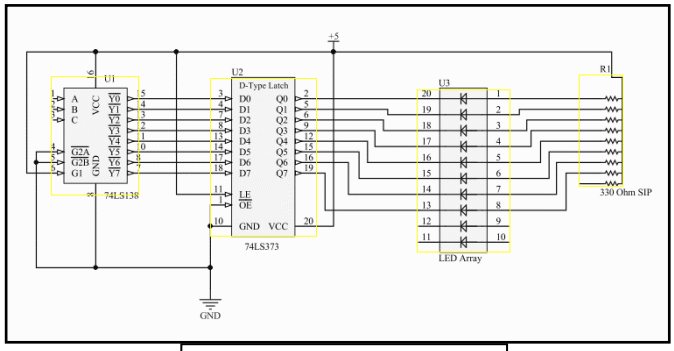

Figure 1 – “Lab02-Fig1”

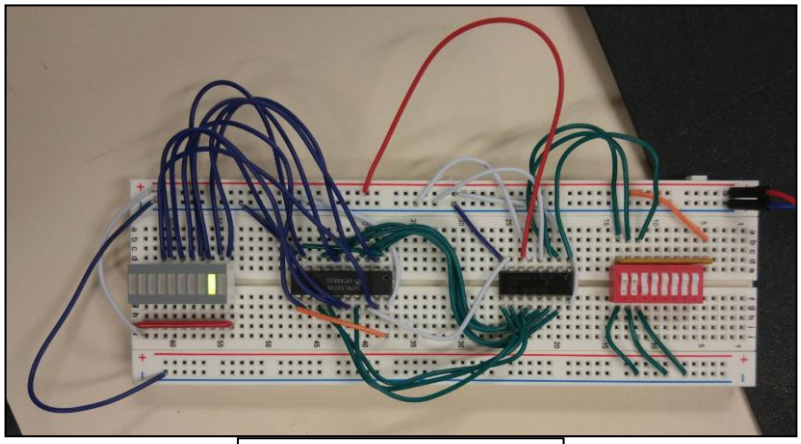

Figure 2 – Circuit 1

2. Once the first circuit was wired, I tested to see if the circuit worked as expected. To test my circuit, I used pins 6, 7, and 8 to be my three inputs for the 3-8 Decoder. As I increased the value of my inputs by counting up in binary, I noticed that the LED array was also counting up by moving by one bit to the right for every bit increase in binary. Below are some photographs taken of my circuit as I counted up in binary on the DIP switches.

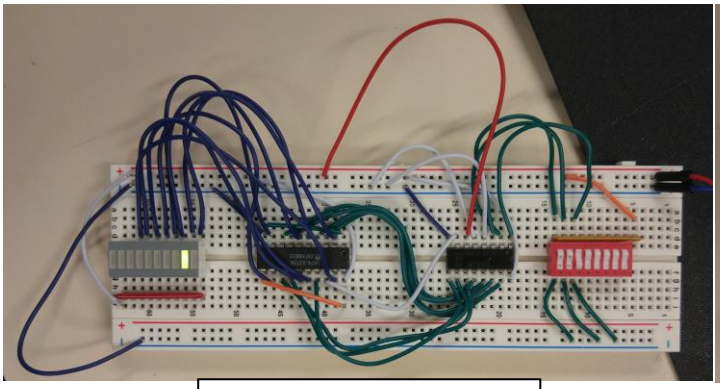

Figure 3 – Circuit 1 (001)

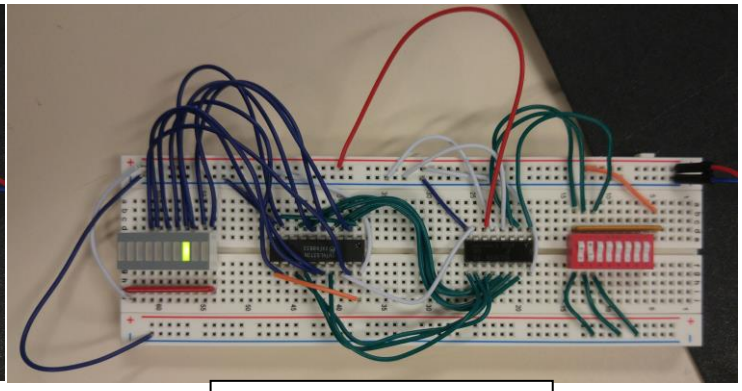

Figure 4 – Circuit 1 (010)

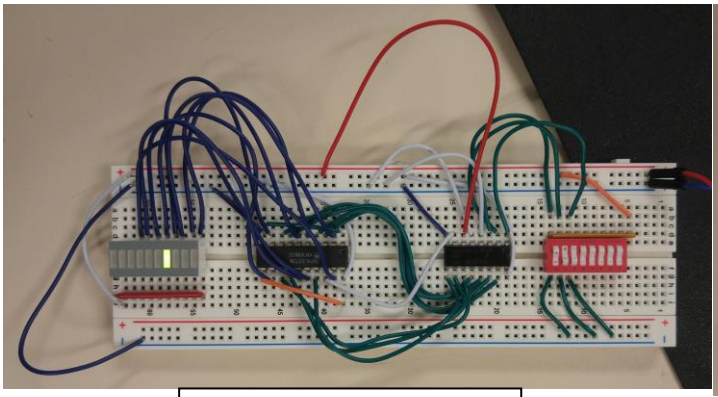

Figure 5 – Circuit 1 (011)

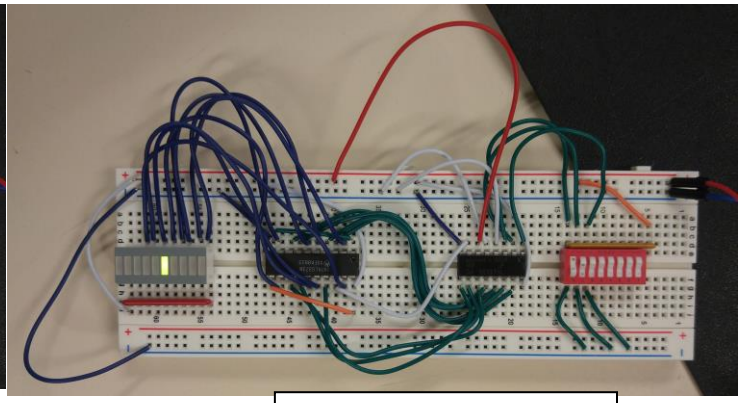

Figure 6 – Circuit 1 (100)

And so on, until I went from 000 to 111.

3. The second part of this lab was to replace the DIP switches with two buttons. This circuit was named "Lab02-Fig1". One would act as the clock, and the other would act as the CLR for the LED array. For this part of the lab, I observed that if the CLR button was held down, it would disable the CLR and it would allow data to be inputted to the memory every time the clock button was pressed. Once the CLR was released, clock cycles would now shift data to the right, deleting bit data.

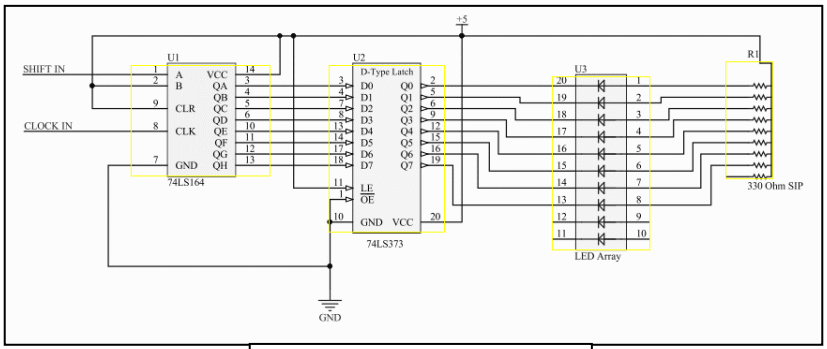

Figure 7 – "Lab02-Fig1"

4. I recorded data, holding down the CLR button while I pressed the Clock button 8 times, then I released the CLR button and pressed the Clock button another 8 times, this allowed the shift register to shift the data out of the register. Images of this process are on the next page:

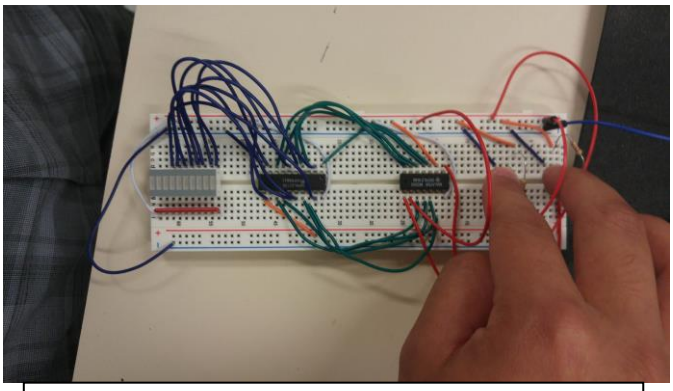

Figure 8 – Circuit 2 (CLR = held, 0 Clock Cycles)

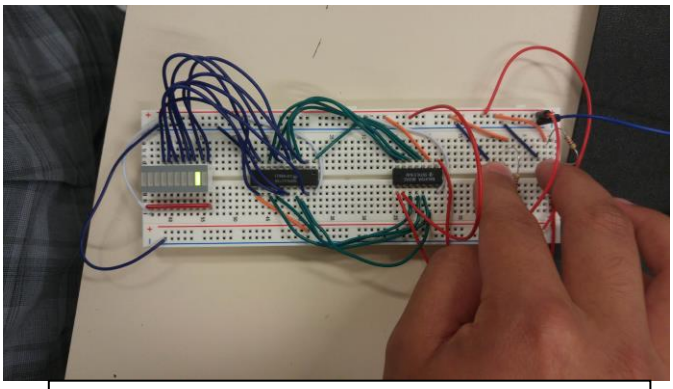

Figure 9 – Circuit 2 (CLR = held, 1 Clock Cycle)

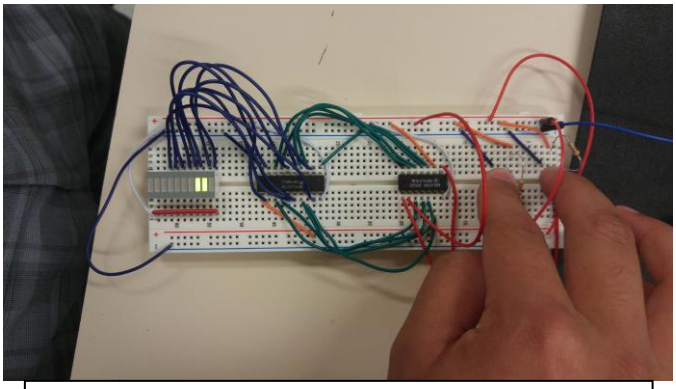

Figure 10 – Circuit 2 (CLR = held, 2 Clock Cycles)

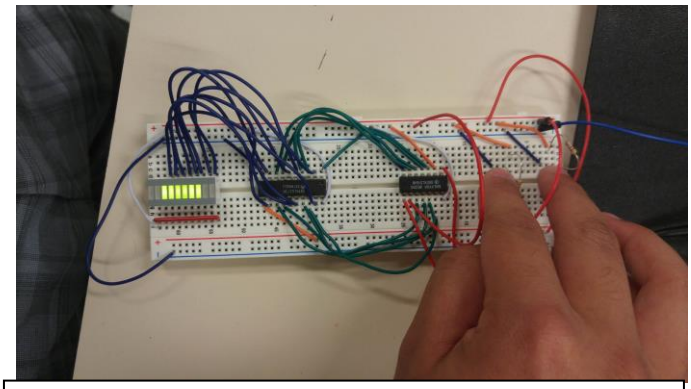

Figure 11 – Circuit 2 (CLR = released, 9 Clock Cycles)

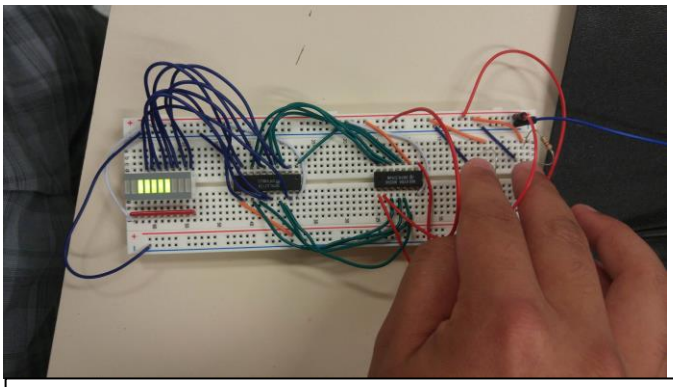

Figure 12 – Circuit 2 (CLR = released, 10 Clock Cycles)

And so on, until all the bits were cleared from the memory.

Questions:

What happens when the LE of the 74LS373 is on low? Why?

- When the LE of the 74LS373 is low, the enable is not on, so changing the bits on the switches does nothing because the enable controls whether the clock cycle affects the IC or not.

Why should you tie the CLR pin on high?

- When you tie the CLR pin on high, it is clearing by default with every clock cycle, until you hold the button, which inverts it.

What function(s) does the 74LS164 provide?

- The 74LS164 is a Parallel-Out Serial Shift Register, which means that with each clock cycle, it will shift a bit of data to the left, increasing the significance of the bit by 1.