Risk Management Plan

1. Physical Layer: Spectral Crowding & Leakage

- **The Risk:** As we utilize a d=6 manifold, the energy levels of the Fluxonium qudit become more "crowded" compared to a standard qubit. Fast control pulses (20ns) have a wider frequency bandwidth, which can lead to **unintentional leakage**—where driving State 3 accidentally excites State 4 or 5.
- **The m107B Fix:** We utilize the **high anharmonicity** inherent in Fluxonium to keep the transitions distinct.
- **Adaptability:** If crowding increases, we will deploy **commensurate pulse timing** or circularly polarized drives to suppress counter-rotating errors that typically degrade fast, low-frequency gates.

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2. Interconnect Layer: Thermal Load & Scalability

- **The Risk:** Scaling to modular data centers increases the number of microwave control lines, creating a **thermal bottleneck**. Each coaxial cable carries heat from room temperature to the 10mK stage, potentially exceeding the dilution refrigerator's cooling power.
- **The m107B Fix:** Our Base-6 protocol natively reduces the "cable-per-bit" ratio. By carrying **2.58 bits per site**, we reduce physical cabling overhead by **~61%**, directly lowering the passive thermal load.
- **Adaptability:** If thermal load remains high, we can transition to **superconducting flex-cables** or frequency-division multiplexing to further densify the I/O without increasing heat transport.

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3. Hardware Layer: Frequency Drift & Calibration

- **The Risk:** Fluxonium qudits are sensitive to magnetic flux fluctuations. Environmental noise can cause the 0–5 energy levels to drift, which would immediately invalidate the pre-programmed **GRAPE pulse sequences**.
- **The m107B Fix:** We integrate an **Active Flux Feedback loop** controlled by a high-speed FPGA. This system monitors "pilot tones" and adjusts the flux bias in real-time to "lock" the manifold frequencies.
- **Adaptability:** In the event of extreme drift, the system can trigger a **"Hot Swap" recalibration**, where a Neural Network optimizer rapidly re-tunes the pulse shapes without shutting down the entire cluster.

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4. Data Layer: Readout Ambiguity

- **The Risk:** Distinguishing six distinct "blobs" in the IQ plane is significantly more difficult than a binary 0/1. Noise in the signal chain can cause the states to overlap, leading to **readout errors**.
- **The m107B Fix:** We utilize **Traveling Wave Parametric Amplifiers (TWPA)** to maximize SNR at the quantum limit and an **SVM-based Neural Discriminator** to draw non-linear boundaries between states.
- **Adaptability:** If fidelity drops, we can implement **2D-readout techniques** (similar to 2D-NMR) to spread spectral information across two axes, effectively separating overlapping peaks.

Risk Category	Technical Challenge	m107B Mitigation Strategy
Physics	Spectral Crowding	Fluxonium Anharmonicity + GRAPE
Thermal	Multi-Fridge Heat Load	61% Cabling Reduction (Base-6)
Drift	Magnetic Flux Fluctuation	Active FPGA Feedback Loop
Readout	6-State Overlap	TWPA + Neural Network Classification

Prob (Probability): 1 (Unlikely) to 10 (Inevitable)

Sev (Severity): 1 (Minor Glitch) to 10 (Project Failure)

RPN (Risk Priority Number): Prob × Sev (Scores > 40 require immediate mitigation)

Failure Mode	Potential Cause	Prob	Sev	RPN	Detection Method	Mitigation Strategy
Spectral Leakage	Fast 20ns pulses exceed the anharmonicity limit, driving state $	3\rangle \to	4\rangle$ unintentionally.	6	8	**48**
Frequency Drift	External magnetic flux noise shifts the 0–5 energy levels, detuning the system.	8	9	**72**	"Pilot Tone" spectroscopy failing to match expected resonance.	**Active Feedback Loop:** FPGA adjusts flux bias every 100μs to lock frequency.
Readout Ambiguity	Signal-to-Noise Ratio (SNR) drops; state "clouds" in IQ plane overlap.	5	7	**35**	Fidelity check drops below 99% threshold.	**Neural Discrimination:** Switch from Euclidean logic to SVM/Neural Net classifier.

Failure Mode	Potential Cause	Prob	Sev	RPN	Detection Method	Mitigation Strategy
Cryo-Link Heat	100+ Waveguides bridge 4K to 10mK stages, overwhelming cooling power.	3	10	**30**	Mixing chamber temperature sensors reading >20mK.	**Density Advantage:** Utilization of Base-6 protocol reduces physical cable count by 61%.
Transduction Loss	(Phase 2 Only) Electro-optic conversion efficiency drops below 1%.	7	9	**63**	Optical power meter at receiver node shows <1 photon/pulse.	**Signal Budgeting:** 6065x signal retention design provides buffer for high loss.

The 72 represents the raw risk of a naked Fluxonium circuit. However, Phase 1 hardware roadmap includes operating at the **Half-Flux Sweet Spot**

$$(\Phi_0/2)$$

to suppress first-order noise, and utilizing **Robust GRAPE** sequences to broaden the control bandwidth.

With these mitigations, the projected effective RPN drops to **15**, turning a critical failure mode into a manageable maintenance task.

Failure Mode	Old RPN	New Prob	New Sev	New RPN
Frequency Drift	**72**	**3** (Sweet Spot)	**5** (Robust Pulses)	**15**

Direct electro-optic conversion is risky. That is why Phase 2 roadmap utilizes **Erbium-doped memory buffers**. By decoupling the storage from the conversion, we transform 'Signal Loss' into 'Signal Latency.'

Furthermore, m107B pulse design provides a **60 dB signal budget**, meaning we can tolerate transduction efficiencies as low as 0.1% and still close the link.

Failure Mode	Old RPN	New Prob	New Sev	New RPN
Transduction Loss	**63**	**4** (6065x Signal Buffer)	**4** (Erbium Memory Retry)	**16**

Compatibility:

Google's current structure uses Transmon where as m107B is Fluxonium. The fix, Hybrid Achitecture, this is assuming Google does not wish to commit to a switch else it switches to Fluxonium and we no longer have a compatibility issue.

m107B is designed as the *Interconnect Node*, not the Compute Node. We use Fluxonium specifically for the 'Long-Haul' link because of its high anharmonicity. Inside the fridge, we can couple the m107B Fluxonium to the standard Sycamore Transmons using a simple capacitive bus.

Compatibility Check	**Status**	**The "m107B" Solution**
Physical Infrastructure	**100% Compatible**	Fits standard SMA ports and dilution fridges.
Control Electronics	**90% Compatible**	Uses standard FPGAs, just needs new firmware code.
Processor Architecture	**Hybrid Required**	Need to "bridge" Transmon to Fluxonium.
Optical Network	**Incompatible (Phase 1)**	Solved by using Microwave Waveguides instead of fiber.