MOUMITA DEY

935 Marietta Street NW, Apt 641◇ Atlanta, Georgia 30318
(470) · 263 · 1484 ◇ mdey6@gatech.edu ◇ moumita.md.dey@gmail.com
http://www.prism.gatech.edu/~mdey6/ ◇ https://www.linkedin.com/in/moumitadeymd

OBJECTIVE

Seeking internship in summer 2018 in fields related to computer architecture.

EDUCATION

Georgia Institute of Technology, Atlanta *Aug 2015 - Present*
Graduate PhD student in School of Electrical and Computer Engineering
Relevant Courses: Advanced Computer Architecture, Advanced Programming Techniques, Interconnection Networks, Advanced VLSI Systems, Physical Design Automation, Advanced Digital Design using Verilog
GPA: 3.77/4.00

VES Institute of Technology, Mumbai, India *Aug 2011 - Jun 2015*
Bachelor of Engineering in Electronics Engineering
Ranked 9th among ∼20,000 students in University of Mumbai in B.E. in Electronics Engineering course
Aggregate: 78.43%

TECHNICAL SKILLS

Programming Languages	C, C++, Verilog, VHDL, Assembly Language (x86)
Software	MatLab, Cadence Virtuoso, Quartus Prime, ModelSim, Xilinx ISE, Code Composer Studio
Simulators	SESC, gem5

EXPERIENCE

Graduate Research Assistant, Georgia Tech Aug 2016 - Present
Advisor: Prof. Milos Prvulovic, Professor, School of Computer Science *Atlanta, GA*

· Working towards the development of a new technique for wirelessly monitoring Internet of Things (IoT) devices for malicious software without affecting the operation of the ubiquitous but low-power equipment.
· Focusing on working on identification and profiling of microarchitectural events such as last level cache misses through sidechannel analysis.

Graduate Teaching Assistant, Georgia Tech Aug 2015 - Jul 2016
Instructors: Dr. Tom Collins & Kevin Johnson, School of ECE *Atlanta, GA*

· Conducting two lab sessions for ∼35 students working on hardware design and prototyping based on Altera DE2 FPGAboard.
· Grade lab reports, presentations, technical documents and proposals pertaining to IEEE guidelines, and hold individual consultations to help students as a part of the Undergraduate Professional Communication Program.

Summer Trainee, Nuclear Power Corporation of India Ltd. Jun 2014 - Jul 2014
R&D-Electronic Systems *Mumbai, India*

· Programmed Altera FPGA to perform Byte Write operation on the Serial EEPROM T24C02B using I2C protocol and subsequently Random Read on the same location.

- Created a PC interface to control the output of DAC IC AD5382, which was programmed by the FPGA depending upon the desired output voltage taken from the user via keyboard using the RS232 protocol.

Research Intern, Bhabha Atomic Research Center Jun 2013 - Jul 2013
Advisor: Asim Kar, Scientific Officer, Department of Remote Handling and Robotics Mumbai, India

- Worked on "Obstacle Avoidance: A Potential Field Theory Approach" project.
- Studied and implemented various popular sensor-based reactive navigation methods. Experimented with the potential field approach and observed results in various simulated environments.
- Designed a novel sector-based navigation algorithm to overcome the shortcomings of the conventional approach. This algorithm analyzes the sensor data projecting into sector map and drives the robot through free sectors closer to the goal.
- The simulation results show that the developed method provides much smoother trajectories for the robot even in cluttered situations.
- Compared this navigation algorithm with the conventional Potential Field Theory algorithm in both a simulated environment based on Microsoft Visual Studio, and on a real robot equipped with laser sensor.

PROJECTS

FPGA Systems Design using Verilog Jan 2017 - May 2017
Instructor: Dr. Timothy Brothers, Georgia Tech Research Institute *Atlanta, GA*

- Designed and implemented various FPGA-based system controllers for GPS, VGA-Serial convertor and irrigation systems in Quartus.
- Implemented image transpose and Sobel operator based edge detection on a grayscale image using an FPGA.

Polish Expression based Floorplanning : Simulated Annealing Aug 2016 - Dec 2016
Instructor: Prof. Sung-Kyu Lim, Professor, School of ECE *Atlanta, GA*

- Created a simulator to perform optimized floorplanning on any given list of hard blocks based on a simulated annealing approach minimizing both area and half perimeter wire length.
- In order to create more room for optimization, the * and + operators in the initial Polish expression were taken randomly. Data structures were created to model the Polish expression and the slicing tree that take into account all internal nodes, including left, right and parent nodes, facilitating fast development of advanced algorithms, and the graphics was created using OpenGL.The cooling rate, initial temperature, cost function and stopping conditions were set based on the saturation observed after multiple runs of simulated annealing.
- Apart from the conventional M1, M2 and M3 moves of simulated annealing, an M4 move was introduced to rotate the operand modules at lower temperatures, easing the path to reach the local minima. The Stockmeyer algorithm applied after the simulated annealing had almost no change as the M4 move was either very close or already at the most optimal solution.
- Overall, it was observed that an average of 65% HPWL reduction, 90% chip area reduction and 80% chip utilization was achieved after testing multiple differently sized circuits on the designed simulator.

Handling C++ STL Libraries Aug 2016 - Dec 2016
Instructor: Prof. George P. Riley, Professor, School of ECE *Atlanta, GA*

- Implemented 2D image Fourier Transform using MPI and pthreads with barrier.
- Using the GMP library, performed RSA encryption, decryption and breaking using Pollard rho algorithm for factorization.
- Explored the OpenGL library by creating a rotating icosahedron of varying vertices.
- Created a custom library identical to the vector STL library containing corresponding functions.

· Implemented Mandelbrot set using OpenGL for graphics and pthreads for speed improvement with zoom function.

Out-of-order Superscalar Processor using Tomasulo Algorithm Jan 2016 - May 2016
Instructor: Prof. Tom Conte, Professor, School of ECE *Atlanta, GA*

· Designed a 5-stage pipeline structure with Fetch, Dispatch, Scheduling, Execute and State Update.
· Implemented two exception handling schemes: ROB with bypass and Checkpoint Repair.
· Experimented successfully on multiple setups.

Approximation on On-Chip Networks for Mitigation of Memory and Bandwidth Walls Jan 2016 - May 2016
Instructor: Prof. Tushar Krishna, Assistant Professor, School of ECE *Atlanta, GA*

· Developed a novel approach to solve the tradeoff problem of limited off-chip bandwidth and long access latency in CMPs by implementing approximation on on-chip networks.
· Based on Rollback-Free Value Prediction approximation technique, which manipulates safe-to-approximate loads in LLC misses.
· Here, safe-to-approximate loads are manipulated by the approximator both at the network interface and in a router using a drop rate parameter, which decides the fate of a traversing flit drop or continue.
· Achieved up to 10% power efficiency and 50% latency improvement for an 8x8 mesh topology at a cost of 80% accuracy with a negligible area overhead.

SRAM Memory System and Arithmetic Unit Aug 2015 - Dec 2015
Instructor: Prof. Saibal Mukhopadhyay, Professor, School of ECE *Atlanta, GA*

· Designed a 50 nm technology based adder system interfaced with 16x32 SRAM array to perform sequential reads and accumulation.
· Achieved full functionality in post-layout simulation and compared its performance against pre-layout simulation.
· The post-layout design with its extracted parasitics achieved a total power consumption of 470 uW with an SRAM array area efficiency of 63.37% when operated on a nominal supply voltage of 800 mV and frequency of 1 GHz.
· In comparison with other teams, our design had capabilities of working at frequencies upto 2.93 GHz even at nominal voltage.

An Innovative Approach to Location based Services and Traffic Management System Jul 2014 - Apr 2015
Instructor: Mr. Hardik Shah, Assistant Professor, VES Institute of Technology *Mumbai, India*

· Project Link: `https://www.youtube.com/watch?v=Ux3pjuXfrpw`
· Built a positioning and navigation system based on the communication between the RF transmitters present on the road and the RF receiver present in the vehicle without using the Internet or GPS, based on offline maps.
· The user has the option of routing through a "way-point". All the distances are calculated using shortest-path algorithm.
· Worked on TI's ARM Cortex M4 Tiva controller and CC2530 SoC for RF communication.
· Developed touch screen GUI and incorporated features such as emergency services and vehicle tracking.
· Implemented the system throughout the college campus.

Kindle for the Blind Aug 2013 - Jan 2014
Texas Instruments Innovation Challenge, India Analog Design Contest 2014 *Mumbai, India*

· Project Link: `https://www.youtube.com/watch?v=ZGs2-nnhLTY`

· Funded by Texas Instruments India (out of 1754 proposals from 321 colleges across India). Competed as semi-finalists in the competition.
· Built a TI's MSP430F5659 microcontroller based device to take voice input from a visually impaired user of the eBook name and display the eBook on the prototypic LED matrix display by loading it from the flash drive containing the eBooks stored in a .txt format.

PUBLICATIONS

· Dey, Moumita, Virag Doshi, Sarvesh Patkar, Vinayak Joshi, and Hardik Shah. "Braill-e-Book: An Innovative Idea for an Economical, User-Friendly and Portable eBook Reader for the Visually Impaired." *International Journal of Scientific and Research Publications* 4, no. 10 (2014): 1.

· Dudwadkar, Asawari, Sarvesh Patkar, Virag Doshi, and Moumita Dey. "An Interactive User Interface for a multi-channel Digital to Analog Converter using an FPGA." *Journal of Information Technology & Computer Applications* 2, no. 1 (2015).