(De/Re)-Composition of Data-Parallel Computations via Multi-Dimensional Homomorphisms

A Deep Dive into the MDH Formalism

ANONYMOUS AUTHOR(S)

Data-parallel computations, such as linear algebra routines (BLAS) and stencil computations, constitute one of the most relevant classes in parallel computing, e.g., due to their importance for deep learning. Efficiently de-composing such computations for the memory and core hierarchies of modern architectures and re-composing the computed intermediate results back to the final result – we say *(de/re)-composition* for short – is key to achieve high performance for computations on, e.g., GPU and CPU. Current high-level approaches to generating data-parallel code are often restricted to a particular subclass of data-parallel computations and architectures (e.g., only linear algebra routines on only GPU, or only stencil computations), and/or the approaches rely on a user-guided optimization process for a well-performing (de/re)-composition of computations, which is complex and error prone for the user.

We formally introduce a systematic (de/re)-composition approach that is general enough to express a broad combination of data-parallel computations targeting different kinds of parallel architectures, inspired by the algebraic formalism for *Multi-Dimensional Homomorphisms (MDH)*. Our approach efficiently targets the memory and core hierarchies of state-of-the-art architectures, by exploiting our introduced (de/re)-composition approach for a correct-by-construction, parametrized cache blocking and parallelization strategy. We show that our approach is powerful enough to express – in the same formalism – the (de/re)-compositions of different existing state-of-the-art approaches, and we demonstrate that the parameters of our strategies enable systematically generating code that can be fully automatically optimized (auto-tuned) for the target parallel architecture and characteristics of the input and output data (e.g., their sizes and memory layouts). Our experiments confirm that our auto-tuned code achieves higher performance than the state of the art, including hand-optimized solutions provided by vendors (such as NVIDIA cuBLAS/cuDNN and Intel oneMKL/oneDNN), on real-world data sets and for a variety of data-parallel computations, including: linear algebra routines, stencil and quantum chemistry computations, data mining algorithms, and computations that recently gained high attention due to their relevance for deep learning.

1 INTRODUCTION

Data-parallel computations constitute one of the most relevant classes in parallel computing. Important examples of such computations include linear algebra routines (BLAS) [Whaley and Dongarra 1998], various kinds of stencil computations (e.g., Jacobi method and convolutions) [Hagedorn et al. 2018], quantum chemistry computations [Kim et al. 2019], and data mining algorithms [Rasch et al. 2019b]. The success of many application areas critically depends on achieving high performance for their data-parallel building blocks on a variety of parallel architectures. For example, highly-optimized BLAS implementations combined with the computational power of modern GPUs currently enable deep learning to significantly outperform other existing machine learning approaches for speech recognition and image classification.

Data-parallel computations are characterized by applying the same function (a.k.a *scalar function*) to each point in a multi-dimensional grid of data (a.k.a. *array*), and combining the obtained results in the grid's different dimensions using so-called *combine operators* [Rasch and Gorlatch 2016].

Figures 1 and 2 illustrate data parallelism using as examples two popular computations: i) linear algebra routine *Matrix-Vector multiplication (*`MatVec`*)*, and ii) stencil computation *Jacobi (*`Jacobi1D`*)*. In the case of `MatVec`, the grid is 2-dimensional and consists of pairs, each pointing to one element of the input matrix $M_{i,k}$ and the vector v_k. To each pair, scalar function $f(M_{i,k}, v_k) :=$

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$$\begin{pmatrix} M_{1,1} & \dots & M_{1,K} \\ \vdots & \ddots & \vdots \\ M_{I,1} & \dots & M_{I,K} \end{pmatrix}, \begin{pmatrix} v_1 \\ \vdots \\ v_K \end{pmatrix} \xmapsto{\texttt{MatVec}} \begin{array}{|ccc|} \hline f(M_{1,1}, v_1) & \dots & f(M_{1,K}, v_K) \\ \vdots & \ddots & \vdots \\ f(M_{I,1}, v_1) & \dots & f(M_{I,K}, v_K) \\ \hline \end{array}^{\circledast_2}_{\circledast_1} = \begin{pmatrix} M_{1,1} * v_1 + \ldots + M_{1,K} * v_K \\ \vdots \\ M_{I,1} * v_1 + \ldots + M_{I,K} * v_K \end{pmatrix} = \begin{pmatrix} w_1 \\ \vdots \\ w_I \end{pmatrix}$$

Fig. 1. Data parallelism illustrated using the example *Matrix-Vector Multiplication* (`MatVec`)

$M_{i,k} * v_k$ (multiplication) is applied, and results in the i-dimension are combined using combine operator $\circledast_1(\,(x_1,\ldots,x_n)\,,\,(y_1,\ldots,y_m)\,) \coloneqq (x_1,\ldots,x_n,y_1,\ldots,y_m)$ (concatenation) and in k-dimension using operator $\circledast_2(\,(x_1,\ldots,x_n)\,,\,(y_1,\ldots,y_m)\,) \coloneqq (x_1+y_1,\ldots,x_n+y_n)$ (point-wise addition). Similarly, the scalar function of `Jacobi1D` is $f(v_{i+0}, v_{i+1}, v_{i+2}) \coloneqq c * (v_{i+0} + v_{i+1} + v_{i+2})$ which computes the Jacobi-specific function for an arbitrary but fixed constant c; `Jacobi1D`'s combine operator $\circledast_1$ is concatenation. We formally define scalar functions and combine operators in Section 2 of this paper.

Achieving high performance for data-parallel computations is considered important in both academia and industry, but has proven to be challenging. In particular, achieving high performance that is portable (i.e., the same program code achieves a consistently high level of performance across different architectures and characteristics of input/output data, such their size and memory layout) and in a user-productive way is identified as an ongoing, major research challenge. This is because for high performance, an efficient *(de/re)-composition* of computations – meaning their *decomposition*, *scalar computation*, and *re-composition* (explained in Figure 3 and discussed thoroughly in this paper) – is required to efficiently target the deep and complex memory and core hierarchies of state-of-the-art architectures, via efficient cache blocking and parallelization strategies [Khronos 2022b; NVIDIA 2022g; OpenMP 2022]. Moreover, to achieve performance that is portable over architectures, the programmer has to consider that architectures often differ significantly in their characteristics [Sun et al. 2019]: depth of memory and core hierarchies, automatically managed caches (as in CPUs) vs manually managed caches (as in GPUs), etc. Productivity is often also hampered: state-of-the-art programming models (such as OpenMP for CPU, CUDA for GPU, and OpenCL for multiple kinds of architectures) currently operate on a low level of abstraction. Thereby, the models require from the programmer explicitly implementing the (de/re)-composition of computations to/from architecture's different memory and core layers, which needs, for example, complex and error-prone index computations, as well as explicitly managing memory and threads on multiple layers.

Current high-level approaches to generating data-parallel code usually struggle with addressing in one combined approach all three challenges: *performance*, *portability*, and *productivity*. For example, approaches such as Apache TVM [Chen et al. 2018a], Halide [Ragan-Kelley et al. 2013], Fireiron [Hagedorn et al. 2020a] and LoopStack [Wasti et al. 2022] achieve high performance, but incorporate the user into the optimization process – by requiring from the user explicitly expressing optimizations in a so-called *scheduling language* – which is error prone and needs expert knowledge about low-level code optimizations, thus hindering user's productivity. In contrast, *polyhedral approaches* such as Facebook's TC [Vasilache et al. 2019], PPCG [Verdoolaege et al. 2013], and

$$\begin{pmatrix} v_1 \\ \vdots \\ v_N \end{pmatrix} \xmapsto{\texttt{Jacobi1D}} \begin{array}{|c|} \hline f(v_1, v_2, v_3) \\ f(v_2, v_3, v_4) \\ \vdots \\ \hline \end{array}^{}_{\circledast_1} = \begin{pmatrix} c * (v_1 + v_2 + v_3) \\ c * (v_2 + v_3 + v_4) \\ \vdots \end{pmatrix} = \begin{pmatrix} w_1 \\ \vdots \\ w_{N-2} \end{pmatrix}$$

Fig. 2. Data parallelism illustrated using the example *Jacobi 1D* (`Jacobi1D`)

Pluto [Bondhugula et al. 2008b] are often fully automatic and thus productive, but usually specifically designed toward a particular architecture (e.g., only GPU as TC or only CPU as Pluto) and thus not portable. *Functional approaches*, such as Lift [Steuwer et al. 2015], are productive for functional programmers (e.g., with experience in *Haskell* [Haskell.org 2022] programming, which is based on small, functional building blocks for expressing computations), but the approaches often have difficulties in automatically achieving the full performance potential of architectures [Rasch et al. 2019a]. Furthermore, many of the existing approaches are specifically designed toward a particular subclass of data-parallel computations only, e.g., only tensor operations (as TC and LoopStack) or only matrix multiplication (as Fireiron), or they require significant extensions for new subclasses (as Lift for matrix multiplication [Remmelg et al. 2016] and stencil computations [Hagedorn et al. 2018]), which further hinders the productivity of the user.

In this paper, we formally introduce a systematic (de/re)-composition approach for data-parallel computations targeting state-of-the-art parallel architectures. We express computations via high-level functional expressions (specifying *what* to compute), in the form of easy-to-use higher-order functions, inspired by the algebraic formalism for *Multi-Dimensional Homomorphisms (MDHs)* [Rasch and Gorlatch 2016][1]. Our higher-order functions are capable of expressing various kinds of data-parallel computations (linear algebra, stencils, etc), in the same formalism and on a high level of abstraction, independently of hardware and optimization details, thereby contributing to user's productivity[2]. As target for our high-level expressions, we introduce functional low-level expressions (specifying *how* to compute) to formally reason about the de- and re-compositions of data-parallel computations; our low-level expressions are designed such that they can be straightforwardly transformed to executable program code (e.g., in OpenMP, CUDA, and OpenCL). To systematically lower our high-level expressions to low-level expressions, we introduce a formally sound, parameterized de-composition and re-composition approach. The parameters of our lowering process enable automatically computing low-level expressions that are optimized (auto-tuned [Balaprakash et al. 2018]) for the particular target architecture and characteristics of the input/output data, thereby achieving fully automatically high, portable performance. For example, we introduce parameters for flexibly choosing the target memory regions for de-composed and re-composed computations, and also parameters for flexibly setting an optimized data access pattern, based on a formal foundation.

We show that our high-level representation is capable of expressing various kinds of data-parallel computations, including computations that recently gained high attention due to their relevance for deep learning [Barham and Isard 2019]. For our low-level representation, we show that it can express the cache blocking and parallelization strategies of state-of-the-art parallel implementations – as generated by scheduling approach TVM and polyhedral compilers PPCG and Pluto – in one uniform formalism. Moreover, we present experimental results to confirm that via

[1] The existing MDH work introduces a proof-of-concept: 1) *high-level program representation* that relies on a semi-formal foundation, straightforward type system, and a higher-order function for expressing computations (but not for managing input and output data); 2) *code generator* specifically designed and optimized for the OpenCL programming model (thereby also being limited to OpenCL). We thoroughly compare to the existing MDH work in Section 6.6.

[2] We consider as the main users of our approach compiler engineers and library designers. Rasch et al. [2020a] show that our approach can also take straightforward, sequential code as input, which makes our approach attractive also to end users.

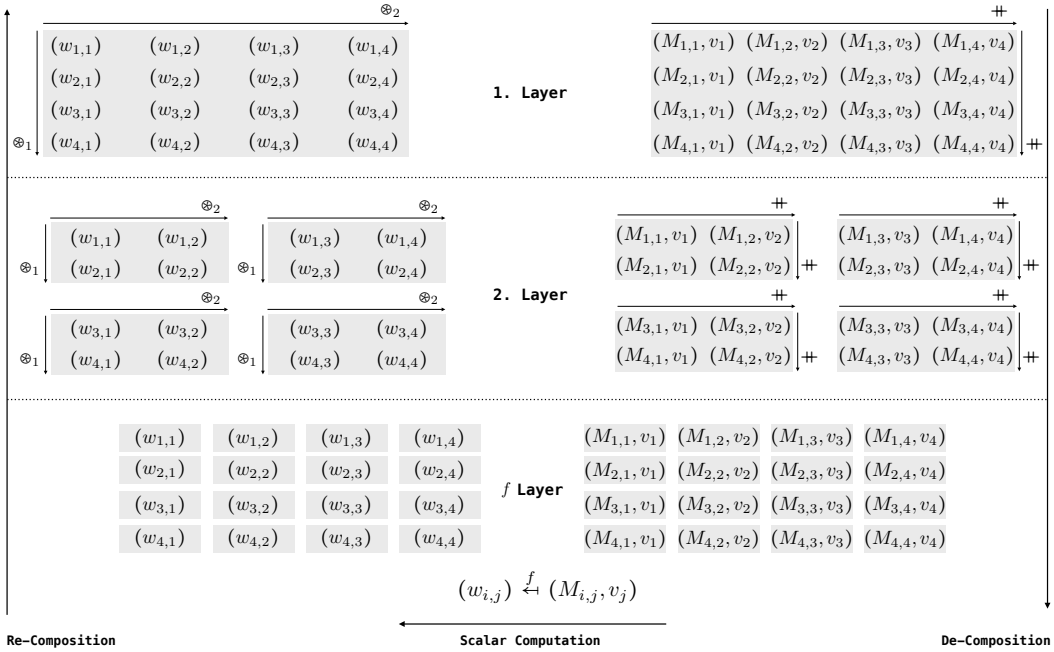


Fig. 3. Example (de/re)-composition of MatVec (Figure 1) on a 4×4 input matrix M and a 4-sized vector v: i) the *de-composition phase* (right part of the figure) partitions the concatenated input data into parts (a.k.a. *tiles* in programming), where $+\!\!+$ denotes the concatenation operator; ii) to each part, scalar function f is applied in the *scalar phase* (bottom part of figure), which is defined for MatVec as: multiplying matrix element $M_{i,j}$ with vector element v_j, resulting in element $w_{i,j}$; iii) the *re-composition phase* (figure's left part) combines the computed parts to the final result, using combine operator $\circledast_1$ for the first dimension (defined as *concatenation* in the case of MatVec) and operator $\circledast_2$ (*addition*) for the second dimension, correspondingly. All basic building blocks (*scalar function*, *combine operator*, ...) and concepts (e.g. *partitioning*) are defined later in this paper, based on algebraic concepts. For simplicity, this example presents a (de/re)-composition on 2 layers only, and we partition the input for this example into parts that have straightforward, equal sizes. Optimized values of semantics-preserving parameters (a.k.a. *tuning parameters*), like the number of parts or the application order of combine operators, are crucial for achieving high performance, as we discuss in this paper. Phases are arranged from right to left, inspired by the application order of function composition, as we also discuss later.

auto-tuning, our (de/re)-composition approach achieves higher performance than the state of the art, including hand-optimized implementations provided by vendors.

Summarized, we make the following three major contributions (illustrated in Figure 4):

(1) We introduce a high-level functional representation, inspired by the algebraic formalism of Multi-Dimensional Homomorphisms (MDHs), that enables uniformly expressing data-parallel computations on a high level of abstraction.

(2) We introduce a low-level functional representation that enables formally expressing and reasoning about (de/re)-compositions of data-parallel computations; our low-level representation is designed such that it can be straightforwardly transformed to executable program code in state-of-practice parallel programming models, including OpenMP, CUDA, and OpenCL.

(3) We introduce a systematic process to fully automatically lower an expression in our high-level representation to a device- and data-optimized expression in our low-level representation, in a formally sound manner, based on auto-tuning.

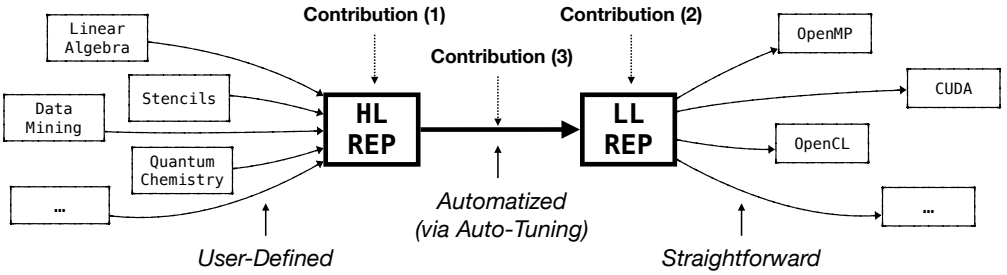


Fig. 4. Overall structure of our approach (contributions highlighted in bold)

The rest of the paper is structured as follows. We introduce our high-level functional representation (Contribution 1) in Section 2, and we show how this representation is used for expressing important data-parallel computations. In Section 3, we discuss our low-level functional representation (Contribution 2), and we confirm that it can express existing state-of-the-art low-level implementations, as generated by state-of-practice approaches TVM (scheduling based) and PPCG/-Pluto (polyhedral based). Section 4 shows how we systematically lower a computation expressed in our high-level representation to an expression in our low-level representation, in a formally sound, auto-tunable manner (Contribution 3). We present experimental results in Section 5, discuss related work in Section 6 (including a thorough comparison to previous work on MDHs), conclude in Section 7, and we present our ideas for future work in Section 8. Our Appendix, in Sections A-E, provides details for the interested reader that should not be required for understanding the basic concepts introduced in this paper.

2 HIGH-LEVEL REPRESENTATION FOR DATA-PARALLEL COMPUTATIONS

We introduce functional building blocks, in the form of higher-order functions, that express data-parallel computations on a high level of abstraction. The goal of our high-level abstraction is to express computations agnostic from hardware and optimization details, and thus in a user-productive manner, while still capturing all information relevant for generating high-performance program code. The building blocks of our abstraction are inspired by the algebraic formalism of *Multi-Dimensional Homomorphisms (MDHs)* which is an approach toward formalizing data parallelism (we compare in detail to the existing work on MDHs in Section 6.6).

Figure 5 shows a basic overview of our high-level representation. We express data-parallel computations using exactly three higher-order functions only (a.k.a. *patterns* or *skeletons* [Gorlatch and Cole 2011] in programming terminology): 1) `inp_view` transforms the domain-specific input data (e.g., a matrix and a vector in the case of matrix-vector multiplication) to a *Multi-Dimensional Array (MDA)* which is our internal data representation and defined later in this section; 2) `md_hom` performs the data-parallel computation; `md_hom` takes as input and output uniformly an MDA; 3) `out_view` transforms the computed MDA back to the domain-specific data representation.

In the following, after informally discussing an introductory example in Section 2.1, we formally define and discuss each higher-order function in detail in Section 2.2 (function `md_hom`) and Section 2.3 (functions `inp_view` and `out_view`). Note that Section 2.2 and Section 2.3 introduce and present the internals and formal details of our approach, which are not relevant for the end user of our system – the user only needs to operate on the abstraction level discussed in Section 2.1.

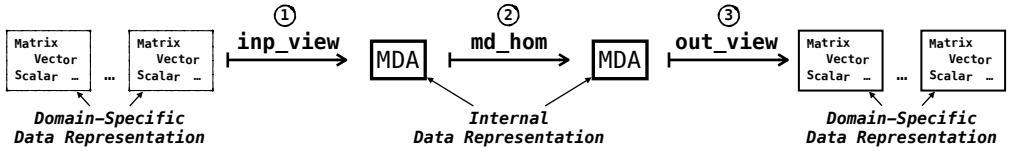


Fig. 5. High-level representation (overview)

2.1 Introductory Example

Figure 6 shows how our high-level representation is used for expressing the simple but illustrative example of matrix-vector multiplication MatVec[3] (Figure 1). Computation MatVec takes as input a matrix $M \in T^{I \times K}$ and vector $v \in T^K$ of arbitrary scalar type[4] T and sizes $I \times K$ (matrix) and K (vector), for arbitrary but fixed positive natural numbers $I, K \in \mathbb{N}$[5]. In the figure, based on index function $(i,k) \to (i,k)$ and $(i,k) \to (k)$, high-level function inp_view computes a function that takes M and v as input and maps them to a 2-dimensional array of size $I \times K$ (referred to as *input MDA* in the following and defined formally in the next subsection). The MDA contains at each point (i,k) the pair $(M_{i,k}, v_k) \in T \times T$ comprising element $M_{i,k}$ within matrix M (first component) and element v_k within vector v (second component). The input MDA is then mapped via function md_hom to an output MDA of size $I \times 1$, by applying multiplication $*$ to each pair $(M_{i,k}, v_k)$ within the input MDA, and combining elements within MDA's first dimension via $+\!\!+$ (concatenation – also defined formally in the next subsection) and in second dimension via + (point-wise addition). Finally, function out_view computes a function that straightforwardly maps the output MDA, of size $I \times 1$, to MatVec's result vector $w \in T^I$, which has scalar type T and is of size I. For the example of MatVec, the output view is trivial, but it can be used in other computations (such as matrix multiplication) to conveniently express more advanced variants of computations (e.g., computing the result matrix of matrix multiplication as transposed, as we demonstrate later).

```
MatVec<T∈TYPE | I,K∈ℕ> := out_view<T>( w:(i,k)↦(i) ) ∘
                              md_hom<I,K>( *, (++,+) ) ∘
                                  inp_view<T,T>( M:(i,k)↦(i,k) , v:(i,k)↦(k) )
```

Fig. 6. High-level expression for Matrix-Vector Multiplication (MatVec)[6]

2.2 Function md_hom

Higher-order function md_hom is introduced by Rasch and Gorlatch [2016] to express Multi-Dimensional Homomorphisms (MDHs) – a formal representation of data-parallel computations – in a convenient and structured way. In the following, we recapitulate the definition of MDHs and function md_hom, but in a more general and formally more precise setting than done in the original MDH work.

[3] The expression in Figure 6 can also be extracted from straightforward, annotated sequential code [Rasch et al. 2020a,b].
[4] We consider as *scalar types* integers $\mathbb{Z}$ (a.k.a. int in programming), floating point numbers $\mathbb{Q}$ (a.k.a. float or double), any fixed collection of types (a.k.a. *record* or *struct*), etc. We denote the set of scalar types as TYPE and provide details on them in the Appendix, Section A.2, for the interested reader.
[5] We denote by $\mathbb{N}$ the set of positive natural number $\{1, 2, \dots\}$, and we use $\mathbb{N}_0$ for the set of natural numbers including 0.
[6] Our technical implementation takes as input a representation that is equivalent to Figure 6, expressed via straightforward program code (see Appendix, Section A.4)

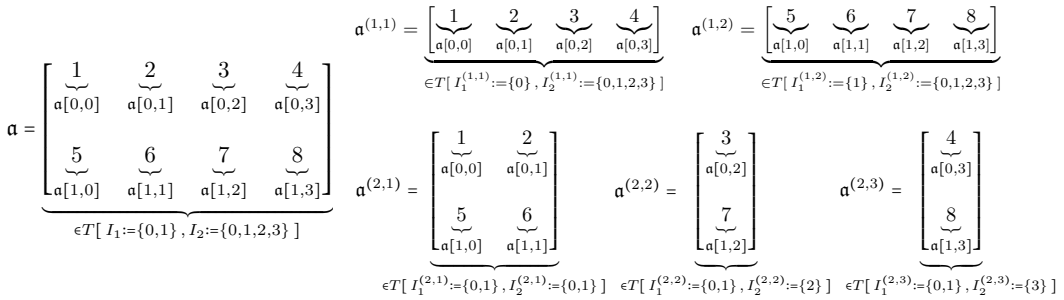


Fig. 7. MDA examples

In order to define Multi-Dimensional Homomorphisms (MDHs), we first need to introduce two central building blocks used in the definition of MDHs: i) *Multi-Dimensional Arrays (MDAs)* – the data type on which MDHs uniformly operate, and ii) *Combine Operators* which we use to combine elements within particular dimensions of an MDA.

Multi-Dimensional Arrays

Definition 1 (Multi-Dimensional Array)**.** Let $\texttt{MDA-IDX-SETs} := \{I \subset \mathbb{N}_0 \mid |I| < \infty\}$ be the set of all finite subsets of natural numbers, to which we also refer to as set of *MDA index sets* in the context of MDAs. Let further $T \in \texttt{TYPE}$ be an arbitrary scalar type, $D \in \mathbb{N}$ a natural number, $I := (I_1, \ldots, I_D) \in \texttt{MDA-IDX-SETs}^D$ a tuple of D-many MDA index sets, and $N := (N_1, \ldots, N_D) := (|I_1|, \ldots, |I_D|)$ the tuple of index sets' sizes.

A *Multi-Dimensional Array (MDA)* $\mathfrak{a}$ that has *dimensionality* D, *size* N, *index sets* I, and *scalar type* T is a function with the following signature:

$$\mathfrak{a} : I_1 \times \ldots \times I_D \to T$$

We refer to $I_1 \times \ldots \times I_D \to T$ as the *type* of MDA $\mathfrak{a}$.

Notation 1. For better readability, we denote MDAs' types and accesses to them using a notation close to programming. We often write:

- $\mathfrak{a} \in T[\, I_1, \ldots, I_D \,]$ instead of $\mathfrak{a} : I_1 \times \ldots \times I_D \to T$ to denote the type of MDA $\mathfrak{a}$;
- $\mathfrak{a} \in T[\, N_1, \ldots, N_D \,]$ instead of $\mathfrak{a} : [0, N_1)_{\mathbb{N}_0} \times \cdots \times [0, N_D)_{\mathbb{N}_0} \to T$;[7]
- $\mathfrak{a}[\, i_1, \ldots, i_D \,]$ instead of $a(i_1, \ldots, i_D)$ to access MDA $\mathfrak{a}$ at position $(i_1, \ldots, i_D)$.

Figure 7 illustrates six example MDAs. The left part of the figure shows MDA $\mathfrak{a}$ which is of type $\mathfrak{a} : I_1 \times I_2 \to T$, for $I_1 = \{0, 1\}$, $I_2 = \{0, 1, 2, 3\}$, and $T = \mathbb{Z}$ (integer numbers). On the right side, five MDAs are shown, named $\mathfrak{a}^{(1,1)}$, $\mathfrak{a}^{(1,2)}$, $\mathfrak{a}^{(2,1)}$, $\mathfrak{a}^{(2,2)}$, $\mathfrak{a}^{(2,3)}$ – the superscripts are part of the names and represent a two-dimensional numbering of the five MDAs. The MDAs $\mathfrak{a}^{(1,1)}$ and $\mathfrak{a}^{(1,2)}$ are of types $\mathfrak{a}^{(1,1)} : I_1^{(1,1)} \times I_2^{(1,1)} \to T$ and $\mathfrak{a}^{(1,2)} : I_1^{(1,2)} \times I_2^{(1,2)} \to T$, for $I_1^{(1,1)} = \{0\}$ and $I_1^{(1,2)} = \{1\}$, and coinciding second dimensions $I_2^{(1,1)} = I_2^{(1,2)} = \{0, 1, 2, 3\}$. The MDAs $\mathfrak{a}^{(2,1)}$, $\mathfrak{a}^{(2,2)}$, and $\mathfrak{a}^{(2,3)}$ are of types $\mathfrak{a}^{(2,1)} : I_1^{(2,1)} \times I_2^{(2,1)} \to T$, $\mathfrak{a}^{(2,2)} : I_1^{(2,2)} \times I_2^{(2,2)} \to T$, and $\mathfrak{a}^{(2,3)} : I_1^{(2,3)} \times I_2^{(2,3)} \to T$, and they coincide in the first dimension $I_1^{(2,1)} = I_1^{(2,2)} = I_1^{(2,3)} = \{0, 1\}$; their second dimensions are $I_2^{(2,1)} = \{0, 1\}$, $I_2^{(2,2)} = \{2\}$, and $I_2^{(2,2)} = \{3\}$. Note that MDAs $\mathfrak{a}^{(1,1)}, \mathfrak{a}^{(1,2)}, \mathfrak{a}^{(2,1)}, \mathfrak{a}^{(2,2)}, \mathfrak{a}^{(2,3)}$ can be

[7] We denote by $[L, U)_{\mathbb{N}_0} := \{\, n \in \mathbb{N}_0 \mid L \leq n < U \,\}$ the half-open interval of natural numbers (including 0) between L (incl.) and U (excl.).

considered as *parts* (a.k.a. *tiles* in programming) of MDA $\mathfrak{a}$. We formally define and use *partitionings* of MDAs in Section 3.

Combine Operators

A central building block in our definition of MDHs is a *combine operator*. Intuitively, we use a combine operator to combine all elements within a particular dimension of an MDA. For example, in Figure 1 (matrix-vector multiplication), we combine elements of the 2-dimensional MDA via combine operator *concatenation* in MDA's first dimension and via operator *point-wise addition* in the second dimension.

Technically, combine operators are functions that take as input two MDAs and yield a single MDA as their output (formal definition follows soon). Per definition, we require that the input MDAs' index sets coincide in all dimensions except in the dimension in which we combine; thereby, we catch undefined cases already at the type level, e.g., trying to concatenate improperly sized MDAs:

$$\underbrace{\underbrace{\begin{bmatrix}1&2&3\\4&5&6\\7&8&9\end{bmatrix}}_{\substack{3\times3\text{-many}\\\text{elements}}} +\!\!+ \underbrace{\begin{bmatrix}11&12\\13&14\\15&16\end{bmatrix}}_{\substack{3\times2\text{-many}\\\text{elements}}} = \underbrace{\begin{bmatrix}1&2&3&11&12\\4&5&6&13&14\\7&8&9&15&16\end{bmatrix}}_{\substack{3\times5\text{-many}\\\text{elements}}}}_{\text{well defined}} \qquad \underbrace{\underbrace{\begin{bmatrix}1&2&3\\4&5&6\\7&8&9\end{bmatrix}}_{\substack{3\times3\text{-many}\\\text{elements}}} +\!\!+ \underbrace{\begin{bmatrix}11&12\\13&14\end{bmatrix}}_{\substack{2\times2\text{-many}\\\text{elements}}} = ?}_{\lightning\ \text{undefined}}$$

Here, on the left, we can reasonably define the concatenation of MDAs that contain 3×3-many elements and 3×2 elements. However, as indicated in the right part of the figure, it is not possible to intuitively concatenate MDAs of sizes 3×3 and 2×2, as the MDAs do not match in their number of elements in any of the two dimensions.

Figure 8 illustrates combine operators informally using the example operators *concatenation* (left part of the figure) and *point-wise addition* (right part). We illustrate concatenation using the example MDAs $\mathfrak{a}^{(1,1)}$ and $\mathfrak{a}^{(1,2)}$ from Figure 7; for point-wise addition, we use MDAs $\mathfrak{a}^{(2,2)}$ and

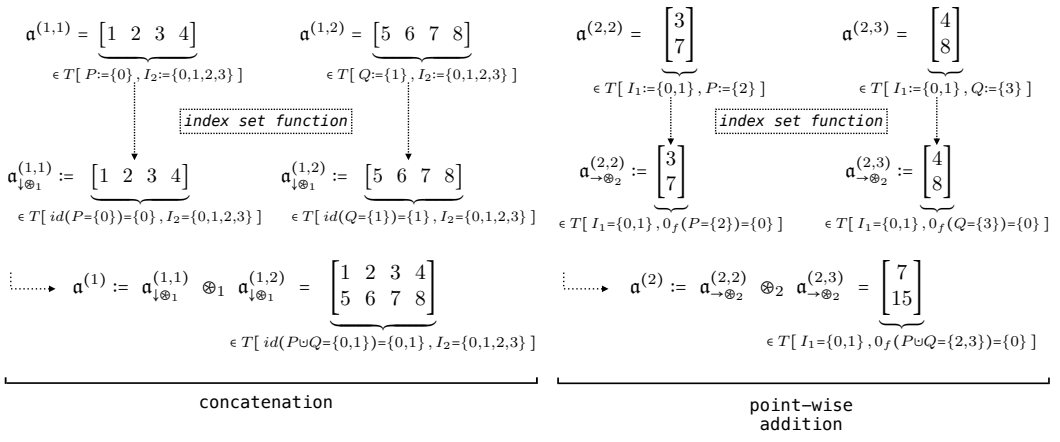


Fig. 8. Illustration of *combine operators* using the examples *concatenation* (left) and *point-wise addition* (right)

$\mathfrak{a}^{(2,3)}$ from Figure 7 (all MDAs are chosen arbitrarily, and the example works the same for other MDAs).

In the case of concatenation (left part of Figure 8), MDAs $\mathfrak{a}^{(1,1)}$ and $\mathfrak{a}^{(1,2)}$ coincide in their second dimension $I_2 := \{0, 1, 2, 3\}$, which is important, because we concatenate in the first dimension, thus requiring coinciding index sets in all other dimensions (as motivated above). In the case of the point-wise addition example (right part of Figure 8), the example MDAs $\mathfrak{a}^{(2,2)}$ and $\mathfrak{a}^{(2,3)}$ coincide in their first dimension $I_1 := \{0, 1\}$, as required for combining the MDAs in the second dimension. The varying index sets of the four MDAs are denoted as P and Q in the figure, which are in the case of the concatenation example, index sets in the first dimension of MDAs $\mathfrak{a}^{(1,1)}$ and $\mathfrak{a}^{(1,2)}$; in the case of the point-wise addition example, the varying index sets of MDAs $\mathfrak{a}^{(2,1)}$ and $\mathfrak{a}^{(2,2)}$ belong to the second dimensions.

In the following, we assume w.l.o.g. that that the varying index sets P and Q of MDAs to combine are disjoint. Our assumption will not be a limitation for us, because we will apply combine operators always to MDA parts that belong to the same MDA, causing the index sets of the parts to be disjoint by construction. For example, in the case of the concatenation example in Figure 8, the MDA parts $\mathfrak{a}^{(1,1)}$ and $\mathfrak{a}^{(1,2)}$ correspond to the first and second row of the same MDA $\mathfrak{a}$ in Figure 7, and in the case of the point-wise addition example, the parts $\mathfrak{a}^{(2,2)}$ and $\mathfrak{a}^{(2,3)}$ represent the third and fourth column of MDA $\mathfrak{a}$.

We define combine operators based on *index set functions* (also introduced formally soon). Index set functions precisely describe, on the type level, the index set of the combined output MDA and thus how an MDA's index set evolves during combination. For this, an index set function takes as input the input MDA's index set in the dimension to combine, and the function yields as its output the index set of the output MDA which is combined in this dimension. In the case of the concatenation example in Figure 8, the index set function is identity *id* and thus trivial. However, in the case of point-wise addition, the corresponding index set function is constant function 0_f which maps any index set to the singleton set $\{0\}$ containing index 0 only. This is because when combining via point-wise addition, the MDA shrinks in the combined dimension to only one element which we aim to uniformly access via MDA index 0. In Figure 8, we denote MDAs $\mathfrak{a}^{(1,1)}$, $\mathfrak{a}^{(1,2)}$, $\mathfrak{a}^{(2,2)}$, $\mathfrak{a}^{(2,3)}$ after applying the corresponding index set function as $\mathfrak{a}^{(1,1)}_{\downarrow\circledast_1}$, $\mathfrak{a}^{(1,2)}_{\downarrow\circledast_1}$, $\mathfrak{a}^{(2,2)}_{\rightarrow\circledast_2}$, $\mathfrak{a}^{(2,3)}_{\rightarrow\circledast_2}$; the combined MDAs are denoted as $\mathfrak{a}^{(1)}$ and $\mathfrak{a}^{(2)}$ in the figure. The concatenation operator is denoted in the figure generically as $\circledast_1$, and point-wise addition is denoted as $\circledast_2$, correspondingly.

We now define *combine operators* formally, and we illustrate this formal definition afterwards using the example operators *concatenation* and *point-wise combination*. For the interested reader, details on some technical design decisions of combine operators are outlined in the Appendix, Section B.1.

Definition 2 (Combine Operator). Let $\texttt{MDA-IDX-SETs} \dot{\times} \texttt{MDA-IDX-SETs} := \{ (P, Q) \in \texttt{MDA-IDX-SETs} \times \texttt{MDA-IDX-SETs} \mid P \cap Q = \varnothing \}$ denote the set of all pairs of MDA index sets that are disjoint. Let further $\Rightarrow^{\texttt{MDA}}_{\texttt{MDA}} : \texttt{MDA-IDX-SETs} \rightarrow \texttt{MDA-IDX-SETs}$ be a function on MDA index sets, $T \in \texttt{TYPE}$ a scalar type, $D \in \mathbb{N}$ an MDA dimensionality, and $d \in [1, D]_{\mathbb{N}}$ an MDA dimension.

We refer to any binary function $\circledast$ of type (parameters in angle brackets are type parameters)

$$\circledast^{<(I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D)\in\texttt{MDA-IDX-SETs}^{D-1},\,(P,Q)\in\texttt{MDA-IDX-SETs}\,\dot{\times}\,\texttt{MDA-IDX-SETs}>} :$$

$$T[\,I_1,\ldots,\underbrace{\Rightarrow^{\texttt{MDA}}_{\texttt{MDA}}(P)}_{\uparrow d},\ldots,I_D\,] \times T[\,I_1,\ldots,\underbrace{\Rightarrow^{\texttt{MDA}}_{\texttt{MDA}}(Q)}_{\uparrow d},\ldots,I_D\,]$$

$$\rightarrow T[\, I_1, \ldots, \underbrace{\Rightarrow^{\mathtt{MDA}}_{\mathtt{MDA}}(P \cup Q)}_{\uparrow\, d}, \ldots, I_D\,]$$

as *combine operator* that has *index set function* $\Rightarrow^{\mathtt{MDA}}_{\mathtt{MDA}}$, *scalar type* T, *dimensionality* D, and *operating dimension* d. We denote combine operator's type concisely as $\mathtt{CO}^{<\Rightarrow^{\mathtt{MDA}}_{\mathtt{MDA}} \mid T \mid D \mid d>}$.

Since function $\circledast$'s ordinary function type $T[\ldots] \times T[\ldots] \rightarrow T[\ldots]$ is generic in parameters $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D)$ and (P, Q) (these type parameters are denoted in angle brackets in Definition 2), we refer to function $\circledast$ as *meta-function*, to the type parameters in angle brackets as *meta-parameters*, and we say *meta-types* to $T[\, I_1, \ldots, \Rightarrow^{\mathtt{MDA}}_{\mathtt{MDA}}(P), \ldots, I_D\,]$ (first input MDA), $T[\, I_1, \ldots, \Rightarrow^{\mathtt{MDA}}_{\mathtt{MDA}}(Q), \ldots, I_D\,]$ (second input MDA), and $T[\, I_1, \ldots, \Rightarrow^{\mathtt{MDA}}_{\mathtt{MDA}}(P \cup Q), \ldots, I_D\,]$ (output MDA), as these types are generic in meta-parameters. Formal definitions and details about our meta-parameter concept are provided in Section A of our Appendix for the interested reader.

We use meta-functions as an analogous concept to *metaprogramming* in programming language theory to achieve high generality. For example, by defining combine operators as meta-functions, we can use the operators on input MDAs that operate on arbitrary index sets while still guaranteeing correctness, e.g., that index sets of the two input MDAs match in all dimensions except in the dimension to combine (as discussed above). For simplicity, we often refrain from explicitly stating meta-parameters when they are clear from the context; for example, when they can be deduced from the types of their particular inputs (a.k.a. *type deduction* in programming).

We now formally discuss the example operators *concatenation* and *point-wise combination*. For high flexibility, we define both operators generically in the scalar type T of their input and output MDAs, the MDAs' dimensionality D, as well as in the dimension d to combine.

Example 1 (Concatenation)**.** We define *concatenation* as function $+\!\!+$ of type

$$+\!\!+^{<T \in \mathtt{TYPE} \mid D \in \mathbb{N} \mid d \in [1,D]_{\mathbb{N}} \mid (I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D) \in \mathtt{MDA\text{-}IDX\text{-}SETs}^{D-1}, (P,Q) \in \mathtt{MDA\text{-}IDX\text{-}SETs} \,\dot{\times}\, \mathtt{MDA\text{-}IDX\text{-}SETs}>} :$$
$$T[\, I_1, \ldots, \underbrace{id(P)}_{\uparrow\, d}, \ldots, I_D\,] \times T[\, I_1, \ldots, \underbrace{id(Q)}_{\uparrow\, d}, \ldots, I_D\,] \rightarrow T[\, I_1, \ldots, \underbrace{id(P \cup Q)}_{\uparrow\, d}, \ldots, I_D\,]$$

where $id : \mathtt{MDA\text{-}IDX\text{-}SETs} \rightarrow \mathtt{MDA\text{-}IDX\text{-}SETs}$ is the identity function on MDA index sets. The function is computed as:

$$+\!\!+^{<T \mid D \mid d \mid (I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D),(P,Q)>}(\mathfrak{a}_1, \mathfrak{a}_2)[\, i_1, \ldots, \ i_d \ , \ldots, i_D\,]$$
$$:= \begin{cases} \mathfrak{a}_1[\, i_1, \ldots, \ i_d \ , \ldots, i_D\,] & , \ i_d \in P \\ \mathfrak{a}_2[\, i_1, \ldots, \ i_d \ , \ldots, i_D\,] & , \ i_d \in Q \end{cases}$$

The function is well defined, because P and Q are disjoint. We usually use an infix notation for $+\!\!+^{<\ldots>}$ (meta-parameters omitted via ellipsis), i.e., we write $\mathfrak{a}_1 +\!\!+^{<\ldots>} \mathfrak{a}_2$ instead of $+\!\!+^{<\ldots>}(\mathfrak{a}_1, \mathfrak{a}_2)$.

The vertical bar in the superscript of $+\!\!+$ denotes that function $+\!\!+$ can be partially evaluated (a.k.a. *Currying* [Curry 1980] in math and *multi staging* [Taha and Sheard 1997] in programming) for particular values of meta-parameters: $T \in \mathtt{TYPE}$ (first stage), $D \in \mathbb{N}$ (second stage), etc. Partial evaluation (formally defined in the Appendix, Definition 21) enables both: 1) expressive typing and thus better error elimination: for example, parameter $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D) \in \mathtt{MDA\text{-}IDX\text{-}SETs}^{D-1}$

can depend on meta-parameter $D \in \mathbb{N}$, because D is defined in an earlier stage, which allows precisely limiting the length of the tuple $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D)$ to $D-1$ index sets; 2) generality: for example, we can instantiate $+\!\!+$ to $+\!\!+^{<T>}$ which is specific for a particular scalar type $T \in \mathtt{TYPE}$, but still generic in meta-parameters $D \in \mathbb{N}$, $d \in [1, D]_{\mathbb{N}}$, ..., as these meta-parameters are defined in later stages. We specify stages and their order according to the recommendations in Haskell Wiki [2013], e.g., using earlier stages for meta-parameters that are expected to change less frequently than other meta-parameters.

It is easy to see that $+\!\!+^{<T\,|\,D\,|\,d>}$ is a combine operator of type $\mathtt{CO}^{<id\,|\,T\,|\,D\,|\,d>}$ for any particular choice of meta-parameters $T \in \mathtt{TYPE}$, $D \in \mathbb{N}$, and $d \in [1, D]_{\mathbb{N}}$.

Example 2 (Point-Wise Combination). We define *point-wise combination*, according to a binary function $\oplus : T \times T \to T$ (e.g. addition), as function $\overrightarrow{\bullet}$ of type

$$\overrightarrow{\bullet}^{<T \in \mathtt{TYPE}\,|\,D \in \mathbb{N}\,|\,d \in [1,D]_{\mathbb{N}}\,|\,(I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D) \in \mathtt{MDA\text{-}IDX\text{-}SETs}^{D-1},(P,Q) \in \mathtt{MDA\text{-}IDX\text{-}SETs} \dot{\times} \mathtt{MDA\text{-}IDX\text{-}SETs}>} :$$

$$\underbrace{T \times T \to T}_{\oplus} \;\to\; \underbrace{T[I_1, \ldots, \underbrace{0_f(P)}_{\uparrow d}, \ldots, I_D] \times T[I_1, \ldots, \underbrace{0_f(Q)}_{\uparrow d}, \ldots, I_D] \to T[I_1, \ldots, \underbrace{0_f(P \uplus Q)}_{\uparrow d}, \ldots, I_D]}_{\text{point-wise combination (according to } \oplus)}$$

where $0_f : \mathtt{MDA\text{-}IDX\text{-}SETs} \to \mathtt{MDA\text{-}IDX\text{-}SETs}$, $I \mapsto \{0\}$ is the constant MDA index set function that maps any index set I to the index set containing MDA index 0 only. The function is computed as:

$$\overrightarrow{\bullet}^{<T\,|\,D\,|\,d\,|\,(I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D),(P,Q)>}(\oplus)(\mathfrak{a}_1, \mathfrak{a}_2)[i_1, \ldots, \underset{\uparrow d}{0}, \ldots, i_D] :=$$
$$\mathfrak{a}_1[i_1, \ldots, \underset{\uparrow d}{0}, \ldots, i_D] \oplus \mathfrak{a}_2[i_1, \ldots, \underset{\uparrow d}{0}, \ldots, i_D]$$

We often write $\oplus$ only, instead of $\overrightarrow{\bullet}(\oplus)$, and we usually use an infix notation for $\oplus$.

Function $\overrightarrow{\bullet}^{<T\,|\,D\,|\,d>}(\oplus)$ (meaning: $\overrightarrow{\bullet}$ is partially applied to ordinary function parameter $\oplus$ and thus still generic in parameters $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D)$ and (P, Q) – formal details provided in the Appendix, Definition 22) is a combine operator of type $\mathtt{CO}^{<0_f\,|\,T\,|\,D\,|\,d>}$ for any binary operator $\oplus : T \times T \to T$.

Multi-Dimensional Homomorphisms

Now that we have defined MDAs (Definition 1) and combine operators (Definition 2), we can define *Multi-Dimensional Homomorphisms (MDH)*. Intuitively, a function h operating on MDAs is an MDH iff we can apply the function independently to parts of its input MDA and combine the obtained intermediate results to the final result using combine operators; this can be imagined as a typical divide-and-conquer pattern. Compared to classical approaches, e.g., *list homomorphisms* [Bird 1989; COLE 1995; Gorlatch 1999], a major characteristic of MDH functions is that they allow (de/re)-composing computations in multiple dimensions (e.g., in Figure 1, in the concatenation as well as point-wise addition dimensions), rather than being limited to a particular dimension only (e.g., only the concatenation dimension or only point-wise addition dimension, respectively). We will see later in this paper that a multi-dimensional (de/re)-composition approach is essential to efficiently exploit the hardware of modern architectures which require fine-grained cache blocking and parallelization strategies to achieve their full performance potential.

Figure 9 illustrates the MDH property informally on a simple, two-dimensional input MDA. In the left part of the figure, we split the input MDA in dimension 1 (i.e., horizontally) into two parts $\mathfrak{a}_1$

and a_2, apply MDH function h independently to each part, and combine the obtained intermediate results to the final result using the MDH function h's combine operator $\circledast_1$. Similarly, in the right part of Figure 9, we split the input MDA in dimension 2 (i.e., vertically) into parts and combine the results via MDH function h's second combine operator $\circledast_2$.

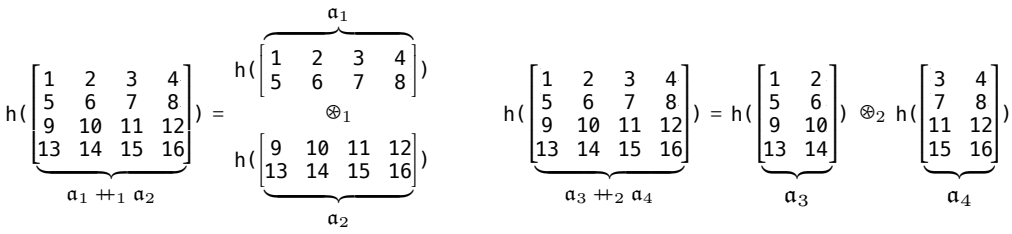


Fig. 9. MDH property illustrated on a two-dimensional example computation

Figure 10 shows an artificial example in which we apply the MDH property (illustrated in Figure 9) recursively. We refer in Figure 10 to the part above the horizontal dashed lines as *de-composition phase* and to the part below dashed lines as *re-composition* phase.

Definition 3 (Multi-Dimensional Homomorphism)**.** Let $T^{\mathsf{INP}}, T^{\mathsf{OUT}} \in \mathsf{TYPE}$ be two arbitrary scalar types, $D \in \mathbb{N}$ a natural number, and $\overset{1}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}}, \ldots, \overset{D}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}} : \mathsf{MDA\text{-}IDX\text{-}SETs} \to \mathsf{MDA\text{-}IDX\text{-}SETs}$ functions on MDA index sets. Let further $+\!\!+_d := +\!\!+^{<T^{\mathsf{INP}} \,|\, D \,|\, d>} \in \mathsf{CO}^{<id \,|\, T^{\mathsf{INP}} \,|\, D \,|\, d>}$ be concatenation (Definition 1) in dimension $d \in [1, D]_{\mathbb{N}}$ on D-dimensional MDAs that have scalar type T^{INP}.

A function

$$h^{<I_1,\ldots,I_D \in \mathsf{MDA\text{-}IDX\text{-}SETs}>} : T^{\mathsf{INP}}[\, I_1, \ldots, I_D \,] \to T^{\mathsf{OUT}}[\, \overset{1}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}}(I_1), \ldots, \overset{D}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}}(I_D) \,]$$

is a *Multi-Dimensional Homomorphism (MDH)* that has *input scalar type* T^{INP}, *output scalar type* T^{OUT}, *dimensionality* D, and *index set functions* $\overset{1}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}}, \ldots, \overset{D}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}}$, iff for each $d \in [1, D]_{\mathbb{N}}$, there exists a combine operator $\circledast_d \in \mathsf{CO}^{<\overset{d}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}} \,|\, T^{\mathsf{OUT}} \,|\, D \,|\, d>}$ (Definition 2), such that for any concatenated input MDA $a_1 +\!\!+_d a_2$ in dimension d, the *homomorphic property* is satisfied:

$$h(\, a_1 +\!\!+_d a_2 \,) \;=\; h(a_1) \circledast_d h(a_2)$$

We denote the type of MDHs concisely as $\mathsf{MDH}^{<T^{\mathsf{INP}}, T^{\mathsf{OUT}} \,|\, D \,|\, (\overset{d}{\Rightarrow}_{\mathsf{MDA}}^{\mathsf{MDA}})_{d \in [1,D]_{\mathbb{N}}}>}$.

MDHs are defined such that applying them to a concatenated MDA in dimension d can be computed by applying the MDH h independently to the MDA's parts a_1 and a_2 and combining the results afterwards by using its combine operator $\circledast_d$, as also informally discussed above. Note that per definition of MDHs, their combine operators are associative and commutative (which follows from the associativity and commutativity of $+\!\!+_d$). Note further that for simplicity, Definition 3 is specialized to MDHs whose input algebraic structure relies on concatenation, as such kinds of MDHs already cover the currently practice-relevant data-parallel computations (as we will see later). We provide a generalized definition of MDHs in Section B.2 of our Appendix, for the algebraically interested reader.

Example 3 (Function Mapping)**.** A simple example MDH is *function mapping* [González-Vélez and Leyton 2010], computed by higher-order function $\mathsf{map}(f)(a)$, which applies a user-defined scalar function $f : T^{\mathsf{INP}} \to T^{\mathsf{OUT}}$ to each element within a D-dimensional MDA a. Function $\mathsf{map}(f)$

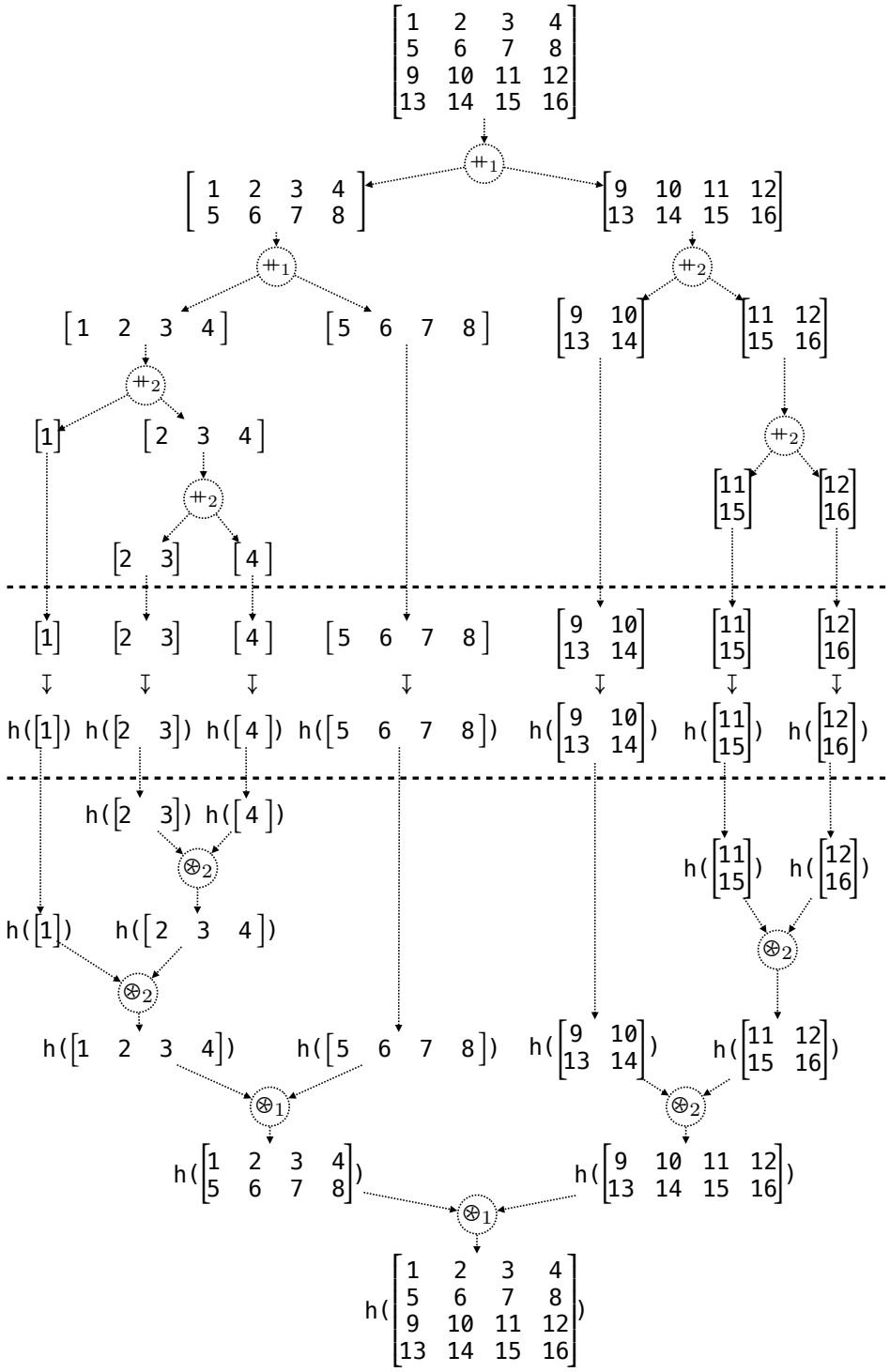


Fig. 10. MDH property recursively applied to a two-dimensional example computation

is an MDH of type $\texttt{MDH}^{<T^{\text{INP}},T^{\text{OUT}}\,|\,D\,|\,id,\ldots,id>}$ whose combine operators are concatenation $+\!\!+$ in all of its D dimensions (Example 1). Function *id* is the index set function of $+\!\!+$ (see Example 1) and consequently also of MDH $\texttt{map}(f)$. Formal details and definitions for *function mapping* can be found in the Appendix, Section B.3.

Example 4 (Reduction). Another MDH function is *reduction* [González-Vélez and Leyton 2010], implemented as higher-order function $\texttt{red}(\oplus)(\mathfrak{a})$, which combines all elements within a D-dimensional MDA $\mathfrak{a}$ using a user-defined binary function $\oplus : T \times T \to T$. Reduction's MDH type is $\texttt{MDH}^{<T,T\,|\,D\,|\,0_f,\ldots,0_f>}$, and its combine operators are point-wise combination $\vec{\bullet}(\oplus)$ in all dimensions (Example 2) which have 0_f index set function. Formal details and definitions for *reduction* can be found in the Appendix, Section B.3.

We show how Examples 3 and 4 (and particularly also more advanced examples) are expressed in our high-level representation in Section 2.5, based on higher-order functions `md_hom`, `inp_view`, and `out_view` (Figure 5) which we introduce in the following.

Higher-Order Function `md_hom`

We define higher-order function `md_hom` which conveniently expresses MDH functions in a uniform and structured manner. For this, we exploit that any MDH function is uniquely determined by its combine operators and its behavior on singleton MDAs, as informally illustrated in the following figure:

$$
\texttt{h}\left(\begin{bmatrix} 1 & 2 & 3 & 4 \\ 5 & 6 & 7 & 8 \\ 9 & 10 & 11 & 12 \\ 13 & 14 & 15 & 16 \end{bmatrix}\right) =
\overset{\circledast_2\;\longrightarrow}{\left.\begin{array}{cccc}
\texttt{h}([1]) & \texttt{h}([2]) & \texttt{h}([3]) & \texttt{h}([4]) \\
\texttt{h}([5]) & \texttt{h}([6]) & \texttt{h}([7]) & \texttt{h}([8]) \\
\texttt{h}([9]) & \texttt{h}([10]) & \texttt{h}([11]) & \texttt{h}([12]) \\
\texttt{h}([13]) & \texttt{h}([14]) & \texttt{h}([15]) & \texttt{h}([16])
\end{array}\right\downarrow}{\scriptstyle\circledast_1}
=
\overset{\circledast_2\;\longrightarrow}{\left.\begin{array}{cccc}
\texttt{f(1)} & \texttt{f(2)} & \texttt{f(3)} & \texttt{f(4)} \\
\texttt{f(5)} & \texttt{f(6)} & \texttt{f(7)} & \texttt{f(8)} \\
\texttt{f(9)} & \texttt{f(10)} & \texttt{f(11)} & \texttt{f(12)} \\
\texttt{f(13)} & \texttt{f(14)} & \texttt{f(15)} & \texttt{f(16)}
\end{array}\right\downarrow}{\scriptstyle\circledast_1}
$$

Here, f is the function on scalar values that behaves the same as h when restricted to singleton MDAs: $f(\mathfrak{a}[i_1,\ldots,i_D]) := h(a)$, for any MDA $\mathfrak{a} \in T[\{i_1\},\ldots,\{i_D\}]$ consisting of only one element accessed by (arbitrary) indices $i_1,\ldots,i_D \in \mathbb{N}_0$. For singleton MDAs, we usually use f instead of h, because f can be defined more conveniently by the user as h (which needs to handle MDAs of arbitrary sizes, and not only singleton MDAs as f). Also, since f takes as input a scalar value (rather than a singleton MDA as h), the type of f also becomes simpler, thereby also further simplifying the definition of scalar functions for the user.

We now formally introduce function `md_hom` which uniformly expresses any MDH function, by using only the MDH's behavior f on scalar values and its combine operators.

Definition 4 (Higher-Order Function `md_hom`)**.** The higher-order function `md_hom` is of type

$$
\texttt{md\_hom}^{<T^{\text{INP}},T^{\text{OUT}}\in\texttt{TYPE}\;|\;D\in\mathbb{N}\;|\;(\overset{d}{\Rightarrow}{}^{\texttt{MDA}}_{\texttt{MDA}}:\texttt{MDA-IDX-SETs}\to\texttt{MDA-IDX-SETs})_{d\in[1,D]_{\mathbb{N}}}>} :
$$

$$
\underbrace{\texttt{SF}^{<T^{\text{INP}},T^{\text{OUT}}>}}_{f} \times \underbrace{\left(\texttt{CO}^{<\overset{1}{\Rightarrow}{}^{\texttt{MDA}}_{\texttt{MDA}}\,|\,T^{\text{OUT}}\,|\,D\,|\,1>} \times \ldots \times \texttt{CO}^{<\overset{D}{\Rightarrow}{}^{\texttt{MDA}}_{\texttt{MDA}}\,|\,T^{\text{OUT}}\,|\,D\,|\,D>}\right)}_{\circledast_1\,,\,\ldots\,,\,\circledast_D}
\to_p \underbrace{\texttt{MDH}^{<T^{\text{INP}},T^{\text{OUT}}\,|\,D\,|\,(\overset{d}{\Rightarrow}{}^{\texttt{MDA}}_{\texttt{MDA}})_{d\in[1,D]_{\mathbb{N}}}>}}_{\texttt{md\_hom}(\,f\,,\,(\circledast_1,\ldots,\circledast_D)\,)}
$$

where $\text{SF}^{<T^{\text{INP}},T^{\text{OUT}}>}$ denotes scalar functions of type $T^{\text{INP}} \to T^{\text{OUT}}$. Function `md_hom` is partial (indicated by $\to_p$ instead of $\to$), which we motivate after this definition. The function takes as input a

scalar function f and a tuple of D-many combine operators $(\otimes_1, \ldots, \otimes_D)$, and it yields a function $\texttt{md\_hom}(\ f\ ,\ (\otimes_1, \ldots, \otimes_D)\ )$ which is defined as

$$\texttt{md\_hom}(\ f\ ,\ (\otimes_1, \ldots, \otimes_D)\ )(\ \mathfrak{a}\ ) \coloneqq \underset{i_1 \in I_1}{\otimes_1} \ldots \underset{i_D \in I_D}{\otimes_D} \vec{f}(\ \mathfrak{a}|_{\{i_1\} \times \ldots \times \{i_D\}}\ )$$

The combine operators' underset notation denotes straightforward iteration (explained formally in the Appendix, Notation 5), and the MDA $\mathfrak{a}|_{\{i_1\} \times \ldots \times \{i_D\}}$ is the restriction of $\mathfrak{a}$ to the MDA containing the single element accessed via MDA indices $(i_1, \ldots, i_D)$. Function $\vec{f}$ behaves like scalar function f, but operates on singleton MDAs (rather than scalars): the function is of type

$$\vec{f}^{<i_1,\ldots,i_D \in \mathbb{N}_0>} : T^{\texttt{INP}}[\ \{i_1\}, \ldots, \{i_D\}\ ] \to T^{\texttt{OUT}}[\ \overset{1}{\Rightarrow}^{\texttt{MDA}}_{\texttt{MDA}}(\ \{i_1\}\ ), \ldots, \overset{D}{\Rightarrow}^{\texttt{MDA}}_{\texttt{MDA}}(\{i_D\}\ )\ ]$$

and defined as

$$\vec{f}(x)[\ j_1, \ldots, j_D\ ] \coloneqq f(\ x[\ i_1, \ldots, i_D\ ]\ )^{8}$$

For $\texttt{md\_hom}(\ f, (\otimes_1, \ldots, \otimes_D)\ )$, we require per definition the homomorphic property (Definition 3), i.e., for each $d \in [1, D]_{\mathbb{N}}$, it must hold:

$$\texttt{md\_hom}(\ f\ ,\ (\otimes_1, \ldots, \otimes_D)\ )(\ \mathfrak{a}_1 +\!\!+_d\ \mathfrak{a}_2\ ) =$$
$$\texttt{md\_hom}(\ f\ ,\ (\otimes_1, \ldots, \otimes_D)\ )(\ \mathfrak{a}_1\ )\ \ \otimes_d\ \ \texttt{md\_hom}(\ f\ ,\ (\otimes_1, \ldots, \otimes_D)\ )(\ \mathfrak{a}_2\ )$$

Using Definition 4, we express any MDH function uniformly via higher-order function md_hom using only the MDH's behavior f on scalar values[9] and its combine operators $\otimes_1, \ldots, \otimes_D$. The other direction also holds: each function expressed via md_hom is an MDH function, because we require the homomorphic property for md_hom.

Note that we can potentially allow in Definition 4 the case $D = 0$ in which we would define the md_hom instance equal to the scalar function f:

$$\texttt{md\_hom}(\ f\ ,\ (\ )\ ) \coloneqq f$$

Note further that function md_hom is defined as partial function, because the homomorphic property is not met for all potential combinations of combine operators, e.g., $\otimes_1 = +$ (point-wise addition) and $\otimes_2 = *$ (point-wise multiplication). However, in many real-world examples, an MDH's combine operators are a mix of concatenations and point-wise combinations according to the same binary function. The following lemma proves that any instance of the md_hom higher-order function for such a mix of combine operators is a well-defined MDH function.

Lemma 1. Let $\oplus : T \to T$ be an arbitrary but fixed associative and commutative binary function on scalar type $T \in \texttt{TYPE}$. Let further $\otimes_1, \ldots, \otimes_D$ be combine operators of which any is either concatenation (Example 1) or point-wise combination according to binary function $\oplus$ (Example 2).

It holds that $\texttt{md\_hom}(\ f, (\otimes_1, \ldots, \otimes_D)\ )$ is well defined.

Proof. See Appendix, Section B.5. □

MDHs use as input and output uniformly an MDA. We introduce higher-order function inp_view to prepare domain-specific inputs (e.g., a matrix and a vector for matrix-vector multiplication) as an MDA, and we use function out_view to transform the output MDA back to the domain-specific data requirements (like storing it as a transposed matrix in the case of matrix multiplication, or

[8] We assume in this work that MDH functions when used on singleton MDAs return a singleton MDA, as such MDHs already cover all real-world cases we currently are aware of.

[9] For simplicity, we ignore that the scalar functions of some MDHs (such as Mandelbrot) also take as input MDA indices, which requires slight, straightforward extension of function md_hom, as outlined in the Appendix, Section B.4.

splitting it into multiple outputs as we will see later with examples). We introduce both higher-order functions in the following.

2.3 View Functions

We start, in Section 2.3.1, by formally introducing *Buffers (BUF)* and *Index Functions* – both concepts are central building blocks in our definition of higher-order functions `inp_view` and `out_view`. In our approach, we use BUFs to represent domain-specific input and output data (scalars, vectors, matrices, etc), and *index functions* are used by the user to conveniently instantiate higher-order functions `inp_view` and `out_view` (e.g., index function $(i,k) \mapsto (i,k)$ and $(i,k) \mapsto (k)$ used in Figure 6 to instantiate `inp_view`, and $(i,k) \mapsto (i)$ used for `out_view`).

Sections 2.3.2 and 2.3.3 introduce *input views* and *output views* which are central concepts in our approach. We define *input views* as arbitrary functions that map a collection of BUFs to an MDA (Figure 5); higher-order function `inp_view` is then defined to conveniently compute an important class of input view functions relevant in real-world applications. Correspondingly, Section 2.3.3 defines *output views* as functions that transform an MDA to a collection of BUFs, and higher-order function `out_view` is defined to conveniently compute important output views.

Finally, we discuss in Section 2.3.4 the relationship between higher-order function `inp_view` and `out_view`: we prove that both functions are inversely related to each other, allowing arbitrarily switching between our internal MDA and the domain-specific BUF representation (as required for our code generation discussed later).

2.3.1 *Preparation.*

We formally introduce *Buffers (BUF)* and *Index Functions* in the following.

Definition 5 (Buffer)**.** Let $T \in \texttt{TYPE}$ be an arbitrary scalar type, $D \in \mathbb{N}_0$ a natural number[10], and $N := (N_1, \ldots, N_D) \in \mathbb{N}^D$ a tuple of natural numbers.

A *Buffer (BUF)* $\mathfrak{b}$ that has *dimensionality* D, *size* N, and *scalar type* T is a function with the following signature:

$$\mathfrak{b} : [0, N_1)_{\mathbb{N}_0} \times \ldots \times [0, N_D)_{\mathbb{N}_0} \rightarrow T \cup \{\bot\}$$

Here, we use $\bot$ to denote the *undefined value*. We refer to $[0, N_1)_{\mathbb{N}_0} \times \ldots \times [0, N_D)_{\mathbb{N}_0} \rightarrow T \cup \{\bot\}$ as the *type* of BUF $\mathfrak{b}$, which we also denote as $T^{N_1 \times \ldots \times N_D}$, and we refer to the set $\texttt{BUF-IDX-SETs} := \{ [0, N)_{\mathbb{N}_0} \mid N \in \mathbb{N} \}$ as *BUF index sets*. Analogously to Notation 1, we write $\mathfrak{b}[\, i_1, \ldots, i_D \,]$ instead of $\mathfrak{b}(i_1, \ldots, i_D)$ to avoid a too heavy usage of parentheses.

In contrast to MDAs, a BUF always operates on a contiguous range of natural numbers starting from 0, and a BUF may contain undefined values. These two differences allow us straightforwardly transforming BUFs to data structures provided by low-level programming languages (e.g., *C arrays* as used in OpenMP, CUDA, and OpenCL). Note that in our generated program code (discussed later in Section 3), we implement MDAs as straightforward aliases that access BUFs, on top of BUFs, so that we do not need to transform MDAs to low-level data structures and/or store them otherwise physically in memory.

Definition 6 (Index Function)**.** Let $D \in \mathbb{N}$ be a natural number (representing an MDA's dimensionality) and $D_b \in \mathbb{N}_0$ (representing a BUF's dimensionality).

An *index function* $\mathfrak{idx}$ from D-dimensional MDA indices to D_b-dimensional BUF indices is any meta-function of type

$$\mathfrak{idx}^{<I_1^{\texttt{MDA}}, \ldots, I_D^{\texttt{MDA}} \in \texttt{MDA-IDX-SETs}^D>} : I_1^{\texttt{MDA}} \times \ldots \times I_D^{\texttt{MDA}} \rightarrow I_1^{\texttt{BUF}} \times \ldots \times I_{D_b}^{\texttt{BUF}}$$

[10] We use the case $D = 0$ to represent scalar values, as we discuss later.

for $(I_1^{\text{BUF}}, \ldots, I_{D_b}^{\text{BUF}}) := \Rightarrow_{\text{BUF}}^{\text{MDA}}(I_1^{\text{MDA}}, \ldots, I_D^{\text{MDA}})$ where $\Rightarrow_{\text{BUF}}^{\text{MDA}} : \texttt{MDA-IDX-SETs}^{D} \to \texttt{BUF-IDX-SETs}^{D_b}$ is an arbitrary but fixed function that maps D-many MDA index sets to D_b-many BUF index sets. We denote the type of index functions as $\texttt{MDA-IDX-to-BUF-IDX}^{<D, D_b \mid \Rightarrow_{\text{BUF}}^{\text{MDA}}>}$.

In words: Index functions have to be capable of operating on any potential MDA index set. This generality will be required later for using index functions also on parts of MDAs whose index sets are subsets of the original MDA's index sets.

We will use index functions to access BUFs. For example, in the case of `MatVec` (Figure 1), we access its input matrix using index function $(i, k) \mapsto (i, k)$ which is of type

$$\texttt{MDA-IDX-to-BUF-IDX}^{<D:=2, D_b:=2 \mid \Rightarrow_{\text{BUF}}^{\text{MDA}}(I_1^{\text{MDA}}, I_2^{\text{MDA}}) := [0, \max(I_1^{\text{MDA}})]_{\mathbb{N}_0}, [0, \max(I_2^{\text{MDA}})]_{\mathbb{N}_0}>}$$

and we use index function $(i, k) \mapsto (k)$ to access `MatVec`'s input vector, which is of type

$$\texttt{MDA-IDX-to-BUF-IDX}^{<D:=2, D_b:=1 \mid \Rightarrow_{\text{BUF}}^{\text{MDA}}(I_1^{\text{MDA}}, I_2^{\text{MDA}}) := [0, \max(I_2^{\text{MDA}})]_{\mathbb{N}_0}>}$$

Further examples of index function, e.g., for stencil computation `Jacobi1D`, are presented in the Appendix, Section B.6, for the interested reader.

2.3.2 Input Views. We define *input views* as any function that compute an MDA from a collection of user-defined BUFs. For example, in the case of `MatVec`, its input view takes as input two BUFs – a matrix and a vector – and it yields a two-dimensional MDA containing pairs of elements taken from the matrix and vector (illustrated in Figure 1). In contrast, the input view of `Jacobi1D` takes as input a single BUF (vector) only, and it computes an MDA containing triples of BUF elements (Figure 2).

Definition 7 (Input View)**.** An *input view* from B-many BUFs, $B \in \mathbb{N}$, of arbitrary but fixed types $T_b^{N_1^b \times \ldots \times N_{D_b}^b}$, $b \in [1, B]_{\mathbb{N}}$, to an MDA of arbitrary but fixed type $T[I_1, \ldots, I_D]$ is any function $\mathfrak{iv}$ of type:

$$\mathfrak{iv} : \underbrace{\bigtimes_{b=1}^{B} T_b^{N_1^b \times \ldots \times N_{D_b}^b}}_{\text{BUFs}} \to_p \underbrace{T[\, I_1, \ldots, I_D \,]}_{\text{MDA}}$$

We denote the type of $\mathfrak{iv}$ as $\texttt{IV}^{<B \mid (D_b)_{b \in [1,B]_{\mathbb{N}}} \mid (N_1^b, \ldots, N_{D_b}^b)_{b \in [1,B]_{\mathbb{N}}} \mid (T_b)_{b \in [1,B]_{\mathbb{N}}}}_{\text{BUFs' Meta-Parameters}} \mid \overbrace{D \mid I_1, \ldots, I_D \mid T}^{\text{MDA's Meta-Parameters}} >$.

Example 5 (Input View – `MatVec`)**.** The input view of `MatVec` on a 1024×512 matrix and 512-sized vector (sizes are chosen arbitrarily), both of integers $\mathbb{Z}$, is of type

$$\texttt{IV}^{\overbrace{<B=2 \mid D_1=2, D_2=1 \mid (N_1^1=1024, N_2^1=512), (N_1^2=512) \mid T_1=\mathbb{Z}, T_2=\mathbb{Z}}^{\text{BUFs' meta-parameters}} \mid \overbrace{D=2 \mid I_1=[0,1024)_{\mathbb{N}_0}, I_2=[0,512)_{\mathbb{N}_0} \mid T=\mathbb{Z}\times\mathbb{Z}}^{\text{MDA's meta-parameters}}>}$$

and defined as

$$\underbrace{[\, M(i,k) \,]_{i \in [0,1024)_{\mathbb{N}_0}, k \in [0,512)_{\mathbb{N}_0}}}_{\text{Matrix}}, \underbrace{[\, v(k) \,]_{k \in [0,512)_{\mathbb{N}_0}}}_{\text{Vector}} \mapsto \underbrace{[\, M(i,k), v(k) \,]_{i \in [0,1024)_{\mathbb{N}_0}, k \in [0,512)_{\mathbb{N}_0}}}_{\text{MDA}}$$

Here, the BUFs' meta-parameters are as follows: $B = 2$ is the number of BUFs (matrix and vector); $D_1 = 2$ is dimensionality of the matrix and $D_2 = 1$ the vector's dimensionality; $(N_1^1, N_2^1) = (1024, 512)$ is the matrix size and $N_1^2 = 512$ the vector's size; $T_1, T_2 = \mathbb{Z}$ are the scalar types of matrix and vector. The MDA's meta-parameters are: $D = 2$ is the computed MDA's dimensionality; I_1, I_2 are the MDA's index sets; parameter $T = \mathbb{Z} \times \mathbb{Z}$ is MDA's scalar type (pairs of matrix/vector elements – see Figure 1).

Example 6 (Input View – `Jacobi1D`). The input view of `Jacobi1D` on a 512-sized vector of integers is of type

$$\mathtt{IV}^{\overbrace{<B=1 \mid D_1=1 \mid (N_1^1=512) \mid T_1=\mathbb{Z}}^{\text{BUFs' meta-parameters}} \mid \overbrace{D=1 \mid I_1=[0,512-2)_{\mathbb{N}_0} \mid T=\mathbb{Z}\times\mathbb{Z}\times\mathbb{Z}}^{\text{MDA's meta-parameters}}>}$$

and defined as

$$\underbrace{[\,v(i)\,]_{i\in[0,512)_{\mathbb{N}_0}}}_{\text{Vector}} \mapsto \underbrace{[\,v(i+0), v(i+1), v(i+2)\,]_{i\in[0,512-2)_{\mathbb{N}_0}}}_{\text{MDA}}$$

We introduce higher-order function `inp_view` which computes important input views conveniently and in a structured manner from user-defined index functions $(\mathfrak{idx}_{b,a})_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}}$ (Definition 6). Here, $B \in \mathbb{N}$ represents the number of BUFs that the computed input view will take as input, and A_b represents the number of accesses to the b-th BUF required for computing an individual MDA element.

In the case of `MatVec` (Figure 1), we use $B := 2$, as `MatVec` has two input BUFs – a matrix M (the first input of `MatVec` and thus identified by $b = 1$) and a vector v (identified by $b = 2$). For the number of accesses, we use for the matrix $A_1 := 1$, as one element is accessed within the matrix M to compute an individual MDA element – matrix element $M[i,k]$ for computing MDA element at position (i,k); for the vector, we use $A_2 := 1$ – the single element $v[k]$ is accessed. The index functions of `MatVec` are: $\mathfrak{idx}_{1,1}(i,k) := (i,k)$ (used to access the matrix) and $\mathfrak{idx}_{2,1}(i,k) := (k)$ (used for the vector).

In contrast, for `Jacobi1D` (Figure 2), we use $B := 1$ (`Jacobi1D` has one input BUF v), $A_1 := 3$ (the BUF is accessed three times to compute an individual MDA element at arbitrary position i: first access $v[i+0]$, second access $v[i+1]$, and third access $v[i+2]$). The index functions of `Jacobi1D` are: $\mathfrak{idx}_{1,1}(i) := (i+0)$, $\mathfrak{idx}_{1,2}(i) := (i+1)$, and $\mathfrak{idx}_{1,3}(i) := (i+2)$.

More generally, higher-order function `inp_view` uses the index functions $\mathfrak{idx}_{b,a}$ to compute an input view that maps BUFs $\mathfrak{b}_1, \ldots, \mathfrak{b}_B$ to an MDA $\mathfrak{a}$ that contains at position $i_1, \ldots, i_D$ the following element:

$$\mathfrak{a}[i_1,\ldots,i_D] := \underbrace{\Big(\underbrace{\big(\underbrace{\mathfrak{b}_1[\,\mathfrak{idx}_{1,1}(i_1,\ldots,i_D)\,]}_{a=1} \in T_1, \ldots, \underbrace{\mathfrak{b}_1[\,\mathfrak{idx}_{1,A_1}(i_1,\ldots,i_D)\,]}_{a=A_1} \in T_1\big)}_{b=1}, \vdots, \underbrace{\big(\underbrace{\mathfrak{b}_B[\,\mathfrak{idx}_{B,1}(i_1,\ldots,i_D)\,]}_{a=1} \in T_B, \ldots, \underbrace{\mathfrak{b}_B[\,\mathfrak{idx}_{B,A_B}(i_1,\ldots,i_D)\,]}_{a=A_B} \in T_B\big)}_{b=B}\Big)}$$

The element consists of B-many tuples – one per BUF – and each such tuple contains A_b-many elements – one element per access to the b-th BUF. For `MatVec`, the element is of the form

$$\mathfrak{a}[i_1,i_2] := \Big(\underbrace{\big(\underbrace{\mathfrak{b}_1[\,\mathfrak{idx}_{1,1}(i_1,i_2) := (i_1,i_2)\,]}_{a=1} \in T_1\big)}_{b=1}, \underbrace{\big(\underbrace{\mathfrak{b}_2[\,\mathfrak{idx}_{2,1}(i_1,i_2) := (i_2)\,]}_{a=1} \in T_2\big)}_{b=2}\Big)$$

and for Jacobi1D, the element is

$$\mathfrak{a}[i_1] := \underbrace{\Big(\underbrace{\mathfrak{b}_1[\,\mathfrak{idx}_{1,1}(i_1) := (i_1+0)\,] \in T_1}_{a=1}, \underbrace{\mathfrak{b}_1[\,\mathfrak{idx}_{1,2}(i_1) := (i_1+1)\,] \in T_1}_{a=2}, \underbrace{\mathfrak{b}_1[\,\mathfrak{idx}_{1,3}(i_1) := (i_1+2)\,] \in T_1}_{a=3}\Big)}_{b=1}$$

In the following, we introduce higher-order function inp_view which computes important input views conveniently and in a uniform, structured manner. Function inp_view takes as input a collection of index functions (Definition 6), and it uses these index functions to compute a corresponding input view (Definition 7), as follows.

Figures 11 and 12 use the examples MatVec and Jacobi1D to informally illustrate how function inp_view uses index functions to compute input views. In the two figures, we use domain-specific identifiers for better clarity: in the case of MatVec, we use for BUFs identifiers M and v instead of $\mathfrak{b}_1$ and $\mathfrak{b}_2$, as well as identifiers i and j instead of i_1 and i_2 for index variables; for Jacobi1D, we use identifier v instead of $\mathfrak{b}_1$, and i instead of i_1.

We now formally define higher-order function inp_view. For high flexibility and formal correctness, function inp_view relies on a type that involves many meta-parameters. The high number of meta-parameters, and the resulting complex type of function inp_view, might appear daunting to the user. However, Notation 2 confirms that despite the complex type of function inp_view, the function can be conveniently used by the user (as also illustrated in Figure 6), because meta-parameters can be automatically deduced from inp_view's input parameters.

Definition 8 (Higher-Order Function inp_view)**.** Function inp_view is of type

$$\texttt{inp\_view}^{<\ \underbrace{B\in\mathbb{N}}_{\text{Number BUFs}}\ |\ \underbrace{A_1,\ldots,A_B\in\mathbb{N}}_{\text{Number BUFs' Accesses}}\ |\ \underbrace{D_1,\ldots,D_{B}\in\mathbb{N}_0}_{\text{BUFs' Dimensionalities}}\ |\ \underbrace{D\in\mathbb{N}}_{\text{MDA Dimensionality}}\ |\ \underbrace{(\Rightarrow_{\text{BUF}}^{\text{MDA}\,b,a}:\texttt{MDA-IDX-SETs}^{D}\to\texttt{BUF-IDX-SETs}^{D_b})_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}}}_{\text{Index Set Functions (MDA indices to BUF indices)}}\ >:$$

$$\underbrace{\underbrace{\underbrace{\underbrace{B}_{b=1}\times\underbrace{A_b}_{a=1}}_{\text{Buffer Access}}\ \texttt{MDA-IDX-to-BUF-IDX}^{<D,D_b\,|\,\Rightarrow_{\text{BUF}}^{\text{MDA}\,b,a}>}}_{\text{Index Function: }\mathfrak{idx}_{b,a}}}_{\text{Index Functions: }\mathfrak{idx}_{1,1},\ldots,\mathfrak{idx}_{B,A_B}} \to \underbrace{\texttt{IV}^{<\overbrace{B\,|\,D_1,\ldots,D_B}^{\text{BUFs' Meta-Parameters}}\,|\,\to\,|\,T_1,\ldots,T_B\in\texttt{TYPE}\,|\ \underbrace{D\,|\,I_1,\ldots,I_D\in\texttt{MDA-IDX-SETs}\,|\,\to}_{\text{MDA's Meta-Parameters}}><\underbrace{N_1^1,\ldots,N_{D_B}^B}_{\text{Postponed Parameters}}\,|\,T>}}_{\text{Input View: }\mathfrak{iv}}$$

for $N_d^b := 1 + \max(\ \bigcup_{a\in[1,A_b]_{\mathbb{N}}} \Rightarrow_{\text{BUF}}^{\text{MDA}\,b,a}(I_1,\ldots,I_D)\ )$ and $T := \times_{b=1}^{B} \times_{a=1}^{A_b} T_b$, and it is defined as:

$$\underbrace{(\mathfrak{idx}_{b,a})_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}}}_{\text{Index Functions}} \mapsto \underbrace{\underbrace{(\,\mathfrak{b}_1,\ldots,\mathfrak{b}_B\,)}_{\text{BUFs}} \overset{\mathfrak{iv}}{\mapsto} \underbrace{\mathfrak{a}}_{\text{MDA}}}_{\text{Input View}}$$

for

$$\mathfrak{a}[i_1,\ldots,i_D] := (\,\mathfrak{a}_{b,a}[i_1,\ldots,i_D]\,)_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}}$$

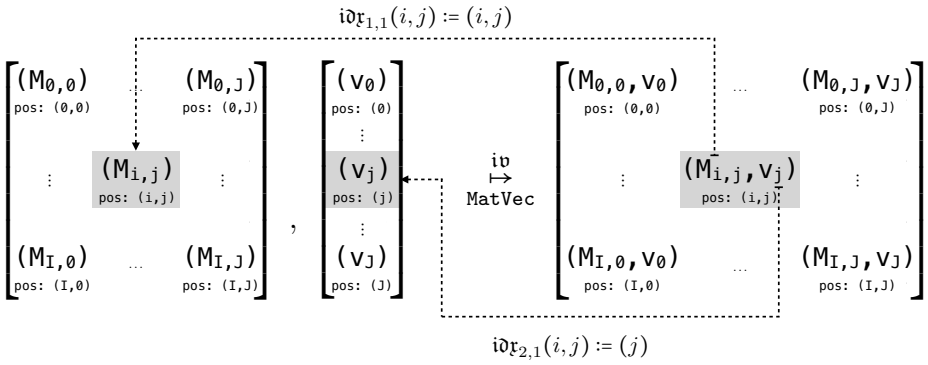


Fig. 11. Input view illustrated using the example MatVec

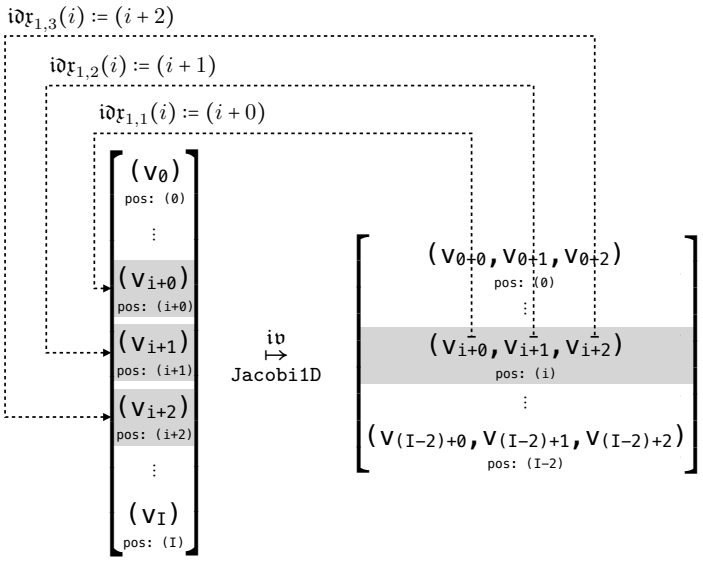


Fig. 12. Input view illustrated using the example Jacobi1D

and

$$\mathfrak{a}_{b,a}[i_1,\ldots,i_D] \;:=\; \mathfrak{b}_b[\;\mathfrak{idx}_{b,a}(i_1,\ldots,i_D)\;]$$

Higher-order function `inp_view` takes as input a collection of index functions that are of types `MDA-IDX-to-BUF-IDX` (Definition 6), and it computes an input view of type `IV` (Definition 7) based on the index functions, as illustrated in Figures 11 and 12.

We use for type `MDA-IDX-to-BUF-IDX` as concrete meta-parameter values (listed in angle brackets) straightforwardly the values of meta-parameters passed to function `inp_view`. Similarly, for type `IV`'s meta-parameters B, $D_1,\ldots,D_B$, and D, we use again straightforwardly the particular meta-parameter values of function `inp_view`.

To be able using the computed input view on arbitrarily typed input buffers and letting the input view compute MDAs that have arbitrary index sets, we keep `IV`'s meta-parameters $T_1,\ldots,T_B$ (scalar types of the computed view's input buffers) and $I_1,\ldots,I_D$ (index sets of the view's returned MDA) flexible. Being flexible in the BUFs' scalar types and MDA's index sets is important for convenience – for example, in the case of `MatVec`, this flexibility allows using the computed input view generically for matrices and vectors that have arbitrary scalar types (e.g., either `int` or `float`) and sizes (I,J) (matrix) and J (vector), for arbitrary $I,J \in \mathbb{N}$, without needing to re-compute a new input view every time again when BUFs' scalar types and/or sizes change.

We automatically compute the sizes N_d^b of BUFs in `IV`'s meta-parameter list (e.g., in the case of `MatVec`, the size of the input matrix (I,J) and vector size J), according to the formula in Definition 8, based on the flexible MDA's index sets (e.g., sets $[0,I)_{\mathbb{N}_0}$ and $[0,J)_{\mathbb{N}_0}$ for `MatVec`). By computing BUF sizes from MDA index sets (rather than requesting the sizes explicitly from the user), we achieve strong error checking: for example, for `MatVec`, we can ensure – already on the type level – that the number of columns of its input matrix and the size of its input vector match. To compute the BUF sizes, we *postpone* via $\rightarrow$ (defined formally in the Appendix, Definition 24) the sizes in `IV`'s meta-parameter list to later meta-parameter stages; this is because the sizes are defined in early stages and thus have no access to the MDA's index sets which are defined in later stages. Our formula in Definition 8 then works as follows: for each BUF b, its size N_d^b has to be well-defined in each of its dimensions d, for all accesses a via the BUF's index functions when used for all indices $I_1,\ldots,I_D$ within the MDA index sets. Here, in the computation of N_d^b, function $\overset{d}{\Rightarrow}^{\mathsf{MDA}\,b,a}_{\mathsf{BUF}}$ computes the d-th component of the D_b-sized output tuple of $\Rightarrow^{\mathsf{MDA}\,b,a}_{\mathsf{BUF}}$ (the computed component is the index set of BUF b in dimension d for the a-th index function used to access the BUF).

We automatically compute also MDA's scalar type T using the formula presented in Definition 8. The formula computes T as a tuple that consists of the BUFs' scalar types, as each MDA element consist of BUF elements (illustrated in Figures 11 and 12). Postponing T in `IV`'s meta-parameter list is done (analogously as for N_d^b), but is actually not required, because the BUFs' scalar types $T_1,\ldots,T_B$ are already defined in earlier meta-parameter stages than T. However, we will see that postponing T is required later in the Definition 10 of higher-order function `out_view`; therefore, we postpone T also in our definition of `inp_view` to increase consistency between our definitions of `inp_view` (Definition 8) and `out_view` (Definition 10).

Note that function `inp_view` is not capable of computing every kind of input view function (Definition 7). For example, `inp_view` cannot be used for computing MDAs that are required for computations on sparse data formats [Hall 2020], because such MDAs need dynamically accessing BUFs. This limitation of `inp_view` can be relaxed by generalizing our index functions toward taking additional, dynamic input arguments, which we consider as future work (as also outlined in Section 8).

Notation 2 (Input Views). Let $\texttt{inp\_view}^{\langle\cdots\rangle}(\ (\ \mathfrak{idx}_{b,a}\ )_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}}\ )$ be a particular instance of higher-order function `inp_view` (meta-parameters omitted via ellipsis for simplicity) for an arbitrary but fixed choice of index functions. Let further $\texttt{ID}_1,\ldots,\texttt{ID}_B \in \Sigma^*$ be arbitrary, user-defined BUF identifiers (e.g., $\texttt{ID}_1$ = "M" and $\texttt{ID}_2$ = "v" in the case of `MatVec`), for an arbitrary, fixed collection of letters $\Sigma = \{A, B, C, \ldots, a, b, c, \ldots, 1, 2, 3, \ldots\}$.

For better readability, we use the following notation for the 2-dimensional structure of index functions taken as input by function `inp_view`, inspired by Lattner et al. [2021]:

$$\texttt{inp\_view}(\ \texttt{ID}_1 : \mathfrak{idx}_{1,1},\ldots,\mathfrak{idx}_{1,A_1}\ \ ,\ldots,\ \ \texttt{ID}_B : \mathfrak{idx}_{B,1},\ldots,\mathfrak{idx}_{B,A_B}\ )$$

We refrain from stating `inp_view`'s meta-parameters in our notation, as the parameters can be automatically deduced from the number and types of index functions.

Example 7. Function `inp_view` is used for `MatVec` and `Jacobi1D` (in Notation 2) as follows:

$$\underline{\texttt{MatVec:}}\qquad \texttt{inp\_view}(\ \underbrace{\underbrace{\texttt{M:}\ \underbrace{(i,k)\mapsto(i,k)}_{a=1}}_{b=1},\ \underbrace{\texttt{v:}\ \underbrace{(i,k)\mapsto(k)}_{a=1}}_{b=2}}\ )$$

$$\underline{\texttt{Jacobi1D:}}\qquad \texttt{inp\_view}(\ \underbrace{\texttt{v:}\ \underbrace{(i)\mapsto(i+0)}_{a=1},\ \underbrace{(i)\mapsto(i+1)}_{a=2},\ \underbrace{(i)\mapsto(i+2)}_{a=3}}_{b=1}\ )$$

2.3.3 Output Views. An *output view* is the counterpart of an input view: in contrast to an input view which maps BUFs to an MDA, an output view maps an MDA to a collection of BUFs. In the following, we define output views, and we introduce higher-order function `out_view` which computes output views in a structured manner, analogously to function `inp_view` for input views.

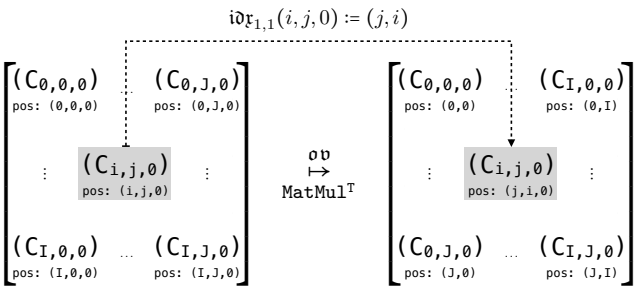


Fig. 13. Output view illustrated using the example *transposed Matrix Multiplication*

Figures 13 and 14 illustrate output views informally using the examples *transposed matrix multiplication* and *double reduction*.

In the case of transposed matrix multiplication, the computed MDA (the computation of matrix multiplication is presented later and not relevant for our following considerations) is stored via an output view as a matrix in a transposed fashion, using index function $(i,j,0)\mapsto(j,i)$. Here,

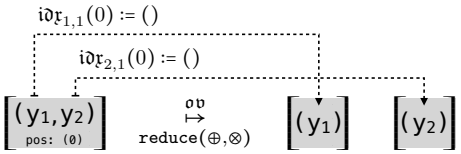


Fig. 14. Output view illustrated using the example *double reduction*

the MDA's third dimension (accessed via index 0) represents the so-called reduction dimension of matrix multiplication, and it contains only one element after the computation, as all elements in this dimension are combined via addition.

For double reduction, we combine the elements within the vector twice – once using operator $\oplus$ (e.g., $\oplus = +$ addition) and once using operator $\otimes$ (e.g, $\otimes = *$ multiplication). The final outcome of double reduction is a singleton MDA containing a pair of two elements that represent the combined vector elements (e.g., the elements' sum and product). We store this MDA via an output view as two individual scalar values, using index functions $(0) \mapsto ()$[11] for both pair elements.

Definition 9 (Output View)**.** An *output view* from an MDA of arbitrary but fixed type $T[I_1, \ldots, I_D]$ to B-many BUFs, $B \in \mathbb{N}$, of arbitrary but fixed types $T_b^{N_1^b \times \ldots \times N_{D_b}^b}$, $b \in [1, B]_{\mathbb{N}}$, is any function $\mathfrak{ov}$ of type:

$$\mathfrak{ov} : \underbrace{T[\, I_1, \ldots, I_D \,]}_{\text{MDA}} \to_p \underbrace{\overset{B}{\underset{b=1}{\times}} T_b^{N_1^b \times \ldots \times N_{D_b}^b}}_{\text{BUFs}}$$

$$\mathsf{OV}^{< \overbrace{D \mid I_1, \ldots, I_D \mid T}^{\text{MDA's Meta-Parameters}} \mid \overbrace{B \mid (D_b)_{b \in [1,B]_{\mathbb{N}}} \mid (N_1^b, \ldots, N_{D_b}^b)_{b \in [1,B]_{\mathbb{N}}} \mid (T_b)_{b \in [1,B]_{\mathbb{N}}}}^{\text{BUFs' Meta-Parameters}} >}$$

We denote the type of $\mathfrak{ov}$ as $\mathsf{OV}^{<D \mid I_1, \ldots, I_D \mid T \mid B \mid (D_b)_{b \in [1,B]_{\mathbb{N}}} \mid (N_1^b, \ldots, N_{D_b}^b)_{b \in [1,B]_{\mathbb{N}}} \mid (T_b)_{b \in [1,B]_{\mathbb{N}}}>}$.

Example 8 (Output View – `MatVec`)**.** The output view of `MatVec` computing a 1024-sized vector (size is chosen arbitrarily), of integers $\mathbb{Z}$, is of type

$$\mathsf{OV}^{\overbrace{<D=2 \mid I_1=[0,1024)_{\mathbb{N}_0}, I_2=\{0\} \mid T=\mathbb{Z}}^{\text{MDA's meta-parameters}} \mid \overbrace{B=1 \mid D_1=1 \mid (N_1^1=1024) \mid T_1=\mathbb{Z}>}^{\text{BUFs' meta-parameters}}}$$

and defined as

$$\underbrace{[\, w(i) \,]_{i \in [0,1024)_{\mathbb{N}_0}, k \in \{0\}}}_{\text{MDA}} \mapsto \underbrace{[\, w(i) \,]_{i \in [0,1024)_{\mathbb{N}_0}}}_{\text{Vector}}$$

Example 9 (Output View – `Jacobi1D`)**.** The output view of `Jacobi1D` computing a $(512-2)$-sized vector of integers is of type

$$\mathsf{OV}^{\overbrace{<D=1 \mid I_1=[0,512-2)_{\mathbb{N}_0} \mid T=\mathbb{Z}}^{\text{MDA's meta-parameters}} \mid \overbrace{B=1 \mid D_1=1 \mid (N_1^1=(512-2)) \mid T_1=\mathbb{Z}>}^{\text{BUFs' meta-parameters}}}$$

and defined as

$$\underbrace{[\, w(i) \,]_{i \in [0,512-2)_{\mathbb{N}_0}, k \in \{0\}}}_{\text{MDA}} \mapsto \underbrace{[\, w(i) \,]_{i \in [0,512-2)_{\mathbb{N}_0}}}_{\text{Vector}}$$

[11] The empty braces denote accessing a scalar value (formal details provided in the Appendix, Section B.7).

We define higher-order function `out_view` formally as follows.

Definition 10 (Higher-Order Function `out_view`). Function `out_view` is of type

$$\texttt{out\_view}^{<} \underbrace{B\in\mathbb{N}}_{\texttt{Number of BUFs}} \mid \underbrace{A_1,\ldots,A_B\in\mathbb{N}}_{\texttt{Number BUFs' Accesses}} \mid \underbrace{D_1,\ldots,D_B\in\mathbb{N}_0}_{\texttt{BUFs' Dimensionalities}} \mid \underbrace{D\in\mathbb{N}}_{\texttt{MDA Dimensionality}} \mid$$

$$\underbrace{(\Rightarrow_{\texttt{BUF}}^{\texttt{MDA}\,b,a}:\texttt{MDA-IDX-SETs}^{D}\to\texttt{BUF-IDX-SETs}^{D_b})_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}}}_{\texttt{Index Set Functions (MDA indices to BUF indices)}}{}^{>}:$$

$$\underbrace{\underbrace{\underbrace{\underbrace{B}_{b=1}}_{\texttt{Buffer}}\times\underbrace{\underbrace{A_b}_{a=1}}_{\texttt{Access}}\ \underbrace{\texttt{MDA-IDX-to-BUF-IDX}^{<D,D_b\mid\Rightarrow_{\texttt{BUF}}^{\texttt{MDA}\,b,a}>}}_{\texttt{Index Function: }\mathfrak{idx}_{b,a}}}_{\texttt{Index Functions: }\mathfrak{idx}_{1,1},\ldots,\mathfrak{idx}_{B,A_B}}\to \texttt{OV}^{\overbrace{<D\mid I_1,\ldots,I_D\in\texttt{MDA-IDX-SETs}\mid\to\mid}^{\texttt{MDA's Meta-Parameters}}\ \underbrace{B\mid D_1,\ldots,D_B\mid\to\mid T_1,\ldots,T_B\in\texttt{TYPE}>}_{\texttt{BUFs' Meta-Parameters}}\underbrace{<N_1^1,\ldots,N_{D_B}^B\mid T>}_{\texttt{Postponed Parameters}}}}_{\texttt{Output View: }\mathfrak{ov}}$$

which differs from `inp_view`'s type only in mapping index functions to `OV` (Definition 9), rather than `IV` (Definition 7). Function `out_view` is defined as:

$$\underbrace{(\mathfrak{idx}_{b,a})_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}}}_{\text{Index Functions}} \mapsto \underbrace{\underbrace{\mathfrak{a}}_{\text{MDA}} \overset{\mathfrak{ov}}{\mapsto} (\underbrace{\mathfrak{b}_1,\ldots,\mathfrak{b}_B}_{\text{BUFs}})}_{\text{Output View}}$$

for

$$\mathfrak{b}_b[\,\mathfrak{idx}_{b,a}(i_1,\ldots,i_D)\,] := \mathfrak{a}_{b,a}[i_1,\ldots,i_D]$$

and

$$(\,\mathfrak{a}_{b,a}[i_1,\ldots,i_D]\,)_{b\in[1,B]_{\mathbb{N}},a\in[1,A_b]_{\mathbb{N}}} := \mathfrak{a}[i_1,\ldots,i_D]$$

i.e., $\mathfrak{a}_{b,a}[i_1,\ldots,i_D]$ is the element at point $i_1,\ldots,i_D$ within MDA $\mathfrak{a}$ that belongs to the a-th access of the b-th BUF. We set $\mathfrak{b}_b[j_1,\ldots,j_{D_b}] := \perp$ (symbol $\perp$ denotes the undefined value) for all BUF indices $(j_1,\ldots,j_{D_b})\in[0,N_1^b)_{\mathbb{N}_0}\times\ldots\times[0,N_D^b)_{\mathbb{N}_0}\setminus\bigcup_{a\in[1,A_b]_{\mathbb{N}}}\overset{d}{\Rightarrow}_{\texttt{BUF}}^{\texttt{MDA}\,b,a}(I_1,\ldots,I_D)$ which are not in the function range of the index functions.

Note that the computed output view $\mathfrak{ov}$ is partial (indicated by $\to_p$ in Definition 9), because for non-injective index functions, it must hold $\mathfrak{idx}_{b,a}(i_1,\ldots,i_D)=\mathfrak{idx}_{b,a'}(i'_1,\ldots,i'_D)\Rightarrow\mathfrak{a}_{b,a}[i_1,\ldots,i_D]=\mathfrak{a}_{b,a'}[i'_1,\ldots,i'_D]$, which may not be satisfied for each potential input MDA of the computed view.

Notation 3 (Output Views). Analogously to Notation 2, we denote `out_view` for a particular choice of index functions as:

$$\texttt{out\_view}(\ \texttt{ID}_1:\mathfrak{idx}_{1,1},\ldots,\mathfrak{idx}_{1,A_1}\ ,\ldots,\ \texttt{ID}_B:\mathfrak{idx}_{B,1},\ldots,\mathfrak{idx}_{B,A_B}\ )$$

Example 10. Function `out_view` is used for `MatVec` and `Jacobi1D` (in Notation 3) as follows:

$$\underline{\texttt{MatVec:}}\quad \texttt{out\_view}(\ \underbrace{\texttt{w}:\underbrace{(i,k)\mapsto(i)}_{\texttt{a=1}}}_{\texttt{b=1}}\ )\qquad \underline{\texttt{Jacobi1D:}}\quad \texttt{out\_view}(\ \underbrace{\texttt{w}:\underbrace{(i)\mapsto(i)}_{a=1}}_{b=1}\ )$$

2.3.4 Relation between View Functions. View functions transform data from their domain-specific representation to the MDA-based representation (via input views) and back (via output views). In our implementation presented later, we aim to access data uniformly in the form of MDAs, thereby being independent of domain-specific data representations. However, we aim to store the data physically in the domain-specific format, as such format is usually the most efficient data representation, e.g., storing the input data of `MatVec` as a matrix and vector, rather than as a single MDA which contains many redundancies (e.g., each vector element once per row of the input matrix, as illustrated in Figure 11).

The following lemma proves that functions `inp_view` and `out_view` are invertible and that they are each others inverses. Consequently, the lemma shows how we can arbitrarily switch between the domain-specific data representation and the MDA representation, and consequently also that we can implicitly identify MDAs with their domain-specific data representation (represented in our formalism as BUFs, Definition 5). For example, for computing `MatVec`, we will specify the computations via pattern `md_hom` which operates on MDAs (see Figure 5), but we use the view functions in our implementation to implicitly forward the MDA accesses to accesses on the physically stored BUFs.

Lemma 2. Let

$$\texttt{inp\_view}(\ \texttt{ID}_1 : \mathfrak{idx}_{1,1}, \ldots, \mathfrak{idx}_{1,A_1}\ , \ldots ,\ \ \texttt{ID}_B : \mathfrak{idx}_{B,1}, \ldots, \mathfrak{idx}_{B,A_B}\ )$$

and

$$\texttt{out\_view}(\ \texttt{ID}_1 : \mathfrak{idx}_{1,1}, \ldots, \mathfrak{idx}_{1,A_1}\ , \ldots ,\ \ \texttt{ID}_B : \mathfrak{idx}_{B,1}, \ldots, \mathfrak{idx}_{B,A_B}\ )$$

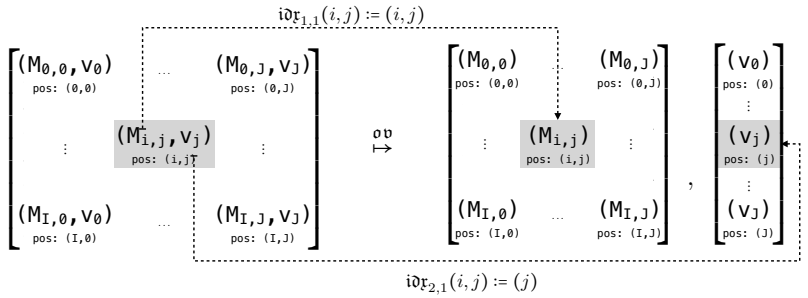
be two arbitrary instances of functions `inp_view` and `out_view` (in Notations 2 and 3), both using the same index functions $\mathfrak{idx}_{1,1}, \ldots, \mathfrak{idx}_{B,A_B}$.

It holds (index functions omitted via ellipsis for brevity):

$$\texttt{inp\_view}(\ldots) \circ \texttt{out\_view}(\ldots) \ = \ \texttt{out\_view}(\ldots) \circ \texttt{inp\_view}(\ldots) \ = \ id$$

Proof. Follows immediately from Definitions 8 and 10. □

The following figure illustrates the lemma using as example the inverse of `MatVec`'s input view (shown in Figure 11):



2.4 Generic High-Level Expression

Figure 15 shows a generic expression in our high-level representation – consisting of higher-order functions `inp_view`, `md_hom`, and `out_view` (Figure 5) – for an arbitrary but fixed choice of index functions, scalar function, and combine operators. We express data-parallel computations using a particular instance of this generic expression in Figure 15.

Note that all meta-parameters of higher-order function `inp_view`, `out_view`, and `md_hom` are automatically deduced from the particular numbers and/or types of the three functions' inputs

(index functions in the case of `inp_view` and `out_view`, and scalar function and combine operators for `md_hom`).

The concrete instance of `md_hom(...)` (i.e., the MDH function returned by `md_hom` for the particular input scalar function and combine operators) has as meta-parameter the MDH function's index sets (see Definition 3) for high flexibility. We use as index sets straightforwardly the input size $(N_1, \ldots, N_D)$ (which abbreviates $([0, N_1)_{\mathbb{N}_0}, \ldots, [0, N_D)_{\mathbb{N}_0})$ - see Notation 1)[12]. Instances of `inp_view(...)` and `out_view(...)` (i.e., the input and output view returned by `inp_view` and `out_view` for concrete index functions) have as meta-parameters the MDA's index sets and the scalar types of BUFs. We explicitly state only the meta-parameter for the BUFs' scalar types in our generic high-level expression (Figure 15), and we avoid explicitly stating the MDA's index sets for simplicity and to avoid redundancies, because the sets can be taken from the `md_hom`'s meta-parameter list.

Note that for better readability of our high-level expressions (Figure 15), we list meta-parameters before parentheses, i.e., instead of writing $\texttt{inp\_view}(\ldots)^{<\ldots>}$, $\texttt{out\_view}(\ldots)^{<\ldots>}$, and $\texttt{md\_hom}(\ldots)^{<\ldots>}$ for the particular instances of higher-order functions, where meta-parameters are listed at the end, we write `inp_view<...>(...)`, `out_view<...>(...)`, and `md_hom<...>(...)`.

$$\texttt{out\_view}\langle T_1^{\texttt{OB}}, \ldots, T_{B^{\texttt{OB}}}^{\texttt{OB}} \rangle\big(\ \texttt{OB}_1 : \mathfrak{id}\mathfrak{x}_{1,1}^{\texttt{OUT}}, \ldots, \mathfrak{id}\mathfrak{x}_{1,A_1^{\texttt{OB}}}^{\texttt{OUT}}\ ,\ \ldots,\ \texttt{OB}_{B^{\texttt{OB}}} : \mathfrak{id}\mathfrak{x}_{B^{\texttt{OB}},1}^{\texttt{OUT}}, \ldots, \mathfrak{id}\mathfrak{x}_{B^{\texttt{OB}},A_{B^{\texttt{OB}}}^{\texttt{OB}}}^{\texttt{OUT}}\ \big)\ \circ$$

$$\texttt{md\_hom}\langle N_1, \ldots, N_D \rangle\big(\ f,\ (\circledast_1, \ldots, \circledast_D)\ \big)\ \circ$$

$$\texttt{inp\_view}\langle T_1^{\texttt{IB}}, \ldots, T_{B^{\texttt{IB}}}^{\texttt{IB}} \rangle\big(\ \texttt{IB}_1 : \mathfrak{id}\mathfrak{x}_{1,1}^{\texttt{INP}}, \ldots, \mathfrak{id}\mathfrak{x}_{1,A_1^{\texttt{IB}}}^{\texttt{INP}}\ ,\ \ldots,\ \texttt{IB}_{B^{\texttt{IB}}} : \mathfrak{id}\mathfrak{x}_{B^{\texttt{IB}},1}^{\texttt{INP}}, \ldots, \mathfrak{id}\mathfrak{x}_{B^{\texttt{IB}},A_{B^{\texttt{IB}}}^{\texttt{IB}}}^{\texttt{INP}}\ \big)$$

Fig. 15. Generic high-level expression for data-parallel computations

2.5 Examples

Figure 16 shows how our high-level representation is used for expressing important data-parallel computations. For brevity, we state only the index functions, scalar function, and combine operators of the higher-order functions; the expression in Figure 15 is then obtained by straightforwardly inserting these building blocks into the higher-order functions.

Subfigure 1. shows how our high-level representation is used for expressing linear algebra routines: 1) `Dot` (*Dot Product*); 2) `MatVec` (*Matrix-Vector Multiplication*); 3) `MatMul` (*Matrix Multiplication*); 4) $\texttt{MatMul}^\intercal$ (*Transposed Matrix Multiplication*) which computes matrix multiplication on transposed input and output matrices; 5) `bMatMul` (*batched Matrix Multiplication*) where multiple matrix multiplications are computed using matrices of the same sizes.

We can observe from the subfigure that our high-level expressions for the routines naturally evolve from each other. For example, the `md_hom` expression for `MatVec` differs from the `md_hom` expression for `Dot` by only containing a further concatenation dimension $+\!\!+$ for its i dimension. We consider this close relation between the high-level expressions of `MatVec` and `Dot` in our approach as natural and favorable, as `MatVec` can be considered as computing multiple times `Dot` – one computation of `Dot` for each value of `MatVec's` i dimension. Similarly, the `md_hom` expression for `MatMul` is very similar to the expression of `MatVec`, by containing the further concatenation

[12] Our formalism allows dynamic shapes, by using symbol $*$ instead of a particular natural number for N_i (formal details provided in the Appendix, Definition 23), which we aim to discuss thoroughly in future work.

md_hom	f	$\circledast_1$	$\circledast_2$	$\circledast_3$	$\circledast_4$
Dot	*	+			
MatVec	*	++	+		
MatMul	*	++	++	+	
MatMul^T	*	++	++	+	
bMatMul	*	++	++	++	+

Views	inp_view A	inp_view B	out_view C
Dot	(k) ↦ (k)	(k) ↦ (k)	(k) ↦ ()
MatVec	(i,k) ↦ (i,k)	(i,k) ↦ (k)	(i,k) ↦ (i)
MatMul	(i,j,k) ↦ (i,k)	(i,j,k) ↦ (k,j)	(i,j,k) ↦ (i,j)
MatMul^T	(i,j,k) ↦ (k,i)	(i,j,k) ↦ (j,k)	(i,j,k) ↦ (j,i)
bMatMul	(b,i,j,k) ↦ (b,i,k)	(b,i,j,k) ↦ (b,k,j)	(b,i,j,k) ↦ (b,i,j)

1) Linear Algebra Routines

md_hom	f	$\circledast_1$	$\circledast_2$	$\circledast_3$	$\circledast_4$	$\circledast_5$	$\circledast_6$	$\circledast_7$	$\circledast_8$	$\circledast_9$	$\circledast_{10}$
Conv2D	*	++	++	+	+						
MCC	*	++	++	++	++	+	+	+			
MCC_Capsule	*	++	++	++	++	+	+	+	++	++	+

Views	inp_view I	inp_view F	out_view O
Conv2D	(p,q,r,s) ↦ (p+r,q+s)	(p,q,r,s) ↦ (r,s)	(p,q,r,s) ↦ (p,q)
MCC	(n,p,...) ↦ (n,p+r,q+s,c)	(n,p,...) ↦ (k,r,s,c)	(n,p,...) ↦ (n,p,q,k)
MCC_Capsule	(n,p,...) ↦ (n,p+r,q+s,c,mi,mk)	(n,p,...) ↦ (k,r,s,c,mk,mj)	(n,p,...) ↦ (n,p,q,k,mi,mj)

2) Convolution Stencils

md_hom	f	$\circledast_1$	...	$\circledast_6$	$\circledast_7$
CCSD(T)	*	++	...	++	+

Views	inp_view A	inp_view B	out_view C
I1	(a,...,g) ↦ (g,d,a,b)	(a,...,g) ↦ (e,f,g,c)	(a,...,g) ↦ (a,...,f)
I2	(a,...,g) ↦ (g,d,a,c)	(a,...,g) ↦ (e,f,g,b)	(a,...,g) ↦ (a,...,f)

3) Quantum Chemistry

md_hom	f	$\circledast_1$	$\circledast_2$	$\circledast_3$
Jacobi1D	J_{1D}	++		
Jacobi2D	J_{2D}	++	++	
Jacobi3D	J_{3D}	++	++	++

Views	inp_view I	out_view O
Jacobi1D	(i1) ↦ (i1+0) , (i1) ↦ (i1+1) , ...	(i1) ↦ (i1)
Jacobi2D	(i1,i2) ↦ (i1+0,i2+1) , ...	(i1,i2) ↦ (i1,i2)
Jacobi3D	(i1,i2,i3) ↦ (i1+0,i2+1,i3+1) , ...	(i1,i2,i3) ↦ (i1,i2,i3)

4) Jacobi Stencils

md_hom	f	$\circledast_1$	$\circledast_2$
PRL	wght	++	$\max_{PRL}$

Views	inp_view N	inp_view E	out_view M
PRL	(i,j) ↦ (i)	(i,j) ↦ (j)	(i,j) ↦ (i)

5) Probabilistic Record Linkage

md_hom	f	$\circledast_1$	$\circledast_2$
Histo	f_{Histo}	+	++
GenHisto	f	⊕	++

Views	inp_view Elems	inp_view Bins	out_view Out
Histo	(e,b) ↦ (e)	(e,b) ↦ (b)	(e,b) ↦ (b)
GenHisto	(e,b) ↦ (e)	(e,b) ↦ (b)	(e,b) ↦ (b)

6) Histogram

md_hom	f	$\circledast_1$
map(f)	f	++
reduce(⊕)	id	⊕
reduce(⊕,⊗)	(x) ↦ (x,x)	(⊕,⊗)

Views	inp_view I	out_view O_1	out_view O_2
map(f)	(i) ↦ (i)	(i) ↦ (i)	
reduce(⊕)	(i) ↦ (i)	(i) ↦ ()	
reduce(⊕,⊗)	(i) ↦ (i)	(i) ↦ ()	(i) ↦ ()

7) Map/Reduce Patterns

md_hom	f	$\circledast_1$	$\circledast_2$
scan(⊕)	id	$+\!\!+_{prefix\text{-}sum}(\oplus)$	
MBBS	id	$+\!\!+_{prefix\text{-}sum}(+)$	+

Views	inp_view A	out_view Out
scan(⊕)	(i) ↦ (i)	(i) ↦ (i)
MBBS	(i,j) ↦ (i,j)	(i,j) ↦ (i)

8) Prefix Sum Computations

Fig. 16. Data-parallel computations expressed in our high-level representation

dimension j for MatMul's j dimension. The same applies to bMatMul: its md_hom expression is the expression of MatMul augmented with one further concatenation dimension.

Regarding $\texttt{MatMul}^\intercal$, the basic computation part of $\texttt{MatMul}^\intercal$ and MatMul are the same, which is exactly reflected in our formalisms: both $\texttt{MatMul}^\intercal$ and MatMul are expressed using exactly the same md_hom expression. The differences between $\texttt{MatMul}^\intercal$ and MatMul lies only in the data accesses – transposed accesses in the case of $\texttt{MatMul}^\intercal$ and non-transposed accesses in the case of MatMul. Data accesses are expressed in our formalism, in a structured way, via the view functions: for example, for $\texttt{MatMul}^\intercal$, we use for its first input matrix A index function $(i, j, k) \mapsto (k, i)$, for transposed access, instead of using index function $(i, j, k) \mapsto (i, k)$ as for MatMul's non-transposed accesses.

Note that all md_hom expressions in the subfigure are well defined according to Lemma 1.

Subfigure 2. shows how convolution-style stencil computations are expressed in our high-level representation: 1) Conv2D expresses a standard convolution that uses a 2D sliding window [Podlozhnyuk 2007]; 2) MCC expresses a so-called *Multi-Channel Convolution* [Dumoulin and Visin 2018] – a generalization of Conv2D that is heavily used in the area of deep learning; 3) MCC_Capsule is a recent generalization of MCC [Hinton et al. 2018] which attracted high attention due to its relevance for advanced deep learning neural networks [Barham and Isard 2019].

While our md_hom expressions for convolutions are quite similar to those of linear algebra routines (they all use multiplication $*$ as scalar function, and a mix of concatenations $+\!\!+$ and point-wise additions + as combine operators), the index functions used for the view functions of convolutions are notably different from those used for linear algebra routines: the index functions of convolutions contain arithmetic expressions (e.g., p+r and q+s), thereby access neighboring elements in their input – a typical access pattern in stencil computations requiring special optimizations [Hagedorn et al. 2018]. Moreover, convolution-style computations are often high-dimensional (e.g., 10 dimensions in the case of MCC_Capsule), whereas linear algebra routines usually rely on less dimensions. Our experiments in Section 5 confirm that optimizations respecting the data access patterns and high dimensionality of convolution computations, as in our approach, usually achieve significantly higher performance than using optimizations chosen toward linear algebra routines as in vendor libraries provided by NVIDIA and Intel for convolutions [Li et al. 2016].

Subfigure 3. shows how quantum chemistry computation *Coupled Cluster* (CCSD(T)) [Kim et al. 2019] is expressed in our high-level representation. The CCSD(T) computation notably differs from those of linear algebra routines and convolution-style stencils, by accessing its high-dimensional input data in sophisticated transposed fashions: for example, the view function of CCSD(T)'s *instance one* (denoted as I1 in the subfigure) uses indices a and b to access the last two dimensions of its A input tensor (rather than the first two dimensions of the tensor, as would be the case for non-transposed accesses).

The subfigure presents only two CCSD(T) instances, for brevity – in our experiments in Section 5, we present experimental results for nine different real-world CCSD(T) instances.

Subfigures 4-6. show computations whose scalar functions and combine operators are different from those used in Subfigures 1-3 (which are straightforward multiplications $*$, concatenation, and point-wise additions + only in Subfigures 1-3). For example, Jacobi stencils (Subfigure 4) use as scalar function the Jacobi-specific computation $\texttt{J}_{\texttt{nD}}$ [Cecilia et al. 2012], and *Probabilistic Record Linkage (PRL)* [Christen 2012], which is used to identify duplicate entries in a data base, uses a PRL-specific both scalar function wght and combine operator $\texttt{max}_{\texttt{PRL}}$ (point-wise combination via the PRL-specific binary function $\texttt{max}_{\texttt{PRL}}$) [Rasch et al. 2019b]. Histograms, in their generalized version [Henriksen et al. 2020] (denoted as GenHisto in Subfigure 6), use an arbitrary, user-defined scalar function f and a user-defined associative and commutative combine operator $\oplus$; the standard

histogram variant Histo is then a particular instance of GenHist, for $\oplus = +$ (point-wise addition) and $f = f_{\texttt{Histo}}$, where $f_{\texttt{Histo}}(e, b) = 1$ iff $e = b$ and $f_{\texttt{Histo}}(e, b) = 0$ otherwise. Histogram's are often analyzed regarding their runtime complexity [Henriksen et al. 2020]; we provide such a discussion for our MDH-based Histogram implementation in the Appendix, Section B.8, for the interested reader.

Subfigure 7. shows how typical map and reduce patterns [González-Vélez and Leyton 2010] are implemented in our high-level representation. Examples map(f) and reduce($\oplus$) (discussed in Examples 3 and 4) are simple and thus straightforwardly expressed in our representation. In contrast, example reduce($\oplus, \otimes$) is more complex and shows how reduce($\oplus$) is extended toward combining the input vector simultaneously twice – once combining vector elements via operator $\oplus$ and once using operator $\otimes$. The outcome of reduce($\oplus, \otimes$) are two scalars – one representing the result of combination via $\oplus$ and the other of combination via $\otimes$ – which we map via the output view to output elements $\texttt{O}_1$ (result of $\oplus$) and $\texttt{O}_2$ (result of $\otimes$), correspondingly; this is also illustrated in Figure 14.

Subfigure 8. presents *prefix-sum computations* [Blelloch 1990] which differ from the computations in Subfigures 1-7 in terms of their combine operators: the operator used for expressing computations in Subfigure 8 is different from concatenation (Example 1) and point-wise combinations (Example 2). Computation scan($\oplus$) uses as combine operator $+\!\!+_{\texttt{prefix-sum}}(\oplus)$ which computes prefix-sum [Gorlatch and Lengauer 1997] (formally defined in the Appendix, Section B.9) according to binary operator $\oplus$, and MBBS (Maximum Bottom Box Sum) [Farzan and Nicolet 2019] uses a particular instance of prefix-sum for $\oplus = +$ (addition).

3 LOW-LEVEL REPRESENTATION FOR DATA-PARALLEL COMPUTATIONS

We introduce our low-level representation for expressing data-parallel computations. In contrast to our high-level representation, our low-level representation explicitly expresses the de-composition and re-composition of computations (informally illustrated in Figure 3). Moreover, our low-level representation is designed such that it can be straightforwardly transformed to executable program code, because it explicitly captures and expresses data movement and parallelization optimizations.

In the following, after briefly discussing an introductory example in Section 3.1, we introduce in Section 3.2 our formal representation of computer systems, to which we refer to as *Abstract System Model (ASM)*. Based on this model, we define *low-level MDAs*, *low-level BUFs*, and *low-level combine operators* in Section 3.3, which are basic building blocks of our low-level representation.

Note that all the details and concepts discussed in this section are transparent to the end user of our system and therefore the user is not exposed to these details: expressions in our low-level representation are fully automatically generated from expressions in our high-level representation for the user (Figure 4), according to the methodologies presented later in Section 4 and auto-tuning [Rasch et al. 2021].

3.1 Introductory Example

Figure 17 illustrates our low-level representation by showing how MatVec (matrix-vector multiplication) is expressed in our representation. In our example, we use an input matrix $M \in T^{512 \times 4096}$ of size 512×4096 (size chosen arbitrarily) that has an arbitrary but fixed scalar type $T \in \texttt{TYPE}$; the input vector $v \in T^{4096}$ is of size 4096, correspondingly.

For better illustration, we consider for this introductory example a straightforward, artificial target architecture that has only two memory layers – *Host Memory (*HM*)* and *Cache Memory (*L1*)* – and one *Core Layer* (COR) only; our examples presented and discussed later in this section target

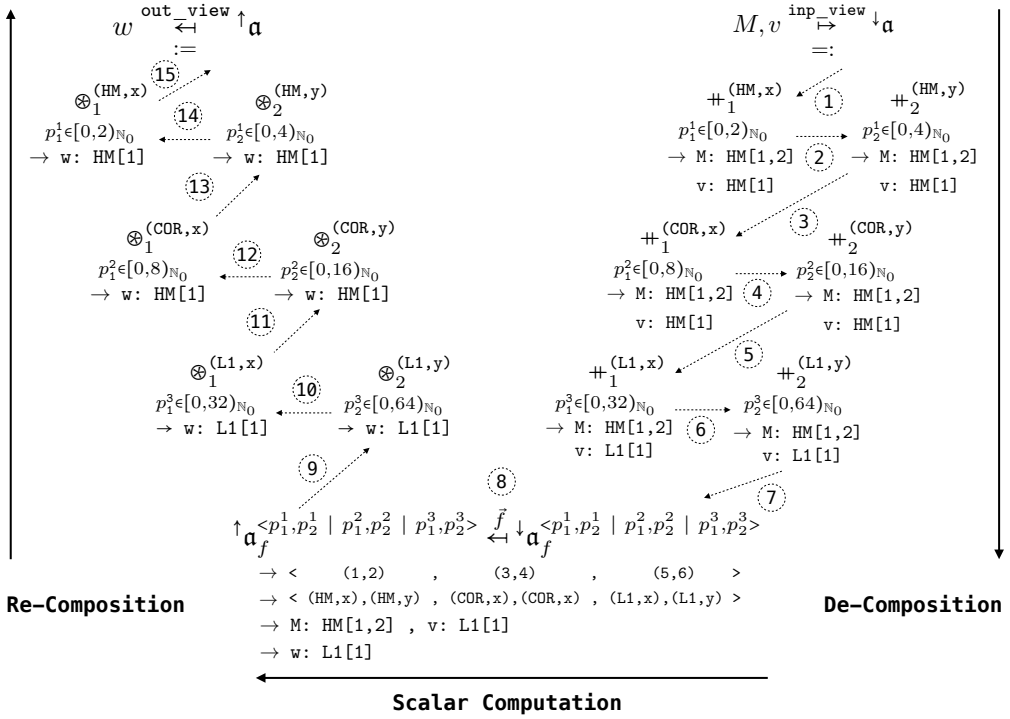


Fig. 17. Low-level expression for straightforwardly computing Matrix-Vector Multiplication (MatVec) on a simple, artificial architecture with two memory layers (HM and L1) and one core layer (COR). Dotted lines indicate data flow.

real-world architectures (e.g., CUDA-capable NVIDIA GPUs). The particular values of tuning parameters (discussed in detail later in this section), such as the number of threads and the order of combine operators, are chosen by hand for this example and as straightforward for simplicity and better illustration.

Our low-level representations work in three phases: 1) *de-composition* (steps 1-7, in the right part of Figure 17), 2) *scalar* (step 8, bottom part of the figure), 3) *re-composition* (steps 9-15, left part). Steps are arranged from right to left, inspired by the application order of function composition.

1. De-Composition Phase: The de-composition phase (steps 1-7 in Figure 17) partitions input MDA $^{\downarrow}\mathfrak{a}$ (in the top right of Figure 17) to the structure $^{\downarrow}\mathfrak{a}_f^{<\cdots>}$ (bottom right) to which we refer to as *low-level MDA* and define formally in the next subsection. The low-level MDA represents a partitioning of MDA $^{\downarrow}\mathfrak{a}$ (a.k.a *hierarchical, multi-dimensional tiling* in programming terminology), where each particular choice of indices $p_1^1 \in [0,2)_{\mathbb{N}_0}$, $p_2^1 \in [0,4)_{\mathbb{N}_0}$, $p_1^2 \in [0,8)_{\mathbb{N}_0}$, $p_2^2 \in [0,16)_{\mathbb{N}_0}$, $p_1^3 \in [0,32)_{\mathbb{N}_0}$, $p_2^3 \in [0,64)_{\mathbb{N}_0}$ refers to an MDA that represents an individual part of MDA $^{\downarrow}\mathfrak{a}$ (a.k.a. *tile* in programming – informally illustrated in Figure 7). The partitions are arranged on multiple layers (indicated by the p's superscripts) and in multiple dimensions (indicated by subscripts) – as illustrated in Figure 18 – according to the memory/core layers of the target architecture and dimensions of the MDH computation: we partition for each of the target architecture's three layers (HM, L1, COR) and in each of the two dimensions of the MDH (dimensions 1 and 2, as we use example MatVec in Figure 17, which represents a two-dimensional MDH computation). Consequently, our

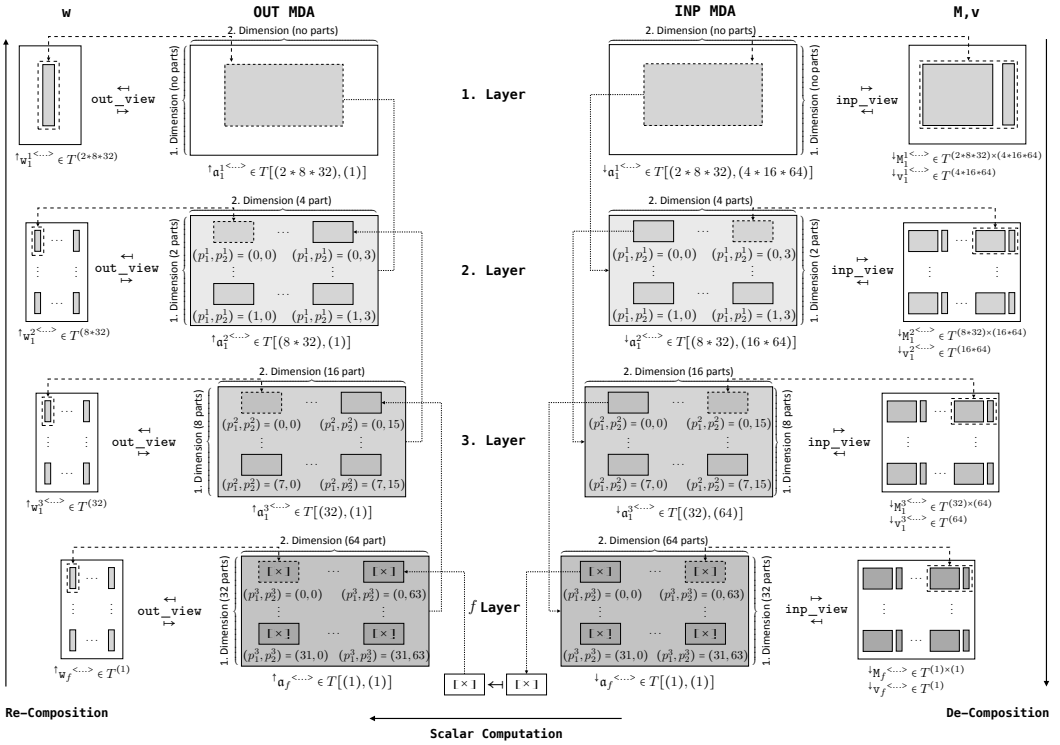


Fig. 18. Illustration of multi-layered, multi-dimensional MDA partitioning using the example MDA from Figure 17. In this example, we use three layers and two dimensions, according to Figure 17.

partitioning approach allows efficiently exploiting each particular layer of the target architecture (both memory and core layers), and also optimizing for both dimensions of the target computation (in the case of MatVec, the i-dimension and also the k-dimension – see Figure 1), allowing for potentially fine-grained data movement and parallelization strategies, as we discuss in the following.

We compute the partitionings of MDAs by applying the concatenation operator (Example 1) inversely[13] (indicated by using =: instead of := in the top right part of Figure 17). For example, we partition in Figure 17 MDA $\downarrow\mathfrak{a}$ first via the inverse of $+\!\!+_1^{(\mathtt{HM},\mathtt{x})}$ in dimension 1 (indicated by the subscript 1 of $+\!\!+_1^{(\mathtt{HM},\mathtt{x})}$; the superscript $(\mathtt{HM},\mathtt{x})$ is explained later) in 2 parts, as p_1^1 iterates over interval $[0,2)_{\mathbb{N}_0} = \{0,1\}$ which consists of two elements (0 and 1) – the interval is chosen arbitrarily for this example. Afterwards, each of the obtained parts is further partitioned, in the second dimension, via $+\!\!+_2^{(\mathtt{HM},\mathtt{y})}$ in 4 parts (p_2^1 iterates over $[0,4)_{\mathbb{N}_0} = \{0,1,2,3\}$ which consists of four elements). The $(2*4)$-many HM parts are then each further partitioned in both dimensions for the COR layer in $(8*16)$ parts, and each individual COR part is again partitioned for the L1 layer in $(32*64)$ parts, resulting in $(2*8*32)*(4*16*64) = 512*4096$ parts in total.

[13] It is easy to see that operator *concatenation* (Example 1) is invertible for any particular choice of meta-parameters (formally proved in the Appendix, Section C.2).

We always use a *full partitioning* in our low-level expressions[14], i.e., each particular choice of indices $p_1^1, p_2^1, p_1^2, p_2^2, p_1^3, p_2^3$ refers to a part that contains a singleton MDA (in Figure 18, the individual MDA elements are denoted via symbol ×, in the bottom part of the figure). By relying on a full partitioning, we can apply scalar function f to these singleton parts in the scalar phase (described in the next paragraph). This is because function f is defined to take as input a single MDA element only (Definition 4), thereby making defining scalar functions more convenient for the user.

The superscript of combine operators, e.g., `(COR,x)` of operator $+\!\!+_1^{(\texttt{COR},\texttt{x})}$, is a so-called *operator tag* (formal definition given in the next subsection). A tag indicates to our code generator whether its combine operator is assigned to a memory layer (and thus computed sequentially in our generated code) or to a core layer (and thus computed in parallel). For example, tag `(COR,x)` indicates that parts processed by operator $+\!\!+_1^{(\texttt{COR},\texttt{x})}$ should be computed by cores `COR`, and thus in parallel; the dimension tag `x` indicates that `COR` layer's `x` dimension should be used for computing the operator (we use dimension `x` for our example architecture as an analogous concept to CUDA's thread/block dimensions x,y,z for GPU architectures [NVIDIA 2022g]), as we also discuss in the next subsection. In contrast, tag `(HM,x)` refers to a memory layer (host memory `HM`) and thus, operator $+\!\!+_1^{(\texttt{HM},\texttt{x})}$ is computed sequentially. Since the current state-of-practice programming approaches (OpenMP, CUDA, OpenCL, ...) have no explicit notion of memory tiles (e.g., by offering the potential variables `tileIdx.x/tileIdx.y/tileIdx.z`, as analogous concepts to CUDA variables `threadIdx.x/threadIdx.y/threadIdx.z`), the dimensions tag `x` in `(HM,x)` is ignored by our code generator (which currently generates OpenMP, CUDA, or OpenCL code), because `HM` refers to a memory layer.

Note that the number of parts (2 parts on layer 1 in dimension 1; 4 parts on layer 1 in dimension 2; ...), the combine operators' tags, and our partition order (e.g. first partitioning in MDA's dimension 1 and afterwards in dimension 2) are chosen arbitrarily for this example and should be optimized (auto-tuned) for a particular target device and characteristics of the input and output data (size, memory layouts, etc.) to achieve high performance, which we discuss in detail later in this section.

2. Scalar Phase: In the scalar phase (step 8 in Figure 17), we apply MDH's scalar function f to the individual MDA elements which are contained by the MDA's singleton parts

$$\downarrow_{f}^{\mathfrak{a}} \langle p_1^1, p_2^1 \mid p_1^2, p_2^2 \mid p_1^3, p_2^3 \rangle$$

for each particular choice of indices $p_1^1, p_2^1, p_1^2, p_2^2, p_1^3, p_2^3$, which results in

$$\uparrow_{f}^{\mathfrak{a}} \langle p_1^1, p_2^1 \mid p_1^2, p_2^3 \mid p_1^3, p_2^3 \rangle$$

In the figure, $\vec{f}$ (introduced in Definition 4) is the slight adaption of function f that operates on a singleton MDA, rather than a scalar.

Annotation → `< (1,2) , ... >` indicates the application order of applying scalar function (in this example, first iterating over p_1^1, then over p_2^1, etc), and we use annotation → `< (HM,x) , ... >` to indicate how the scalar computation is assigned to the target architecture (this is described in detail later in this section). Annotations → `M: HM , v: L1` and → `w: L1` (in the bottom part of Figure 17) indicate the memory regions to be used for reading and writing the input scalar of function f (also described later in detail).

[14] Our future work (outlined in Section 8) aims to additionally allow coarser-grained partitioning schemas as well, e.g., to target domain-specific hardware extensions (such as *NVIDIA Tensor Cores* [NVIDIA 2017] which compute 4 × 4 matrices immediately in hardware, rather than 1 × 1 matrices as obtained in the case of a full partitioning).

3. Re-Composition Phase: Finally, the re-composition phase (steps 9-15 in Figure 17) combines the computed parts $\uparrow a \, {}_{f}^{<p_1^1,p_2^1 \mid p_1^2,p_2^2 \mid p_1^3,p_2^3>}$ (bottom left in the figure) to the final result $\uparrow a$ (top left) via MDH's combine operators, which are in the case of matrix-vector multiplication $\circledast_1 := +\!\!+$ (concatenation) and $\circledast_2 := +$ (point-wise addition). In this example, we first combine the `L1` parts in dimension 2 and then in dimension 1; afterwards, we combine the `COR` parts in both dimensions, and finally the `HM` parts. Analogously to before, this order of combine operators and their tags are also chosen arbitrarily for this example and should be auto-tuned for high performance.

In the de- and re-composition phases, the arrow notation below combine operators allow efficiently exploiting architecture's memory hierarchy, by indicating the memory region to read from (de-composition phase) or to write to (re-composition phase); the annotations also indicate the memory layouts to use. We exploit these memory and layout information in both: i) our code generation to assign combine operators' input and output data to memory regions and to chose memory layouts for the data (row major, column major, etc); ii) our formalism to specify constraints of programming models, e.g., that in CUDA, results of GPU cores can only be combined in designated memory regions [NVIDIA 2022f]. For example, annotation → `M: HM[1,2] , v: L1[1]` below an operator in the de-composition phase indicates to our code generator that the parts (a.k.a tiles) of matrix M used for this computation step should be read from host memory `HM` and that parts of vector v should be copied to and accessed from fast `L1` memory. The annotation also indicates that `M` should be stored using a row-major memory layout (as we use `[1,2]` and not `[2,1]`). The memory regions and layouts are chosen arbitrarily for this example and should be chosen as optimized for the particular target architecture and characteristics of the input and output data (we currently rely on auto-tuning [Rasch et al. 2021] for choosing optimized values of performance-critical parameters, as we discuss in Section 5).

Formally, the arrow notation of combination operators is a concise notation to hide MDAs and BUFs for intermediate results, which is discussed in the Appendix, Section C.3, for the interested reader.

Excursion: Code Generation

Our low-level expressions can be straightforwardly transformed to executable program code in imperative-style programming languages (such as OpenMP, CUDA, and OpenCL). As code generation is not the focus of this work, we demonstrate our code generation approach briefly using the example of Figure 17. Details about our code generation process are provided in Section E of our Appendix, and will be presented and illustrated in detail in our future work.

We implement MDAs via *preprocessor directives*. In the case of `MatVec`, we implement its input MDA, according to Definition 8, as: `#define inp_mda(i,k) M[i][k],v[k]`

Combine operators are implemented as sequential or parallel loops. For example, the operator $+\!\!+_1^{(\texttt{HM},\texttt{x})}$ is assigned to memory layer `HM` and thus implemented as a sequential loop (loop range indicated by $[0,2)_{\mathbb{N}_0}$), and operator $+\!\!+_1^{(\texttt{COR},\texttt{x})}$ is assigned to core layer `COR` and thus implemented as a parallel loop (e.g., a loop annotated with `#pragma omp parallel for` in OpenMP [OpenMP 2022], or variable `threadIdx.x` in CUDA [NVIDIA 2022g]).

Correspondingly, our three phases (de-composition, scalar, and re-composition) each correspond to an individual loop nest; we generate the nests as fused when the tags of combine operators have the same order in phases, as in Figure 17: `(HM,x)` → `(HM,y)` → `(COR,x)` → ... → `(L1,y)`. Note that our currently targeted programming models (OpenMP, CUDA, and OpenCL) have no explicit notion of *tiles*, e.g., by offering the potential variables `tileIdx.x`/`tileIdx.y`/`tileIdx.z` for managing tiles automatically in the programming model (similarly as variables `threadIdx.x`/`threadIdx.y`/`threadIdx.z` automatically manage threads in CUDA). Consequently, the dimension information

within tags are currently ignored by our code generator when the operator tag refers to a memory layer (such as dimension `x` in tag `(HM,x)` which refers to memory layer `HM`).

We implement operators' memory regions as straightforward allocations in the corresponding memory region (e.g., CUDA's `device`, `shared`, or `register` memory [NVIDIA 2022g], according to the arrow annotations in our low-level expression); memory layouts are also implemented via pre-processor directives, e.g., `#define M(i,k) M[k][i]` when storing `MatVec`'s input matrix M as transposed.

Code optimizations that are applied on a lower abstraction level than proposed by our representation in Example 17 are beyond the scope of this work and outlined in Section E.3 of our Appendix, e.g., loop fusion and loop unrolling which are applied to program code on the low, loop-based abstraction level.

In the following, we introduce in Section 3.2 our formal representation of a computer system (which can be a single device, but also a multi-device or a multi-node system, as we discuss soon), and we illustrate our formal system representation using the example architectures targeted by programming models OpenMP, CUDA, and OpenCL. Afterwards, in Section 3.3, we formally define the basic building blocks of our low-level representation – *low-level MDAs*, *low-level BUFs*, and *low-level combine operators* – based on our formal system representation.

3.2 Abstract System Model (ASM)

Definition 11 (Abstract System Model)**.** An *L-Layered Abstract System Model (ASM)*, $L \in \mathbb{N}$, is any pair of two positive natural numbers

$$(\,\mathtt{NUM\_MEM\_LYRs}\,,\,\mathtt{NUM\_COR\_LYRs}\,) \in \mathbb{N} \times \mathbb{N}$$

for which $\mathtt{NUM\_MEM\_LYRs} + \mathtt{NUM\_COR\_LYRs} \;=\; L$.

Our ASM can model architectures with arbitrarily deep memory and core hierarchies[15]: `NUM_MEM_LYRs` denotes the target architecture's number of memory layers and `NUM_COR_LYRs` the architecture's number of core layers, correspondingly. For example, the artificial architecture we use in Figure 17 is represented as an ASM instance as follows (bar symbols denote set cardinality):

$$\mathtt{ASM}_{\mathtt{artif.}} := (\;\; |\{\mathtt{HM},\mathtt{L1}\}| \;\;,\;\; |\{\mathtt{COR}\}| \;\;) = (2,1)$$

The instance is a pair consisting of the numbers 2 and 1 which represent the artificial architecture's two memory layers (`HM` and `L1`) and its single core layers (`COR`).

Example 11. We show particular ASM instances that represent the device models of state-of-practice approaches OpenMP, CUDA, and OpenCL:

$$\begin{aligned}
\mathtt{ASM}_{\mathtt{OpenMP}} &:= (\;\; |\{\mathtt{MM},\mathtt{L2},\mathtt{L1}\}| \;\;,\;\; |\{\mathtt{COR}\}| \;\;) = (3,1)\\
\mathtt{ASM}_{\mathtt{OpenMP+L3}} &:= (\;\; |\{\mathtt{MM},\mathtt{L3},\mathtt{L2},\mathtt{L1}\}| \;\;,\;\; |\{\mathtt{COR}\}| \;\;) = (4,1)\\
\mathtt{ASM}_{\mathtt{OpenMP+L3+SIMD}} &:= (\;\; |\{\mathtt{MM},\mathtt{L3},\mathtt{L2},\mathtt{L1}\}| \;\;,\;\; |\{\mathtt{COR},\mathtt{SIMD}\}| \;\;) = (4,2)\\
\mathtt{ASM}_{\mathtt{CUDA}} &:= (\;\; |\{\mathtt{DM},\mathtt{SM},\mathtt{RM}\}| \;\;,\;\; |\{\mathtt{SMX},\mathtt{CC}\}| \;\;) = (3,2)\\
\mathtt{ASM}_{\mathtt{CUDA+WRP}} &:= (\;\; |\{\mathtt{DM},\mathtt{SM},\mathtt{RM}\}| \;\;,\;\; |\{\mathtt{SMX},\mathtt{WRP},\mathtt{CC}\}| \;\;) = (3,3)\\
\mathtt{ASM}_{\mathtt{OpenCL}} &:= (\;\; |\{\mathtt{GM},\mathtt{LM},\mathtt{PM}\}| \;\;,\;\; |\{\mathtt{CU},\mathtt{PE}\}| \;\;) = (3,2)
\end{aligned}$$

[15] We deliberately do not model into our ASM representation an architecture's particular number of cores and sizes of memory regions, because our optimization process is designed to be generic in these numbers and sizes for high flexibility.

OpenMP is often used to target $(3 + 1)$-layered architectures which rely on 3 memory regions (main memory MM, and caches L2 and L1) and 1 core layer (COR). OpenMP-compatible architectures sometimes also contain the L3 memory region, and they may allow exploiting SIMD parallelization (a.k.a. *vectorization* [Klemm et al. 2012]), which are expressed in our ASM representation as a further memory or core layer, respectively.

CUDA's target architectures are $(3+2)$-layered: they consist of *Device Memory (*DM*)*, *Shared Memory (*SM*)*, and *Register Memory (*RM*)*, and they offer as cores so-called *Streaming Multiprocessors (*SMX*)* which themselves consist of *Cuda Cores (*CC*)*. CUDA also has an implicit notion of so-called *Warps (*WRP*)* which are not explicitly represented in the CUDA programming model [NVIDIA 2022g], but often exploited by programmers – via special intrinsics (e.g., *shuffle* and *tensor core intrinsics* [NVIDIA 2017, 2018]) – to achieve highest performance.

OpenCL-compatible architectures are designed analogously to those targeted by the CUDA programming model; consequently, both OpenCL- and CUDA-compatible architectures are represented by the same ASM instance in our formalism. Apart from straightforward syntactical differences between OpenCL and CUDA [StreamHPC 2016], we see as the main differences between the two programming models (from our ASM-based abstraction level) that OpenCL has no notion of warps, and it uses a different terminology – *Global/Local/Private Memory (*GM/LM/PM*)* instead of device/shared/register memory, and *Compute Unit (*CU*)* and *Processing Element (*PE*)*, rather than SMX and CC.

In the following, we consider memory regions and cores of ASM-represented architectures as arrangeable in an arbitrary number of dimensions. Programming models for such architectures often have native support for such arrangements. For example, in the CUDA model, memory is accessed via arrays which can be arbitrary-dimensional (a.k.a *multi-dimensional C arrays*), and cores are programmed in CUDA via threads which are arranged in CUDA's so-called dimensions x, y, z; further thread dimensions can be explicitly programmed in CUDA, e.g., by embedding them in the last dimension z. Details on our arrangements of memory and cores are provided in the Appendix, Section C.4.

We express constraints of programming models – for example, that in CUDA, SMX can combine their results in DM only [NVIDIA 2022f] – via so-called *tuning parameter constraints*, which we discuss later in this section.

Note that we call our abstraction *Abstract System Model* (rather than *Abstract Architecture Model*, or the like), because it can also represent systems consisting of multiple devices and/or nodes, etc. For example, our ASM representation of a multi-GPU system is:

$$\mathsf{ASM}_{\mathtt{Multi\text{-}GPU}} := \left(\left|\{\mathsf{HM}, \mathsf{DM}, \mathsf{SM}, \mathsf{RM}\}\right|, \left|\{\mathsf{GPU}, \mathsf{SMX}, \mathsf{CC}\}\right| \right) = (4, 3)$$

It extends our ASM-based representation of CUDA devices (Example 11) by *Host Memory (*HM*)* which represents the memory region of the system containing the GPUs (and in which the intermediate results of different GPUs are combined), and it introduces the further core layer GPU representing the system's GPUs. Analogously, our ASM representation of a multi-node, multi-GPU system is:

$$\mathsf{ASM}_{\mathtt{Multi\text{-}Node\text{-}Multi\text{-}GPU}} := \left(\left|\{\mathsf{NM}, \mathsf{HM}, \mathsf{DM}, \mathsf{SM}, \mathsf{RM}\}\right|, \left|\{\mathsf{NOD}, \mathsf{GPU}, \mathsf{SMX}, \mathsf{CC}\}\right| \right) = (5, 4)$$

It adds to ASM $\mathsf{ASM}_{\mathtt{Multi\text{-}GPU}}$ the memory layer (*Node Memory (*NM*)*) which represents the memory region of the host node, and it adds core layer (*Node* (NOD)) which represents the compute nodes. Our approach is currently designed for *homogeneous systems*, i.e., all devices/nodes/... are assumed to be identical. We aim to extend our approach toward *heterogeneous systems* (which may consist of different devices/nodes/...) as future work, inspired by dynamic load balancing approaches [Chen et al. 2010].

3.3 Basic Building Blocks

We introduce the three main basic building blocks of our low-level representation: 1) *low-level MDAs* which represent multi-layered, multi-dimensionally arranged collection of ordinary MDAs (Definition 1) – one ordinary MDA per memory/core layer of their target ASM and for each dimension of the MDA computation (illustrated in Figure 18); 2) *low-level BUFs* which are a collection of ordinary BUFs (Definition 5) and that have a notion *memory regions* and *memory layouts*; 3) *low-level combine operators* which represent combine operators (Definition 2) to which the layer and dimension of their target ASM is assigned that are intended to be used to compute the operator in our generated code (e.g., a core layer to compute the operator in parallel).

Definition 12 (Low-Level MDA)**.** Let be $L \in \mathbb{N}$ (representing an ASM's number of layers) and $D \in \mathbb{N}$ (representing an MDH's number of dimensions). Let further be $P = ((P_1^1, \ldots, P_D^1) , \ldots , (P_1^L, \ldots, P_D^L)) \in \mathbb{N}^{L \times D}$ an arbitrary tuple of L-many D-tuples of positive natural numbers, $T \in \texttt{TYPE}$ a scalar type, and $I := ((I_d^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>} \in \texttt{MDA-IDX-SETs})_{d \in [1,D]_{\mathbb{N}}})^{< (p_1^1,\ldots,p_D^1) \in P_1^1 \times \ldots \times P_D^1 \mid \ldots \mid (p_1^L,\ldots,p_D^L) \in P_1^L \times \ldots \times P_D^L >}$ an arbitrary collection of D-many MDA index sets (Definition 1) for each particular choice of indices $(p_1^1, \ldots, p_D^1) \in P_1^1 \times \ldots \times P_D^1 \;,\; \ldots \;,\; (p_D^L, \ldots, p_D^L) \in P_1^L \times \ldots \times P_D^L$[16] (illustrated in Figure 18).

An L-layered, D-dimensional, P-partitioned *low-level MDA* that has scalar type T and index sets I is any function $\mathfrak{a}_{ll}$ of type:

$$\mathfrak{a}_{ll}^{\overbrace{<(p_1^1,\ldots,p_D^1) \in P_1^1 \times \ldots \times P_D^1}^{\text{Partitioning: Layer 1}} \mid \ldots \mid \overbrace{(p_1^L,\ldots,p_D^L) \in P_1^L \times \ldots \times P_D^L>}^{\text{Partitioning: Layer } L}} : I_1^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>} \times \ldots \times I_D^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>} \to T$$

We use low-level MDAs in the following to represent partitionings of MDAs (as illustrated soon and formally discussed the Appendix, Section C.7).

Next, we introduce *low-level BUFs* which work similarly as BUFs (Definition 5), but are tagged with a memory region and a memory layout. While these tags have no effect on operators' semantics, they indicate later to our code generator in which memory region the BUF is stored and which memory layout to chose for storing the BUF. Moreover, we use these tags to formally define constraints of programming models, e.g., that according to the CUDA specification [NVIDIA 2022f], SMX cores can combine their results in memory region DM only.

Definition 13 (Low-Level BUF)**.** Let be $L \in \mathbb{N}$ (representing an ASM's number of layers) and $D \in \mathbb{N}$ (representing an MDH's number of dimensions). Let further $P = ((P_1^1, \ldots, P_D^1) , \ldots , (P_1^L, \ldots, P_D^L)) \in \mathbb{N}^{L \times D}$ be an arbitrary tuple of L-many D-tuples of positive natural numbers, $T \in \texttt{TYPE}$ a scalar type, and $N := ((N_d^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>} \in \mathbb{N})_{d \in [1,D]_{\mathbb{N}}})^{< (p_1^1,\ldots,p_D^1) \in P_1^1 \times \ldots \times P_D^1 \mid \ldots \mid (p_1^L,\ldots,p_D^L) \in P_1^L \times \ldots \times P_D^L >}$ be a BUF's size (Definition 5) for each particular choice of $p_1^1, \ldots, p_D^L$.

An L-layered, D-dimensional, P-partitioned *low-level BUF* that has scalar type T and size N is any function $\mathfrak{b}_{ll}$ of type ($\twoheadrightarrow$ denotes bijection):

$$\mathfrak{b}_{ll}^{\overbrace{<\texttt{MEM} \in [1,\texttt{NUM\_MEM\_LYRS}]_{\mathbb{N}}}^{\text{Memory Region}} \mid \overbrace{\sigma : [1,D]_{\mathbb{N}} \twoheadrightarrow [1,D]_{\mathbb{N}}>}^{\text{Memory Layout}} \overbrace{<(p_1^1,\ldots,p_D^1) \in P_1^1 \times \ldots \times P_D^1}^{\text{Partitioning: Layer 1}} \mid \ldots \mid \overbrace{(p_1^L,\ldots,p_D^L) \in P_1^L \times \ldots \times P_D^L>}^{\text{Partitioning: Layer } L}} : [0, N_1^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>})_{\mathbb{N}_0} \times \ldots \times [0, N_D^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>})_{\mathbb{N}_0} \to T$$

[16] Analogously to Notation 1, we identify each $P_d^l \in \mathbb{N}$ implicitly also with the interval $[0, P_d^l)_{\mathbb{N}_0}$ (inspired by set theory).

We refer to MEM as low-level BUF's *memory region* and to σ as its *memory layout*, and we refer to the function

$$\mathfrak{b}_{ll}^{\mathsf{trans}<\overbrace{\mathsf{MEM}\in[1,\mathsf{NUM\_MEM\_LYRs}]_{\mathbb{N}}}^{\text{Memory Region}} \mid \overbrace{\sigma:[1,D]_{\mathbb{N}}\twoheadrightarrow[1,D]_{\mathbb{N}}}^{\text{Memory Layout}}><\overbrace{(p_1^1,\ldots,p_D^1)\in P_1^1\times\ldots\times P_D^1}^{\text{Partitioning: Layer 1}} \mid \ldots \mid \overbrace{(p_1^L,\ldots,p_D^L)\in P_1^L\times\ldots\times P_D^L}^{\text{Partitioning: Layer } L}>} : [0, N_{\sigma(1)}^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>})_{\mathbb{N}_0} \times \ldots \times [0, N_{\sigma(D)}^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>})_{\mathbb{N}_0} \to T$$

that is defined as

$$\mathfrak{b}_{ll}^{\mathsf{trans}<\mathsf{MEM}\mid\sigma><p_1^1,\ldots,p_D^1\mid\ldots\mid p_1^L,\ldots,p_D^L>}(i_{\sigma(1)},\ldots,i_{\sigma(D)}) := \mathfrak{b}_{ll}^{<\mathsf{MEM}\mid\sigma><p_1^1,\ldots,p_D^1\mid\ldots\mid p_1^L,\ldots,p_D^L>}(i_1,\ldots,i_D)$$

as $\mathfrak{b}_{ll}$'s *transposed function representation*.

Finally, we introduce *low-level combine operators*. We define such operators to behave the same as ordinary combine operators (Definition 2), but we additionally tag them with a layer of their target ASM. Similarly as for low-level BUFs, the tag has no effect on semantics, but it is used in our code generation to assign the computation to the hardware (e.g., indicating that the operator is computed by either an SMX, WRP, or CC when targeting CUDA – see Example 11). Also, we use the tags to define model-specific constraints in our formalism (as also discussed for low-level BUFs). We also tag the combine operator with a dimension of the ASM layer, enabling later in our optimization process to express advanced data access patterns (a.k.a. *swizzles* [Phothilimthana et al. 2019]). For example, when targeting CUDA, flexibly mapping ASM dimensions on CC layer (in CUDA terminology, the dimensions are called `threadIdx.x`, `threadIdx.y`, and `threadIdx.z`) to array dimensions enables the well-performing *coalesced global memory accesses* [NVIDIA 2022f] for both transposed and non-transposed data layouts, by only using different dimension tags.

Definition 14 (ASM Level)**.** We call pairs $(l_{\mathsf{ASM}}, d_{\mathsf{ASM}})$, consisting of an ASM layer $l_{\mathsf{ASM}} \in [1, L]_{\mathbb{N}}$ and an ASM dimension $d_{\mathsf{ASM}} \in [1, D]_{\mathbb{N}}$, an *ASM Level (*ASM-LVL[17]*)* (terminology motivated in the Appendix, Section C.5).

Definition 15 (Low-Level Combine Operator)**.** Let be $L \in \mathbb{N}$ (representing an ASM's number of layers) and $D \in \mathbb{N}$ (representing an MDH's number of dimensions). Let further be $\circledast \in \mathsf{CO}^{<\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}} \mid T \mid D \mid d>}$ an arbitrary D-dimensional combine operator (Definition 2).

The *low-level representation* $\circledast^{<(l_{\mathsf{ASM}}, d_{\mathsf{ASM}})\in\mathsf{ASM\text{-}LVL}>}$ of operator $\circledast$ is a function that for each pair

$$(l_{\mathsf{ASM}}, d_{\mathsf{ASM}}) \in \{\ (l, d) \mid l \in [1, L]_{\mathbb{N}},\ d \in [1, D]_{\mathbb{N}}\ \} \subset \mathsf{ASM\text{-}LVL}$$

has the same type and semantics as $\circledast$:

$$\circledast^{<l_{\mathsf{ASM}}, d_{\mathsf{ASM}}>} \in \mathsf{CO}^{<\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}} \mid T \mid D \mid d>} \quad , \quad \circledast^{<l_{\mathsf{ASM}}, d_{\mathsf{ASM}}>}(a, b) := \circledast(a, b)$$

i.e., $\circledast^{<l_{\mathsf{ASM}}, d_{\mathsf{ASM}}>}$ works exactly as combine operator $\circledast$, but its type is enriched with a meta-parameter that captures an ASM layer $l_{\mathsf{ASM}} \in [1, L]_{\mathbb{N}}$ and dimension $d_{\mathsf{ASM}} \in [1, D]_{\mathbb{N}}$.

Note that in Figure 17, for better readability, we use domain-specific identifiers for ASM layers: `HM:=1` as an alias for the ASM layer that has id 1, `L1:=2` for layer id 2, and `COR:=3` for layer id 3. For dimensions, we use aliases $x := 1$ for ASM dimension 1 and $y := 2$ for ASM dimension 2, correspondingly.

$$\mathfrak{b}_1^{\texttt{IB}}, \ldots, \mathfrak{b}_{B^{\texttt{IB}}}^{\texttt{IB}} \overset{\texttt{inp\_view}}{\mapsto} {}^{\downarrow}\mathfrak{a} \;=:$$

$$\begin{array}{ll}
\overset{\leftrightarrow_{\texttt{prt-ass}}(1,1)}{\#_1} & \overset{\leftrightarrow_{\texttt{prt-ass}}(1,\texttt{D})}{\#_D} \\
p_1^1 \in \#\texttt{PRT}(1,1) & p_{\texttt{D}}^1 \in \#\texttt{PRT}(1,\texttt{D}) \\
\rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{IB}} : {\downarrow}\text{-mem}(1,1)[\sigma_{\downarrow\text{-mem}}(1,1)(1), \ldots, \sigma_{\downarrow\text{-mem}}(1,1)(D_1^{\texttt{IB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}} : {\downarrow}\text{-mem}(1,1)[\sigma_{\downarrow\text{-mem}}(1,1)(1), \ldots, \sigma_{\downarrow\text{-mem}}(1,1)(D_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}})]\end{array}}_{\hookrightarrow\ \sigma_{\downarrow\text{-ord}}(1,1)} & \rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{IB}} : {\downarrow}\text{-mem}(1,D)[\sigma_{\downarrow\text{-mem}}(1,D)(1), \ldots, \sigma_{\downarrow\text{-mem}}(1,D)(D_1^{\texttt{IB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}} : {\downarrow}\text{-mem}(1,D)[\sigma_{\downarrow\text{-mem}}(1,D)(1), \ldots, \sigma_{\downarrow\text{-mem}}(1,D)(D_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}})]\end{array}}_{\hookrightarrow\ \sigma_{\downarrow\text{-ord}}(1,\texttt{D})} \\
\vdots & \vdots \\
\overset{\leftrightarrow_{\texttt{prt-ass}}(\texttt{L},1)}{\#_1} & \overset{\leftrightarrow_{\texttt{prt-ass}}(\texttt{L},\texttt{D})}{\#_D} \\
p_1^L \in \#\texttt{PRT}(\texttt{L},1) & p_{\texttt{D}}^L \in \#\texttt{PRT}(\texttt{L},\texttt{D}) \\
\rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{IB}} : {\downarrow}\text{-mem}(L,1)[\sigma_{\downarrow\text{-mem}}(L,1)(1), \ldots, \sigma_{\downarrow\text{-mem}}(L,1)(D_1^{\texttt{IB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}} : {\downarrow}\text{-mem}(L,1)[\sigma_{\downarrow\text{-mem}}(L,1)(1), \ldots, \sigma_{\downarrow\text{-mem}}(L,1)(D_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}})]\end{array}}_{\hookrightarrow\ \sigma_{\downarrow\text{-ord}}(\texttt{L},1)} & \rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{IB}} : {\downarrow}\text{-mem}(L,D)[\sigma_{\downarrow\text{-mem}}(L,D)(1), \ldots, \sigma_{\downarrow\text{-mem}}(L,D)(D_1^{\texttt{IB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}} : {\downarrow}\text{-mem}(L,D)[\sigma_{\downarrow\text{-mem}}(L,D)(1), \ldots, \sigma_{\downarrow\text{-mem}}(L,D)(D_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}})]\end{array}}_{\hookrightarrow\ \sigma_{\downarrow\text{-ord}}(\texttt{L},\texttt{D})}
\end{array}$$

$${}^{\downarrow}\mathfrak{a}_f^{<p_1^1, \ldots,\ p_D^1\ \mid\ \ldots\ \mid\ p_1^L, \ldots,\ p_D^L>}$$

(a) De-Composition Phase

$$\begin{array}{l}
{}^{\downarrow}\mathfrak{a}_f^{<p_1^1, \ldots,\ p_D^1\ \mid\ \ldots\ \mid\ p_1^L, \ldots,\ p_D^L>} \overset{\vec{f}}{\mapsto} {}^{\uparrow}\mathfrak{a}_f^{<p_1^1, \ldots,\ p_D^1\ \mid\ \ldots\ \mid\ p_1^L, \ldots,\ p_D^L>} \\
\quad \rightarrow < \ \sigma_{f\text{-ord}}(1,1)\ ,\ \ldots\ ,\ \sigma_{f\text{-ord}}(\texttt{L},\texttt{D})\ > \\
\quad \rightarrow < \leftrightarrow_{f\text{-ass}}(1,1)\ ,\ \ldots\ ,\ \leftrightarrow_{f\text{-ord}}(\texttt{L},\texttt{D})\ > \\
\rightarrow \quad \mathfrak{b}_1^{\texttt{IB}} :\ f^{\downarrow}\text{-mem}[\sigma_{f^{\downarrow}\text{-mem}}(1), \ldots, \sigma_{f^{\downarrow}\text{-mem}}(D_1^{\texttt{IB}})]\ ,\ \ldots\ ,\ \mathfrak{b}_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}} :\ f^{\downarrow}\text{-mem}[\sigma_{f^{\downarrow}\text{-mem}}(1), \ldots, \sigma_{f^{\downarrow}\text{-mem}}(D_{\texttt{B}^{\texttt{IB}}}^{\texttt{IB}})] \\
\rightarrow \quad \mathfrak{b}_1^{\texttt{OB}} :\ f^{\uparrow}\text{-mem}[\sigma_{f^{\uparrow}\text{-mem}}(1), \ldots, \sigma_{f^{\uparrow}\text{-mem}}(D_1^{\texttt{OB}})]\ ,\ \ldots\ ,\ \mathfrak{b}_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}} :\ f^{\uparrow}\text{-mem}[\sigma_{f^{\uparrow}\text{-mem}}(1), \ldots, \sigma_{f^{\uparrow}\text{-mem}}(D_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}})]
\end{array}$$

(b) Scalar Phase

$$\mathfrak{b}_1^{\texttt{OB}}, \ldots, \mathfrak{b}_{B^{\texttt{OB}}}^{\texttt{OB}} \overset{\texttt{out\_view}}{\leftarrow\!\!\shortmid} {}^{\uparrow}\mathfrak{a} \;:=$$

$$\begin{array}{ll}
\overset{\leftrightarrow_{\texttt{prt-ass}}(1,1)}{\circledast_1} & \overset{\leftrightarrow_{\texttt{prt-ass}}(1,\texttt{D})}{\circledast_D} \\
p_1^1 \in \#\texttt{PRT}(1,1) & p_{\texttt{D}}^1 \in \#\texttt{PRT}(1,\texttt{D}) \\
\rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{OB}} : {\uparrow}\text{-mem}(1,1)[\sigma_{\uparrow\text{-mem}}(1,1)(1), \ldots, \sigma_{\uparrow\text{-mem}}(1,1)(D_1^{\texttt{OB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}} : {\uparrow}\text{-mem}(1,1)[\sigma_{\uparrow\text{-mem}}(1,1)(1), \ldots, \sigma_{\uparrow\text{-mem}}(1,1)(D_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}})]\end{array}}_{\hookrightarrow\ \sigma_{\uparrow\text{-ord}}(1,1)} & \rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{OB}} : {\uparrow}\text{-mem}(1,D)[\sigma_{\uparrow\text{-mem}}(1,D)(1), \ldots, \sigma_{\uparrow\text{-mem}}(1,D)(D_1^{\texttt{OB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}} : {\uparrow}\text{-mem}(1,D)[\sigma_{\uparrow\text{-mem}}(1,D)(1), \ldots, \sigma_{\uparrow\text{-mem}}(1,D)(D_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}})]\end{array}}_{\hookrightarrow\ \sigma_{\uparrow\text{-ord}}(1,\texttt{D})} \\
\vdots & \vdots \\
\overset{\leftrightarrow_{\texttt{prt-ass}}(\texttt{L},1)}{\circledast_1} & \overset{\leftrightarrow_{\texttt{prt-ass}}(\texttt{L},\texttt{D})}{\circledast_D} \\
p_1^L \in \#\texttt{PRT}(\texttt{L},1) & p_{\texttt{D}}^L \in \#\texttt{PRT}(\texttt{L},\texttt{D}) \\
\rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{OB}} : {\uparrow}\text{-mem}(L,1)[\sigma_{\uparrow\text{-mem}}(L,1)(1), \ldots, \sigma_{\uparrow\text{-mem}}(L,1)(D_1^{\texttt{OB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}} : {\uparrow}\text{-mem}(L,1)[\sigma_{\uparrow\text{-mem}}(L,1)(1), \ldots, \sigma_{\uparrow\text{-mem}}(L,1)(D_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}})]\end{array}}_{\hookrightarrow\ \sigma_{\uparrow\text{-ord}}(\texttt{L},1)} & \rightarrow \underbrace{\begin{array}{l}\mathfrak{b}_1^{\texttt{OB}} : {\uparrow}\text{-mem}(L,D)[\sigma_{\uparrow\text{-mem}}(L,D)(1), \ldots, \sigma_{\uparrow\text{-mem}}(L,D)(D_1^{\texttt{OB}})] \\ \vdots \\ \mathfrak{b}_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}} : {\uparrow}\text{-mem}(L,D)[\sigma_{\uparrow\text{-mem}}(L,D)(1), \ldots, \sigma_{\uparrow\text{-mem}}(L,D)(D_{\texttt{B}^{\texttt{OB}}}^{\texttt{OB}})]\end{array}}_{\hookrightarrow\ \sigma_{\uparrow\text{-ord}}(\texttt{L},\texttt{D})}
\end{array}$$

$${}^{\uparrow}\mathfrak{a}_f^{<p_1^1, \ldots,\ p_D^1\ \mid\ \ldots\ \mid\ p_1^L, \ldots,\ p_D^L>}$$

(c) Re-Composition Phase

Fig. 19. Generic low-level expression for data-parallel computations

No.	Name	Range	Description
0	#PRT	MDH-LVL $\to \mathbb{N}$	number of parts
D1	$\sigma_{\downarrow\text{-ord}}$	MDH-LVL $\twoheadrightarrow$ MDH-LVL	de-composition order
D2	$\leftrightarrow_{\downarrow\text{-ass}}$	MDH-LVL $\twoheadrightarrow$ ASM-LVL	ASM assignment (de-composition)
D3	$\downarrow\text{-mem}^{\langle\text{ib}\rangle}$	MDH-LVL $\to$ MR	memory regions of input BUFs (ib)
D4	$\sigma^{\langle\text{ib}\rangle}_{\downarrow\text{-mem}}$	MDH-LVL $\to [1,\ldots,D^{\text{IB}}_{\text{ib}}]_{\mathcal{S}}$	memory layouts of input BUFs (ib)
S1	$\sigma_{f\text{-ord}}$	MDH-LVL $\twoheadrightarrow$ MDH-LVL	scalar function order
S2	$\leftrightarrow_{f\text{-ass}}$	MDH-LVL $\twoheadrightarrow$ ASM-LVL	ASM assignment (scalar function)
S3	$f^{\downarrow}\text{-mem}^{\langle\text{ib}\rangle}$	MR	memory region of input BUF (ib)
S4	$\sigma^{\langle\text{ib}\rangle}_{f^{\downarrow}\text{-mem}}$	$[1,\ldots,D^{\text{IB}}_{\text{ib}}]_{\mathcal{S}}$	memory layout of input BUF (ib)
S5	$f^{\uparrow}\text{-mem}^{\langle\text{ob}\rangle}$	MR	memory region of output BUF (ob)
S6	$\sigma^{\langle\text{ob}\rangle}_{f^{\uparrow}\text{-mem}}$	$[1,\ldots,D^{\text{OB}}_{\text{ob}}]_{\mathcal{S}}$	memory layout of output BUF (ob)
R1	$\sigma_{\uparrow\text{-ord}}$	MDH-LVL $\twoheadrightarrow$ MDH-LVL	re-composition order
R2	$\leftrightarrow_{\uparrow\text{-ass}}$	MDH-LVL $\twoheadrightarrow$ ASM-LVL	ASM assignment (re-composition)
R3	$\uparrow\text{-mem}^{\langle\text{ob}\rangle}$	MDH-LVL $\to$ MR	memory regions of output BUFs (ob)
R4	$\sigma^{\langle\text{ob}\rangle}_{\uparrow\text{-mem}}$	MDH-LVL $\to [1,\ldots,D^{\text{OB}}_{\text{ob}}]_{\mathcal{S}}$	memory layouts of output BUFs (ob)

Table 1. Tuning parameters of our low-level expressions

3.4 Generic Low-Level Expression

Figure 19 shows a generic expression in our low-level representation: it targets an arbitrary but fixed L-layered ASM instance, and it implements – on low level – the generic instance of our high-level expression in Figure 15. Inserting into the low-level expression a particular value for ASM's numbers of layer L, as well as particular values for the generic parameters of the high-level expression in Figure 15 (dimensionality D, combine operators $\otimes_1,\ldots,\otimes_d$, and input/output views) results in an instance of the expression in Figure 19 that remains generic in tuning parameters only; this auto-tunable instance will be the focus of our discussion in the remainder of this section.

In Section 4, we show that we fully automatically compute the auto-tunable low-level expression for a concrete ASM instance and high-level expression, and we automatically optimize this tunable

[17] For simplicity, we refrain from annotating identifier ASM-LVL with values L and D (e.g., $\text{ASM-LVL}^{\langle L,D\rangle}$), because both values will usually be clear from the context.

expression for a particular target device and characteristics of the input and output data using auto-tuning [Rasch et al. 2021]. Our final outcome is a concrete (non-generic) low-level expression (as in Figure 17) that is auto-tuned for the particular target device (represented via an ASM instance, e.g., ASM instance $\texttt{ASM}_{\texttt{CUDA}}$ when targeting an NVIDIA Ampere GPU) and high-level MDH expression; from this auto-tuned low-level expression, we can straightforwardly generate executable program code, because all the major optimization decisions have already been made in the previous auto-tuning step. Our overall approach is illustrated in Figure 4.

Auto-Tunable Parameters. Table 1 lists the tuning parameters of our auto-tunable low-level expressions. Different values of tuning parameters lead to semantically equal variants of the auto-tunable low-level expression (which we prove formally in Section 4), but the variants will be translated to differently optimized code variants.

In the following, we explain the 15 tuning parameters in Table 1. We give our explanations in a general, formal setting that is independent of a particular computation and programming model; the parameters are discussed afterwards for the concrete example computation *matrix multiplication* in models OpenMP, CUDA, and OpenCL.

In Table 1, we refer to combine operators in Figure 17 using pairs (l, d) to which we refer to as *MDH Levels (*`MDH-LVL`*)* (terminology motivated in the Appendix, Section C.6). We use the pairs as enumeration for operators in the de-composition or re-composition phase, respectively.

Definition 16 (MDH Level)**.** We define set `MDH-LVL` as:

$$\texttt{MDH-LVL} := \{\ (l, d) \mid l \in [1, L]_{\mathbb{N}}, d \in [1, D]_{\mathbb{N}}\}^{18}$$

For example, in the de-composition phase of Figure 17 (right part of the figure), pair $(1, 1) \in$ `MDH-LVL` points to the first combine operator, as the operator operates on the first layer $l = 1$ and in the first dimension $d = 1$ (discussed in Section 3.1). Analogously, pairs $(1, 2), (2, 1) \in$ `MDH-LVL` point to the second and third operator, etc. An operator's enumeration can be easily deduced from its corresponding p variable: the variable's superscript indicates the operator's corresponding layer l and the variable's subscript indicates its dimension d.

Our tuning parameters in Table 1 have constraints: 1) *algorithmic constraints* which have to be satisfied by all target programming models; 2) *model constraints* which are specific for particular programming models only (CUDA-specific constraints, OpenCL-specific constraints, etc), e.g., that the results of CUDA's thread blocks can only be combined in designated memory regions [NVIDIA 2022f]. We discuss algorithmic constraints in the following, together with our tuning parameters; model constraints are discussed in our Appendix, Section C.1, for the interested reader.

In the following, we present our 15 tuning parameters in Table 1. Dotted lines separate parameters for different phases: parameters `D1-D4` customize the de-composition phase, parameters `S1-S6` the scalar phase, and parameters `R1-R4` the re-composition phase, correspondingly; the parameter `0` impacts all three phases (separated by a straight line in the table).

Note that our parameters do not aim to introduce novel optimization techniques, but to unify, generalize, and combine together well-proven optimizations, based on a formal foundation, toward an efficient, overall optimization process that applies to various combinations of data-parallel computations, architectures, and characteristics of input and output data (e.g., their size and memory layout).

[18] The same as for identifier `ASM-LVL`, we refrain from annotating identifier `MDH-LVL` with values L and D. Note that `MDH-LVL` and `ASM-LVL` (Definition 15) both refer to the same set of pairs, but we use identifier `MDH-LVL` when referring to MDH levels and identifier `ASM-LVL` when referring to ASM levels, correspondingly, for better clarity.

Parameter `0`*:* Parameter `#PRT` is a function that maps pairs in `MDH-LVL` to natural numbers; the parameter determines *how much* data are grouped together into parts in our low-level expression in Figure 19 (and consequently also in our generated code later) by setting the particular number of parts (a.k.a. *tiles*) used in our expression. For example, in Figure 17, we use $\texttt{\#PRT}(1,1) := 2$ which causes combine operators $+\!\!+_1^{(\texttt{HM},\texttt{x})}$ and $\circledast_1^{(\texttt{HM},\texttt{x})}$ to iterate over interval $[0,2)_{\mathbb{N}_0}$, and we use $\texttt{\#PRT}(1,2) := 4$ to let operators $+\!\!+_2^{(\texttt{HM},\texttt{y})}$ and $\circledast_2^{(\texttt{HM},\texttt{x})}$ iterate over interval $[0,4)_{\mathbb{N}_0}$, etc.

To ensure a full partitioning (so that we obtain singleton MDAs in the scalar phase to which scalar function f can be applied, as discussed above), we require the following algorithmic constraint for the parameter:

$$\prod_{l \in [1,L]_{\mathbb{N}}} \texttt{\#PRT}(l,d) \;=\; N_d, \;\text{ for all } d \in [1,D]_{\mathbb{N}}$$

Here, N_d is the input size in dimension d (Figure 15).

In our generated code, the number of parts directly translates to the number of *tiles* which are computed either sequentially (a.k.a. *cache blocking* [Lam et al. 1991]) or in parallel in our code, depending on the combine operators's tags (which are chosen via Parameters `D2,S2,R2` as discussed soon). In our example from Figure 17, we process the parts belonging to combine operators tagged with `HM` and `L1` sequentially, via `for`-loops, because `HM` and `L1` correspond to ASM's memory layers (note that Parameter `0` only chooses the number of tiles; the parameter has no effect on explicitly copying data into fast memory resources, which is the purpose of Parameters `D3,R3,S1,S2`); `COR` parts are computed in parallel in our code, because `COR` corresponds to ASM's core layer, and thus, the number of `COR` parts determines the number of threads used in our generated code.

An optimized number of tiles is known to be essential for high performance [Bacon et al. 1994], e.g., due to its impact for locality-aware data accesses (number of sequentially computed tiles) and efficiently exploiting parallelism (number of tiles computed in parallel, which corresponds to the number of threads used in our generated code).

Parameters `D1,S1,R1`*:* These three parameters are permutations on `MDH-LVL`, determining *when* data is accessed and combined. The parameters specify the order (indicated by symbol $\hookrightarrow$ in Figure 19) of combine operators in the de-composition and re-composition phases (parameters `D1` and `R1`), and the order of applying scalar function f to parts (parameter `S1`). Thereby, the parameters specify when parts are processed during computation.

In our generated code, combine operators are implemented as sequential/parallel loops such that the parameters enable optimizing loop orders (a.k.a. *loop permutation* [McKinley et al. 1996]). For combine operators assigned (via parameter `R2`) to ASM's core layer and thus computed in parallel, parameter `R1` particularly determines when the computed results of threads are combined: if we used in the re-composition phase of Figure 17 combine operators tagged with `(COR,x)` and `(COR,y)` immediately after applying scalar function f (i.e., in steps ⑩ and ⑪, rather than steps ⑫ and ⑬), we would combine the computed intermediate results of threads multiple times, repeatedly after each individual computation step of threads, and using the two operators at the end of the re-composition phase (in steps ⑭ and ⑮) would combine the result of threads only once, at the end of the re-composition phase.

Note that each phase corresponds to an individual loop nest which we fuse together when parameters `D1,S1,R1` (as well as parameters `D2,S2,R2`) coincide.

Parameters `D2,S2,R2`*:* These parameters (symbol $\twoheadrightarrow$ in the table denotes bijection) map MDH levels to ASM levels, thereby determining *which* data is assigned to which ASM level (similar to the concept of `bind` in scheduling languages [Apache TVM Documentation 2022a]), by setting

the operators' tags. Consequently, the parameters determine which parts should be computed sequentially in our generated code and which parts in parallel. For example, in Figure 17, we use $\leftrightarrow_{\downarrow\texttt{-ass}}(2,1) := (\texttt{COR},\texttt{x})$ and $\leftrightarrow_{\downarrow\texttt{-ass}}(2,2) := (\texttt{COR},\texttt{y})$, thereby assigning the computation of MDA parts on layer 2 in both dimensions to ASM's COR layers in the de-composition phase, which causes processing the parts in parallel in our generated code. In CUDA-like approaches which have a notion of cores on multiple layers, the parameter particularly determines the thread layer to be used for parts computed in parallel (e.g., `block` or `thread` in CUDA).

Using these parameters, we are able to flexibly set data access patterns in our generated code. In Figure 17, we assign parts on layer 2 to COR layers, which results in a so-called block access pattern of cores: we start $8 * 16$ threads, according to the $8 * 16$ core parts, and each thread processes a part of the input MDA representing a block of 32×64 MDA elements within the input data. If we had assigned in the figure the first computation layer to ASM's COR layer (in the figure, this layer is assigned to ASM's HM layer), we would start $2 * 4$ threads and each thread would process MDA parts of size $(8 * 32) \times (16 * 64)$; assigning the last MDH layer to CORs would result in $(2 * 8 * 32) \times (4 * 16 * 64)$ threads each processing MDA parts containing a single MDA element only (a.k.a. *strided access*).

The parameters also enable expressing so-called *swizzle* access patterns [Phothilimthana et al. 2019]. For example, in CUDA, processing consecutive data elements in data dimension 1 by threads that are consecutive in thread dimension 2 (a.k.a `threadIdx.y` dimension in CUDA) can achieve higher performance due to the hardware design of fast memory resources in NVIDIA GPUs. Such swizzle patterns can be easily expressed and auto-tuned in our approach; for example, by interchanging in Figure 17 tags `(COR,x)` and `(COR,y)`. For memory layers (such as HM and L1), the dimension tags x and y currently have no effect on our generated code, as the programming models we target at the moment (OpenMP, CUDA, and OpenCL) have no explicit notion of tiles. However, this might change in the future when targeting new kinds of programming models, e.g., for upcoming architectures.

Parameters D3,R3 *and* S3,S5*:* Parameters D3 and R3 set for each BUF the memory region to use, thereby determining *where* data is read from or written to, respectively. In the table, we use $\texttt{ib} \in [1, B^{\texttt{IB}}]_{\mathbb{N}}$ to refer to a particular input BUF and $\texttt{ob} \in [1, B^{\texttt{OB}}]_{\mathbb{N}}$ to refer to an output BUF, correspondingly. Parameter D3 specifies the memory region to read from, and parameter R3 the regions to write to. The set $\texttt{MR} := [1, \texttt{NUM\_MEM\_LYRs}]_{\mathbb{N}}$ denotes the ASM's memory regions.

Similarly to parameters D3 and R3, parameters S3 and S5 set for scalar function f the memory regions for the input and output scalar.

Exploiting fast memory resources of architectures is a fundamental optimization [Bondhugula 2020; Hristea et al. 1997; Mei et al. 2014; Salvador Rohwedder et al. 2023], particularly due to the performance gap between processors' cores and their memory system [Oliveira et al. 2021; Wilkes 2001].

Parameters D4,R4 *and* S4,S6*:* These parameters set the memory layouts of BUFs, thereby determining *how* data is accessed in memory; for brevity in Table 1, we denote the set of all BUF permutations $[1, D]_{\mathbb{N}} \rightarrowtail\!\!\!\!\!\rightarrow [1, D]_{\mathbb{N}}$ (Definition 13) as $[1, \ldots, D]_{\mathcal{S}}$ (symbol $\mathcal{S}$ is taken from the notation of *symmetric groups* [Sagan 2001]). In the case of our matrix-vector multiplication example in Figure 17, we use a standard memory layout for all matrices, which we express via the parameters by setting them to the identity function, e.g., $\sigma^{\texttt{<M>}}_{\downarrow\texttt{-mem}}(1,1) := id$ (Parameter D4) for the matrix read by operator $+\!\!+_1^{(\texttt{HM},\texttt{x})}$.

An optimized memory layout is important to access data in a locality-aware and thus efficient manner.

3.5 Examples

Figures 20-23 show how our low-level representation is used for expressing the (de/re)-compositions of concrete, state-of-the-art implementations, using the popular example of matrix multiplication (`MatMul`) on a real-world input size taken from the `ResNet-50` [He et al. 2015] deep learning neural network (training phase). To challenge our formalism: i) we express implementations generated and optimized according to notably different approaches: scheduling approach TVM using its recent Ansor [Zheng et al. 2020a] optimization engine which is specifically designed and optimized toward deep learning computations; polyhedral compilers PPCG and Pluto with auto-tuned tile sizes; ii) we consider optimizations for two fundamentally different kinds of architectures: NVIDIA Ampere GPU and Intel Skylake CPU. We consider our study as challenging for our formalism, because it needs to express – in the same formal framework – the (de/re)-compositions of implementations generated and optimized according to notably different approaches (scheduling-based and polyhedral-based) and for significantly different kinds of architectures (GPU and CPU). Experimental results for TVM, PPCG, and Pluto (including the `MatMul` study used in this section) are presented and discussed in Section 5, as the focus of this section is on analyzing and discussing the expressivity of our low-level representation, rather than its experimental evaluation.

In Figures 20-23, we list our low-level representation's particular tuning parameter values for expressing the TVM- and PPCG/Pluto-generated implementations, which concisely describe the (de/re)-composition strategies used by TVM, PPCG and Pluto for `MatMul` on GPU or CPU for the ResNet-50's input size; inserting these tuning parameter values into our generic low-level expression in Figure 19 results in the formal representation of the (de/re)-composition strategies used by TVM, PPCG and Pluto.

In the following, we describe the columns of the tables in Figures 20-23, each of which listing particular values of tuning parameters in Table 1: column `0` in Figures 20-23 lists values of tuning parameter `0` in Table 1, column `D1` of tuning parameter `D1`, etc. As all four tables follow the same structure, we focus on describing the particular example table in Figure 20 (example chosen arbitrarily), which shows the (de/re)-composition used in TVM's generated CUDA code for `MatMul` on NVIDIA Ampere GPU using input matrices of sizes 16×2048 and 2048×1000 taken from ResNet-50[19]. Note that for clarity, we use in the figures domain-specific aliases, instead of numerical values, to better differentiate between different ASM layers and memory regions. For example, we use in Figure 20 as aliases `DEV` := 1, `SHR` := 2, and `REG` := 3 to refer to CUDA's three memory layers (device memory layer `DEV`, shared memory layer `SHR`, and register memory layer `REG`), and we use `DM` := 1, `SM` := 2, and `RM` := 3 to refer to CUDA's memory regions device `DM`, shared `SM`, and register `RM`; aliases `BLK` := 4 and `THR` := 5 refer to CUDA's core layers which are programmed via blocks and threads in CUDA. We differentiate between memory layers and memory regions for the following reason: for example, using tuning parameter `0` in Table 1, we partition input data hierarchically for each particular memory layer of the target architecture (sometime possibly into one part only, which is equivalent to not partitioning). However, depending on the value of tuning parameter `D3`, we do not necessarily copy the input's parts always into the corresponding memory regions (e.g., a part on `SHR` layer is not necessarily copied into shared memory `SM`), for example, when the architecture provides automatically managed memory regions (as caches in CPUs) or

[19] For the interested reader, TVM's corresponding, Ansor-generated scheduling program is presented in our Appendix, Section C.8.

when only some parts of the input are accessed multiple times (e.g., the input vector in the case of matrix-vector multiplication, but not the input matrix), etc.

Column `0`. The column lists the particular number of parts (a.k.a. *tiles*) used in TVM's multi-layered, multi-dimensional partitioning strategy for `MatMul` on the ResNet-50's input matrices of sizes 16×2048 and 2048×1000. We can observe from this column that the input MDA, which is initially of size $(16, 1000, 2048)$ for the ResNet-50's input matrices (follows from `MatMul`'s particular input view functions shown in Figure 16), is partitioned into $(2 * 50 * 1)$-many parts (indicated by the first three rows in column 1): 2 parts in the first dimension, 50 parts in the second dimension, and 1 part in the third dimension. Each of these parts is then further partitioned into $(2 * 1 * 8)$-many parts (rows 4,5,6), and these parts are again partitioned into $(4 * 20 * 1)$-many further parts (rows 7,8,9), etc.

Columns `D1`, `S1`, `R1`. These 3 columns describe the order in which parts are processed in the different phases: de-composition (column `D1`), scalar phase (column `S1`), and re-composition (column `R1`). For example, we can observe from column `R1` that TVM's CUDA code first combines parts on layer 1 in dimensions 1, 2, 3 (indicated via 1, 2, 3 in rows 1, 2, 3 of column `R1`); afterwards, parts on layer 3 in dimensions 1, 2, 3 are processed (indicated via 1, 2, 3 in rows 7, 8, 9 of column `R1`), etc.

Note that TVM uses the same order in all three phases (i.e., columns `D1`, `S1`, `R1` coincide). Most likely this is because in CUDA, iteration over memory tiles are programmed via for-loops such that columns `D1`, `S1`, `R1` represent loop orders – using the same order of loops in columns `D1`, `S1`, `R1` consequently allows TVM to generate the loop nests of the three different phases as fused, in one single loop nest (rather than three individual nests), which usually achieves high performance in CUDA.

Note further that the order of parts that are processed in parallel (columns `D2`, `S2`, `R2`, described in the next paragraph, determine if parts are processed in parallel or not) effects when results of blocks and threads are combined (a.k.a. *parallel reduction* [Harris et al. 2007]), e.g., early in the computation and thus often (but probably at the cost of low memory consumption) or late and thus only once (but requiring possibly more memory), etc.

Columns `D2`, `S2`, `R2`. The columns determine how computations are assigned to the target architecture. In our example in Figure 20, the $(2 * 50 * 1)$-many parts in the first partitioning layer (rows 1-3) are assigned to CUDA blocks (`BLK`); consequently, each such part is computed by an individual block (i.e., TVM uses a so-called *grid size* of `2,50,1` in its generated CUDA code for `MatMul`). The $(4 * 20 * 1)$-many parts in the third partitioning layer (rows 7-9) are processed by CUDA threads (`THR`) (i.e., the CUDA *block size* in the TVM-generated code is `4,20,1`). All other parts, e.g, those belonging to the $(2 * 1 * 8)$-many parts in the second partitioning layer (rows 4-6), are assigned to CUDA's memory layers (denoted as `DEV`, `SHR`, `REG` in Figure 20) and thus processed sequentially, via for-loops.

Columns `D3`, `S3`, `S5`, `R3`. While column `0` sets the multi-layered, multi-dimensional partitioning strategy used in TVM's CUDA code (according to the CUDA model's multi-layered memory and core hierarchies, shown in Example 11), column `0` does not indicate how CUDA's fast memory regions are exploited in the TVM-generated CUDA code for `MatMul` – column `0` only describes TVM's partitioning of the input/output computations such that parts of the input and output data can potentially fit into fast memory resources.

The actual assignment of parts to memory regions is set via columns `D3` (memory regions to be used for input data), columns `S3` and `S5` (memory regions to be used for the scalar computations), and column `R3` (memory regions to be used for storing the computed output data). For example, column `D3` indicates that in TVM's CUDA code for `MatMul`, parts of the A and B input matrices are

stored in CUDA's fast shared memory SM (rows 10-15), and column R3 indicates that each thread computes its results within CUDA's faster register memory RM (rows 10-15).

Our flexibility of separating the tiling strategy (Parameter 0) from the actual usage of memory regions (columns D3, S3, S5, R3) allows us, for example, to store parts belonging to one input buffer into fast memory resources (e.g., the input vector of matrix-vector multiplication, whose values are accessed multiple times), but not parts of other buffers (e.g., the input matrix of matrix-vector multiplication, whose values are accessed only once) or only subparts of buffers, etc.

Note that in the case of Figure 23 which shows Pluto's (de/re)-composition for OpenMP code, the memory tags in columns D3, S3, S5, R3 have no effect on the generated code: OpenMP relies on its target device's implicit memory management mechanism (e.g., CPU caches), rather than exposing the memory hierarchy explicitly to the programmer. Consequently, the memory tags are ignored by our OpenMP code generator and only emphasize the implementer's intention, e.g., that in Figure 23, each of the $(2 * 962 * 218)$-many tiles (rows 7-9) are intended by the implementer to be processed in L2 memory (even though this decision is eventually made automatically in the CPU hardware's automatic cache engine).

Columns D4, S4, S6, R4. These columns set the memory layout to be used for memory allocations in the CUDA code. TVM choses in all cases CUDA's standard transpositions layout (indicated by [1,2], called *row-major* layout, instead of [2,1] which is known as *column-major*). Since the same layout and memory region is used on consecutive layers, the same memory allocation is re-used in the CUDA code. For example, only one memory region is allocated in shared memory for input buffer A; the region is accessed in the computations of all SHR, REG tiles as well as CC tiles in dimensions x and z. Similarly, only one region is allocated in register memory for computing the results of SHR, REG, and DEV tiles.

TVM's (de/re)-composition for MatMul in CUDA on NVIDIA Ampere GPU

Part.	*De-Comp. Phase*					*Scalar Phase*						*Re-Comp. Phase*			
0	D1	D2	D3		D4	S1	S2	S3		S4	S5	S6	R1	R2	R3	R4
			A	B	A,B			A	B	A,B	C	C			C	C
2	1	BLK,y	DM	DM	[1,2]	1	BLK,y						1	BLK,y	DM	[1,2]
50	2	BLK,x	DM	DM	[1,2]	2	BLK,x						2	BLK,x	DM	[1,2]
1	3	BLK,z	DM	DM	[1,2]	3	BLK,z						3	BLK,z	DM	[1,2]
2	14	DEV,x	SM	SM	[1,2]	14	DEV,x						14	DEV,x	RM	[1,2]
1	15	DEV,y	SM	SM	[1,2]	15	DEV,y						15	DEV,y	RM	[1,2]
8	7	DEV,z	DM	DM	[1,2]	7	DEV,z						7	DEV,z	RM	[1,2]
4	4	THR,y	DM	DM	[1,2]	4	THR,y						4	THR,y	DM	[1,2]
20	5	THR,x	DM	DM	[1,2]	5	THR,x	RM	RM	[1,2]	RM	[1,2]	5	THR,x	DM	[1,2]
1	6	THR,z	DM	DM	[1,2]	6	THR,z						6	THR,z	DM	[1,2]
1	9	SHR,x	SM	SM	[1,2]	9	SHR,x						9	SHR,x	RM	[1,2]
1	10	SHR,y	SM	SM	[1,2]	10	SHR,y						10	SHR,y	RM	[1,2]
128	8	SHR,z	SM	SM	[1,2]	8	SHR,z						8	SHR,z	RM	[1,2]
1	12	REG,x	SM	SM	[1,2]	12	REG,x						12	REG,x	RM	[1,2]
1	13	REG,y	SM	SM	[1,2]	13	REG,y						13	REG,y	RM	[1,2]
2	11	REG,z	SM	SM	[1,2]	11	REG,z						11	REG,z	RM	[1,2]

Fig. 20. TVM's (de/re)-composition for MatMul in CUDA on GPU expressed in our low-level representation

TVM's (de/re)-composition for MatMul in OpenCL on Intel Skylake CPU

Part.	*De-Comp. Phase*					*Scalar Phase*						*Re-Comp. Phase*			
0	D1	D2	D3		D4	S1	S2	S3		S4	S5	S6	R1	R2	R3	R4
			A	B	A,B			A	B	A,B	C	C			C	C
1	1	WG,1	GM	GM	[1,2]	1	WG,1						1	WG,1	GM	[1,2]
125	2	WG,0	GM	GM	[1,2]	2	WG,0						2	WG,0	GM	[1,2]
1	3	WG,2	GM	GM	[1,2]	3	WG,2						3	WG,2	GM	[1,2]
1	14	GLB,0	LM	LM	[1,2]	14	GLB,0						14	GLB,0	PM	[1,2]
1	15	GLB,1	LM	LM	[1,2]	15	GLB,1						15	GLB,1	PM	[1,2]
16	7	GLB,2	GM	GM	[1,2]	7	GLB,2						7	GLB,2	PM	[1,2]
16	4	WI,1	GM	GM	[1,2]	4	WI,1						4	WI,1	GM	[1,2]
1	5	WI,0	GM	GM	[1,2]	5	WI,0	PM	PM	[1,2]	PM	[1,2]	5	WI,0	GM	[1,2]
1	6	WI,2	GM	GM	[1,2]	6	WI,2						6	WI,2	GM	[1,2]
1	9	LCL,0	LM	LM	[1,2]	9	LCL,0						9	LCL,0	PM	[1,2]
1	10	LCL,1	LM	LM	[1,2]	10	LCL,1						10	LCL,1	PM	[1,2]
128	8	LCL,2	LM	LM	[1,2]	8	LCL,2						8	LCL,2	PM	[1,2]
1	12	PRV,0	LM	LM	[1,2]	12	PRV,0						12	PRV,0	PM	[1,2]
8	13	PRV,1	LM	LM	[1,2]	13	PRV,1						13	PRV,1	PM	[1,2]
1	11	PRV,2	LM	LM	[1,2]	11	PRV,2						11	PRV,2	PM	[1,2]

Fig. 21. TVM's (de/re)-composition for `MatMul` in OpenCL on CPU expressed in our low-level representation

PPCG's (de/re)-composition for MatMul in CUDA on NVIDIA Ampere GPU

Part.	*De-Comp. Phase*					*Scalar Phase*						*Re-Comp. Phase*			
0	D1	D2	D3		D4	S1	S2	S3		S4	S5	S6	R1	R2	R3	R4
			A	B	A,B			A	B	A,B	C	C			C	C
16	1	BLK,y	DM	DM	[1,2]	1	BLK,y						1	BLK,y	DM	[1,2]
8	2	BLK,x	DM	DM	[1,2]	2	BLK,x						2	BLK,x	DM	[1,2]
1	3	BLK,z	DM	DM	[1,2]	3	BLK,z						3	BLK,z	DM	[1,2]
1	7	DEV,x	DM	DM	[1,2]	7	DEV,x						7	DEV,x	DM	[1,2]
1	8	DEV,y	DM	DM	[1,2]	8	DEV,y						8	DEV,y	DM	[1,2]
1	9	DEV,z	DM	DM	[1,2]	9	DEV,z						9	DEV,z	DM	[1,2]
1	4	THR,y	DM	DM	[1,2]	4	THR,y						4	THR,y	RM	[1,2]
125	5	THR,x	DM	DM	[1,2]	5	THR,x	RM	RM	[1,2]	RM	[1,2]	5	THR,x	RM	[1,2]
1	6	THR,z	DM	DM	[1,2]	6	THR,z						6	THR,z	RM	[1,2]
1	10	SHR,x	SM	DM	[1,2]	10	SHR,x						10	SHR,x	RM	[1,2]
1	11	SHR,y	SM	DM	[1,2]	11	SHR,y						11	SHR,y	RM	[1,2]
1181	12	SHR,z	SM	DM	[1,2]	12	SHR,z						12	SHR,z	RM	[1,2]
1	13	REG,x	SM	DM	[1,2]	13	REG,x						13	REG,x	RM	[1,2]
1	14	REG,y	SM	DM	[1,2]	14	REG,y						14	REG,y	RM	[1,2]
1	15	REG,z	SM	DM	[1,2]	15	REG,z						15	REG,z	RM	[1,2]

Fig. 22. PPCG's (de/re)-composition for `MatMul` in CUDA on GPU expressed in our low-level representation

Pluto's (de/re)-composition for MatMul in OpenMP on Intel Skylake CPU

Part.	*De-Comp. Phase*					*Scalar Phase*						*Re-Comp. Phase*			
0	D1	D2	D3		D4	S1	S2	S3		S4	S5	S6	R1	R2	R3	R4
			A	B	A,B			A	B	A,B	C	C			C	C
8	1	COR,0	MM	MM	[1,2]	1	COR,0						1	COR,0	MM	[1,2]
1	2	COR,1	MM	MM	[1,2]	2	COR,1						2	COR,1	MM	[1,2]
1	3	COR,2	MM	MM	[1,2]	3	COR,2						3	COR,2	MM	[1,2]
1	4	MM,0	MM	MM	[1,2]	4	MM,0						4	MM,0	MM	[1,2]
1	5	MM,1	MM	MM	[1,2]	5	MM,1						5	MM,1	MM	[1,2]
9	6	MM,2	MM	MM	[1,2]	6	MM,2						6	MM,2	MM	[1,2]
2	7	L2,0	L2	L2	[1,2]	7	L2,0						7	L2,0	L2	[1,2]
962	8	L2,1	L2	L2	[1,2]	8	L2,1	L1	L1	[1,2]	L1	[1,2]	8	L2,1	L2	[1,2]
218	9	L2,2	L2	L2	[1,2]	9	L2,2						9	L2,2	L2	[1,2]
1	10	L1,0	L1	L1	[1,2]	10	L1,0						10	L1,0	L1	[1,2]
1	11	L1,1	L1	L1	[1,2]	11	L1,1						11	L1,1	L1	[1,2]
1	12	L1,2	L1	L1	[1,2]	12	L1,2						12	L1,2	L1	[1,2]

Fig. 23. Pluto's (de/re)-composition for `MatMul` in OpenMP on CPU expressed in our low-level representation

4 LOWERING: FROM HIGH LEVEL TO LOW LEVEL

We have designed our formalism such that an expression in our high-level representation (such as in Figure 6) can be systematically lowered to an expression in our low-level representation (as in Figure 17). We confirm this by parameterizing the high-level expression in Figure 15 – step-by-step – in the tuning parameters listed in Table 1, in a formally sound manner, which results exactly in the low-level expression in Figure 19.

Parameter `0`. According to Definition 12, we use the L-layered, D-dimensional, P-partitioned low-level representation ${}^{\downarrow}\mathfrak{a}_f$ of $\mathfrak{a}$ for

$$P := \Big(\underbrace{\underbrace{(\#\mathsf{PRT}(1,1), \ldots, \#\mathsf{PRT}(1,D))}_{\text{Dimension 1}} \; , \ldots , \underbrace{(\#\mathsf{PRT}(L,1), \ldots, \#\mathsf{PRT}(L,D))}_{\text{Dimension } D}}_{\text{Layer 1}} \; , \ldots , \underbrace{\underbrace{(\#\mathsf{PRT}(L,1), \ldots, \#\mathsf{PRT}(L,D))}_{\text{Dimension 1}} \; \underbrace{\#\mathsf{PRT}(L,D))}_{\text{Dimension } D}}_{\text{Layer } L} \Big)$$

where #PRT denotes the number of partitions (Parameter `0` in Table 1).

Applying the homomorphic property (Definition 4) $L * D$ times, we get:

$$\mathsf{md\_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, a \,) \;=$$

$$\underbrace{\underbrace{\overset{\circledast_1}{p_1^1 \in \#\mathsf{PRT}(1,1)} \; \cdots \; \overset{\circledast_D}{p_D^1 \in \#\mathsf{PRT}(1,D)}}_{\text{Dimension 1}} \; \cdots \; \underbrace{\overset{\circledast_1}{p_1^L \in \#\mathsf{PRT}(L,1)} \; \cdots \; \overset{\circledast_D}{p_D^L \in \#\mathsf{PRT}(L,D)}}_{\text{Dimension } D}}_{\text{Layer 1}} \qquad \underbrace{\qquad\qquad\qquad\qquad}_{\text{Layer } L}$$

$$\mathsf{md\_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, {}^{\downarrow}\mathfrak{a}_f^{<p_1^1, \ldots, p_D^1 \mid \ldots \mid p_1^L, \ldots, p_D^L>} \,)$$

where ${}^{\downarrow}\mathfrak{a}_f^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>}$ is defined as:

$$
{}^{\downarrow}\mathfrak{a}_f \;=:\; \underbrace{\underbrace{\underbrace{+\!\!+_1}_{p_1^1 \in P_1^1} \;\ldots\; \underbrace{+\!\!+_D}_{p_D^1 \in P_D^1}}_{\text{Dimension 1}} \;\ldots\; \underbrace{\underbrace{+\!\!+_1}_{p_1^L \in P_1^L} \;\ldots\; \underbrace{+\!\!+_D}_{p_D^L \in P_D^L}}_{\text{Dimension 1}}}_{\text{Layer 1}} \qquad \underbrace{\qquad\qquad\qquad\qquad\qquad\qquad}_{\text{Dimension } D}}_{\text{Layer } L} \qquad {}^{\downarrow}\mathfrak{a}_f^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>}
$$

Since each part ${}^{\downarrow}\mathfrak{a}_f^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>}$ contains a single scalar value only (according to the algorithmic constraint of Parameter 1, discussed in Section 3.4), it holds

$$
\texttt{md\_hom}(\, f \,,\, (\circledast_1,\ldots,\circledast_D)\,)(\, {}^{\downarrow}\mathfrak{a}_f^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>}\,) = \vec{f}(\, {}^{\downarrow}\mathfrak{a}_f^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>}\,)
$$

for $\vec{f}$ defined as in Definition 4. □

Parameter D1. Parameter D1 reorders concatenation operators $+\!\!+_1,\ldots,+\!\!+_D$ (Example 1) which are of types $+\!\!+_d \in \texttt{CO}^{<id\,|\,T\,|\,D\,|\,d>}$ for arbitrary but fixed $T \in \texttt{TYPE}$ and $D \in \mathbb{N}$. We prove our assumption w.l.o.g. for the case $D = 2$; the general case $D \in \mathbb{N}$ follows analogously.

Let $+\!\!+_{d_1} \in \texttt{CO}^{<id\,|\,T\,|\,D\,|\,d_1>}$ and $+\!\!+_{d_2} \in \texttt{CO}^{<id\,|\,T\,|\,D\,|\,d_2>}$ be two arbitrary concatenation operators that coincide in meta-parameters T and D, but may differ in their operating dimensions d_1 and d_2. We have to show

$$
(a_1 +\!\!+_{d_1} a_2) +\!\!+_{d_2} (a_3 +\!\!+_{d_1} a_4) \;=\; (a_1 +\!\!+_{d_2} a_3) +\!\!+_{d_1} (a_2 +\!\!+_{d_2} a_4)
$$

which follows from the definition of the concatenation operator $+\!\!+$ in Example 1. □

Parameters D2, S2, R2. These parameters replaces combine operators (Definition 2) by low-level combine operators (Definition 15) which has no effect on semantics. □

Parameters D3, S3, S5, R3. These parameters set the memory tags of low-level BUFs (Definition 13), which have no effect on semantics. □

Parameters D4, S4, S6, R4. The parameters change the memory layout of low-level BUFs (Definition 13), which does not affect extensional equality. □

Parameters S1. This parameter sets the order in which function f is applied to parts, which is trivially sound for any order. □

Parameters R1. Similarly to parameter D1, parameter R1 reorders combine operators $\circledast_1,\ldots,\circledast_D$. In contrast to parameter D1, the combine operators reordered by parameter R1 are not restricted to be concatenation.

We prove our assumption by exploiting the MDH property (Definition 3) together with the proof of parameter D1, as follows:

$$
\begin{array}{lll}
 & & (a_1 \;\circledast_{d_1}\; a_2) \;\circledast_{d_2}\; (a_3 \;\circledast_{d_1}\; a_4) \\
= & \texttt{md\_hom}(\ldots)(& (a_1 \;+\!\!+_{d_1}\; a_2) \;+\!\!+_{d_2}\; (a_3 \;+\!\!+_{d_1}\; a_4) \quad) \\
= & \texttt{md\_hom}(\ldots)(& (a_1 \;+\!\!+_{d_2}\; a_3) \;+\!\!+_{d_1}\; (a_2 \;+\!\!+_{d_2}\; a_4) \quad) \\
= & & (a_1 \;\circledast_{d_2}\; a_3) \;\circledast_{d_1}\; (a_2 \;\circledast_{d_2}\; a_4) \quad \checkmark
\end{array}
$$

□

5 EXPERIMENTAL RESULTS

All experiments described in this section can be reproduced using [TOPLAS Artifact 2022].

We experimentally evaluate our approach by comparing it to popular representatives of four important classes:

(1) *scheduling approach*: TVM [Chen et al. 2018a] which generates GPU and CPU code from programs expressed in TVM's high-level program representation;
(2) *polyhedral compilers*: PPCG [Verdoolaege et al. 2013] for GPUs[20] and Pluto [Bondhugula et al. 2008b] for CPUs, which automatically generate executable program code in CUDA (PPCG) or OpenMP (Pluto) from straightforward, unoptimized C programs;
(3) *functional approach*: Lift [Steuwer et al. 2015] which generates OpenCL code from a Lift-specific, functional program representation;
(4) *domain-specific libraries*: NVIDIA cuBLAS [NVIDIA 2022b] and NVIDIA cuDNN [NVIDIA 2022e], as well as Intel oneMKL [Intel 2022c] and Intel oneDNN [Intel 2022b], which offer the user easy-to-use, domain-specific building blocks for programming. The libraries internally rely on pre-implemented assembly code that is optimized by experts for their target application domains: linear algebra (cuBLAS and oneMKL) or convolutions (cuDNN and oneDNN), respectively. To make comparison against the libraries challenging for us, we compare to all routines provided by the libraries. For example, the cuBLAS library offers three, semantically equal but differently optimized routines for computing `MatMul`: `cublasSgemm` (the default `MatMul` implementation in cuBLAS), `cublasGemmEx` which is part of the `cuBLASEx` extension of cuBLAS [NVIDIA 2022c], and the most recent `cublasLtMatmul` which is part of the `cuBLASLt` extension [NVIDIA 2022d]; each of these three routines may perform differently on different problem sizes (NVIDIA usually recommends to naively test which one performs best for the particular target problem). To make comparison further challenging for us, we exhaustively test for each routine all of its so-called `cublasGemmAlgo_t` variants, and report the routine's runtime for the best performing variant only. In the case of oneMKL, we compare also to its *JIT engine* [Intel 2019] which is specifically designed and optimized toward for small problem sizes. We also compare to library *EKR* [Hentschel et al. 2008] which computes data mining example `PRL` (Figure 16) on CPUs – the library is implemented in the Java programming language and parallelized via *Java Threads*, and the library is used in practice by the *Epidemiological Cancer Registry* in North Rhine-Westphalia (Germany) which is the currently largest cancer registry in Europe.

We compare to the approaches experimentally in terms of:

i) *performance*: via a runtime comparison of our generated code against code that is generated according to the related approaches;
ii) *portability*: based on the *Pennycook Metric* [Pennycook et al. 2019] which mathematically defines portability[21] as:

$$\Phi(a,p,H) = \begin{cases} \frac{|H|}{\sum_{i \in H} \frac{1}{e_i(a,p)}} & \text{if } i \text{ is supported, } \forall i \in H \\ 0 & \text{otherwise} \end{cases}$$

[20] We cannot compare to polyhedral compiler TC [Vasilache et al. 2019] which is optimized toward deep learning computations on GPUs, because TC is not under active development anymore and thus is not working for newer CUDA architectures [Facebook Research 2022]. Rasch et al. [2019a] show that our approach – already in its proof-of-concept version – achieves higher performance than TC for popular computations on real-world data sets.
[21] Pennycook's metric is actually called *Performance Portability (PP)*. Since performance portability particularly includes functional portability, we refer to Pennycook's PP also more generally as *Portability* only.

In words: "for a given set of platforms H, the *performance portability* Φ of an application a solving problem p is defined as $\Phi(a, p, H)$, where $e_i(a, p)$ is the performance efficiency (i.e. a ratio of observed performance relative to some proven, achievable level of performance) of application a solving problem p on platform i; value $\Phi(a, p, H)$ is 0, if any platform in H is unsupported by a running p." [Pennycook et al. 2019]. Consequently, Pennycook defines portability as a real value in the interval $[0, 1]_{\mathbb{R}}$ such that a value close to 1 indicates *high* portability and a value close to 0 indicates *low* portability. Here, platforms H represents a set of devices (CPUs, GPUs, ...), an application a is in our context a framework (such as TVM, a polyhedral compiler, or our approach), problems p are our case studies, and $e_i(a, p)$ is computed as the runtime $a^{\text{best}}_{p,i}$ of the application that achieves the best observed runtime for problem p on platform i, divided by the runtime of application a for problem p running on platform i.

iii) *productivity*: by intuitively arguing that our approach achieves the same/lower/higher productivity as the related approaches, using the representative example computation *Matrix-Vector Multiplication (*`MatVec`*)* (Figure 6) – classical code metrics, like *Lines of Code (LOC)*, COCOMO [Boehm et al. 1995], McCabe's cyclomatic complexity [McCabe 1976], and Halstead development effort [Halstead 1977] are not meaningful for comparing the short and concise programs in high-level languages as proposed by the related work as well as our approach.

In the following, after discussing our application case studies, experimental setup, auto-tuning system, and code generator, we compare our approach to each of the four above mentioned classes of approaches in Sections 5.1-5.4.

Application Case Studies

We use for experiments in this section popular example computations from Figure 16 that belong to different classes of computations:

- Linear Algebra Subroutines (BLAS): *Matrix Multiplication* (`MatMul`) and *Matrix-Vector Multiplication* (`MatVec`);
- Stencil Computations: *Jacobi Computation* (`Jacobi3D`) and *Gaussian Convolution* (`Conv2D`) which differ from linear algebra routines by accessing neighboring elements in their input data;
- Quantum Chemistry: *Coupled Cluster (*`CCSD(T)`*)* computations which differ from linear algebra routines and stencil computations by accessing their high-dimensional input data in complex, transposed fashions;
- Data Mining: *Probabilistic Record Linkage* (`PRL`) which differs from the previous computations by relying on a PRL-specific combine operator and scalar function, instead of straightforward additions or multiplications as previous computations;
- Deep Learning: the most time-intensive computations within the popular neural networks `ResNet-50` [He et al. 2015], `VGG-16` [Simonyan and Zisserman 2014], and `MobileNet` [Howard et al. 2017], according to their TensorFlow implementations [TensorFlow 2022a,b,c]. Deep learning computations rely on advanced variants of linear algebra routines and stencil computations, e.g., `MCC` and `MCC_Capsule` for computing convolution-like stencils, instead of the classical `Conv2D` variant of convolution (Figure 16) – the deep learning variants are considered as significantly more challenging to optimize than their classical variants [Barham and Isard 2019].

We use for experiments this subset of computations from Figure 16 to make experimenting challenging for us: state-of-practice approaches, such as TVM and vendor libraries from NVIDIA and Intel, are specifically designed and optimized toward these computations. To make experimenting

further challenging for us, we consider data sizes and characteristics either taken from real-world computations (e.g., from the *TCCG* benchmark suite [Springer and Bientinesi 2016] for quantum chemistry computations) or sizes that are preferable for our competitors, e.g., powers of two for which many competitors are highly optimized, e.g., vendor libraries. For the deep learning case studies, we use data characteristics (sizes, strides, padding strategy, image/filter formats, etc.) taken from the particular implementations of the neural networks when computing the popular *ImageNet* [Krizhevsky et al. 2012] data set (the particular characteristics are listed in our Appendix, Section D.1, for the interested reader). For all experiments, we use single precision floating point numbers (a.k.a. `float` or `fp32`), as such precision is the default in TensorFlow and many other frameworks.

Experimental Setup

We run our experiments on a cluster containing two different kinds of GPUs and CPUs:

- `NVIDIA Ampere GPU A100-PCIE-40GB`
- `NVIDIA Volta GPU V100-SXM2-16GB`
- `Intel Xeon Broadwell CPU E5-2683 v4 @ 2.10GHz`
- `Intel Xeon Skylake CPU Gold-6140 @ 2.30GHz`

We represent the two CUDA GPUs in our formalism using model $\texttt{ASM}_{\texttt{CUDA+WRP}}$ (Example 11). We rely on model $\texttt{ASM}_{\texttt{CUDA+WRP}}$, rather than the CUDA's standard model $\texttt{ASM}_{\texttt{CUDA}}$ (also in Example 11), in order to exploit CUDA's (implicit) warp level for a fair comparison to competitors: warp-level optimizations are exploited by our competitors, e.g., for *shuffle operations* [NVIDIA 2018] which combine the results of threads within a warp with high performance. To fairly compare to TVM and PPCG, we avoid exploiting warps' *tensor core intrinsics* [NVIDIA 2017] in all experiments, which compute the multiplication of small matrices with high performance [Feng et al. 2022], because these intrinsics are not used in the TVM- and PPCG-generated CUDA code. For the two CPUs, we rely on model $\texttt{ASM}_{\texttt{OpenCL}}$ (Example 11) for generating OpenCL code. The same as our approach, TVM also generates OpenCL code for CPUs; Pluto relies on the OpenMP approach for CPUs.

For all experiments, we use the currently newest versions of frameworks, libraries, and compilers, as follows. We compile our generated GPU code using library `CUDA NVRTC` [NVIDIA 2022h] from `CUDA Toolkit 11.4`, and we use `Intel's OpenCL runtime` version `18.1.0.0920` for compiling CPU code. For both compilers, we do not set any flags so that they run in their default modes. For the related approaches, we use the following versions of frameworks, libraries, and compilers:

- `TVM` [Apache 2022] version `0.8.0` which also uses our system's `CUDA Toolkit` version `11.4` for GPU computations and `Intel's runtime` version `18.1.0.0920` for computations on CPU;
- `PPCG` [Michael Kruse 2022] version `0.08.04` using flag `--target=cuda` for generating CUDA code, rather than OpenCL, as CUDA is usually better performing than OpenCL on NVIDIA GPUs, and we use flag `--sizes` followed by auto-tuned tile sizes – we rely on the *Auto-Tuning Framework (ATF)* [Rasch et al. 2021] for choosing optimized tile size values (as we discuss in the next subsection);
- `Pluto` [Uday Bondhugula 2022] commit `12e075a` using flag `--parallel` for generating OpenMP-parallelized C code (rather than sequential C), as well as flag `--tile` to use ATF-tuned tile sizes for `Pluto`; the `Pluto`-generated OpenMP code is compiled via `Intel's icx` compiler version `2022.0.0` using the `Pluto`-recommended optimization flags `-O3 -qopenmp`;
- `NVIDIA cuBLAS` [NVIDIA 2022b] from `CUDA Toolkit 11.4`, using the NVIDIA-recommended compiler flags `-fast -O3 -DNDEBUG`;

- NVIDIA cuDNN [NVIDIA 2022e] from CUDA Toolkit 11.4, using the NVIDIA-recommended compiler flags -fast -O3 -DNDEBUG;
- Intel oneMKL [Intel 2022c] compiled with Intel's icpx compiler version 2022.0.0, using flags -DMKL_ILP64 -qmkl=parallel -L${MKLROOT}/lib/intel64 -liomp5 -lpthread -lm -ldl, as recommended for oneMKL by Intel's *Link Line Advisor* tool [Intel 2022a], as well as standard flags -O3 -NDEBUG;
- Intel oneDNN [Intel 2022b] also compiled with Intel's icpx compiler version 2022.0.0, using flags -I${DNNLROOT}/include -L${DNNLROOT}/lib -ldnnl, according to oneDNN's documentation, as well as standard flags -O3 -NDEBUG;
- EKR [Hentschel et al. 2008] executed via Java SE 1.8.0 Update 281.

We profile runtimes of CUDA and OpenCL programs using the corresponding, event-based profiling APIs provided by CUDA and OpenCL. For Pluto which generates OpenMP-annotated C code, we measure runtimes via system call clock_gettime [GNU/Linux 2022]. In the case of C++ libraries Intel oneMKL and Intel oneDNN, we use C++'s chrono library [C++ reference 2022]. Libraries NVIDIA cuBLAS and NVIDIA cuDNN are also based on the CUDA programming model; thus, we profile them also via CUDA events. To measure the runtimes of the EKR Java library, we use Java function System.currentTimeMillis().

All measurements of CUDA and OpenCL programs contain the pure program runtime only (a.k.a. *kernel runtime*). The runtime of *host code*[22] is not included in the reported runtimes, as performance of host code is not relevant for this work and the same for all approaches.

In all experiments, we collect measurements until the 99% confidence interval was within 5% of our reported means, according to the guidelines for *scientific benchmarking of parallel computing systems* by Hoefler and Belli [2015].

Auto-Tuning

The auto-tuning process of our approach relies completely on the generic *Auto Tuning Framework (ATF)* [Rasch et al. 2021]. The ATF framework has proven to be efficient for exploring large search spaces that are based on constrained tuning parameters (as our space introduced in Section 3.4). We use ATF, out of the box, exactly as described by Rasch et al. [2021]: 1) we straightforwardly represent in ATF our search space (Table 1) via *tuning parameters* which express the parameters in the table and their constraints; 2) we use ATF's pre-implemented cost functions for CUDA and OpenCL to measure the cost of our generated OpenCL and CUDA codes (in this work, we consider as cost program's runtime, rather than its energy consumption, etc); 3) we start the tuning process using ATF's default search technique (*AUC bandit* [Ansel et al. 2014]). ATF then fully automatically determines a well-performing tuning parameter configuration for the particular combination of a case study, architecture, and input/output characteristics (size, memory layout, etc).

For scheduling approach TVM, we use its Ansor [Zheng et al. 2020a] optimization engine which is specifically designed and optimized toward generating optimized TVM schedules. Polyhedral compilers PPCG and Pluto do not provide own auto-tuning systems; thus, we use for them also the ATF framework for auto-tuning, the same as for our approach. For both compilers, we additionally also report their runtimes when relying on their internal heuristics, rather than on auto-tuning, to fairly compare to them.

To achieve the best possible performance results for TVM, PPCG, and Pluto, we auto-tune each of these frameworks individually for each particular combination of case study, architecture, and

[22] *Host code* is required in approaches CUDA and OpenCL for program execution – it compiles the CUDA and OpenCL programs, performs data transfers between host and device, etc.

input/output characteristics, the same as for our approach. For example, we start for TVM one tuning run when auto-tuning case study MatMul for architecture GPU on one input size, and another, new tuning run for a new input size, etc.

Hand-optimized libraries NVIDIA cuBLAS/cuDNN and Intel oneMKL/oneDNN rely on heuristics provided by experts, rather than auto-tuning. By relying on heuristics, the libraries avoid the time-intensive process of auto-tuning. However, auto-tuning is well amortized in many application areas (e.g., deep learning), because the auto-tuned implementations are re-used in many program runs. Moreover, auto-tuning avoids the complex and costly process of hand optimization by experts, and it often achieves higher performance than hand optimizations, as confirmed later by our experiments.

For a fair comparison, we use for each tuning run uniformly the same tuning time of 12h. Even though for many computations well-performing tuning results could often also be found in less than 12h for our approach as well as for other frameworks, we use such generous tuning time for all frameworks to avoid auto-tuning issues in our reported results – analyzing, improving, and accelerating the auto-tuning process is beyond the scope of this work and intended for our future work (as also outlined in Section 8). In particular, TVM's Ansor optimizer was often able to find well performing optimization decisions in 6h of tuning time or less. This is because Ansor explores a small search space that is specifically designed and optimized toward deep learning computations – Ansor's space is a proper subset of our space, as our space aims at capturing general optimizations that apply to a broad class of data-parallel computations. Thereby, Ansor usually struggles with achieving high performance for computations not taken from the deep learning area, as we confirm in our experiments later.

To improve the auto-tuning efficiency for our implementations, we rely on a straightforward cost model that shrinks our search space in Table 1 before starting our ATF-based auto-tuning process: i) we always use the same values for Parameters D1, S1, R1 as well as for Parameters D2, S2, R2, thereby generating the same loop structure for all three phases (de-composition, scalar, and re-composition) such that the structures can be generated as a fused loop nest; ii) we restrict Parameters D2, S2, R2 to two values – one value that let threads process outer parts (a.k.a. *blocked access* or *outer parallelism*, respectively) and one to let threads process inner parts (*strided access* or *inner parallelism*); all other permutations are currently ignored for simplicity or because they have no effect on the generated code (e.g., permutations of Parameters D2, S2, R2 that only differ in dimension tags belonging to memory layers, as discussed in the previous sections); iii) we restrict Parameters D3, S3, S5, R3 such that each parameter is invariant under different values of d of its input pairs $(l, d) \in$ MDH-LVL, i.e., we always copy full tiles in memory regions (and not a full tile of one input buffer and a half tile of another input buffer, which sometimes might achieve higher performance when memory is a limited resource). Our cost model is straightforward and might filter out configurations of our search space that achieve potentially higher performance than we report for our approach in Sections 5.1-5.4. We aim to substantially improve our naive cost model in future work, based on *operational semantics* for our low-level representation, in order to improve the auto-tuning quality and to reduce (or even avoid) tuning time.

Code Generator

We provide a straightforward, proof-of-concept code generator, implemented in C++. Our generator takes as input the high-level representation of the target computation (Figure 16), in the form of a straightforward text file (see Appendix, Section A.4), and it fully automatically generates auto-tuned program code, based on the concepts and methodologies introduced and discussed in this paper and the ATF auto-tuning framework. In our future work, we aim to integrate our code generation approach into the *MLIR* compiler framework [Lattner et al. 2021], building on work-in-progress

results [Google SIG MLIR Open Design Meeting 2020], thereby making our work better accessible for the community.

5.1 Scheduling Approaches

Performance. Figures 24-29 report the performance of the TVM-generated code, which is in CUDA for GPUs and in OpenCL for CPUs. We observe that we usually achieve the high performance of TVM and often perform even better. For example, in Figure 28, we achieve a speedup > 2× over TVM on NVIDIA Ampere GPU for matrix multiplications as used in the inference phase of the ResNet-50 neural network – an actually favorable example for TVM which is designed and optimized toward deep learning computations executed on modern GPUs. Our performance advantage over TVM is because we parallelize and optimize more efficiently reduction-like computations – in the case of MatMul (Figure 16), its 3rd-dimension (a.k.a. *k*-dimension). The difficulties of TVM with reduction computations becomes particularly obvious when computing dot products (Dot) on GPUs (Figure 24): the Dot's main computation part is a reduction computation (via point-wise addition, see Figure 16), thus requiring reduction-focussed optimization, in particular when targeting the highly-parallel architecture of GPUs: in the case of Dot (Figure 24), our MDH-generated CUDA code exploits parallelization over CUDA blocks, whereas the Ansor-generated TVM code exploits parallelization over threads within in a single block only, because TVM currently cannot use blocks for parallelizing reduction computations [Apache TVM Community 2022a]. Furthermore, while TVM's Ansor rigidly parallelizes outer dimensions [Zheng et al. 2020a], our ATF-based tuning process has auto-tuned our tuning parameters D2, S2, R2 in Table 1 to exploit parallelism for inner dimensions, which achieves higher performance for this particular MatMul example used in ResNet-50. Also, for MatMul-like computations, Ansor always caches parts of the input in GPU's shared memory, and it computes these cached parts always in register memory. In contrast, our caching strategy is auto-tunable (via parameters D3, S3 S5, R3 in Table 1), and ATF has determined to not cache the input matrices into fast memory resources for the MatMul example in ResNet-50. Surprisingly, Ansor does not exploit fast memory resources for Jacobi stencils (Figure 25), as required to achieve high performance for them: our MDH-generated and ATF-tuned CUDA kernel for Jacobi uses register memory for both inputs (image buffer and filter) when targeting NVIDIA Ampere GPU (small input size), thereby achieving a speedup over TVM+Ansor of 1.93× for Jacobi. Most likely, Ansor fails to foresee the potential of exploiting fast memory resources for Jacobi stencils, because the Jacobi's index functions used for memory accesses (Figure 16) are injective. For the MatMul example of ResNet-50's training phase (Figure 28), we achieve a speedup over TVM on NVIDIA Ampere GPU of 1.26×, because auto-tuning determined to store parts of input matrix *A* as transposed into fast memory (via parameter D4 in Table 1). Storing parts of the input/output data as transposed is not considered by Ansor as optimization, perhaps because such optimization must be expressed in TVM's high-level language, rather than scheduling language [Apache TVM Community 2022c]. For MatVec on NVIDIA Ampere GPU (Figure 24), we achieve a speedup over TVM of 1.22× for the small input size, by exploiting a so-called *swizzle pattern* [Phothilimthana et al. 2019]: our ATF tuner has determined to assign threads that are consecutive in CUDA's x-dimension to the second MDA dimension (via parameters D2, S2, R2 in Table 1), thereby accessing the input matrix in a GPU-efficient manner (a.k.a *coalesced global memory accesses* [NVIDIA 2022f]). In contrast, for MatVec computations, Ansor assigns threads with consecutive x-ids always to the first data dimension, in a non-tunable manner, causing lower performance.

Our positive speedups over TVM on CPU are for the same reasons as discussed above for GPU. For example, we achieve a speedup of > 3× over TVM on Intel Skylake CPU for MCC (Figure 29) as used in the training phase of the MobileNet neural network, because we exploit fast memory resources more efficiently than TVM: our auto-tuning process has determined to use register memory for the

MCC's second input (the filter buffer F, see Table 16) and using no fast memory for the first input (image buffer I), whereas Ansor uses shared memory rigidly for both inputs of MCC. Moreover, our auto-tuning process has determined to parallelize the inner dimensions of MCC, while Ansor always parallelizes outer dimensions. We achieve the best speedup over TVM for MCC on an input size taken from TVM's own tutorials [Apache TVM Documentation 2022b] (Figure 25), rather than from neural networks (as in Figures 28 and 29). This is because TVM's MCC size includes large reduction computations, which are not efficiently optimized by TVM (as discussed above).

The TVM compiler achieves higher performance than our approach for some examples in Figures 24-29. However, in most cases, this has a technical reason only: TVM uses the NVCC compiler for compiling CUDA code, while our proof-of-concept code generator relies on NVIDIA's NVRTC library which surprisingly generates less efficient CUDA assembly than NVCC. In three cases, the higher performance of TVM over our approach is because our ATF auto-tuning framework was not able to find a better performing tuning configuration than TVM's Ansor optimization engine; the three cases are: 1) MCC (capsule variant) from ResNet-50's training phase on Intel Skylake CPU, 2) MCC from VGG-16's inference phase on NVIDIA Ampere GPU, and 3) MCC (capsule variant) from VGG-16's training phase on NVIDIA Ampere GPU. However, when we manually set the Ansor-found tuning configuration also for our approach (analogously as done in Section 3.5), instead of using the ATF-found configuration, we achieve for these three cases exactly the same high performance as TVM+Ansor, i.e., the well-performing configurations are contained in our MDH-based search space. Most likely, Ansor was able to find this well-performing configuration automatically, because it explores a smaller search space that is particularly designed for deep learning computations. To avoid such tuning issues in our approach, we aim to substantially improve our auto-tuning process in future work: we plan to introduce an analytical cost model that assists (or even replaces) our auto-tuner, as we also outline in Section 8.

Note that the TVM compiler crashes for our data mining example PRL, because TVM has difficulties with computations relying on user-defined combine operators [Apache TVM Community 2022d].

Portability. Figure 30 reports the portability of the TVM compiler over our GPU and CPU architectures. The portability measurements are based on the Pennycook metric where a value close to 1 indicates high portability and a value close to 0 low portability, correspondingly. We observe that except for the example of transposed matrix multiplication $\text{GEMM}^\intercal$, we always achieve higher portability than TVM. The higher portability of TVM for $\text{GEMM}^\intercal$ is because TVM achieves for this example higher performance than our approach on NVIDIA Volta GPU. However, the higher performance of TVM is only due to the fact that TVM uses NVIDIA's NVCC for compiling CUDA code, while we currently rely on NVIDIA's NVRTC library which surprisingly generates less efficient CUDA assembly, as discussed above.

Productivity. Listing 1 shows how matrix-vector multiplication (MatVec) is implemented in TVM's high-level program representation which is embedded into the Python programming language. In line 1, the input size $(I, K) \in \mathbb{N} \times \mathbb{N}$ of matrix $M \in T^{I \times K}$ (line 2) and vector $v \in T^K$ (line 3) are declared, in the form of function parameters; the matrix and vector are named M and v and both are assumed to contain elements of scalar type T = float32 (floating point numbers). Line 5 defines a so-called *reduction axis* in TVM in which all values are combined in line 8 via te.sum (addition). The basic computation part of MatVec – multiplying matrix element M[i,k] with vector element v[k] – is also specified in line 8.

While we see the MatVec implementations of TVM (Listing 1) and our approach (Figure 6) basically on the same level of abstraction, we consider our approach in general as more expressive. This is because our approach supports multiple reduction dimensions that may rely on different combine operators, e.g., as required for expressing the MBBS example in Figure 16 with which TVM

```
1  def MatVec(I, K):
2      M = te.placeholder((I, K), name='M', dtype='float32')
3      v = te.placeholder((K,), name='v', dtype='float32')
4
5      k = te.reduce_axis((0, K), name='k')
6      w = te.compute(
7          (I,),
8          lambda i: te.sum(M[i, k] * v[k], axis=k)
9      )
10     return [M, v, w]
```

Listing 1. TVM program expressing Matrix-Vector Multiplication (MatVec)

is struggling – adding support for multiple, different reduction dimensions is considered in the TVM community as a non-trivial extension of TVM [Apache TVM Community 2020, 2022b]. Also, we consider our approach as slightly less error-prone: we automatically compute the expected sizes of matrix M (as $I \times K$) and vector v (as K), based on the user-defined input size (I, K) in line 1 and index functions $(i, k) \mapsto (i, k)$ for the matrix and $(i, k) \mapsto (k)$ for the vector in line 8 (see Definition 8). In contrast, TVM redundantly requests these matrix and vector sizes from the user for computing the function specification of its generated MatVec code (once in lines 2 and 3 of Listing 1, and again in lines 5 and 7), which lets TVM generate incorrect low-level code – without issuing an error message – when the user sets sizes different from $I \times K$ for the matrix and K for the vector in lines 2 and 3 [Apache TVM Community 2022f].

5.2 Polyhedral Compilers

Performance. Figures 24-29 report for our application case studies the performance of the PPCG-generated CUDA code for GPUs and of the OpenMP-annotated C code generated by polyhedral compiler Pluto for CPUs. For a fair comparison, we report for both polyhedral compilers their performance achieved for ATF-tuned tile sizes (denoted as PPCG+ATF/Pluto+ATF in Figures 24-29), as well as the performance of the two compilers when relying on their internal heuristics instead of auto-tuning (denoted as PPCG and Pluto in the figures). In some cases, PPCG's heuristic crashed with error `too many resources requested for launch`, because the heuristic seems to not take into account device-specific constraints, e.g., limited availability of GPUs' fast memory resources.

We observe that our MDH-based approach achieves better performance than PPCG and Pluto in all cases – sometimes by multiple orders of magnitude – in particular for deep learning computations (Figures 28 and 29). This is caused by the rigid optimization goals of PPCG and Pluto, e.g., always parallelizing outer dimensions, which causes severe performance losses. For example, we achieve a speedup over PPCG of $> 13\times$ on NVIDIA Ampere GPU and of $> 60\times$ over Pluto on Intel Skylake CPU for MCC as used in the inference phase of the real-world ResNet-50 neural network. Compared to PPCG, our better performance for this MCC example is because PPCG has difficulties with efficiently parallelizing computations relying on more than 3 dimension; most likely, this is because CUDA offers per default 3 dimensions for parallelization (called x, y, z dimension in CUDA). However, MCC relies on 7 parallelizable dimensions (as shown in Figure 16); exploiting the parallelization opportunities of the 4 further dimensions (as done in our generated CUDA code) is essential to achieve high performance for this MCC example from ResNet-50. Our performance advantage over Pluto for the MCC example is because Pluto parallelizes the outer dimensions of MCC only; however, the dimension has a size of only 1 for this real-world example, resulting in starting only 1 thread in the Pluto-generated OpenMP code.

For dot products Dot (Figure 24), we can observe that PPCG fails to generate parallel CUDA code, because PPCG cannot parallelize and optimize computations which rely solely on combine operators different from concatenation, as we also discuss in Section 6.2. In Section 6.2, we also discuss that we do not consider the performance issues of PPCG and Pluto as weaknesses of the polyhedral approach in general, but of the particular polyhedral transformations used in PPCG and Pluto.

Note that Pluto crashes for our data mining examples (Figure 27), with `Error extracting polyhedra from source file`, which is due to the complex scalar function of the example, which involves if-statements. Moreover, Intel's icx compiler struggles with compiling the Pluto-generated OpenMP code for quantum chemistry computations (Figure 26): we aborted icx's compilation process after 24h compilation time. The icx's issues with the Pluto-generated code are most likely because of too aggressive loop unrolling of Pluto – the Pluto-generated OpenMP code has often a size > 50MB for our real-world quantum chemistry examples.

Portability. Since PPCG and Pluto are each designed for particular architectures only, they achieve the lowest portability of 0 for all our studies, according to the Pennycook metric. To simplify for PPCG and Pluto the portability comparison with our approach, we compute the Pennycook metric additionally also for two restricted sets of devices: only GPUs to make comparison against our approach easier for PPCG, and only CPUs for Pluto.

Figures 31-35 report the portability of PPCG when considering only GPUs, as well as the portability of Pluto for only CPUs. We observe that we achieve higher portability for all our studies, as we constantly achieve higher performance than the two polyhedral compilers for the studies.

Note that even when restricting our set of devices to only GPUs for PPCG or only CPUs for Pluto, the two polyhedral compilers still achieve a portability of 0 for some examples, because they fail to generate code for them (as discussed above).

Productivity. Listing 2 shows the input program of polyhedral compilers PPCG and Pluto for MatVec. Both take as input easy-to-implement, straightforward, sequential C code. We consider these two polyhedral compilers as more productive than our approach (as well as scheduling/functional approaches and polyhedral compilers relying on a DSL, rather than sequential programs, as TC [Vasilache et al. 2019]), because both compilers fully automatically generate optimized parallel code from unoptimized, sequential programs.

Rasch et al. [2020a,b] show that our approach can achieve the same, high user productivity as polyhedral compilers, by using a polyhedral frontend for our approach: we can alternatively take as input the same sequential user programs as PPCG and Pluto, instead of programs implemented in our high-level program representation (as in Figure 6). The sequential input program is then transformed via polyhedral tool *pet* [Verdoolaege and Grosser 2012] to its polyhedral representation which is then automatically transformed to our high-level program representation, according to the methodology presented by Rasch et al. [2020a,b].

```
1 for( int i = 0 ; i < M ; ++i )
2   for( int k = 0 ; k < K ; ++k )
3       w[i] += M[i][k] * v[k];
```

Listing 2. PPCG/Pluto program expressing Matrix-Vector Multiplication (MatVec)

5.3 Functional Approaches

Our previous work [Rasch et al. 2019a] already shows that while functional approaches provide a solid formal foundation for computations, they typically have performance and portability

issues; for this, our previous work used the state-of-the-art Lift [Steuwer et al. 2015] framework as running example (which, to the best of our knowledge, has so far not been improved toward higher performance and/or better portability). Therefore, we refrain from a further performance and portability evaluation of Lift and focus in the following on analyzing and discussing the productivity potentials of functional approaches, using again the state-of-the-art Lift approach as running example. We discuss the performance and portability issues of functional approaches from a general perspective thoroughly in Section 6.3.

Performance/Portability. Already experimentally evaluated in previous work [Rasch et al. 2019a] and discussed in general terms in Section 6.3.

Productivity. Listing 3 shows the implementation of MatVec in the Lift approach. In line 1, type parameters n and m are declared via Lift building block nFun – type parameters are limited to natural numbers in the Lift formalism. Line 2 declares a function in Lift that takes as input a matrix of size m × n and a vector of size n, correspondingly; the matrix and vector are both assumed to consist of float numbers (floating point numbers). The computation of MatVec is specified in lines 3 and 4: the map function of Lift in line 3 iterates over all rows of the matrix, each row is pair-wise combined with the input vector via Lift pattern zip, multiplication * is applied to each pair in the combined vector via Lift's map pattern in line 4, and the obtained products are finally combined via addition + using Lift's reduce pattern.

```
1 nFun(n => nFun(m =>
2   fun(matrix: [[float]n]m => fun(xs: [float]n =>
3     matrix :>> map(fun(row =>
4       zip(xs, row) :>> map(*) :>> reduce(+, 0)
5     )) )) ))
```

Listing 3. Lift program expressing Matrix-Vector Multiplication (MatVec)

Already for expressing MatVec, we can observe that Lift relies on a vast set of small, functional building blocks (five building blocks for MatVec: nFun, fun, map, zip, and reduce), and the blocks have to be composed and nested in complex ways for expressing computations. Consequently, we consider programming in Lift-like approaches as complex and their productivity for the user as limited. Moreover, Lift-like approaches often need fundamental extension for targeting new kinds of computations, e.g., so-called *macro-rules* which had to be added to Lift for efficiently targeting matrix multiplications [Remmelg et al. 2016] and primitives slide and pad together with optimization *overlapped tiling* for expressing stencil computations [Hagedorn et al. 2018]. This need for extensions limits the expressiveness of the Lift language and thus hinders productivity.

In contrast to Lift, our approach relies on exactly three higher-order functions (Figure 5) to express various kinds of data-parallel computations (Figure 16): 1) inp_view (Definition 8) which prepares the input data; our inp_view function is designed as general enough to subsume – in a structured manner – the subset of all Lift patterns intended to change the view on input data, including patterns zip, pad, and slide; 2) md_hom (Definition 3) expresses the actual computation and subsumes all Lift patterns performing actual computations (fun, map, reduce, ...); 3) out_view (Definition 10) expresses the view on output data and is designed to work similarly as function inp_view (Lemma 2). Our three functions are always composed straightforwardly in the same, fixed order (Figure 5), and they do not rely on complex function nesting for expressing computations.

Note that even though our language is designed as minimalistic, it should cover the expressivity of the `Lift` language[23] and beyond: for example, we are currently not aware of any `Lift` program being able to express the prefix-sum examples in Figure 16. For the above reasons, we consider programming in our high-level language as more productive for the user than programming in `Lift`-like functional languages. Furthermore, as discussed in Section 5.2, our approach can take as input also straightforward, sequential program code, which further contributes to the productivity of our approach.

[23] This work is focussed on dense computations. `Lift` supports sparse computations [Pizzuti et al. 2020] which we consider as future work (as also outlined in Section 8). We consider `Lift`'s approach, based on their so-called *position dependent arrays*, as a great inspiration for our future goal.

Linear Algebra	NVIDIA Ampere GPU							
	Dot		MatVec		MatMul		$MatMul^T$	bMatMul
	2^{24}	10^7	4096,4096	8192,8192	10,500,64	1024,1024,1024	10,500,64	16,10,500,64
TVM+Ansor	172.48	128.22	1.74	1.23	1.00	1.00	1.00	1.17
PPCG	–	–	5.44	2.95	2.20	2.73	3.40	162.92
PPCG+ATF	–	–	4.22	2.77	1.20	1.87	1.32	3.06
cuBLAS	1.10	1.11	1.14	1.01	1.40	0.92	1.60	1.50
cuBLASEx	–	–	–	–	1.20	0.91	1.60	1.33
cuBLASLt	–	–	–	–	1.20	0.88	1.60	–

Linear Algebra	NVIDIA Volta GPU							
	Dot		MatVec		MatMul		$MatMul^T$	bMatMul
	2^{24}	10^7	4096,4096	8192,8192	10,500,64	1024,1024,1024	10,500,64	16,10,500,64
TVM+Ansor	82.28	67.97	1.06	1.04	1.00	1.08	0.80	1.00
PPCG	–	–	2.67	1.71	1.40	3.07	2.60	111.98
PPCG+ATF	–	–	2.44	2.24	1.00	2.16	1.20	2.83
cuBLAS	1.06	1.09	1.10	1.07	2.60	1.11	1.80	1.83
cuBLASEx	–	–	–	–	1.80	0.30	1.40	1.17
cuBLASLt	–	–	–	–	1.20	0.96	1.40	–

Linear Algebra	Intel Skylake CPU							
	Dot		MatVec		MatMul		$MatMul^T$	bMatMul
	2^{24}	10^7	4096,4096	8192,8192	10,500,64	1024,1024,1024	10,500,64	16,10,500,64
TVM+Ansor	5.07	6.14	1.03	3.39	1.06	1.15	1.02	1.10
Pluto	5.40	6.48	2.49	6.24	3.21	12.25	5.45	14.30
Pluto+ATF	5.39	6.01	1.43	3.38	2.98	4.78	4.79	2.14
oneMKL	0.64	0.57	0.42	3.83	6.27	0.69	3.42	0.98
oneMKL(JIT)	–	–	–	–	0.65	–	1.13	–

Linear Algebra	Intel Broadwell CPU							
	Dot		MatVec		MatMul		$MatMul^T$	bMatMul
	2^{24}	10^7	4096,4096	8192,8192	10,500,64	1024,1024,1024	10,500,64	16,10,500,64
TVM+Ansor	5.60	8.46	1.21	1.63	1.20	1.11	1.11	1.00
Pluto	4.78	6.73	3.01	1.28	4.89	5.26	6.74	11.97
Pluto+ATF	4.75	6.72	2.91	1.21	1.94	2.85	3.46	1.23
oneMKL	1.03	0.41	0.57	0.59	2.00	0.66	1.98	0.84
oneMKL(JIT)	–	–	–	–	1.03	–	1.30	–

Fig. 24. Speedup (higher is better) of our approach for linear algebra routines on GPUs and CPUs over: i) scheduling approach TVM, ii) polyhedral compilers PPCG (GPU) and Pluto (CPU), as well as iii) hand-optimized libraries provided by vendors. Dash symbol "-" means this framework does not support this combination of architecture, computation, and data characteristic.

Stencils	NVIDIA Ampere GPU				
	Jacobi3D		Conv2D		MCC
	256,256,256	512,512,512	224,224,5,5	4096,4096,5,5	1,512,7,7,512,3,3
TVM+Ansor	1.93	2.04	1.00	2.32	1.63
PPCG	4.19	5.27	1.58	2.36	–
PPCG+ATF	1.08	1.02	1.22	1.38	9.37
cuDNN	–	–	2.20	5.29	2.44

Stencils	NVIDIA Volta GPU				
	Jacobi3D		Conv2D		MCC
	256,256,256	512,512,512	224,224,5,5	4096,4096,5,5	1,512,7,7,512,3,3
TVM+Ansor	2.05	1.86	1.00	2.00	1.50
PPCG	7.01	13.87	1.45	1.75	–
PPCG+ATF	1.03	1.00	1.23	1.34	8.28
cuDNN	–	–	2.60	3.58	4.42

Stencils	Intel Skylake CPU				
	Jacobi3D		Conv2D		MCC
	256,256,256	512,512,512	224,224,5,5	4096,4096,5,5	1,512,7,7,512,3,3
TVM+Ansor	2.30	1.64	1.59	2.46	2.76
Pluto	3.65	2.66	2.39	1.38	143.80
Pluto+ATF	1.81	1.38	2.09	1.06	61.47
oneDNN	3.92	2.60	6.47	2.83	3.91

Stencils	Intel Broadwell CPU				
	Jacobi3D		Conv2D		MCC
	256,256,256	512,512,512	224,224,5,5	4096,4096,5,5	1,512,7,7,512,3,3
TVM+Ansor	2.21	1.78	3.14	3.98	3.99
Pluto	2.10	1.67	2.29	2.17	74.48
Pluto+ATF	1.29	1.05	1.74	1.25	74.47
oneDNN	16.09	15.02	7.29	16.42	7.69

Fig. 25. Speedup (higher is better) of our approach for stencil computations on GPUs and CPUs over: i) scheduling approach TVM, ii) polyhedral compilers PPCG (GPU) and Pluto (CPU), as well as iii) hand-optimized libraries provided by vendors. Dash symbol "-" means this framework does not support this combination of architecture, computation, and data characteristic.

Quantum Chemistry	NVIDIA Ampere GPU							
	abcdef-gdab-efgc	abcdef-gdac-efgb	abcdef-gdbc-efga	abcdef-geab-dfgc	abcdef-geac-dfgb	abcdef-gebc-dfga	abcdef-gfab-degc	abcdef-gfbc-dega
TVM+Ansor	1.15	1.07	1.25	1.00	1.36	1.05	1.00	1.15
PPCG	10585.85	10579.40	9819.81	11211.57	10181.14	10482.81	11693.21	10585.85
PPCG+ATF	11.19	15.60	14.06	11.45	11.81	12.06	11.72	11.19

Quantum Chemistry	NVIDIA Volta GPU							
	abcdef-gdab-efgc	abcdef-gdac-efgb	abcdef-gdbc-efga	abcdef-geab-dfgc	abcdef-geac-dfgb	abcdef-gebc-dfga	abcdef-gfab-degc	abcdef-gfbc-dega
TVM+Ansor	1.09	0.93	1.04	1.03	1.01	1.11	1.01	1.09
PPCG	6466.22	6019.64	6300.31	6468.40	6608.80	5256.49	6602.22	6466.22
PPCG+ATF	8.28	9.61	9.38	7.21	6.60	5.14	7.77	8.28

Quantum Chemistry	Intel Skylake CPU							
	abcdef-gdab-efgc	abcdef-gdac-efgb	abcdef-gdbc-efga	abcdef-geab-dfgc	abcdef-geac-dfgb	abcdef-gebc-dfga	abcdef-gfab-degc	abcdef-gfbc-dega
TVM+Ansor	1.60	1.50	2.06	1.70	1.20	2.12	1.56	1.60
Pluto	147.45	151.55	206.60	162.58	157.43	145.17	321.66	147.45
Pluto+ATF	1.89	2.01	1.89	1.80	1.82	1.92	1.84	1.89

Quantum Chemistry	Intel Broadwell CPU							
	abcdef-gdab-efgc	abcdef-gdac-efgb	abcdef-gdbc-efga	abcdef-geab-dfgc	abcdef-geac-dfgb	abcdef-gebc-dfga	abcdef-gfab-degc	abcdef-gfbc-dega
TVM+Ansor	1.06	1.28	1.16	1.15	1.29	1.13	2.07	1.06
Pluto	–	–	–	–	–	–	–	–
Pluto+ATF	–	–	–	–	–	–	–	–

Fig. 26. Speedup (higher is better) of our approach for quantum chemistry computations Coupled Cluster (CCSD(T)) on GPUs and CPUs over: i) scheduling approach TVM, and ii) polyhedral compilers PPCG (GPU) and Pluto (CPU). Dash symbol "-" means this framework does not support this combination of architecture, computation, and data characteristic.

Data Mining	NVIDIA Ampere GPU					
	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
TVM+Ansor	–	–	–	–	–	–
PPCG	1.49	1.05	1.12	1.22	1.37	1.56
PPCG+ATF	1.40	1.22	1.50	1.63	1.83	2.12

Data Mining	NVIDIA Volta GPU					
	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
TVM+Ansor	–	–	–	–	–	–
PPCG	1.11	1.15	1.10	1.30	1.51	1.82
PPCG+ATF	1.26	1.37	1.47	1.77	2.07	2.48

Data Mining	Intel Skylake CPU					
	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
TVM+Ansor	–	–	–	–	–	–
Pluto	–	–	–	–	–	–
Pluto+ATF	–	–	–	–	–	–
EKR	6.18	5.39	9.62	19.87	26.42	24.78

Data Mining	Intel Broadwell CPU					
	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
TVM+Ansor	–	–	–	–	–	–
Pluto	–	–	–	–	–	–
Pluto+ATF	–	–	–	–	–	–
EKR	8.01	9.17	23.58	66.90	119.33	167.19

Fig. 27. Speedup (higher is better) of our approach for data mining algorithm Probabilistic Record Linkage (PRL) on GPUs and CPUs over: i) scheduling approach TVM, and ii) polyhedral compilers PPCG (GPU) and Pluto (CPU), as well as the iii) hand-implemented Java CPU implementation used by *EKR* – the largest cancer registry in Europa. Dash symbol "-" means this framework does not support this combination of architecture, computation, and data characteristic.

Deep Learning	NVIDIA Ampere GPU									
	ResNet-50				VGG-16				MobileNet	
	Training		Inference		Training		Inference		Training	Inference
	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MCC
TVM+Ansor	1.00	1.26	1.05	2.22	0.93	1.42	0.88	1.14	0.94	1.00
PPCG	3456.16	8.26	–	7.89	1661.14	7.06	5.77	5.08	2254.67	7.55
PPCG+ATF	3.28	2.58	13.76	5.44	4.26	3.92	9.46	3.73	3.31	10.71
cuDNN	0.92	–	1.85	–	1.22	–	1.94	–	1.81	2.14
cuBLAS	–	1.58	–	2.67	–	0.93	–	1.04	–	–
cuBLASEx	–	1.47	–	2.56	–	0.92	–	1.02	–	–
cuBLASLt	–	1.26	–	1.22	–	0.91	–	1.01	–	–

Deep Learning	NVIDIA Volta GPU									
	ResNet-50				VGG-16				MobileNet	
	Training		Inference		Training		Inference		Training	Inference
	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MCC
TVM+Ansor	0.75	1.21	0.72	1.79	1.00	1.11	1.06	1.00	1.00	1.00
PPCG	1976.38	5.88	–	5.64	994.16	3.41	8.21	2.51	1411.92	7.26
PPCG+ATF	3.43	3.54	3.42	4.93	3.85	3.15	8.13	2.05	3.49	3.56
cuDNN	1.21	–	1.29	–	2.80	–	3.50	–	2.32	3.14
cuBLAS	–	1.33	–	1.14	–	1.09	–	1.04	–	–
cuBLASEx	–	1.21	–	1.07	–	1.04	–	1.03	–	–
cuBLASLt	–	1.00	–	1.07	–	1.04	–	1.02	–	–

Deep Learning (Capsule)	NVIDIA Ampere GPU					
	ResNet-50		VGG-16		MobileNet	
	Training	Inference	Training	Inference	Training	Inference
	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule
TVM+Ansor	0.96	1.00	0.79	1.02	0.88	0.99
PPCG	4642.24	–	1013.55	–	4017.74	–
PPCG+ATF	25.98	85.33	4.41	13.64	8.89	22.12
cuDNN	–	–	–	–	–	–

Deep Learning (Capsule)	NVIDIA Volta GPU					
	ResNet-50		VGG-16		MobileNet	
	Training	Inference	Training	Inference	Training	Inference
	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule
TVM+Ansor	0.95	1.01	1.05	0.97	1.04	0.87
PPCG	2935.40	–	945.16	–	2885.90	–
PPCG+ATF	19.24	19.68	8.28	12.29	8.84	6.41
cuDNN	–	–	–	–	–	–

Fig. 28. Speedup (higher is better) of our approach for the most time-intensive computations used in deep learning neural networks ResNet-50, VGG-16, and MobileNet on GPUs over: i) scheduling approach TVM, ii) polyhedral compilers PPCG (GPU), as well as iii) hand-optimized libraries provided by vendors. Dash symbol "-" means this framework does not support this combination of architecture, computation, and data characteristic.

Deep Learning	Intel Skylake CPU									
	ResNet-50				VGG-16				MobileNet	
	Training		Inference		Training		Inference		Training	Inference
	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MCC
TVM+Ansor	1.53	1.05	1.14	1.20	1.97	1.14	2.38	1.27	3.01	1.40
Pluto	355.81	49.57	364.43	13.93	130.80	93.21	186.25	36.30	152.14	75.37
Pluto+ATF	13.08	19.70	170.69	6.57	3.11	6.29	53.61	8.29	3.50	25.41
oneDNN	0.39	–	5.07	–	1.22	–	9.01	–	1.05	4.20
oneMKL	–	0.44	–	1.09	–	0.88	–	0.53	–	–
oneMKL(JIT)	–	6.43	–	8.33	–	27.09	–	9.78	–	–

Deep Learning	Intel Broadwell CPU									
	ResNet-50				VGG-16				MobileNet	
	Training		Inference		Training		Inference		Training	Inference
	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MCC
TVM+Ansor	1.53	1.60	1.29	1.53	1.32	1.00	1.27	1.02	2.42	1.92
Pluto	4349.20	40.41	137.21	15.96	1865.07	53.57	113.40	24.10	2255.00	53.85
Pluto+ATF	6.43	8.93	61.60	6.91	5.07	4.38	42.63	4.45	6.43	29.18
oneDNN	1.30	–	1.81	–	2.94	–	2.85	–	1.83	4.47
oneMKL	–	1.45	–	1.36	–	1.35	–	0.50	–	–
oneMKL(JIT)	–	19.78	–	9.77	–	50.58	–	10.70	–	–

Deep Learning (Capsule)	Intel Skylake CPU					
	ResNet-50		VGG-16		MobileNet	
	Training	Inference	Training	Inference	Training	Inference
	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule
TVM+Ansor	0.94	1.14	3.50	1.18	2.94	1.59
Pluto	209.36	265.77	–	166.45	160.49	159.34
Pluto+ATF	14.33	265.77	3.33	60.66	4.40	57.21
oneDNN	–	–	–	–	–	–

Deep Learning (Capsule)	Intel Broadwell CPU					
	ResNet-50		VGG-16		MobileNet	
	Training	Inference	Training	Inference	Training	Inference
	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule
TVM+Ansor	2.61	1.30	3.55	1.00	1.32	2.24
Pluto	–	–	–	–	–	–
Pluto+ATF	4418.82	56.17	75.77	2173.72	202.34	158.52
oneDNN	–	–	–	–	–	–

Fig. 29. Speedup (higher is better) of our approach for the most time-intensive computations used in deep learning neural networks ResNet-50, VGG-16, and MobileNet on CPUs over: i) scheduling approach TVM, ii) polyhedral compilers Pluto (CPU), as well as iii) hand-optimized libraries provided by vendors. Dash symbol "-" means this framework does not support this combination of architecture, computation, and data characteristic.

Linear Algebra	Pennycook Metric							
	Dot		MatVec		MatMul		$MatMul^T$	bMatMul
	2^{24}	10^7	4096,4096	8192,8192	10,500,64	1024,1024,1024	10,500,64	16,10,500,64
MDH+ATF	0.88	0.64	0.65	0.85	0.88	0.54	0.94	0.95
TVM+Ansor	0.01	0.02	0.54	0.47	0.83	0.50	0.97	0.89

Stencils	Pennycook Metric				
	Jacobi3D		Conv2D		MCC
	256,256,256	512,512,512	224,224,5,5	4096,4096,5,5	1,512,7,7,512,3,3
MDH+ATF	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.47	0.55	0.59	0.37	0.41

Quantum Chemistry	Pennycook Metric							
	abcdefg-gdab-efgc	abcdefg-gdac-efgb	abcdefg-gdbc-efga	abcdefg-geab-dfgc	abcdefg-geac-dfgb	abcdefg-gebc-dfga	abcdefg-gfab-degc	abcdefg-gfbc-dega
MDH+ATF	1.00	0.98	1.00	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.82	0.82	0.73	0.82	0.82	0.74	0.71	0.84

Data Mining	Pennycook Metric					
	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
MDH+ATF	1.00	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.00	0.00	0.00	0.00	0.00	0.00

Deep Learning	Pennycook Metric									
	ResNet-50				VGG-16				MobileNet	
	Training		Inference		Training		Inference		Training	Inference
	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MCC
MDH+ATF	0.67	0.76	0.91	1.00	0.98	0.95	0.97	0.68	0.98	1.00
TVM+Ansor	0.53	0.62	0.89	0.59	0.76	0.81	0.70	0.61	0.54	0.75

Deep Learning (Capsule)	Pennycook Metric					
	ResNet-50		VGG-16		MobileNet	
	Training	Inference	Training	Inference	Training	Inference
	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule
MDH+ATF	0.96	1.00	0.94	0.99	0.97	0.96
TVM+Ansor	0.71	0.90	0.44	0.95	0.63	0.69

Fig. 30. Portability (higher is better), according to Pennycook metric, of our approach and TVM over GPUs and CPUs for case studies. Polyhedral compilers PPCG/Pluto and vendor libraries by NVIDIA and Intel are not listed: due to their limitation to certain architectures, all of them achieve the lowest portability of 0 only.

Linear Algebra	Pennycook Metric (GPUs only)							
	Dot		MatVec		MatMul		MatMul^T	bMatMul
	2^{24}	10^7	4096,4096	8192,8192	10,500,64	1024,1024,1024	10,500,64	16,10,500,64
MDH+ATF	1.00	1.00	1.00	1.00	1.00	0.45	0.89	1.00
TVM+Ansor	0.01	0.01	0.71	0.88	1.00	0.42	1.00	0.92
PPCG	0.00	0.00	0.25	0.43	0.56	0.15	0.30	0.01
PPCG+ATF	0.00	0.00	0.30	0.40	0.91	0.21	0.71	0.34
cuBLAS	0.93	0.91	0.89	0.96	0.50	0.42	0.52	0.60
cuBLASEx	0.00	0.00	0.00	0.00	0.67	0.98	0.60	0.00
cuBLASLt	0.00	0.00	0.00	0.00	0.83	0.48	0.60	0.00

Linear Algebra	Pennycook Metric (CPUs only)							
	Dot		MatVec		MatMul		MatMul^T	bMatMul
	2^{24}	10^7	4096,4096	8192,8192	10,500,64	1024,1024,1024	10,500,64	16,10,500,64
MDH+ATF	0.78	0.48	0.48	0.74	0.79	0.67	1.00	0.90
TVM+Ansor	0.15	0.06	0.44	0.32	0.71	0.60	0.94	0.86
Pluto	0.15	0.07	0.18	0.24	0.20	0.08	0.16	0.07
Pluto+ATF	0.15	0.07	0.23	0.37	0.31	0.18	0.24	0.55
oneMKL	0.99	1.00	1.00	0.41	0.17	1.00	0.37	1.00
oneMKL(JIT)	0.00	0.00	0.00	0.00	0.98	0.00	0.83	0.00

Fig. 31. Portability (higher is better), according to Pennycook metric, for linear algebra routines computed on only GPUs or CPUs, respectively. The restriction simplifies for frameworks with limited architectural support (such as polyhedral compilers and vendor libraries) the portability comparisons against our approach.

Stencils	Pennycook Metric (GPUs only)				
	Jacobi3D		Conv2D		MCC
	256,256,256	512,512,512	224,224,5,5	4096,4096	1,512,7,7,512,3,3
MDH+ATF	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.50	0.51	1.00	0.46	0.64
PPCG	0.18	0.10	0.66	0.49	0.00
PPCG+ATF	0.95	0.99	0.82	0.74	0.11
cuDNN	0.00	0.00	0.42	0.23	0.29

Stencils	Pennycook Metric (CPUs only)				
	Jacobi3D		Conv2D		MCC
	256,256,256	512,512,512	224,224,5,5	4096,4096	1,512,7,7,512,3,3
MDH+ATF	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.44	0.58	0.42	0.31	0.30
Pluto	0.35	0.46	0.43	0.56	0.01
Pluto+ATF	0.65	0.83	0.52	0.86	0.01
oneDNN	0.10	0.11	0.15	0.10	0.17

Fig. 32. Portability (higher is better), according to Pennycook metric, for stencil computations computed on only GPUs or CPUs, respectively. The restriction simplifies for frameworks with limited architectural support (such as polyhedral compilers and vendor libraries) the portability comparisons against our approach.

Quantum Chemistry	Pennycook Metric (GPUs only)							
	abcdefg-gdab-efgc	abcdefg-gdac-efgb	abcdefg-gdbc-efga	abcdefg-geab-dfgc	abcdefg-geac-dfgb	abcdefg-gebc-dfga	abcdefg-gfab-degc	abcdefg-gfbc-dega
MDH+ATF	1.00	0.96	1.00	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.90	0.96	0.87	0.99	0.84	0.93	0.99	1.00
PPCG	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PPCG+ATF	0.10	0.08	0.09	0.11	0.11	0.12	0.10	0.15

Quantum Chemistry	Pennycook Metric (CPUs only)							
	abcdefg-gdab-efgc	abcdefg-gdac-efgb	abcdefg-gdbc-efga	abcdefg-geab-dfgc	abcdefg-geac-dfgb	abcdefg-gebc-dfga	abcdefg-gfab-degc	abcdefg-gfbc-dega
MDH+ATF	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.75	0.72	0.62	0.70	0.80	0.62	0.55	0.72
Pluto	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Pluto+ATF	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Fig. 33. Portability (higher is better), according to Pennycook metric, for quantum chemistry computation Coupled Cluster (CCSD(T)) computed on only GPUs or CPUs, respectively. The restriction simplifies for frameworks with limited architectural support (such as polyhedral compilers and vendor libraries) the portability comparisons against our approach.

Data Mining	Pennycook Metric (GPUs only)					
	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
MDH+ATF	1.00	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.00	0.00	0.00	0.00	0.00	0.00
PPCG	0.77	0.91	0.90	0.80	0.69	0.59
PPCG+ATF	0.75	0.77	0.67	0.59	0.51	0.43

Data Mining	Pennycook Metric (CPUs only)					
	2^{15}	2^{16}	2^{17}	2^{18}	2^{19}	2^{20}
MDH+ATF	1.00	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.00	0.00	0.00	0.00	0.00	0.00
Pluto	0.00	0.00	0.00	0.00	0.00	0.00
Pluto+ATF	0.00	0.00	0.00	0.00	0.00	0.00
EKR	0.14	0.14	0.06	0.02	0.01	0.01

Fig. 34. Portability (higher is better), according to Pennycook metric, for data mining algorithm Probabilistic Record Linkage (PRL) computed on only GPUs or CPUs, respectively. The restriction simplifies for frameworks with limited architectural support (such as polyhedral compilers and vendor libraries) the portability comparisons against our approach.

Deep Learning	Pennycook Metric (GPUs only)									
	ResNet-50				VGG-16				MobileNet	
	Training		Inference		Training		Inference		Training	Inference
	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MCC
MDH+ATF	0.82	1.00	0.84	1.00	0.96	0.95	0.94	1.00	0.97	1.00
TVM+Ansor	0.96	0.81	0.98	0.50	1.00	0.75	0.97	0.93	1.00	1.00
PPCG	0.00	0.14	0.00	0.15	0.00	0.18	0.14	0.26	0.00	0.13
PPCG+ATF	0.24	0.33	0.11	0.19	0.24	0.27	0.11	0.35	0.28	0.14
cuBLAS	0.76	0.00	0.55	0.00	0.48	0.00	0.35	0.00	0.47	0.38
cuBLASEx	0.00	0.69	0.00	0.53	0.00	0.95	0.00	0.96	0.00	0.00
cuBLASLt	0.00	0.75	0.00	0.55	0.00	0.97	0.00	0.97	0.00	0.00
cuDNN	0.00	0.88	0.00	0.87	0.00	0.98	0.00	0.98	0.00	0.00

Deep Learning	Pennycook Metric (CPUs only)									
	ResNet-50				VGG-16				MobileNet	
	Training		Inference		Training		Inference		Training	Inference
	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MatMul	MCC	MCC
MDH+ATF	0.56	0.61	1.00	1.00	1.00	0.94	1.00	0.51	1.00	1.00
TVM+Ansor	0.37	0.50	0.82	0.73	0.61	0.87	0.55	0.45	0.37	0.60
Pluto	0.00	0.01	0.00	0.07	0.00	0.01	0.01	0.02	0.00	0.02
Pluto+ATF	0.05	0.04	0.01	0.15	0.24	0.17	0.02	0.08	0.20	0.04
oneMKL	0.87	0.00	0.29	0.00	0.48	0.00	0.17	0.00	0.69	0.23
oneMKL(JIT)	0.00	0.82	0.00	0.82	0.00	0.85	0.00	1.00	0.00	0.00
oneDNN	0.00	0.06	0.00	0.11	0.00	0.02	0.00	0.05	0.00	0.00

Deep Learning (Capsule)	Pennycook Metric (GPUs only)					
	ResNet-50		VGG-16		MobileNet	
	Training	Inference	Training	Inference	Training	Inference
	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule
MDH+ATF	0.95	1.00	0.88	0.98	0.94	0.93
TVM+Ansor	1.00	0.99	0.98	0.99	0.98	1.00
PPCG	0.00	0.00	0.00	0.00	0.00	0.00
PPCG+ATF	0.04	0.02	0.14	0.08	0.11	0.07
cuDNN	0.00	0.00	0.00	0.00	0.00	0.00

Deep Learning (Capsule)	Pennycook Metric (CPUs only)					
	ResNet-50		VGG-16		MobileNet	
	Training	Inference	Training	Inference	Training	Inference
	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule	MCC_Capsule
MDH+ATF	0.97	1.00	1.00	1.00	1.00	1.00
TVM+Ansor	0.55	0.82	0.28	0.92	0.47	0.52
Pluto	0.00	0.00	0.00	0.00	0.00	0.00
Pluto+ATF	0.00	0.01	0.03	0.00	0.01	0.01
oneDNN	0.00	0.00	0.00	0.00	0.00	0.00

Fig. 35. Portability (higher is better), according to Pennycook metric, for deep learning computations computed on only GPUs or CPUs, respectively. The restriction simplifies for frameworks with limited architectural support (such as polyhedral compilers and vendor libraries) the portability comparisons against our approach.

5.4 Domain-Specific Approaches

Performance. Figures 24-29 report for completeness also performance results achieved by domain-specific approaches. Since domain-specific approaches are specifically designed and optimized toward particular applications domains and often also architectures (e.g., only linear algebra routines on only GPU), we consider comparing to them as challenging for us: our approach is designed and optimized toward data-parallel computations in general, from arbitrary application domains (the same as also TVM, polyhedral compilers, and many functional approaches), and our approach is also flexibel in the target parallel architecture.

We observe in Figures 24-29 that the domain-specific libraries `NVIDIA cuBLAS/cuDNN` (for linear algebra routines and convolutions on GPUs) and `Intel oneMKL/oneDNN` (for linear algebra routines and convolutions on CPUs) sometimes perform better and sometimes worse than our approach. The better performance of libraries over our approach is most likely[24] because the libraries internally rely on assembly-level optimizations, while we currently focus on the higher CUDA/OpenCL abstraction level which offers less optimization opportunities [Goto and Geijn 2008; Lai and Seznec 2013]. The `cuBLASEx` extension of `cuBLAS` achieves in one case – `MatMul` on `NVIDIA Volta GPU` for square 1024×1024 input matrices – significantly higher performance than our approach. The high performance is achieved by `cuBLASEx` when using its algorithm variant `CUBLAS_GEMM_ALGO1_TENSOR_OP` which casts the `float`-typed inputs implicitly to the half precision type (a.k.a. `half` or `fp16`), allowing `cuBLASEx` exploiting the GPU's tensor core extension [NVIDIA 2017]. Thereby, `cuBLASEx` achieves significantly higher performance than our approach, because tensor cores compute small matrix multiplication immediately in hardware; however, at the cost of a significant precision loss: the `half` scalar type achieves only half the accuracy achieved by scalar type `float`. When using `cuBLASEx`'s default algorithm `CUBLAS_GEMM_DEFAULT` (rather than algorithm `CUBLAS_GEMM_ALGO1_TENSOR_OP`), which retains the `float` type and thus meets the accuracy expected from the computation, we achieve a speedup of $1.11\times$ over `cuBLASEx`. For the interested reader, we report in our Appendix, Section D.2, the runtime of `cuBLASEx` for all its algorithm variants, including reports for the accuracy achieved by the different variants.

The reason for the better performance of our approach over NVIDIA and Intel libraries is most likely because our approach allows generating code that is also optimized (auto-tuned) for data characteristics, which is important for high performance [Tillet and Cox 2017]. In contrast, the vendor libraries usually rely for each computation on pre-implemented implementations each optimized toward only average high performance for a range of data characteristics (size, memory layout, etc). By relying on these fixed, pre-implemented implementations, the libraries avoid the auto-tuning overhead. However, auto-tuning is often amortized, particularly for deep learning computations – the main target of libraries `NVIDIA cuDNN` und `Intel oneDNN` – because the auto-tuned implementations are re-used in many program runs. Moreover, we achieve better performance for convolutions (Figure 25), because the libraries re-use optimizations for these computations originally intended for linear algebra routines [Li et al. 2016], while our optimization space (Table 1) is designed as general and not oriented toward linear algebra.

Compared to the `EKR` library (Figure 27), we achieve higher performance, because the `EKR`'s Java implementation inefficiently handles memory: the library is implemented using Java's `ArrayList` data structure which is convenient to use for the Java programmer, but inefficient in terms of performance, because the structure internally performs costly memory reallocations.

Portability. Similarly to polyhedral compilers `PPCG` and `Pluto`, the domain-specific approaches work for particular architectures only. The domain-specific approaches are also restricted to a

[24] Since the Intel and NVIDIA libraries are not open source, we cannot explain their performance behavior with certainty.

narrow set of studies, e.g., only linear algebra routines as NVIDIA cuBLAS and Intel oneMKL or only data mining example PRL as EKR. Consequently, the approaches achieve for these unsupported studies the lowest portability of only 0 in Figure 30 as well as Figures 31-35. For their target studies, domain-specific approaches can achieve high portability. This is because the approaches are specifically designed and optimized toward these studies, e.g., via application-specific assembly-level optimizations which are currently beyond the scope of our work.

Productivity. Listing 4 shows the implementation of MatVec in domain-specific approach NVIDIA cuBLAS; the implementation of MatVec in other domain-specific approaches, e.g., Intel oneMKL, is analogous to the implementation in Listing 4. We consider domain-specific approaches as most productive for their target domain: in the case of MatVec, the user simply calls the high-level function cublasSgemv and passes to it the input matrices (omitted via ellipsis in the listing) together with some meta information (memory layout of matrices, etc); cuBLAS then automatically starts the GPU computation for MatVec.

Besides the fact that domain-specific approaches typically target only particular target architectures, a further fundamental productivity issue of domain-specific approaches is that they can only be used for a narrow class of computations, e.g., only linear algebra routines as NVIDIA cuBLAS and Intel oneMKL. Moreover, in the case of domain-specific libraries from NVIDIA and Intel, it is often up to the user to manually choose among different, semantically equal but differently performing implementations for high performance. For example, the cuBLAS library offers three different routines for computing matrix multiplications – routines cublasSgemm (part of standard cuBLAS), cublasGemmEx (part of the cuBLASEx extension of cuBLAS), and routine cublasLtMatmul (part of the cuBLASLt extension) – and the routines often also offer different, so-called *algorithms* (e.g., 42 algorithm variants in the case cuBLASEx) which impact the internal optimization process. When striving for the highest performance potentials of libraries, the user is in charge of naively testing each possible combination of routine and algorithm variant (as we have done in Figures 24-29 to make experimenting challenging for us). In addition, the user must be aware that different combinations of routines and algorithms can produce results of reduced accuracy (as discussed above), which can be critical for accuracy-sensitive use cases.

```
1 cublasSgemv( /* ... */ );
```

Listing 4. cuBLAS program expressing Matrix-Vector Multiplication (MatVec)

6 RELATED WORK

Three major classes of approaches currently focus on code generation and optimization for data-parallel computations: 1) scheduling, 2) polyhedral, and 3) functional. In the following, we compare in Sections 6.1-6.3 our approach to each of these three classes – in terms of *performance*, *portability*, and *productivity*. In contrast to Section 5, which has compared our approach against these classes experimentally, this section is focussed on discussions in a more general, non-experimental context. Afterwards, we outline domain-specific approaches in Section 6.4, which are specifically designed and optimized toward their target application domains. In Section 6.5, we briefly outline approaches focussing on optimizations at the algorithmic level of abstraction which we consider as higher-level optimizations than proposed by our approach and as greatly combinable with our work. Finally, we discuss in Section 6.6 the differences between our approach introduced in this paper and the already existing work on MDHs.

6.1 Scheduling Approaches

Popular examples of scheduling approaches include TVM [Chen et al. 2018a], Halide [Ragan-Kelley et al. 2013], Elevate [Hagedorn et al. 2020b], DaCe [Ben-Nun et al. 2019], Tiramisu [Baghdadi et al. 2019], CHiLL [Chen et al. 2008; Khan et al. 2013], Clay [Bagnères et al. 2016], UTF [Kelly and Pugh 1998], URUK [Girbal et al. 2006], Fireiron [Hagedorn et al. 2020a], DISTAL [Yadav et al. 2022], and LoopStack [Wasti et al. 2022]. While scheduling approaches usually achieve high performance, they often have difficulties with achieving portability and productivity, as we discuss in the following.[25]

Performance. Scheduling approaches usually achieve high performance. For this, the approaches incorporate human expert knowledge into their optimization process which is based on two major steps: 1) a human expert implements an optimization program (a.k.a *schedule*) in a so-called *scheduling language* – the program specifies the basic optimizations to perform, such as tiling and parallelization; 2) an auto-tuning system (or, alternatively, a human hardware expert) chooses performance-critical parameter values of the optimizations implemented in the schedule, e.g., particular values of tile sizes and concrete numbers of threads.

Our experiments in Section 5 show that compared to scheduling approach TVM (using its recent Ansor optimizer [Zheng et al. 2020a] for schedule generation), our approach achieves competitive and sometimes even better performance, e.g., speedups up to 2.22× on GPU and 3.55× on CPU over TVM+Ansor for computations taken from TVM's favorable application domain (deep learning). Section 5 discusses that our better performance is due to the design and structure of our general optimization space (Table 1) which can be efficiently explored fully automatically using state-of-the-art auto tuning techniques [Rasch et al. 2021]. We focus on TVM in our experiments (rather than, e.g. Halide) to make experimenting challenging for us: TVM+Ansor has proved to achieve higher performance on GPUs and CPUs than popular state-of-practice approaches [Zheng et al. 2020a], including Halide, pyTorch [Paszke et al. 2019], and the recent FlexTensor optimizer [Zheng et al. 2020b].

Recent approach TensorIR [Feng et al. 2022] is a compiler for deep learning computations that achieves higher performance than TVM on NVIDIA GPUs. However, this performance gain over TVM is mainly achieved by exploiting the domain-specific *tensor core* [NVIDIA 2017] extensions of NVIDIA GPUs, which compute in hardware the multiplications of small, low-precision 4×4 matrices. For this, TensorIR introduces the concept of *blocks* which represent sub-computations, e.g., for computing matrix multiplication on 4×4 sub-matrices. These blocks are than mapped by TensorIR to domain-specific hardware extensions, such as NVIDIA's tensor cores, leading to high performance.

While domain-specific hardware extensions are not targeted by this paper, we can naturally exploit them in our approach, similar to TensorIR, as we plan for our future work: the sub-computations targeted by the current hardware extensions, like matrix multiplication on 4×4 matrices, can be straightforwardly expressed in our approach (Figure 16). Thus, we can match these sub-expressions in our low-level representation and map them to hardware extensions in our generated code. For this, instead of relying on a full partitioning in our low-level representation (as in Figure 17) such that we can apply scalar function f to the fully de-composed data (consisting of a single data element only in the case of a full partitioning), we plan to rely on a coarser-grained partitioning schema, e.g., down to only 4×4 matrices (rather than 1×1 matrices, as in the case of a full partitioning). This allows us replacing scalar function f (which in the case of matrix multiplication is

[25] Rasch et al. [2023] introduce (optionally) a scheduling language for MDH to incorporate expert knowledge into MDH's optimization process, e.g., to achieve 1) better optimization, as an auto-tuning system might not always make the same high-quality optimization decisions as a human expert, or 2) faster auto-tuning, as some (or even all) optimization decisions might be made by the expert user and thus are not left to the costly auto-tuner.

a simple scalar multiplication $*$) with the operation supported by the hardware extension, such as matrix multiplication on 4×4 matrices. We expect for our future work to achieve the same advantages over TensorIR as over TVM, because apart from supporting domain-specific hardware extensions, TensorIR is very similar to TVM.

Portability. While scheduling approaches achieve high performance, they tend to struggle with achieving portability. This is because even though the approaches often provide different, pre-implemented backends (e.g., a CUDA backend to target NVIDIA GPUs and an OpenCL backend for CPUs), they do not propose any structured methodology about how new backends can be added, e.g., for potentially upcoming architectures, with potentially deeper memory and core hierarchies than GPUs and CPUs. This might be particularly critical (or requiring significant development effort) for the application area of deep learning which is the main target of many scheduling approaches, e.g., TVM and TensorIR, and for which new architectures are arising continuously [Hennessy and Patterson 2019].

In contrast, we introduce in this paper a formally precise recipe for correct-by-construction code generation in different backends (including OpenMP, CUDA, and OpenCL), generically in the target architecture: we introduce an architecture-agnostic low-level representation (Section 3) as target for our high-level programs (Section 2), and we describe formally how our high-level programs are automatically lowered to our low-level representation (Section 4), based on the architecture-agnostic optimization space in Table 1. Our Appendix, Section E, outlines how executable, imperative-style program code is straightforwardly generated from low-level expressions, which we plan to discuss and illustrate in detail in our future work.

Productivity. Scheduling approaches rely on a two-step optimization process, as discussed above: implementing a schedule (first step) and choosing optimized values of performance-critical parameters within that schedule (second step). While the second step often can be easily automatized, e.g., via auto-tuning [Chen et al. 2018b], the first step – implementing a schedule – usually has to be conducted manually by the user for high performance, which requires expert knowledge and thus hinders productivity. The lack of formal foundation of many scheduling approaches further complicates implementing schedules for the user, as implementation becomes error prone and hardly predictable. For example, Fireiron's schedules can achieve high performance, close to GPUs' peak, but schedules in Fireiron can easily generate incorrect low-level code: Fireiron cannot guarantee that optimizations expressed in its scheduling language are semantics preserving, e.g., based on a formal foundation as done in this work, making programming Fireiron's schedules error prone and complex for the user. Similarly, TVM is sometimes unable to detect user errors in both its high-level language (as discussed in Section 5.1) as well as scheduling language [Apache TVM Community 2022e]. Safety in parallel programming is an ongoing major demand, in particular from industry [Khronos 2022a].

Auto schedulers, such as Halide's optimization engine [Mullapudi et al. 2016] and TVM's recent Ansor [Zheng et al. 2020a], aim at automatically generating well-performing, correct schedules for the user. However, a major flaw of the current auto schedulers is that even though they work well for some computations (e.g., from deep learning, as TVM's Ansor), they may perform worse for others. For example, our approach achieves a speedup over TVM+Ansor of $> 100\times$ already for straightforward dot products. This is because Ansor does not exploit multiple thread blocks and uses only a small number of threads for reduction computations, which is usually beneficial for reductions as computed within convolutions and matrix multiplications used in deep learning applications (because parallelization can be better exploited for outer loops of these computations), but not for pure reductions.

To avoid the productivity issues of scheduling approaches, we have designed our optimization process as fully auto-tunable, thereby freeing the user from the burden and complexity of making complex optimization decisions. Our optimization space (Table 1) is designed as agnostic of a target application area and hardware architecture, thereby achieving high performance for various combinations of applications and architectures (Section 5). Correctness of optimizations is ensured in our approach by introducing a formal foundation that enables mathematical reasoning about correctness (Section 4). Our optimization process is designed as *correct-by-construction*, meaning that any valid optimization decisions (i.e., a particular choice of tuning parameters in Table 1 that satisfy the constraints) leads to a correct expression in our low-level expression (Figure 19). In contrast, approaches such as introduced by Clément and Cohen [2022] formally validate optimization decisions of scheduling approaches in already generated low-level code. Thereby, such approaches work potentially for arbitrary scheduling approaches (Halide, TVM, ...), but they cannot save the user at the high abstraction level from implementing incorrect optimizations (e.g., via easy-to-understand, high-level error messages indicating that an invalid optimization decisions is made) or restricting the optimization space otherwise to valid decisions only, e.g., for an efficient auto-tuning process, because the approaches check already generated low-level program code.

Scheduling approaches often also suffer from expressivity issues. For example, Fireiron is restricted to computing only matrix multiplications on only NVIDIA GPUs, and TVM does not support computations that rely on multiple combine operators different from concatenation [Apache TVM Community 2020, 2022b], e.g., as required for expressing the *Maximum Bottom Box Sum* example in Figure 16. Also, TVM has difficulties with user-defined combine operators [Apache TVM Community 2022d] and thus crashes for example *Probabilistic Record Linkage* in Figure 16. In contrast to TVM, we introduce a formal methodology about of how to manage different kinds of arbitrary, user-defined combine operators (Section 3), which is considered as challenging [Apache TVM Community 2020].

6.2 Polyhedral Approaches

Polyhedral approaches such as TC [Vasilache et al. 2019], PPCG [Verdoolaege et al. 2013], Pluto [Bondhugula et al. 2008b], Polly [Grosser et al. 2012], and the recent AKG [Bastoul et al. 2022] rely on a formal, geometrically-inspired representation, called *polyhedral model*. Polyhedral approaches often achieve high user productivity, e.g., by automatically parallelizing and optimizing straightforward sequential code. However, the approaches tend to have problems with achieving high performance and portability when used for generating low-level code, as we outline in the following. In Section 6.5, we revisit the polyhedral approach as a potential frontend for our approach, as polyhedral transformations have proven to be efficient when used for high-level code optimizations (e.g., *loop skewing* [Wolf and Lam 1991]), rather than low-level code generation.

Performance. Polyhedral compilers tend to struggle with achieving their full performance potential. We argue that this performance issue of polyhedral compilers is mainly caused by the following two major reasons.

While we consider the set of polyhedral transformation (so-called *affine transformation*) as broad, expressive, and powerful, each polyhedral compiler implements a subset of expert-chosen transformations. This subset of transformations, as well as the application order of transformations, are usually fixed in a particular polyhedral compiler and chosen toward specific optimization goals only, e.g., coarse-grained parallelization and locality-aware data accesses (a.k.a. *Pluto algorithm* [Bondhugula et al. 2008a]), causing the search spaces of polyhedral compilers to be a proper subset of our space in Table 1 only. Consequently, computations that require for high performance other subsets of polyhedral transformations and/or application orders of transformations (e.g.,

transformations toward fine-grained parallelization) might not achieve their full performance potential when compiled with a particular polyhedral compiler.

In contrast to the currently existing polyhedral compilers, we have designed our optimization process as generic in goals: for example, our space is designed such that the degree of parallelization (coarse, fine, ...) is completely auto-tunable for the particular combination of target architecture and computation to optimize. We consider it as an interesting future work to investigate the strength and weaknesses of the polyhedral model for expressing our generic optimization space.

We see the second reason for potential performance issues in polyhedral compilers in their difficulties with reduction-like computations. This is mainly caused by the fact that the polyhedral model captures less semantic information than the high-level program representation introduced in Section 2 of this paper: combine operators which are used to combine the intermediate results of computations (e.g., operator + from Example 2 for combining the intermediate results of the dot products within matrix multiplication) are not explicitly represented in the polyhedral model; the polyhedral model is rather focussed on modeling memory accesses and their relative order only. Most likely, these semantic information are missing in the polyhedral model, because polyhedral approaches were originally intended to fully automatically optimize sequential code (such as Pluto and PPCG) – extracting combine operators automatically from sequential code is challenging and often even impossible (Rice's theorem).

In contrast, our proposed high-level representation explicitly captures combine operators (Figure 16), by requesting these operators explicitly from the user. This is important, because the operators are often required for generating code that fully utilizes the highly parallel hardware of state-of-the-art parallel architectures (GPUs, etc), as discussed in Section 5. Similarly to our approach, polyhedral compiler TC also requests combine operators explicitly from the user. However, TC is restricted to operators `+` (addition), `*` (multiplication), `min` (minimum), and `max` (maximum) only, thereby TC is not able to express important examples in Figure 16, e.g., PRL which is popular in data mining. Moreover, TC outsources the computation of its combine operators to the NVIDIA CUB library [NVIDIA 2022a]; most likely as a workaround, because TC relies on the polyhedral model which is not designed to capture and exploit semantic information about combine operators for optimization. Thereby, TC is dependent on external approaches for computing combine operators, which might not always be available (e.g., for upcoming architectures).

Workarounds have been proposed by the polyhedral community to target reduction-like computations [Doerfert et al. 2015; Reddy et al. 2016]. However, these approaches are limited to a subset of computations, e.g., by not supporting user-defined scalar types [Doerfert et al. 2015] (as required for our PRL example in Figure 16), or by being limited to GPUs only [Reddy et al. 2016]. Comparing the semantic information captured in the polyhedral model vs our MDH-based representation have been the focus of discussions between polyhedral experts and MDH developers [Google SIG MLIR Open Design Meeting 2020].

Portability. The polyhedral approach, in its general form, is a framework offering transformation rules (affine transformations), and each individual polyhedral compiler implements a set of such transformations which are then instantiated (e.g., with particular tile sizes) and applied when compiling a particular application. However, individual polyhedral compilers (e.g., PPCG and Pluto) apply a fixed set of affine transformations, thereby directly generating a schedule that is optimized for a particular target architecture only, e.g., only GPU (as PPCG) or only CPU (as Pluto), and it remains open which affine transformations have to be used and how for other architectures, e.g., upcoming accelerators for deep learning computations [Hennessy and Patterson 2019] with potentially more complex memory and core hierarchies than GPUs and CPUs. Moreover, while we introduce an explicit low-level representation (Section 3), the polyhedral approach does not

introduce representations on different abstraction levels: the model relies on one representation that is transformed via affine transformations. Apart from the ability of our low-level representation to handle combine operators (which we consider as complex and important), we see the advantages of our explicit low-level representation in, for example, explicitly representing memory regions, which allows formally defining important correctness constraints, e.g., that GPU architectures allow combining the results of threads in designated memory regions only – shared and device memory, but not registers (outlined in Section C.1 of our Appendix). Furthermore, our low-level representation also allows straightforwardly generating executable code from it (focus of Section E in our Appendix, and planned to be discussed thoroughly in future work). In contrast, code generation from the polyhedral model has proven challenging [Bastoul et al. 2022; Grosser et al. 2015; Vasilache et al. 2022].

Productivity. Most polyhedral compilers achieve high user productivity, by fully automatically parallelizing and optimizing straightforward sequential code (as Pluto and PPCG). Our approach currently relies on a DSL (Domain-Specific Language) for expressing computations, as discussed in Section 2; thus, our approach can be considered as less productive than many polyhedral compilers. However, Rasch et al. [2020a,b] confirm that DSL programs in our approach can be automatically generated from sequential code (optionally annotated with simple, OpenMP-like directives for expressing combine operators, enabling advanced optimizations), by using polyhedral tool `pet` [Verdoolaege and Grosser 2012] as a frontend for our approach. Thereby, we are able to achieve the same, high user productivity as polyhedral compilers. We consider this direction – combing the polyhedral model with our approach – as promising, as it enables benefitting from the advantages of both directions: optimizing sequential programs and making them parallelizable using polyhedral techniques (like *loop skewing*, as also outlined in Section 6.5), and mapping the optimized and parallelizable code eventually to parallel architectures based on the concepts and methodologies introduced in this paper.

6.3 Functional Approaches

Functional approaches map data-parallel computations that are expressed via small, formally defined building blocks (a.k.a. patterns [Gorlatch and Cole 2011]), such as `map` and `reduce`, to the memory and core hierarchies of parallel architectures, based on a strong formal foundation. Notable functional approaches include Accelerate [Chakravarty et al. 2011], Obsidian [Svensson et al. 2011], so-called *skeleton libraries* [Aldinucci et al. 2017; Enmyren and Kessler 2010; Ernstsson et al. 2018; Steuwer et al. 2011], and the modern Lift approach [Steuwer et al. 2015] (recently also known as RISE [Steuwer et al. 2022]).

In the following, as functional approaches usually follow the same basic concepts and methodologies, we focus on comparing to Lift, because Lift is more recent than, e.g., Accelerate and Obsidian.

Performance. Functional approaches tend to struggle with achieving their full performance potential, often caused by the design of their optimization spaces. For example, analogously to our approach, functional approach Lift relies on an internal low-level representation [Steuwer et al. 2017] that is used as target for Lift's high-level programs. However, Lift's transformation process, from high level to low level, turned out to be challenging: Lift's lowering process relies on an infinitely large optimization space – identifying a well-performing configuration within that space is too complex to be done automatically, in general, due to the space's large and complex structure. As a workaround, Lift currently uses approach Elevate [Hagedorn et al. 2020b] to incorporate user knowledge into the optimization process; however, at the cost of productivity, as manually expressing optimization is challenging, particularly for non-expert users.

In contrast, our optimization process is designed as auto-tunable (Table 1), thereby achieving fully automatically high performance, as confirmed in our experiments (Section 5), without involving the user for optimization decisions. In particular, our previous work already showed that our approach – even in its original version [Rasch and Gorlatch 2016; Rasch et al. 2019a] – can significantly outperform Lift on GPU and CPU [Rasch et al. 2019a]. Our performance advantage over Lift is mainly caused by the design of our optimization process: relying on formally defined tuning parameters (Table 1) – rather than on formal transformation rules that span a too large and complex search space, as in Lift – thereby contributing to a simpler, fully auto-tunable optimization process.

Portability. The current functional approaches usually are designed and optimized toward code generation in a particular programming model only. For example, Lift inherently relies on the OpenCL programming model, because OpenCL works for multiple kinds of architectures: NVIDIA GPU, Intel CPU, etc. However, we see two major disadvantages in addressing the portability issue via OpenCL only: 1) GPU-specific optimizations (such as *shuffle operations* [NVIDIA 2018]) are available only in the CUDA programming model, but not OpenCL; 2) the set of OpenCL-compatible devices is broad but still limited; in particular, in the *new golden age for computer architectures* [Hennessy and Patterson 2019], upcoming architectures are arising continuously and may not support the OpenCL standard. We consider targeting new programming models as challenging for Lift, as its formal low-level representation is inherently designed for OpenCL [Steuwer et al. 2017]; targeting further programming models with Lift would require the design and implementation of new low-level representations, which we do not consider as straightforward.

To allow easily targeting new programming models with our approach, we have designed our formalism as generic in the target model: our low-level representation (Figure 19) and optimization space (Table 1) are designed and optimized toward an abstract system model (Definition 11) which is capable of representing the device models of important programming approaches, including OpenMP, CUDA, and OpenCL (Example 11). Furthermore, we have designed our high- and low-level representations as minimalistic (Figures 15 and 19), e.g., by relying on three higher-order functions only for expressing programs at the high abstraction level, which simplifies and reduces the development effort for implementing code generators for programming models.

In addition, we believe that compared to our approach, the following basic design decisions of Lift (and similar functional approaches) complicate the process of code generation for them and increase the development effort for implementing code generators: 1) relying on a vast set of small patterns for expressing computations, rather than aiming at a minimalistic design as we do (also discussed in Section 5.3); 2) relying on complex function nestings and compositions for expressing computations, rather than avoiding nesting and relying on a fixed composition structure of functions, as in our approach (Figure 5); 3) requiring new patterns for targeting new classes of data-parallel computations (such as patterns `slide` and `pad` for stencils [Hagedorn et al. 2018]), which have to be non-trivially integrated into Lift's type and optimization system (often via extensions of the systems [Hagedorn et al. 2018; Remmelg et al. 2016]), instead of relying on a fixed set of expressive patterns (Figure 15) and generalized optimizations (Table 1) that work for various kinds of data-parallel computations (Figure 16); 4) expressing high-level and low-level concepts in the same language, instead of separating high-level and low-level concepts for a more structured and thus simpler code generation process (Figure 4). We consider these four design decisions as disadvantageous for code generation, because they require from a code generator handling various kinds of patterns (decision 1), and the patterns need to be translated to significantly different code variants, depending on their nesting level and composition order (decision 2). Moreover, each extension of patterns (decision 3) might affect code generation also for the already supported patterns, because the existing patterns need to be combined with the new ones via composition and

nesting (decision 2). We consider mixing up high-level and low-level concepts in the same language (decision 4) as further complicating the code generation process, because code generators cannot be implemented in clear, distinct stages: *high-level language → low-level language → executable program code.*

Productivity. Functional approaches are expressive frameworks – to the best of our knowledge, the majority of these approaches should be able to express (possibly after some extension) many of the high-level programs that can also be expressed via our high-level representation (e.g., those presented in Figure 16).

A main difference we see between the high-level representations of existing functional approaches and the representation introduced by our approach is that the existing approaches rely on a vast set of higher-order functions for expressing computations; these functions have to be functionally composed and nested in complex ways for expressing computations. For example, expressing matrix multiplication in Lift requires also involving Lift's pattern `transpose` (also when operating on non-transposed input matrices) [Remmelg et al. 2016], as per design in Lift, multi-dimensional data is considered as an array of arrays (rather than a multi-dimensional array, as in our approach as well as polyhedral approaches). In contrast, we aim to keep our high-level language minimalistic, by expressing data-parallel computations using exactly three higher-order functions and which are always used in the same, fixed order (shown in Figure 5). Work-in-progress results confirm that due to the minimalistic and structured design of our high-level representation, programs in our representation can even be systematically generated from straightforward, sequential program code [Rasch et al. 2020a,b].

Functional approaches also tend to require extension when targeting new application areas, which hinders the expressivity of the frameworks and thus also their productivity. For example, functional approach Lift [Steuwer et al. 2015] required notable extension for targeting, e.g., matrix multiplications (so-called *macro-rules* had to be added to Lift [Remmelg et al. 2016]) and stencil computations (primitives `slide` and `pad` were added and Lift's tiling optimization had to be extended toward *overlapped tiling* [Hagedorn et al. 2018]). In contrast, the generality of our approach allows expressing matrix multiplications and stencils out of the box, without relying on domain-specific building blocks.

6.4 Domain-Specific Approaches

Many approaches focus on code generation and optimization for particular domains. A popular domain-specific approach is *ATLAS* [Whaley and Dongarra 1998] which offers a convenient user interface for automatically generating and optimizing CPU code for the domain of linear algebra[26]. Similarly to ATLAS, approach *FFTW* [Frigo and Johnson 1998] is specifically designed and optimized for *Fast Fourier Transform (FFT)*, and *SPIRAL* [Puschel et al. 2005] targets the domain of *Digital Signal Processing (DSP)*.

Nowadays, the best performing, state-of-practice domain-specific approaches are often provided by vendors and specifically designed and optimized toward their target application domain and also architecture. For example, the popular vendor library NVIDIA cuBLAS [NVIDIA 2022b] is optimized by hand, on the assembly level, toward computing linear algebra routines on NVIDIA GPUs – cuBLAS is considered in the community as gold standard for computing linear algebra routines on GPUs. Similarly, Intel's oneMKL library [Intel 2022c] computes with high performance linear algebra routines on Intel CPUs, and libraries NVIDIA cuDNN [NVIDIA 2022e] and Intel

[26] Previous work [Rasch et al. 2021] shows that MDH (already in its original, proof-of-concept implementation) achieves higher performance than ATLAS.

oneDNN [Intel 2022b] work well for convolution computations on either NVIDIA GPU (cuDNN) or Intel CPU (oneDNN), respectively.

In the following, we discuss domain-specific approaches in terms of *performance*, *portability*, and *productivity*.

Performance. Domain-specific approaches, such as cuBLAS and cuDNN, usually achieve high performance. This is because the approaches are hand-optimized by performance experts – on the assembly level – to exploit the full performance potential of their target architecture. In our experiments, we show that our approach often achieves competitive and sometimes even better performance than domain-specific approaches provided by NVIDIA and Intel, which is mainly due to their portability issues over different data characteristics, as we discuss in the next paragraph.

Portability. Domain-specific approaches usually struggle with achieving portability over different architectures. This is because the approaches are often implemented in architecture-specific assembly code to achieve high performance. The domain-specific approaches often also struggle with achieving portability over different characteristics of their input and output data: they usually rely on a set of pre-implemented implementations that are each designed and optimized toward average high performance over a range of input characteristic (e.g., their sizes). In contrast, our approach (as well as many scheduling and polyhedral approaches) allow automatically optimizing (auto-tuning) kernels for particular data characteristics, which is important for performance [Tillet and Cox 2017], thereby often achieving higher performance than domain-specific approaches for advanced data characteristics (small, uneven, irregularly shaped, ...), e.g., as used in deep learning. The costly time for auto-tuning is well amortized in many application areas, because the auto-tuned implementations are re-used in many program runs. Moreover, auto-tuning avoids the time-intensive and costly process of hand optimization by human experts.

Productivity. Domain-specific approaches usually achieve highest productivity for their target domain (e.g., linear algebra), by providing easy to use high-level abstractions. However, the approaches suffer from significant expressivity issues, because – per design – they are inherently restricted to their target application domain only. Also, the approaches are often inherently bound to only particular architectures, e.g., only GPU (as NVIDIA cuBLAS and cuDNN) or only CPU (as Intel oneMKL and oneDNN). Domain-specific vendor libraries, such as NVIDIA cuBLAS and Intel oneMKL, also tend to offer the user differently performing variants of computations; the variants have to be naively tested by the user when striving for the full performance potentials of approaches (as discussed in Section 5.4), which is cumbersome for the user.

6.5 Higher-Level Approaches

There is a broad range of existing work that is focused on higher-level optimizations than proposed by this work. We consider such higher-level approaches as greatly combinable with our approach. For example, the polyhedral approach is capable of expressing algorithmic-level optimizations, like *loop skewing* [Wolf and Lam 1991], to make programs parallelizable; such optimizations are beyond the scope of this work, but they can be combined with our approach as demonstrated by Rasch et al. [2020a,b]. Similarly, we consider approaches introduced by Farzan and Nicolet [2019]; Frigo et al. [1999]; Gunnels et al. [2001]; Yang et al. [2021], which also focus on algorithmic-level optimizations, as greatly combinable with our approach: algorithmically optimizing user code according to the approaches' techniques, and using our methodologies to eventually map the optimized code to low-level code for parallel architectures.

Futhark [Henriksen et al. 2017], Dex [Paszke et al. 2021], and ATL [Liu et al. 2022] are further approaches focussed on high-level program transformations, like advanced *flattening* mechanisms [Henriksen et al. 2019], thereby optimizing programs at the algorithmic level of abstraction. We consider using our work as backend for these approaches as promising: the three approaches often struggle with mapping their algorithmically optimized program variants eventually to the multi-layered memory and core hierarchies of state-of-the-art parallel architectures, which is exactly the focus of this work.

6.6 Existing Work on MDH

Our work is inspired by the algebraic approach of Multi-Dimensional Homomorphisms (MDHs) which is introduced in the work-in-progress paper [Rasch and Gorlatch 2016]. The MDH approach, as presented in the previous work, relies on a semi-formal foundation and focuses on code generation for the OpenCL programming model only [Rasch et al. 2019a]. This work makes major contributions over the existing work on MDHs and its OpenCL code generation approach.

We introduce a full formalization of MDH's high-level program representation. In our new formalism, we rely on expressive typing: for example, we encode MDHs' data sizes into our type system, e.g., by introducing both *index sets* for MDAs (Definition 1) and *index set functions* for combine operators (Definition 2), and we respect and maintain these sets and functions thoroughly during MDH computations (Definition 3). Our expressive typing significantly contributes to correct and simplified code generation, as all relevant type and data size information are contained in our formal, low-level program representation (Figure 19) from which we eventually generate executable program code (Section 3). In contrast, the existing MDH work considers multi-dimensional arrays (MDAs) of arbitrary sizes and dimensionalities to be all of the same, straightforward type, which has greatly simplified the design of the proof-of-concept MDH formalism introduced by Rasch and Gorlatch [2016] (in particular, the definition and usage of combine operators), but at the cost of significantly harder and error-prone code generation: all the missing, type-relevant information need to be elaborated by the implementer of the code generator in the existing MDH work, e.g., allocation sizes of fast memory resources used for caching input data or for storing computed intermediate results. Furthermore, while the original MDH work [Rasch and Gorlatch 2016] is focused on introducing higher-order function `md_hom` only, this work in particular also introduces higher order functions `inp_view` and `out_view` (Section 2.3) which express input and output views in a formally structured and concise manner, and which are central building blocks for expressing computations (Figure 16). Also, by introducing and exploiting the index set concept for MDAs, we have improved the definition of the concatenation operator ++ (Example 1) toward commutativity, which is required for important optimizations. e.g., loop permutations (expressed via Parameters `D1`, `S1`, `R1` in Table 1).

A further substantial improvement is the introduction of our low-level representation (Section 3). It relies on a novel combination of tuning parameters (Table 1) that enhance, generalize, and extend the existing, proof-of-concept MDH parameters which capture a subset of OpenCL-orientated features only [Rasch et al. 2019a]. Moreover, while the existing MDH work introduces formally only parameters for flexibly choosing numbers of threads [Rasch and Gorlatch 2016] (which corresponds to a very limited variant of our tuning parameter `0` in Table 1, because our parameter `0` also choses numbers of memory tiles and is not restricted to OpenCL); the other OpenCL parameters are introduced and discussed by Rasch et al. [2019a] only informally, from a technical perspective. With our novel parameter set, we are able to target various kinds of programming models (e.g., also CUDA, as in Section 5) and also to express important optimizations that are beyond the existing work on MDH, e.g., optimizing the memory access pattern of MDH computations: for example, we achieve speedups $> 2\times$ over existing MDH for the deep learning computations discussed in Section 5.

Our new tuning parameters are expressive enough to represent state-of-the-art, data-parallel implementations, e.g., as generated by scheduling and polyhedral approaches (Figures 20-23), and our experiments in Section 5 confirm that auto-tuning our parameters enables performance beyond the state of the art, including hand-optimized solutions provided by vendors, which is not possible when using the existing MDH approach. The expressivity of our parameters in particular also enables comparing significantly differently optimized implementations (e.g., scheduling-optimized vs. polyhedral-optimized, as in Section 3.5), based on the values of formally specified tuning parameters, which we consider as promising for structured performance analysis in future work. Moreover, our new low-level representation targets architectures that may have arbitrarily deep memory and core hierarchies, by having optimized our representation toward an *Abstract System Model* (Definition 11). In contrast, the existing MDH work is focused on OpenCL-compatible architectures only.

Our experimental evaluation extends previous MDH experiments by comparing also to the popular state-of-practice approach TVM which is attracting increasing attention from both academia [Apache Software Foundation 2021] and industry [OctoML 2022]. Also, we compare to the popular polyhedral compilers PPCG and Pluto, as well as the currently newest versions of hand-optimized high-performance libraries provided by vendors. Furthermore, we have included a real-world case study in our experiments, considering the most time-intensive computations within the three popular deep learning neural networks `ResNet-50`, `VGG-16`, and `MobileNet`; the study also includes Capsule-style convolution computations, which are considered as challenging to optimize [Barham and Isard 2019]. Moreover, Table 16 analyzes MDH's expressivity using new examples: it shows that MDH – based on the new contributions of this work (e.g., view functions) – is capable of expressing computations `bMatMuL`, `MCC_Capsule`, `Histo`, `scan`, and `MBBS`, which have not been expressed via MDH in previous work. Our experiments confirm that we achieve high performance for `bMatMuL` and `MCC_Capsule` on GPUs and CPUs, and our future work aims to thoroughly analyze our approach for computations `Histo`, `scan`, and `MBBS` in terms of performance, portability, and productivity.

7 CONCLUSION

We introduce a formal (de/re)-composition approach for data-parallel computations targeting state-of-the-art parallel architectures. Our approach aims to combine three major advantages over related approaches – performance, portability, and productivity – by introducing formal program representations on both: 1) high level, for conveniently expressing – in one uniform formalism – various kinds of data-parallel computations (including linear algebra routines, stencil computations, data mining algorithms, and quantum chemistry computations), agnostic from hardware and optimization details, while still capturing all information relevant for generating high-performance program code; 2) low level, which allows uniformly reasoning – in the same formalism – about optimized (de/re)-compositions of data-parallel computations targeting different kinds of parallel architectures (GPUs, CPUs, etc). We lower our high-level representation to our low-level representation, in a formally sound manner, by introducing a generic search space that is based on performance-critical parameters. The parameters of our lowering process enable fully automatically optimizing (auto-tuning) our low-level representations for a particular target architecture and characteristics of the input and output data, and our low-level representation is designed such that it can be straightforwardly transformed to executable program code in imperative-style programming approaches (including OpenMP, CUDA, and OpenCL). Our experiments confirm that due to the design and structure of our generic search space in combination with auto-tuning, our approach achieves higher performance on GPUs and CPUs than popular state-of-practice approaches, including hand-optimized libraries provided by vendors.

8 FUTURE WORK

We consider this work as a promising starting point for future directions. A major future goal is to extend our approach toward expressing and optimizing simultaneously multiple data-parallel computations (e.g., matrix multiplication followed by convolution), rather than optimizing computations individually and thus independently from each other only (e.g., only matrix multiplication or only convolution). Such extension enables optimizations, such as *kernel fusion*, which is important for the overall application performance and considered as challenging [Fukuhara and Takimoto 2022; Li et al. 2022; Wahib and Maruyama 2014]. We see this work as a promising foundation for our future goal, because it enables expressing and reasoning about different computations in the same formal framework. Targeting computations on sparse input/output data formats, inspired by Ben-Nun et al. [2017]; Hall [2020]; Kjolstad et al. [2017]; Pizzuti et al. [2020], is a further major goal, which requires extending our approach toward irregularly-shaped input and output data, similarly as done by Pizzuti et al. [2020]. Regarding our optimization process, we aim to introduce an analytical cost model for computations expressed in our formalism – based on operational semantics – thereby accelerating (or even avoiding) the auto-tuning overhead, similarly as done by Li et al. [2021]; Muller and Hoffmann [2021]. Moreover, we aim to incorporate machine-learning based methods into our optimization process [Leather et al. 2014], instead of relying on empirical auto-tuning methods only. To make our work better accessible for the community, we aim to implement our approach into *MLIR* [Lattner et al. 2021] which offers a reusable compiler infrastructure. The contributions of this work give a precise, formal recipe of how to implement our introduced methods into approaches like MLIR. Moreover, relying on the MLIR framework will contribute to a structured code generation process in assembly-level programming models, like LLVM [Lattner and Adve 2004] and NVIDIA PTX [NVIDIA 2022i]. We consider targeting assembly languages as important for our future work: assembly code offers further, low-level optimization opportunities [Goto and Geijn 2008; Lai and Seznec 2013], thereby enabling our approach to potentially achieve higher performance than presented in this work for our MDH-generated CUDA and OpenCL code. Also, we aim to extend our approach toward distributed multi-device systems that are heterogeneous, inspired by dynamic load balancing approaches [Chen et al. 2010] and advanced data distributions techniques [Yadav et al. 2022]. Targeting domain-specific hardware extensions, such as *NVIDIA Tensor Cores* [NVIDIA 2017], is also an important goal for our future work, as such extensions allow significantly accelerating computations for the target of the extensions (e.g., deep learning [Markidis et al. 2018]).

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APPENDIX

Our Appendix provides details for the interested reader, which should not be required for understanding the basic ideas presented in this paper.

A MATHEMATICAL FOUNDATION

We rely on a set theoretical foundation, based on ZFC set theory [Ciesielski 1997]. We avoid class theory, such as NBG [von Neumann 1925], by assuming, for example, that our universe of types contains all relevant representatives (`int`, `float`, `struct`, etc), but is not the "class of all types". Thereby, we avoid fundamental issues [Russell 2020] which are not relevant for this work.

A.1 Family

Definition 17 (Family)**.** Let I and A be two sets. A *family* F from I to A is any set

$$F := \{ \ (i, a) \mid i \in I \wedge a \in A \ \}$$

such that the following two properties are satisfied:

- *left-total*: $\forall i \in I : \ \exists a \in A : \ (i, a) \in F$
- *right-unique*: $(i, a) \in F \ \wedge \ (i, a') \in F \ \Rightarrow \ a = a'$

We refer to I also as *index set* of family F and to A as F's *image set*. If I has a strict total order $<$, we refer to F also as *ordered family*.

Notation 4 (Family)**.** Let F be a family from I to A.
We write:

- F_i for the unique $a \in A$ such that $(i, a) \in F$;
- $(F_i)_{i \in I}$ instead of F to explicitly state F's index and image sets in our notation;
- $(\ F_{i_1,\ldots,i_n} \ )_{i_1 \in I_1,\ldots,i_n \in I_n}$ instead of $(\ldots (\ F_{i_1,\ldots,i_n} \ )_{i_n \in I_n} \ \ldots)_{i_1 \in I_1}$.

Alternatively, depending on the context, we use the following notation:

- $F^{<i>}$ instead of F_i;
- $(F_i)^{<i \in I>}$ instead of $(F_i)_{i \in I}$;
- $(\ F_{i_1,\ldots,i_n} \ )^{<i_1 \in I_1 \mid \ldots \mid i_n \in I_n>}$ instead of $(\ F_{i_1,\ldots,i_n} \ )_{i_1 \in I_1,\ldots,i_n \in I_n}$.

For nested families, each index set I_k may depend on the earlier-defined values $i_1, \ldots, i_{k-1}$ (not explicitly stated above for brevity).

Definition 18 (Tuple)**.** We identify n-tuples as families that have index set $[1, n]_{\mathbb{N}}$.

Example 12 (Tuple)**.** A 2-tuple (a, b) (a.k.a *pair*) is a family $(F_i)_{i \in I := [1,2]_{\mathbb{N}}}$ for which $F_1 = a$ and $F_2 = b$.

A.2 Scalar Types

We denote by

$$\texttt{TYPE} := \{ \ \texttt{int}, \texttt{int8}, \texttt{int16}, \ldots, \texttt{float}, \texttt{double}, \ldots, \texttt{struct}, \ldots \ \}$$

our set of *scalar types*, where `int8` and `int16` represent 8-bit/16-bit integer numbers, `float` and `double` are the types of single/double precision floating point numbers (IEEE 754 standards), `structs` contain a fixed set of other scalar types, etc. For simplicity, we interpret integer types (`int`, `int8`, `int16`, ...) uniquely as integers $\mathbb{Z}$, floating point number types (`float` and `double`) as rationale numbers $\mathbb{Q}$, etc.

For high flexibility, we avoid fixing TYPE to a particular set of scalar types, i.e., we assume that TYPE contains all practice-relevant types. This is legal, because our formalism makes no assumptions on the number and kinds of scalar types.

We consider operations on scalar types (addition, multiplication, etc) to be: 1) *atomic*: we do not aim at parallelizing or otherwise optimizing operations on scalar values in this work; 2) *size preserving*: we assume that all values of a scalar type have the same arbitrary but fixed size.

Note that we can potentially also define, for example, the set of arbitrarily sized matrices $\{T^{m \times n} \mid m, n \in \mathbb{N}, T \in \mathsf{TYPE}\}$ as scalar type in our approach. However, this would prevent any kind of formal reasoning about performance and type correctness of matrix-related operations (e.g., matrix multiplication), like parallelization (due to our atomic assumption above) or type correctness (e.g., assuring in matrix multiplication that number of columns of the first input matrix coincides with and number of rows of the second matrix: due to our size preservation assumption above, we would not be able to distinguish matrices based on their sizes).

A.3 Functions

Definition 19 (Function)**.** Let $A \in \mathsf{TYPE}$ and $B \in \mathsf{TYPE}$ be two scalar types.

A *(total) function* f is a tuple of the form

$$f \in \{ \; (\underbrace{(A, B)}_{\text{function type}} , \underbrace{G_f}_{\substack{\text{function} \\ \text{graph}}}) \mid G_f \subseteq \{ (a, b) \mid a \in A \wedge b \in B \} \; \}$$

that satisfies the following two properties:

- *left-total*: $\forall a \in A : \exists b \in B : (a, b) \in G_f$;
- *right-unique*: $(a, b) \in G_f \; \wedge \; (a, b') \in G_f \; \Rightarrow \; b = b'$.

We write $f(a)$ for the unique $b \in B$ such that $(a, b) \in G_f$. Moreover, we denote f's function type as $A \to B$, and we write $f : A \to B$ to state that f has function type $A \to B$.

We refer to:

- A as the *domain* of f
- B as the *co-domain* (or *range*) of f
- (A, B) as the *type* of f
- G_f as the *graph* of f

If f does not satisfy the left total property, we say f is *partial*, and we denote f's type as $f : A \to_p B$ (where $\to$ is replaced by $\to_p$).

We allow functions to have so-called *dependent types* [Xi and Pfenning 1999] for expressive typing. For example, dependent types enable encoding the sizes of families into the type system, which contributes to better error checking. We refer to dependently typed functions as *meta-functions*, as outlined in the following.

Definition 20 (Meta-Function)**.** We refer to any family of functions

$$(\; f^{<i>} : A^{<i>} \to B^{<i>} \;)^{<i \in I>}$$

as *meta-function*. In the context of meta-functions, we refer to index $i \in I$ also as *meta-parameter*, to index set I as *meta-parameter type*, to $A^{<i \in I>}$ and $B^{<i \in I>}$ as meta-types (as both are generic in meta-parameter $i \in I$), and to $A^{<i>} \to B^{<i>}$ for concrete i as meta-function f's ordinary function type.

In the following, we often write:

- $f^{<i \in I>} : A^{<i>} \to B^{<i>}$ instead of $(\; f^{<i>} : A^{<i>} \to B^{<i>} \;)^{<i \in I>}$;

- $f^{<i>} : A' \to B^{<I>}$ (or $f^{<i>} : A^{<i>} \to B'$) iff $A^{<i>} = A'$ (or $B^{<i>} = B'$) for all $i \in I$.

We use *multi-stage meta-functions* as a concept analogous to *multi staging* [Taha and Sheard 1997] in programming and similar to *currying* in mathematics.

Definition 21 (Multi-Stage Meta-Function)**.** A *multi-stage meta-function* is a nested family of functions:

$$f^{\overbrace{< i_1 \in I_1^{<>} >}^{\text{stage } 1} \ldots \overbrace{< i_S \in I_S^{<i_1,\ldots,i_{S-1}>} >}^{\text{stage } S} : \underbrace{A^{<i_1,\ldots,i_S>} \to B^{<i_1,\ldots,i_S>}}_{\texttt{function instance}}}$$

Here, $I_s^{<i_1,\ldots,i_{s-1}>}$, $s \in [1,S]_{\mathbb{N}}$, is the meta-parameter type on stage s, which may depend on all meta-parameters of the previous stages $i_1, \ldots, i_{s-1}$. We refer to such meta-functions also as *S-stage meta-functions*, and we denote their type also as

$$f^{<i_1 \in I_1 \mid \ldots \mid i_S \in I_S>} : A^{<i_1,\ldots,i_S>} \to B^{<i_1,\ldots,i_S>}$$

and access to them as

$$f^{<i_1 \mid \ldots \mid i_S>}(x)$$

where different stages are separated by vertical bars.

We allow partially applying parameters (meta and ordinary) of meta-functions.

Definition 22 (Partial Meta-Function Application)**.** Let

$$f^{<i_1 \in I_1 \mid \ldots \mid i_S \in I_S>} : A^{<i_1,\ldots,i_S>} \to B^{<i_1,\ldots,i_S>}$$

be a meta-function (meta-parameters of meta-types $I_1, \ldots, I_S$ omitted for brevity).

- The *partial application* of meta-function f on stage s to meta-parameter $\hat{i}_s$ is the meta-function

  $$f'^{<i_1 \in \hat{I}_1 \mid \ldots \mid i_{s-1} \in \hat{I}_{s-1} \mid i_{s+1} \in I_{s+1} \mid \ldots \mid i_S \in I_S>} : A^{<i_1,\ldots,i_{s-1},\hat{i}_s,i_{s+1}\ldots,i_S>} \to B^{<i_1,\ldots,i_{s-1},\hat{i}_s,i_{s+1},\ldots,i_S>}$$

  where $\hat{I}_1 \subseteq I_1, \ldots \hat{I}_{s-1} \subseteq I_{s-1}$ are the largest sets such that $\hat{i}_s \in I_s^{<i_1,\ldots,i_{s-1}>}$ for all $i_1 \in \hat{I}_1, \ldots, i_{s-1} \in \hat{I}_{s-1}$. The function is defined as:

  $$f'^{<i_1 \mid \ldots \mid i_{s-1} \mid i_{s+1} \mid \ldots \mid i_S>}(x) := f^{<i_1 \mid \ldots \mid i_{s-1} \mid \hat{i}_s \mid i_{s+1} \mid \ldots \mid i_S>}(x)$$

  We write for f''s type also

  $$f^{<i_1 \in \hat{I}_1 \mid \ldots \mid i_{s-1} \in \hat{I}_{s-1} \mid \hat{i}_s \mid i_{s+1} \in I_{s+1} \mid \ldots \mid i_S \in I_S>} : A^{<i_1,\ldots,i_{s-1},\hat{i}_s,i_{s+1}\ldots,i_S>} \to B^{<i_1,\ldots,i_{s-1},\hat{i}_s,i_{s+1},\ldots,i_S>}$$

  where f' is replaced by f and $i_s \in I_s$ is replaced by the concrete value $\hat{i}_s$.
- The *partial application* of meta-function f to ordinary parameter x is the meta-function

  $$f'^{<i_1 \in \hat{I}_1 \mid \ldots \mid i_S \in \hat{I}_S>} : \underbrace{B_1^{<i_1,\ldots,i_S>} \to B_2^{<i_1,\ldots,i_S>}}_{:= B^{<i_1,\ldots,i_S>}}$$

  where $\hat{I}_1 \subseteq I_1, \ldots \hat{I}_S \subseteq I_S$ are the largest sets such that $x \in A^{<i_1,\ldots,i_S>}$ for all $i_1 \in \hat{I}_1, \ldots, i_S \in \hat{I}_S$. The function is defined as:

  $$f'^{<i_1 \mid \ldots \mid i_S>}(x') := f^{<i_1 \mid \ldots \mid i_S>}(x)(x')$$

We allow *generalizing* meta-parameters. For example, by generalizing meta-parameters for input sizes, we can use functions on arbitrarily sized inputs (a.k.a. *dynamic size* in programming). In our generated code, meta-parameters are available at compile time such that concrete meta-parameter values can be exploited for generating well-performing code (e.g., for static loop boundaries). Consequently, generalization increases expressivity of the generated code, e.g., by being able to process differently sized inputs without requiring re-compilation for unseen input sizes, but usually at the cost of performance.

Definition 23 (Generalized Meta-Parameters)**.** Let

$$f^{<i_1 \in I_1 \mid \ldots \mid i_s \in I_s \mid \ldots \mid i_S \in I_S>} : A^{<i_1,\ldots,i_s,\ldots,i_S>} \to B^{<i_1,\ldots,i_s,\ldots,i_S>}$$

be a meta-function (meta-parameters of $I_1, \ldots, I_S$ omitted for brevity) such that

$$f^{<i_1 \mid \ldots \mid i_s \mid \ldots \mid i_S>}(x) = f^{<i_1 \mid \ldots \mid i'_s \mid \ldots \mid i_S>}(x)$$

i.e., f's behavior is invariant under different values of meta-parameter i_s in stage s.

The *generalization* of f in meta-parameter $s \in [1, S]_{\mathbb{N}}$ is the meta-function

$$f'^{<i_1 \in I_1 \mid \ldots \mid i_{s-1} \in I_{s-1} \mid i_{s+1} \in I_{s+1} \mid \ldots \mid i_S \in I_S>} :$$

$$\bigcup_{i_s \in I_s^{<i_1,\ldots,i_{s-1}>}} A^{<i_1 \mid \ldots \mid i_{s-1} \mid i_s \mid i_{s+1} \mid \ldots \mid i_S>} \to \bigcup_{i_s \in I_s^{<i_1,\ldots,i_{s-1}>}} B^{<i_1 \mid \ldots \mid i_{s-1} \mid i_s \mid i_{s+1} \mid \ldots \mid i_S>}$$

which is defined as:

$$f'^{<i_1 \mid \ldots \mid i_{s-1} \mid i_{s+1} \mid \ldots \mid i_S>}(x) := f'^{<i_1 \mid \ldots \mid i_s \mid i_{s+1} \mid \ldots \mid i_S>}(x)$$

for an arbitrary $i_s \in I_s$ such that $x \in A^{<i_1 \mid \ldots \mid i_{s-1} \mid i_s \mid i_{s+1} \mid \ldots \mid i_S>}$.

We write for f's type also

$$f^{<i_1 \in I_1 \mid \ldots \mid i_{s-1} \in I_{s-1} \mid * \in I_s \mid i_{s+1} \in I_{s+1} \mid \ldots \mid i_S \in I_S>} : A^{<i_1,\ldots,i_S>} \to B^{<i_1,\ldots,i_S>}$$

where i_s is replaced by $*$, and for access to f

$$f^{<i_1 \mid \ldots \mid i_{s-1} \mid * \mid i_{s+1} \mid \ldots \mid i_S>}(x)$$

We use *postponed meta-parameters* to change the order of meta-parameters of already defined meta-functions. For example, we use postponed meta-parameters in Definition 8 to compute the values of meta-parameters based on the particular meta-parameter values of later stages.

Definition 24 (Postponed Meta-Parameters)**.** Let

$$f^{<i_1 \in I_1 \mid \ldots \mid i_s \in I_s \mid \ldots \mid i_S \in I_S>} : A^{<i_1,\ldots,i_s,\ldots,i_S>} \to B^{<i_1,\ldots,i_s,\ldots,i_S>}$$

be a meta-function (meta-parameters of $I_1, \ldots, I_S$ omitted via ellipsis for brevity) such that for each $k \in (s, S]_{\mathbb{N}}$, it holds:

$$I_k^{<i_1 \mid \ldots \mid i_s \mid \ldots \mid i_{k-1}>} = I_k^{<i_1 \mid \ldots \mid i'_s \mid \ldots \mid i_{k-1}>}$$

i.e., the I_k are invariant under different values of meta-parameter i_s in stage s, such that i_s can be ignored in the parameter list of I_k.

Function f' is function f *postponed* on stage s to meta-type

$$\hat{I}_s^{<i_1 \mid \ldots \mid i_{s-1} \mid i_{s+1} \mid \ldots \mid i_S>} \subseteq I_s^{<i_1 \mid \ldots \mid i_{s-1}>}$$

which, in contrast to I_s, may also depend on meta-parameter values $i_{s+1}, \ldots, i_S$, iff f' is of type

$$f'^{<i_1 \in I_1^{<\ldots>} \mid \ldots \mid i_{s-1} \in I_{s-1}^{<\ldots>} \mid i_{s+1} \in I_{s+1}^{<\ldots>} \mid \ldots \mid i_S \in I_S^{<\ldots>} >< i_s \in \hat{I}_s^{<i_1,\ldots,i_S>}>} : A^{<i_1,\ldots,i_s,\ldots,i_S>} \to B^{<i_1,\ldots,i_s,\ldots,i_S>}$$

and defined as:

$$f'^{<i_1|\ldots|i_{s-1}|i_{s+1}|\ldots|i_S><i_s>}(a) = f^{<i_1|\ldots|i_{s-1}|i_s|i_{s+1}|\ldots|i_S>}(a)$$

We write for f''s type also

$$f^{<i_1\in I_1^{<\ldots>}|\ldots|i_{s-1}\in I_{s-1}^{<\ldots>}|\rightarrow|i_{s+1}\in I_{s+1}^{<\ldots>}|\ldots|i_S\in I_S^{<\ldots>}><i_s\in \hat{I}_s^{<\ldots>}>} : A^{<i_1,\ldots,i_s,\ldots,i_S>} \rightarrow B^{<i_1,\ldots,i_s,\ldots,i_S>}$$

where f' is replaced by f and i_s by symbol "→". For access to f', we write

$$f^{<i_1|\ldots|i_{s-1}|\rightarrow|i_{s+1}|\ldots|i_S><i_s>}(x)$$

When using a binary function for combining a family of elements, we often use the following notation.

Notation 5 (Iterative Function Application)**.** Let $\circledast : T \times T \rightarrow T$ be an arbitrary associative and commutative binary function on scalar type $T \in \texttt{TYPE}$. Let further x be an arbitrary family that has index set $I := \{i_1, \ldots, i_N\}$ and image set $\{x_i\}_{i\in I} \subseteq T$.

We write $\underset{i\in I}{\circledast} x_i$ instead of $x_{i_1} \circledast \ldots \circledast x_{i_N}$ (infix notation).

A.4 MatVec Expressed in MDH DSL

Our MatVec example from Figure 6 is expressed in MDH's high-level *Domain-Specific Language (DSL)*, used as input by our proof-of-concept MDH compiler, as follows:

```
1 MatVec<T in TYPE | I,K in IN> :=
2       out_view<T>( w:(i,k)->(i) ) o
3         md_hom<I,K>( *, (++,+) ) o
4           inp_view<T,T>( M:(i,k)->(i,k) ,
5                          v:(i,k)->(k)   )
```

Listing 5. MatVec expressed in MDH's DSL

Our compiler takes an expresssion as in Listing 5 as input, and it generates auto-tunable code from it, according to the methods presented in this paper (particularly in Section E). Our compile times currently vary for our examples in Figure 16 from < 1 Minute for low-dimensional examples (e.g., linear algebra routines) to 5 Minutes for high-dimensional examples (such as quantum chemistry computations). We aim to significantly reduce our compile times and to desribe our code generation process in our future work, as code generation is not the focus of this paper.

In addtion, we also offer an implementation of our MDH approach and its high-level DSL embedded in the *Python* programming language [Schulze 2023], as Python is becoming increasingly popular in both academia and industry [TIOBE 2023].

B ADDENDUM SECTION 2

B.1 Design Decisions: Combine Operators

We list some design decisions for combine operators (Definition 2).

Note 1.

- We deliberately restrict index set function $\Rightarrow^{\text{MDA}}_{\text{MDA}}$ to compute the index set in the particular dimension d only, and not of all D Dimensions (i.e., the function's output is in MDA-IDX-SETs and not MDA-IDX-SETs^D), because this enables applying combine operator $\circledast$ iteratively:

$$(\ldots((a_1 \circledast^{<(P,Q)>} a_2) \circledast^{<(P\cup Q,R)>} a_3) \circledast^{<(P\cup Q\cup R,\ldots)>} \ldots$$

for MDAs $\mathfrak{a}_1, \mathfrak{a}_2, \mathfrak{a}_3, \ldots$ that have index sets $\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(P), \Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(Q), \Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(R), \ldots$ in dimension d. This is because the index set of the output MDA changes only in dimension d, to the new index set $\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(P \cup Q)$, $\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(P \cup Q) \cup R), \ldots$, so that the output MDA can be used as input for a new application of $\circledast$.

- It is a design decision that a combine operator's index set function $\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}$ takes as input the MDA index set P or Q in the particular dimension d only, rather than the all sets $(I_1, \ldots, I_D)$. Our approach can be easily extended to index set functions $\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}} : \mathtt{MDA\text{-}IDX\text{-}SETs}^D \rightarrow \mathtt{MDA\text{-}IDX\text{-}SETs}$ that take the entire MDA's index sets as input. However, we avoid this additional complexity, because we are currently not aware of any real-world application that would benefit from such extension.
- For better convenience, we could potentially define the meta-type of combine operators (Definition 2) such that meta-parameter $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D)$ is separated from parameter (P, Q) in a distinct, earlier stage (Definition 21). This would allow automatically deducing $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D)$ from the input MDAs' types, whereas for meta-parameter (P, Q), automatic deduction is usually not possible: function $\Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}$ has to be either invertible for automatically deducing P and Q from the input MDAs or invariant under different values of P and Q. Consequently, separating parameter $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D)$ in a distinct, earlier stage would allow avoiding explicitly stating this parameter, by deducing it from the input MDAs' type, and only explicitly stating parameter (P, Q), e.g., $\circledast_2^{<(P,Q)>}(a, b)$ instead of $\circledast_2^{<(I_1)\,|\,(P,Q)>}(a, b)$ for $a \in T[I_1, \Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(P)]$ and $b \in T[I_1, \Rightarrow^{\mathsf{MDA}}_{\mathsf{MDA}}(Q)]$.
  We avoid separating $(I_1, \ldots, I_{d-1}, I_{d+1}, \ldots, I_D)$ and (P, Q) in this work, as we focus on concatenation (Example 1), prefix-sum (Example 15), and point-wise combination (Example 2) only, which have invertible or P/Q-invariant index set functions, respectively. Consequently, for the practice-relevant combine operators considered in this work, we can deduce all meta-parameters automatically.

B.2 Generalized Notion of MDHs

The MDH Definition 3 can be generalized to have an arbitrary algebraic structure as input.

Definition 25 (Multi-Dimensional Homomorphism)**.** Let

$$\mathcal{A}^{\downarrow} := \left(T^{\mathsf{INP}}[\overset{1}{\Rightarrow}^{\mathsf{MDA}\downarrow}_{\mathsf{MDA}}(*), \ldots, \overset{D}{\Rightarrow}^{\mathsf{MDA}\downarrow}_{\mathsf{MDA}}(*)] \,,\, ({}^{\downarrow}\circledast_d)_{d \in [1,D]_{\mathbb{N}}} \right)$$

and

$$\mathcal{A}^{\uparrow} := \left(T^{\mathsf{OUT}}[\overset{1}{\Rightarrow}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(*), \ldots, \overset{D}{\Rightarrow}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(*)] \,,\, ({}^{\uparrow}\circledast_d)_{d \in [1,D]_{\mathbb{N}}} \right)$$

be two algebraic structures, where

$$({}^{\downarrow}\circledast_d \in \mathsf{CO}^{<\overset{d}{\Rightarrow}^{\mathsf{MDA}\downarrow}_{\mathsf{MDA}} \,|\, T^{\mathsf{INP}} \,|\, D \,|\, d>})_{d \in [1,D]_{\mathbb{N}}}$$

and

$$({}^{\uparrow}\circledast_d \in \mathsf{CO}^{<\overset{d}{\Rightarrow}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}} \,|\, T^{\mathsf{OUT}} \,|\, D \,|\, d>})_{d \in [1,D]_{\mathbb{N}}}$$

are tuples of combine operators, for $D \in \mathbb{N}$, $T^{\mathsf{INP}}, T^{\mathsf{OUT}} \in \mathsf{TYPE}$, $\overset{d}{\Rightarrow}^{\mathsf{MDA}\downarrow}_{\mathsf{MDA}}, \overset{d}{\Rightarrow}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}} : \mathtt{MDA\text{-}IDX\text{-}SETs} \rightarrow \mathtt{MDA\text{-}IDX\text{-}SETs}$, and the two structures' carrier sets

$$T^{\mathsf{INP}}[\overset{1}{\Rightarrow}^{\mathsf{MDA}\downarrow}_{\mathsf{MDA}}(*), \ldots, \overset{D}{\Rightarrow}^{\mathsf{MDA}\downarrow}_{\mathsf{MDA}}(*)]$$

and

$$T^{\mathsf{OUT}}[\overset{1}{\Rightarrow}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(*), \ldots, \overset{D}{\Rightarrow}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(*)]$$

denote the set of MDAs that are in the function domain of combine operators (the star symbol is used for indicating the function range of index functions).

A *Multi-Dimensional Homomorphism (MDH)* from the algebraic structure $\mathcal{A}^{\downarrow}$ to the structure $\mathcal{A}^{\uparrow}$ is any function

$$h^{<I_1,\ldots,I_D \in \texttt{MDA-IDX-SETs}>} : T^{\texttt{INP}}[\overset{1}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}(I_1),\ldots,\overset{D}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}(I_D)] \rightarrow T^{\texttt{OUT}}[\overset{1}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\uparrow}(I_1),\ldots,\overset{D}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\uparrow}(I_D)]$$

that satisfies the *homomorphic property*:

$$h(\ a_1 \,{}^{\downarrow}\!\otimes_d\, a_2\ ) \;=\; h(a_1)\,{}^{\uparrow}\!\otimes_d\, h(a_2)$$

The MDH Definition 3 is a special case of our generalized MDH Definition 25 above, for ${}^{\downarrow}\otimes_d = +\!\!+^{<T^{\texttt{INP}}\,|\,D\,|\,d>}$ (Example 1).

Higher-order function `md_hom` (originally introduced in Definition 4) is defined for the generalized MDH Definition 25 as follows.

Definition 26 (Higher-Order Function `md_hom`). The higher-order function `md_hom` is of type

$$\begin{aligned}
&\texttt{md_hom}^{<T^{\texttt{INP}},T^{\texttt{OUT}}\in\texttt{TYPE}\ |\ D\in\mathbb{N}\ |\ (\overset{d}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}:\texttt{MDA-IDX-SETs}\rightarrow\texttt{MDA-IDX-SETs})_{d\in[1,D]_{\mathbb{N}}},\\
&\qquad\qquad (\overset{d}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\uparrow}:\texttt{MDA-IDX-SETs}\rightarrow\texttt{MDA-IDX-SETs})_{d\in[1,D]_{\mathbb{N}}}>}:\\
&\underbrace{(\ \texttt{CO}^{<\overset{1}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}\,|\,T^{\texttt{OUT}}\,|\,D\,|\,1>}\times\ldots\times\texttt{CO}^{<\overset{D}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}\,|\,T^{\texttt{OUT}}\,|\,D\,|\,D>}\ )}_{{}^{\downarrow}\otimes_1,\ldots,{}^{\downarrow}\otimes_D}\ \times\\
&\underbrace{\texttt{SF}^{<T^{\texttt{INP}},T^{\texttt{OUT}}>}}_{f}\ \times\\
&\underbrace{(\ \texttt{CO}^{<\overset{1}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\uparrow}\,|\,T^{\texttt{OUT}}\,|\,D\,|\,1>}\times\ldots\times\texttt{CO}^{<\overset{D}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\uparrow}\,|\,T^{\texttt{OUT}}\,|\,D\,|\,D>}\ )}_{{}^{\uparrow}\otimes_1,\ldots,{}^{\uparrow}\otimes_D}\\
&\qquad\qquad\qquad\qquad\rightarrow_p\ \underbrace{\texttt{MDH}^{<T^{\texttt{INP}},T^{\texttt{OUT}}\,|\,D\,|\,(\overset{d}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow})_{d\in[1,D]_{\mathbb{N}}},(\overset{d}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\uparrow})_{d\in[1,D]_{\mathbb{N}}}>}}_{\texttt{md_hom}(\ (\otimes_1^{\downarrow},\ldots,\otimes_D^{\downarrow})\ ,\ f\ ,\ (\otimes_1^{\uparrow},\ldots,\otimes_D^{\uparrow})\ )}
\end{aligned}$$

The function takes as input a scalar function f and two tuples of D-many combine operators $({}^{\downarrow}\otimes_1,\ldots,{}^{\downarrow}\otimes_D)$ and $({}^{\uparrow}\otimes_1,\ldots,{}^{\uparrow}\otimes_D)$, and it yields a function $\texttt{md\_hom}(\ ({}^{\downarrow}\otimes_1,\ldots,{}^{\downarrow}\otimes_D)\ ,\ f\ ,\ ({}^{\uparrow}\otimes_1,\ldots,{}^{\uparrow}\otimes_D)\ )$ which is defined as:

$$\begin{aligned}
&{}^{\downarrow}a && \in T^{\texttt{INP}}[\ \overset{1}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}(I_1),\ldots,\overset{D}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}(I_D)\ ]\\
=:&\\
&\underset{i_1\in I_1}{{}^{\downarrow}\otimes_1}\ldots\underset{i_D\in I_D}{{}^{\downarrow}\otimes_D}\,{}^{\downarrow}a^{<i_1,\ldots,i_d>} && \in T^{\texttt{INP}}[\ \overset{1}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}(\{i_1\}),\ldots,\overset{D}{\Rightarrow}_{\texttt{MDA}}^{\texttt{MDA}\downarrow}(\{i_D\})\ ]\\
\mapsto&\\
&\underset{i_1\in I_1}{+\!\!+_1}\ldots\underset{i_D\in I_D}{+\!\!+_D}\,{}^{\downarrow}a_f^{<i_1,\ldots,i_d>} && \in T^{\texttt{INP}}[\ \{i_1\},\ldots,\{i_D\}\ ]\\
\overset{\vec{f}}{\mapsto}&
\end{aligned}$$

$$\underset{i_1\in I_1}{+\!\!+_1}\ \ldots\ \underset{i_D\in I_D}{+\!\!+_D}\ {}^{\uparrow}\mathfrak{a}_f^{<i_1,\ldots,i_d>} \qquad \in T^{\mathsf{OUT}}[\,\{i_1\},\ldots,\{i_D\}\,]$$

$$\mapsto$$

$$\underset{i_1\in I_1}{{}^{\uparrow}\circledast_1}\ \ldots\ \underset{i_D\in I_D}{{}^{\uparrow}\circledast_D}\ {}^{\uparrow}\mathfrak{a}^{<i_1,\ldots,i_d>} \qquad \in T^{\mathsf{OUT}}[\,\overset{1}{\Rightarrow}{}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(\,\{i_1\}\,),\ldots,\overset{D}{\Rightarrow}{}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(\,\{i_D\}\,)\,]$$

$$=:$$

$$\mathfrak{a}' \qquad \in T^{\mathsf{OUT}}[\overset{1}{\Rightarrow}{}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(\,I_1\,),\ldots,\overset{D}{\Rightarrow}{}^{\mathsf{MDA}\uparrow}_{\mathsf{MDA}}(\,I_D\,)]$$

Here, $\vec{f}$ denotes the adaption of function f to operate on MDAs comprising a single value only: it is of type

$$\vec{f}^{<i_1,\ldots,i_D\in\mathbb{N}>} : T^{\mathsf{INP}}[\,\{i_1\},\ldots,\{i_D\}\,] \to T^{\mathsf{OUT}}[\,\{i_1\},\ldots,\{i_D\}\,]$$

and defined as

$$\vec{f}(x)[\,i_1,\ldots,i_D\,] := f(x[\,i_1,\ldots,i_D\,])$$

We refer to the first application of $\mapsto$ as *de-composition*, to the application of $\overset{\vec{f}}{\mapsto}$ as *scalar function application*, and to the second application of $\mapsto$ as *re-composition*.

For $\mathtt{md\_hom}(\,(\circledast_1^{\downarrow},\ldots,\circledast_d^{\downarrow}),\,f,\,(\circledast_1^{\uparrow},\ldots,\circledast_d^{\uparrow})\,)$, we require per definition the homomorphic property (Definition 25), i.e., for each $d\in[1,D]_{\mathbb{N}}$, it must hold:

$$\mathtt{md\_hom}(\,({}^{\downarrow}\circledast_1,\ldots,{}^{\downarrow}\circledast_D)\,,\,f\,,\,({}^{\uparrow}\circledast_1,\ldots,{}^{\uparrow}\circledast_D)\,)(\,\mathfrak{a}_1\,{}^{\downarrow}\circledast_d\,\mathfrak{a}_2\,) \;=$$

$$\mathtt{md\_hom}(\,({}^{\downarrow}\circledast_1,\ldots,{}^{\downarrow}\circledast_D)\,,\,f\,,\,({}^{\uparrow}\circledast_1,\ldots,{}^{\uparrow}\circledast_D)\,)(\,\mathfrak{a}_1\,)$$

$${}^{\uparrow}\circledast_d$$

$$\mathtt{md\_hom}(\,({}^{\downarrow}\circledast_1,\ldots,{}^{\downarrow}\circledast_D)\,,\,f\,,\,({}^{\uparrow}\circledast_1,\ldots,{}^{\uparrow}\circledast_D)\,)(\,\mathfrak{a}_2\,)$$

B.3 Simple MDH Examples

Function Mapping. Function $\mathtt{map}^{<T^{\mathsf{INP}},T^{\mathsf{OUT}}\,|\,D\,|\,(I_1,\ldots,I_D)>}(f)$ maps a function $f : T^{\mathsf{INP}} \to T^{\mathsf{OUT}}$ to each element of an MDA that has scalar type $T^{\mathsf{INP}} \in \mathsf{TYPE}$, dimensionality $D\in\mathbb{N}$, and index sets $I := (I_1,\ldots,I_D) \in \mathtt{MDA\text{-}IDX\text{-}SETs}^D$.

The function is of type

$$\mathtt{map}^{<T^{\mathsf{INP}},T^{\mathsf{OUT}}\in\mathsf{TYPE}\,|\,D\in\mathbb{N}\,|\,(I_1,\ldots,I_D)\in\mathtt{MDA\text{-}IDX\text{-}SETs}^D>} :$$

$$\underbrace{T^{\mathsf{INP}}\to T^{\mathsf{OUT}}}_{f} \;\to\; \underbrace{T^{\mathsf{INP}}[\,I_1,\ldots,I_D\,]\;\to\;T^{\mathsf{OUT}}[\,I_1,\ldots,I_D\,]}_{\mathtt{map}^{<T^{\mathsf{INP}},T^{\mathsf{OUT}}\,|\,D\,|\,(I_1,\ldots,I_D)>}(f)}$$

and it is computed as:

$$\mathfrak{a} \;\overset{\mathtt{map}^{<T^{\mathsf{INP}},T^{\mathsf{OUT}}\,|\,D\,|\,(I_1,\ldots,I_D)>}(f)}{\mapsto}\; \underset{i_1\in I_1}{+\!\!+_1}\ \ldots\ \underset{i_D\in I_D}{+\!\!+_D}\ \vec{f}_{\mathtt{map}}(\,\mathfrak{a}|_{\{i_1\}\times\ldots\times\{i_D\}}\,)$$

Here, $+\!\!+_d := +\!\!+^{<T^{\mathsf{OUT}}\,|\,D\,|\,d>}$ denotes concatenation (Example 1) in dimension d, MDA $\mathfrak{a}|_{\{i_1\}\times\ldots\times\{i_D\}}$ is the restriction of $\mathfrak{a}$ to the single element accessed via indices $(i_1,\ldots,i_D)$, and $\vec{f}_{\mathtt{map}}$ denotes the adaption of function f to operate on MDAs comprising a single value only: it is of type

$$\vec{f}_{\mathtt{map}}^{<i_1,\ldots,i_D\in\mathbb{N}>} : T^{\mathsf{INP}}[\,\{i_1\},\ldots,\{i_D\}\,] \to T^{\mathsf{OUT}}[\,\{i_1\},\ldots,\{i_D\}\,]$$

and defined as

$$\vec{f}_{\mathtt{map}}(x)[\,i_1,\ldots,i_D\,] := f(x[\,i_1,\ldots,i_D\,])$$

It is easy to see that $\texttt{map}^{<T^{\texttt{INP}},T^{\texttt{OUT}}\,|\,D>}(f)$ is an MDH of type $\texttt{MDH}^{<T^{\texttt{INP}},T^{\texttt{OUT}}\,|\,D\,|\,id,\ldots,id>}$ whose combine operators are concatenation $+\!\!+_d \in \texttt{CO}^{<id\,|\,T^{\texttt{OUT}}\,|\,D\,|\,d>}$ in all dimensions $d \in [1,D]_{\mathbb{N}}$.

We have chosen map function's order of stages – $T^{\texttt{INP}}, T^{\texttt{OUT}} \in \texttt{TYPE}$ (stage 1), $D \in \mathbb{N}$ (stage 2), and $(I_1,\ldots,I_D)\texttt{MDA-IDX-SETs}^D$ (stage 3) – according to the recommendations in Haskell Wiki [2013], i.e., earlier stages (such as the scalar types $T^{\texttt{INP}}, T^{\texttt{OUT}}$) are expected to change less frequently than later stages (e.g., the MDAs' index sets $I_1,\ldots,I_D$).

Reduction. Function $\texttt{red}^{<T\,|\,D\,|\,(I_1,\ldots,I_D)>}(\oplus)$ combines all elements within an MDA that has scalar type $T \in \texttt{TYPE}$, dimensionality $D \in \mathbb{N}$, and index sets $I := (I_1,\ldots,I_D) \in \texttt{MDA-IDX-SETs}^D$, using an associative and commutative binary function $\oplus : T \times T \to T$.

The function is of type

$$\texttt{red}^{<T\in\texttt{TYPE}\,|\,D\in\mathbb{N}\,|\,(I_1,\ldots,I_D)\in\texttt{MDA-IDX-SETs}^D>} : \underbrace{T\times T\to T}_{\oplus} \to \underbrace{T[\,I_1,\ldots,I_D\,]\to T[\,1,\ldots,1\,]}_{\texttt{red}^{<T\,|\,D\,|\,(I_1,\ldots,I_D)>}(\oplus)}$$

and it is computed as:

$$\mathfrak{a} \overset{\texttt{red}^{<T\,|\,D\,|\,(I_1,\ldots,I_D)>}(\oplus)}{\mapsto} \underset{i_1\in I_1}{\overrightarrow{\bullet_1}}(\oplus) \;\ldots\; \underset{i_D\in I_D}{\overrightarrow{\bullet_D}}(\oplus)\; \vec{f}_{\texttt{red}}(\,\mathfrak{a}|_{\{i_1\}\times\ldots\times\{i_D\}}\,)$$

Here, $\overrightarrow{\bullet_d}(\oplus) := \overrightarrow{\bullet}^{<T\,|\,D\,|\,d>}(\oplus)$ denotes point-wise combination (Example 2) in dimension d, MDA $\mathfrak{a}|_{\{i_1\}\times\ldots\times\{i_D\}}$ is defined as above, and $\vec{f}_{\texttt{red}}$ is the function of type

$$\vec{f}_{\texttt{red}}^{<i_1,\ldots,i_D\in\mathbb{N}>} : T^{\texttt{INP}}[\,\{i_1\},\ldots,\{i_D\}\,] \to T^{\texttt{OUT}}[\,\{0\},\ldots,\{0\}\,]$$

that is defined as

$$\vec{f}_{\texttt{red}}(x)[\,0,\ldots,0\,] := x[\,i_1,\ldots,i_D\,]$$

It is easy to see that $\texttt{red}^{<T\,|\,D>}(\oplus)$ is an MDH of type $\texttt{MDH}^{<T,T\,|\,D\,|\,0_f,\ldots,0_f>}$ whose combine operators are point-wise addition $\overrightarrow{\bullet_d}(\oplus) \in \texttt{CO}^{<id\,|\,T\,|\,D\,|\,d>}$ in all dimensions $d \in [1,D]_{\mathbb{N}}$. The same as for function map, function red's order of meta-parameter stages are chosen according to [Haskell Wiki 2013].

B.4 Design Decisions: md_hom

We list some design decisions for higher-order function md_hom (Definition 4).

Note 2. For some MDHs (such as Mandelbrot), the scalar function f (Definition 4) is dependent on the position in the input MDA, i.e., it takes as arguments, in addition to $\mathfrak{a}[i_1,\ldots,i_D]$, also the indices $i_1,\ldots,i_D$. Such MDHs can be easily expressed via md_hom after a straightforward type adjustment: type $\text{SF}^{<T^{\texttt{INP}},T^{\texttt{OUT}}>}$ has to be defined as the set of functions $f : T^{\texttt{INP}} \times \texttt{MDA-IDX-SETs}^D \to T^{\texttt{OUT}}$ (rather than of functions $f : T^{\texttt{INP}} \to T^{\texttt{OUT}}$, as in Definition 4).

Since we do not aim at forcing scalar functions to always take MDA indices as input arguments – for expressing most computations, this is not required (Figure 16) and only causes additional complexity – we assume in the following two different definitions of pattern md_hom: one variant exactly as in Definition 4, and one variant with the adjusted type for scalar functions and that passes automatically indices $i_1,\ldots,i_D$ to f. The two variants can be easily differentiated, via an additional, boolean meta-parameter USE_MDA_INDICES: first variant iff USE_MDA_INDICES = false and second variant iff USE_MDA_INDICES = true.

For simplicity, we focus in this paper on the first variant (as in Definition 4), because, in practice, it is the more common variant, and because all insights presented in this work apply to both variants.

B.5 Proof md_hom Lemma

We prove Lemma 1.

Proof. Let $\mathfrak{a}_1 \in T[I_1^{\mathfrak{a}_1}, \ldots, I_D^{\mathfrak{a}_1}]$ and $\mathfrak{a}_2 \in T[I_1^{\mathfrak{a}_2}, \ldots, I_D^{\mathfrak{a}_2}]$ be two arbitrary MDAs for which $I_d^{\mathfrak{a}_1} \cap I_d^{\mathfrak{a}_2} = \varnothing$, for $d \in [1, D]_{\mathbb{N}}$ arbitrary but fixed, i.e., the two MDAs are concatenable in dimension d.

According to Definition 4, we have to show that

$$\texttt{md\_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, \mathfrak{a}_1 +\!\!+_d \mathfrak{a}_2 \,) = \texttt{md\_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, \mathfrak{a}_1 \,) \;\circledast_d\; \texttt{md\_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, \mathfrak{a}_2 \,)$$

For this, we first show for arbitrary $k \in [1, D)_{\mathbb{N}}$ that

$$\ldots \underset{i_k \in I_k}{\circledast_k} \underset{i_{k+1} \in I_{k+1}}{\circledast_{k+1}} \ldots \; x|_{\ldots,\{i_k\},\{i_{k+1}\},\ldots} = \ldots \underset{i_{k+1} \in I_{k+1}}{\circledast_{k+1}} \underset{i_k \in I_k}{\circledast_k} \ldots \; x|_{\ldots,\{i_k\},\{i_{k+1}\},\ldots}$$

from which follows

$$\underset{i_1 \in I_1}{\circledast_1} \ldots \underset{i_D \in I_D}{\circledast_D} x|_{\{i_1\},\ldots,\{i_D\}} = \underset{i_\sigma(1) \in I_\sigma(1)}{\circledast_\sigma(1)} \ldots \underset{i_\sigma(D) \in I_\sigma(D)}{\circledast_\sigma(D)} x|_{\{i_1\},\ldots,\{i_D\}}$$

for any permutation $\sigma : \{1, \ldots, D\} \twoheadrightarrow \{1, \ldots, D\}$. Afterwards, in our assumption above, we can assume w.l.o.g. that $d = 1$.

Case 1: $[\circledast_k = \circledast_{k+1}]$ Follows immediately from the commutativity of $+\!\!+$ or $\overrightarrow{\bullet}(\oplus)$ for commutative $\oplus$, respectively. ✓

Case 2: $[\circledast_k \neq \circledast_{k+1}]$ Trivial, as it is either $\circledast_k = +\!\!+$ or $\circledast_{k+1} = +\!\!+$, and

$$(\underset{i_d \in I_d}{+\!\!+} x|_{\ldots,\{i_d\},\ldots})[i_1, \ldots, i_D] = (x|_{\ldots,\{i_d\},\ldots})[i_1, \ldots, i_D]$$

according to the definition of MDA concatenation $+\!\!+$ (Example 1). ✓

Let now be $d = 1$ (see assumption above), it holds:

$$\begin{aligned}
&\texttt{md_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, \mathfrak{a}_1 +\!\!+_1 \mathfrak{a}_2 \,) \\
&= \underset{i_1 \in I_1}{\circledast_1} \ldots \underset{i_D \in I_D}{\circledast_D} \vec{f}(\, (\mathfrak{a}_1 +\!\!+_1 \mathfrak{a}_2)|_{\{i_1\}\times\ldots\times\{i_D\}} \,) \\
&= \underset{i_1 \in I_1^{\mathfrak{a}_1}}{\circledast_1} \ldots \underset{i_D \in I_D}{\circledast_D} \vec{f}(\, \mathfrak{a}_1|_{\{i_1\}\times\ldots\times\{i_D\}} \,) \;\circledast_1\; \underset{i_1 \in I_1^{\mathfrak{a}_2}}{\circledast_1} \ldots \underset{i_D \in I_D}{\circledast_D} \vec{f}(\, \mathfrak{a}_2|_{\{i_1\}\times\ldots\times\{i_D\}} \,) \\
&= \texttt{md_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, \mathfrak{a}_1 \,) \;\circledast_1\; \texttt{md_hom}(\, f \,,\, (\circledast_1, \ldots, \circledast_D)\,)(\, \mathfrak{a}_2 \,) \quad ✓
\end{aligned}$$

□

B.6 Examples of Index Functions

We present examples of index functions (Definition 6).

Example 13 (Matrix-Vector Multiplication)**.** The index functions we use for expressing Matrix-Vector Multiplication (MatVec) are:

- Input Matrix:

$$\mathfrak{idx}(i,k) := (i,k) \in \texttt{MDA-IDX-to-BUF-IDX}^{<D=2,D_1=2\,|\,\Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}>}$$
$$\text{for } \Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}(I_1^{\texttt{MDA}}, I_2^{\texttt{MDA}}) := [0, \max(I_1^{\texttt{MDA}})]_{\mathbb{N}_0}, [0, \max(I_2^{\texttt{MDA}})]_{\mathbb{N}_0}$$

- Input Vector:

$$\mathfrak{idx}(i,k) := (k) \in \texttt{MDA-IDX-to-BUF-IDX}^{<D=2,D_1=1\,|\,\Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}>}$$
$$\text{for } \Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}(I_1^{\texttt{MDA}}, I_2^{\texttt{MDA}}) := [0, \max(I_2^{\texttt{MDA}})]_{\mathbb{N}_0}$$

- Output Vector:

$$\mathfrak{idx}(i,k) := (i) \in \texttt{MDA-IDX-to-BUF-IDX}^{<D=2,D_1=1\,|\,\Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}>}$$
$$\text{for } \Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}(I_1^{\texttt{MDA}}, I_2^{\texttt{MDA}}) := [0, \max(I_1^{\texttt{MDA}})]_{\mathbb{N}_0}$$

Example 14 (Jacobi 1D). The index functions we use for expressing Jacobi 1D (`Jacobi1D`) are:

- Input Buffer, 1. Access:

$$\mathfrak{idx}(i) := (i+0) \in \texttt{MDA-IDX-to-BUF-IDX}^{<D=1,D_1=1\,|\,\Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}>}$$
$$\text{for } \Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}(I_1^{\texttt{MDA}}) := [0, \max(I_1^{\texttt{MDA}}) + 0]_{\mathbb{N}_0}$$

- Input Buffer, 2. Access:

$$\mathfrak{idx}(i) := (i+1) \in \texttt{MDA-IDX-to-BUF-IDX}^{<D=1,D_1=1\,|\,\Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}>}$$
$$\text{for } \Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}(I_1^{\texttt{MDA}}) := [0, \max(I_1^{\texttt{MDA}}) + 1]_{\mathbb{N}_0}$$

- Input Buffer, 3. Access:

$$\mathfrak{idx}(i) := (i+2) \in \texttt{MDA-IDX-to-BUF-IDX}^{<D=1,D_1=1\,|\,\Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}>}$$
$$\text{for } \Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}(I_1^{\texttt{MDA}}) := [0, \max(I_1^{\texttt{MDA}}) + 2]_{\mathbb{N}_0}$$

- Output Buffer:

$$\mathfrak{idx}(i) := (i) \in \texttt{MDA-IDX-to-BUF-IDX}^{<D=1,D_1=1\,|\,\Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}>}$$
$$\text{for } \Rightarrow^{\texttt{MDA}}_{\texttt{BUF}}(I_1^{\texttt{MDA}}) := [0, \max(I_1^{\texttt{MDA}})]_{\mathbb{N}_0}$$

B.7 Representation of Scalar Values

Scalar values can be considered as 0-dimensional BUFs (Definition 5). Consequently, in Definition 5, the cartesian product $[0, N_1)_{\mathbb{N}_0} \times \ldots \times [0, N_D)_{\mathbb{N}_0}$ is empty for $D = 0$, and thus results in the neutral element of the cartesian product. As any singleton set can be considered as neutral element of cartesian product (up to bijection), we define the set $\{\epsilon\}$ containing the dedicated symbol epsilon only, as the uniquely determined neutral element of cartesian product (inspired by the notation of the *empty word*).

We often refrain from explicitly stating symbol ϵ, e.g., by writing $\mathfrak{b}$ instead of $\mathfrak{b}[\epsilon]$ for accessing a BUF, or $(i_1, \ldots, i_D) \to ()$ instead of $(i_1, \ldots, i_D) \to (\epsilon)$ for index functions.

Note that alternatively, scalar values can be considered as any multi-dimensional BUF containing a single element only. For example, a scalar value s can be represented as 1-dimensional BUF

$\mathtt{b}_{1D}[0] := s$, or a 2-dimensional BUF $\mathtt{b}_{2D}[0,0] := s$, or a 3-dimensional BUF $\mathtt{b}_{3D}[0,0,0] := s$, etc. However, this results in an ambiguous representation of scalar values, which we aim to avoid by considering scalars as 0-dimensional BUFs, as described above.

B.8 Runtime Complexity of Histograms

Our implementation of Histograms (Subfigure 5 in Figure 16) has a *work complexity* of $\mathcal{O}(E * B)$, where E is the number of elements to check and B the number of bins, i.e., our MDH Histogram implementation is not work efficient. However, our Histograms' *step complexity* [Harris et al. 2007] is $\mathcal{O}(log(E))$: step complexity is often used for parallel algorithms and assumes an infinite number of cores, i.e., we can ignore in our implementation of Histogram the concatenation dimension B (which has a step complexity of $\mathcal{O}(1)$) and take into account its reduction dimension B only, which has a step complexity of $log(B)$ (parallel reduction [Harris et al. 2007]). In contrast, related approaches [Henriksen et al. 2020] are often work efficient, by having a work complexity of $\mathcal{O}(B)$; however, their high work efficiency is at the cost of their step complexity which is also $\mathcal{O}(B)$, rather than $\mathcal{O}(log(B))$ as for our implementation in Subfigure 5, thereby being asymptotically less efficient for parallel machines consisting of many cores. Our future work will show that the work-efficient Histogram implementation introduced in Henriksen et al. [2020] can also be expressed in our approach, by using for scalar function f an optimized micro kernel for Histogram computation, similarly as done in the related work.

B.9 Combine Operator of Prefix-Sum Computations

We define *prefix-sum* which is the combine operator of compute pattern `scan` and example `MBBS` in Section 2.5.

Example 15 (Prefix-Sum)**.** We define *prefix-sum*, according to a binary function $\oplus : T \times T \to T$ (e.g. addition), as function $\circledast_{\texttt{prefix-sum}}$ of type

$$\circledast_{\texttt{prefix-sum}}^{<T \in \texttt{TYPE} \mid D \in \mathbb{N} \mid d \in [1,D]_{\mathbb{N}} \mid (I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D) \in \texttt{MDA-IDX-SETs}^{D-1}, (P,Q) \in \texttt{MDA-IDX-SETs} \dot{\times} \texttt{MDA-IDX-SETs}>} :$$

$$\underbrace{T \times T \to T}_{\oplus} \to \underbrace{T[I_1,\ldots,\underbrace{id(P)}_{\uparrow d},\ldots,I_D] \times T[I_1,\ldots,\underbrace{id(Q)}_{\uparrow d},\ldots,I_D] \to T[I_1,\ldots,\underbrace{id(P \uplus Q)}_{\uparrow d},\ldots,I_D]}_{\texttt{prefix-sum (according to } \oplus)}$$

where id : `MDA-IDX-SETs` $\to$ `MDA-IDX-SETs` is the identity function on MDA index sets. The function is computed as (w.l.o.g., we assume $max(P) < max(Q)$ for commutativity):

$$\circledast_{\texttt{prefix-sum}}^{<T \mid D \mid d \mid (I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D),(P,Q)>} (\oplus)(\mathfrak{a}_1,\mathfrak{a}_2)[i_1,\ldots,i_d,\ldots,i_D]$$

$$:= \begin{cases} \mathfrak{a}_1[i_1,\ldots,i_d,\ldots,i_D] & , \; i_d \in P \\ \mathfrak{a}_1[i_1,\ldots,max(P),\ldots,i_D] \oplus \mathfrak{a}_2[i_1,\ldots,i_d,\ldots,i_D] & , \; i_d \in Q \end{cases}$$

Function $\circledast_{\texttt{prefix-sum}}^{<T \mid D \mid d>}(\oplus)$ (meaning: $\circledast_{\texttt{prefix-sum}}$ is partially applied to ordinary function parameter $\oplus$; formal details provided in the Appendix, Definition 22) is a combine operator of type $\texttt{CO}^{<id \mid T \mid D \mid d>}$ for any binary operator $\oplus : T \times T \to T$.

No.	Constraint	
0	$\prod_{d \in [1,D]_{\mathbb{N}}} \#\mathrm{PRT}(\overleftarrow{\mathrm{CC}}^{\bullet\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\bullet\text{-MDH}}) \leq 1024$	(Number of CCs limited)
R3	$\#\mathrm{PRT}(\overleftarrow{\mathrm{BLK}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) > 1 \wedge \circledast_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \neq +\!\!+_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \Rightarrow \uparrow\text{-mem}^{\langle ob \rangle}(\overleftarrow{\mathrm{BLK}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) \in \{\mathrm{DM}\}$	(SMXs combine in DM)
	$\#\mathrm{PRT}(\overleftarrow{\mathrm{CC}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) > 1 \wedge \circledast_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \neq +\!\!+_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \Rightarrow \uparrow\text{-mem}^{\langle ob \rangle}(\overleftarrow{\mathrm{CC}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) \in \{\mathrm{DM}, \mathrm{SM}\}$	(CCs combine in DM/SM)

Table 2. CUDA model constraints on tuning parameters

No.	Constraint	
0	$\prod_{d \in [1,D]_{\mathbb{N}}} \#\mathrm{PRT}(\overleftarrow{\mathrm{CC}}^{\bullet\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\bullet\text{-MDH}}) \leq 1024$	(Number of CCs limited)
R3	$\#\mathrm{PRT}(\overleftarrow{\mathrm{BLK}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) > 1 \wedge \circledast_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \neq +\!\!+_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \Rightarrow \uparrow\text{-mem}^{\langle ob \rangle}(\overleftarrow{\mathrm{BLK}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) \in \{\mathrm{DM}\}$	(SMXs combine in DM)
	$\#\mathrm{PRT}(\overleftarrow{\mathrm{WRP}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) > 1 \wedge \circledast_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \neq +\!\!+_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \Rightarrow \uparrow\text{-mem}^{\langle ob \rangle}(\overleftarrow{\mathrm{WRP}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) \in \{\mathrm{DM}, \mathrm{SM}\}$	(WRPs combine in DM/SM)

Table 3. CUDA+WRP model constraints on tuning parameters

No.	Constraint	
0	$\prod_{d \in [1,D]_{\mathbb{N}}} \#\mathrm{PRT}(\overleftarrow{\mathrm{WI}}^{\bullet\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\bullet\text{-MDH}}) \leq C_{\mathrm{DEV}}$	(Number of PEs limited)
R3	$\#\mathrm{PRT}(\overleftarrow{\mathrm{WG}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) > 1 \wedge \circledast_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \neq +\!\!+_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \Rightarrow \uparrow\text{-mem}^{\langle ob \rangle}(\overleftarrow{\mathrm{WG}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) \in \{\mathrm{GM}\}$	(CUs combine in GM)
	$\#\mathrm{PRT}(\overleftarrow{\mathrm{WI}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) > 1 \wedge \circledast_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \neq +\!\!+_{\overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}} \Rightarrow \uparrow\text{-mem}^{\langle ob \rangle}(\overleftarrow{\mathrm{WI}}^{\uparrow\text{-MDH}}, \overleftarrow{\mathrm{d}}^{\uparrow\text{-MDH}}) \in \{\mathrm{GM}, \mathrm{LM}\}$	(PEs combine in GM/LM)

Table 4. OpenCL model constraints on tuning parameters

C ADDENDUM SECTION 3

C.1 Constraints of Programming Models

Constraints of programming models can be expressed in our formalism; we demonstrate this using the example models CUDA and OpenCL. For this, we add to the general, model-unspecific constraints (described in Section 3.4) the new, model-specific constraints listed in Tables 2 or 3 for CUDA or the constraints in Table 4 for OpenCL, respectively. For brevity, we use in the following:

$$(l_{\mathsf{MDH}}, d_{\mathsf{MDH}}) := \leftrightarrow^{-1}_{\bullet\text{-}\mathsf{ass}} (l_{\mathsf{ASM}}, d_{\mathsf{ASM}}), \quad \bullet \in \{\downarrow, f, \uparrow\}$$

In Tables 2 and 3 for CUDA, the constraint No. 1 (which constrains tuning parameter No. 1 in Table 1) limits the number of cuda cores (CC) to 1024, according to the CUDA specification [NVIDIA 2022g]. The constraints on tuning parameter 14 specify that the results of SMX can be combined in device memory (DM) only, and that of CCs/WRPs in only device memory (DM) or shared memory (SM). Note that in the case of Table 3, CCs are not constrained in parameter 14, as CCs within a WRP have access to all CUDA memory regions: DM, SM, as well as RM (via warp shuffles [NVIDIA 2018]).

In Table 4 for OpenCL, the constraints are similar to the CUDA's constraints in Tables 2: they limit the number of PEs to C_{DEV} (which is a device-specific constant in OpenCL), and they specify the valid memory regions for combining the results of cores, according to the OpenCL specification [Khronos 2022b].

Note that the tables present some important example constraints only and are not complete: for example, CUDA and OpenCL devices are also constrained regarding their memory sizes (shared/private memory), which is not considered in the tables.

C.2 Inverse Concatenation

Definition 27 (Inverse Concatenation)**.** The inverse of operator *concatenation* (Example 1) is function $+\!\!+^{-1}$ which is of type

$$+\!\!+^{-1<T\in\mathsf{TYPE}\,|\,D\in\mathbb{N}\,|\,d\in[1,D]_{\mathbb{N}}\,|\,(I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D)\in\mathsf{MDA\text{-}IDX\text{-}SETs}^{D-1},(P,Q)\in\mathsf{MDA\text{-}IDX\text{-}SETs}\,\dot{\times}\,\mathsf{MDA\text{-}IDX\text{-}SETs}>}:$$

$$T[I_1,\ldots,\underbrace{id(P\uplus Q)}_{\uparrow d},\ldots,I_D] \to T[I_1,\ldots,\underbrace{id(P)}_{\uparrow d},\ldots,I_D] \times T[I_1,\ldots,\underbrace{id(Q)}_{\uparrow d},\ldots,I_D]$$

where id : MDA-IDX-SETs → MDA-IDX-SETs is the identity function on MDA index sets. The function is computed as:

$$+\!\!+^{-1<T\,|\,D\,|\,d\,|\,(I_1,\ldots,I_{d-1},I_{d+1},\ldots,I_D),(P,Q)>}(\mathfrak{a}) := (\mathfrak{a}_1, \mathfrak{a}_2)$$

for

$$\mathfrak{a}_1[i_1,\ldots,\ i_d\ ,\ldots,i_D] := \mathfrak{a}[i_1,\ldots,\ i_d\ ,\ldots,i_D],\ \ i_d \in P$$

and

$$\mathfrak{a}_2[i_1,\ldots,\ i_d\ ,\ldots,i_D] := \mathfrak{a}[i_1,\ldots,\ i_d\ ,\ldots,i_D],\ \ i_d \in Q$$

i.e., $\mathfrak{a}_1$ and $\mathfrak{a}_2$ behave exactly as MDA $\mathfrak{a}$ on their restricted index sets P or Q, respectively.

We often write for $(\mathfrak{a}_1, \mathfrak{a}_2) := +\!\!+^{-1<\ldots>}(\mathfrak{a})$ (meta-parameters omitted via ellipsis) also $\mathfrak{a} =: \mathfrak{a}_1 +\!\!+^{<\ldots>} \mathfrak{a}_2$. Our notation is justified by the fact that the inverse of MDA $\mathfrak{a}$ is uniquely determined as the two MDAs $\mathfrak{a}_1$ and $\mathfrak{a}_2$ which are equal to $\mathfrak{a}$ when concatenating them (follows immediately from the definition of inverse functions).

C.3 Example 17 in Verbose Math Notation

Figures 36-38 show our low-level representation from Example 17 in verbose math notation. The symbols $\blacksquare_\perp, \ldots, \blacksquare_f$ used in the figures are a textual abbreviation for:

$$\begin{array}{lll|l|l|l}
\blacksquare_\perp & := & *,* & *,* & *,* \\
\blacksquare_1^1 & := & *,* & *,* & *,* \\
\blacksquare_2^1 & := & p_1^1,* & *,* & *,* \\
\blacksquare_1^2 & := & p_1^1,p_2^1 & *,* & *,* \\
\blacksquare_2^2 & := & p_1^1,p_2^1 & p_1^2,* & *,* \\
\blacksquare_1^3 & := & p_1^1,p_2^1 & p_1^2,p_2^2 & *,* \\
\blacksquare_2^3 & := & p_1^1,p_2^1 & p_1^2,p_2^2 & p_1^3,* \\
\blacksquare_f & := & p_1^1,p_2^1 & p_1^2,p_2^2 & p_1^3,p_2^3
\end{array}$$

where symbol $*$ indicates generalization in meta-parameters (Definition 23).

In Example 17, the arrow annotation of combine operators is formally an abbreviation. For example, operator $+\!\!+_2^{(\texttt{COR},\texttt{y})}$ in Figure 17 is annotated with → `M: HM[1,2],v: HM[1]` which abbreviates

$$\ldots \quad {}^{\downarrow}\mathrm{a}_2^{2<p_1^1,p_2^1 \mid p_1^2,p_2^2:=* \mid p_1^3:=*,p_2^3:=*>} \quad =: \quad \underset{p_2^2 \in [0,16)_{\mathbb{N}_0}}{+\!\!+_2^{(\texttt{COR},\texttt{y})}} \quad \ldots$$

Here, ${}^{\downarrow}\mathrm{a}_2^2$ represents the low-level MDA (Definition 12) that is already partitioned for layer 1 in dimensions 1 and 2, and for layer 2 in dimension 1 (because in Figure 17, operators $+\!\!+_1^{(\texttt{HM},\texttt{x})}$, $+\!\!+_2^{(\texttt{HM},\texttt{y})}$, $+\!\!+_1^{(\texttt{COR},\texttt{x})}$ appear before operator $+\!\!+_2^{(\texttt{COR},\texttt{y})}$), but not yet for layer 2 in dimension 2 as well as for layer 3 in both dimensions (indicated by symbol $*$ which is described formally in Definition 23 of our Appendix). In our generated code (discussed in Section E of our Appendix), we store low-level MDAs, like ${}^{\downarrow}\mathrm{a}_2^2$, using their domain-specific data representation, as the domain-specific representation is usually more efficient: in the case of `MatVec`, we physically store matrix M and vector v for the input MDA, and vector w for the output MDA. For example, low-level MDA

$${}^{\downarrow}\mathrm{a}_2^{2<p_1^1,p_2^1 \mid p_1^2,p_2^2:=* \mid p_1^3:=*,p_2^3:=*>}$$

can be transformed via view functions (Definitions 8 and 10) to *low-level BUFs* (Definition 13)

$$M_2^{2<\texttt{HM} \mid id><p_1^1,p_2^1 \mid p_1^2,p_2^2:=* \mid p_1^3:=*,p_2^3:=*>}$$

and

$$v_2^{2<\texttt{HM} \mid id><p_1^1,p_2^1 \mid p_1^2,p_2^2:=* \mid p_1^3:=*,p_2^3:=*>}$$

and back (Lemma 2). Similarly as for data structures in low-level programming models (e.g., *C arrays* as in OpenMP, CUDA, and OpenCL), low-level BUFs are defined to have an explicit notion of memory regions and memory layouts.

In Figure 36, we de-compose the input MDA ${}^{\downarrow}\mathfrak{a}$, step by step, for the MDH levels $(1,1), \ldots, (3,2)$:

$${}^{\downarrow}\mathfrak{a} =: {}^{\downarrow}\mathfrak{a}_\perp^{<\blacksquare_\perp>} \rightarrow {}^{\downarrow}\mathfrak{a}_1^{1<\blacksquare_1^1>} \rightarrow {}^{\downarrow}\mathfrak{a}_2^{1<\blacksquare_2^1>} \rightarrow {}^{\downarrow}\mathfrak{a}_1^{2<\blacksquare_1^2>} \rightarrow {}^{\downarrow}\mathfrak{a}_2^{2<\blacksquare_2^2>} \rightarrow {}^{\downarrow}\mathfrak{a}_1^{3<\blacksquare_1^3>} \rightarrow {}^{\downarrow}\mathfrak{a}_2^{3<\blacksquare_2^3>} \rightarrow {}^{\downarrow}\mathfrak{a}_f^{<\blacksquare_f>}$$

The input MDAs $({}^{\downarrow}\mathfrak{a}_d^l)_{l \in [1,3]_{\mathbb{N}}, d \in [1,2]_{\mathbb{N}}}$ and ${}^{\downarrow}\mathfrak{a}_f$ are all low-level MDA representations (Definition 12). We use as partitioning schema P (Definition 12)

$$P := \big((P_1^1, P_2^1),\ (P_1^2, P_2^2),\ (P_1^3, P_2^3) \big) = \big((2,4),\ (8,16),\ (32,64) \big)$$

and we use the index sets I_d from Definition 28 (which define a uniform index set partitioning) as follows:

$$\left(\underset{+\!\!+_d}{\overset{d}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}(I_d^{<p_1^1,p_2^1 \mid p_1^2,p_2^2 \mid p_1^3,p_2^3>})^{<(p_1^1,p_2^1)\in P_1^1\times P_2^1 \mid (p_1^2,p_2^2)\in P_1^2\times P_2^2 \mid (p_1^3,p_2^3)\in P_1^3\times P_2^3>} \right)_{d\in[1,D]_{\mathbb{N}}}$$

Here, $\underset{+\!\!+_d}{\overset{d}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}$ denotes the index set function of combine operator concatenation (Example 1), which is the identity function and explicitly stated for the sake of completeness only. Note that in Figure 36, we access low-level MDAs ${}^{\downarrow}\mathfrak{a}_d^l$ as generalized in some partition sizes, via $*$ (Definition 23), according to the definitions of the $\blacksquare_d^l$.

Each MDA ${}^{\downarrow}\mathfrak{a}$ can be transformed to its domain-specific data representation matrix ${}^{\downarrow}M$ and vector ${}^{\downarrow}v$ and vice versa, using the view functions, as discussed above.

Figure 37 shows our scalar phase, which is formally trivial.

In Figure 38, we re-compose the computed data ${}^{\uparrow}\mathfrak{a}_f{}^{<\blacksquare_f>}$, step by step, to the final result ${}^{\uparrow}\mathfrak{a}$:

$${}^{\uparrow}\mathfrak{a}_f{}^{<\blacksquare_f>} \rightarrow {}^{\uparrow}\mathfrak{a}_1^1{}^{<\blacksquare_1^1>} \rightarrow {}^{\uparrow}\mathfrak{a}_2^1{}^{<\blacksquare_2^1>} \rightarrow {}^{\uparrow}\mathfrak{a}_2^2{}^{<\blacksquare_2^2>} \rightarrow {}^{\uparrow}\mathfrak{a}_1^3{}^{<\blacksquare_1^3>} \rightarrow {}^{\uparrow}\mathfrak{a}_2^3{}^{<\blacksquare_2^3>} \rightarrow {}^{\uparrow}\mathfrak{a}_\perp{}^{<\blacksquare_\perp>} =: {}^{\uparrow}\mathfrak{a}$$

Analogously to the de-composition phase, each output MDA $({}^{\uparrow}\mathfrak{a}_d^l)_{l\in[1,3]_{\mathbb{N}},d\in[1,2]_{\mathbb{N}}}$ and ${}^{\uparrow}\mathfrak{a}_f$ is a low-level MDA representation, for P as defined above and index sets

$$\left(\underset{\circledast_d}{\overset{d}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}(I_d^{<p_1^1,p_2^1 \mid p_1^2,p_2^2 \mid p_1^3,p_2^3>})^{<(p_1^1,p_2^1)\in P_1^1\times P_2^1 \mid (p_1^2,p_2^2)\in P_1^2\times P_2^2 \mid (p_1^3,p_2^3)\in P_1^3\times P_2^3>} \right)_{d\in[1,D]_{\mathbb{N}}}$$

where $\underset{\circledast_d}{\overset{d}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}$ are the index set functions of the combine operators (Definition 2) used in the re-composition phase. The same as in the de-composition phase, we access the output low-level MDAs as generalized in some partition sizes, according to our definitions of the $\blacksquare_d^l$, and we identify each MDA with its domain-specific data representation (the output vector w).

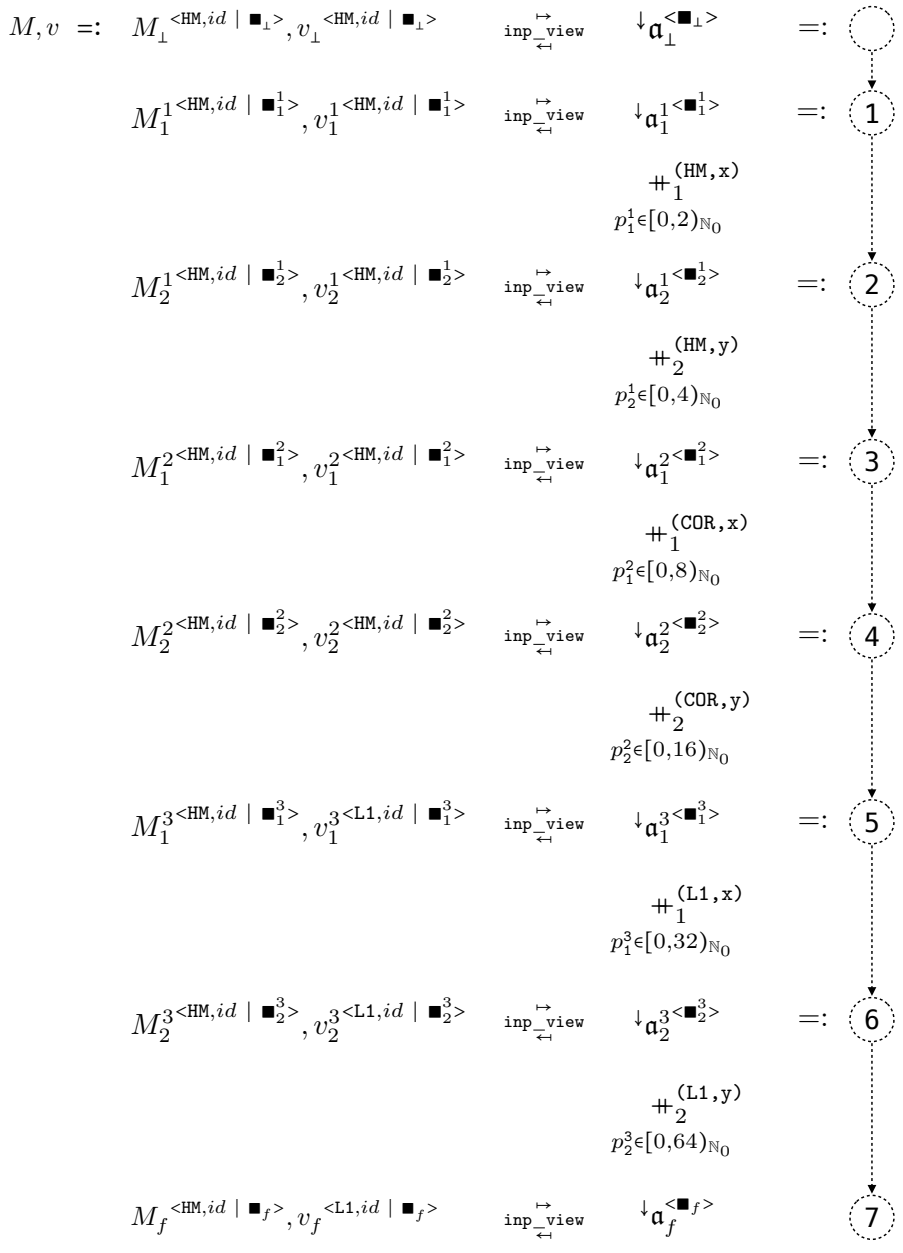
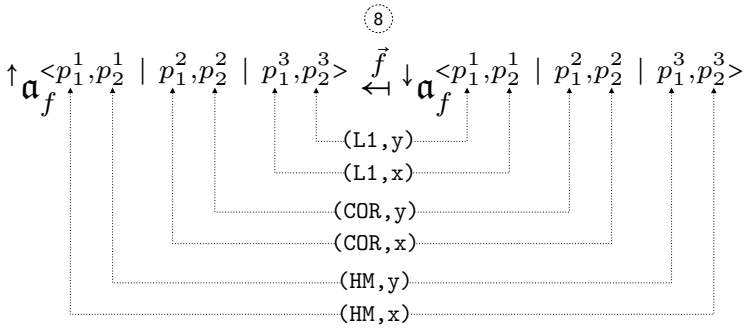


Fig. 36. De-composition phase of Example 17 in verbose math notation.



$$\text{for all:}\quad p_1^1 \in P_1^1\ ,\ p_2^1 \in P_2^1\ ,\\ p_1^2 \in P_1^2\ ,\ p_2^2 \in P_2^2\ ,\\ p_1^3 \in P_1^3\ ,\ p_2^3 \in P_2^3$$

Fig. 37. Scalar phase of Example 17 in verbose math notation.

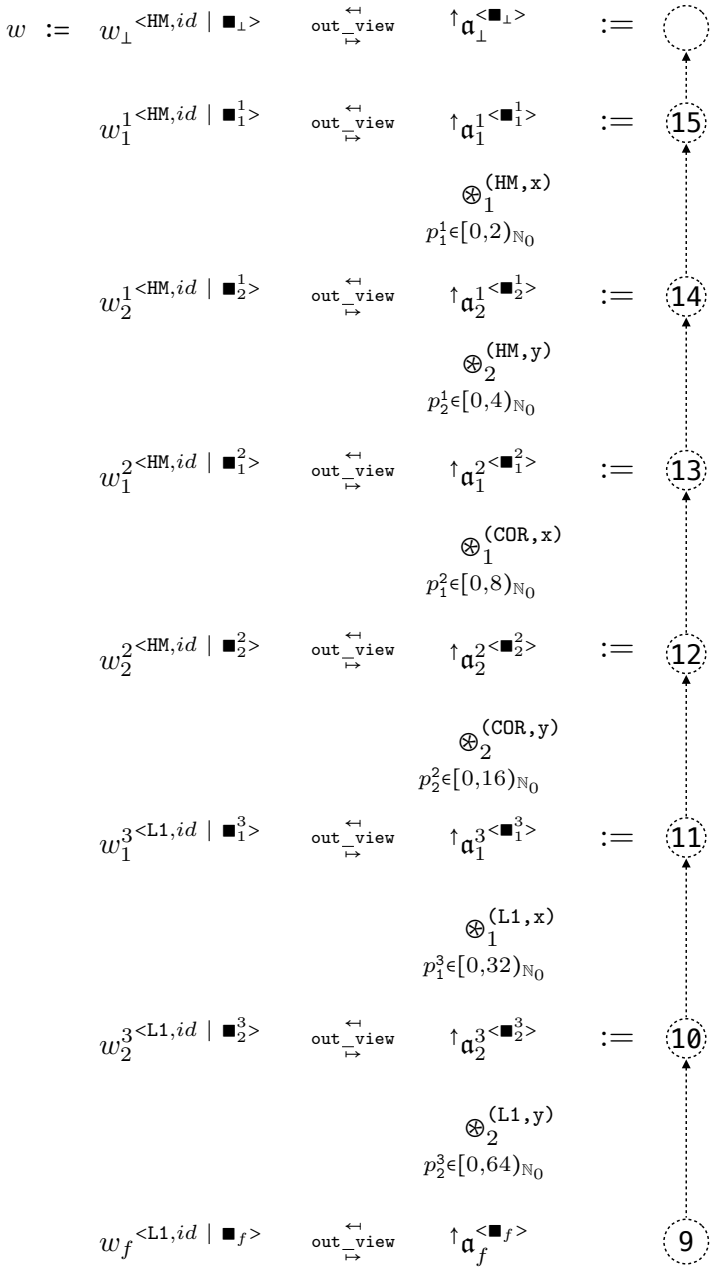


Fig. 38. Re-composition phase of Example 17 in verbose math notation.

C.4 Multi-Dimensional ASM Arrangements

We demonstrate how we arrange memory regions and cores of ASM-represented systems (Section 3.2) in multiple dimensions using the example of CUDA.

Cores (COR):. In CUDA, SMX cores are programmed via so-called *CUDA Blocks*, and CUDA's CC cores are programmed via *CUDA Threads*. CUDA has native support for arranging its blocks and threads in up to three dimensions which are called x, y, and z in CUDA [NVIDIA 2022f]. Consequently, even though the original CUDA specification [NVIDIA 2022g] introduces SMX and CC without having an order, the CUDA programmer benefits from imagining SMX and CC as three-dimensionally arranged.

Additional dimensions can be explicitly programmed in CUDA. For example, to add a fourth dimension to CUDA, we can embed the additional dimension in the CUDA's z dimension, thereby splitting CUDA dimension z in the explicitly programmed dimensions z_1 (third dimension) and z_2 (fourth dimension), as follows:

```
z_1 := z % Z_1 and z_2 := z / Z_1
```

Here, Z_1 represents the number of threads in the additional dimension, and symbol % the modulo operator.

Memory (MEM):. In CUDA, memory is managed via *C arrays* which may be multi-dimensional: to arrange (DIM_1 × ... × DIM_D)-many memory regions, each of size N, we use a CUDA array of the following type (pseudocode):

```
array[ DIM_1 ]...[ DIM_D ][ N ]
```

Note that CUDA implicitly arranges its *shared* and *private* memory allocations in multiple dimensions, depending on the number of blocks and threads: a shared memory array of type `shared_array[ DIM_1 ]...[ DIM_D ][ N ]` is internally managed in CUDA as `shared_array[ blockIdx.x ][ blockIdx.y ][ blockIdx.z ][ DIM_1 ]...[ DIM_D ][ N ]`, i.e., each CUDA block has its own shared memory region. Analogously, a private memory array `private_array[ DIM_1 ]...[ DIM_D ][ N ]` is managed in CUDA as `private_array[ blockIdx.x ][ blockIdx.y ][ blockIdx.z ][ threadIdx.x ][ threadIdx.y ][ threadIdx.z ][ DIM_1 ]...[ DIM_D ][ N ]`, correspondingly. Our arrangement methodology continues the CUDA's approach by explicitly programming the additional arrangement dimensions DIM_1, ..., DIM_D.

Figure 39 illustrates our multi-dimensional core and memory arrangement using the example of CUDA for $D = 2$ (two-dimensional arrangement).

C.5 ASM Levels

ASM levels are pairs $(l_{\text{ASM}}, d_{\text{ASM}})$ consisting of an ASM layer $l_{\text{ASM}} \in \mathbb{N}$ and ASM dimension $d_{\text{ASM}} \in \mathbb{N}$.

Figure 40 illustrates ASM levels using the example of CUDA's thread hierarchy. The figure shows that thread hierarchies can be considered as a tree in which each level is uniquely determined by a particular combination of a layer (block or thread in the case of CUDA) and dimension (x, y, or z). In the figure, we use lvl as an abbreviation for *level*, l for *layer*, and d for *dimension*.

For ASM layers and dimensions, we usually use their domain-specific identifiers, e.g., BLK/CC and x/y/z as aliases for numerical values of layers and dimensions.

C.6 MDH Levels

MDH levels are pairs $(l_{\text{MDH}}, d_{\text{MDH}})$ consisting of an MDH layer $l_{\text{MDH}} \in \mathbb{N}$ and MDH dimension $d_{\text{MDH}} \in \mathbb{N}$.

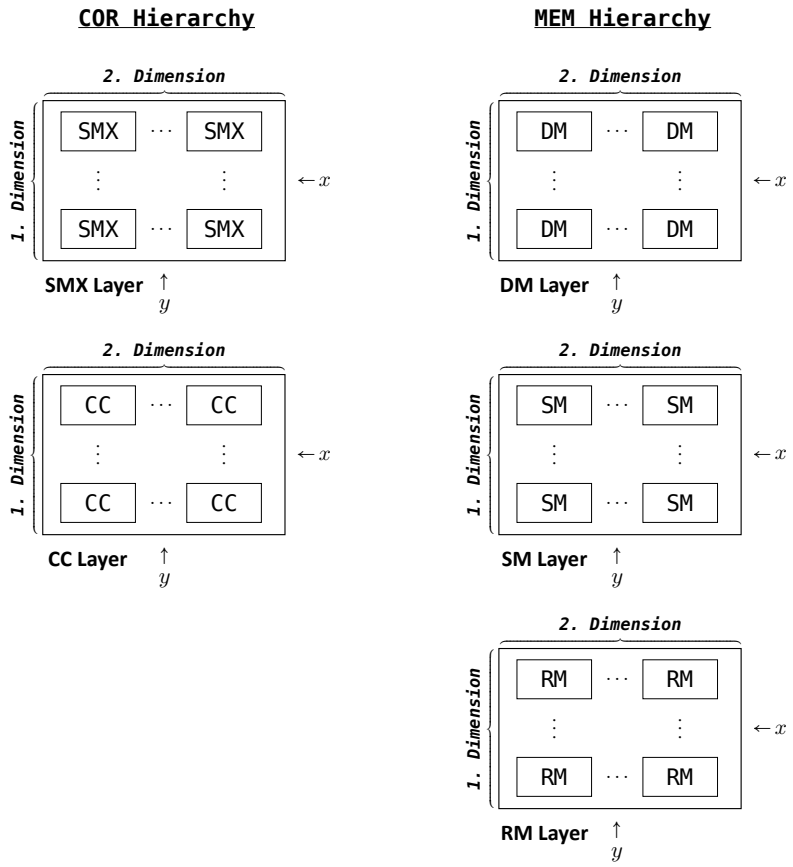


Fig. 39. Multi-dimensional ASM arrangement illustrated using CUDA for the case $D = 2$ (two dimensions)

Figure 41 illustrates MDH levels using as example the de-composition phase in Figure 17. The levels $(l_{\text{MDH}}, d_{\text{MDH}})$ can be derived from the super- and subscripts of combine operators' variables $p^{l_{\text{MDH}}}_{d_{\text{MDH}}}$.

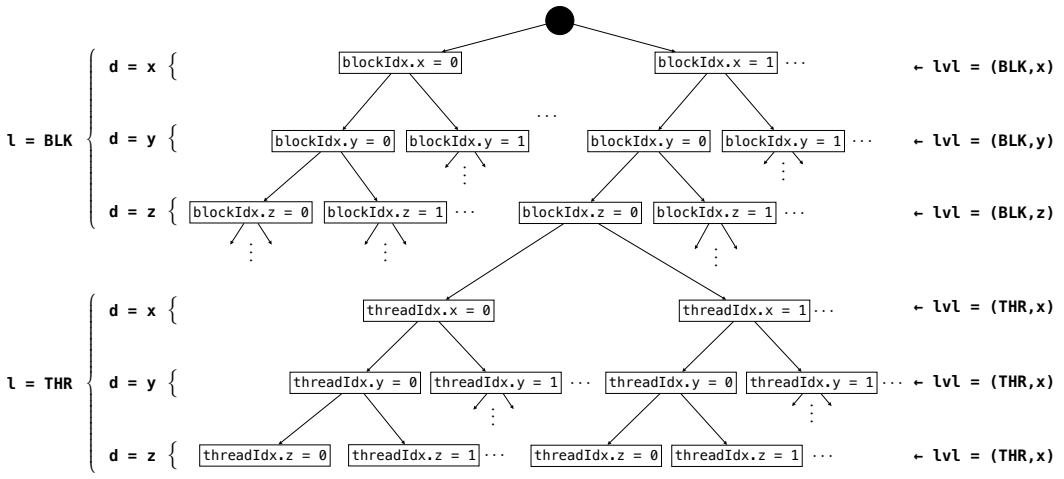


Fig. 40. ASM levels illustrated using CUDA's thread hierarchy

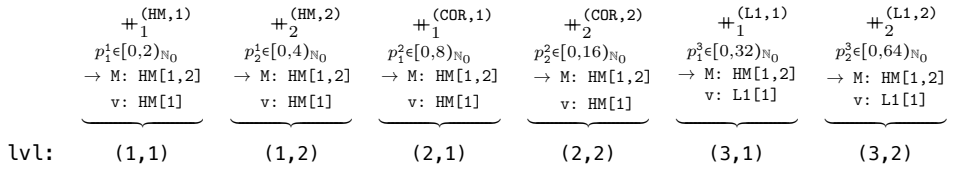


Fig. 41. MDH levels illustrated using as example the de-composition phase in Figure 17

C.7 MDA Partitioning

We demonstrate how we partition MDAs into equally sized parts (a.k.a. *uniform partitioning*).

Definition 28 (MDA Partitioning)**.** Let $\mathfrak{a} \in T[I_1, \ldots, I_D]$ be an arbitrary MDA that has scalar type $T \in \texttt{TYPE}$, dimensionality $D \in \mathbb{N}$, index sets $I = (I_1, \ldots, I_D) \in \texttt{MDA-IDX-SETS}^D$, and size $N = \{|I_1|, \ldots, |I_D|\} \in \mathbb{N}^D$. We consider $I_d = \{i_1^d, \ldots, i_{N_d}^d\}$, $d \in [1, D]_{\mathbb{N}}$, such that $i_1^d < \ldots < i_{N_d}^d$ represents a sorted enumeration of the elements in I_d. Let further $P = (\,(P_1^1, \ldots, P_D^1)\,, \ldots,\, (P_1^L, \ldots, P_D^L)\,)$ be an arbitrary tuple of L-many D-tuples of positive natural numbers such that $\prod_{l \in [1,L]_{\mathbb{N}}} P_d^l$ divides N_d (the number of indices of MDA $\mathfrak{a}$ in dimension d), for each $d \in \{1, \ldots, D\}$.

The *L-layered, D-dimensional, P-partitioning of MDA* $\mathfrak{a}$ is the L-layered, D-dimensional, P-partitioned low-level MDA $\mathfrak{a}_{\texttt{prt}}$ (Definition 12) that has scalar type T and index sets

$$I_d^{<p_d^1,\ldots,p_d^L>} :=$$

$$\{i_j \in I_d \mid j = OS + j',\ \text{for}\ \ OS := \sum_{l \in [1,L]_{\mathbb{N}}} p_d^l * \frac{N_d}{\prod_{l' \in [1,l]_{\mathbb{N}}} P_d^{l'}}\ \ \text{and}\ \ j' \in PS := \frac{N_d}{\prod_{l' \in [1,L]_{\mathbb{N}}} P_d^{l'}}\}$$

i.e., set $I_d^{<p_d^1,\ldots,p_d^L>}$ denotes for each choice of parameters $p_d^1, \ldots, p_d^L$ a part of the uniform partitioning of the ordered index set I_d (OS in the formula above represents the OffSet to the part, and PS

the Part's Size). The partitioned MDA $\mathfrak{a}_{\texttt{prt}}$ is defined as:

$$\mathfrak{a} \;=:\; \underbrace{\underset{p_1^1 \in P_1^1}{+\!\!+_1} \;\ldots\; \underset{p_D^1 \in P_D^1}{+\!\!+_D}}_{\text{Layer 1}} \;\ldots\; \underbrace{\underset{p_1^L \in P_1^L}{+\!\!+_1} \;\ldots\; \underset{p_D^L \in P_D^L}{+\!\!+_D}}_{\text{Layer } L} \; \mathfrak{a}_{\texttt{prt}}^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>}$$

i.e., the parts $\mathfrak{a}_{\texttt{prt}}^{<p_1^1,\ldots,p_D^1 \mid \ldots \mid p_1^L,\ldots,p_D^L>}$ are defined such that concatenating them results in the original MDA $\mathfrak{a}$.

C.8 TVM Schedule for `MatMul`

Listing 6 shows TVM's Ansor-generated schedule program for `MatMul` on input matrices of sizes 16×2048 and 2048×1000 taken from ResNet-50's training phase, discussed in Section 3.5. Code formatting, like names of variables and comments, have been shortened and adapted in the listing for brevity.

```
# exploiting fast memory resources for computed results
matmul_local, = s.cache_write([matmul], "local")
matmul_1, matmul_2, matmul_3 = tuple(matmul_local.op.axis) + tuple(matmul_local.op.reduce_axis)
SHR_1, REG_1 = s[matmul_local].split(matmul_1, factor=1)
THR_1, SHR_1 = s[matmul_local].split(SHR_1, factor=1)
DEV_1, THR_1 = s[matmul_local].split(THR_1, factor=4)
BLK_1, DEV_1 = s[matmul_local].split(DEV_1, factor=2)
SHR_2, REG_2 = s[matmul_local].split(matmul_2, factor=1)
THR_2, SHR_2 = s[matmul_local].split(SHR_2, factor=1)
DEV_2, THR_2 = s[matmul_local].split(THR_2, factor=20)
BLK_2, DEV_2 = s[matmul_local].split(DEV_2, factor=1)
SHR_3, REG_3 = s[matmul_local].split(matmul_3, factor=2)
DEV_3, SHR_3 = s[matmul_local].split(SHR_3, factor=128)
s[matmul_local].reorder(BLK_1, BLK_2, DEV_1, DEV_2, THR_1, THR_2, DEV_3, SHR_3, SHR_1, SHR_2, REG_3, REG_1, REG_2)

# low-level optimizations:
s[matmul_local].pragma(BLK_1, "auto_unroll_max_step", 512)
s[matmul_local].pragma(BLK_1, "unroll_explicit", True)

# tiling
matmul_1, matmul_2, matmul_3 = tuple(matmul.op.axis) + tuple(matmul.op.reduce_axis)
THR_1, SHR_REG_1 = s[matmul].split(matmul_1, factor=1)
DEV_1, THR_1 = s[matmul].split(THR_1, factor=4)
BLK_1, DEV_1 = s[matmul].split(DEV_1, factor=2)
THR_2, SHR_REG_2 = s[matmul].split(matmul_2, factor=1)
DEV_2, THR_2 = s[matmul].split(THR_2, factor=20)
BLK_2, DEV_2 = s[matmul].split(DEV_2, factor=1)
s[matmul].reorder(BLK_1, BLK_2, DEV_1, DEV_2, THR_1, THR_2, SHR_REG_1, SHR_REG_2)
s[matmul_local].compute_at(s[matmul], THR_2)

# block/thread assignments:
BLK_fused = s[matmul].fuse(BLK_1, BLK_2)
s[matmul].bind(BLK_fused, te.thread_axis("blockIdx.x"))
DEV_fused = s[matmul].fuse(DEV_1, DEV_2)
s[matmul].bind(DEV_fused, te.thread_axis("vthread"))
THR_fused = s[matmul].fuse(THR_1, THR_2)
s[matmul].bind(THR_fused, te.thread_axis("threadIdx.x"))

# exploiting fast memory resources for first input matrix:
A_shared = s.cache_read(A, "shared", [matmul_local])
A_shared_ax0, A_shared_ax1 = tuple(A_shared.op.axis)
A_shared_ax0_ax1_fused = s[A_shared].fuse(A_shared_ax0, A_shared_ax1)
A_shared_ax0_ax1_fused_o, A_shared_ax0_ax1_fused_i = s[A_shared].split(A_shared_ax0_ax1_fused, factor=1)
s[A_shared].vectorize(A_shared_ax0_ax1_fused_i)
A_shared_ax0_ax1_fused_o_o, A_shared_ax0_ax1_fused_o_i = s[A_shared].split(A_shared_ax0_ax1_fused_o, factor=80)
s[A_shared].bind(A_shared_ax0_ax1_fused_o_i, te.thread_axis("threadIdx.x"))
s[A_shared].compute_at(s[matmul_local], DEV_3)

# exploiting fast memory resources for second input matrix:
# ... (analogous to lines 40 – 47)
```

Listing 6. TVM schedule for Matrix Multiplication on NVIDIA Ampere GPU (variable names shortened for brevity)

D ADDENDUM SECTION 5

D.1 Data Characteristics used in Deep Neural Networks

Figure 42 shows the data characteristics used for the deep learning experiments in Figures 28 and 29 of Section 5. We use real-world characteristics taken from the neural networks `ResNet-50`, `VGG-16`, and `MobileNet`. For each network, we consider computations `MCC` and `MatMul` (Table 16), because these are the networks' most time-intensive building blocks. Each computation is called in each network on different data characteristics – we use for each combination of network and computation the two most time-intensive characteristics. Note that the MobileNet network does not use `MatMul` in its implementation.

The capsule variants `MCC_Capsule` in Figures 28 and 29 of Section 5 have the same characteristics as those listed for `MCC`s in Figure 42 – the only difference is that `MCC_Capsule`, in addition to the dimensions `N`, `H`, `W`, `K`, `R`, `S`, `C`, uses three additional dimensions `MI`, `MJ`, `MK`, each with a fixed size of 4. This is because `MCC_Capsule` operates on 4×4 matrices, rather than scalars as `MCC` does.

Network	Phase	N	H	W	K	R	S	C	Stride H	Stride W	Padding	P	Q	Image Format	Filter Format	Output Format
ResNet-50	Training	16	230	230	64	7	7	3	2	2	VALID	112	112	NHWC	KRSC	NPQK
	Inference	1	230	230	64	7	7	3	2	2	VALID	112	112	NHWC	KRSC	NPQK
VGG-16	Training	16	224	224	64	3	3	3	1	1	VALID	224	224	NHWC	KRSC	NPQK
	Inference	1	224	224	64	3	3	3	1	1	VALID	224	224	NHWC	KRSC	NPQK
MobileNet	Training	16	225	225	32	3	3	3	2	2	VALID	112	112	NHWC	KRSC	NPQK
	Inference	1	225	225	32	3	3	3	2	2	VALID	112	112	NHWC	KRSC	NPQK

(a) Data characteristics used for `MCC` experiments

Network	Phase	M	N	K	Transposition
ResNet-50	Training	16	1000	2048	NN
	Inference	1	1000	2048	NN
VGG-16	Training	16	4096	25088	NN
	Inference	1	4096	25088	NN

(b) Data characteristics used for `MatMul` experiments

Fig. 42. Data characteristics used for experiments in Section 5

D.2 Runtime and Accuracy of cuBLASEx

Listing 7 shows the runtime of `cuBLASEx` for its different *algorithm* variants. For demonstration, we use the example of matrix multiplication `MatMul` on `NVIDIA Volta GPU` for square input matrices of sizes 1024×1024. For each algorithm variant, we list both: 1) the runtime achieved by `cuBLASEx` (in nanoseconds `ns`), as well as 2) the maximum absolute deviation ($\texttt{delta}_{\texttt{max}}$ values) compared to a straightforward, sequential CPU computation. For example, the $\texttt{delta}_{\texttt{max}}$ value of algorithm `CUBLAS_GEMM_DEFAULT` is `3.14713e-05`, i.e., at least one value $c^{\text{GPU}}_{i,j}$ in the GPU-computed output matrix deviates by `3.14713e-05` from its corresponding, sequentially computed value $c^{\text{seq}}_{i,j}$ such that $|c^{\text{GPU}}_{i,j}| = |c^{\text{seq}}_{i,j}| + \texttt{3.14713e-05}$ (bar symbols $|\ldots|$ denote absolute value). All other GPU-computed values $c^{\text{GPU}}_{i',j'}$ deviate from their sequentially computed CPU-variant by `3.14713e-05` or less.

Note that `cuBLASEx` offers 42 algorithm variants, but not all of them are supported for all potential characteristics of the input and output data (size, memory layout, ...). For our `MatMul` example, the list of unsupported variants includes: `CUBLAS_GEMM_ALGO1`, `CUBLAS_GEMM_ALGO12`, etc.

```
CUBLAS_GEMM_DEFAULT: 188416ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO2: 190464ns (delta_max: 6.86646e-05)
CUBLAS_GEMM_ALGO3: 186368ns (delta_max: 6.86646e-05)
CUBLAS_GEMM_ALGO4: 185344ns (delta_max: 6.86646e-05)
CUBLAS_GEMM_ALGO5: 181248ns (delta_max: 6.86646e-05)
CUBLAS_GEMM_ALGO6: 181248ns (delta_max: 6.86646e-05)
CUBLAS_GEMM_ALGO7: 178176ns (delta_max: 4.1008e-05)
CUBLAS_GEMM_ALGO8: 189440ns (delta_max: 4.1008e-05)
CUBLAS_GEMM_ALGO9: 171008ns (delta_max: 4.1008e-05)
CUBLAS_GEMM_ALGO10: 188416ns (delta_max: 4.1008e-05)
CUBLAS_GEMM_ALGO11: 191488ns (delta_max: 4.1008e-05)
CUBLAS_GEMM_ALGO18: 185344ns (delta_max: 2.67029e-05)
CUBLAS_GEMM_ALGO19: 172032ns (delta_max: 2.67029e-05)
CUBLAS_GEMM_ALGO20: 192512ns (delta_max: 2.67029e-05)
CUBLAS_GEMM_ALGO21: 201728ns (delta_max: 1.90735e-05)
CUBLAS_GEMM_ALGO22: 177152ns (delta_max: 1.90735e-05)
CUBLAS_GEMM_ALGO23: 194560ns (delta_max: 1.90735e-05)
CUBLAS_GEMM_DEFAULT_TENSOR_OP: 184320ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO0_TENSOR_OP:  62464ns (delta_max: 0.0131454)
CUBLAS_GEMM_ALGO1_TENSOR_OP:  52224ns (delta_max: 0.0131454)
CUBLAS_GEMM_ALGO2_TENSOR_OP:  190464ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO3_TENSOR_OP:  189440ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO4_TENSOR_OP:  183296ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO5_TENSOR_OP:  183296ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO6_TENSOR_OP:  183296ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO7_TENSOR_OP:  189440ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO8_TENSOR_OP:  183296ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO9_TENSOR_OP:  189440ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO10_TENSOR_OP: 188416ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO11_TENSOR_OP: 183296ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO12_TENSOR_OP: 183296ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO13_TENSOR_OP: 188416ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO14_TENSOR_OP: 183296ns (delta_max: 3.14713e-05)
CUBLAS_GEMM_ALGO15_TENSOR_OP: 189440ns (delta_max: 3.14713e-05)
```

Listing 7. Runtime of cuBLASEx for its different *algorithm* variants on NVIDIA Volta GPU when computing MatMul on square 1024×1024 input matrices

E CODE GENERATION

This section outlines how imperative-style pseudocode is generated from our low-level program representation in Section 3. Code optimizations that are below the abstraction level of our low-level representation (like loop fusion and loop unrolling) are considered in this work as *code-level optimizations* and briefly outlined in Section E.3. We aim to discuss and illustrate our code generation approach in detail in future work.

In the following, we highlight tuning parameters gray in our pseudocode which are substituted by concrete, optimized values in our executable program code. Static parameters, such as scalar types and the number of input/output buffers, are denoted in math font and also substituted by concrete values in our executable code. We list meta-parameters in angle brackets `<...>`, and other static function annotations in double angle brackets `<<...>>`, e.g., `idx<<OUT>><<1,1>>` for denoting in our pseudocode index function $\mathfrak{idx}_{1,1}^{\mathsf{OUT}}$ used in Figure 15.

Overall Structure

Listing 8 shows the overall structure of our generated code. We implement a particular expression in our low-level representation (Figure 19) as a compute kernel that is structured in the following phases: 0) preparation (Section E.0), 1) de-composition phase (Section E.1), 2) scalar phase (Section E.2), 3) re-composition phase (Section E.3).

```
kernel mdh(
  T_1^IB trans_ll_IB<<⊥>><<1>><*,...,*>,...,T_B^IB trans_ll_IB<<⊥>><<B^IB>><*,...,*>,
  T_1^OB trans_ll_OB<<⊥>><<1>><*,...,*>,...,T_B^OB trans_ll_OB<<⊥>><<B^OB>><*,...,*>
)

  // 0. preparation
  ...
  // 2. de-composition phase
  ...
  // 3. scalar phase
  ...
  // 4. re-composition phase
  ...
}
```

Listing 8. Overall structure of our generated code

E.0 Preparation

Listing 9 shows the preparation phase. It prepares in five sub-phases the basic building blocks used in our low-level representation: 1) `md_hom` (Section E.0.1), 2) `inp_view` (Section E.0.2), 3) `out_view` (Section E.0.3), 4) BUFs (Section E.0.4), 5) MDAs (Section E.0.5).

```
// 0. preparation
  // 0.1. md_hom
  ...
  // 0.2. inp_view
  ...
  // 0.3. out_view
  ...
  // 0.4. BUFs
  ...
  // 0.5. MDAs
  ...
```

Listing 9. Preparation Phase

E.0.1 md_hom.

Listing 10 shows the user-defined scalar function and low-level combine operators (Definition 15) which are both provided by the user via higher-order function md_hom (Definition 4).

Listing 11 shows how we pre-implement for the user the two combine operators *concatenation* (Example 1) and *point-wise combination* (Example 2).

Listing 12 shows how we pre-implement the *inverse of concatenation* (Definition C.2), which we will use in the de-composition phase (via Definition 28).

```
1  // 0.1. md_hom
2
3    // 0.1.1. scalar function
4    f( T^INP inp ) -> T^OUT out
5    {
6      // ... (user defined)
7    }
8
9    // 0.1.2. combine operators
10   ∀d ∈ [1, D]_ℕ :
11   co<<d>><I_1, ..., I_{d-1}, I_{d+1}, ..., I_D ∈ MDA-IDX-SETs, (P, Q) ∈ MDA-IDX-SETs ẋ MDA-IDX-SETs>(
12     T^OUT[I_1, ..., I_{d-1}, ⇒^d_MDA(P) , I_{d+1}, ..., I_D] lhs ,
13     T^OUT[I_1, ..., I_{d-1}, ⇒^d_MDA(Q) , I_{d+1}, ..., I_D] rhs ) -> T^OUT[I_1, ..., I_{d-1}, ⇒^d_MDA(P ⊎ Q), I_{d+1}, ..., I_D] res
14   {
15     // ... (user defined)
16   }
```

Listing 10. Scalar Function & Combine Operators

```
1  // 0.1.2. combine operators
2
3    // pre-implemented combine operators
4
5    // concatenation
6    ∀d ∈ ℕ :
7    cc<<d>><I_1, ..., I_{d-1}, I_{d+1}, ..., I_D ∈ MDA-IDX-SETs, (P, Q) ∈ MDA-IDX-SETs ẋ MDA-IDX-SETs>(
8      T^OUT[I_1, ..., I_{d-1}, id(P) , I_{d+1}, ..., I_D] lhs ,
9      T^OUT[I_1, ..., I_{d-1}, id(Q) , I_{d+1}, ..., I_D] rhs ) -> T^OUT[I_1, ..., I_{d-1}, id(P ⊎ Q), I_{d+1}, ..., I_D] res
10   {
11     int i_1 ∈ I_1
12       ⋱
13         int i_{d-1} ∈ I_{d-1}
14           int i_{d+1} ∈ I_{d+1}
15             ⋱
16               int i_D ∈ I_D
17               {
18                 int i_d ∈ P
19                   res[ i_1,...,i_d,...,i_D] := lhs[ i_1,...,i_d,...,i_D];
20                 int i_d ∈ Q
21                   res[ i_1,...,i_d,...,i_D] := rhs[ i_1,...,i_d,...,i_D];
22               }
23   }
24
25   // point-wise combination
```

```
∀d ∈ ℕ:
pw<<d>><I_1, ..., I_{d-1}, I_{d+1}, ..., I_D ∈ MDA-IDX-SETs, (P, Q) ∈ MDA-IDX-SETs ×̇ MDA-IDX-SETs>(
  ⊕ : T^OUT × T^OUT → T^OUT )( T^OUT[I_1, ..., I_{d-1}, 0_f(P), I_{d+1}, ..., I_D] lhs ,
                               T^OUT[I_1, ..., I_{d-1}, 0_f(Q), I_{d+1}, ..., I_D] rhs )
-> T^OUT[I_1, ..., I_{d-1}, 0_f(P ⊎ Q), I_{d+1}, ..., I_D] res
{
  int i_1 ∈ I_1
    ⋱
      int i_{d-1} ∈ I_{d-1}
        int i_{d+1} ∈ I_{d+1}
          ⋱
            int i_D ∈ I_D
            {
              res[ i_1,...,i_{d-1} , 0 , i_{d+1},...,i_D]
                :=          lhs[ i_1,...,i_{d-1} , 0 , i_{d+1},...,i_D]
                    atomic(⊕) rhs[ i_1,...,i_{d-1} , 0 , i_{d+1},...,i_D];
            }
}
```

Listing 11. Pre-Implemented Combine Operators

```
// 0.1.2. combine operators

  // pre-implemented combine operators

  // inverse concatenation
  ∀d ∈ ℕ:
  cc_inv<<d>><I_1, ..., I_{d-1}, I_{d+1}, ..., I_D ∈ MDA-IDX-SETs, (P, Q) ∈ MDA-IDX-SETs ×̇ MDA-IDX-SETs>(
    T^INP[I_1, ..., I_{d-1}, id(P ⊎ Q), I_{d+1}, ..., I_D] res ) -> ( T^INP[I_1, ..., I_{d-1}, id(P) , I_{d+1}, ..., I_D] lhs ,
                                                                      T^INP[I_1, ..., I_{d-1}, id(Q) , I_{d+1}, ..., I_D] rhs )
  {
    int i_1 ∈ I_1
      ⋱
        int i_{d-1} ∈ I_{d-1}
          int i_{d+1} ∈ I_{d+1}
            ⋱
              int i_D ∈ I_D
              {
                int i_d ∈ P
                  res[ i_1,...,i_d,...,i_D] =: lhs[ i_1,...,i_d,...,i_D];
                int i_d ∈ Q
                  res[ i_1,...,i_d,...,i_D] =: rhs[ i_1,...,i_d,...,i_D];
              }
  }
```

Listing 12. Pre-Implemented Combine Operators

E.0.2 inp_view .

Listing 13 shows the user-defined index functions provided by the user via higher-order function inp_view (Definition 8).

```
// 0.2. inp_view

  // index functions
  ∀b ∈ [1, B^IB]_ℕ, a ∈ [1, A_b^IB]_ℕ: ∀d ∈ [1, D_b^IB]_ℕ:
  static
  idx<<INP>><<b,a>><<d>>( int i_MDA_1 , ... , i_MDA_D ) -> int i_BUF_d
```

```
7   {
8       // ... (user defined)
9   }
```

Listing 13. Index Functions (input)

E.0.3 `out_view`.

Listing 14 shows the user-defined index functions provided by the user via higher-order function `out_view` (Definition 10).

```
1   // 0.3. out_view
2
3     // index functions
4     ∀b ∈ [1, B^OB]_ℕ, a ∈ [1, A_b^OB]_ℕ: ∀d ∈ [1, D_b^OB]_ℕ:
5     static
6     idx<<OUT>><<<b,a>>><<<d>>>( int i_MDA_1 , ... , i_MDA_D ) -> int i_BUF_d
7     {
8         // ... (user defined)
9     }
```

Listing 14. Index Functions (output)

E.0.4 BUFs.

Listing 15 shows our implementation of low-level BUFs (Definition 13). We compute BUFs' sizes using the ranges of their index functions (Definitions 8 and 10). Moreover, we partially evaluate BUFs' meta-parameters `MEM` (memory region) and σ (memory layout) immediately, as the same values are re-used for them during program runtime.

The BUFs in lines 30 and 45 as well as in lines 69 and 84 represent the BUFs' transposed function representation (Definition 13), and the BUFs in lines 23, 37, and 52 as well as in lines 62, 76, and 91 are the transposed BUFs' ordinary low-level BUF representation.

```
1   // 0.4. BUFs
2
3     // 0.4.1. compute BUF sizes
4     ∀IO ∈ {IB, OB}: ∀b ∈ [1, B^IO]_ℕ ∀d ∈ [1, D_b^IO]_ℕ:
5     static N<<IO>><<<b>>><<<d>>>( mda_idx_set I_1 , ... , I_D ) -> int N_b_d
6     {
7       N_b_d := 0;
8
9       i_1 ∈ I_1
10        ⋱
11          i_D ∈ I_D
12          {
13            ∀a ∈ [1, A_b^IB]_ℕ:
14            N_b_d :=max 1 + idx<<IO>><<<b,a>>><<<d>>>( i_1,...,i_D );
15          }
16    }
17
18    // 0.4.2. input BUFs
19
20    // initial BUFs
21    ∀b ∈ [1, B^IB]_ℕ:
22    static ll_IB<<⊥>><<<b>>>< ▼_1^(⊥) ∈ #PRT(1,1) , ... , ▼_D^(⊥) ∈ #PRT(L,D) >( int i_1,...,
23      int i_D_b^IB ) -> T_b^IB a
24    {
```

```
25    a := trans_ll_IB<<⊥>><<b>><<▼^(⊥)_1,...,▼^(⊥)_L>[ i_1 , ... , i_D^IB ];
26  }
27
28  // de-composition BUFs
29  ∀(l,d) ∈ MDH-LVL: ∀b ∈ [1,B^IB]_ℕ:
30  auto trans_ll_IB<<l,d>><<b>><<▼^(l,d)_1 ∈ #PRT(1,1) ,...,▼^(l,d)_L ∈ #PRT(L,D) >
31    := ↓-mem^<b>(l,d)  T_b^IB[ N<<INP>><<b>><< σ^<b>_↓-mem(l,d)(1)  >>( (⇒^d_#^MDA_MDA(N_d))_{d∈[1,D]_ℕ} ) ,
32                                  ⋮
33                       N<<INP>><<b>><< σ^<b>_↓-mem(l,d)(D_b^IB) >>( (⇒^d_#^MDA_MDA(N_d))_{d∈[1,D]_ℕ} ) ];
34
35  ∀(l,d) ∈ MDH-LVL: ∀b ∈ [1,B^IB]_ℕ:
36  static ll_IB<<l,d>><<b>><<▼^(l,d)_1 ∈ #PRT(1,1) ,...,▼^(l,d)_L ∈ #PRT(L,D) >( int i_1,...,
37    int i_D_b^IB ) -> T_b^IB a
38  {
39    a := trans_ll_IB<<l,d>><<b><<▼^(l,d)_1,...,▼^(l,d)_L>[ i_ σ^<b>_↓-mem(l,d)(1)  , ... ,
40      i_ σ^<b>_↓-mem(l,d)(D_b^IB)  ];
41  }
42
43  // scalar BUFs
44  ∀b ∈ [1,B^IB]_ℕ:
45  auto trans_ll_IB<f>><<b>><<▼^(f)_1 ∈ #PRT(1,1) ,...,▼^(f)_L ∈ #PRT(L,D) >
46    := f↓-mem^<b>  T_b^IB[ N<<INP>><<b>><< σ^<b>_f↓-mem(1)  >>( (⇒^d_#^MDA_MDA(N_d))_{d∈[1,D]_ℕ} ) ,
47                                ⋮
48                       N<<INP>><<b>><< σ^<b>_f↓-mem(D_b^IB) >>( (⇒^d_#^MDA_MDA(N_d))_{d∈[1,D]_ℕ} ) ];
49
50  ∀b ∈ [1,B^IB]_ℕ:
51  static ll_IB<<f>><<b>><<▼^(f)_1 ∈ #PRT(1,1) ,...,▼^(f)_L ∈ #PRT(L,D) >( int i_1,...,
52    int i_D_b^IB ) -> T_b^IB a
53  {
54    a := trans_ll_IB<<f>><<b><<▼^(f)_1,...,▼^(f)_L>[ i_ σ^<b>_f↓-mem(1)  , ... , i_ σ^<b>_f↓-mem(D_b^IB)  ];
55  }
56
57  // 0.4.3. output BUFs
58
59  // initial BUFs
60  ∀b ∈ [1,B^OB]_ℕ:
61  static ll_OB<<⊥>><<b>><<▲^(⊥)_1 ∈ #PRT(1,1) ,...,▲^(⊥)_L ∈ #PRT(L,D) >( int i_1,...,
62    int i_D_b^OB ) -> T_b^OB a
63  {
64    a := trans_ll_OB<<⊥>><<b>><<▲^(⊥)_1,...,▲^(⊥)_L>[ i_1 , ... , i_D_b^OB ];
65  }
66
67  // re-composition BUFs
68  ∀(l,d) ∈ MDH-LVL: ∀b ∈ [1,B^OB]_ℕ:
69  auto trans_ll_OB<<l,d>><<b>><<▲^(l,d)_1 ∈ #PRT(1,1) ,...,▲^(l,d)_L ∈ #PRT(L,D) >
```

```
:= ↑-mem<b>(l, d)  T_b^OB[ N<<OUT>>><<b>>><< σ_{↑-mem}^{<b>}(l, d)(1)  >>( ( ⇉_{⊛ MDA}^{d MDA}(N_d) )_{d∈[1,D]_ℕ} ) ,
                          ⋮
                   N<<OUT>>><<b>>><< σ_{↑-mem}^{<b>}(l, d)(D_b^OB) >>( ( ⇉_{⊛ MDA}^{d MDA}(N_d) )_{d∈[1,D]_ℕ} ) ];

∀(l, d) ∈ MDH-LVL : ∀b ∈ [1, B^OB]_ℕ :
static ll_OB<<l, d>>><<b>>>< ▲_1^{(l,d)1} ∈ #PRT(1, 1) , ... , ▲_D^{(l,d)L} ∈ #PRT(L, D) >( int i_1, ... ,
  int i_D_b^OB ) -> T_b^OB a
{
  a := trans_ll_OB<<l, d>>><<b>>>< ▲_1^{(l,d)1}, ... , ▲_D^{(l,d)L} >[ i_ σ_{↑-mem}^{<b>}(l, d)(1)  , ... ,
    i_ σ_{↑-mem}^{<b>}(l, d)(D_b^OB) ];
}

// scalar BUFs
∀b ∈ [1, B^OB]_ℕ :
auto trans_ll_OB<f>>><<b>>>< ▲_1^{(f)1} ∈ #PRT(1, 1) , ... , ▲_D^{(f)L} ∈ #PRT(L, D) >
  := f↑-mem<b>  T_b^OB[ N<<OUT>>><<b>>><< σ_{f↑-mem}^{<b>}(1)  >>( ( ⇉_{⊛ MDA}^{d MDA}(N_d) )_{d∈[1,D]_ℕ} ) ,
                          ⋮
                   N<<OUT>>><<b>>><< σ_{f↑-mem}^{<b>}(D_b^OB) >>( ( ⇉_{⊛ MDA}^{d MDA}(N_d) )_{d∈[1,D]_ℕ} ) ];

∀b ∈ [1, B^OB]_ℕ :
static ll_OB<<f>>><<b>>>< ▲_1^{(f)1} ∈ #PRT(1, 1) , ... , ▲_D^{(f)L} ∈ #PRT(L, D) >( int i_1, ... ,
  int i_D_b^OB ) -> T_b^OB a
{
  a := trans_ll_OB<<f>>><<b>>>< ▲_1^{(f)1}, ... , ▲_D^{(f)L} >[ i_ σ_{f↑-mem}^{<b>}(1)  , ... , i_ σ_{f↑-mem}^{<b>}(D_b^OB) ];
}
```

Listing 15. Low-Level BUFs

where $\blacktriangledown_{\mathfrak{d}}^{(\bullet)\mathfrak{l}}$ and $\blacktriangle_{\mathfrak{d}}^{(\bullet)\mathfrak{l}}$, for $\bullet \in \{\bot\} \cup \texttt{MDH-LVL} \cup \{\texttt{f}\}$, are textually replaced by:

$$\blacktriangledown_{\mathfrak{d}}^{(\bullet)\mathfrak{l}} = \begin{cases} p_{\mathfrak{d}}^{\mathfrak{l}} & : \sigma_{\downarrow\text{-ord}}(\mathfrak{l}, \mathfrak{d}) < \bullet \\ * & : \text{else} \end{cases}$$

$$\blacktriangle_{\mathfrak{d}}^{(\bullet)\mathfrak{l}} = \begin{cases} p_{\mathfrak{d}}^{\mathfrak{l}} & : \sigma_{\uparrow\text{-ord}}(\mathfrak{l}, \mathfrak{d}) < \bullet \\ * & : \text{else} \end{cases}$$

(symbol $*$ is taken from Definition 23) where $<$ is defined according to the lexicographical order on $\texttt{MDH-LVL} = [1, L]_{\mathbb{N}} \times [1, D]_{\mathbb{N}}$, and:

$$\forall (l, d) \in \texttt{MDH-LVL} : \bot :< (l, d) :< f$$

Functions

$$\overset{1}{\underset{++}{\Rightarrow}}_{\text{MDA}}^{\text{MDA}}, \ \dots, \ \overset{D}{\underset{++}{\Rightarrow}}_{\text{MDA}}^{\text{MDA}}$$

are the index set functions *id* of combine operator concatenation ⧺ (Example 1), and functions

$$\overset{1}{\underset{\circledast}{\Rightarrow}}\text{MDA}, \ldots, \overset{D}{\underset{\circledast}{\Rightarrow}}\text{MDA}$$

are the index set functions of combine operators $\circledast_1, \ldots, \circledast_D$.

Note that we use generous BUFs sizes (lines 31-33, 46-48, 70-72, 85-87), as imperative-style programming models usually struggle with non-contiguous index ranges. We discuss optimizations targeting BUF sizes in Section E.3.

Note further that we do not need to initialize output buffers with neutral elements of combine operators in lines 64, 79, and 93 of Listing 15, as the buffers are initialized implicitly in the re-composition phase (Section E.3).

E.0.5 MDAs.

Listing 16 shows our implementation of low-level MDAs (Definitions 12 and 28).

Note that for a particular choice of meta-parameters, low-level BUFs (Definition 13) are ordinary BUFs (Definition 5), as required by the types of functions `inp_view` and `out_view` (Definitions 8 and 10).

```
1  // 0.5. MDAs
2
3    // 0.5.1. partitioned index sets
4    ∀d ∈ [1, D]ℕ :
5    static I<<d>><p_d^1 ∈ #PRT(1, d) , ... , p_d^L ∈ #PRT(L, d) >( int j' ) -> int i_j
6    {
7      i_j := ( p_d^1 * ( N_d / ( #PRT(1, d) )                ) +
8                 ⋮
9               p_d^L * ( N_d / ( #PRT(1, d) *...* #PRT(L, d) ) ) + j' );
10   }
11
12   // 0.5.2. input MDAs
13   ∀• ∈ {⊥} ∪ MDH-LVL ∪ {f}:
14   static ll_inp_mda<<•>>< (•)▼_1^1 ∈ #PRT(1, 1) , ... , (•)▼_D^L ∈ #PRT(L, D) >( int i_1 , ... ,
15     int i_D ) -> T_b^IB a
16   {
17     ∀b ∈ [1, B^IB]ℕ , a ∈ [1, A_b^IB]ℕ :
18     a := ll_IB<<•>><<b>>< (•)▼_1^1 , ... , (•)▼_D^L >( idx<<INP>><<b , a>><< 1 >>( i_1 , ... , i_D ) ,
19                                                        ⋮
20                                                idx<<INP>><<b , a>><<D_b^IB>>( i_1 , ... , i_D ) );
21   }
22
23   // 0.5.3. output MDAs
24   ∀• ∈ {⊥} ∪ MDH-LVL ∪ {f}:
25   static ll_out_mda<<•>>< (•)▲_1^1 ∈ #PRT(1, 1) , ... , (•)▲_D^L ∈ #PRT(L, D) >( int i_1 , ... ,
26     int i_D ) -> T_b^OB a
27   {
28     ∀b ∈ [1, B^OB]ℕ , a ∈ [1, A_b^OB]ℕ :
29     a := ll_OB<<•>><<b>>< (•)▲_1^1 , ... , (•)▲_D^L >( idx<<OUT>><<b , a>><< 1 >>( i_1 , ... , i_D ) ,
30                                                        ⋮
31                                                idx<<OUT>><<b , a>><<D_b^OB>>( i_1 , ... , i_D ) );
32   }
```

Listing 16. Low-Level MDAs

For computing the partitioned index sets (lines 3-10), we exploit the following proposition.

Proposition 1. Let $\mathfrak{a} \in T[N_1, \ldots, N_D]$ be an arbitrary MDA that operates on contiguous index sets $[1, N_d)_{\mathbb{N}}$, $d \in [1, D]_{\mathbb{N}}$. Let further be

$$\mathfrak{a}^{<(p_1^1,\ldots,p_d^1)\in P_1^1\times\ldots\times P_D^1 \;\mid\; \ldots \;\mid\; (p_1^L,\ldots,p_D^L)\in P_1^L\times\ldots\times P_D^L>} : I_1^{<p_1^1 \cdots p_1^L>} \times \ldots \times I_D^{<p_D^1 \cdots p_D^L>} \to T$$

an arbitrary L-layered, D-dimensional, P-partitioning of MDA $\mathfrak{a}$.

It holds that j-th element within an MDA's part is accessed via index j:

$$I_d^{<p_d^1 \cdots p_d^L>} = \{ \underbrace{\sum_{l\in[1,L]_{\mathbb{N}}} p_d^l * \frac{N_d}{\prod_{l'\in[1,l]_{\mathbb{N}}} P_d^{l'}}}_{\text{OS}} + 0, \underbrace{\sum_{l\in[1,L]_{\mathbb{N}}} p_d^l * \frac{N_d}{\prod_{l'\in[1,l]_{\mathbb{N}}} P_d^{l'}}}_{\text{OS}} + 1, \quad \ldots \}$$

Proof. Since MDA $\mathfrak{a}$'s index sets are contiguous ranges of natural numbers, it holds the i_j – the index to access the j-th element within an MDA's part (Definition 28) – is equal to j itself. □

E.1 De-Composition Phase

Listing 17 shows our implementation of the de-composition phase (Figure 19).

```
1  // 1. de-composition phase
2
3    // 1.1. initialization
4    ll_inp_mda<<⊥>> =: ll_inp_mda<< σ↓-ord(1,1) >>
5
6    // 1.2. main
7    int p_σ↓-ord(1,1) ∈< ↔↓-ass (1,1) > #PRT ( σ↓-ord(1,1) )
8    {
9      ll_inp_mda<< σ↓-ord(1,1) >> =:cc< σ↓-ord(1,1) > inp_mda<< σ↓-ord(1,2) >>;
10     int p_σ↓-ord(1,2) ∈< ↔↓-ass (1,2) > #PRT ( σ↓-ord(1,2) )
11     {
12       ll_inp_mda<< σ↓-ord(1,2) >> =:cc< σ↓-ord(1,2) > inp_mda<< σ↓-ord(1,3) >>;
13         ⋱
14           int p_σ↓-ord(L,D) ∈< ↔↓-ass (L,D) > #PRT ( σ↓-ord(L,D) )
15           {
16             ll_inp_mda<< σ↓-ord(L,D) >> =:cc< σ↓-ord(L,D) > inp_mda<<f>>;
17           }
18         ⋰
19     }
20   }
```

Listing 17. De-Composition Phase

where

```
ll_inp_mda<<l,d>> =:cc<l,d> ll_inp_mda<<l',d'>>
```

abbreviates

```
ll_inp_mda<<l',d'>><(l',d')▼1_1,...,(l',d')▼L_D>, ll_inp_mda<<l,d>><(l,d)▼1_1,...,(l,d)▼L_D>
:=  cc_inv<<d>><1⇒MDA ∥MDA( I<<1>><(l,d)■1_1,...,(l,d)■L_1>(0) ), // I_1
```

$$\begin{array}{ll} \vdots & \texttt{//}\ \ldots, I_{d-1}, I_{d+1}, \ldots \\ \overset{D}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}\texttt{(I<<}D\texttt{>><}\overset{(l,d)}{\blacksquare}{}^{1}_{D}\texttt{,...,}\overset{(l,d)}{\blacksquare}{}^{L}_{D}\texttt{>(0)),} & \texttt{//}\ I_D \\ \overset{d}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}\texttt{(I<<}\,d\,\texttt{>><}\overset{(l,d)}{\boxplus}{}^{1}_{d}\texttt{,...,}\overset{(l,d)}{\boxplus}{}^{L}_{d}\texttt{>(0)),} & \texttt{//}\ P \\ \overset{d}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}\texttt{(I<<}\,d\,\texttt{>><}\overset{(l,d)}{\boxtimes}{}^{1}_{d}\texttt{,...,}\overset{(l,d)}{\boxtimes}{}^{L}_{d}\texttt{>(0))} & \texttt{//}\ Q \\ \texttt{>(ll\_inp\_mda<<l,d>><}\overset{(l,d)}{\blacktriangledown}{}^{1}_{1}\texttt{,...,}\overset{(l,d)}{\blacktriangledown}{}^{L}_{D}\texttt{>)} & \end{array}$$

Here, functions $\overset{1}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}, \ldots, \overset{D}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}$ are the index set functions *id* of combine operator concatenation $+\!\!+_1, \ldots, +\!\!+_D$ (Example 1), and $\overset{(\bullet)}{\blacksquare}{}^{\mathfrak{l}}_{\mathfrak{d}}$, $\overset{(\bullet)}{\boxplus}{}^{\mathfrak{l}}_{\mathfrak{d}}$, $\overset{(\bullet)}{\boxtimes}{}^{\mathfrak{l}}_{\mathfrak{d}}$, for $\bullet \in \texttt{MDH-LVL}$, are textually replaced by:

$$\overset{(\bullet)}{\blacksquare}{}^{\mathfrak{l}}_{\mathfrak{d}} := \begin{cases} p\_(\mathfrak{l},\mathfrak{d}) & : \ \sigma_{\downarrow\text{-ord}}(\mathfrak{l},\mathfrak{d}) < \bullet \\ [p\_(\mathfrak{l},\mathfrak{d}),\ \#\mathsf{PRT}(\mathfrak{l},\mathfrak{d})\ )_{\mathbb{N}_0} & : \ (\mathfrak{l},\mathfrak{d}) = \bullet \\ [0,\ \#\mathsf{PRT}(\mathfrak{l},\mathfrak{d})\ )_{\mathbb{N}_0} & : \ \sigma_{\downarrow\text{-ord}}(\mathfrak{l},\mathfrak{d}) > \bullet \end{cases}$$

$$\overset{(\bullet)}{\boxplus}{}^{\mathfrak{l}}_{\mathfrak{d}} := \begin{cases} p\_(\mathfrak{l},\mathfrak{d}) & : \ \sigma_{\downarrow\text{-ord}}(\mathfrak{l},\mathfrak{d}) < \bullet \\ p\_(\mathfrak{l},\mathfrak{d}) & : \ (\mathfrak{l},\mathfrak{d}) = \bullet \\ [0,\ \#\mathsf{PRT}(\mathfrak{l},\mathfrak{d})\ )_{\mathbb{N}_0} & : \ \sigma_{\downarrow\text{-ord}}(\mathfrak{l},\mathfrak{d}) > \bullet \end{cases}$$

$$\overset{(\bullet)}{\boxtimes}{}^{\mathfrak{l}}_{\mathfrak{d}} := \begin{cases} p\_(\mathfrak{l},\mathfrak{d}) & : \ \sigma_{\downarrow\text{-ord}}(\mathfrak{l},\mathfrak{d}) < \bullet \\ (p\_(\mathfrak{l},\mathfrak{d}),\ \#\mathsf{PRT}(\mathfrak{l},\mathfrak{d})\ )_{\mathbb{N}_0} & : \ (\mathfrak{l},\mathfrak{d}) = \bullet \\ [0,\ \#\mathsf{PRT}(\mathfrak{l},\mathfrak{d})\ )_{\mathbb{N}_0} & : \ \sigma_{\downarrow\text{-ord}}(\mathfrak{l},\mathfrak{d}) > \bullet \end{cases}$$

where $<$ is defined as lexicographical order, according to Section E.0.4.
Note that we re-use `inp_mda<<`l,d`>>` for the intermediate results given by different iterations of variable `p_(l,d)`. Correctness is ensured, as it holds:

$$A \subseteq B \ \Rightarrow\ \overset{d}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}(A) \ \subseteq\ \overset{d}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}(B)$$

MDA `inp_mda<<`l,d`>>` has the following type when used for the intermediate result in a particular iteration of `p_(l,d)`:

$$\overset{1}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}(I_1^{<\overset{(l,d)}{\blacksquare}{}^{1}_{1},\ldots,\overset{(l,d)}{\blacksquare}{}^{1}_{D}|\ldots|\overset{(l,d)}{\blacksquare}{}^{L}_{1},\ldots,\overset{(l,d)}{\blacksquare}{}^{L}_{D}>}) \times \ldots \times \overset{D}{\underset{+\!\!+}{\Rightarrow}}{}^{\mathsf{MDA}}_{\mathsf{MDA}}(I_D^{<\overset{(l,d)}{\blacksquare}{}^{1}_{1},\ldots,\overset{(l,d)}{\blacksquare}{}^{1}_{D}|\ldots|\overset{(l,d)}{\blacksquare}{}^{L}_{1},\ldots,\overset{(l,d)}{\blacksquare}{}^{L}_{D}>}) \to T^{\mathsf{INP}}$$

Here, for a set $P \subseteq [0,\ \#\mathsf{PRT}(l,d)\ )_{\mathbb{N}_0}$, index set $I_d^{<\ldots|\ldots P\ldots|\ldots>}$ denotes $\bigcup_{p_d^l \in P} I_d^{<\ldots|\ldots p_d^l\ldots|\ldots>}$.

E.2 Scalar Phase

Listing 18 shows our implementation of the scalar phase (Figure 19).

```
1  // 2. scalar phase
2  int p_ σ_f-ord(1,1) ∈^{<↔_f-ass (1,1)>} #PRT( σ_f-ord(1,1) )
3    ⋱
4      int p_ σ_f-ord(L,D) ∈^{<↔_f-ass (L,D)>} #PRT( σ_f-ord(L,D) )
5      {
6        (
7          ll_out_mda<<f>>><<
8              p_(1,1) ,..., p_(1,D),
9                                ...
10             p_(L,1) ,..., p_(L,D)>>><<b, a>>(
11                 ⇒^1_⊛^MDA( I<<1>><p_(1,1),...,p_(L,1)>(0) ) ,
12                 ⋮
13                 ⇒^D_⊛^MDA( I<<D>><p_(1,D),...,p_(L,D)>(0) ) )
14         )_{b∈[1,B^OB]_ℕ, a∈[1,A_b^OB]_ℕ} := f( ( ll_inp_mda<<f>>><< p_(1,1) ,..., p_(1,D),
15                                                                  ...
16                                                                  p_(L,1) ,..., p_(L,D)>>><<b, a>>(
17                                                      ⇒^d_#^MDA( I<<1>><p_(1,1),...,p_(L,1)>(0) ) ,
18                                                          ⋮
19                                                      ⇒^d_#^MDA( I<<D>><p_(1,D),...,p_(L,D)>(0) ) )
20                                                )_{b∈[1,B^IB]_ℕ, a∈[1,A_b^IB]_ℕ} )
21     }
```

Listing 18. Scalar Phase

E.3 Re-Composition Phase

Listing 19 shows our implementation of the re-composition phase (Figure 19).

```
1  // 3. re-composition phase
2
3    // 3.1. main
4    int p_ σ↑-ord(1,1) ∈< ↔↑-ass (1,1) > #PRT ( σ↑-ord(1,1) )
5    {
6      int p_ σ↑-ord(1,2) ∈< ↔↑-ass (1,2) > #PRT ( σ↑-ord(1,2) )
7      {
8        ⋱
9          int p_ σ↑-ord(L,D) ∈< ↔↑-ass (L,D) > #PRT ( σ↑-ord(L,D) )
10         {
11           ll_out_mda<< σ↑-ord(L,D) >> :=co< σ↑-ord(L,D) > out_mda<<f>>;
12         }
13       ⋰
14       ll_out_mda<< σ↑-ord(1,2) >> :=co< σ↑-ord(1,2) > out_mda<< σ↑-ord(1,3) >>;
15     }
16     ll_out_mda<< σ↑-ord(1,1) >> :=co< σ↑-ord(1,1) > out_mda<< σ↑-ord(1,2) >>;
17   }
18
19   // 3.2. finalization
20   ll_out_mda<<⊥>> := ll_out_mda<< σ↑-ord(1,1) >>
```

Listing 19. Re-Composition Phase

where

$$\texttt{ll\_out\_mda<<}l,d\texttt{>>} :=_{\texttt{co<}l,d\texttt{>}} \texttt{ll\_out\_mda<<}l',d'\texttt{>>}$$

abbreviates

$$\begin{aligned}
&\texttt{ll_out_mda<<}l,d\texttt{>><}\overset{(l,d)}{\blacktriangle}{}^{1}_{1},\ldots,\overset{(l,d)}{\blacktriangle}{}^{L}_{D}\texttt{>}\\
&\texttt{:= co<<d>><}\overset{1}{\underset{\circledast}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}\texttt{(I<< 1 >><}\overset{(l,d)}{\blacksquare}{}^{1}_{1},\ldots,\overset{(l,d)}{\blacksquare}{}^{L}_{1}\texttt{>(0)), // } I_1\\
&\qquad\qquad\vdots \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \texttt{// } \ldots, I_{d-1}, I_{d+1}, \ldots\\
&\qquad\qquad\overset{D}{\underset{\circledast}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}\texttt{(I<<}D\texttt{>><}\overset{(l,d)}{\blacksquare}{}^{1}_{D},\ldots,\overset{(l,d)}{\blacksquare}{}^{L}_{D}\texttt{>(0)), // } I_D\\
&\qquad\qquad\\
&\qquad\qquad\overset{d}{\underset{\circledast}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}\texttt{(I<<}d\texttt{>><}\overset{(l,d)}{\boxplus}{}^{1}_{d},\ldots,\overset{(l,d)}{\boxplus}{}^{L}_{d}\texttt{>(0)), // } P\\
&\qquad\qquad\overset{d}{\underset{\circledast}{\Rightarrow}}{}^{\texttt{MDA}}_{\texttt{MDA}}\texttt{(I<<}d\texttt{>><}\overset{(l,d)}{\boxtimes}{}^{1}_{d},\ldots,\overset{(l,d)}{\boxtimes}{}^{L}_{d}\texttt{>(0)) // } Q\\
&\qquad\texttt{>(ll_out_mda<<}l,d\texttt{>><}\overset{(l,d)}{\blacktriangle}{}^{1}_{1},\ldots,\overset{(l,d)}{\blacktriangle}{}^{L}_{D}\texttt{>,}\\
&\qquad\qquad\texttt{ll_out_mda<<}l',d'\texttt{>><}\overset{(l',d')}{\blacktriangle}{}^{1}_{1},\ldots,\overset{(l',d')}{\blacktriangle}{}^{L}_{D}\texttt{>)}
\end{aligned}$$

Here, functions $\overset{1}{\underset{\circledast}{\Rightarrow}}_{\texttt{MDA}}^{\texttt{MDA}}, \ldots, \overset{D}{\underset{\circledast}{\Rightarrow}}_{\texttt{MDA}}^{\texttt{MDA}}$ are the index set function of combine operators $\circledast_1, \ldots, \circledast_D$ (Definition 2), and $\overset{(\bullet)}{\blacksquare}_{\mathfrak{l}}^{\mathfrak{l}}$, $\overset{(\bullet)}{\boxplus}_{\mathfrak{l}}^{\mathfrak{l}}$, $\overset{(\bullet)}{\boxtimes}_{\mathfrak{l}}^{\mathfrak{l}}$, for $\bullet \in$ MDH-LVL, are textually replaced by:

$$\overset{(\bullet)}{\blacksquare}_{\mathfrak{l}}^{\mathfrak{l}} := \begin{cases} p\_(\mathfrak{l},\mathfrak{d}) & : \ \sigma_{\uparrow\texttt{-ord}}(\mathfrak{l},\mathfrak{d}) < \bullet \\ [0, p\_(\mathfrak{l},\mathfrak{d})]_{\mathbb{N}_0} & : \ (\mathfrak{l},\mathfrak{d}) = \bullet \\ [0, \ \texttt{\#PRT}(\mathfrak{l},\mathfrak{d}) \ )_{\mathbb{N}_0} & : \ \sigma_{\uparrow\texttt{-ord}}(\mathfrak{l},\mathfrak{d}) > \bullet \end{cases}$$

$$\overset{(\bullet)}{\boxplus}_{\mathfrak{l}}^{\mathfrak{l}} := \begin{cases} p\_(\mathfrak{l},\mathfrak{d}) & : \ \sigma_{\uparrow\texttt{-ord}}(\mathfrak{l},\mathfrak{d}) < \bullet \\ [0, p\_(\mathfrak{l},\mathfrak{d}))_{\mathbb{N}_0} & : \ (\mathfrak{l},\mathfrak{d}) = \bullet \\ [0, \ \texttt{\#PRT}(\mathfrak{l},\mathfrak{d}) \ )_{\mathbb{N}_0} & : \ \sigma_{\uparrow\texttt{-ord}}(\mathfrak{l},\mathfrak{d}) > \bullet \end{cases}$$

$$\overset{(\bullet)}{\boxtimes}_{\mathfrak{l}}^{\mathfrak{l}} := \begin{cases} p\_(\mathfrak{l},\mathfrak{d}) & : \ \sigma_{\uparrow\texttt{-ord}}(\mathfrak{l},\mathfrak{d}) < \bullet \\ p\_(\mathfrak{l},\mathfrak{d}) & : \ (\mathfrak{l},\mathfrak{d}) = \bullet \\ [0, \ \texttt{\#PRT}(\mathfrak{l},\mathfrak{d}) \ )_{\mathbb{N}_0} & : \ \sigma_{\uparrow\texttt{-ord}}(\mathfrak{l},\mathfrak{d}) > \bullet \end{cases}$$

where $<$ is defined as lexicographical order, according to Section E.0.4.

Note that we assume for index set functions $\overset{d}{\underset{\circledast}{\Rightarrow}}_{\texttt{MDA}}^{\texttt{MDA}}$ that

$$A \subseteq B \ \Rightarrow \ \overset{d}{\underset{\circledast}{\Rightarrow}}_{\texttt{MDA}}^{\texttt{MDA}}(A) \ \subseteq \ \overset{d}{\underset{\circledast}{\Rightarrow}}_{\texttt{MDA}}^{\texttt{MDA}}(B)$$

(which holds for all kinds of index set functions used in this paper, e.g., in Examples 1 and 2) so that we can re-use `out_mda<<`l,d`>>` for the intermediate results given by different iterations of `p_(l,d)`. MDA `inp_mda<<`l,d`>>` has the following type when used for the intermediate result in a particular iteration of variable `p_(l,d)`:

$$T^{\texttt{INP}}\Big[\overset{1}{\underset{\circledast}{\Rightarrow}}_{\texttt{MDA}}^{\texttt{MDA}}\big(I_1^{\langle \overset{(l,d)_1}{\blacksquare}_1, \ldots, \overset{(l,d)_1}{\blacksquare}_D \mid \ldots \mid \overset{(l,d)_L}{\blacksquare}_1, \ldots, \overset{(l,d)_L}{\blacksquare}_D \rangle} \big) \ , \ \ldots \ , \ \overset{D}{\underset{\circledast}{\Rightarrow}}_{\texttt{MDA}}^{\texttt{MDA}}\big(I_D^{\langle \overset{(l,d)_1}{\blacksquare}_1, \ldots, \overset{(l,d)_1}{\blacksquare}_D \mid \ldots \mid \overset{(l,d)_L}{\blacksquare}_1, \ldots, \overset{(l,d)_L}{\blacksquare}_D \rangle} \big) \Big]$$

Note that in line 11 of Listing 19, we implicitly override the uninitialized value in `out_mda<<l,d>>` (not explicitly stated in the listing for brevity), thereby avoiding initializing output buffers with neutral elements of combine operators.

CODE-LEVEL OPTIMIZATIONS

We consider optimizations that are below the abstraction level of our low-level representation (Section 3) as *code-level optimizations*. For some of these code-level optimizations, like loop fusion, we do not want to rely on the underlying compiler (e.g., the OpenMP/CUDA/OpenCL compiler): we exactly know the structure of our code presented in Section E, thus being able to implement code-level optimizations without requiring complex compiler analyses for optimizations.

Since code-level optimizations are not the focus of this work, we give a brief, basic overview of our these optimizations which our systems performs for the underlying compiler (OpenMP, CUDA,

OpenCL, etc). We will thoroughly discuss our code-level optimizations and how we apply them to our code in future work. Further code-level optimizations, like loop unrolling, are currently mostly left to the underlying compiler, e.g., the OpenMP, CUDA, or OpenCL compiler. In our future work, we aim to incorporate code-level optimizations, such as loop unrolling, into our auto-tunable optimization process.

Loop Fusion. In Listings 17, 18, 19, the lines containing symbol "∈" are mapped to for-loops. These loops can often be fused; for example, when parameters 3, 6, 11 in Table 1 coincide (as in Figure 17). Besides reducing the overhead caused by loop control structures, loop fusion in particular allows significantly reducing the memory footprint: we can re-use the same memory region for each BUF partition (Definition 13), rather than allocating memory for all these partition.

Buffer Elimination. In Listing 15, we allocate BUFs for each combination of a layer and dimension. However, when memory regions and memory layouts of BUFs coincide, we can avoid a new BUF allocation, by re-using the BUF of the upper level, thereby again reducing memory footprint.

Buffer Size Reduction. We can reduce the sizes of BUFs when specific classes of index functions are used for views (Definitions 8 and 10). For example, in the case of *Dot Product (*`DOT`*)* (Figure 16), when accessing its input in a strided fashion – via index function $k \mapsto (2 * k)$, instead of function $k \mapsto (k)$ (as in Figure 16) – we would have to allocate BUFs (Listing 15, lines 30 and 45) of size $2 * K$ for an input size of $K \in \mathbb{N}$; in these BUFs, each second value (accessed via indices $2 * k + 1$) would be undefined. We avoid this waste of memory, by using index function $k \mapsto (k)$ instead of $k \mapsto (2 * k)$ for allocated BUFs (Listing 16, lines 18-20 and 29-31, case "$\bullet \neq \perp$"), which avoids index functions' leading factors and potential constant additions. Thereby, we reduce the memory footprint from $2 * K$ to K. Furthermore, according to our partitioning strategy (Listing 16, line 5, and Listings 17, 18, 19), we often access BUFs via offsets: $k \mapsto (2 * k)$ for $k \in \{OS + k' \mid k' \in \mathbb{N}\}$ and offset $OS \in \mathbb{N}$. We avoid such offset by using $k \mapsto (\ 2 * (k - OS)\ )$, thereby further reducing the memory footprint.

Memory Operation Minimization. In our code, we access BUFs uniformly via MDAs (Listing 16), which may cause unnecessary memory operations. For example, in the de-composition phase (Listing 17) of, e.g., matrix multiplication (`MatMul`) (Figure 16), we iterate over all dimensions of the input (i.e., the i, j, k dimensions) for de-composition (Listing 12). However, the A input matrix of `MatMul` is accessed via MDA indices i and k only (Figure 16). We avoid these unnecessary memory operations (J-many in the case of an input MDA of size J in dimension j) by using index 0 only in dimension j for the de-composition of the A matrix. Analogously, we use index 0 only in the i dimension for the de-composition of `MatMul`'s B matrix which is accessed via MDA indices k and j only. Moreover, we exploit all available parallelism for memory copy operations. For example, for `MatMul`, we use also the threads intended for the j dimension when de-composing the A matrix, and we use the threads in the i dimension for the B matrix. For this, we flatten the thread ids over all dimensions i, j, k and re-structure them only in dimensions i, k (for the A matrix) or k, j (for the B matrix).

Constant Substitution. We use constants whenever possible. For example, in CUDA, variable `threadIdx.x` returns the thread id in dimension x. However, in our code, we use constant `0` instead of `threadIdx.x` when only one thread is started in dimension `x`, enabling the CUDA compiler to significantly simplify arithmetic expressions.