Sigma-Delta Analog to Digital Converter

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Electrical Engineering and Computer Engineering Capstone Design Project 2018-19

Background

Pulse code (or Delta) modulation is a modulation method to encode an analog signal into a 1-bit binary pulse train. It works by encoding the changes or delta between samples instead of the sample itself. The Sigma-Delta ADC uses pulse code modulation in combination with oversampling the input signal, and digital filtering to produce high resolution. The advantage of this ADC is that the oversampling shapes quantization noise into the higher frequencies and then the lowpass digital decimator filter rejects that noise, only looking at the lower frequency bands of interest. Figure 1 below shows the overview of the Sigma-Delta ADC architecture.

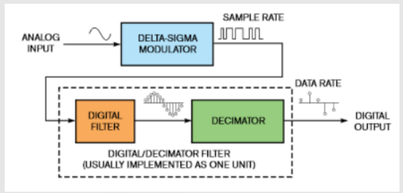

Figure 1: Sigma-Delta ADC Architecture overview

Project Overview

The specifications of this project were to design and implement an 8-bit Sigma-Delta ADC. The ADC was designed with a voltage swing of ± 5V and a maximum signal bandwidth of 40KHz.

To achieve 8 Effective Number Of Bits (ENOB) the Signal to Noise Ratio (SNR) of about 50dB is needed according to the calculation below. Using Figure 2, an SNR of 50dB corresponds to an oversampling ratio of about 32. Using this ratio and the specified maximum signal bandwidth, an oversampling frequency of about 5.2MHz is needed to achieve the desired specifications

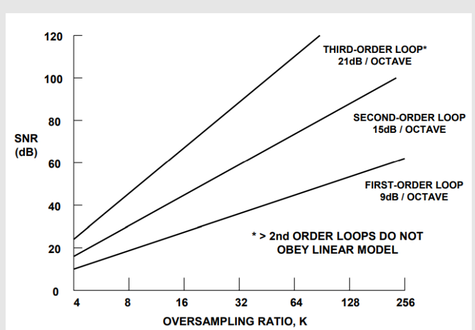

Figure 2: SNR vs Oversampling Ratio

$$ENOB = \frac{SNR - 1.76dB}{6.02dB}$$

System Design

There are two parts to the system design of this project, the analog system and the digital system. The analog system is a second order sigma-delta modulator. It consists of two integrators, a latched comparator that acts as a 1-bit ADC and a CMOS switch that acts as a 1-bit DAC. As seen in Figure 3 below these components are arranged in a feedback topology. The advantage of this topology is that the error signal is filtered. The output of the modulator is fed into a digital system implemented in an FPGA, shown in Figure 4. The digital system does three tasks: 1. Provide a system clock for the analog modulator system, 2. Filter the high frequency noise, 3. Send the filtered signal serially to a host computer.

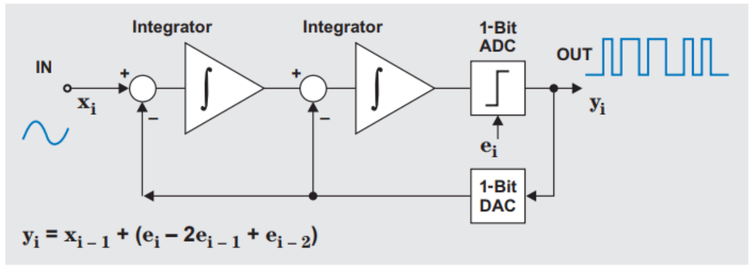

Figure 3: Second Order Sigma-Delta Modulator

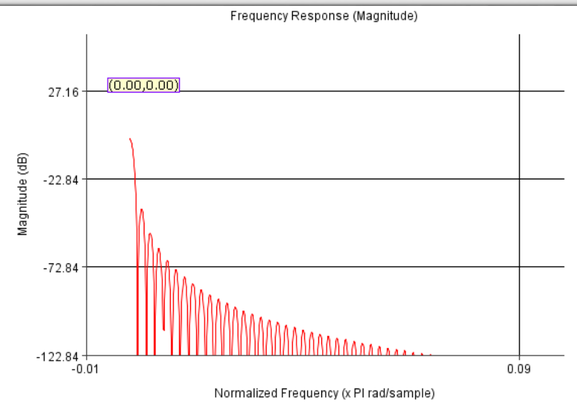

Figure 5: CIC Filter

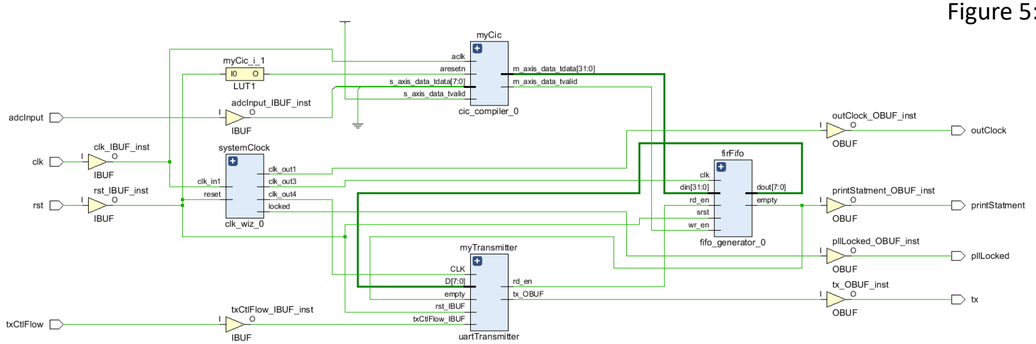

Figure 4: Digital System Implemented in FPGA

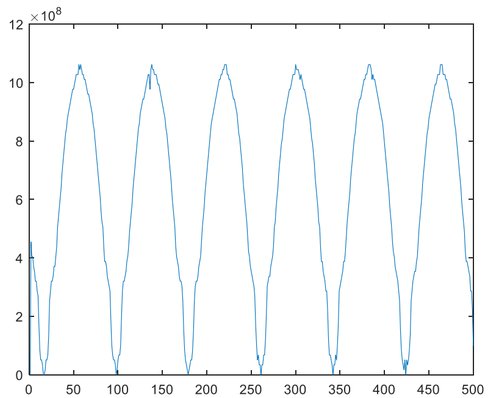

Figure 6: Output of the CIC Filter

Testing & Conclusions

Testing is done by running a MATLAB script to read the data out of the FPGA over UART and plot the data. As seen in Figure 6 above the resultant resolution is very high. This corresponds to an ENOB of about 29.5 bits, outperforming the design specifications. However in testing, the usable signal bandwidth is just below 1KHz. The cause for this is most certainly the digital filtering architecture. Further improvements on the design can be made to achieve better signal usable signal bandwidth . The analog system can be upgraded to a third-order modulator. The digital system can be upgraded with a better filtering architecture as well. One such architecture would be to use multiple digital filters instead of only one. A single Cascaded Integrator-Comb (CIC) filter is used in this design decimate (downsample) the high-speed signal pulse code modulation. Better architectures typically use two to three FIR filters in conjunction with the CIC filter to provide better usable signal bandwidth.