**Department of Computer Science and Engineering**
**University of Barisal**

Course: Computer Architecture | Marks: 50 | Time: 60 Min

Instructor: Dr. Md. Manjur Ahmed

**Question:**

1. Assuming that ENIAC had the capability to have multiple vacuum tubes in the ON and OFF state simultaneously, why is this representation "wasteful" and what range of integer values could we represent using the 20 vacuum tubes? (5 Marks)
2. When a block that is resident in the cache is to be replaced, there are two cases to consider. Describe the write through and write back. (10 Marks)
3. Consider a two-level cache with access time 5 nsec and 80 nsec respectively. If the hit ratio is 95% and 75% respectively in the two caches and main memory access time is 250 nsec. What is the effective access time? (10 Marks)
4. Suppose three interrupt handlers A, B and C (having priority level A>B>C) with Interrupt Service Routine (ISR) 10, 30 and 20 respectively. Graphically show the transfer of control for interrupt sequence of C, A and B at time t=10, 25 and 45 respectively. (10 Marks)
5. Regarding Address Bus, Bus width determines maximum memory capacity of system. For example, 8080 has 16 bit address bus. Then how much memory space it will provide ? (5 Marks)
6. Describe the bottleneck for Cache Design. (10 Marks)

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