Executive Summary

- Master's of Electrical Engineering candidate at the University of Waterloo with a focus on Integrated Circuits
- Has designed and taped out a Mixed Signal IC design (SRAM) on TSMC 65nm
- Grad coursework focused on analog & RF/Microwave circuits, and several related design projects
- Comfortable with scripting languages for EDA design automation, such as SKILL, TCL, and Python
- Previous industry experience in PCB design, and firmware / embedded systems

Education

University of Waterloo

MASc, Electrical Engineering, 2019-Present (Expected December 2020) BASc, Electrical Engineering, 2013-2018

Research

Waterloo CDR Group

Low voltage, offset tolerent SRAM Sense Amplifiers.

Courses & Projects

Advanced Analog Integrated Circuits

OTA, 50uA current reference, 2 stage differential amp with CMFB, switch-cap $2x\ S/H$

RF Integrated Circuits

2GHz differential LNA, on-chip transformer, 900MHz RF to 1MHz IF FET switch mixer, 1.9-2GHz LC Tank VCO (1MHz Phase Noise <-125dBc/Hz)

Nonlinear Microwave/RF Circuits and Devices

Theory & techniques for characterization, design, and simulation of nonlinear circuits. Course project is a diode double balanced mixer for WiFi band (2.4-2.5GHz)

Data Converters

System level design and specification of ADC/DAC, characterization of key specifications (ex: ENOB, DNL, INL, SFDR), over/undersampling, frequency selection

Skills

Analog / Mixed Signal, Digital, RF Integrated Circuits, PCB Design, Firmware Schematic Capture, Layout AMS Simulation, Verification, Monte Carlo TSMC 65nm

Tools

ADS

Cadence Virtuoso, Encounter SoC, Innovus Calibre DRC, LVS, PERX EAGLE, KiCad, DipTrace, Altium

Languages

Python, C/C++, SKILL, MATLAB, TCL, Verilog, VerilogA, VerilogAMS, Bash, Shell scripts

Experience

Graduate Research Assistant Waterloo CDR Group Jan 2019-Present Waterloo, ON

- Design and tapeout of a full custom SRAM block on TSMC 65nm in order to test new sense amplifier ideas, optimizing for 0.4V or lower operation
- Followed a schematic-driven Analog-On-Top flow with Cadence Virtuoso
- Used Verilog and Innovus for block implementation of some digital subcomponents, and top-level integration of the whole chip with other students' work
- Performed simulations with Spectre and VerilogAMS
- \bullet Monte Carlo simulations of V_{th} mismatch, and post-processing data with Python
- Wrote SKILL and TCL scripts to assist with block implementations and top-level integration
- Designing a test rig PCB for the chip using KiCad

Software/Hardware Developer May-Dec 2018 Clear Blue Technologies Toronto, ON

- Designed hardware and software for an automated testing rig that performed black-box testing of load management functionality for the company's core product
- Expanded software infrastructure for automated hardware/firmware QA
- Developed test equipment drivers for use in various QA systems

Staff Hardware Engineer (Intern) Sept-Dec 2017 Nuvation Engineering Waterloo, ON

- Developed a battery discharge model that directed the design of a Megawatt-scale battery pack for a multi-million dollar Energy Storage System (ESS)
- Designed the full ECAD/MCAD solution for a control interface product
- Determined product requirements and captured them in product proposals and hardware description documents (HDD)
- Conducted schematic and PCB layout reviews

Firmware Developer (Intern) Sept-Dec 2016 Cognitive Systems Waterloo, ON

- SDR firmware development in C on a custom DSP vector processor
- Primarily worked on an LTE stack, implementing highly optimized routines that met the ETSI/3GPP LTE specifications
- Contributed significantly to a 67% overall speed improvement of the stack, with individual blocks having up to 200x speed and memory improvements over previous implementations.

Hardware Designer (Intern) Jan-Apr 2016 Ecologix Cambridge, ON

- Circuit design and PCB layout on multiple projects, including a 20kW HVAC system power supply with power factor correction, and an LCD keypad interface board for use in all future products
- Designed circuits, schematic, and PCB layout using EAGLE
- Selected components, sourced components, and minimized design costs
- Tested, debugged, and repaired faulty boards