COEN 313 Lab 2 (UR-X)

by

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"I certify that this submission is my original work and meets the Faculty's Expectations of Originality"

Objective

The main objective of the second lab is to familiarize with structural and concurrent VHDL. Another objective is to learn different VHDL coding styles (concurrent signal assignment and with port maps).

Introduction

To demonstrate understanding of a sum of minterms circuit on the Nexys board, it is required to code the circuit using VHDL. First, an AND-gate, an OR-gate, and a NOT-gate were coded to get the gate components used for port map statements. Using those gates, a sum of minterms VHDL code will be implemented using this function: OUT = A'BC + A'BC + ABC.

The code will then be simulated on the terminal by creating a do file to generate a truth table of the result of the equation. Finally, using the software Vivado, the sum of minterms will be programmed to the Nexys board to be demonstrated.

Here is a truth table of what to be expected for the sum of minterms demonstration on the Nexys board using the LED outputs:

LED outputs Nexys-A7100T	V10	U11	U12	V15
Inputs/outputs	A	B	C	OUT
	0	0	0	0
	0	0	1	1
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	0
	1	1	0	0
	1	1	1	1

Results

Below are the VHDL code of the sum of minterms and the three gates used to implement it.

Not-gate VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;

entity m_not is
port(A : in std_logic ; OUTPUT : out std_logic);
end m_not;

architecture mdk_arch of m_not is
begin
OUTPUT <= (not A);
end mdk_arch;
```

AND-gate VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
entity m_and is
port(A,B,C : in std_logic ; OUTPUT : out std_logic);
end m_and;

architecture mdk_arch of m_and is
begin
OUTPUT <= A and B and C;
end mdk_arch;
```

OR-gate VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
entity m_or is
port(A,B,C : in std_logic ; OUTPUT : out std_logic);
end m_or;

architecture mdk_arch of m_or is
begin
OUTPUT <= A or B or C;
end mdk_arch;
```

Sum of minterms VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;

entity sum_of_minterms is
port( a,b,c           : in std_logic;
      output          : out std_logic);
end sum_of_minterms;

architecture mdk_arch of sum_of_minterms is

-- declare the components found in our entity

component m_not
port(A : in std_logic ; OUTPUT : out std_logic);
end component;

component m_and
port(A,B,C : in std_logic ; OUTPUT : out std_logic);
end component;

component m_or
port(A,B,C : in std_logic ; OUTPUT : out std_logic);
end component;

-- declare signals used to interconnect components

signal s1, s2, s3, s4, s5 : std_logic;


-- declare configuration specification

for U1, U2 : m_not use entity WORK.m_not(mdk_arch);
for U3, U4, U5: m_and use entity WORK.m_and(mdk_arch);
for U6 : m_or use entity WORK.m_or(mdk_arch);

begin

U1 : m_not port map(A => A, OUTPUT => s1 );
U2 : m_not port map(A => B, OUTPUT => s2 );
U3 : m_and port map(A => s1, B => s2, C => C, OUTPUT => s3);
U4 : m_and port map(A => s1, B => B, C => C, OUTPUT => s4);
U5 : m_and port map(A => A, B => B, C => C, OUTPUT => s5);
U6 : m_or port map(A => s3, B => s4, C => s5, OUTPUT => output);

end mdk_arch;
```

Sum of minterms simulation

```
[lyra] [/home/m/ma_kaba/Modelsim/Code] > vsim -c -do ../DO/sum_of_minterms.do sum_of_minterms
Reading /nfs/sw_cmc/x86_64.EL7/tools/mentor.2011/modelsim_6.6g/modeltech/tcl/vsim/pref.tcl

# 6.6g

# vsim -do ../DO/sum_of_minterms.do -c sum_of_minterms
# //  ModelSim SE-64 6.6g May 23 2012 Linux 3.10.0-1160.42.2.el7.x86_64
# //
# //  Copyright 1991-2012 Mentor Graphics Corporation
# //             All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND
# //  PROPRIETARY INFORMATION WHICH IS THE PROPERTY
# //  OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading work.sum_of_minterms(mdk_arch)#1
# Loading work.m_not(mdk_arch)#1
# Loading work.m_and(mdk_arch)#1
# Loading work.m_or(mdk_arch)#1
# do ../DO/sum_of_minterms.do
# 0 0 0 0
# 0 0 1 1
# 0 1 0 0
# 0 1 1 1
# 1 0 0 0
# 1 0 1 0
# 1 1 0 0
# 1 1 1 1
#
#
VSIM 2>
```

To simulate the sum of minterms code, a do file was created to mimic the truth table of the inputs and then show the result of the output. The simulation was executed on the terminal and as we can see above, the output is correct.

Questions

1. Sum of minterms CSA code

```
library IEEE;
use IEEE.std_logic_1164.all;

entity sum_of_minterms is
port( a,b,c           : in std_logic;
      output          : out std_logic);
end sum_of_minterms;

architecture mdk_arch of sum_of_minterms is
        signal signal1, signal2, signal3:std_logic;
begin
        signal1 <= (not a) and (not b) and c;
        signal2 <= (not a) and b and c;
        signal3 <= a and b and c;
        output <= signal1 or signal2 or signal3

end mdk_arch;
```

This code represents the same equation of the sum of minterms using CSA statements instead of port maps.

Sum of minterms CSA simulation

```
[mistral] [/home/m/ma_kaba/Modelsim/Code] > vsim -c -do ../DO/sum_of_minterms.do sum_of_mintermscsa
Reading /nfs/sw_cmc/x86_64.EL7/tools/mentor.2011/modelsim_6.6g/modeltech/tcl/vsim/pref.tcl

# 6.6g

# vsim -do ../DO/sum_of_minterms.do -c sum_of_mintermscsa
# //  ModelSim SE-64 6.6g May 23 2012 Linux 3.10.0-1062.12.1.el7.x86_64
# //
# //  Copyright 1991-2012 Mentor Graphics Corporation
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# //
# //  THIS WORK CONTAINS TRADE SECRET AND
# //  PROPRIETARY INFORMATION WHICH IS THE PROPERTY
# //  OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading work.sum_of_mintermscsa(mdk_arch)#1
# do ../DO/sum_of_minterms.do
# 0 0 0 0
# 0 0 1 1
# 0 1 0 0
# 0 1 1 1
# 1 0 0 0
# 1 0 1 0
# 1 1 0 0
# 1 1 1 1
#
#
VSIM 2>
```

The simulation of the CSA statements of the sum of minterms shows a perfect simulation of the output

2. The hardware that would result is a buffer because the inverse of input_1 is stored in first. Then, the inverse of first is stored in second. Which is assigned as output. Therefore, the output is nothing but the same signal input_1.

Conclusion

To conclude, this second lab offered good learning of structural and concurrent VHDL. It provided a meaningful exercise on different VHDL coding styles (concurrent signal assignment and port maps) and familiarization of combinational logic minimization performed by logic synthesis tools.

Appendix

Sum_of_minterms.do

```
force a 0
force b 0
force c 0
run 2
examine a b c output
force a 0
force b 0
force c 1
run 2
examine a b c output
force a 0
force b 1
force c 0
run 2
examine a b c output
force a 0
force b 1
force c 1
run 2
examine a b c output
force a 1
force b 0
force c 0
run 2
examine a b c output
force a 1
force b 0
force c 1
run 2
examine a b c output
force a 1
force b 1
force c 0
run 2
examine a b c output
force a 1
force b 1
force c 1
run 2
examine a b c output
```

Sum_of_minterms.xdc

```
# Vivado does not support old UCF syntax
# must use XDC syntax

set_property -dict { PACKAGE_PIN V10 IOSTANDARD LVCMOS33 } [ get_ports { a }];
set_property -dict { PACKAGE_PIN V11 IOSTANDARD LVCMOS33 } [ get_ports { b }   ] ;
set_property -dict { PACKAGE_PIN U12 IOSTANDARD LVCMOS33 } [ get_ports { c }  ] ;
set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 } [ get_ports { output } ] ;
```

Sum_of_minterms.tcl

```
# TCL script for running vivado in batch mode to synthesize sum_of_minterms.vhd
# Mamadou Kaba
# February 16, 2022

# To run the script first source the Vivado env file:
# source /CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/settings64_CMC_central_license.c

#
#Then issue the following command from the Linux prompt:
# vivado -log sum_of_minterms.log -mode batch -source tedcircuit_script.tcl

# read in the VHDL source code files and the xdc constraints file

read_vhdl  { ../Code/m_not.vhd  ../Code/m_and.vhd ../Code/m_or.vhd ../Code/sum_of_minterms.vhd }
read_xdc sum_of_minterms.xdc

# the -top refers to the top level VHDL entity name
# the -part specfies the target Xilinx FPGA
synth_design -top sum_of_minterms -part xc7a100tcsg324-1

opt_design
place_design
route_design

report_timing_summary

# generate the bitsteam file
write_bitstream -force sum_of_minterms.bit
```

Sum_of_minterms.log

```
#-----------------------------------------------------------
# Vivado v2018.2 (64-bit)
# SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
# IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
# Start of session at: Tue Mar  8 14:56:29 2022
# Process ID: 10345
# Current directory: /nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT
# Command line: vivado -log sum_of_minterms.log -mode batch -source
sum_of_minterms.tcl
# Log file:
/nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT/sum_of_minterms.log
# Journal file:
/nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT/vivado.jou
#-----------------------------------------------------------
source sum_of_minterms.tcl
# read_vhdl  { ../Code/m_not.vhd  ../Code/m_and.vhd ../Code/m_or.vhd
../Code/sum_of_minterms.vhd }
# read_xdc sum_of_minterms.xdc
# synth_design -top sum_of_minterms -part xc7a100tcsg324-1
Command: synth_design -top sum_of_minterms -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 10415
---------------------------------------------------------------------------
-------
Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 .
Memory (MB): peak = 1401.078 ; gain = 85.805 ; free physical = 11713 ;
free virtual = 23525
---------------------------------------------------------------------------
-------
INFO: [Synth 8-638] synthesizing module 'sum_of_minterms'
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:8]
INFO: [Synth 8-3491] module 'm_not' declared at
'/nfs/home/m/ma_kaba/Modelsim/Code/m_not.vhd:4' bound to instance 'U1' of
component 'm_not'
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:37]
INFO: [Synth 8-638] synthesizing module 'm_not'
[/nfs/home/m/ma_kaba/Modelsim/Code/m_not.vhd:8]
INFO: [Synth 8-256] done synthesizing module 'm_not' (1#1)
[/nfs/home/m/ma_kaba/Modelsim/Code/m_not.vhd:8]
INFO: [Synth 8-3491] module 'm_not' declared at
'/nfs/home/m/ma_kaba/Modelsim/Code/m_not.vhd:4' bound to instance 'U2' of
component 'm_not'
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:38]
INFO: [Synth 8-3491] module 'm_and' declared at
'/nfs/home/m/ma_kaba/Modelsim/Code/m_and.vhd:3' bound to instance 'U3' of
component 'm_and'
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:39]
INFO: [Synth 8-638] synthesizing module 'm_and'
[/nfs/home/m/ma_kaba/Modelsim/Code/m_and.vhd:7]
INFO: [Synth 8-256] done synthesizing module 'm_and' (2#1)
[/nfs/home/m/ma_kaba/Modelsim/Code/m_and.vhd:7]
INFO: [Synth 8-3491] module 'm_and' declared at
'/nfs/home/m/ma_kaba/Modelsim/Code/m_and.vhd:3' bound to instance 'U4' of
```

```
component 'm_and'
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:40]
INFO: [Synth 8-3491] module 'm_and' declared at
'/nfs/home/m/ma_kaba/Modelsim/Code/m_and.vhd:3' bound to instance 'U5' of
component 'm_and'
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:41]
INFO: [Synth 8-3491] module 'm_or' declared at
'/nfs/home/m/ma_kaba/Modelsim/Code/m_or.vhd:3' bound to instance 'U6' of
component 'm_or'
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:42]
INFO: [Synth 8-638] synthesizing module 'm_or'
[/nfs/home/m/ma_kaba/Modelsim/Code/m_or.vhd:7]
INFO: [Synth 8-256] done synthesizing module 'm_or' (3#1)
[/nfs/home/m/ma_kaba/Modelsim/Code/m_or.vhd:7]
INFO: [Synth 8-256] done synthesizing module 'sum_of_minterms' (4#1)
[/nfs/home/m/ma_kaba/Modelsim/Code/sum_of_minterms.vhd:8]
---------------------------------------------------------------------------
-------
Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 .
Memory (MB): peak = 1445.719 ; gain = 130.445 ; free physical = 11724 ;
free virtual = 23538
---------------------------------------------------------------------------
-------
Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------
-------
Start Handling Custom Attributes
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed =
00:00:05 . Memory (MB): peak = 1445.719 ; gain = 130.445 ; free physical =
11724 ; free virtual = 23538
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed =
00:00:05 . Memory (MB): peak = 1445.719 ; gain = 130.445 ; free physical =
11724 ; free virtual = 23538
---------------------------------------------------------------------------
-------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Processing XDC Constraints
Initializing timing engine
Parsing XDC File
[/nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT/sum_of_minterms.xdc]
Finished Parsing XDC File
[/nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT/sum_of_minterms.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while
reading constraint file
[/nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT/sum_of_minterms.xdc].
These constraints will be ignored for synthesis but will be used in
```

```
implementation. Impacted constraints are listed in the file
[.Xil/sum_of_minterms_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in
[.Xil/sum_of_minterms_propImpl.xdc] to another XDC file and exclude this
new file from synthesis with the used_in_synthesis property (File
Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed =
00:00:00 . Memory (MB): peak = 1797.469 ; gain = 0.000 ; free physical =
11385 ; free virtual = 23231
-------------------------------------------------------------------------
-------
Finished Constraint Validation : Time (s): cpu = 00:00:12 ; elapsed =
00:00:46 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11504 ; free virtual = 23350
-------------------------------------------------------------------------
-------
-------------------------------------------------------------------------
-------
Start Loading Part and Timing Information
-------------------------------------------------------------------------
-------
Loading part: xc7a100tcsg324-1
-------------------------------------------------------------------------
-------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:12 ;
elapsed = 00:00:46 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free
physical = 11504 ; free virtual = 23350
-------------------------------------------------------------------------
-------
-------------------------------------------------------------------------
-------
Start Applying 'set_property' XDC Constraints
-------------------------------------------------------------------------
-------
-------------------------------------------------------------------------
-------
Finished applying 'set_property' XDC Constraints : Time (s): cpu =
00:00:12 ; elapsed = 00:00:46 . Memory (MB): peak = 1797.469 ; gain =
482.195 ; free physical = 11504 ; free virtual = 23350
-------------------------------------------------------------------------
-------
-------------------------------------------------------------------------
-------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:12 ; elapsed =
00:00:46 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11504 ; free virtual = 23351
-------------------------------------------------------------------------
-------
Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------
-------
Start RTL Component Statistics
```

```
---------------------------------------------------------------------------
-------
Detailed RTL Component Info :
---------------------------------------------------------------------------
-------
Finished RTL Component Statistics
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------
-------
Hierarchical RTL Component report
---------------------------------------------------------------------------
-------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start Part Resource Summary
---------------------------------------------------------------------------
-------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------
-------
Finished Part Resource Summary
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------
-------
Warning: Parallel synthesis criteria is not met
---------------------------------------------------------------------------
-------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:13 ;
elapsed = 00:00:47 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free
physical = 11494 ; free virtual = 23341
---------------------------------------------------------------------------
-------
Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
-------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:18 ;
elapsed = 00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free
physical = 11366 ; free virtual = 23221
```

```
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start Timing Optimization
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Timing Optimization : Time (s): cpu = 00:00:18 ; elapsed =
00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11366 ; free virtual = 23221
---------------------------------------------------------------------------
-------
Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
-------
Start Technology Mapping
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Technology Mapping : Time (s): cpu = 00:00:18 ; elapsed =
00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11366 ; free virtual = 23221
---------------------------------------------------------------------------
-------
Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
-------
Start IO Insertion
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start Final Netlist Cleanup
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Final Netlist Cleanup
```

```
-------------------------------------------------------------------------------
-------
-------------------------------------------------------------------------------
-------
Finished IO Insertion : Time (s): cpu = 00:00:18 ; elapsed = 00:00:59 .
Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical = 11366 ;
free virtual = 23221
-------------------------------------------------------------------------------
-------
Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
-------------------------------------------------------------------------------
-------
Start Renaming Generated Instances
-------------------------------------------------------------------------------
-------
-------------------------------------------------------------------------------
-------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:18 ; elapsed
= 00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical
= 11366 ; free virtual = 23221
-------------------------------------------------------------------------------
-------
Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
-------
Start Rebuilding User Hierarchy
-------------------------------------------------------------------------------
-------
-------------------------------------------------------------------------------
-------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:18 ; elapsed =
00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11366 ; free virtual = 23221
-------------------------------------------------------------------------------
-------
-------------------------------------------------------------------------------
-------
Start Renaming Generated Ports
-------------------------------------------------------------------------------
-------
-------------------------------------------------------------------------------
-------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:18 ; elapsed =
00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11366 ; free virtual = 23221
-------------------------------------------------------------------------------
-------
-------------------------------------------------------------------------------
-------
Start Handling Custom Attributes
```

```
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:18 ; elapsed =
00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11366 ; free virtual = 23221
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start Renaming Generated Nets
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:18 ; elapsed =
00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11366 ; free virtual = 23221
---------------------------------------------------------------------------
-------
---------------------------------------------------------------------------
-------
Start Writing Synthesis Report
---------------------------------------------------------------------------
-------
Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+
Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |IBUF |     3|
|3     |OBUF |     1|
+------+-----+------+
Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     5|
|2     |  U6     |m_or   |     1|
+------+---------+-------+------+
---------------------------------------------------------------------------
-------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed =
00:00:59 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11366 ; free virtual = 23221
---------------------------------------------------------------------------
-------
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:10 ; elapsed =
00:00:22 . Memory (MB): peak = 1797.469 ; gain = 130.445 ; free physical =
11421 ; free virtual = 23276
Synthesis Optimization Complete : Time (s): cpu = 00:00:18 ; elapsed =
00:01:00 . Memory (MB): peak = 1797.469 ; gain = 482.195 ; free physical =
11432 ; free virtual = 23286
```

```
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 3 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File
[/nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT/sum_of_minterms.xdc]
Finished Parsing XDC File
[/nfs/home/m/ma_kaba/Modelsim/SUM_OF_MINTERMS_SCRIPT/sum_of_minterms.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
INFO: [Common 17-83] Releasing license: Synthesis
26 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:20 ; elapsed = 00:01:01 . Memory (MB):
peak = 1797.469 ; gain = 494.844 ; free physical = 11409 ; free virtual =
23264
# opt_design
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or
device 'xc7a100t'
Running DRC as a precondition to command opt_design
Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more
information.
Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.37 . Memory (MB): peak =
1820.477 ; gain = 23.008 ; free physical = 11410 ; free virtual = 23265
Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 1ab97e180
Time (s): cpu = 00:00:07 ; elapsed = 00:00:33 . Memory (MB): peak =
2116.672 ; gain = 296.195 ; free physical = 11063 ; free virtual = 22939
Starting Logic Optimization Task
Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 1ab97e180
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells
Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 1ab97e180
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed
0 cells
Phase 3 Sweep
Phase 3 Sweep | Checksum: 1ab97e180
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells
Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 1ab97e180
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
```

```
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are
BUFGs and removed 0 cells.
Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 1ab97e180
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and
removed 0 cells
Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 1ab97e180
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and
removed 0 cells
Starting Connectivity Check Task
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
Ending Logic Optimization Task | Checksum: 1ab97e180
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period <
2.00 ns.
Ending Power Optimization Task | Checksum: 1ab97e180
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 1ab97e180
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak =
2116.672 ; gain = 0.000 ; free physical = 11079 ; free virtual = 22954
INFO: [Common 17-83] Releasing license: Implementation
16 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:33 . Memory (MB):
peak = 2116.672 ; gain = 319.203 ; free physical = 11079 ; free virtual =
22954
# place_design
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or
device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for
more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for
more information.
Starting Placer Task
INFO: [Place 30-611] Multithreading enabled for place_design using a
maximum of 8 CPUs
Phase 1 Placer Initialization
Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 .
Memory (MB): peak = 2180.703 ; gain = 0.000 ; free physical = 11076 ; free
virtual = 22952
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 12e9560db
```

```
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak =
2180.703 ; gain = 0.000 ; free physical = 11076 ; free virtual = 22952
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 .
Memory (MB): peak = 2180.703 ; gain = 0.000 ; free physical = 11076 ; free
virtual = 22952
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum:
12e9560db
Time (s): cpu = 00:00:00.50 ; elapsed = 00:00:00.39 . Memory (MB): peak =
2204.715 ; gain = 24.012 ; free physical = 11073 ; free virtual = 22948
Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 1f7110ab3
Time (s): cpu = 00:00:00.55 ; elapsed = 00:00:00.41 . Memory (MB): peak =
2204.715 ; gain = 24.012 ; free physical = 11073 ; free virtual = 22948
Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 1f7110ab3
Time (s): cpu = 00:00:00.56 ; elapsed = 00:00:00.42 . Memory (MB): peak =
2204.715 ; gain = 24.012 ; free physical = 11073 ; free virtual = 22948
Phase 1 Placer Initialization | Checksum: 1f7110ab3
Time (s): cpu = 00:00:00.56 ; elapsed = 00:00:00.42 . Memory (MB): peak =
2204.715 ; gain = 24.012 ; free physical = 11073 ; free virtual = 22948
Phase 2 Global Placement
Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 1f7110ab3
Time (s): cpu = 00:00:00.59 ; elapsed = 00:00:00.43 . Memory (MB): peak =
2204.715 ; gain = 24.012 ; free physical = 11071 ; free virtual = 22946
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical
synthesis in placer
Phase 2 Global Placement | Checksum: 2177059ed
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.57 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11057 ; free virtual = 22932
Phase 3 Detail Placement
Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 2177059ed
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.57 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11057 ; free virtual = 22933
Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 167e786c5
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.59 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11058 ; free virtual = 22933
Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 2177059ed
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.60 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11059 ; free virtual = 22934
Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 2177059ed
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.60 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11059 ; free virtual = 22934
Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.94 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.94 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 10caf6c3b
```

```
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.94 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 3 Detail Placement | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.94 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 4 Post Placement Optimization and Clean-Up
Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.94 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.95 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.95 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.95 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 10caf6c3b
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.95 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11052 ; free virtual = 22927
Ending Placer Task | Checksum: d9e33483
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.96 . Memory (MB): peak =
2316.766 ; gain = 136.062 ; free physical = 11070 ; free virtual = 22945
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
# route_design
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or
device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for
more information.
Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a
maximum of 8 CPUs
Checksum: PlaceDB: 66236874 ConstDB: 0 ShapeSum: 73bfcc0f RouteDB: 0
Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: a1653d08
Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak =
2375.773 ; gain = 59.008 ; free physical = 10916 ; free virtual = 22791
Post Restoration Checksum: NetGraph: 66f884e7 NumContArr: 3a6cb821
Constraints: 0 Timing: 0
Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will
operate in resource-optimization mode.
Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: a1653d08
Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak =
2381.762 ; gain = 64.996 ; free physical = 10884 ; free virtual = 22759
Phase 2.2 Pre Route Cleanup
```

```
Phase 2.2 Pre Route Cleanup | Checksum: a1653d08
Time (s): cpu = 00:00:17 ; elapsed = 00:00:14 . Memory (MB): peak =
2381.762 ; gain = 64.996 ; free physical = 10884 ; free virtual = 22759
Phase 2 Router Initialization | Checksum: a1653d08
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10880 ; free virtual = 22756
Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: fad1fef8
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10879 ; free virtual = 22754
Phase 4 Rip-up And Reroute
Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: cd373753
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10879 ; free virtual = 22754
Phase 4 Rip-up And Reroute | Checksum: cd373753
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10879 ; free virtual = 22754
Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: cd373753
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10879 ; free virtual = 22754
Phase 6 Post Hold Fix
Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: cd373753
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10879 ; free virtual = 22754
Phase 6 Post Hold Fix | Checksum: cd373753
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10879 ; free virtual = 22754
Phase 7 Route finalize
Router Utilization Summary
  Global Vertical Routing Utilization    = 0.000565783 %
  Global Horizontal Routing Utilization  = 0.000639386 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets                  = 0
  Number of Unrouted Nets                = 0
  Number of Partially Routed Nets        = 0
  Number of Node Overlaps                = 0
Congestion Report
North Dir 1x1 Area, Max Cong = 0.900901%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 5.40541%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.
------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
```

```
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Phase 7 Route finalize | Checksum: cd373753
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2389.027 ; gain = 72.262 ; free physical = 10878 ; free virtual = 22754
Phase 8 Verifying routed nets
 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: cd373753
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2392.027 ; gain = 75.262 ; free physical = 10877 ; free virtual = 22752
Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 17bd8e52f
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2392.027 ; gain = 75.262 ; free physical = 10877 ; free virtual = 22752
INFO: [Route 35-16] Router Completed Successfully
Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak =
2392.027 ; gain = 75.262 ; free physical = 10911 ; free virtual = 22786
Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
8 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:19 ; elapsed = 00:00:15 . Memory (MB):
peak = 2392.031 ; gain = 75.266 ; free physical = 10911 ; free virtual =
22786
# report_timing_summary
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type:
min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a
maximum of 8 CPUs
Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
------------------------------------------------------------------------
------------------------
| Tool Version : Vivado v.2018.2 (lin64) Build 2258646 Thu Jun 14 20:02:38
MDT 2018
| Date         : Tue Mar  8 14:59:14 2022
| Host         : mistral.encs.concordia.ca running 64-bit Scientific Linux
release 7.7 (Nitrogen)
| Command      : report_timing_summary
| Design       : sum_of_minterms
| Device       : 7a100t-csg324
| Speed File   : -1  PRODUCTION 1.22 2018-03-21
------------------------------------------------------------------------
------------------------
Timing Summary Report
------------------------------------------------------------------------
----------------------
| Timer Settings
| --------------
------------------------------------------------------------------------
----------------------
  Enable Multi Corner Analysis               :  Yes
  Enable Pessimism Removal                   :  Yes
  Pessimism Removal Resolution               :  Nearest Common Node
  Enable Input Delay Default Clock           :  No
  Enable Preset / Clear Arcs                 :  No
  Disable Flight Delays                      :  No
```

```
  Ignore I/O Paths                            :  No
  Timing Early Launch at Borrowing Latches    :  false
  Corner  Analyze    Analyze
  Name    Max Paths  Min Paths
  ------  ---------  ---------
  Slow    Yes        Yes
  Fast    Yes        Yes
check_timing report
Table of Contents
-----------------
1. checking no_clock
2. checking constant_clock
3. checking pulse_width_clock
4. checking unconstrained_internal_endpoints
5. checking no_input_delay
6. checking no_output_delay
7. checking multiple_clock
8. checking generated_clocks
9. checking loops
10. checking partial_input_delay
11. checking partial_output_delay
12. checking latch_loops
1. checking no_clock
--------------------
 There are 0 register/latch pins with no clock.
2. checking constant_clock
--------------------------
 There are 0 register/latch pins with constant_clock.
3. checking pulse_width_clock
-----------------------------
 There are 0 register/latch pins which need pulse_width check
4. checking unconstrained_internal_endpoints
--------------------------------------------
 There are 0 pins that are not constrained for maximum delay.
 There are 0 pins that are not constrained for maximum delay due to
constant clock.
5. checking no_input_delay
--------------------------
 There are 0 input ports with no input delay specified.
 There are 0 input ports with no input delay but user has a false path
constraint.
6. checking no_output_delay
---------------------------
 There are 0 ports with no output delay specified.
 There are 0 ports with no output delay but user has a false path
constraint
 There are 0 ports with no output delay but with a timing clock defined on
it or propagating through it
7. checking multiple_clock
--------------------------
 There are 0 register/latch pins with multiple clocks.
8. checking generated_clocks
----------------------------
 There are 0 generated clocks that are not connected to a clock source.
9. checking loops
-----------------
 There are 0 combinational loops in the design.
10. checking partial_input_delay
--------------------------------
 There are 0 input ports with partial input delay specified.
```

```
11. checking partial_output_delay
---------------------------------
 There are 0 ports with partial output delay specified.
12. checking latch_loops
------------------------
 There are 0 combinational latch loops in the design through latch input
------------------------------------------------------------------------------
----------------------
| Design Timing Summary
| ---------------------
------------------------------------------------------------------------------
----------------------
    WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total Endpoints
WHS(ns)      THS(ns)  THS Failing Endpoints  THS Total Endpoints
WPWS(ns)     TPWS(ns)  TPWS Failing Endpoints  TPWS Total Endpoints
    -------      -------  --------------------  -------------------
-------      -------  --------------------  -------------------     -----
---     --------  ----------------------  --------------------

         NA           NA                      NA                    NA
NA           NA                     NA                   NA           NA
NA                       NA                     NA
There are no user specified timing constraints.
------------------------------------------------------------------------------
----------------------
| Clock Summary
| -------------
------------------------------------------------------------------------------
----------------------
------------------------------------------------------------------------------
----------------------
| Intra Clock Table
| -----------------
------------------------------------------------------------------------------
----------------------
Clock             WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total
Endpoints      WHS(ns)      THS(ns)  THS Failing Endpoints  THS Total
Endpoints     WPWS(ns)     TPWS(ns)  TPWS Failing Endpoints  TPWS Total
Endpoints
-----             -------      -------  --------------------  -----------
--------      -------      -------  --------------------  ---------------
----     --------     --------  ----------------------  -------------------
--
------------------------------------------------------------------------------
----------------------
| Inter Clock Table
| -----------------
------------------------------------------------------------------------------
----------------------
From Clock    To Clock          WNS(ns)      TNS(ns)  TNS Failing
Endpoints  TNS Total Endpoints      WHS(ns)      THS(ns)  THS Failing
Endpoints  THS Total Endpoints
----------    --------          -------      -------  --------------------
-  -------------------      -------      -------  --------------------  -
------------------
------------------------------------------------------------------------------
----------------------
| Other Path Groups Table
| -----------------------
------------------------------------------------------------------------------
----------------------
```

```
Path Group    From Clock    To Clock          WNS(ns)      TNS(ns)  TNS
Failing Endpoints  TNS Total Endpoints      WHS(ns)      THS(ns)  THS
Failing Endpoints  THS Total Endpoints
----------    ----------    --------          -------      -------  ------
--------------  --------------------      -------      -------  ----------
----------  --------------------
------------------------------------------------------------------------------
----------------------
| Timing Details
| --------------
------------------------------------------------------------------------------
----------------------
# write_bitstream -force sum_of_minterms.bit
Command: write_bitstream -force sum_of_minterms.bit
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or
device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design
Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set
in the current_design.  Configuration bank voltage select (CFGBVS) must be
set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct
configuration voltage, in order to determine the I/O voltage support for
the pins in bank 0.  It is suggested to specify these either using the
'Edit Device Properties' function in the GUI or directly in the XDC file
using the following syntax:
 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND
 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0
Refer to the device configuration user guide for more information.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for
more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./sum_of_minterms.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:13 . Memory
(MB): peak = 2743.852 ; gain = 351.820 ; free physical = 10852 ; free
virtual = 22747
INFO: [Common 17-206] Exiting Vivado at Tue Mar  8 14:59:27 2022...
```