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ARM7 Introduction

(ARM7 tdmi version)

1) 32 bit MC

It is a 32 bit microcontroller. It is 8-times powerful than 8051. 8051 does 8-bit operation in one ~~co~~ cycle. ARM ~~does~~ does 32-bit operation in one cycle.

•) 32 Bit ALU

Means it does 32-bit operation in one cycle.

•) 32 bit data bus

3	2	1	0	00 00
7	6	5	4	01 00
B	A	9	8	10 00
F	E	D	C	11 00
:	:	:	:	

we have learnt aligned data and misaligned data in 8086. 8086 has 16-bit data.

It can transfer 16-bit in one cycle but the location must be aligned.

If the locations (two location, one location is 8 bit) is misaligned it requires two cycle.

2,3 } first even address }
4,5 } second odd address } ↓
8,9 }
~~ad~~ aligned data.

1,2 } misaligned data.
3,4 }

8086 supports aligned and misaligned data transfers. ~~beck~~ because of ~~flexible~~ flexibility.

ARM is a performance based controller/processors. It does not support misaligned data.

flexibility ~~gi~~ makes ~~less~~ reduce performance rigidity gets high performance.

Because of rigidity in ARM it gives tremendously high performance.

It (ARM) can transfer 32 bit data in one cycle.

The ~~eta~~ four consequtive locations must be aligned.

The first location (of four) must be start wit '0' or '4' or '8' or 'C'. (left one)

there is common between them.

two bit of 0,4,8,C ~~is~~ are zero.

0 → 00 | 00
4 → 01 | 00
8 → 10 | 00
C → 11 | 00

•) 32 bit Instrs. (RISC char)

ARM stands for (Advanced risc Machine)

RISC stands for ('Reduced Instruction set computer')

8086, 8085, 8051 are CISC processors.

ARM7 is a ~~[illegible]~~ RISC processor.

CISC processors give flexibility.

RISC processors give performance.

Benefits of RISC in ARM7

all the instructions in ARM is 32 bit.

Every instructions are fetched in one cycle. and ~~a~~ instructions are in aligned from.

•) 32 bit address bus

$\therefore 2^{32} = 4GB$ Mem $\boxed{\begin{matrix}\text{Prog}\\+\\\text{Mem}\end{matrix}} \to 4GB$

It has 32 bit address bus. it allows 4GB of memory to use to keep program or data.

•) Von Neuman Model (Common Mem - Prog and Data)

ARM is based on Von Neuman Model.

There are two models in which processors are managed.

→ Von Neuman Model.

→ ~~Hard~~ Harvard Model.

Von Neuman Model says there will be only one Memory for storing both ~~Memor~~ program and data. ARM is based on it.

According to Harvard Model there will be two memory for storing program and data separately.

8051 is based on Harvard Model.

it has 64KB Mem for program (ROM)
64 KB Mem for data (RAM)

·) 3 stage pipeline

- → F
- → D
- → E

8086 has two stage pipelining.

Pipelining means divide the process of instructions into independent sections and overlapping them

3stage pipelining

first instruct fetched.
then decode.
while first is decoding the second will be fetched.
After it.
first ~~we~~ will ~~exceding~~ executing,
at the time second is decoding,
at the same time the third one will be fetching.

it continues for further all the instructions.

So when one instruction is executing, the next one will be decoding and the next next one

will be fetching.
This is the three stage pipeling.

The operation occurs like

F → D → E → E → E → E → . .

RISC processing gives actual performance & ~~pipeling~~ pipelining.

In The ~~CI~~ CISC processors ~~pip~~ sometimes pipelining breaks for several reason.

a) 32
37 regs - 32 bits each
16 available at a time
(R0 to R15)

CISC processors are based on memory, there are few no. of registers in 8086 there 16 bit 4 registers (AX, BX, CX and DX). or 8 reg of 8 bit (AL, AH, . . DL, DH)

RISC processors are based on registers. In ARM there are 37 registers. Every register is 32 bit.
16 registers are available at a time.
(R0 to R15)

we can use all the 37 registers in different mode modes.

•) Load-Store Model

CISC processors ~~to~~ perform operation ~~at~~ Both in registers and memory. Ex: 8086.

But in ARM all operations are done through registers. Only two instructions are done on Memory.

1. Load (receive) the instr/data from the memory.

2. Store the data to the memory.

That's why it is called Load Store Model. Because of this type of rigidity it gives the high performance.

"All the mobile phones ~~are~~ processors are based on ARM."

All arithmatic, logic operations are done through registers.

•) 7 operating Modes   # It ~~is~~ has seven operating modes.

1. ~~Superviseda~~ Supervisor
2. User (99% of time ~~this~~ this mode is being used)
3. System
4. FIQ
5. IRQ
6. Undefined
7. Abott

•) 7 Interrupts / ~~exec~~ exceptions   # 7 interrupts are from 5 modes.

User mode and system mode donot need any interrupt.

1. Reset
2. Undefined
3. Prefetch abott
4. Data abott
5. Software interrupt
6. IRQ
7. FIQ.

Interrupts are also called ~~interru~~ exceptions.

•) 7 addressing Modes

It has seven addressing modes

1. Immediate
2. ~~Rigid~~ Register
3. Direct
4. Registero indirect
5. Register Relative
6. Based inbxed
7. Based with scaled index

•) 3 data formats (8, 16, 32 bit)

It supports 3 types of data format.

It work on 8 bit, 16 bit and 32 bit numbers.

8 bit = 1 byte

16 bit = half word

32 bit = word

Byte is universal size = 8 bit.

As ARM 32 processoro.

So, 1 WORD = 32 bit.

$\frac{1}{2}$ WORD = 16 bit.