ARM7 CPSR - Flag Register

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CPSR flag register of ARM
Current Program Status Register (CPSR)

ARM7 - CPSR (Flag Register)

N	Z	C	V	...	I	F	T	Mode

C: 'C' is the carry flag.
when there is carry, it becomes 1.
" " no carry it becomes 0.

Z: is like zero flag.
when the result is zero it, Z = 1
when the " ≠ 0, Z = 0.

V: 'V' is an overflow flag.

when the value is out of range for sign bit numbers.
it becomes 1. otherwise it remains 0.

For example, for 8 bit sign bit number.

the range is:

8 bit singed NO.
-80 . . +7F

Example-1:

```
 +42     0100 0010
 +43     0100 0011
 ---     ---------
 +85     1000 0011
         ---------
         LDO-  V = 1
               N = 0
```

here the value is out of range.
that means there occurs an overflow.

But the msb of the sign bit of the result is negative.

when when there occurs an overflow, ~~there result~~ the sign bit of the result shows the wrong value.

N: 'N' is the sign flag like in Intel.

In Intel if SF (sign flag) shows the MSB of the result.

That means if there is an overflow,

SF=0 → the number is negative } shows the opposite one of result.
SF=1 → the number is positive }
(example-1)

If there is no overflow

SF=0 → positive result } correct to result.
SF=1 → negative result }
(example-2)

Example-2

+23H	0010	0011
+31H	0011	0001
54	0101	0100

→ V=0
N=0

But in ARM processors 'N' bit always gives the correct answer.

if N=0 -> the result is positive
; N=1 -> the result is negative.

If there is no overflow
N gives the same value of MSB.
If there occurs overflow N
gives the opposite of MSB of
the result.
Hence N shows always sign of
the result.

IRQ, FIQ:

IRQ is the normal interrupt.
In this interrupt when this interrupt
occurs the result of the current
program ~~status~~ stores some location.
and go to the interrupt. Because
when ~~the~~ it will back to the
main program, it could restore the
results of /status of the main
program.

FIQ is the fast interrupt.
When this interrupt occurs rather than storing the results, the processor uses the new set of registers to operator to respond the interrupt.

I bit
'I' is used to disable IRQ (normal interrupt)

F bit
'F' is used to disable FIQ (Fast interrupt)

when I, F = 0 => interrupt enabled.
I, f = 1 => interrupt disabled.

The default value of I and f is 1.

(I and f flags are opposite of interrupt flags in Intel.)

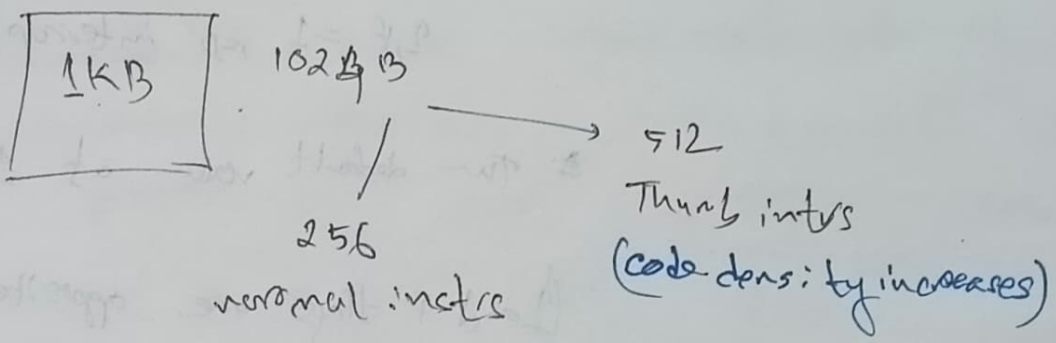
T bit
In ARM7 there are two states two we to operate the procesor in it.
1. Normal state.
2. Thumb state.

In normal state the instructions are 32 bit. In thumb state the instrs are 16 bit.

Obviously the normal state instrs are more powerful than thumb state instr.

Sometimes cost, longitivity, power consumption, mem size are more important than performance. In that case thumb instructions are used.

For example,



in 1B of memory, 256 instrs can be stored in normal state.

But if we use thumb instrs we can store 512 instrs, which is double of normal instrs.

ARM E
→ Responds fast (first priority)

ARM M →
(cheapest, less power consumption)

* In thumb state we can store twice no. of instrs than in normal ins instrs. for a size of memory.

* code density increases in thumb state.

* The default value of T is 0.
it is in normal state.
if T=1, the processor is in Thumb state.

Modes:

There are 7 operating modes in ARM processor. The bits in "Mode" indicates in which mode the processor is working right now.

1. Supervisor mode
2. User mode
3. System mode
4. IRQ Mode
5. FIQ Mode
6. Undefined Mode
7. Abort Mode

SPSR (save program status registers)

SPSR is the same as CPSR.

when an processors moves from one mode to another it stores the current status into the SPSR.

while coming back from that mode to previous one. The CPSR restores the status from SPSR.