Dmitry Messerman

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Location: Haifa, Israel (may to relocate to Herzliya, if needed)

# Professional Summary

EDA CAD tool expert with over 20 years of experience in the development, support, and deployment of backend CAD tools and flows for high-speed and analog custom design.

Known for exceptional debugging and problem-solving abilities, with a strong track record of optimizing CAD tools and environments thus enabling efficient, scalable workflows.

# Work Experience

**Principal Engineer at Intel Corporation, Haifa, Israel**  
- Led the development, deployment, and support of in-house and commercial EDA tools for backend verification.  
- Played a key role in the architecture, development and deployment of internal tools for:  
 • BIOS power-up memory training SW/Hardware co-simulation  
 • Platform signal and power integrity, Backend multivendor Analog Design flows

• Resistance, Capacitance and Inductance extraction

- Recognized for exceptional debugging and problem-solving capabilities in multivendor CAD environments.  
- Granted 3 U.S. patents in the areas of Resistance, Capacitance and inductance extraction.  
- Co-authored a technical paper in the field of platform signal integrity.

# Education

Ph.D. in Electrical Engineering, St. Petersburg Polytechnic University, Russian Federation

M.Sc. in Electrophysics, St. Petersburg Polytechnic University, Russian Federation

# Skills

- Programming Languages: C/C++, Python, Perl, Tcl, Skill, MATLAB   
- EDA Tools: Virtuoso (including Analog Design Environment), Liberate and  
- Languages: English, Hebrew, Russian

# Publications and patents

1. Yan J., Aydiner A., Messerman D., Zhu J., Camacho Mora A., Liao J., Ma M., Jiao D. Efficient Equalization Optimization Algorithm for Signaling Analysis. Nonlinear System 2019 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO).
2. Reisfeld G., Messerman D., Bone N., Lazar A. VARAN: variability analysis for memory cell robustness. Proc. SPIE 6925, 69250L, 2008.
3. Messerman D., Seltser M. Reorganizing rectangular layout structures for improved extraction. - United States Patent 7389001 B2, 2008.
4. Chakravarty S., Ben-Noon Y., Chiprout E., Mazumder M., Messerman D. Inductance Modeling. - United States Patent 7325208 B2, 2008.