Dmitry Messerman

**Senior VLSI CAD Engineer**

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# Professional Summary

**Power and signal integrity tools expert** with over 10 years of experience in development of power and signal integrity solutions for advanced silicon package and printed circuit board

**EDA CAD tool expert** with over 10 years of experience in the development, support, and deployment of backend CAD and Silicon Debug tools for high-speed and analog custom design

**Developed and delivered career development mentoring classes** to experienced engineers

**Renowned for multi-disciplinary expertise, exceptional debugging and problem-solving skills**

# Technical Skills

Programming Languages: Python, C/C++, Perl, Tcl, Skill, MATLAB

Multiple Cadence, Synopsys and Siemens tools for Power and Signal Integrity, VLSI design and verification

# Work Experience

**2018 – Present: Principal Engineer, Intel Corporation**

* **Defining, co-development and deploying multi-technology simulation** for Analog Custom Design
  + Solution integrates multiple blocks employing technologies supplied by Intel Foundry and leading 3rd party foundry
* **Defining and comprehensive QA platform** for CAD Analog design solutions
  + Platform supports more than 30 in-house and vendor capabilities integrated in RTL2GDS flow for Analog Design
* **Leading customization, QA effort and Customer support** of Design Engineers and Layout Designers in Analog design domain
  + Deployment of the above solution led to a drastic reduction in SW defects thus contributing to significant increase in design engineers and layout designers productivity
* **Developed and delivered career development mentoring classes** to experienced engineers

**1998 - 2018: CAD SW Engineering Team Lead, Intel Corporation (*Principal Engineer from 2006*)**

* **Leading development of in-house Power and Signal Integrity solutio**n for silicon package and printed circuit board.
  + Developing Fast Signal to Noise Ratio (SNR) estimation algorithm for PCB and silicon package interconnect
* **Leading development of post-silicon debug tools**:

- **Platform HW/SW co-simulation** for BIOS MRC training validation

- **Structure-Based Functional Tests (SBFT) coverage improvement** based on genetic algorithm

* **Leading definition, architecture and implementation of in-house Parasitics Extraction and Reliability verification tools**
  + Parasitics extraction tool has been **used in production for ~10 years**
  + Reliability verification tool has been **used in production for ~20 years**
* **Developing modeling algorithms in multiple areas:** 
  + **Accurate and fast resistance extraction from VLSI layout** - computational geometry algorithm, **patent granted**
  + **Surrogate modeling of silicon heat dissipation in tester environment** based on diffusion equations solver

# Education

**Ph.D. in Electrical Engineering**, St. Petersburg Polytechnic University, Russian Federation.

*Developed 2-D Maxwell full-wave solver for high voltage transmission line above two-layer ground*

**M.Sc. in Electrophysics**, St. Petersburg Polytechnic University, Russian Federation.

# Publications and patents

1. Yan J., Aydiner A., **Messerman D**., Zhu J., Camacho Mora A., Liao J., Ma M., Jiao D. Efficient Equalization Optimization Algorithm for Signaling Analysis. Nonlinear System 2019 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO).
2. Reisfeld G., **Messerman D.**, Bone N., Lazar A. VARAN: variability analysis for memory cell robustness. Proc. SPIE 6925, 69250L, 2008.
3. **Messerman D.**, Seltser M. Reorganizing rectangular layout structures for improved extraction. - United States Patent 7389001 B2, 2008.
4. Chakravarty S., Ben-Noon Y., Chiprout E., Mazumder M., **Messerman D.** Inductance Modeling. - United States Patent 7325208 B2, 2008.

# Languages

**English** – full professional proficiency, **Hebrew** - fluent, **Russian** – native.