Dmitry Messerman

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Location: Haifa, Israel

# Professional Summary

EDA CAD tool expert with over 20 years of experience in the development, support, and deployment of backend CAD and Silicon Debug tools for high-speed and analog custom design.

**Renowned for multi-disciplinary expertise, problem solving and algorithm development.**

# Work Experience

**Principal Engineer at Intel Corporation, Haifa, Israel 1992 - present**  
- Led the development, deployment customization and support of in-house and commercial EDA backend tools

- Collaborated with LLNL on a multi-grid solver for fast voltage droop modeling in Intel processors

- Developed modeling algorithms in multiple areas, for example:

- Fast resistance extraction from VLSI layout - computational geometry algorithm, patent granted

- Fast Signal to Noise Ratio (SNR) estimation algorithm for PCB and silicon package interconnect

- Led development of several post-silicon debug tools. The most prominent project:

- Platform HW/SW co-simulation for BIOS MRC training validation

- Development, customization and support of in-house block and full chip level VLSI layout editors

- **Recognized for exceptional debugging and problem-solving capabilities** in CAD software and Linux

**Physicist and software engineer in FrantzTech Ltd 1990 – 1992**

* Co-developed ultrasound image processing algorithm for early detection of diffused liver diseases

# Education

Ph.D. in Electrical Engineering, St. Petersburg Polytechnic University, Russian Federation

- Developed 2-D Maxwell full-wave solver for high voltage transmission line above two-layer ground

M.Sc. in Electrophysics, St. Petersburg Polytechnic University, Russian Federation

# Skills

- Programming Languages: Python, C/C++, Perl, Tcl, Skill, MATLAB  
- Cadence, Synopsys and Siemens EDA tools for VLSI analog and custom design and verification

- Languages: English, Hebrew, Russian

# Publications and patents

1. Yan J., Aydiner A., **Messerman D**., Zhu J., Camacho Mora A., Liao J., Ma M., Jiao D. Efficient Equalization Optimization Algorithm for Signaling Analysis. Nonlinear System 2019 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO).
2. Reisfeld G., **Messerman D.**, Bone N., Lazar A. VARAN: variability analysis for memory cell robustness. Proc. SPIE 6925, 69250L, 2008.
3. **Messerman D.**, Seltser M. Reorganizing rectangular layout structures for improved extraction. - United States Patent 7389001 B2, 2008.
4. Chakravarty S., Ben-Noon Y., Chiprout E., Mazumder M., **Messerman D.** Inductance Modeling. - United States Patent 7325208 B2, 2008.