Dmitry Messerman

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Location: Haifa, Israel (may to relocate to Herzliya, if needed)

# Professional Summary

EDA CAD tool expert with over 20 years of experience in the development, support, and deployment of backend CAD tools and flows for high-speed and analog custom design.

Renowned for outstanding skills in debugging, problem-solving and algorithm development.

# Work Experience

**Principal Engineer at Intel Corporation, Haifa, Israel 1992 - present**  
- Led the development, deployment, and support of in-house and commercial EDA backend tools

- Developed modeling algorithms in multiple areas

- Fast resistance modeling for VLSI layout - computational geometry algorithm

- Surrogate modeling of silicon heat dissipation in tester environment based on diffusion equations solver

- Fast cross-coupling noise estimation algorithm for PCB and silicon package interconnect

- Recognized for exceptional debugging and problem-solving capabilities in CAD software.  
- Granted 3 U.S. patents in the areas of Resistance, Capacitance and inductance extraction from VLSI layout  
- Co-authored a technical papers in platform signal integrity and VLSI memory cells robustness domains

**Physicist and software engineer in FrantzTech Ltd 1990 – 1992**

* Co-developed ultrasound image processing algorithm for early detection of diffused liver diseases

# Education

Ph.D. in Electrical Engineering, St. Petersburg Polytechnic University, Russian Federation

M.Sc. in Electrophysics, St. Petersburg Polytechnic University, Russian Federation

# Skills

- Programming Languages: Python, C/C++, Perl, Tcl, Skill, MATLAB   
- EDA Tools: Cadence, Synopsys and Siemens tools for VLSI analog design and verification

- Languages: English, Hebrew, Russian

# Publications and patents

1. Yan J., Aydiner A., Messerman D., Zhu J., Camacho Mora A., Liao J., Ma M., Jiao D. Efficient Equalization Optimization Algorithm for Signaling Analysis. Nonlinear System 2019 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO).
2. Reisfeld G., Messerman D., Bone N., Lazar A. VARAN: variability analysis for memory cell robustness. Proc. SPIE 6925, 69250L, 2008.
3. Messerman D., Seltser M. Reorganizing rectangular layout structures for improved extraction. - United States Patent 7389001 B2, 2008.
4. Chakravarty S., Ben-Noon Y., Chiprout E., Mazumder M., Messerman D. Inductance Modeling. - United States Patent 7325208 B2, 2008.