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HEAT SINK DESIGN

WHAT?

Modern chips generate high fluxes that risk overheating. This project optimizes rectangular and triangular fin heat sinks for a 100 × 100 mm chip dissipating 70 W in 3 m/s forced air at 20°C, targeting a base temperature below 70°C.

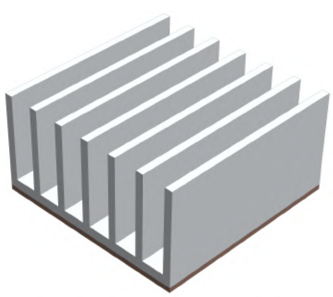
HOW?

Table 1: Approach for heat sink design and validation.

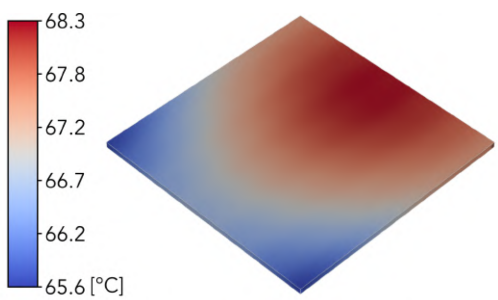
Step	Description / Method
1. Analytical setup	Flat plate convection model under laminar flow ($u_\infty = 3$ m/s, $T_\infty = 20$°C), implemented in **Python**. Calculated $\overline{Nu}_L = 0.664 Re_L^{1/2} Pr^{1/3}$, $h = \overline{Nu}_L k_f / L$.
2. Geometry and resistances	Defined chip size 100×100 mm with $N = 7$, $S = 16$ mm, $t = 4$ mm, fin height $L_f = 45$ mm, and base thickness $L_b = 5$ mm, using **aluminum**. Computed A_f, A_b, A_t, and calculated η_f, η_0, R_b, R_{t0}, and base temperature $T_b = T_\infty + PR_{tot}$.
3. Geometry comparison	Applied the model to rectangular and triangular fins, calculated T_b.
4. CFD validation	Built 3D geometry in **SolidWorks** (a, d) and simulated in Ansys **Fluent** with $P = 70$ W, adiabatic sides, and 3 m/s airflow, comparing CFD T_b with 1D predictions.

RESULTS

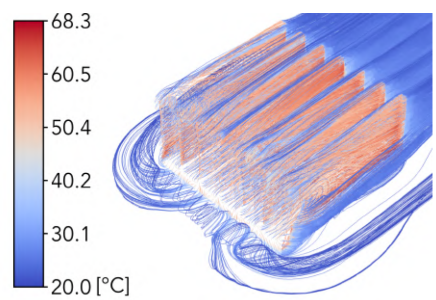
- For the rectangular fins 1D model predicted **66.4°C**, CFD gave **67.4°C** (**1.5%** difference) with **±3%** variation (b). Base was cooler at the leading edge and hotter at the trailing edge (c). CFD confirmed 1D with minor 3D effects.



a) Rectangular heat sink

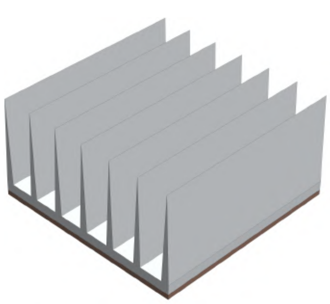


b) Base temperature distribution

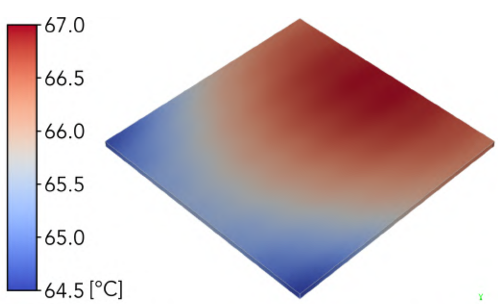


c) Flow pathlines with temperature

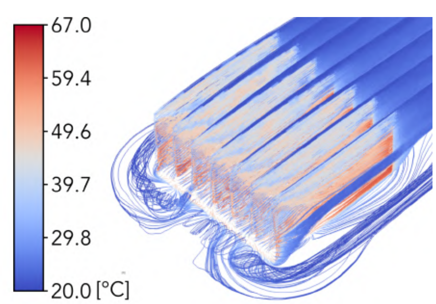
- For the triangular fins 1D model predicted **68.8°C**, CFD gave **66.1°C** (**3.9%** difference) with **±3.5%** variation (e). Base showed similar leading edge cooling and trailing edge heating (f). CFD confirmed 1D with minor 3D effects.



d) Triangular heat sink



e) Base temperature distribution



f) Flow pathlines with temperature

- 1D and CFD confirmed finned heat sinks kept the base below 70°C for a 70 W load. Without fins it reached **344.2°C**, reduced by **80%**. Rectangular matched CFD within **1.5%**, while **triangular** used **36%** less material with cooler results.

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FAN LOCATION OPTIMIZATION IN ICEPAK

WHAT?

ICs generate significant heat, requiring efficient cooling for reliability. The goal of this project is to determine the optimum fan location in a system level IC cooling setup using Ansys Icepak, ensuring chip temperatures remain below 70°C.

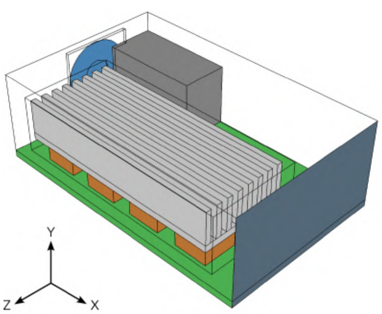
HOW?

Table 1: Approach for fan location optimization in Icepak.

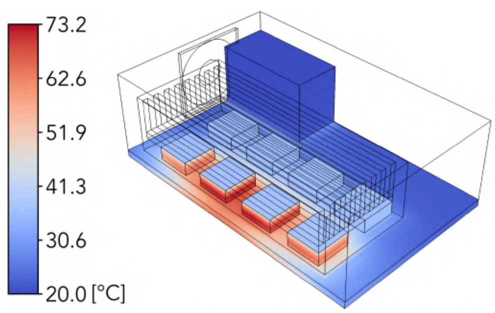
Step	Description / Method
1. Problem setup	Modeled IC chips, bonded fin heat sink (8 fins, 0.008 m), PCB, and perforated grille in **Icepak**.
2. Fan definition	Applied nonlinear fan curve and set boundary conditions for forced convection cooling.
3. Parameterization	Defined fan location (z) as a variable and tested **two** cases: z = 0.1 m (a) and z = 0.165 m (d).
4. Post-processing	Post-processed CFD results in Ansys **CFD Post**, analyzing temperature contours and airflow velocity magnitudes to evaluate chip cooling and fan placement performance.

RESULTS

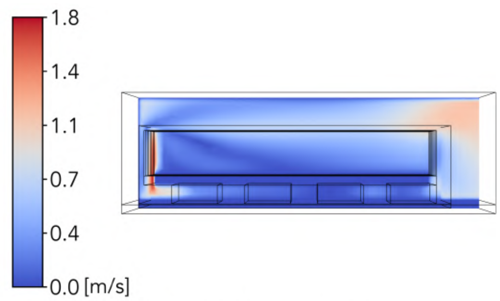
- CFD predicted a peak chip temp. of **73.2°C** (b), above the 70°C limit. Chips near the fan inlet cooled better, while trailing edge chips overheated. Velocity contours (c) showed recirculation and weak airflow, reducing effectiveness.



a) System geometry, fan at z = 0.1 m

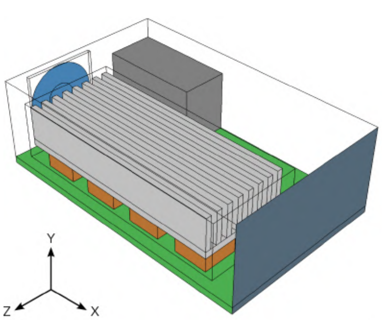


b) Temperature distribution on chips

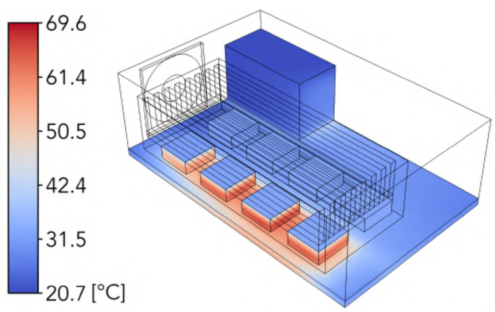


c) Airflow velocity contours

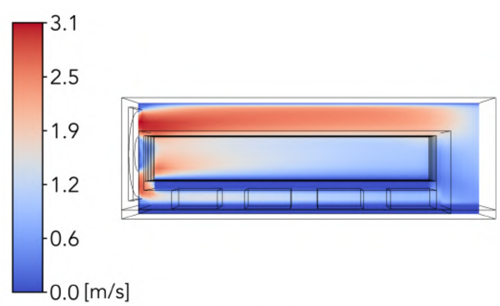
- Relocating the fan downstream improved airflow and cooling. CFD showed chip temperature dropped to 69.6 °C (e). Airflow (f) aligned with fins, strengthening convection. Trailing edge chips cooled better, and temp. spread narrowed.



d) System geometry, fan at z = 0.165 m



e) Temperature distribution on chips



f) Airflow velocity contours

- The study confirmed fan position strongly affects heat transfer. At z = 0.1 m, peak chip temperature reached 73.2°C, while relocating the fan to z = 0.165 m reduced it to 69.6°C, a **5%** reduction with more balanced airflow. The optimized location improved reliability and thermal margin, highlighting the importance of airflow management in IC cooling.