

Mohammad Nayem Hossain

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Education

North South University

B.Sc. in Electrical and Electronics Engineering; **CGPA: 3.01/4.00**

Dissertation Topic: *Chiral standing waves and its trapping force on chiral particles*

Dhaka, Bangladesh

2014 – 2019

Dhaka College

Higher Secondary Certificate (HSC); **GPA: 4.50/5.00**

Dhaka, Bangladesh

2011 – 2012

Noakhali Zilla School

Secondary School Certificate (SSC); **GPA: 5.00/5.00**

Noakhali, Bangladesh

2009 – 2010

Research Interests

Embedded System Design; Wireless Communication Systems; RF Integrated Circuits; Analog Integrated Circuits and Systems

Skills

Programming: Python, C, Verilog, Bash

EDA Tools: Virtuoso, Conformal, PVS (Cadence) & Tanner, Calibre (Mentor Graphics)

Parasitic Extraction: Star RC (Synopsys)

Simulation Tools: Spectre (Cadence), COMSOL Multiphysics, Multisim, Logisim

Tools, Software & Platforms: Microsoft Power BI, MS Office (Excel, Word, PowerPoint, Outlook), \LaTeX , Linux

Languages: Bengali (Native), English (Professional)

Work Experience

Synapse Design Inc.

Analog Layout Design Engineer, Analog and Mixed Signal Dept.

Dhaka, Bangladesh

June 2022 - June 2023

- Worked on some notable blocks of critical IPs such as: **DCO** (*Digitally Controlled Oscillator*) - part of a clock generation module; **PLL** (*Phase Locked Loop*) - part of a high speed SERDES.
- **Responsibilities:**
 - Developed a proper routing and pin placement throughout the DCO to sync the pin with the digital controller unit of the clock generation module.
 - Maintained the device and routing matching for PLL to achieve the desired frequency range, signal integrity and area utilization.
 - Collaborated closely with circuit designer to optimize circuit performance by addressing parasitic issues, leading to an increase in operating frequency.
 - Provided training and mentorship to junior engineers to support their professional development and enhance their skills within the team.
- **Technology Nodes used:** TSMC - 5nm, 7nm

Ulkasemi Pvt. Limited

Assistant Engineer, IC Mask Design Dept.

Dhaka, Bangladesh

February 2021 - May 2022

- Contributed to several blocks in some major projects such as: **PVT Sensor** - part of the Test Chip; **Receiver unit** - part of a Network module.
- Developed and maintained Bash scripts to automate tasks.
- **Responsibilities:**
 - Utilized common centroid matching technique for transistor placement to keep the parasitics the same on both sides, especially for sub-block Rx differential amplifier.
 - Built custom standard cells to achieve optimum efficiency, minimize crosstalk, and optimize power flow.
 - Developed and incorporated signal ESD (Electrostatic Discharge) protection in response to increased input voltage requirements within the design by collaborating with a circuit engineer.
 - Worked extensively on cross-site projects with people in multiple time zones.
- **Technology Nodes used:** TSMC - 5nm, Intel - 22nm

North South University

Under-Graduate Assistant, Department of Electrical & Computer Engineering

Dhaka, Bangladesh

May 2019 - August 2019

• Responsibilities:

- Conducted tutorial sessions for students needing extra help outside of class hours.
- Assisted faculty members in course-related work, such as preparing course materials and organizing class activities.
- Graded homework and assignments, ensuring fair and consistent grading across all students.
- Provided feedback to students to help them improve their understanding of course concepts.

Research Experience

Chiral standing waves and its trapping force on chiral particles

• Short Description:

- This study investigates trapping forces on chiral particles in a field with two counter-propagating, orthogonally polarized plane waves. It models the particles as chiral dipoles and analyzes the optical force. Results reveal a strong correlation with field symmetry and material asymmetry. This method can trap chiral Mie objects, offering potential applications in chirality identification and selective trapping.

• Associated Lab: *NSU Optics Lab*

Relevant Coursework

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|--|----------------------------------|-------------------------|
| • Introduction to VLSI Design | • Electromagnetic Fields & Waves | • Digital Logic Design |
| • Semiconductor Devices and Technology | • Analog Electronics I & II | • Communication Systems |
| | • Signals and Systems | • Computer Architecture |

Professional Training

Tahoe VLSI Training Institute

September 2019 - December 2019

- Performed block level synthesis using Genus to transform a high level design into a gate level representation.
- Assessed the logical equivalence of the design by using the Conformal tool.
- Carried out the placement and routing for block level designs.
- Executed clock tree synthesis (CTS) and static timing analysis.
- Evaluated the design through LVS and DRC inspections.

Test Scores

IELTS Academic Test

September 2023

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|-----------------|---------------|---------------|-----------------|----------------|
| • Overall - 7.5 | • Reading - 8 | • Writing - 7 | • Listening - 7 | • Speaking - 7 |
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Scholarship & Awards

- **Robotics Competition:** Earned 1st place for outstanding performance in the national robotics competition hosted by the Military Institute of Science & Technology.
- **Financial Aid:** Achieved 25% tuition waiver from Spring 2015 to Summer 2018, North South University, Bangladesh.

Certifications

- **Virtuoso Layout Design Basics**, issued by **Cadence Design Systems**

Extracurricular Activities

IEEE NSU Robotics and Automation Society

Member

Dhaka, Bangladesh

2015 – 2016

JAAGO Foundation

Volunteer

Dhaka, Bangladesh

2014 – 2015

Volunteer for Bangladesh (VBD)

Community Volunteer

Dhaka, Bangladesh

2014 – 2015