Mohammad Nayem Hossain

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SUMMARY

Analog Layout Engineer with a demonstrated history of working in the semiconductor industry while gathering experience by involving various projects in different process nodes for block and top level. Skilled in floor planning, placement, routing, matching techniques, verification (LVS and DRC), and RC checks.

WORK EXPERIENCE

Analog Layout Design Engineer **Jun 2022 – Present**
***Synapse Design**, IC Mask Design* *Dhaka, Bangladesh*

- Contributed to the layout design of PLL, Low Voltage Bandgap, CLKBUF, and other critical components for a high-speed SERDES project using a 6nm process node.
- Expertise in planning and distributing power grids for full chip designs and implementing compact layouts with proper routing techniques.
- Capable of using symmetrical array-wise routing and device placement, as well as matching differential pair MOSFETs and implementing Powerfets and triple guard rings to prevent leakage.
- Engaging in close collaboration with teams from different functions to ensure that the design meets all necessary sign-off requirements.

Assistant Engineer **Feb 2021 – May 2022**
***Ulkasemi Limited**, IC Mask Design* *Dhaka, Bangladesh*

- Worked on multiple projects aimed at creating custom SOC in Planar and FinFet technologies from 22nm down to 4nm process node including Comparator, Operational amplifiers of different topologies, Bias generators, Bandgap reference, Phase Locked Loop etc.
- Skilled in power planning, floor planning and device placement with consideration of device matching, critical device, device orientation, critical signals and shielding of critical nets in different subblocks and macroblocks.
- Possesses a good understanding of CMOS concepts and layout issues such as noise and distortion, latch-up, antenna effects, electro-migration issues, ESD, IR, and Shielding.
- Maintaining symmetric routing to keep the same parasitic parameters on both nets solving the timing issues by maintaining a shorter route.
- Experience in working with full custom, p-cell and standard cell-based layouts.
- Worked extensively on cross-site projects with people in multiple time zones.

Intern **Jun 2018 – Aug 2019**
***United Power Generation & Distribution Company Ltd**, Electrical Engineering Dept.* *Dhaka, Bangladesh*

- **Responsibilities:**
  - Accountable for ensuring uninterrupted power supply by maintaining the Switchgear protection unit.
  - Collecting data from the SCADA system and analyzing it for insights.
  - Assisted in operating and monitoring the Gen-set and Engine system.
  - Maintained Wärtsilä & Rolls-Royce Engine and ensured their proper functioning.
  - Reported progress updates at weekly team meetings.

EDUCATION

North South University **Dhaka, Bangladesh**
BS in Electrical and Electronic Engineering; CGPA: 3.01 out of 4.00 (83%-85%) *2015 – 2019*

- Dissertation Topic: Chiral standing waves and its trapping force on chiral particles

Dhaka College **Dhaka, Bangladesh**
Higher Secondary Certificate; Science Group; GPA: 4.50 out of 5.00 *2011 – 2013*

Noakhali Zilla School **Noakhali, Bangladesh**
Secondary School Certificate; Science Group; GPA: 5.00 out of 5.00 *2009 – 2011*

PROFESSIONAL TRAINING

Tahoe VLSI Training Institute **Aug 2019 - Dec 2019**

- Performed block-level & full-chip synthesis using Genus
- Placement and routing of full-chip & block-level design
- Analyzed the logical equivalence of the design
- Execution of CTS and Static timing analysis
- Evaluation of the design by checking LVS & DRC

RESEARCH WORKS

- **Chiral standing waves and its trapping force on chiral particles** [Tianhang Zhang, M.R.C. Mahdy, Shadman Sajid Dewan, **Md. Nayem Hossain**, Hamim Mahmud Rivy, Nabila Masud, Ziaur Rahman Jony] This paper proposed a case where the optical force exerted on an object is purely due to the chirality while there is zero force on a non-chiral object. It also revealed the underlying physics of this force by modelling the particle as a chiral diploe and analytical study of the optical energy.

UNDERGRADUATE COURSEWORK

- **Elective Courses:** EEE413-Verilog HDL: Modeling, Simulation and Synthesis, EEE411-Introduction to VLSI Design, EEE410-Semiconductor Devices and Technology
- **EEE Core Courses:** EEE361-Electromagnetic Fields & Waves, EEE311&111-Analog Electronics II&I, EEE221-Signals and Systems, EEE211-Digital Logic Design
- **Mathematical Courses:** MAT125-Introduction to Linear Algebra, MAT350-Engineering Mathematics, MAT361-Probability and Statistics

SKILLS

- **Programming Languages:** Python, Verilog, Bash
- **EDA tools: Cadence:** Virtuoso, Conformal, PVS **Mentor Graphics:** Tanner, Calibre
- **Synthesis & PnR tools:** Genus & Innovus
- **Simulation Tools and Others:** COMSOL Multiphysics, Multisim, Logisim
- **Packages:** MS Word, MS PowerPoint, MS Excel, and LaTeX
- **Languages:** Bengali (Native), and English (Proficient)

LICENSES & CERTIFICATIONS

- **Virtuoso Layout Design Basics**, issued by **Cadence Design Systems**

EXTRACURRICULAR ACTIVITIES

JAAGO Foundation **Dhaka, Bangladesh**
Volunteer *2014 – 2015*

- JAAGO Foundation works to better the nation by fulfilling the educational needs of underprivileged children. I attended several events organised by JAAGO, including The Great Kindness Challenge, World Environment Day & Universal Children's Day.

HONORS & AWARDS

- 1st Prize for outstanding performance from the biggest national robotics competition organised by the Military Institute of Science & Technology.
- Merit-based partial scholarship for four consecutive years awarded by North South University.