

# **ME 311: Microprocessors and Automatic Control**

Sequential logic fundamentals  
Flipflops (latches):  
RS and D latches



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1



Life Skill

## **How to reduce time required for study?**

- Fact: if we sit for study for 2 hrs actual time our mind is at study (productive time) is only 30 mins on an average!
- How can we change this?
- Focus concentration?? How?
- By training our mind to get rid of things: the way we train our body to be strong

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2

2



## Recap

- RS flip flop constructed to get notion of memory in circuits
- Truth table: forbidden inputs

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3

3



## Basic Concept

- Use feedback in digital circuits
- Output =  $f(\text{input}, \text{previous input})$
- How and why feedback gives ability to remember a state? → we will see in few lectures
- These circuits form basic blocks for building memory elements

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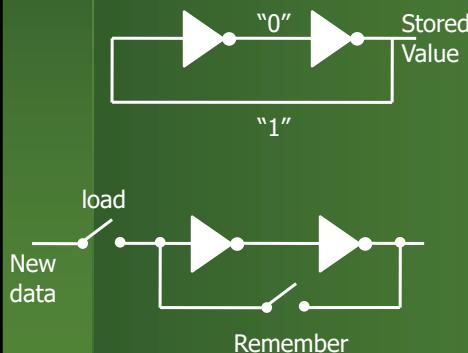
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## Using feedback to create memory



- Example: two inverters with feedback
- Will hold the value as long as power is applied
- How to get a new value in memory cell??
  - Selectively break feedback path

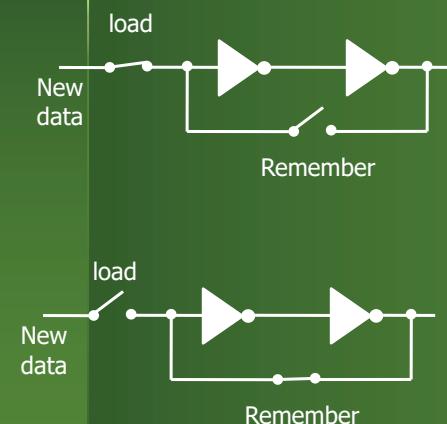
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5

5



## Using feedback to create memory



- To load value
  - Open remember switch
  - Press load switch and give 0 or 1 on new data as need be
  - Close remember switch
  - Open load switch

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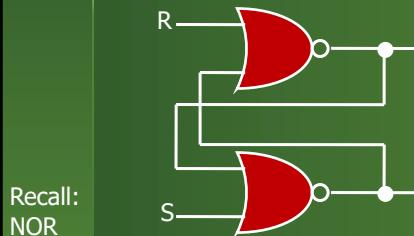
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6



## R-S Flip Flop (Latch)

Another way of using feedback without need of switches to load



Recall:  
NOR

Truth table

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

- How do we analyze circuit shown?
- NOR gate with feedback from other
- Recall NOR truth table
- Observe: NOR gate with one 0 input → inverter wrt other input

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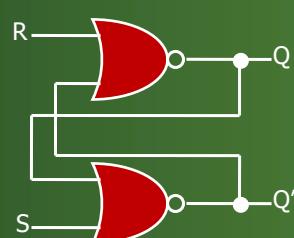
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7



## R-S Latch

Summarize the analysis in form of Truth table!!



Recall: NOR  
Truth table

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

- R=0, S=1: similar condition
- R=0, S=0: inverters in feedback → HOLD

R	S	Q	Q'
1	0	0	1
0	1	1	0
0	0	HOLD	HOLD
1	1	0	0

} 'Load'  
'Remember'  
?

Notice that current Value is same as the previous or in other words current value depends on previous

Hence notion of time is required to study such circuits

These are kept red for a reason that this condition should be avoided  
Q: BUT Why? → let's see ...

8



# This presentation

- Introducing notion of time into circuits using clock to enable RS latch using other gates
- Concept of edge triggering useful for implementation and simplicity in scaling
- D flip flop construction and use.

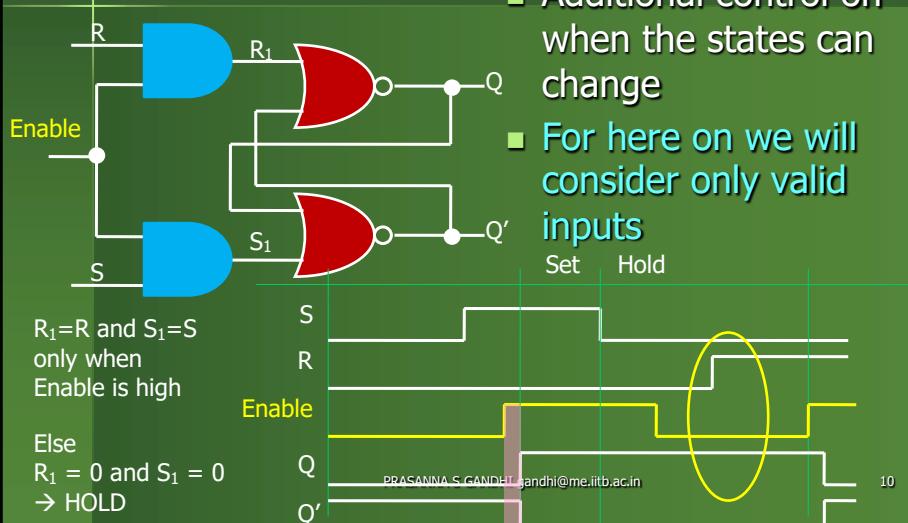
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9

9



## Gated R-S Latch



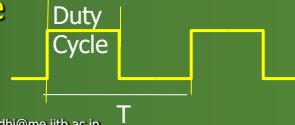
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# Clock

- Used to keep track of time
  - Allow sufficient time to have states  $R', S'$  settle and then have their effect transferred to  $Q, Q'$
  - Control on when the state changes take place
  - Synchronization of several devices put together
- Periodic signal with duty cycle
  - Example: 50% duty cycle
  - Used in place of enable



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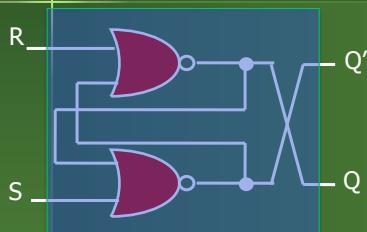
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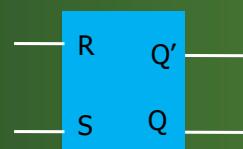


# R-S Latch

Compact Representation



- Recall that each nor gate further has so many CMOS transistors
- At hardware everything is combination of CMOS transistors...

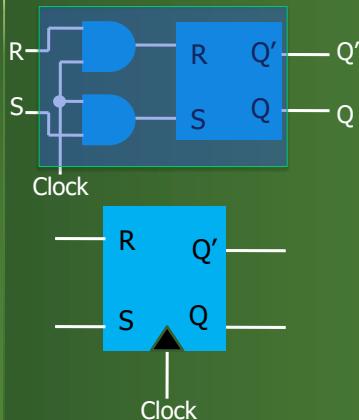


12



## Gated R-S Latch

Compact Representation



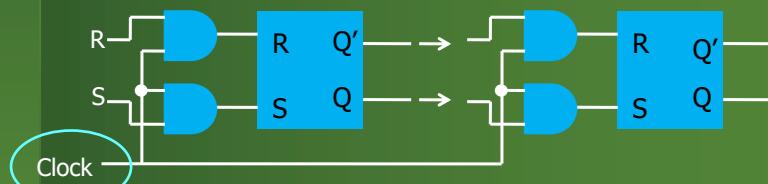
- We will consider more compact representation shown because we may need to connect many such latches together to achieve desired application
- Recall that each nor gate further has so many CMOS transistors
- At hardware everything is combination of CMOS transistors...

13



## Connecting Latches

- To transfer stored value from one latch to another
- Think what will happen if we connect two Gated RS FFs as shown below (imagine if there are 10 or 100 such things connected in series !! )



- How to control changes racing through the circuit?
- Can you think of a solution? What we want is the next latch should be disabled when first is enabled

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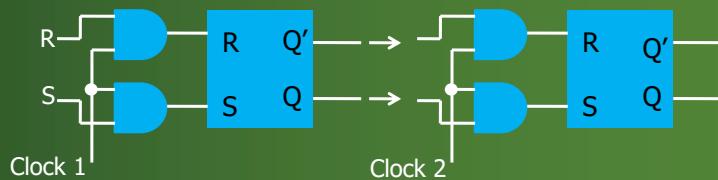
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14



## Connecting Latches

- One of the solutions to use separate clock for each of the latches. Lets analyze..
- Q: will this work? Yes it will theoretically.



- What it means to implement is we will need so many different clocks (recall scaling) with precise time delay
- Too much to demand from hardware. Can there be another solution??

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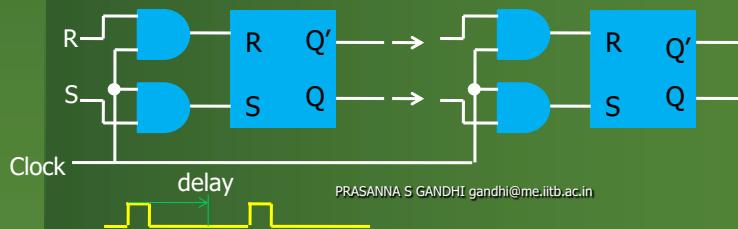
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15



## Connecting Latches

- How to control changes racing through circuit?
- One of the solutions could be change clock duty cycle!!
- In configuration below clock duty cycle needs to be designed carefully (Should be **less than** delay or time for change in Q to happen once R is changed and clock enabled) so changes in first latch would happen but will not be transmitted to second latch
- Hmm! May work. But precision is needed in designing clock duty cycle and implementation is too cumbersome (why? how much would be this time physically? Few femtoseconds or nanoseconds)



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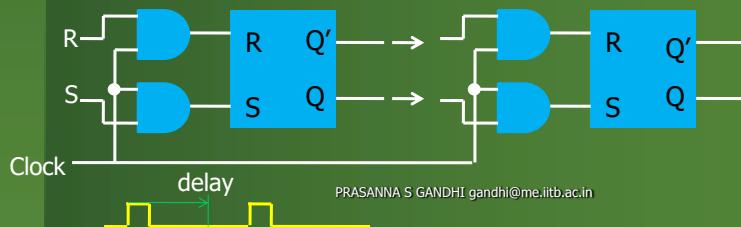
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16



## Connecting Latches

- So do you see difficulty in the previous solution?
  - On one side we need to make duty cycle small however latches have to be enabled for ‘enough’ time for inputs to have desired effect
  - Another problem is practically how do we implement such small duty cycles!!
- → so need some alternative arrangement



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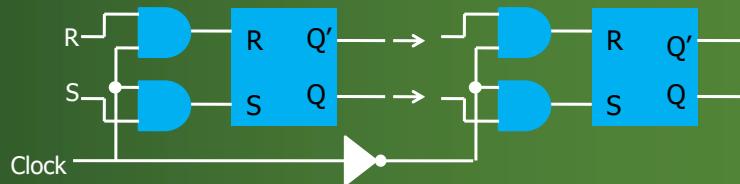
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17



## Connecting Latches

- Another approach: use different polarities of clock on two latches by introducing inverter as shown



- ☺ so now second latch will be disabled during time the first is enabled so changes cannot rush through they will proceed in steps corresponding to half clock cycle

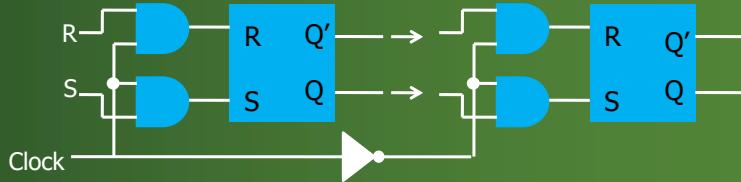
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18

18



## Connecting Latches



- Do you see any other problem??
- Think of connecting several of them in complex fashion (need not necessarily in series)
- Would it be **easily** scalable or not

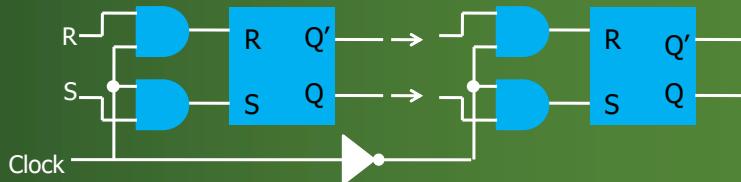
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19

19



## Connecting Latches



- Two flavors of latches those enabled on clock high and others on clock low
- So need to keep track of which all in circuit should be enabled on clock high and others on clock low
- This may become unmanageable for still larger circuits:  
“latches with only opposite polarities can be connected” : constraint

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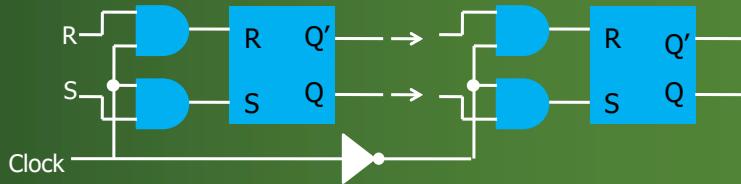
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## Connecting Latches



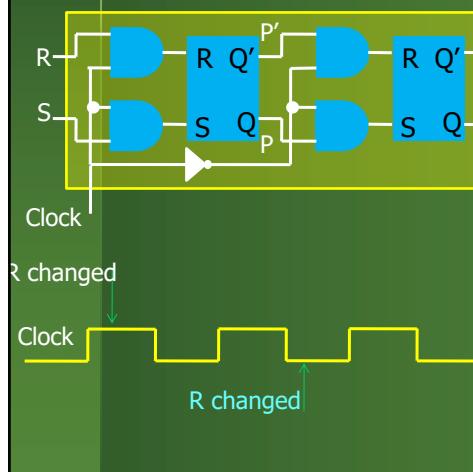
- Q: What solution you can think of?
- Just combine the entire thing in one block
- If you think of complex circuit building with such blocks. They all will have only one polarity of clock for all blocks
- Flip side: ⚡ use double the number of transistors
- Q: when and how the changes will take place in such circuit?

21

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## Connecting Latches

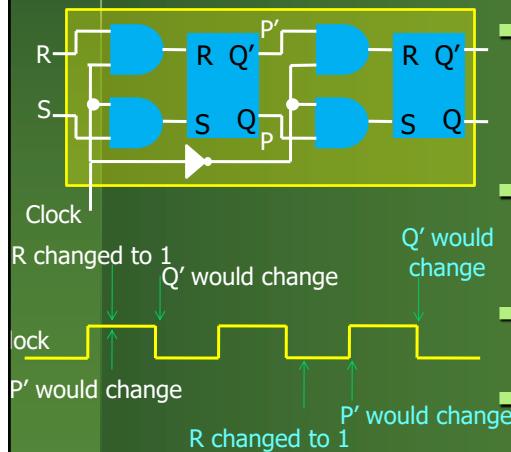


- So question is when input R is changed, when  $Q'$  (output of overall block) would see the corresponding change?
- In first half of clock cycle effect of R change will be transferred to  $P'$
- When the next clock goes down
- See the two cases considered on clock waveform
- Question when  $Q'$  will change corresponding to R?

22



## Connecting Latches

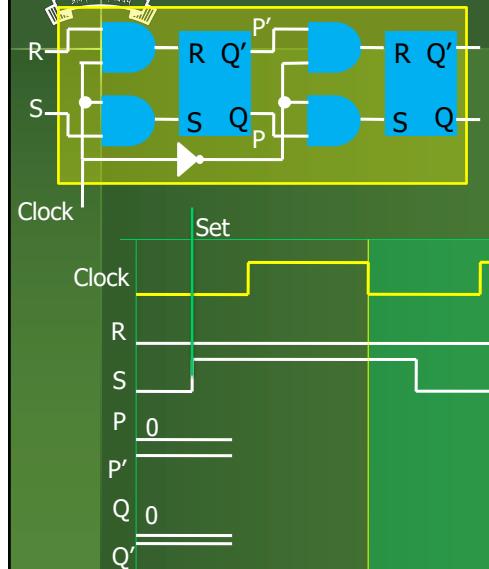


- So question is when input R is changed, when Q' (output of overall block) would see the change?
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23



## Connecting Latches



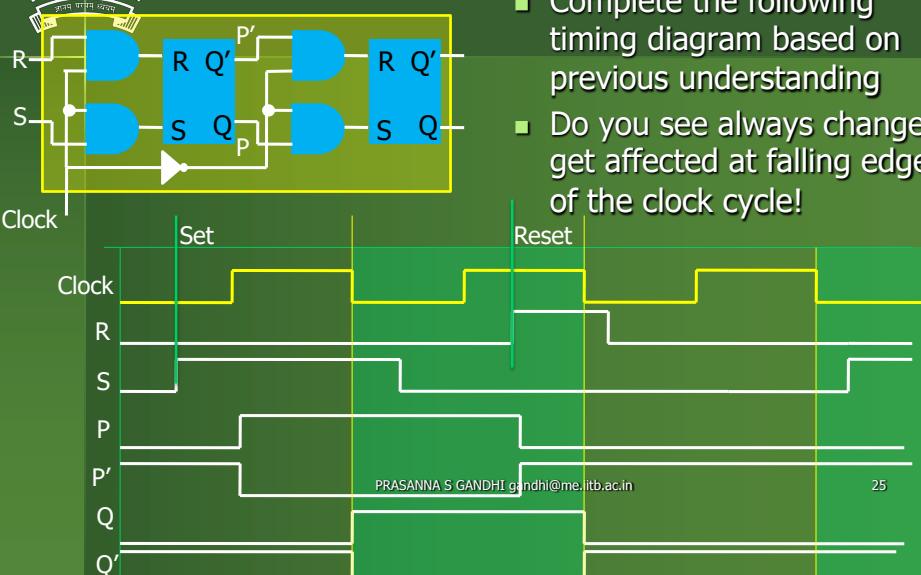
- Complete the following timing diagram based on previous understanding

24



## Connecting Latches

- Complete the following timing diagram based on previous understanding
- Do you see always changes get affected at falling edge of the clock cycle!



25

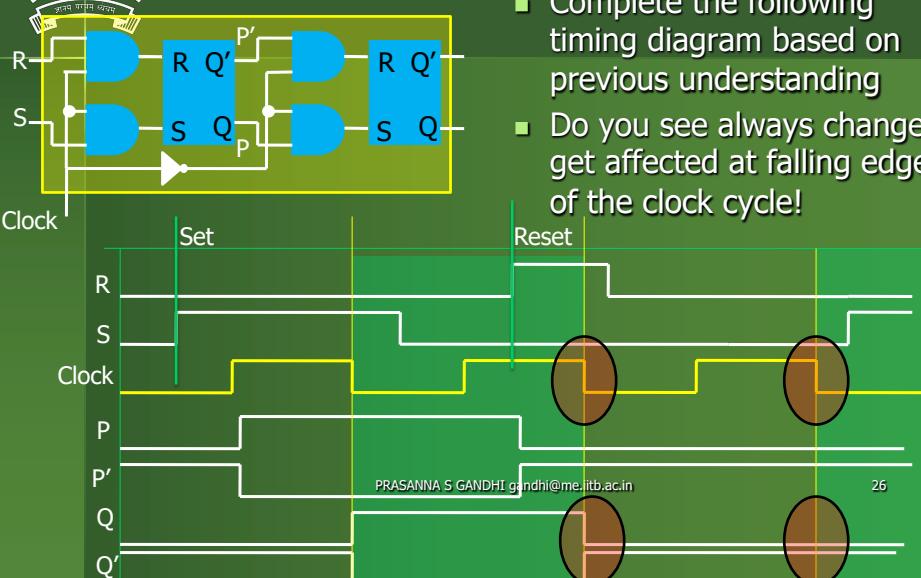
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25



## Connecting Latches

- Complete the following timing diagram based on previous understanding
- Do you see always changes get affected at falling edge of the clock cycle!



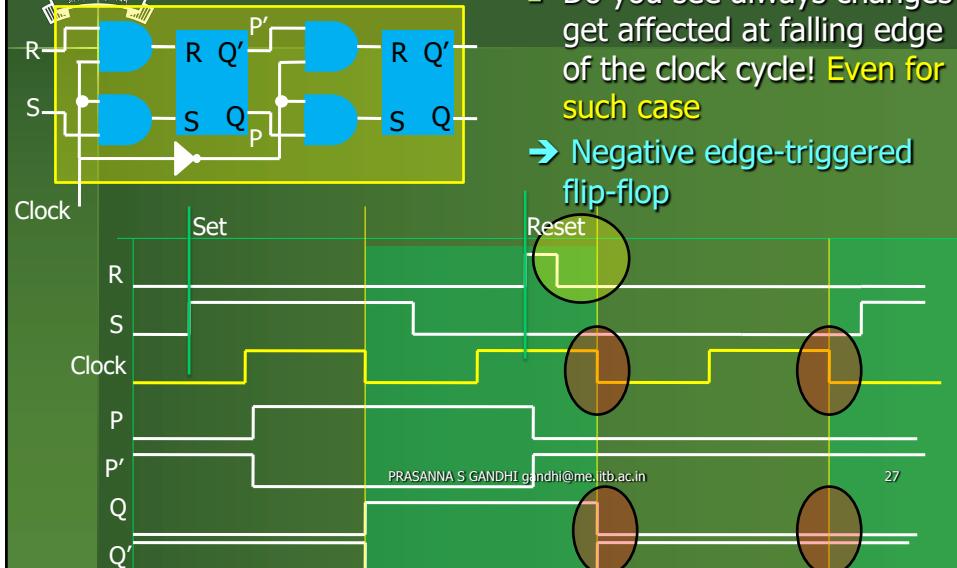
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26



## Connecting Latches



27

- Do you see always changes get affected at falling edge of the clock cycle! Even for such case  
→ Negative edge-triggered flip-flop

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27



## Connecting Latches

- So what have we achieved so far?
- The way to connect multiple number of latches to build complex circuits such that the changes get transferred sequentially in sync with clock
- We add one more facility before going in for use of all these in some applications! Ok!!

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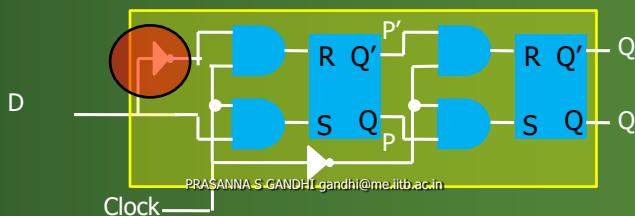
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28



## D Flip-Flop

- What if we use inverter between R and S, we will have only one input designated as D.
- Q: can you think how this circuit will behave?
- Since R and S cannot be both zero when clock is enable storing of value will happen only during clock cycle!!



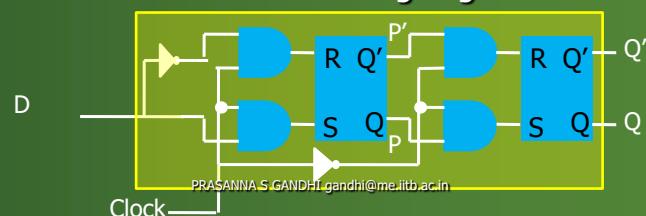
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29



## D Flip-Flop

- The new value at D will get transferred to  $Q'$  on the next falling edge of clock
- Cannot just hold previous value. New value is 'read' every clock cycle ( $D - \text{data}$ )
- Till it affects the output, the previous value is still available at the output
- Whatever data value is at the D input, that value will be stored at the next falling edge of clock



30

30



## D Flip-flop

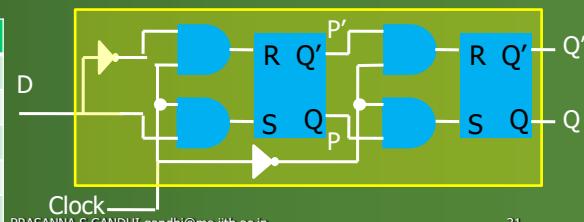
■ This is called D Flip-flop (flip-flop instead of latch since insensitive to momentary glitches at input)

- Characteristics equation is simple

$$Q^+ = D$$

- D-negative edge-triggered flip-flop
- Many other variants of flip-flop are available. Ex JK flip-flop

Clk	D	Q	Next Q
1	0	0	0
2	1	0	1
3	0	1	0
4	1	1	1
No clk	0	0	0
No clk	1	0	0



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31

◀ Value is HELD between two clock triggers

31



## THANK YOU

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32

32

16