TUTORIAL 2

1) : State true or false with proper justification
   1. 8 bit memory can have size only upto 256 bytes.
   2. in 16 bit memory each register can store only 2^16 distinct data values
   3. The maximum no of memory registers that can be accessed from a 4 line address bus is 16
   4. When OE pin of any 8-bit register is made high, data from register is transferred to one of the lines of databus bitwise (1 clock cycle per bit) in 8 clock cycles
   5. It is possible to transfer data from one memory location to the other without using the external register
   6. Number of address-lines in a microcontroller must be greater than the number of data-lines.

Solution

1. False

Reason :- 8 bits equal to one byte

2.True

Reason :- Each 16 bit register can store 2^16 values

3.True

Reason :- Maximum number of memory registers that can be accessed is 2^4 values

4.False

Reason :- data is transferred simultaneously to all 8 lines

5.False

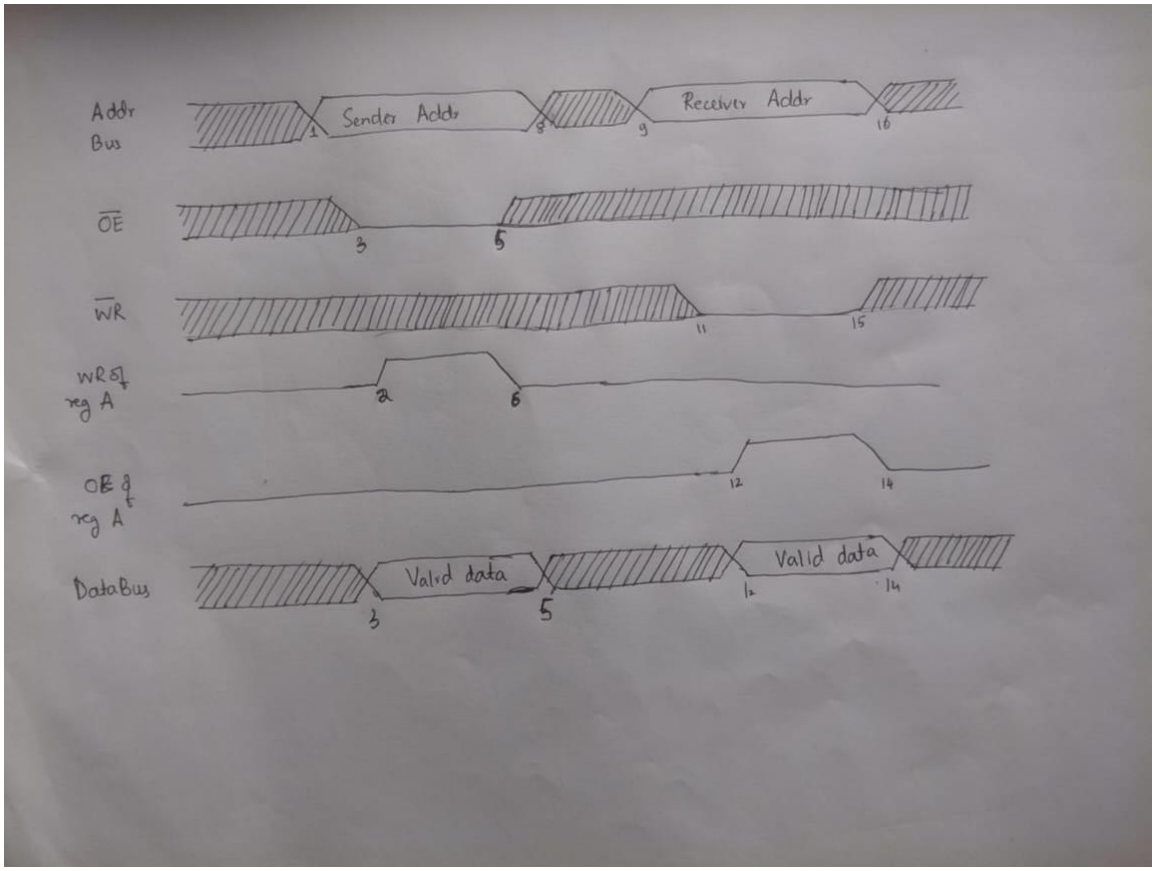
6.False

Not necessarily we can have the number of data lines equal to number of address lines

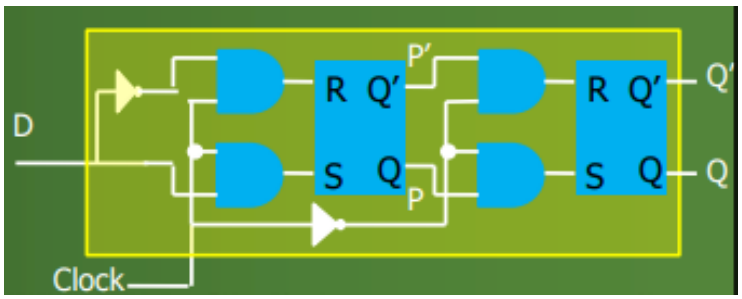
2) Write a sequence of operations to transfer the data from one memory location to the other memory location via external register A. Draw a corresponding timing diagram?

Solution

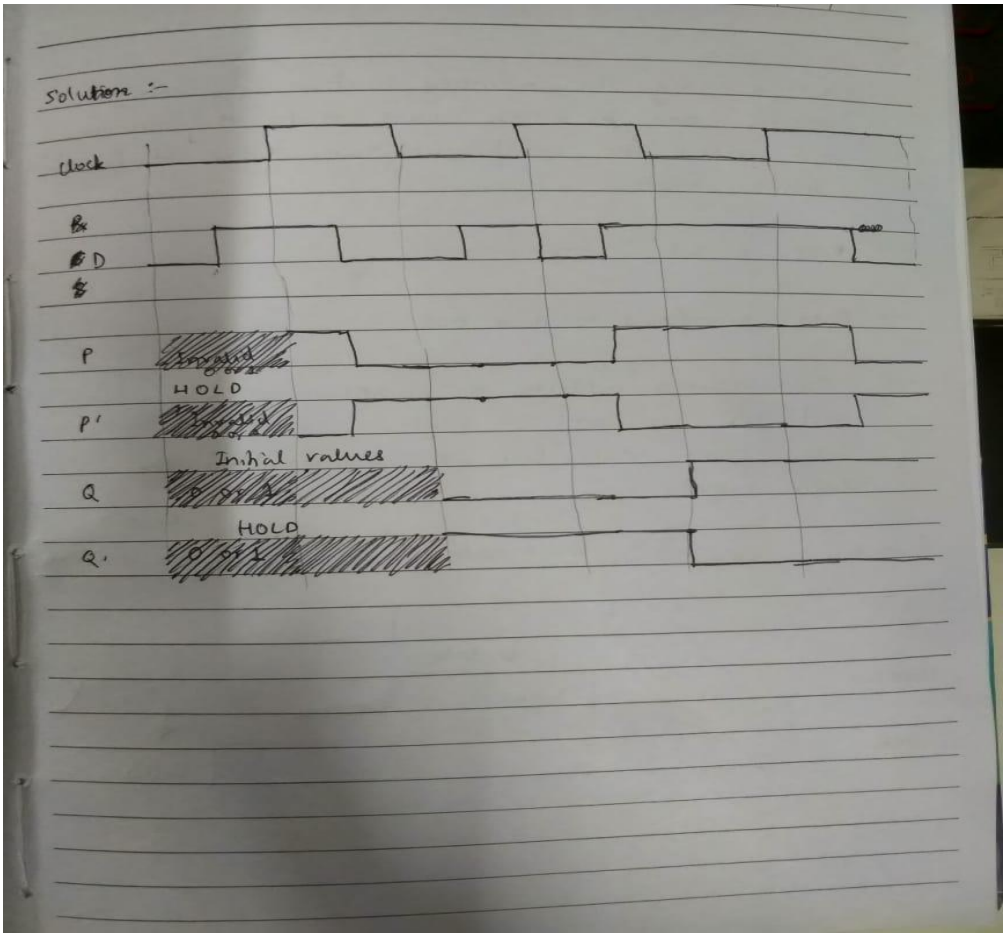
- First step is to access the memory location of register from where data has to be read
- When the address is put into the address bus we enable the OE (Read Enable) to transfer data from the memory location to data bus
- Next, we enable the WR (write) of the register A to store the data
- After writing we disable WR, and load a new address into the address bus it is of the memory location where the data has to be sent/stored
- We enable the WR of the memory so that data can be transferred from data bus to memory location
- Next, we enable the OE of register A to transfer data from the register to data bus
- We then disable the write enable of memory and OE of register A



3) Given the internal circuit of D flip flop constructed using gated RS flip flop. Refer to the truth table of RS flip flop and sketch signals P, and Q with reference to clock when input is given to D pin as shown. Is this positive or negative edge triggered D flip-flop?

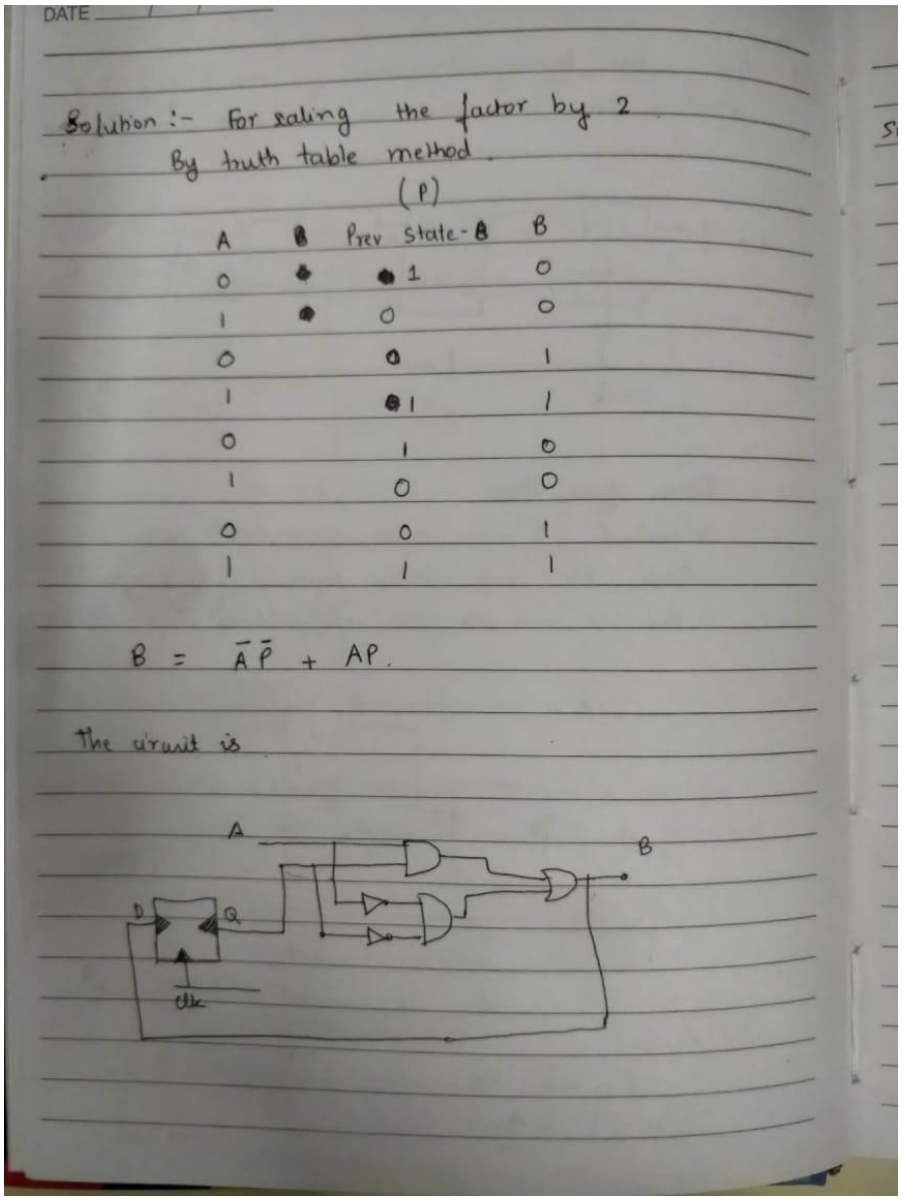


Solution :

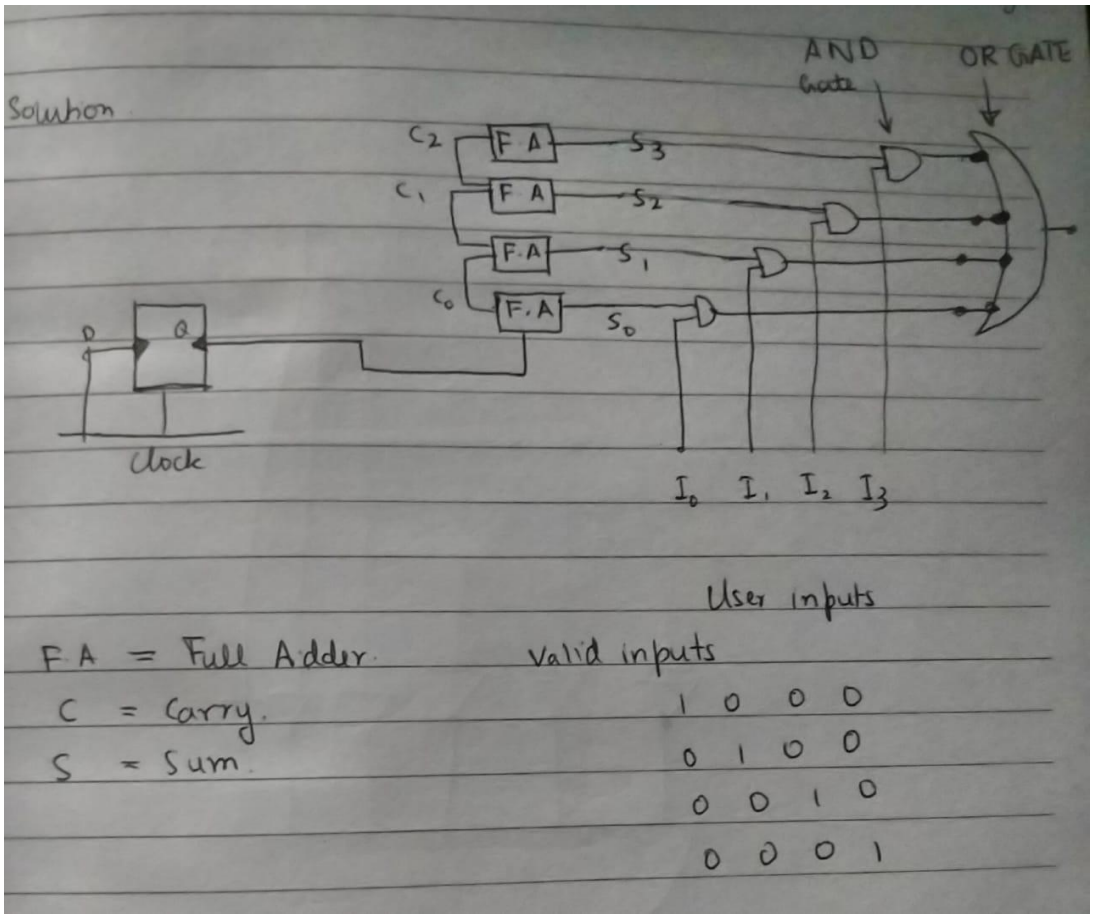


4) Design a sequential circuit with clock as an input such that the output signal is a clock with time period = 1,2,4,8 times the clock cycle
(It is enough of you show for just 2 and demonstrate scalability for 4, rest is scalable)
There are many ways to solve this problem. Please write all assumptions, you can also use blocks like half-adders, full adders etc

Solution : a)



Solution b)



c) using counters