Exam 28 April 2015, questions

Computer Architecture (The University of Edinburgh)

UNIVERSITY OF EDINBURGH

COLLEGE OF SCIENCE AND ENGINEERING

SCHOOL OF INFORMATICS

INFR09009 COMPUTER ARCHITECTURE

Tuesday 28th April 2015

14:30 to 16:30

INSTRUCTIONS TO CANDIDATES

Answer any TWO questions.

All questions carry equal weight.

CALCULATORS MAY NOT BE USED IN THIS EXAMINATION

Year 3 Courses

Convener: S. Viglas
External Examiners: A. Cohn, T. Field

THIS EXAMINATION WILL BE MARKED ANONYMOUSLY

1. (a) At the New York Macworld Expo Keynote on July 18, 2001, Steve Jobs described an 867 MHz G4 as completing a task in 45 seconds while a 1.7 GHz Pentium 4 took 82 seconds for the same task. How can the Pentium 4 (with a higher clock frequency) perform worse than the G4? [*4 marks*]

   (b) For each of the following assertions, state true or false and justify your answer with reasons.

      i. Microarchitectural techniques (such as caching and pipelining) help reduce execution time by decreasing the number of instructions executed. [*2 marks*]

      ii. The compiler typically needs to know about the microarchitecture of the target processor in order for it to be able to generate correct code. [*2 marks*]

      iii. Instruction set design can impact the clock cycle time. [*2 marks*]

      iv. It is possible to decrease clock cycle time by increasing the number of pipeline stages. [*2 marks*]

      v. Whether or not a processor is RISC (Reduced Instruction Set Computer) is decided purely by the number of instructions supported by the processor. [*2 marks*]

      vi. Pipelining is a technique for exploiting Instruction Level Parallelism (ILP). [*2 marks*]

   (c) What is a branch target buffer? [*1 mark*]

   (d) Explain why a branch target buffer will not work well for predicting the target address of return instructions? [*2 marks*]

   (e) Design a hardware structure that will be able to predict the target address of return instructions well. Explain its workings with an example. [*6 marks*]

2. (a) Does the classical 5-stage pipeline experience WAR hazards? If so, explain, with the help of an example, how WAR hazards are handled. If not, explain why WAR hazards do not occur. [*2 marks*]

   (b) Does the classical 5-stage pipeline experience WAW hazards? If so, explain, with the help of an example, how WAW hazards are handled. If not, explain why WAW hazards do not occur. [*2 marks*]

   (c) Consider an extended pipeline where the classical 5-stage pipeline is extended with multi-cycle operations. Will the extended pipeline experience WAR hazards? If so, explain, with the help of an example, how WAR hazards are handled in such a pipeline. If not, explain why WAR hazards do not occur. [*2 marks*]

   (d) Will the same extended pipeline (classical 5-stage pipeline extended with multicycle operations) experience WAW hazards? If so, explain, with the help of an example, how WAW hazards are handled in such a pipeline. If not, explain why WAW hazards do not occur. [*2 marks*]

   (e) Explain, with the help of an example, how WAR hazards are handled by Scoreboarding? [*3 marks*]

   (f) How does the Tomasulo algorithm eliminate WAR and RAW hazards? [*3 marks*]

   (g) For the following fragment of MIPS-like assembly code, identify all data hazards in this code sequence, characterising each one as RAW, WAR or WAW. [*4 marks*]

```
LD      R1, 0(R8)
DIV     R2, R1, R3
DIV     R6, R5, R4
ADD     R1, R6, R7
```

   (h) For the same code fragment, present a table to show how each instruction would progress through a 5-stage pipelined processor with normal forwarding and bypassing hardware, extended with multicycle operations. For this problem, assume the following:

   - 1 Integer ALU of latency 1 cycle.
   - 1 Integer divide unit of latency 3 cycles; the divide unit is not pipelined.

   State any other assumption you make. *Hint:* Your table should have one row per instruction, and one column per clock cycle period, with time increasing from left to right. Each table entry should indicate the pipeline stage for which the instruction is present at the given cycle. [*7 marks*]

3. For the following questions, consider a two-level cache hierarchy with the following parameters:

   - L1 cache: n_1 sets, a_1 associativity, b_1 block size, replacement policy: LRU (if applicable)
   - L2 cache: n_2 sets, a_2 associativity, b_2 block size, replacement policy: LRU (if applicable)

   (a) "Architects typically opt for a much larger L1 cache compared to L2". Is this statement true or false? Justify your answer with reasons. [*3 marks*]

   (b) How is the local L2 miss-rate different from the global L2 miss-rate? Explain why local L2 cache miss rates are typically much higher than global L2 miss rates? [*4 marks*]

   (c) What does it mean for an L2 cache to be inclusive? [*2 marks*]

   (d) What does it mean for an L2 cache to be exclusive? [*2 marks*]

   (e) Is it possible for an L2 cache to be neither inclusive nor exclusive [*2 marks*]

   (f) State one advantage and one disadvantage of having an inclusive L2 cache. [*2 marks*]

   (g) Let us suppose that both L1 and L2 are direct-mapped caches ($a_1 = a_2 = 1$). Further, let us assume $b_1 = 4$ bytes and $b_2 = 8$ bytes, and $n_1 = 4$ and $n_2 = 8$. For these parameters, is L2 guaranteed to be inclusive? If so, argue why that is the case. If inclusion is not guaranteed, provide a counter-example. [*5 marks*]

   (h) Let us suppose both L1 and L2 are 2-way set associative ($a_1 = a_2 = 2$). Further, let us assume both caches have the same block size ($b_1 = b_2 = 8$ bytes), and $n_1 = 4$ and $n_2 = 8$. For these parameters, is L2 guaranteed to be inclusive? If so, argue why that is the case. If inclusion is not guaranteed, provide a counter-example. [*5 marks*]