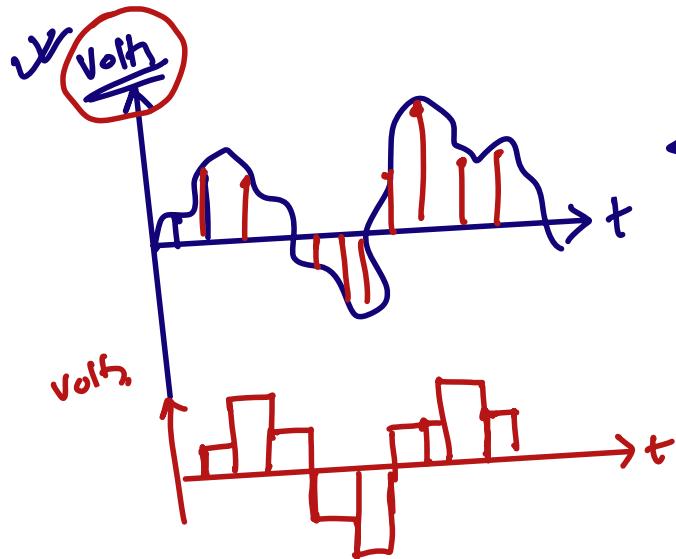


Analog to Digital Converters



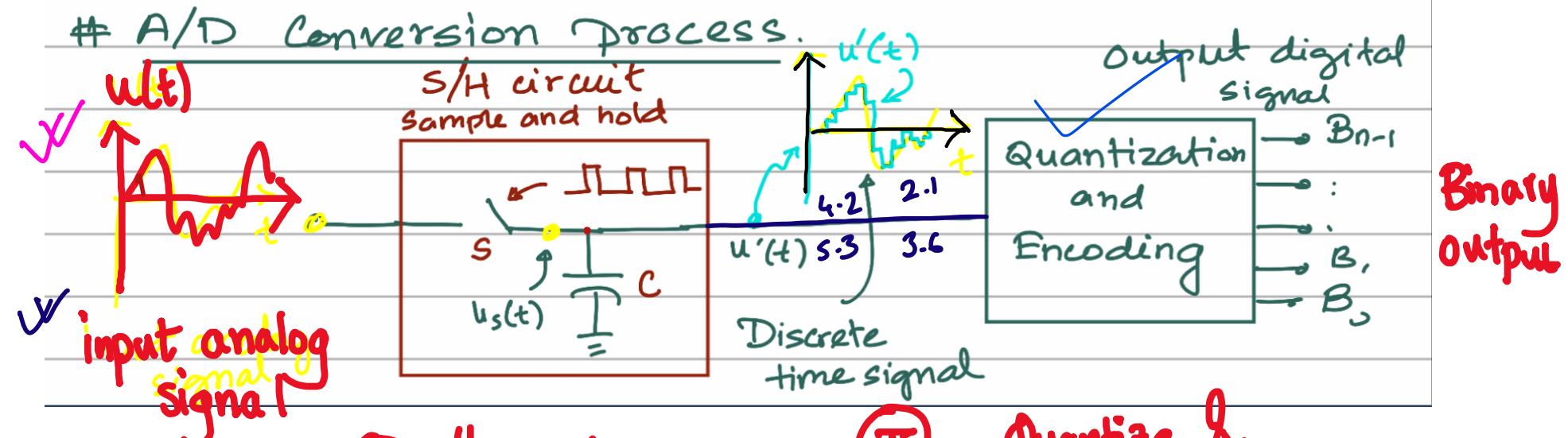
detected by a microphone

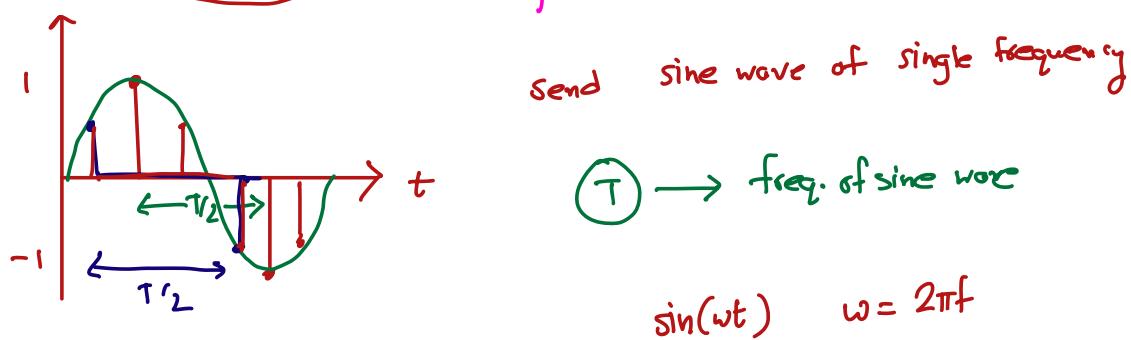
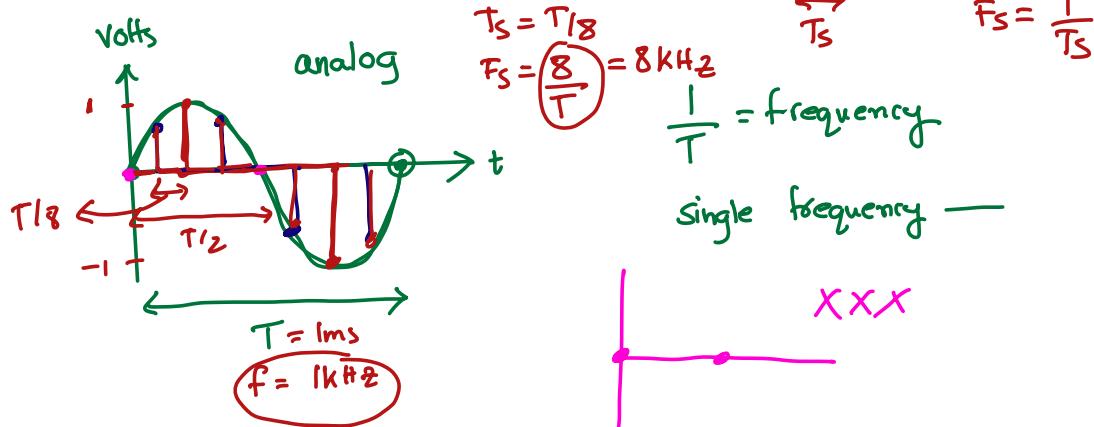
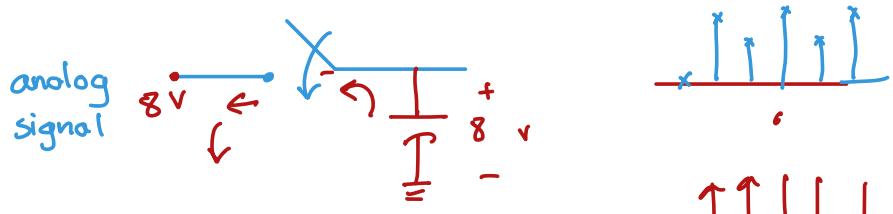
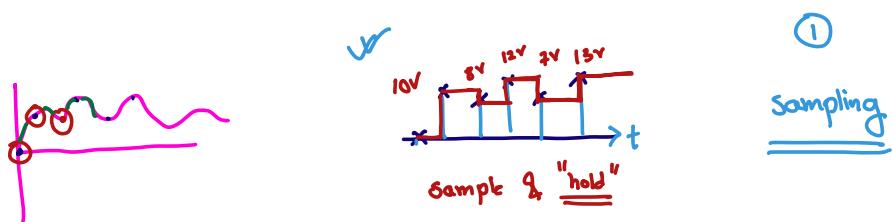
"transducer"

detect an analog signal such as
voice / light \rightsquigarrow electrical signal

Block diagram of the overall process

example: Environment \rightarrow Transducer \rightarrow Computer \rightarrow speaker





Fourier Series / Transform

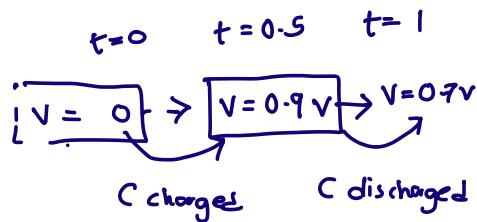
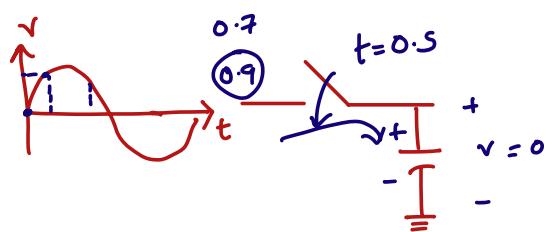
$$\begin{aligned}
 \text{any signal} &= \sum_{i=0}^{\infty} a_i \sin(\omega_i t) + b_i \cos(\omega_i t) \\
 \sqrt{V} \text{ wavy line} &= 3 \sin(3t) + 4 \sin(2t) + 1 \sin(t) \\
 &\quad f = \frac{3}{2\pi} \quad f = \frac{2}{2\pi} \quad f = \frac{1}{2\pi}
 \end{aligned}$$

signal $F_s > 2 \times \underline{f_{\max}}$

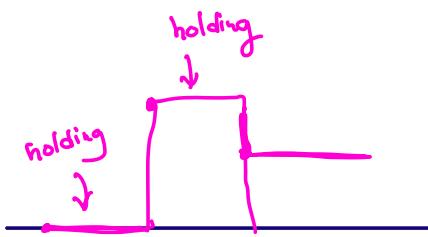
$$f_{\max} = \frac{3}{2\pi} \text{ Hz}$$

$$\boxed{F_s > \frac{6}{2\pi} \text{ Hz}}$$

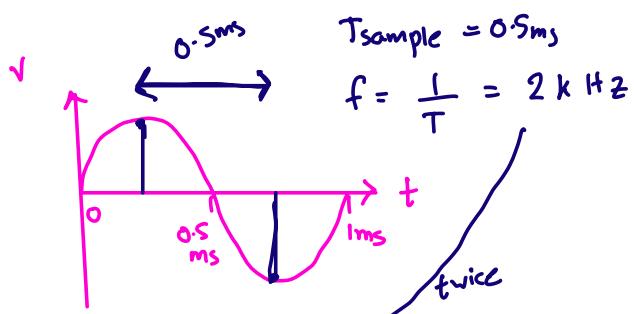
Nyquist theorem: f_{\max} $\underline{F_s \geq 2f_{\max}}$ for complete reconstruction of the signal.



$$0.7 \xrightarrow{\text{RC circuit}} \frac{1}{T} \begin{matrix} + \\ - \end{matrix} \stackrel{0.9 \rightarrow 0.7}{=} \begin{matrix} + \\ - \end{matrix}$$



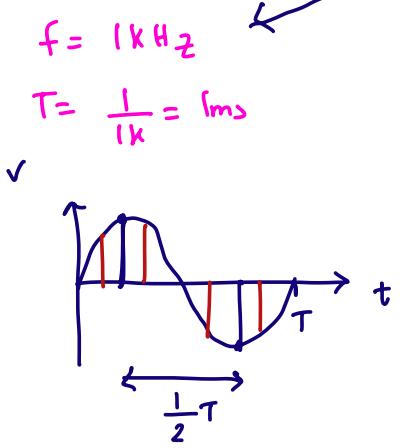
Capacitor to charge / discharge



$$\frac{1}{T_s} = F_s$$

$F_s = \text{sampling frequency}$

1000 kHz



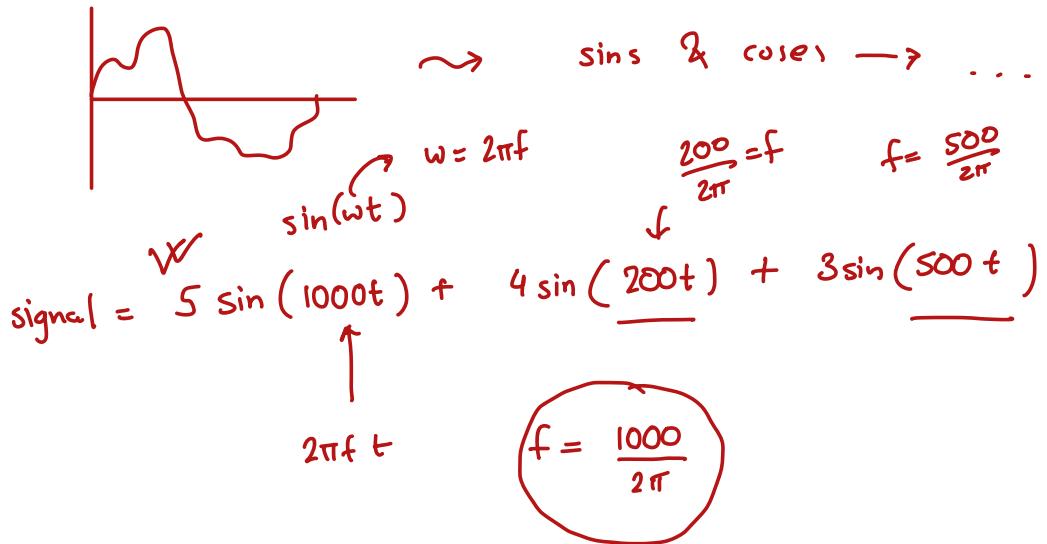
"transmitting a single-tone sine wave!"

only 1 frequency component

Theoretically: Nyquist theorem

Wave of f freq. Sample $2f$ rate for no information loss

$$\text{any signal} = \sum_{i=0}^{\infty} a_i \sin(\omega_i t) + b_i \cos(\nu_i t)$$

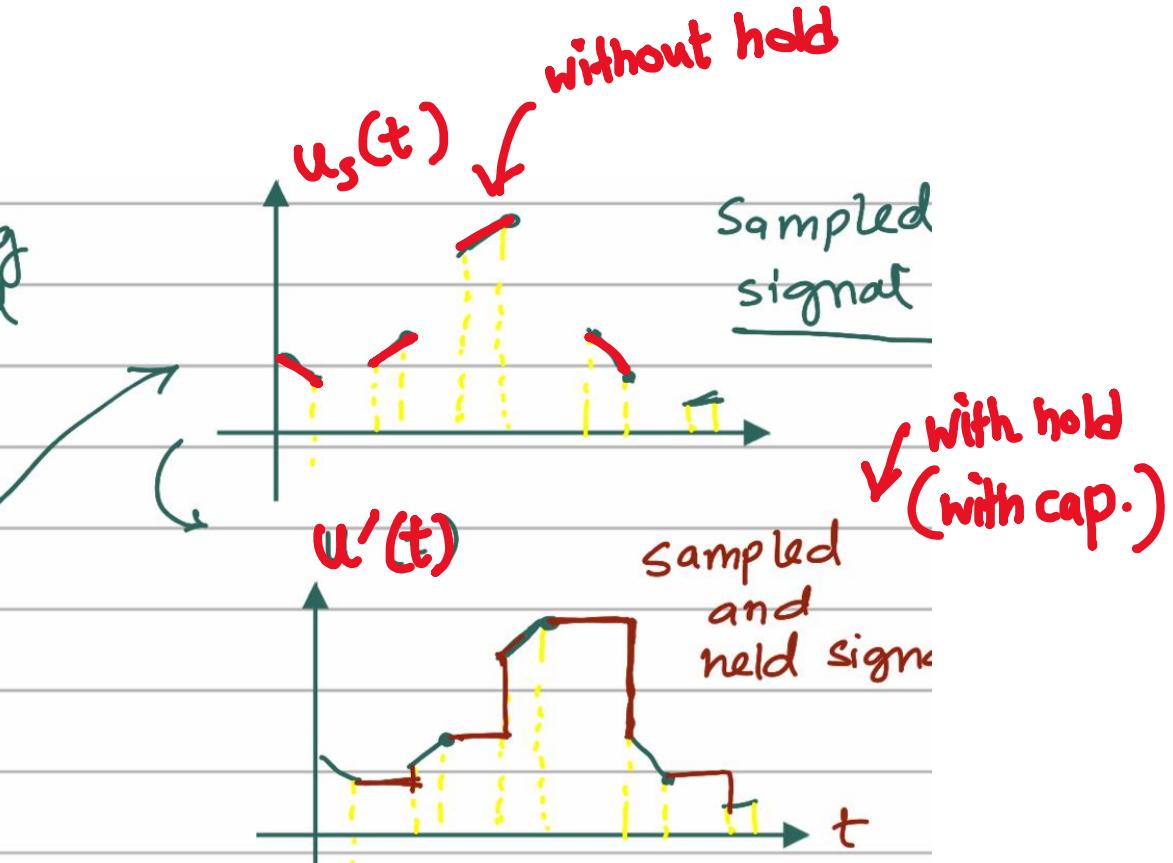
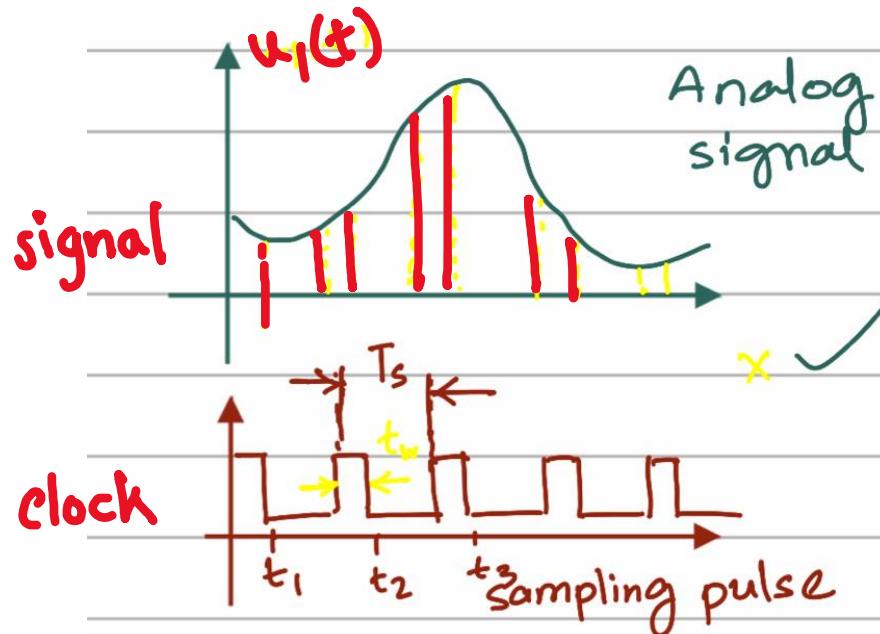


set our sampling rate of $F_s > 2f_{\max}$

in that case all of the sine waves can be reconstructed.

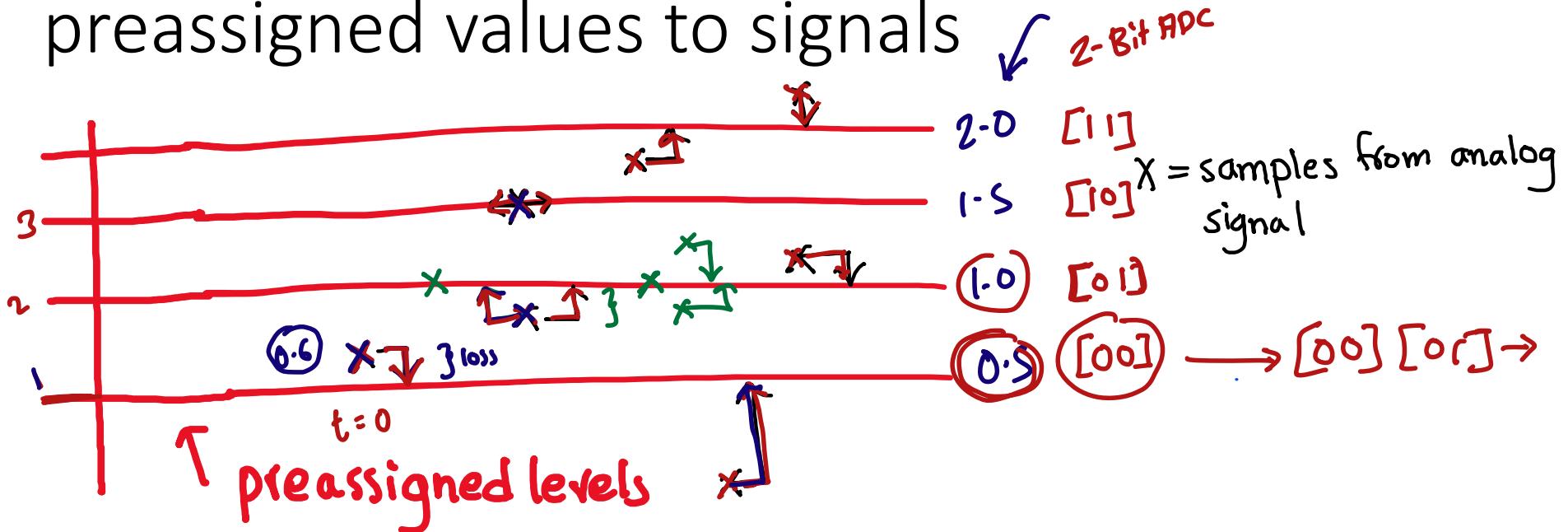
$$\text{signal} = \underset{\text{vv low}}{\text{amp}} \sin(\omega_{\text{vv high}} t)$$

Sample and hold



This hold operation is done using the capacitor
pseudo continuous!

Quantisation: process of assigning fixed preassigned values to signals

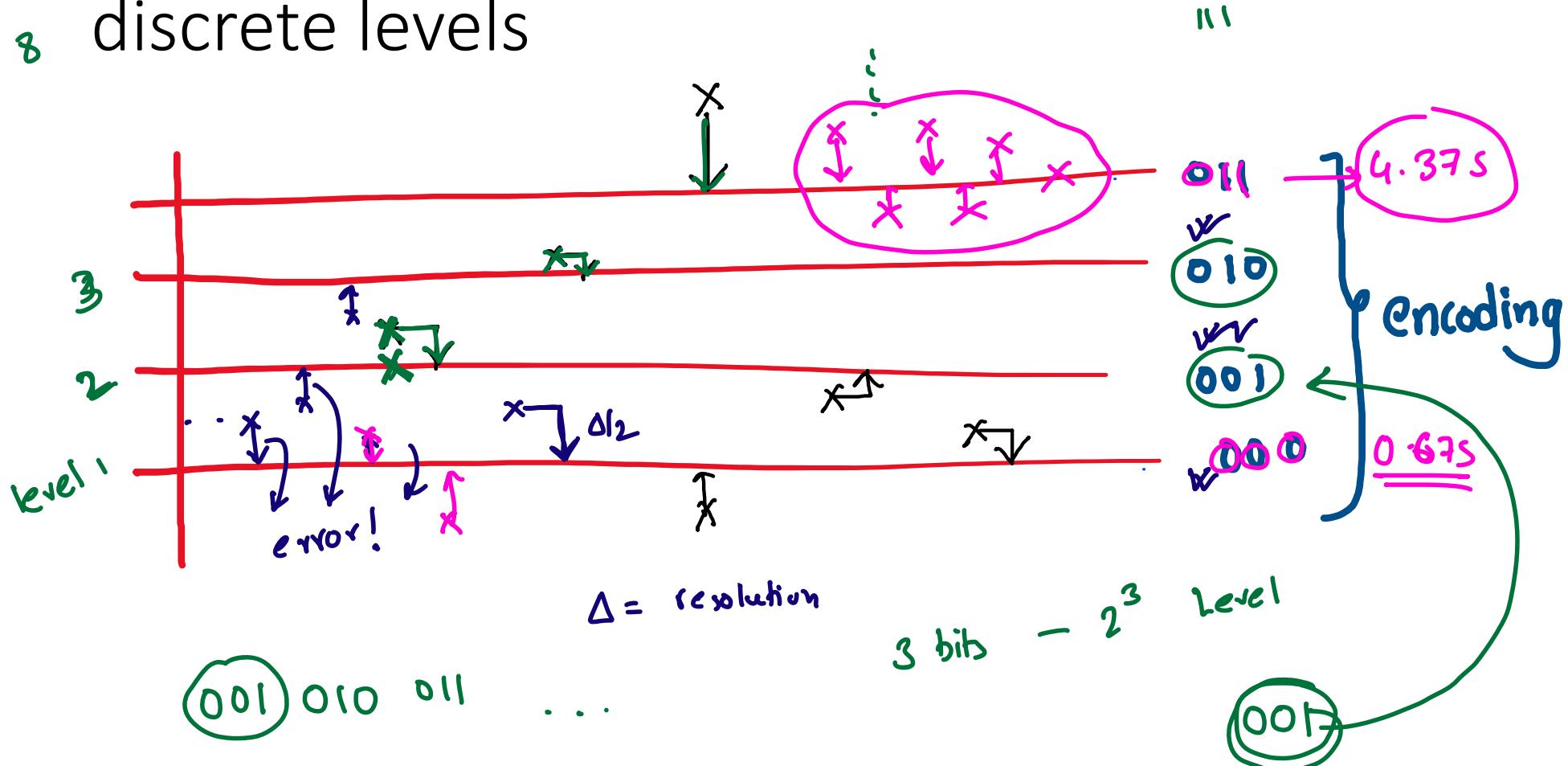


- Mainly 2 types that we will learn
- Mid-rise quantisation and Mid-thread quantisation

"Quantization noise"

Encoding: Binary representations of the discrete levels

8

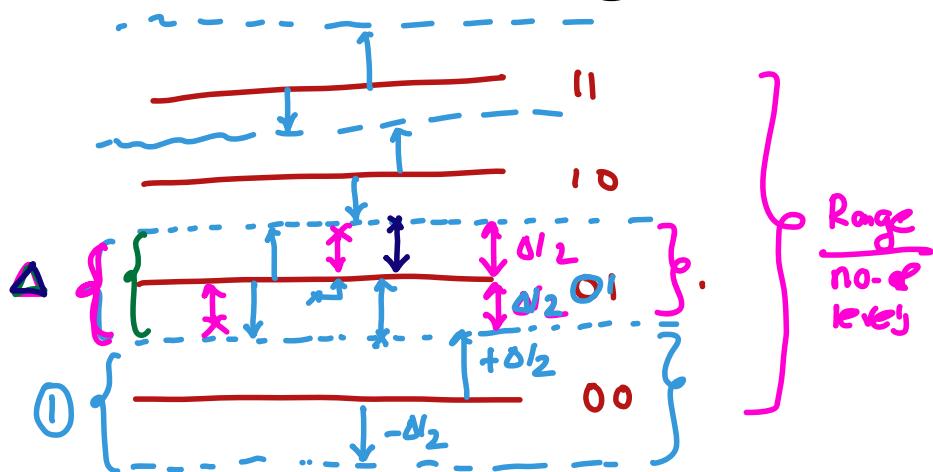


000 001

• • •

111

Closer look at quantisation and encoding



Step 1: know your formulae

[2 bits]	00	3bit	000
	01	:	:
	10		
	11		111
		2^N	

$$\checkmark N = \text{number of bits in the ADC converter} = n$$

$$\checkmark \Delta = \underline{\text{resolution}} = \frac{V_{\max} - V_{\min}}{2^n} \quad \left. \begin{array}{l} \text{analog} \\ \rightarrow \end{array} \right. \frac{10 - 0}{2^n} = \underline{10V}$$

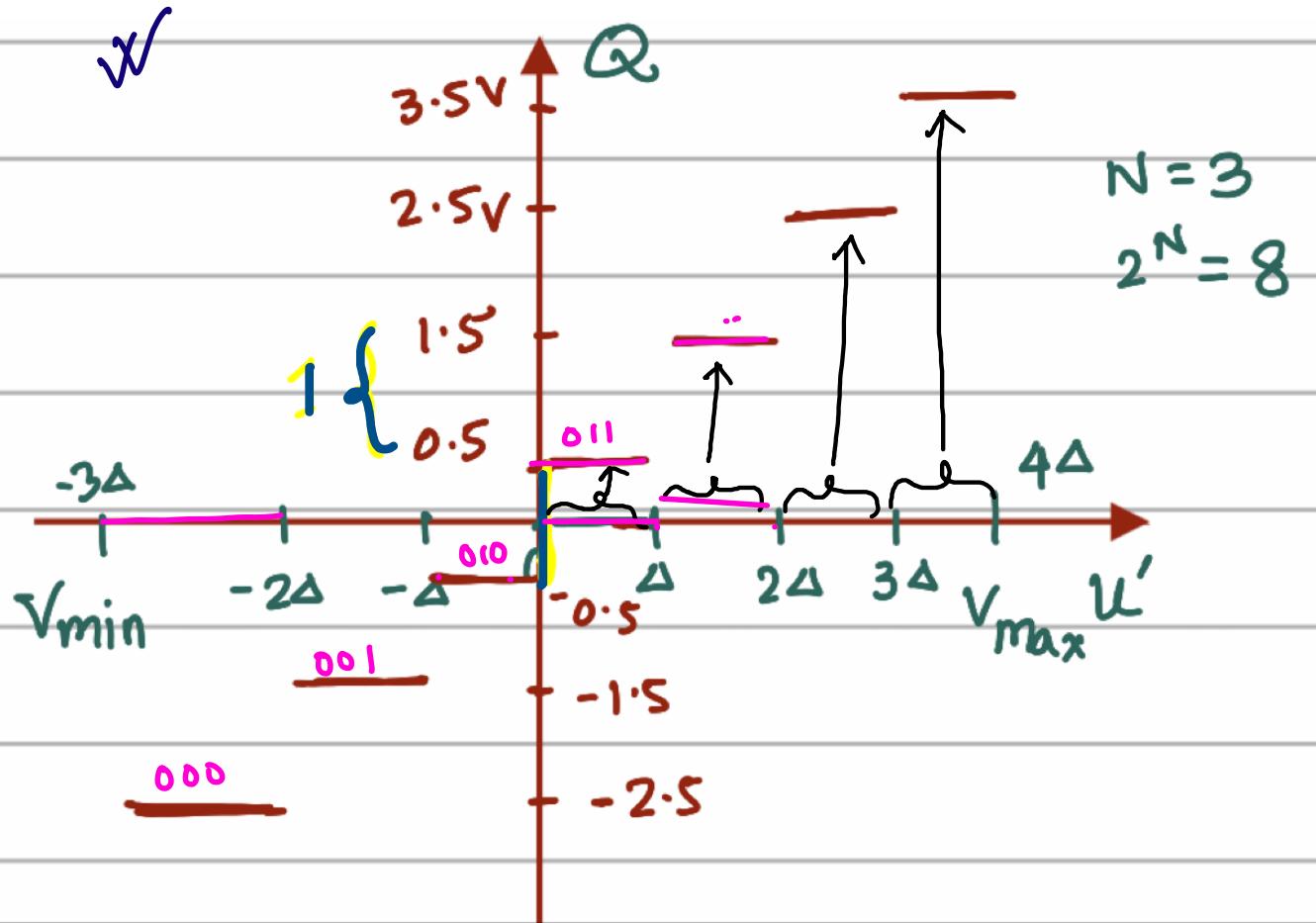
no. of discrete levels 8

difference between adjacent voltage levels

$$2^N = \text{number of levels} \quad \text{max error} = \frac{\Delta}{2}$$

$$V_{\max} / V_{\min} = \text{max/min of analog voltage}$$

Type 1: Mid-rise quantisation



↓ ↓

$N=3$ $2^N = 8$ levels

Sampled values within
1st level
 $0 - \Delta \rightarrow$ 1st level
 $\Delta - 2\Delta \rightarrow$ 2nd level
⋮
so on

Continued...

$N=3$



Let V_{max} & V_{min} of analog signal be 10V & 0V respectively. $V_{max} = 10V$, $V_{min} = 0V$

$$\Delta = \frac{V_{max} - V_{min}}{2^N} = \frac{10}{8} = 1.25 \quad (\text{mid } \cancel{\text{thread}} \text{ rise})$$

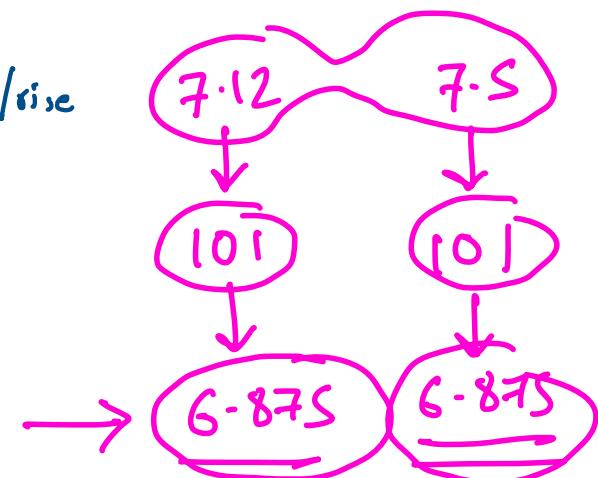
	$0 - \Delta$	$0 - 1.25$	000 ✓	0.625
②	$\Delta - 2\Delta$	$1.25 - 2.5$	001 ✓	1.875
	$2\Delta - 3\Delta$	$2.5 - 3.75$	010 ✓	3.125
				4.375
		$3.75 - 5.0$	011 ✓	5.625
		$5.0 - 6.25$	100 ✓	6.875
		$6.25 - 7.5$	101 ✓	8.125
		$7.5 - 8.75$	110 ✓	9.375
		$8.75 - 10.0$	111 ✓	=

how to quickly identify mid-thread/rise

$$\frac{V_{max} + V_{min}}{2} = \frac{10+0}{2} = 5 \quad \checkmark$$

5 is not a "mid" or quantized level.

\therefore it is mid-rise





analog signal

$$\begin{array}{l} \text{max} = 10 \text{V} \\ \text{min} = 0 \text{V} \end{array}$$

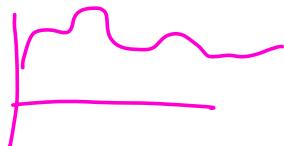
$$\text{range} = 10 - 0 = 10 \text{V}$$

$N = 3$
(ADC)

$$2^3 = 8 \quad (000 \rightarrow 111)$$

$$\Delta = \frac{10 \text{V}}{8 \text{ Level}}$$

$$= \begin{array}{c} 0.625 \\ 1.25 \\ 1.875 \\ 2.5 \end{array}$$



	Range	Range	Range
①	0 - Δ	0 - 1.25	1.875
②	Δ - 2 Δ	1.25 - 2.5	3.125
③	2 Δ - 3 Δ	.	4.375
④	3 Δ - 4 Δ	.	5.625
⑤	4 Δ - 5 Δ	.	6.875
⑥	5 Δ - 6 Δ	.	8.125
⑦	6 Δ - 7 Δ	.	9.375
⑧	7 Δ - 8 Δ	.	10.625

001

2

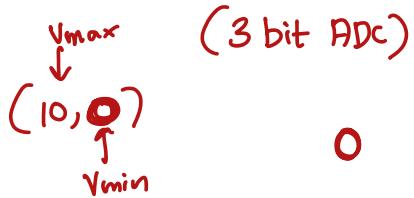
000 111

1.25 - 2.5
1.875

$$N = 3$$

analog $\Rightarrow V_{\max}, V_{\min}$

$$\Delta = \frac{10 - 0}{2^3} = \frac{10}{8} = 1.25$$



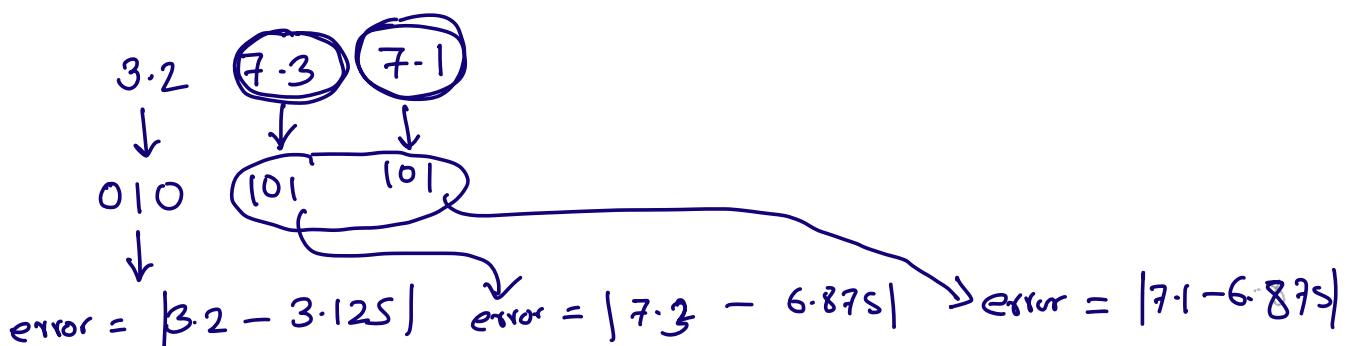
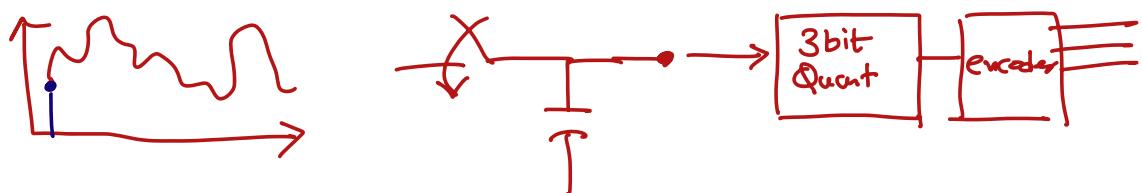
(Quantized level)

midpoint (v) encoding

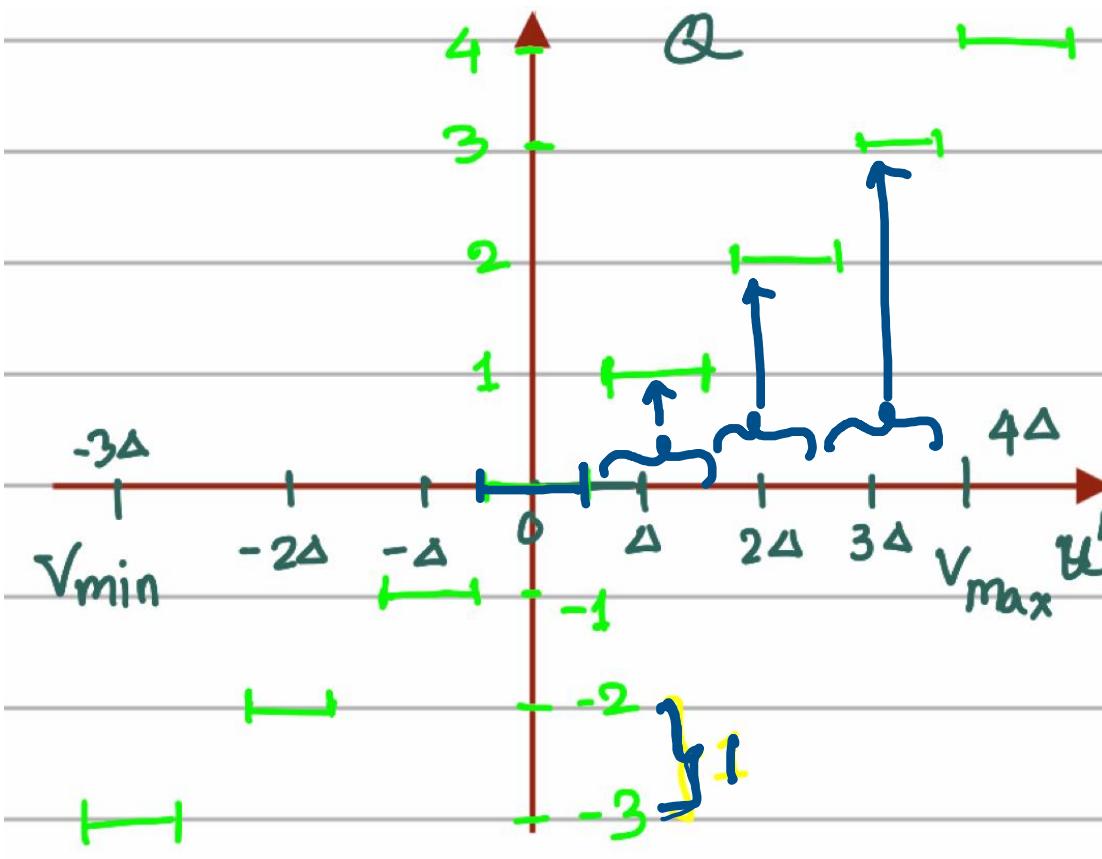
	Range	Range (v)	midpoint (v)	encoding
①	$0 - 0 + \Delta$	$0 - 1.25$	0.625	000
②	$\Delta - 2\Delta$	$1.25 - 2.5$	1.875	001
③	$2\Delta - 3\Delta$	$2.5 - 3.75$	3.125	010
④	$3\Delta - 4\Delta$	$3.75 - 5.0$	4.375	011
⑤	$4\Delta - 5\Delta$	$5.0 - 6.25$	5.625	100
⑥	$5\Delta - 6\Delta$	$6.25 - 7.5$	6.875	101
⑦	$6\Delta - 7\Delta$	$7.5 - 8.75$	8.125	110
⑧	$7\Delta - 8\Delta$	$8.75 - 10.0$	9.375	111

$$\frac{V_{\max} + V_{\min}}{2} = \frac{10 + 0}{2}$$

Mid - Rize



Type 2: Mid-thread quantisation level



$$-\frac{\Delta}{2} - +\frac{\Delta}{2} = 1^{\text{st}} \text{ level!}$$

$$+\frac{\Delta}{2} - +\frac{3\Delta}{2} = 2^{\text{nd}} \text{ level!}$$

$$\frac{3\Delta}{2} : \frac{5\Delta}{2} = 3^{\text{rd}} \text{ level!}$$

p^{th} level!

$$\left(V_{\min} - \frac{\Delta}{2}\right) — \left(V_{\min} - \frac{\Delta}{2}\right) + \Delta$$

$$V_{\min} = 0 \quad N = 3 \text{ bit}$$

$$V_{\max} = 10$$

Mid-thread!

Range

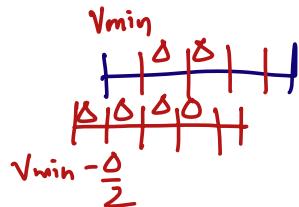
$$\left(0 - \frac{\Delta}{2}\right) — \left(0 - \frac{\Delta}{2}\right) + \Delta$$

$$\textcircled{1} = -\frac{\Delta}{2} — + \frac{\Delta}{2}$$

$$\textcircled{2} \quad \left(\frac{\Delta}{2}\right) — \left(\frac{3\Delta}{2}\right) = \frac{3\Delta}{2} - \frac{\Delta}{2} = \Delta$$

$$\textcircled{3} \quad \frac{3\Delta}{2} — \dots \frac{3\Delta}{2} + \Delta = \frac{5\Delta}{2}$$

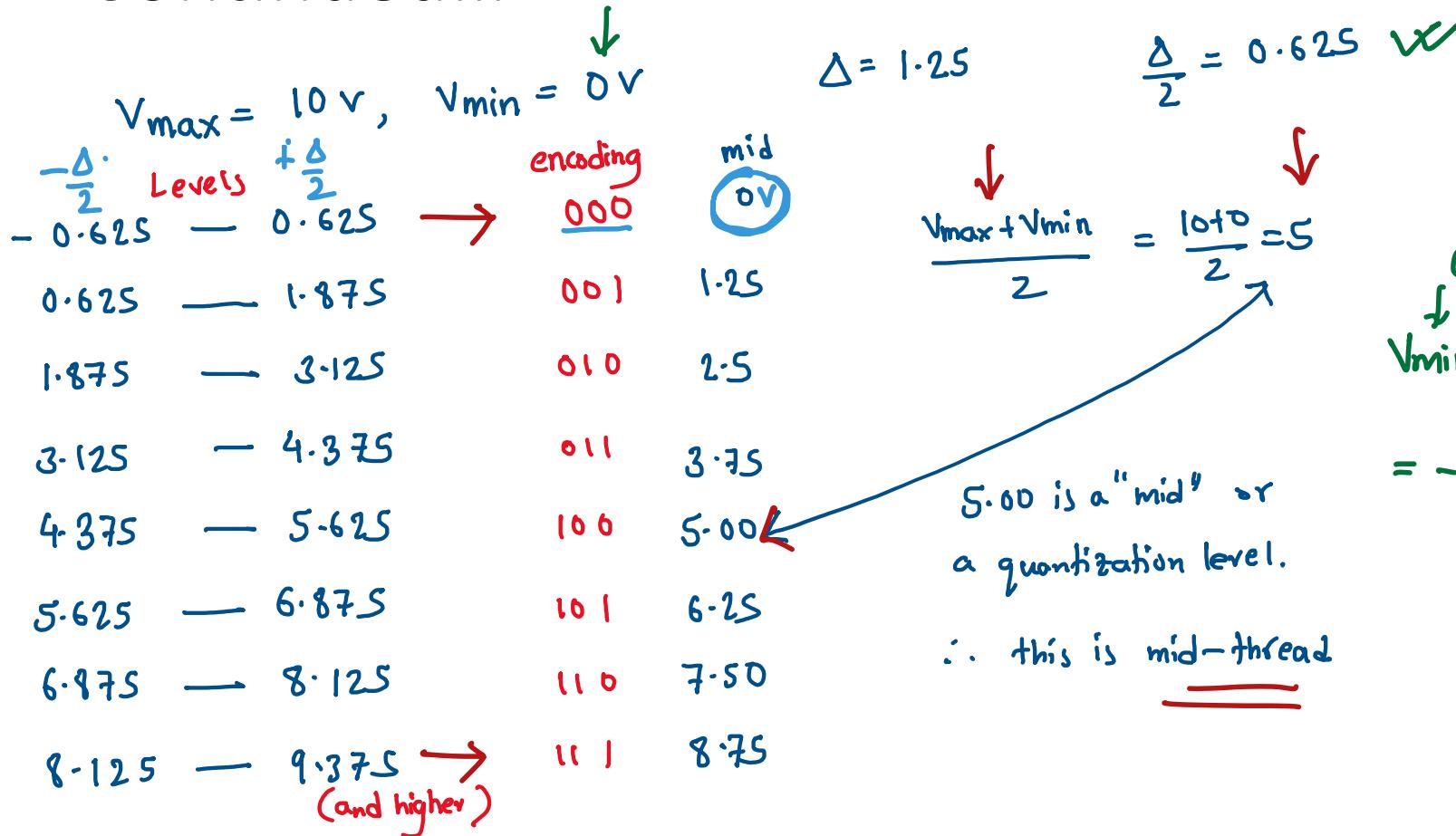
$$\frac{5\Delta}{2} — \frac{5\Delta}{2} + \Delta = \frac{7\Delta}{2}$$



Continued...

3-bit ADC

$$\Delta = \frac{V_{\max} - V_{\min}}{2^N} = \frac{10 - 0}{2^3} = 1.25$$



PRO

ADVANTAGE ?!

Mid-thread vs Mid-Rise?

DISADVANTAGES ?!

CON

Loss of information happen in A/D converters? Which stage is responsible?



- Understanding the analog infatuation!



Hardware 1: Flash A/D converter

$$N = 3, 2^N = 8$$

Midrise quantization:



$V_+ > V_-$, $V_o = \text{High}$

$V_+ < V_-$, $V_o = \text{Low}$

$$V_{ref}^+ = 9.375 \text{ V}$$

$$V_{ref}^- = -0.675 \text{ V}$$

$$I = \frac{V_{ref}^+ - V_{ref}^-}{8R} = \frac{10}{8R}$$

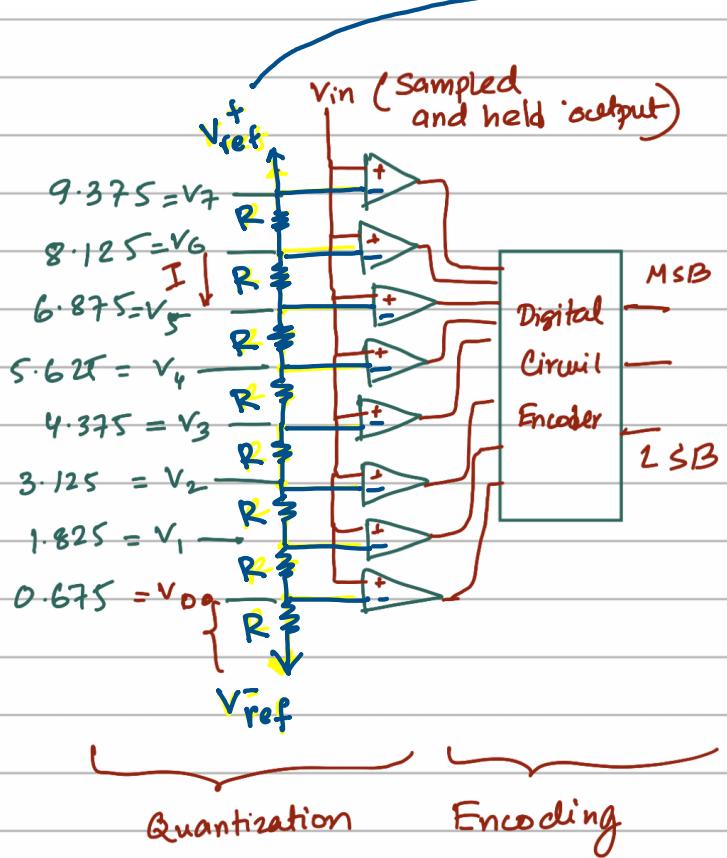
$$IR = V_o - V_{ref}^-$$

$$\Rightarrow V_o = V_{ref}^- + IR$$

$$= -0.675 + \frac{10}{8}$$

$$= 0.675$$

$$V_1 = V_o + IR = 1.825$$



mid values = quantized level values

Properties:

- fast: one clk cycle required to convert analog - digital data
- Requires a lot of component



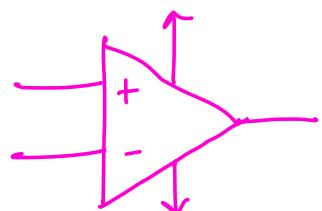
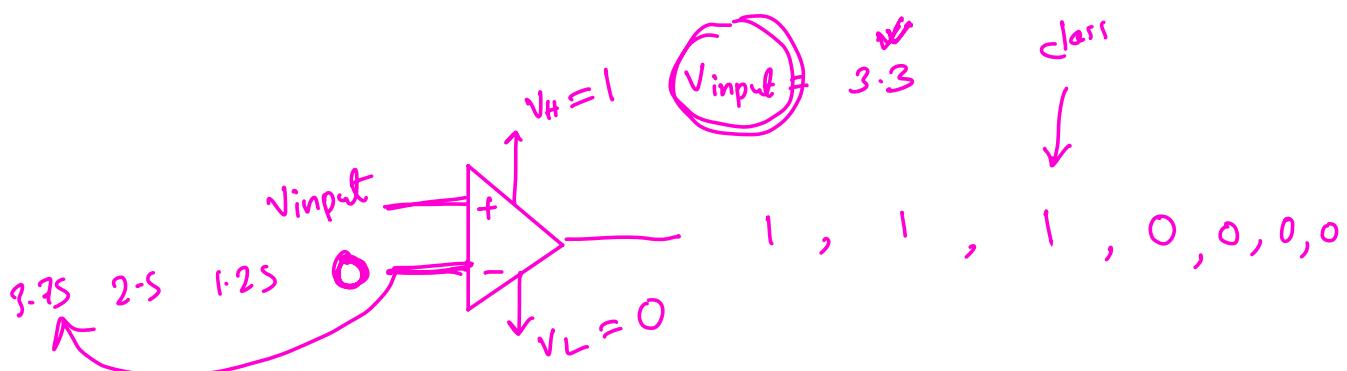
$$V_+ > V_- \quad V_H$$

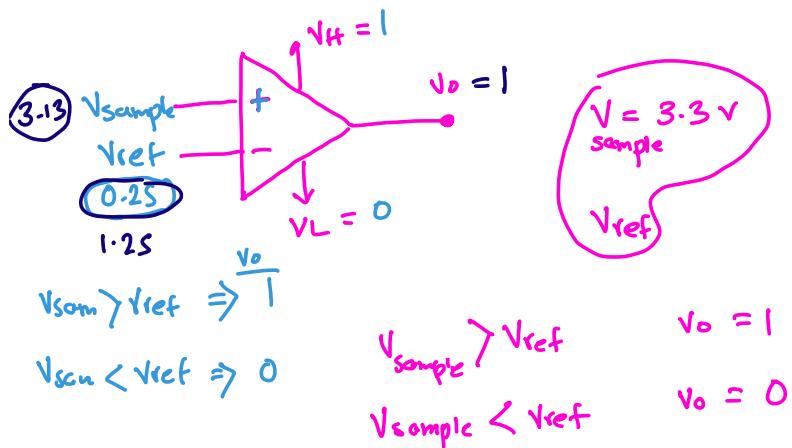
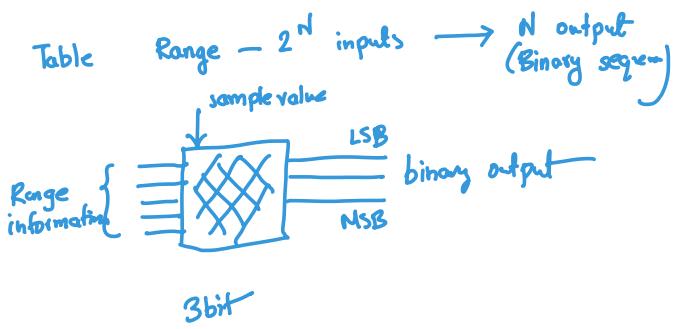
$$\frac{V_o}{V_H} = \begin{cases} 1 & V_+ > V_- \\ 0 & V_- > V_+ \end{cases}$$

Range (V)	midpoint (v)	encoding		
0 - 1.25	0.625	000 H	1.	1 ✓
1.25 - 2.5	1.875	001 H	1.	1 ✓
2.5 - 3.75	3.125	010 H	1.	1 ✓
3.75 - 5.0	4.375	011 L	1.	0 X
5.0 - 6.25	5.625	100 L	0	0
6.25 - 7.5	6.875	101 L	0	0
7.5 - 8.75	8.125	110 L	0	0
8.75 - 10.0	9.375	111 L	0	0

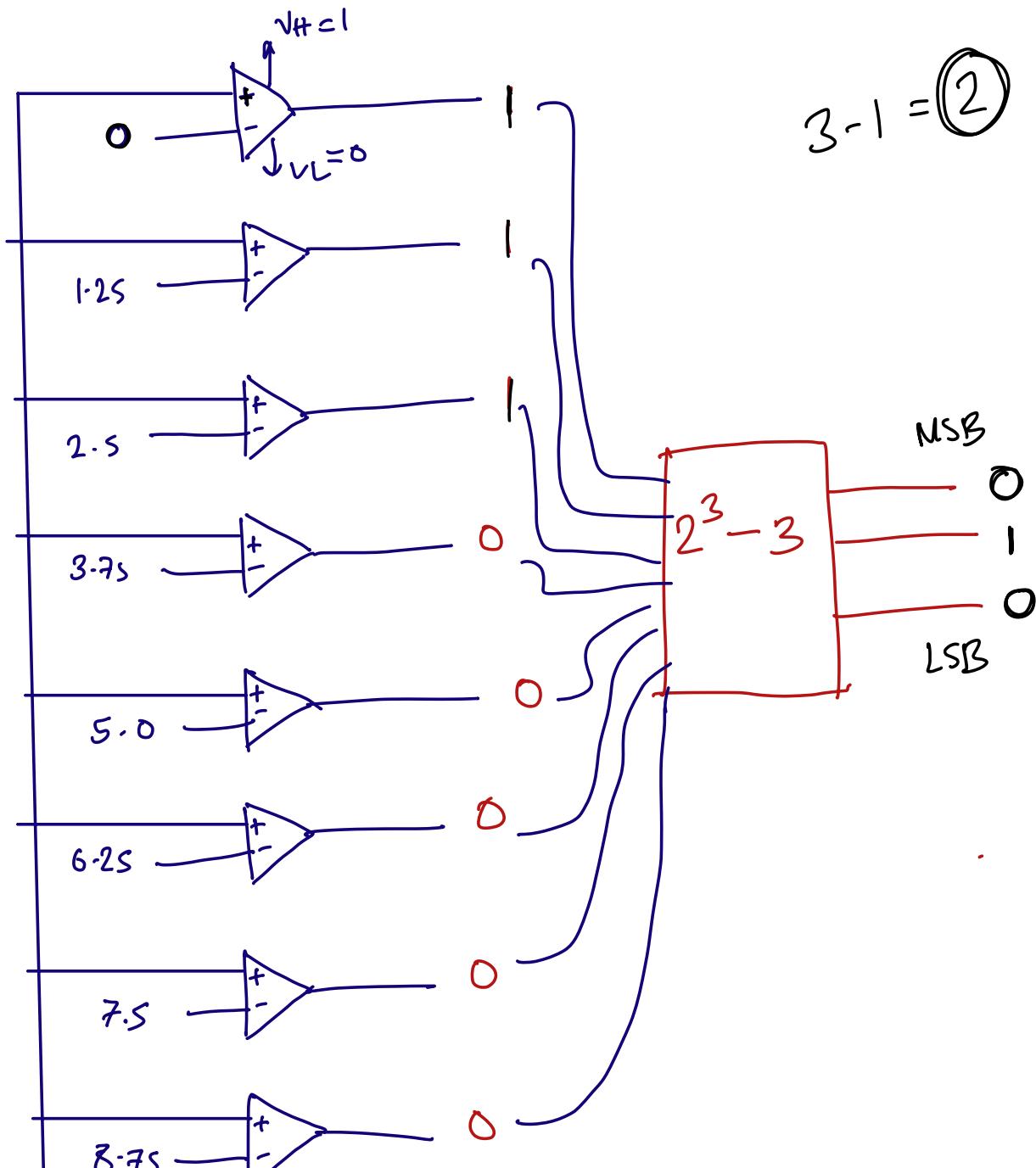
↓ ↓

1. 1 ✓
1. 1 ✓
1. 1 ✓
1. 0 X
0. 0
0. 0
0. 0





$V_H = 1, V_L = 0$ for all comparators



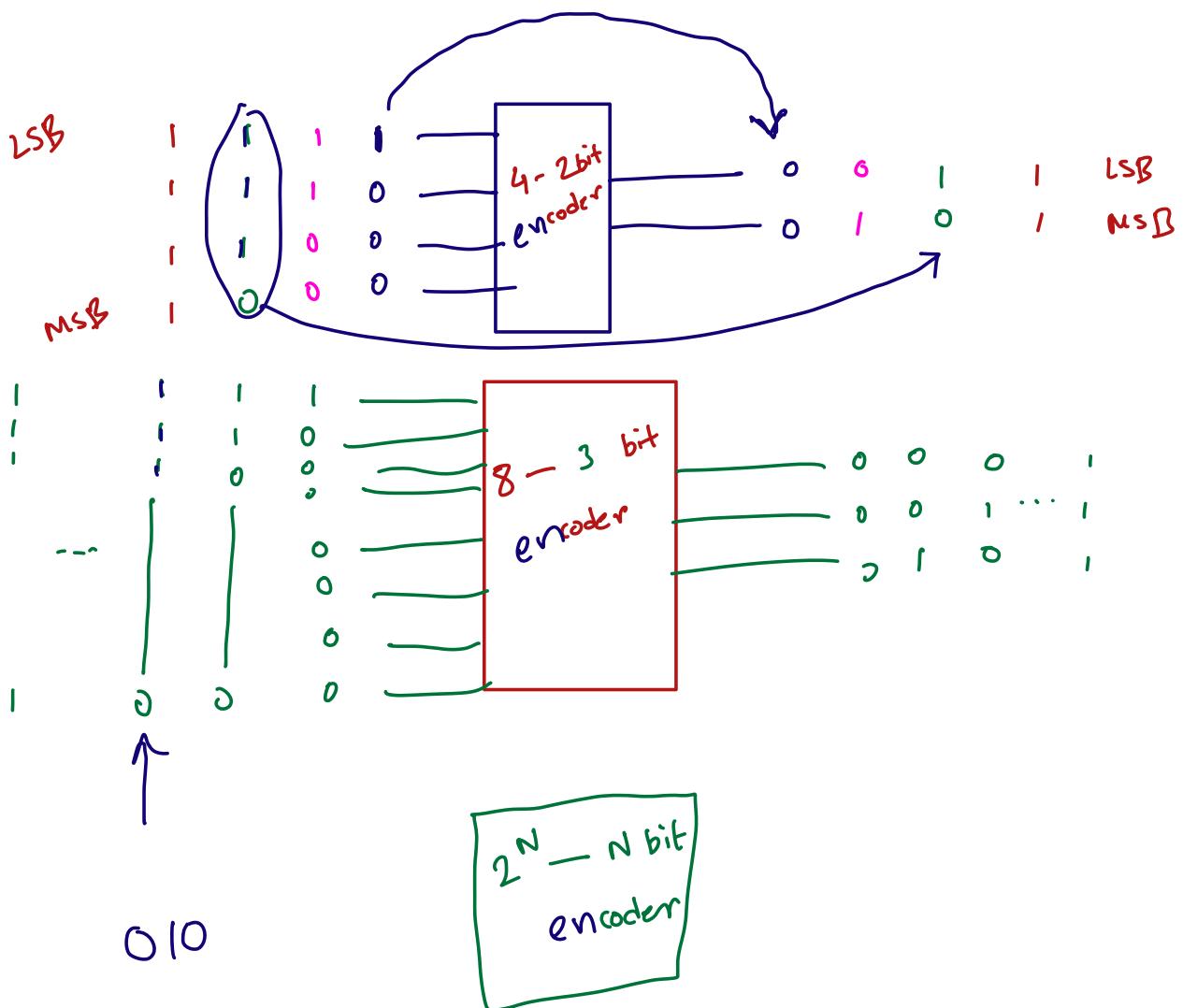
$$V_{\text{sample}} = \underline{\underline{3.13 \text{ V}}}$$

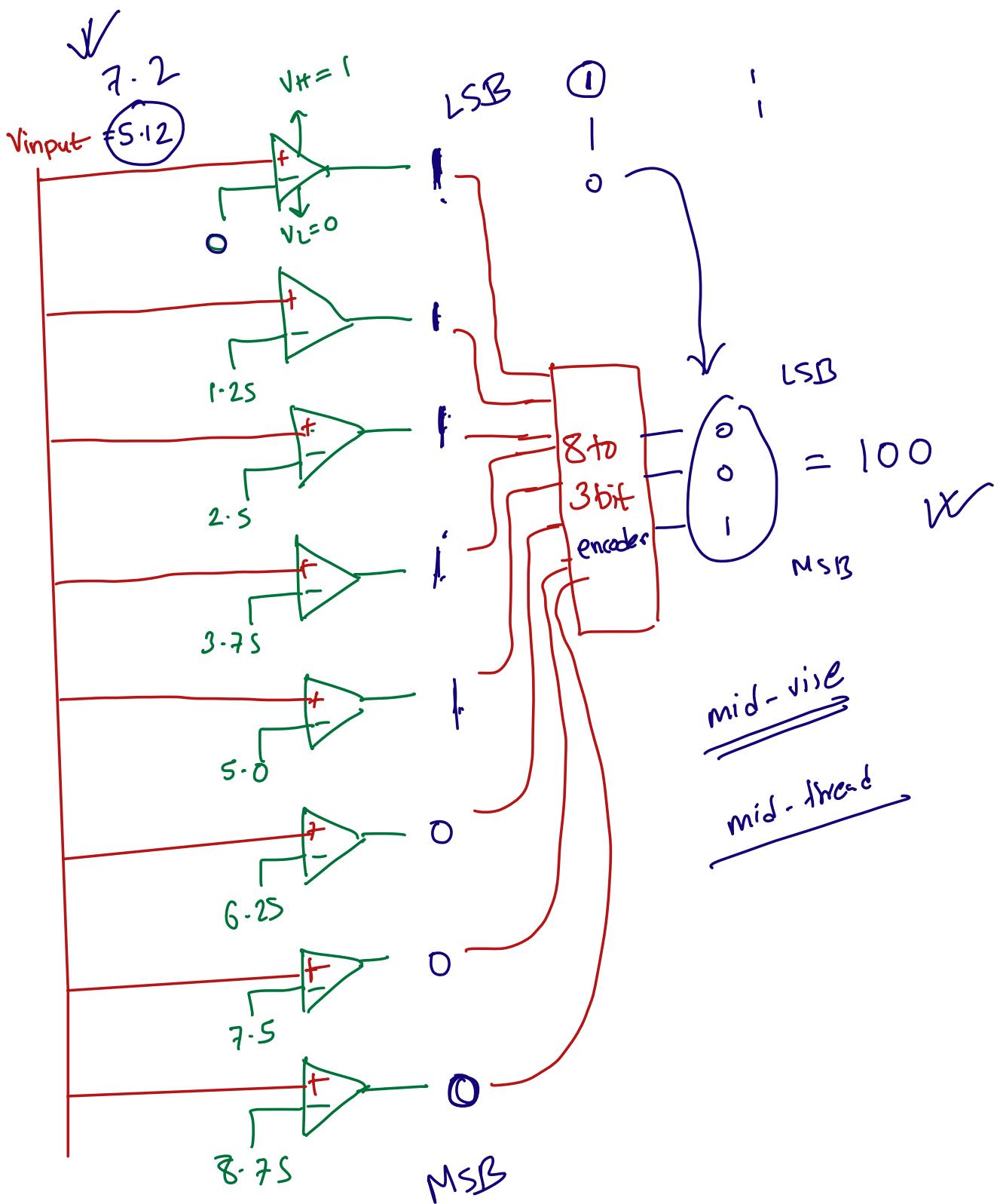
$$3-1 = \textcircled{2}$$

Truth table

encoder

<u>00000000</u>	w	↓	x xx
10000000	0	$(1-p)=0$	000 w
11000000			001 w
11100000	$(3-1)=2$		010
⋮			
<u>11111111</u>			111



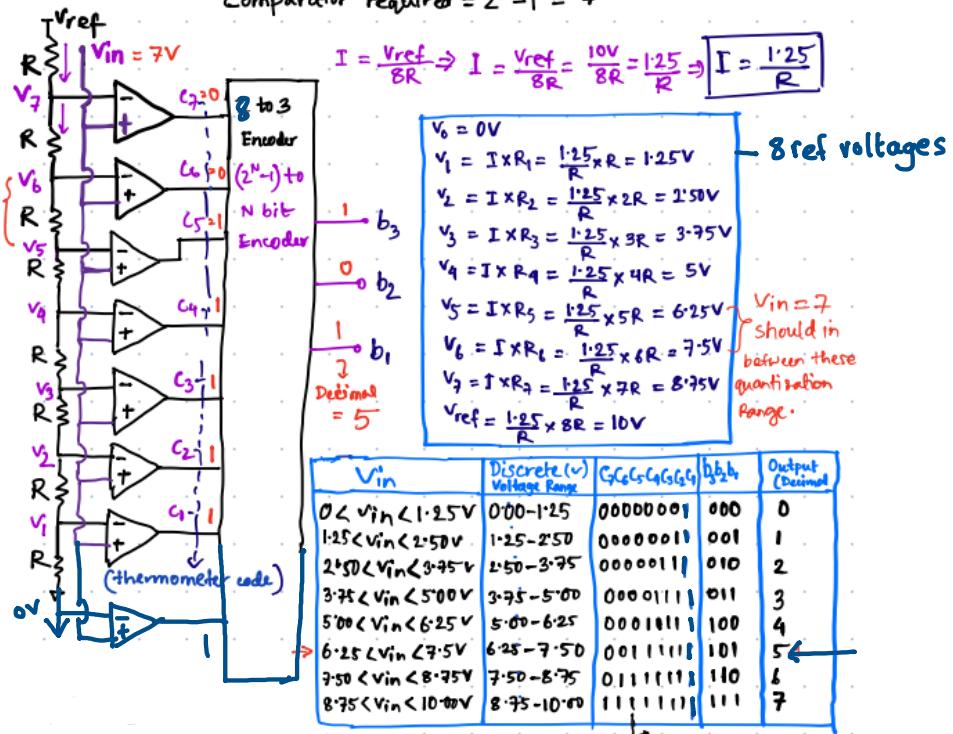


Design a 3-bit Flash ADC. Given Vin = 7V and V-ref = 10V

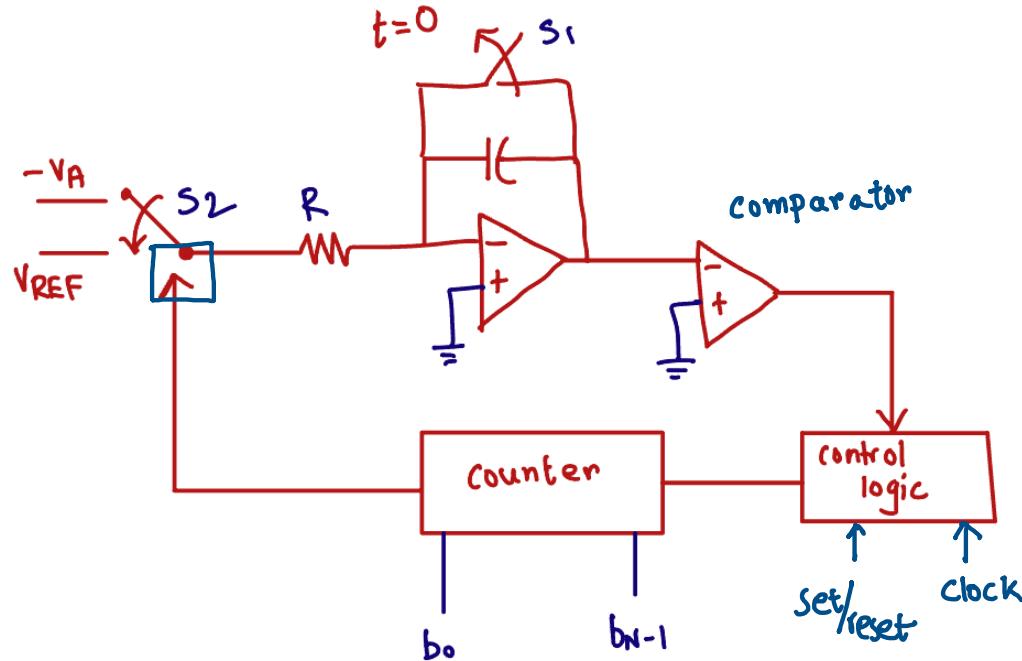
Design a 3-bit Flash ADC. Find the resistor and comparator required by the ADC. Given, Vin = 7V and Vref = 10V

Solution N = 3; Resistor required = $2^N = 2^3 = 8$

Comparator required = $2^3 - 1 = 7$



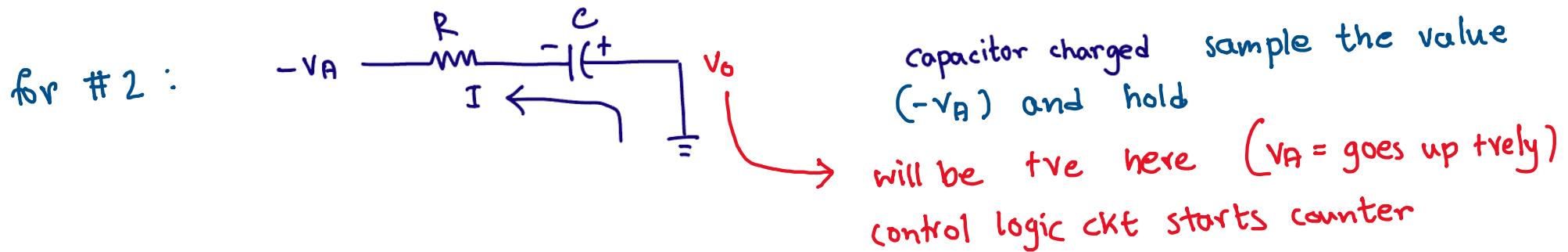
Hardware 2: Dual slope A/D converter



Continued...

#1: $t < 0$, S_1 closed, S_2 open

#2: $t_1 = 0$, S_1 open, $S_2 \rightarrow -V_A$ sample and hold

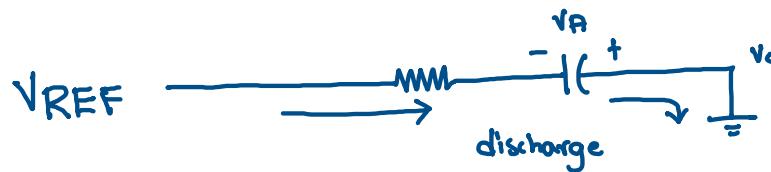


Counter counts $0 - 2^N - 1$

3: Once counting finished \rightarrow ① $S_2 \rightarrow V_{ref}$

② Capacitor discharges

③ V_o declines



moment of switching
ie. S_2 changes
position...

$$V_C = V_A \\ V_A > V_{REF}$$

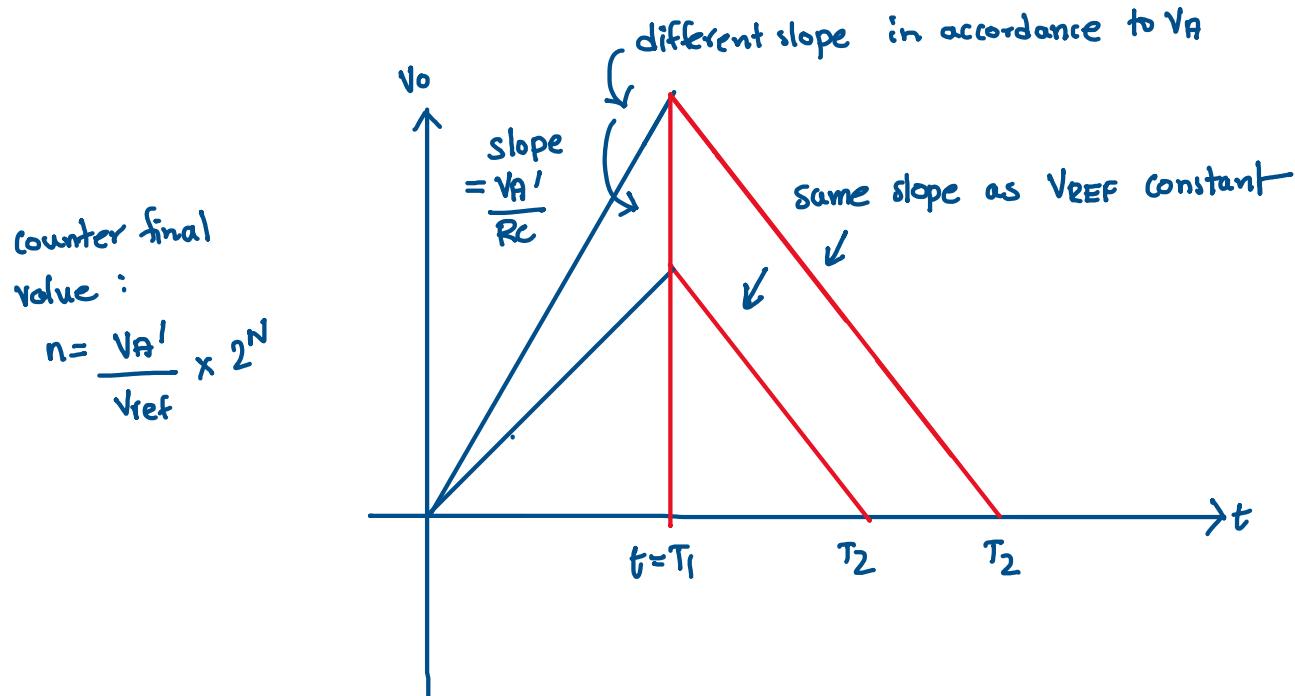
V_o starts to decrease
until it reaches V_{REF}

#4: when V_o decrease to a negative value at $t = T_2$, V_o goes to a
negative value ...

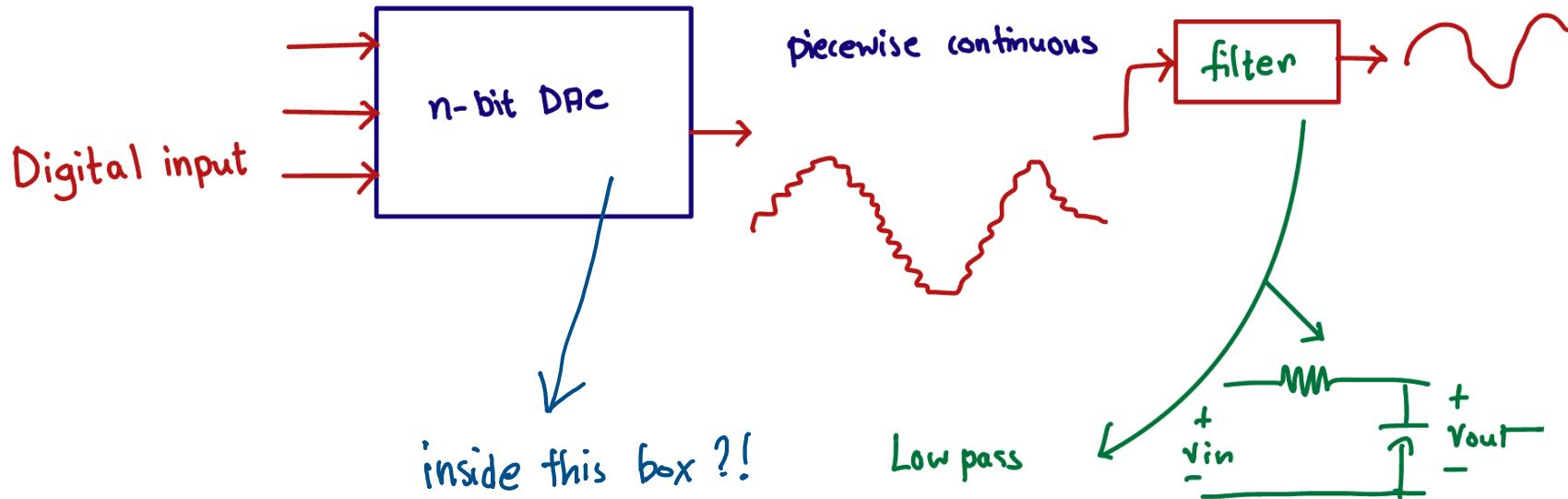
↓
comparator gives high output to control logic ckt and freezes
counter.

#5: this frozen binary value is our digital output.

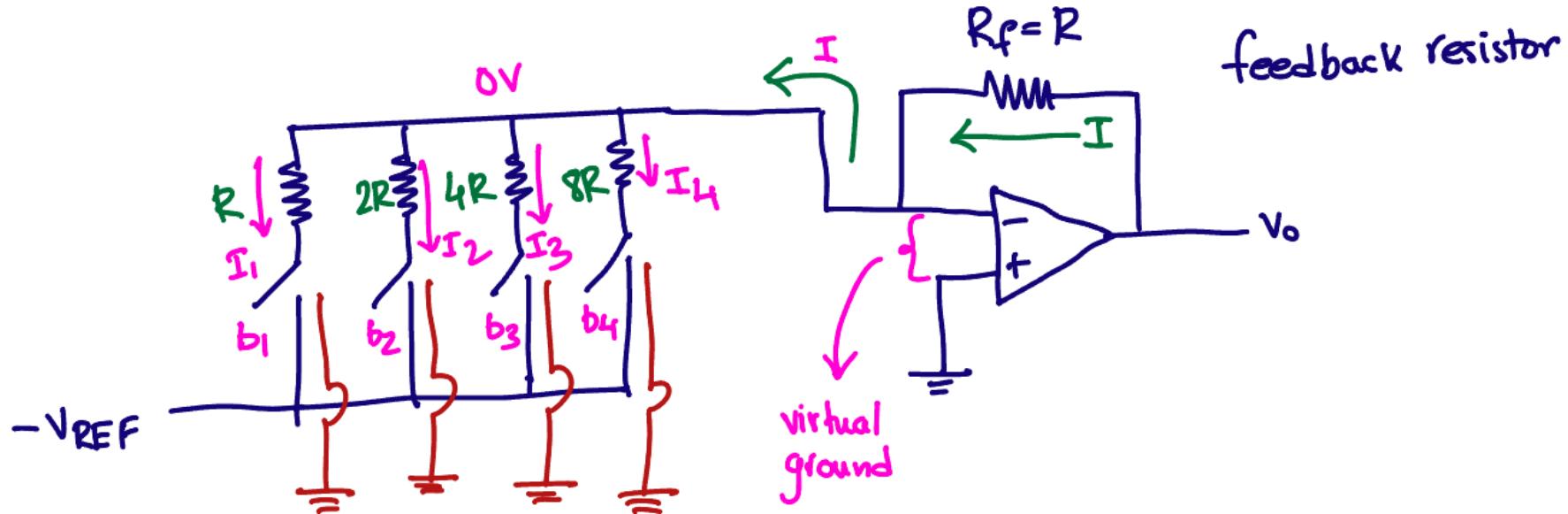
Graphically: Dual Slope ADC



Digital to analog converter



Binary Weighted Resistor



$$I = I_1 + I_2 + I_3 + I_4$$

$$I = \frac{V_o - 0}{R}$$

$$I_1 = \frac{0 - V_{ref}}{R} \\ (b_1 = 1)$$

OR
depending
on switch
position

$$= \frac{0}{R} \\ (b_1 = 0)$$

$$\left. \begin{array}{l} I_1 = b_1 \frac{V_{ref}}{R} \\ \end{array} \right\}$$

if $b_1 = 1$ switch S_1 is connected to $-V_{REF}$.
if $b_1 = 0$ " S_1 " " 0V.

Similarly $I_2 = \frac{0 - (-V_{REF})}{2R}$ if $b_2 = 1$ or $I_2 = 0$ if $b_2 = 0$

$$\therefore I_2 = b_2 \frac{V_{ref}}{2R}$$

$$\dots I_3 = b_3 \frac{V_{ref}}{4R} \dots$$

$$I = \sum_{i=1}^n I_i = \frac{V_o}{R} = b_1 \frac{V_{ref}}{R} + b_2 \frac{V_{ref}}{2R} + \dots$$

$$V_o = V_{ref} \left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right)$$

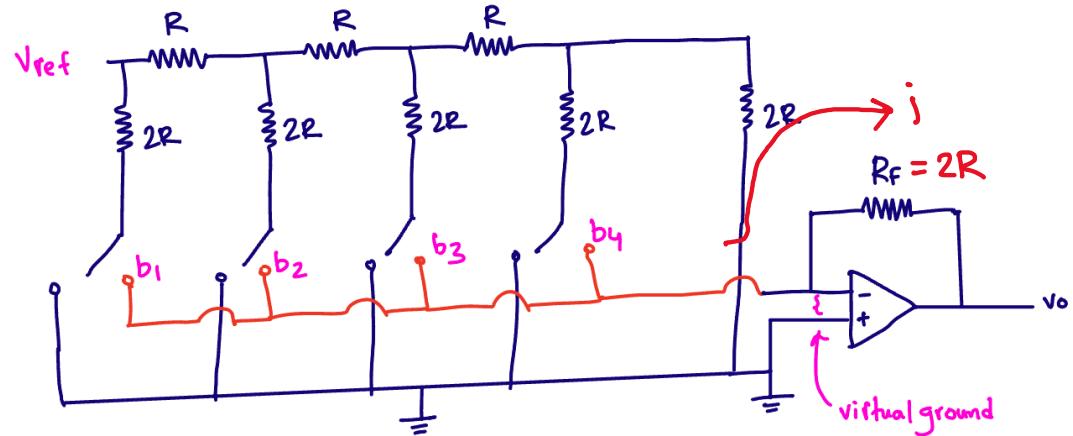
∴ if $b_n = 1010$

$$V_o = V_{ref} \left(1 + \frac{0}{2} + \frac{1}{4} + \frac{0}{8} \right)$$

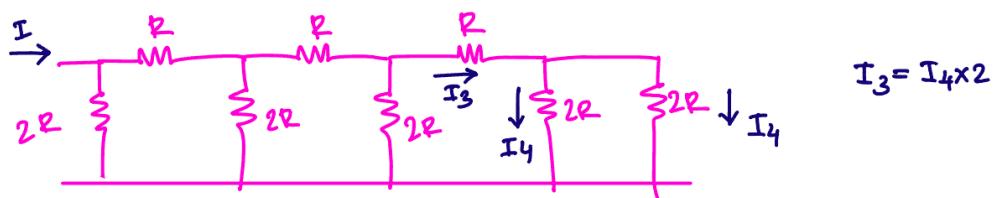
$$V_o = 16 \left(1 + \frac{1}{4} \right) = 20 \quad \left\{ \text{e.g. } V_{ref} = 16 \right\}$$

problem: making exact valued resistors
often multiple series-parallel connections necessary.

R-2R Ladder

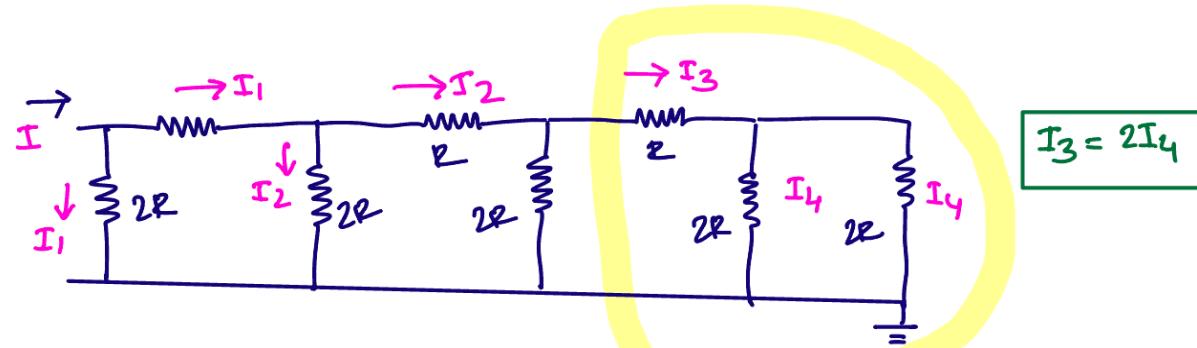


Wherever switch stays same ckt is maintained as the switch always provides connection to (-ve) / (+ve) terminal of op-amp \rightarrow virtual ground.

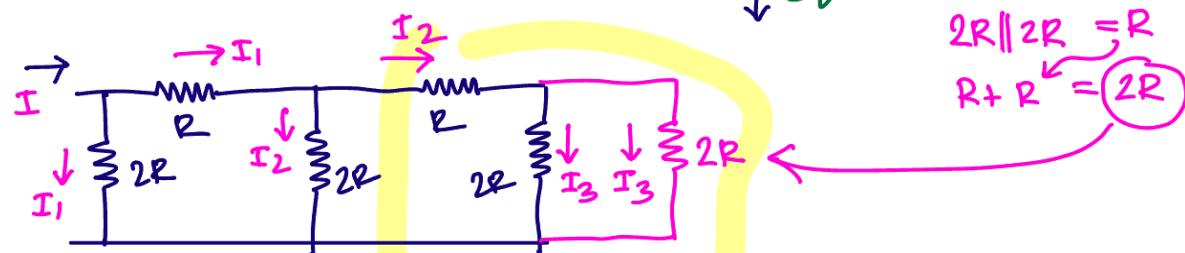


XX difference betw 2 connections
when switch connects (-ve) port \rightarrow current can flow

A simple trick



$$I_3 = 2I_4$$

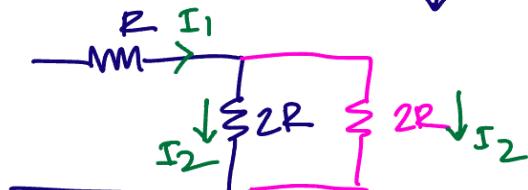


$$I_2 = 2I_3$$

$$2R \parallel 2R = R$$

$$R + R = 2R$$

again



$$I_1 = 2I_2$$

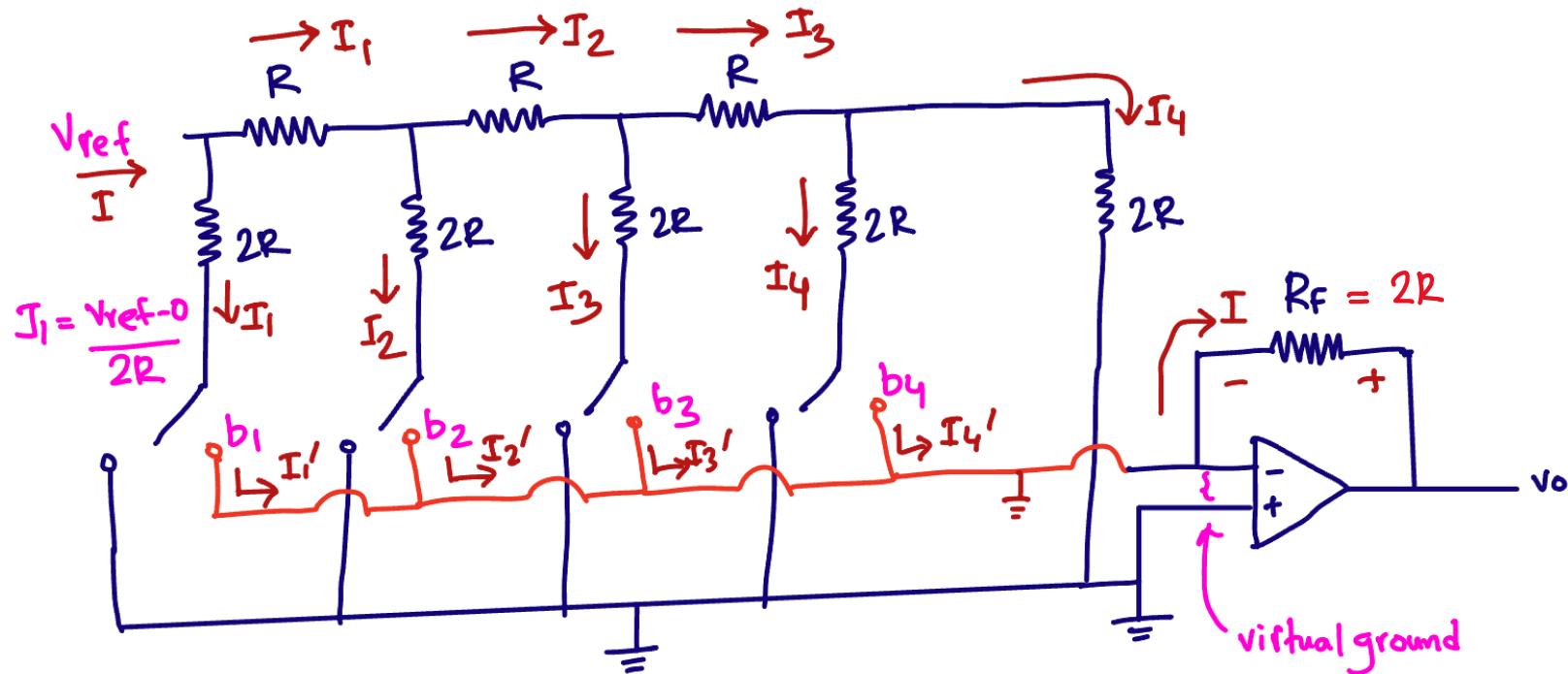
∴ we find that

$$I_1 = \frac{I}{2}$$

$$I_2 = \frac{I_1}{2} = \frac{I}{4}$$

$$I_3 = \frac{I_2}{2} = \frac{I}{8}$$

$$I_4 = \frac{I_3}{2} = \frac{I}{16}$$



$$I = \frac{0 - V_o}{R_F} = \frac{V_o}{R_F}, \quad I_1' = b_1 I_1 \quad \left(\begin{array}{l} \text{if } b_1=0, I_1'=0 \\ b_1=1, I_1'=I_1 \end{array} \right)$$

$$I_2' = b_2 I_2 \quad I_3' = b_3 I_3 \quad I_4' = b_4 I_4$$

$$I = b_1 \frac{V_{ref}}{2R} + b_2 \frac{V_{ref}}{4R} + b_3 \frac{V_{ref}}{8R} + b_4 \frac{V_{ref}}{16R} = \frac{-V_o}{R_F}$$

$$V_o = (-V_{ref}) \left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right) \quad (R_F = 2R)$$