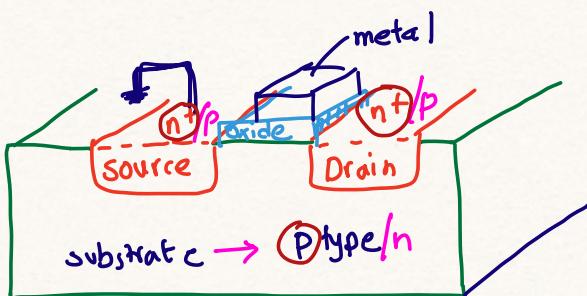


## Mos logic family

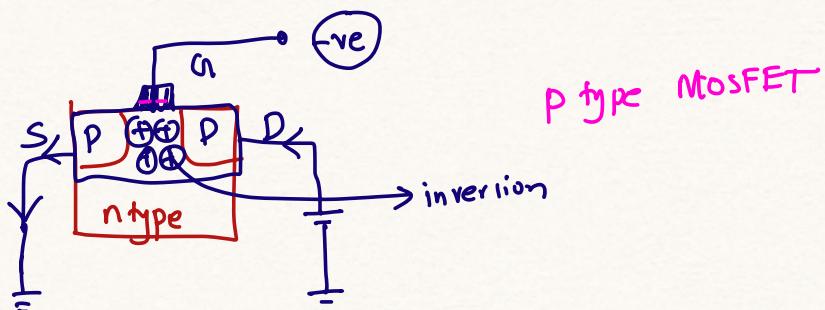
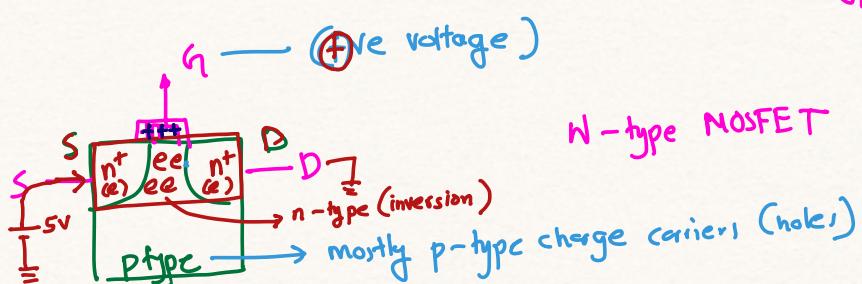
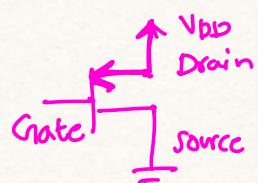
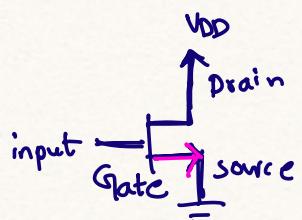
Unipolar logic families : current conduction → only 1 type of charge carried (e/hole)

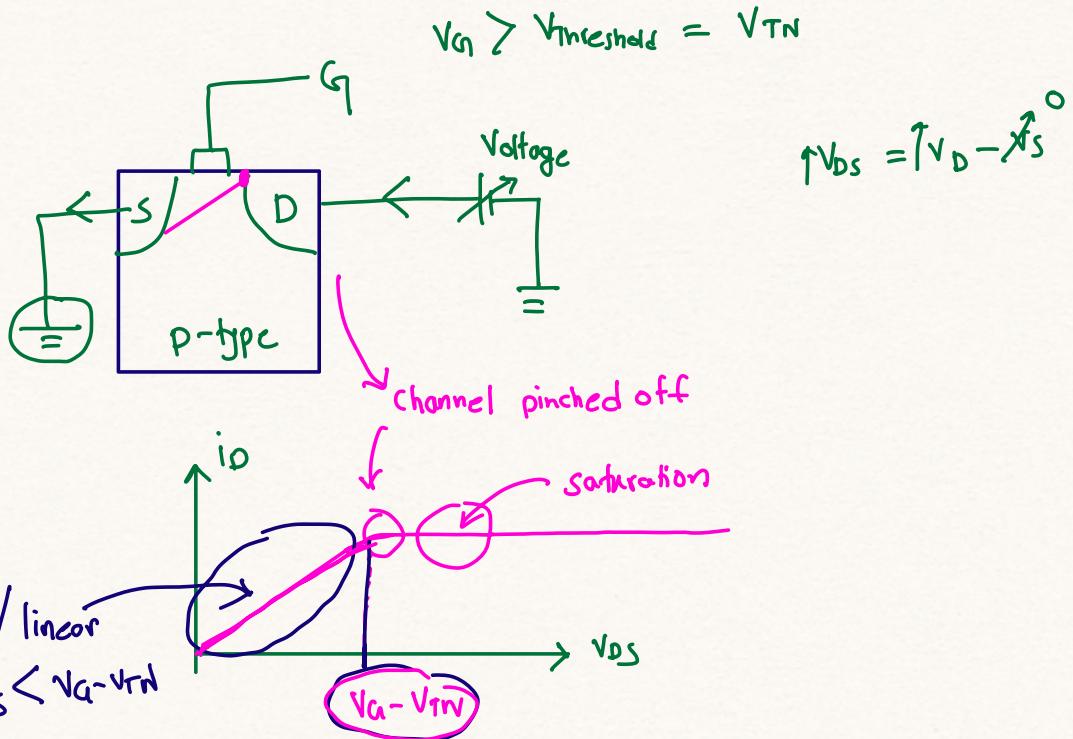
### Internal structure of MosFETs



(N MOS) p type substrates → lowest  $r$

(P MOS) n " " → highest  $r$





$$V_{DS} = V_D - i_s R_o$$

$V_{DS} = V_G - V_{TN}$  we reach saturation

Saturation region  $\rightarrow V_{DS} > V_G - V_{TN}$

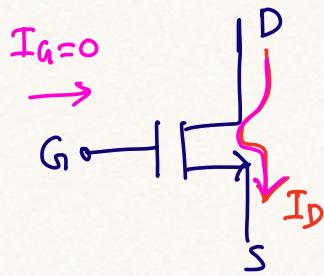
### Operating modes:

- ① cut off
- ② linear / triode
- ③ saturation

FET  
field effect  
Transistor

### n MosFET

$$V_{TN} > 0$$

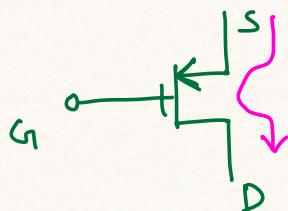


✓ ① cutoff :  $V_{GS} < V_{TN}$

② triode :  $V_{GS} > V_{TN}$  and  $V_{DS} < \frac{V_{GS} - V_{TN}}{2}$

③ saturation :  $V_{GS} > V_{TN}$  and  $V_{DS} \geq V_{GS} - V_{TN}$   
(Transition :  $V_{DS} = V_{GS} - V_{TN}$ )

### p type



① cutoff :  $V_{SG} < |V_{TP}|$  <sup>threshold</sup>

② triode :  $V_{SG} > |V_{TP}|$ ,  
 $V_{SD} < \frac{V_{SG} + V_{TP}}{2}$

③ saturation :  $V_{SG} > |V_{TP}|$   
 $V_{SD} \geq V_{SG} + V_{TP}$

(Transition  $V_{SD} = V_{SG} + V_{TP}$ )

## Current - Voltage Relationship

NMOS

$\times$  Triode:  $i_D = k_n [2(v_{ds} - v_{tn})^{v_{ds}} - v_{ds}^2]$

$\times$  Saturation:  $i_D = k_n (v_{ds} - v_{tn})^2$   $\downarrow$   $v_{ds} = v_{us} - v_{tn}$

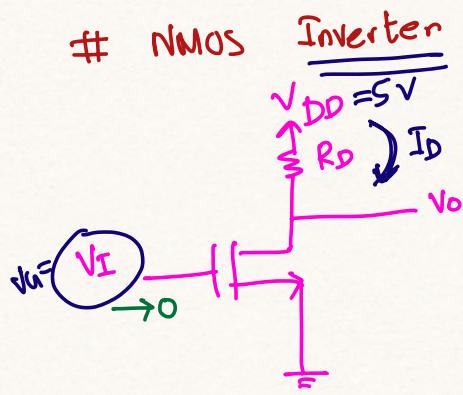
Conduction

PMOS

$\times$  Triode:  $i_D = k_p [2(v_{sg} + v_{tp})^{v_{sd}} - v_{sd}^2]$

$$i_D = k_p (v_{sg} + v_{tp})^2$$

$k_n \neq k_p$



$$(a) V_I = 5V$$

$$Q. \quad V_O = ?$$

- given
- (a)  $V_F = 5V$
  - (b)  $V_I = 1.5V$

Specs:

$$\begin{aligned} V_{DD} &= 5V, \quad R_D = 20k\Omega \\ V_{TN} &= 0.5V, \quad k_n = 0.3mA/V^2 \end{aligned}$$

$$V_G > V_{TN}$$

thought process

$$\left\{ \begin{array}{l} V_D = V_O = \text{Low} \\ V_S = 0 \\ V_G = \text{high} \end{array} \right.$$

$$V_{DS} ?$$

$$V_{DS} < (V_{GS} - V_{TN})$$

educated assumption: fricke.

$$V_G \gg V_D$$

$$i_D = k_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

$$\begin{aligned} V_D &= V_O \\ V_S &= 0 \end{aligned}$$

$$i_D = 0.3 [2(5 - 0.5)V_O - V_O^2]$$

$$V_{DS} = V_O - 0 = V_O$$

$$V_G = 5V$$

also

$$i_D = \frac{V_{DD} - V_O}{R_D}$$

$$V_{GS} = 5 - 0 = 5$$

$$0.3 [2(5 - 0.5)V_O - V_O^2] = \frac{5 - V_O}{20k}$$

$$6V_O^2 - 55V_O + 5 = 0$$

$i_D$  negative

$$V_O = \begin{cases} 9.074 & V \\ 0.092 & V \end{cases}$$

$i_D$  (true)

$$V_{DS} = V_0 = 0.092$$

$$V_{AS} - V_T = 5 - 0.5 = 4.5$$

$$\therefore V_{DS} < V_{AS} - V_T \quad (\text{Triode})$$

$\therefore$  assumption correct

(b)  $V_I = 1.5V$  assume sat. ( $V_I = 20V$ )

$$i_D = k_n (V_{AS} - V_{TN})^2$$

$$= 0.3 \text{ mA}$$

$$i_D = \frac{V_{DS}}{\frac{5 - V_0}{20k}} = 0.3$$

$$V_0 = -1V$$

$$\left\{ \begin{array}{l} V_{DS} = -1 \\ (V_{AS} - V_{TN}) = 1 \end{array} \right\} \quad V_{DS} < V_{AS} - V_T$$

assumption is wrong.

$\rightarrow$  Triode mode

$$i_D = 0.3m [2(1.5 - 0.5)V_0 - V_0^2] = \frac{5 - V_0}{20k}$$

$$i_D = \frac{5 - V_0}{20} \quad 0.3V_0^2 + 0.65V_0 - 0.25 = 0$$

$$V_0 = \begin{cases} 1.67V & X \leftarrow \\ 0.5V & X \checkmark \end{cases}$$

Verification :

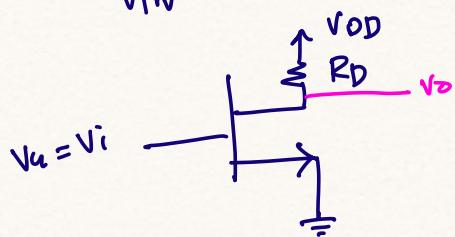
$$V_{DS} = 1.67 \quad > \quad V_{GS} - V_{TN} = 1$$

$$\cancel{V_{DS} = 0.5} \quad < \quad V_{GS} - V_{TN} = 1 \quad \checkmark$$

# Determine the  $I_D, V_o$  for  $V_{DD} = 2.5V, R_D = 20k\Omega$

$V_{TN} = 0.5V, K_n = 0.3 \text{ mA/V}^2$ .

(a)  $V_I = 2V$   
 (b)  $V_I = 0.3V$



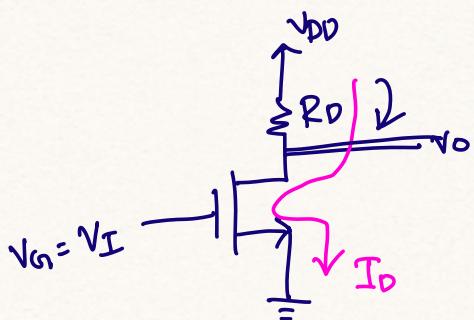
Determine the "transition point"  
 ① "maximum drain current,  $I_{D\max}$ "  
 ② "maximum power dissipation"  
 ③ "maximum drain current,  $I_D$ "

### Inverter

Specs:

②  $V_{DD} = \underline{2.5V}$ ,  $R_D = 20k\Omega$ ,

$$V_{TN} = 0.5V, k_n = 0.3mA/V^2$$



$$I_D = \frac{V_{DD} - V_o}{R_D}$$

$V_o$  is minimum  $I_D$  is maximum  
 $V_G$  to be maximum (inverter)

Let  $V_{DD} = 2.5$   $V_o = V_{DS} = \text{Low}$

assume  $\underline{V_{DS}} < V_{GS} - V_T \rightarrow \underline{\text{triode}}$

$$i_D = \frac{2.5 - V_o}{20k} = (0.3 \times 10^{-3}) [2(2.5 - 0.5) - V_o]$$

$$6V_o - 2.5V_o + 2.5 = 0$$

$$V_o = \begin{cases} 0.1025V \\ 4.064V \end{cases} \quad (\text{id neg}) \times$$

verification for triode  $\left\{ \begin{array}{l} V_o = 0.1025V \\ \text{triode correct!} \end{array} \right.$

$$V_{GS} - V_T = 2.5 - 0.5 = 2V$$

$$i_{D \max} = \frac{2.5 - 0.1025}{20k} = 0.1198 \text{ mA}$$

(1) Transition at  $v_{DS} = v_{GS} - v_{TN}$

at transition  $\begin{cases} v_o = ? \\ i_D = ? \\ v_i = ? \end{cases}$

$i_D = \frac{v_{DD} - v_o}{R_D}$

$i_D = k_n (2(v_{GS} - v_{TN}) v_{DS} - v_{DS}^2)$   
 $= k_n (2(v_{DS}) v_{DS} - v_{DS}^2)$   
 $= k_n (v_{DS}^2) \quad \checkmark$

at transition :  $i_{D \text{ sat.}} = k_n (v_{GS} - v_{TN})^2 \quad //$

$$k_n (v_{GS} - v_{TN})^2 = \frac{v_{DD} - v_{DS}}{R}$$

$$k_n (v_{DS})^2 = \frac{v_{DD} - v_{DS}}{R}$$

$$k_n (v_o)^2 = \frac{v_{DD} - v_o}{R} \quad \left\{ \begin{array}{l} v_{DD} = 2.5V \\ R = 20k \\ k_n = 0.3 \text{ m} \end{array} \right\}$$

$$6v_o^2 + v_o - 2.5 = 0$$

$$v_o = \begin{cases} 3.40V & \times \quad I_D \text{ negative} \\ 0.567V & \checkmark \end{cases}$$

$I_D = \frac{2.5 - 0.567}{R_D(k\Omega)}$

$= \underline{\underline{mA}}$

$\checkmark$   $v_o = 0.567V = v_{DS}$

$v_I = v_{AS} = 1.067V$

$$v_{DS} = v_{AS} - v_{TN}$$

$$v_{AS} = v_{DS} + v_{TN}$$

$$= 0.567 + 0.5$$

$$v_{AS} = 1.067V$$

## NMOS NOR Gate

00	}	V <sub>D</sub>
01		
10		
11		

I<sub>D</sub>

Cmos  $\rightarrow$  NMOS  
 $\rightarrow$  PMOS

- Basic operation
- Logic implementation

$$\left\{ V_D, I_D \right\} \\ (\bar{a} + b) \cdot \bar{c} = f$$

$$\frac{V_{TH}}{V_H} = \frac{V_H}{R_1 + R_2} \frac{R_1}{R_1 + R_2}$$

$\checkmark$

$R_1, R_2$

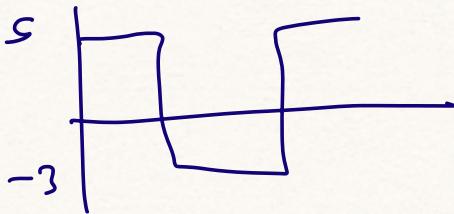
$$V_{TL} = V_L \frac{R_1}{R_1 + R_2}$$

-3

$R_1 = ?$

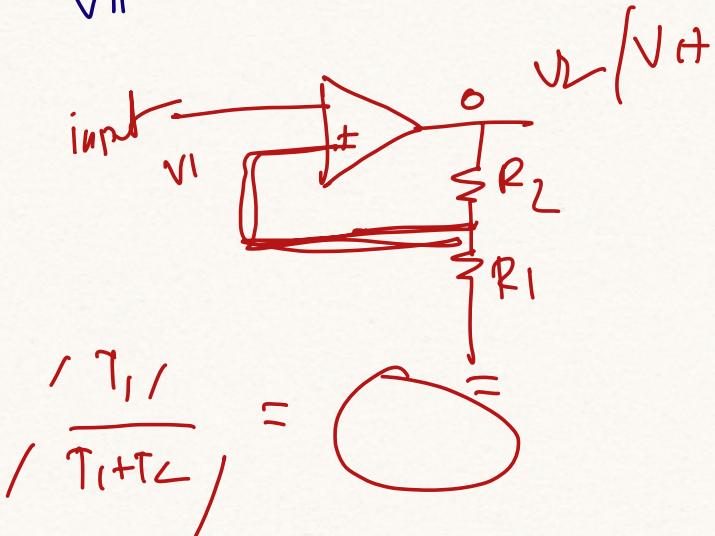
$R_2 = ?$

$$\frac{R_1}{R_1 + R_2} = \frac{V_{TH}}{V_H}$$



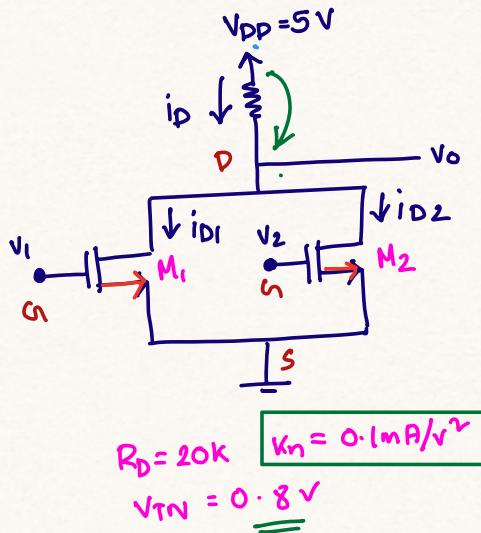
$V_{T_1}$  Nu

$\sqrt{T_1 T_L} R -$



$$\text{Duty} = \frac{T_1}{T_1 + T_L} = \dots \rightarrow$$

## NMOS NOR GATE Example :



Case 1

$$v_1 = v_2 = 0V$$

$$V_{GS1} = V_{G1} - V_{S1} = 0 - 0 < 0.8V$$

$$V_{GS2} = V_{G2} - V_{S2} = 0 - 0 < 0.8V$$

Both cutoff

$$i_{D1} = i_{D2} = 0$$

$$v_o = V_{DD} = 5V$$

case 2

$$\underline{v_1 = 5V} \quad \underline{v_2 = 0}$$

grounded

$$V_{GS2} = \underline{V_{G2}} - \underline{V_{S2}} = \underline{0} - \underline{0} = 0 < 0.8V \quad M_2 \rightarrow \text{c/o}$$

$$\checkmark V_{GS1} = V_{G1} - V_{S2} = 5 - 0 = 5 > 0.8V \quad \left. \begin{array}{l} \text{Triode} \\ \text{sat.} \end{array} \right\} \quad (V_{DS} = 20V \text{ (NOR)})$$

assume triode region:

$$\therefore V_{DS} < (V_{GS} - V_T)$$

$$i_{D1} = i_D = K_n \left( 2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2 \right) \quad \checkmark$$

$$i_D = \frac{V_{DD} - V_o}{R_D} \quad \checkmark \quad (V_{DS} = V_o)$$

$$\frac{5 - V_o}{20K} = 0.1m \left( 2(5 - 0.8) V_o - V_o^2 \right)$$

$$2V_o^2 - 9.4V_o + 5 = 0$$

$$V_o = \frac{0.29V}{8.6V} \quad \left. \begin{array}{l} \checkmark \\ X \end{array} \right\} I_D \text{ negative}$$

$$V_0 = 0.29V$$

check

$$(V_{AS} > V_{TN}) \quad \checkmark$$

$$5 > 0.8$$

$$\underline{\underline{}}$$

$$+ \quad V_{DS} < (V_{AS} + V_{TN}) \quad \checkmark$$

$$= V_0 = 0.29 < 5 + 0.8 = 5.8 \quad \underline{\underline{}}$$

$\therefore$  Triode

assumption correct!

$$i_D = \frac{5 - 0.29}{20k} = 0.2354 \text{ mA}$$

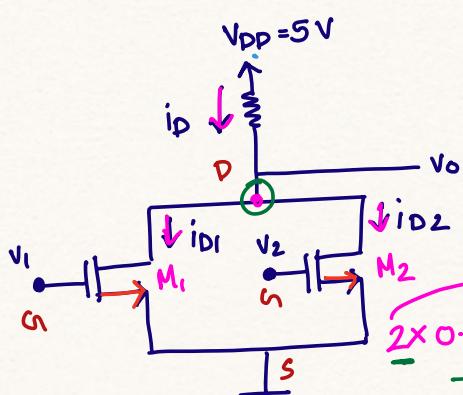
case: ③  $V_1 = 0V, V_2 = 5V$

values will be same as  $M_1 \neq M_2$  has  $k_{n1} = k_{n2}$

if  $k_{n1} \neq k_{n2}$  → values in case ② & ③ varies

case ④

$$V_1 = V_2 = 5V$$



Assume Triode as:

NOR Gate →  $V_0 = 10V$  when  $V_1, V_2 = 5V$

$$V_0 = V_{DS} = \text{Low}$$

$$V_{DS} < (V_{AS} - V_{TN}) \rightarrow \underline{\underline{\text{Triode}}}$$

$$i_{D1} + i_{D2} = i_D$$

$$2 \times 0.1m [2 \times (5 - 0.8) V_0 - V_0] = \frac{5 - V_0}{20k}$$

$$V_0 = \frac{4.17V}{0.149V} \approx 28V$$

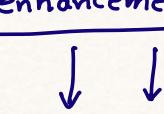
$i_D$  is pos. but there will be problem regarding state.  
Do yourself.

$$V_b = 0.149V$$

$$i_D = 0.243 \text{ mA}$$

$$I_{D1} = I_{D2} = \frac{i_D}{2}$$

NMOS inverter with enhancement load.



enhancement type, (n & p type)



Enhancement type n-MOS

$V_{TN} < 0$

$$V_{GS} = 0 \rightarrow \text{on}$$

large neg. value to turn off ...

$\times$  clo :  $V_{GS} < V_{TN}$

$\times$  Triode :  $V_{GS} > V_{TN}$  and  $V_{DS} \leq V_{GS} - V_{TN}$

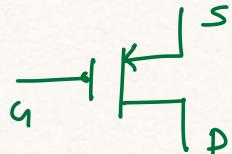
$\times$  Sat :  $V_{GS} > V_{TN}$  and  $V_{DS} \geq V_{GS} - V_{TN}$

} same as  
depletion type n-MOS

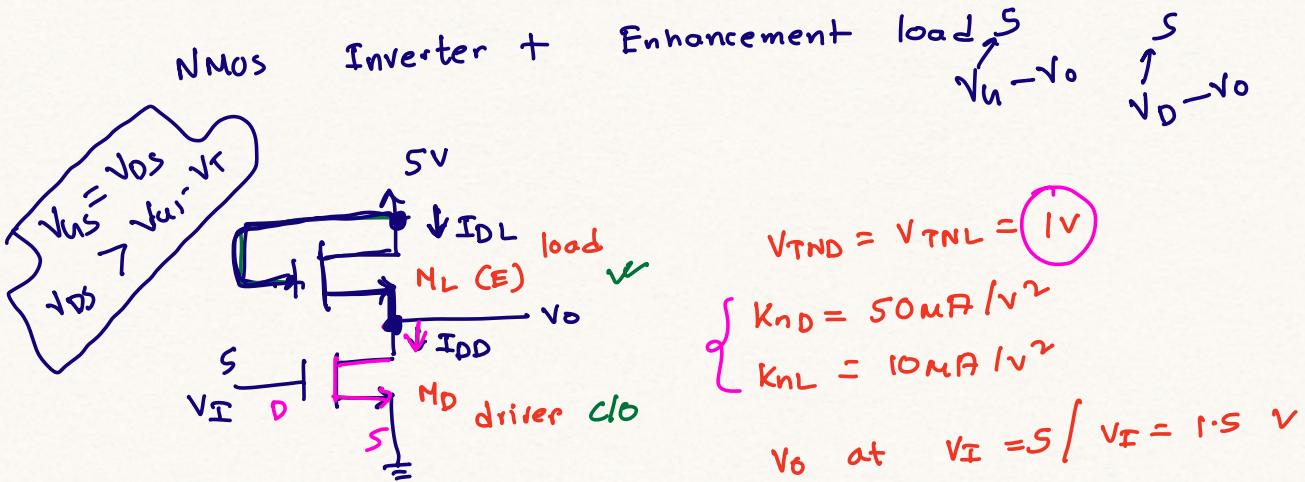
Enhancement type P-MOS

$$V_{GS} = 0 \rightarrow \text{on}$$

$V_{TP} < 0$



$\times$  other eqn same as depletion type P-MOS.



case 1:  $V_I = 0 \text{ V}$

$$V_{DS0} = 0 < V_{TN} = 1 \text{ V}$$

M<sub>D</sub> would be in clo  $\therefore I_D = 0$

$$\text{For } M_L \quad V_{DL} = V_{GL} = 5 \text{ V}$$

$$\therefore V_{DS} = V_{DS}$$

$$V_{DS} > V_{DS} - V_{TN}$$

sat

$$V_{DS} > V_{DS} - V_{TN}$$

$$(5 - V_O) > (5 - V_O) - 1$$

$$\rightarrow I_{Dsat} = k_{nL} (V_{DS} - V_{TN})^2 = 0$$

$$\underline{\underline{V_{DS}}} = V_{TN}$$

$$\frac{V_{GL} - V_{SL}}{5 - V_O} = V_{TN}$$

$$V_O = 4$$

$$k_{nL} (V_{DS} - V_{TN})^2 = 0$$

$$V_{DS} = V_{TN}$$

$$V_{u} - V_s = 1$$

$$5 - V_O = 1$$

$$V_O = 4$$

case 2  $v_i = 5V$

$M_L \rightarrow \text{sat} \times$

$M_D \rightarrow \underline{\text{assume}} \quad \underline{\text{triode}} \quad \checkmark \quad (\text{inverter}, V_D = V_o = \text{Low}$   
 $\therefore V_{DS} < V_{GS} - V_T \text{ probably})$

$$I_{DD} = k_n n_D \left( 2(V_{GS_D} - V_{TN_D}) V_{DS_D} - \underline{\underline{V_{DS_D}}} \right) \checkmark \quad (\text{triode})$$

$$\hookrightarrow I_{DL} = k_n L \left( V_{GS_L} - V_{TN_L} \right)^2 \quad \checkmark \quad (\text{sat at load})$$

$$\checkmark 0.05 \left[ 2(5 - 0 - 1) V_o - \underline{\underline{V_o}} \right] = 0.01 (5 - V_o - 1)$$

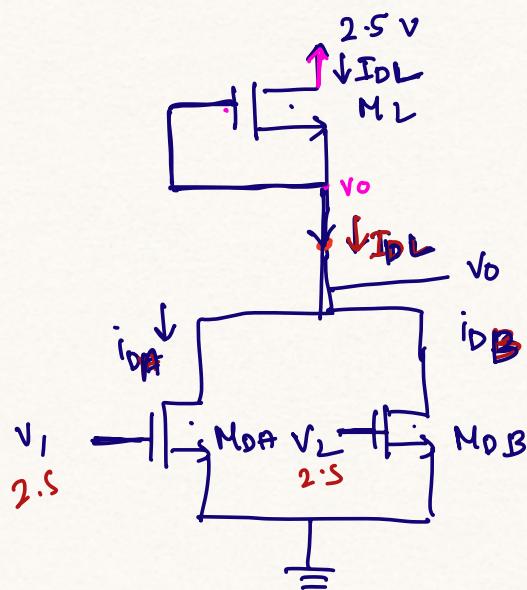
$$\checkmark 6V_o^2 - 48V_o + 16 = 0$$

$$V_o = \begin{cases} \frac{7.65}{2} V & \rightarrow \text{higher than } \underline{\underline{V_{DD}}} \\ 0.34 V & \rightarrow \checkmark \end{cases}$$

verification :  $\underline{\underline{V_{DS_D}}} = 0.34 V < \frac{V_{GS_D} - V_{TN_D}}{5 - 1} = 4$

$\therefore \text{triode assumption correct!}$

NNOS NoR gate with Depletion load



$$V_{TNL} = -0.6 \text{ V}$$

$$V_{TND} = 0.4 \text{ V}$$

$$\left\{ \begin{array}{l} kn' = 100 \mu A / V^2 \\ \left( \frac{w}{l} \right)_L = 1 \end{array} \right\}$$

$$\textcircled{*} \quad k = (100\mu A/N^2 \times 1)$$

$$*\left(\frac{W}{L}\right)_D = 4$$

$$W_{KnD} = (100_{NP}/v^2 \times 4)$$

$$\textcircled{*} \quad k_{\text{MP}} = 400 \text{ MP/V}^2$$

$$\left. \begin{array}{l} k_n = \text{conduction before} \\ = k_n' (w/l) \end{array} \right\}$$

$$\underline{\underline{\text{case:}}} \quad (\nu_1, \nu_2) = 2.5\nu \checkmark$$

$$V_0 = \text{Low}$$

## Load

$$V_{DSL} = 2 \cdot S - V_0$$

$$V_{\text{threshold}}$$

$$> v_{ASL} - v_{INL}$$

$$= (v_0 - v_0) - (-0.6)$$

$$V_{DS} = 2.5 - v_o \quad > \quad 0 + 0.6 v_i$$

NOR gate  
both input high

$v_o$  is small  $\rightarrow v_D$  for drivers is small  
 $v_{DS_D} < v_{AS_D} - v_{TD}$   $\therefore$  assume triode

$\frac{v_{DS_D}}{=}$

$\begin{matrix} \text{Load} \\ (\text{sub}) \end{matrix} \quad \begin{matrix} \text{Driver} \\ (\text{triode}) \end{matrix}$

$i_{D_L} \downarrow \quad \downarrow \quad i_{D_A} \downarrow$

$$\left[ k_n' \left( \frac{w}{l} \right) \right] (0 - (-0.6)) =$$

$$k_n' \left( \frac{w}{l} \right) (2(2.5 - 0 - 0.4) v_o - v_o^2)$$

$$+ k_n' \left( \frac{w}{l} \right) \frac{(2(2.5 - 0 - 0.4) v_o - v_o^2)}{I_{DB}}$$

$$4v_o^2 - 16.8v_o + 0.36 = 0$$

$$v_o = \begin{cases} 4.178v & > v_{DD} \times \\ 0.02153v & \checkmark \end{cases}$$

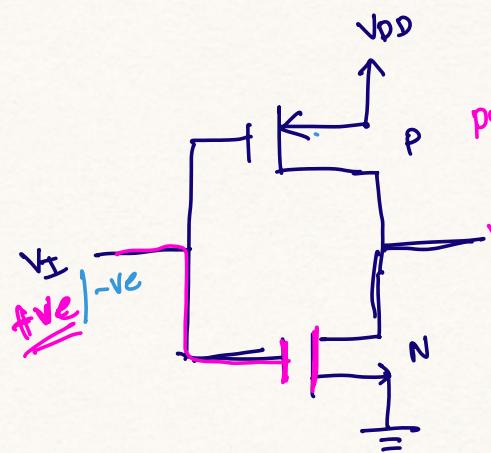
$$i_{D_L} = k_n (v_{AS_L} - v_{TN_L})^2 = 0.036 \text{ mA}$$

$$i_{D_A} = i_{DB} = k_n \left( 2(v_{AS_D} - v_{TN_D}) v_{DS_D} - v_{DS_D}^2 \right)$$

$$= 0.018 \text{ mA}$$

## Cmos Logic family

C = complementary



pull up network

$$V_o = 0 / V_{DD}$$

pull down network

$$V_{DD}$$

$$V_P$$

$$V_N$$

$$V_D$$

$$V_{DD}$$

$$V_I$$

$$V_I$$

$$V_I$$

$$V_I$$

CMOS inverter

(Low)

$$V_o = 0$$

if  $V_I$  is high

$V_N$  on

$V_P$  off

$V_I$  is low (Low)

(High)

$V_N$  is off

$V_P$  on

NOR

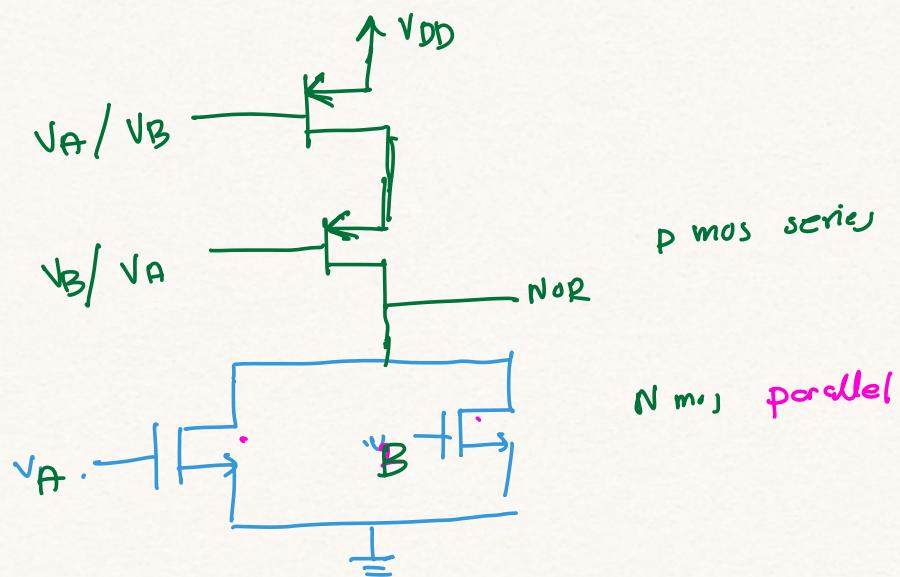
$$Y = \overline{A+B}$$

↑  
ORR

A, B input

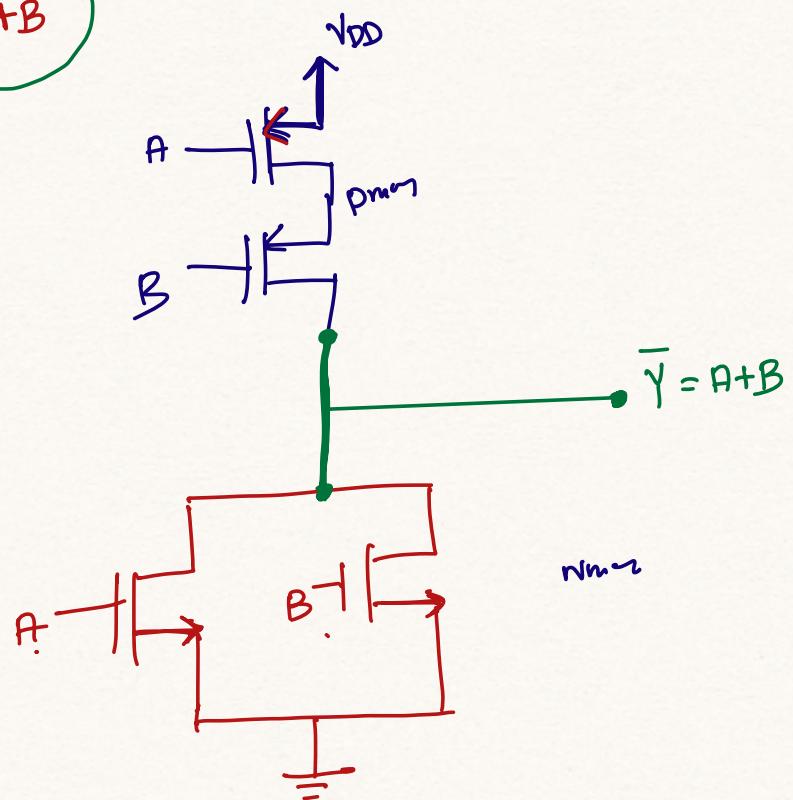
Y output

2 input  $\rightarrow$  2 Nmos  
~~2 Pmos~~

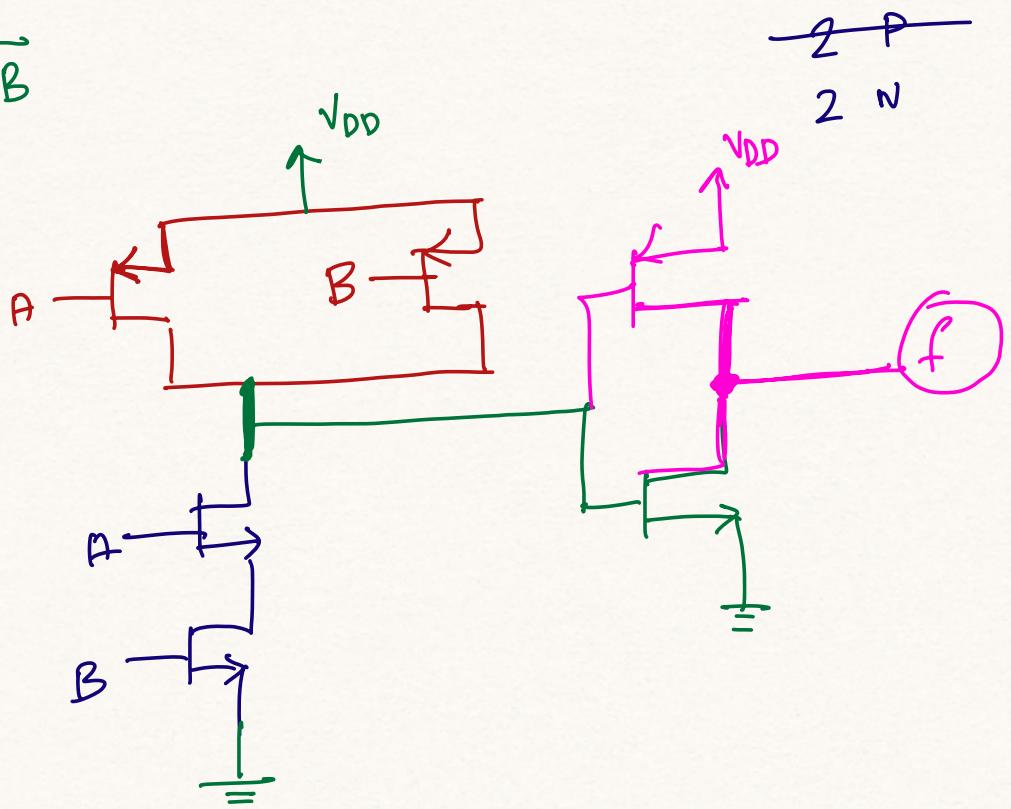


$V_1$	$V_2$	$V_o$
0	0	1
0	1	0
1	0	0
1	1	0

$$Y = \overline{A+B}$$

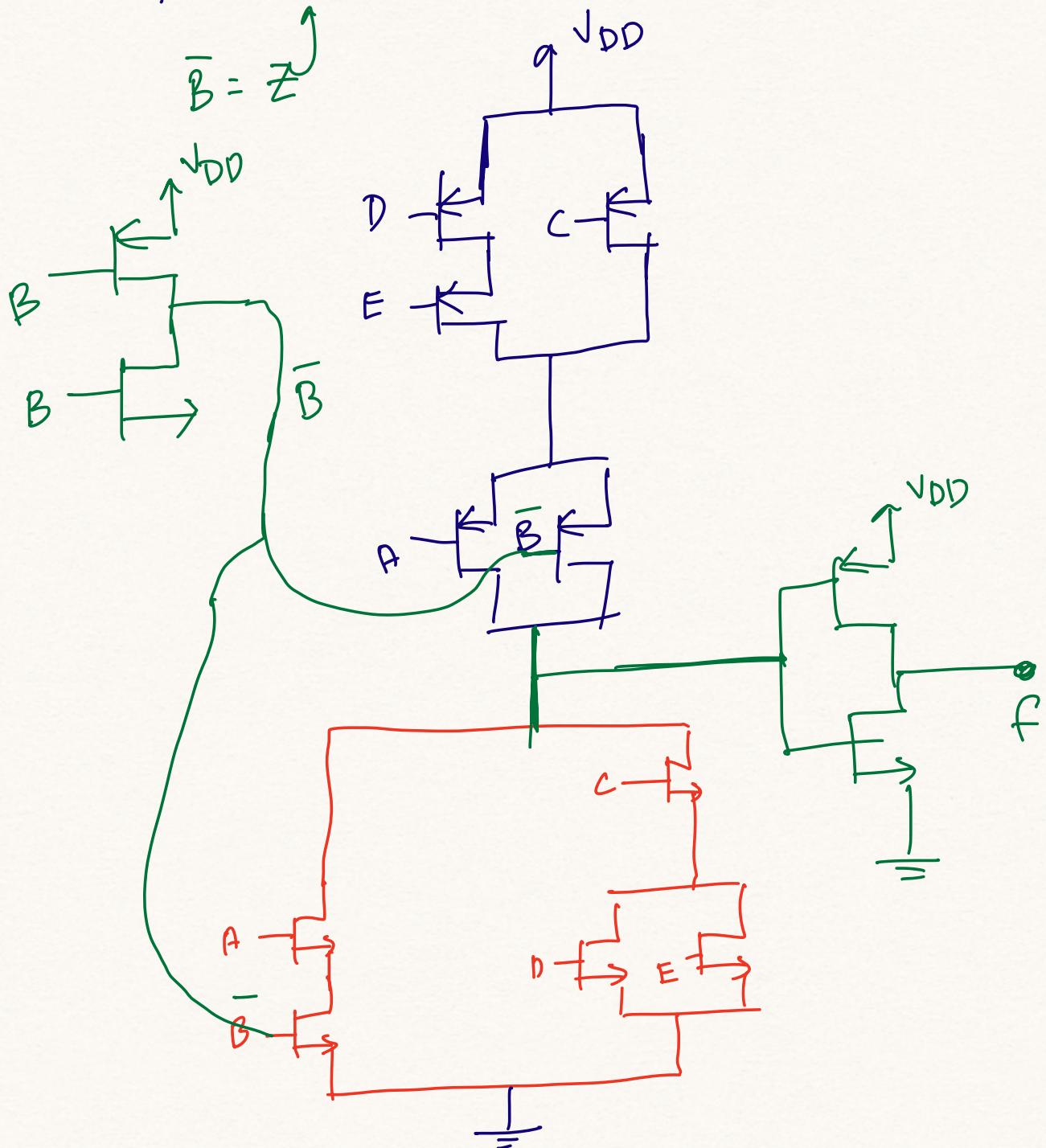


$$Y = \overline{A \cdot B}$$

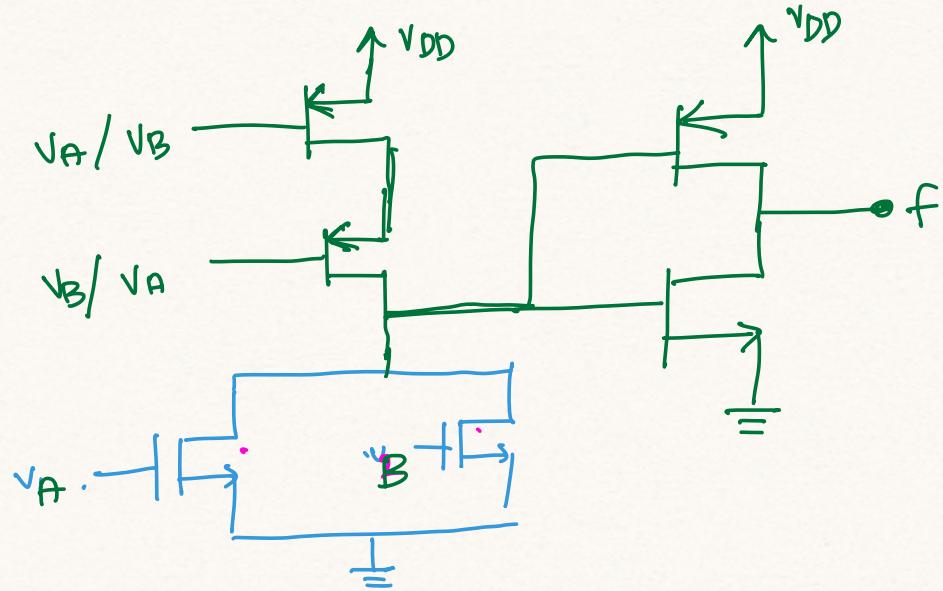


$$f = \bar{A}\bar{B} + C(D+E)$$

( $N - S$   
 $P - S$ )



$$f = (A+B)$$



### Algorithm

① start with N-mos

② design the logic

(parallel  $\rightarrow$  (N) OR type)

(series  $\rightarrow$  (N) AND type)

③ if we have  $f = \overbrace{\text{something}}$  we stop.

④ " " ,  $f = \overbrace{\text{something}}$ , we apply  $\circ \underline{\text{NOT}}$  get in the end.

⑤ joint Nmos network and PMos network

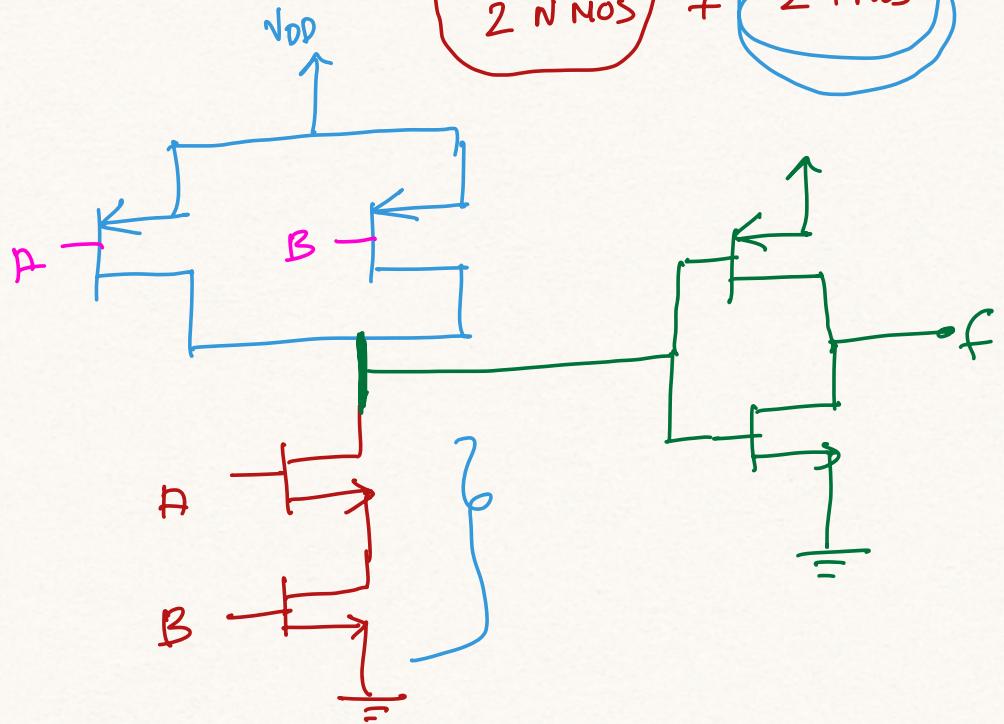
⑥ mark joining of Nmos network and PMos network as  $\underline{\underline{v_0}}$

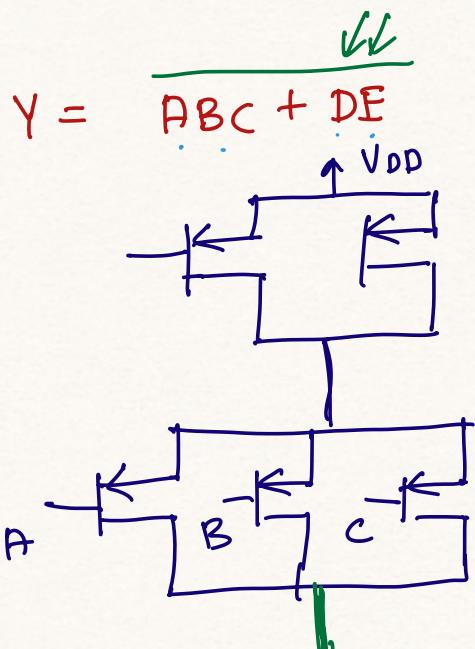
$$y = \overline{AB}$$

AND  
ORR



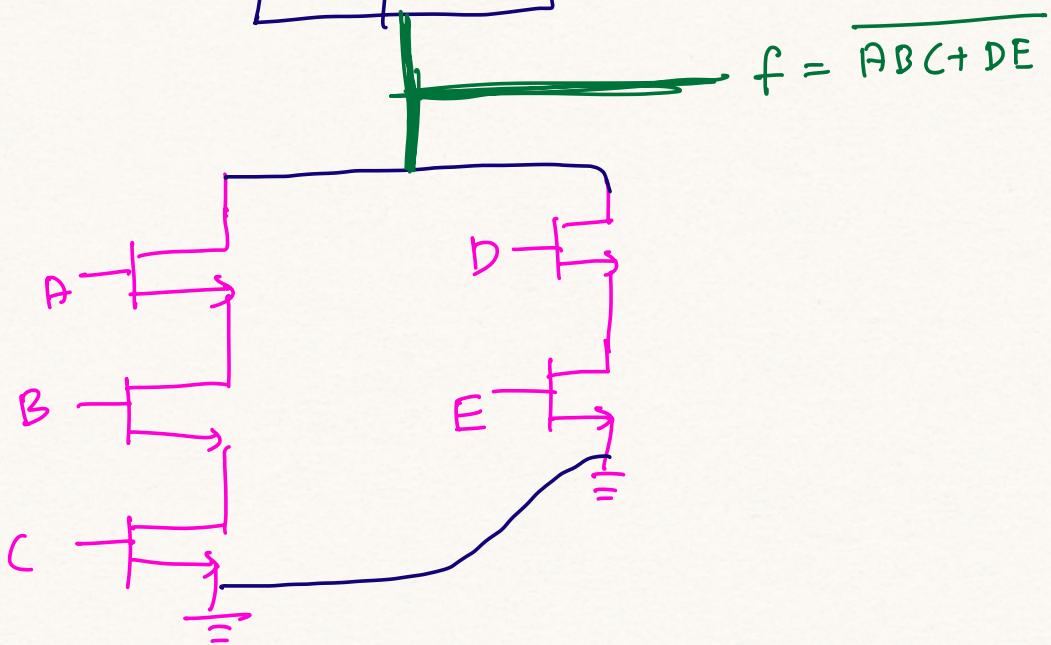
A B  
2 N MOS + 2 PMOS



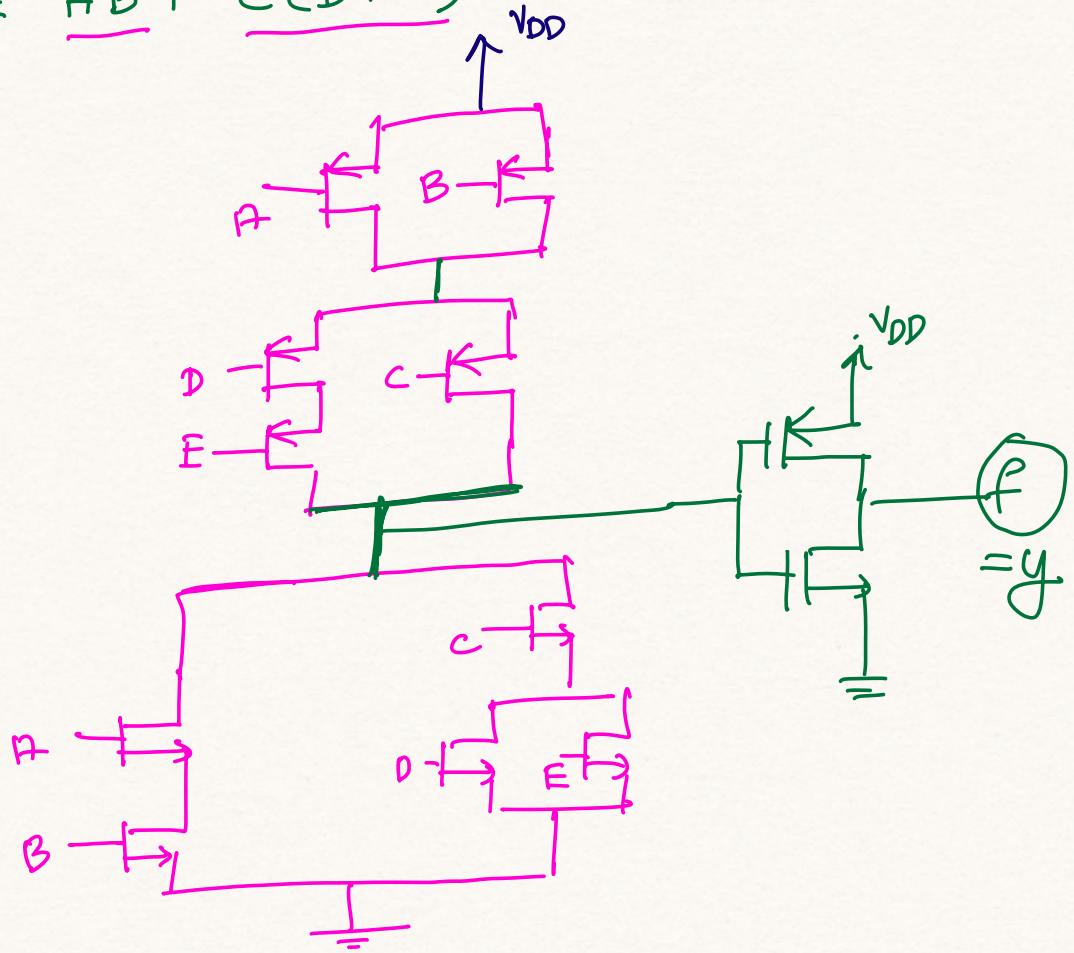


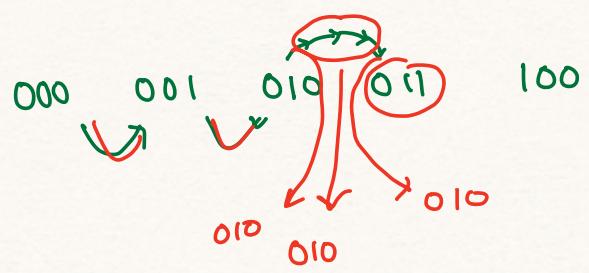
$\curvearrowleft$  N MOS  $\rightarrow S$

$\curvearrowright$  PMOS  $\rightarrow S$



$$Y = \underline{AB} + \underline{C(D+E)}$$





$011 \rightarrow ③$   $m = 3$

