

Review of CSE 251 : Electronic Circuits & devices

electronics: method or process used to control the flow of electrons using external electric field.

examples : spintronics , photonics ...

\downarrow \downarrow
control control optical wave
spin by by E field
 E field

→ Material classification in three categories: depending on conductivity

1. Metal	$10^{-13} \Omega m$
2. Insulators	$10^1 - 10^{-4} \Omega m$
3. Semiconductors	$10^{-10} \Omega m$

Concept of bands: → collection of discrete energy levels \nearrow conduction band \searrow valence band

- Electronic Band gap theorem

valence band: energy band formed by a series of energy levels containing valence electrons .

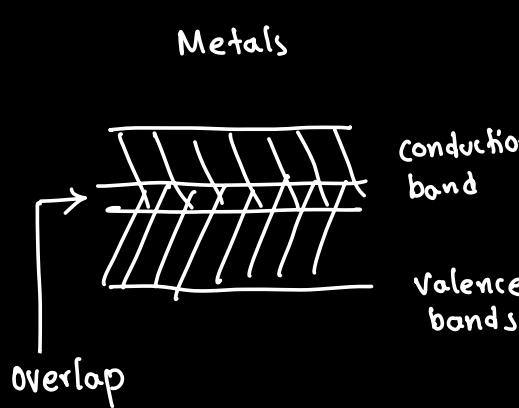
Low energy state , below fermi level

conduction band: when energized e^- may move from valence to conduction band.

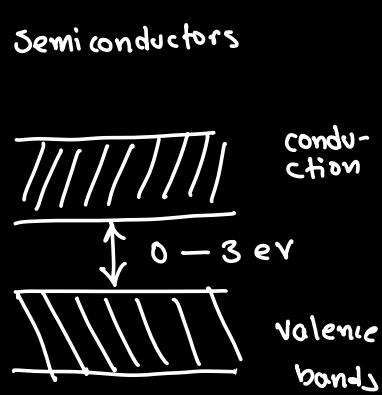
- Band of e^- orbitals that e^- bounce up into from valence band
- collection of energy bands above the fermi level
- e^- in conduction band are free to move
- current flow due to these e^- in conduction band

Fermi level: highest energy level which can be occupied by an e^- at 0K

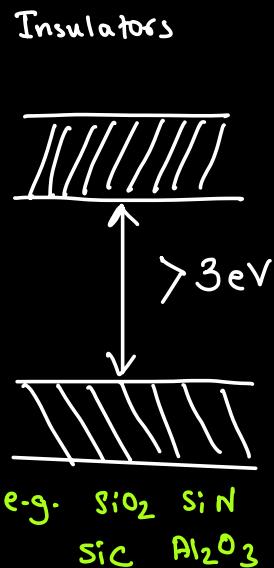
Energy levels in the 3 categories:



e.g.
Al, Ag, Cu, Na, Mg



e.g.
Si, Ge, GaAs, GaN



e.g. SiO_2 Si_3N_4
 SiC Al_2O_3

Silicon most widely used semi-conductor material in electronic devices

→ Semiconductors

1. Intrinsic semiconductor : Pure semiconductor material
(limited use → e.g. PIN diodes in LED)

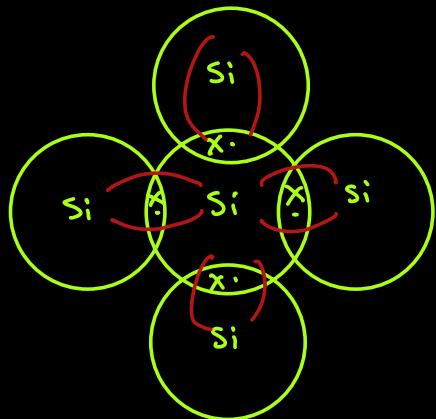
2. Extrinsic semiconductor : Impurity introduced here
(possibilities & applications → boundless!)

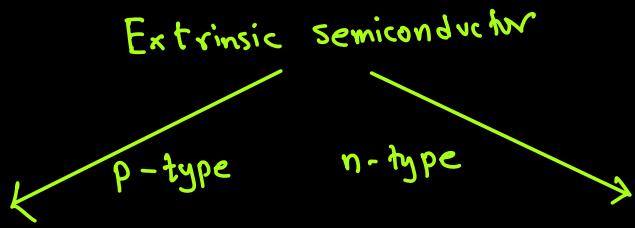
Visualizations

Si electron configuration : $1s^2 2s^2 2p^4$ 3s² 3p²

valence e^-

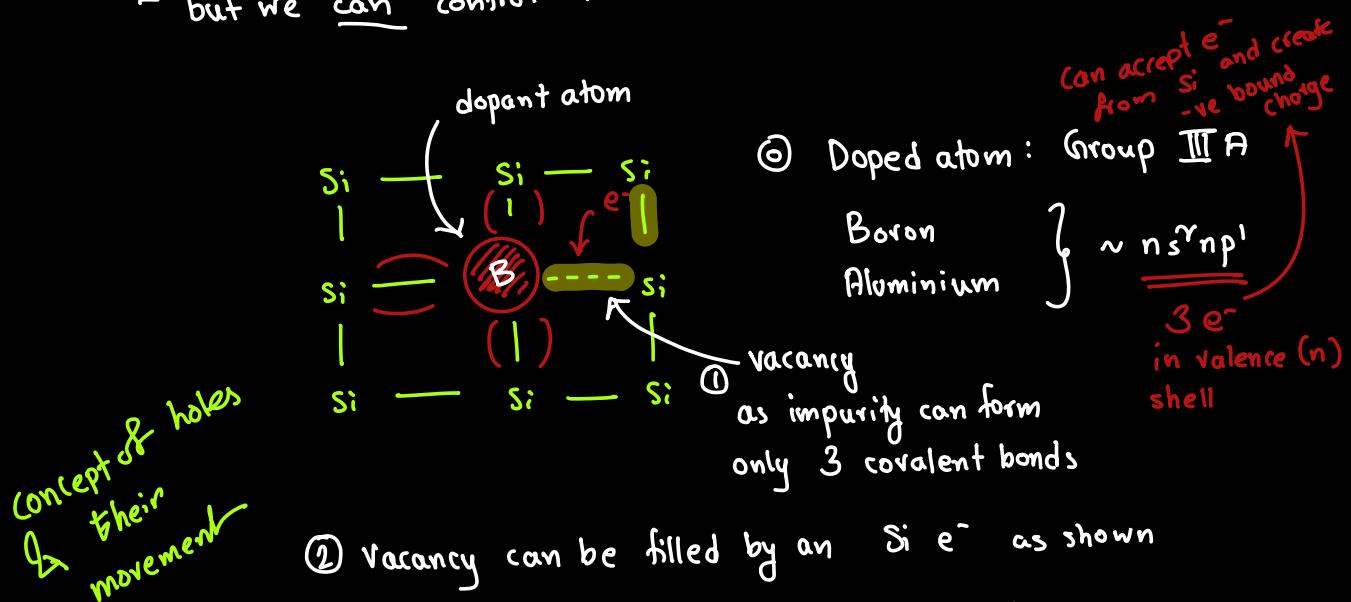
pure crystal → intrinsic semiconductor





① P type semiconductor

- we cannot control where we place the impurity atoms
- but we can control where we can place them



② Vacancy can be filled by an $Si e^-$ as shown

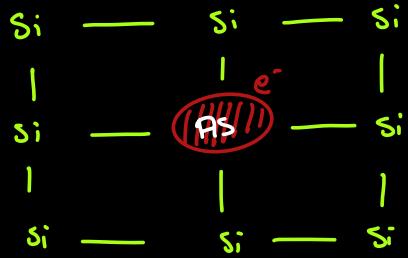
③ Vacancy \rightarrow absence of $e^- \rightarrow$ holes

④ movement of vacancies \rightarrow movement of holes

⑤ Majority charge carrier : hole

⑥ Boron can accept an e^- & form -ve bound charge

② N-type semiconductor

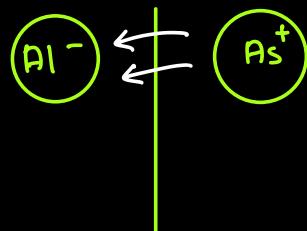
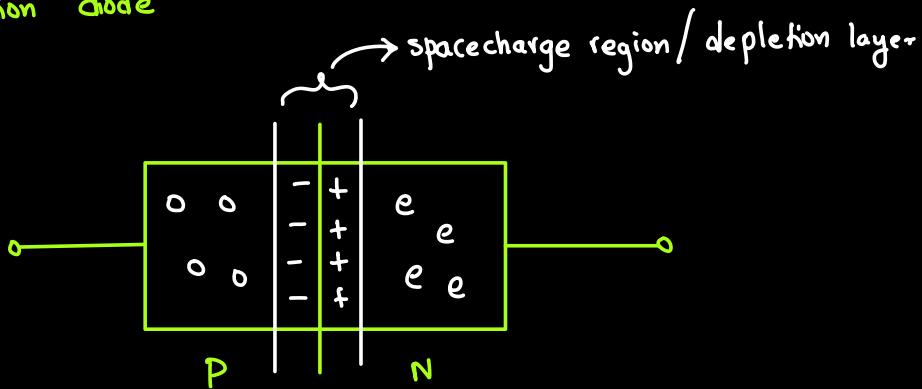


⑥ Dopant atom: Group VA
P, Sb, As $ns^2 np^3$

① Majority charge carrier is
 e^-

② As can just release an e^-
and form five bound charge

→ p-n junction diode



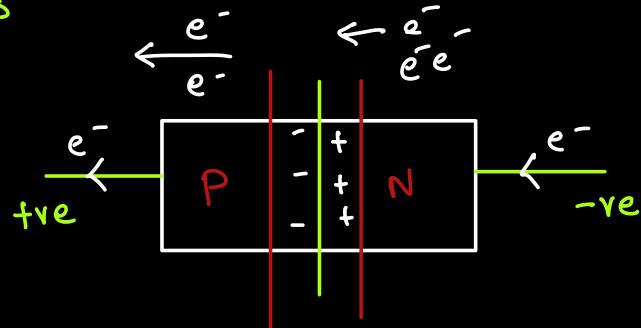
diffusion process

junction is fundamental to electronics
electronics would not be possible without it

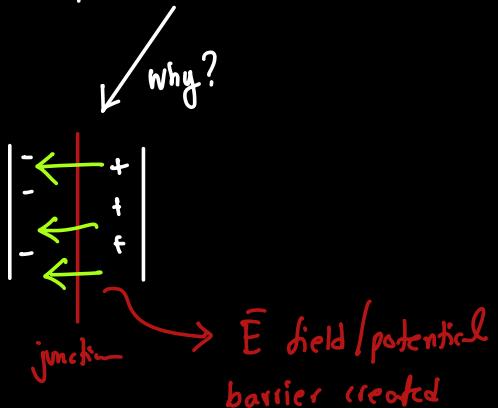
Two modes



Forward Bias



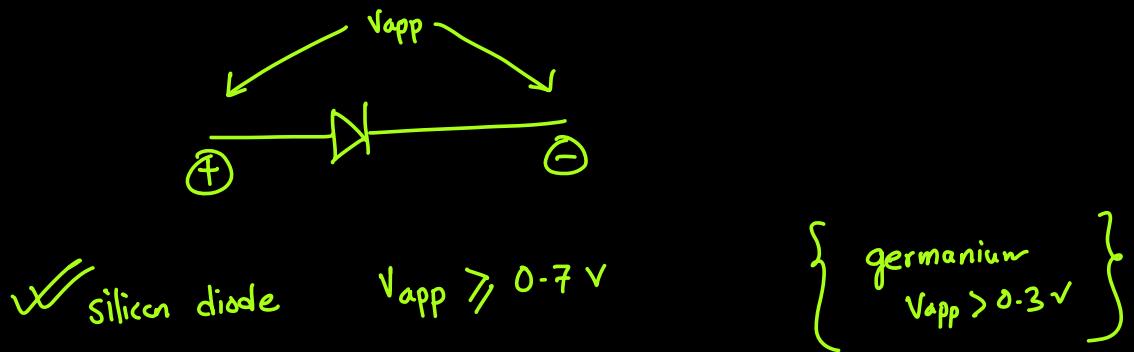
- ① high enough voltage applied
- ② e^- will move from N \rightarrow P side and out
- ③ voltage not high enough
- ④ e^- will not be able to cross depletion region
- ⑤ in space charge region



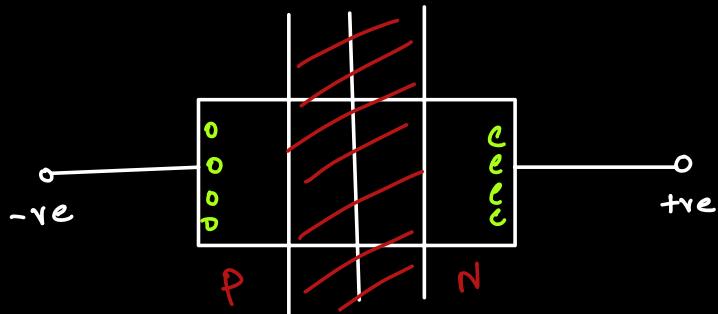
If field direction is \leftarrow , e^- pushed in \rightarrow direction

considering cases ①, ②,

⑥ e^- move N \rightarrow P, holes P \rightarrow N against barrier



Reverse bias

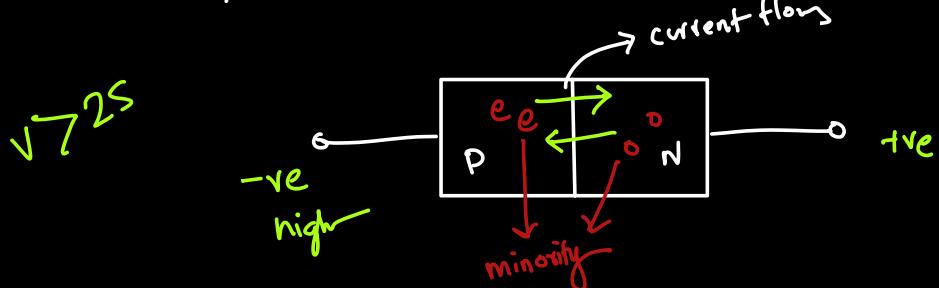


- ① increase in width of depletion region
- ② more diffusion needed to balance out and so more space charge formed ③ → not imp. for this course



→ # Breakdown

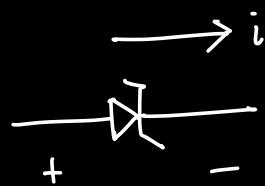
if reverse bias voltage is high \rightarrow diode may conduct



- ① Voltage (rev.) high enough to cause minority carriers to move to the other junction.

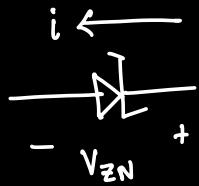
Zener diode

Breakdown mode is utilized in application



Forward conduction

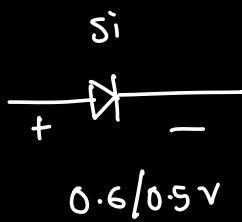
0.7V



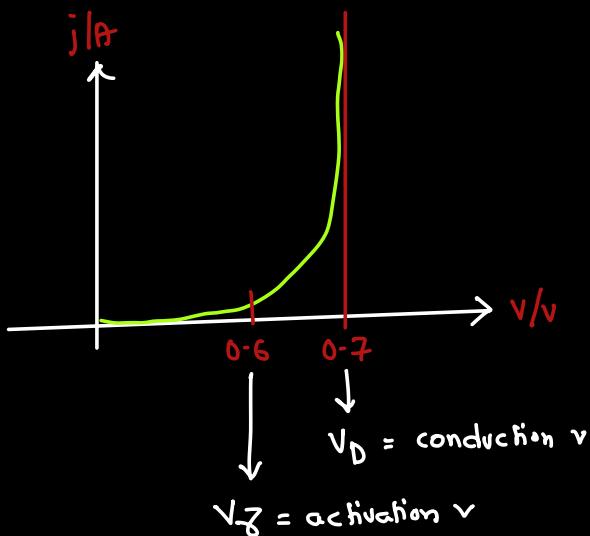
Zener Voltage

V_{reverse} > V_{ZN} → conduction

Activation voltage / Turn on voltage



0.6/0.5V



Conduction Voltage Drop model:

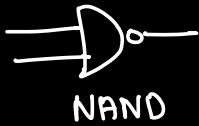
$$\textcircled{1} \quad \begin{array}{c} \xrightarrow{\hspace{1cm}} \\ \text{Zener Diode Symbol} \\ + \quad - \end{array} = \begin{array}{c} \xrightarrow{\hspace{1cm}} \\ \text{Voltage Source} \\ + \quad - \\ V_D = 0.7V \end{array}$$

$$\textcircled{2} \quad \begin{array}{c} \xrightarrow{\hspace{1cm}} \\ \text{Zener Diode Symbol} \\ - \quad + \end{array} = \begin{array}{c} \xleftarrow{\hspace{1cm}} \\ \text{Current Source} \\ - \quad + \end{array}$$

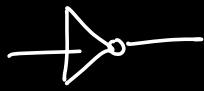
* In Question → see if activation voltage mentioned
if not → ignore use conduction voltage

Review of 251 ends (for diodes)

Introduction to Digital logic families



NAND



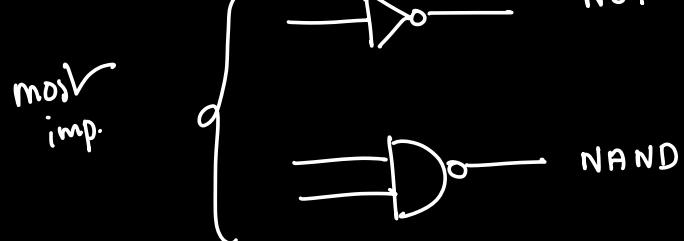
NOT



NOR

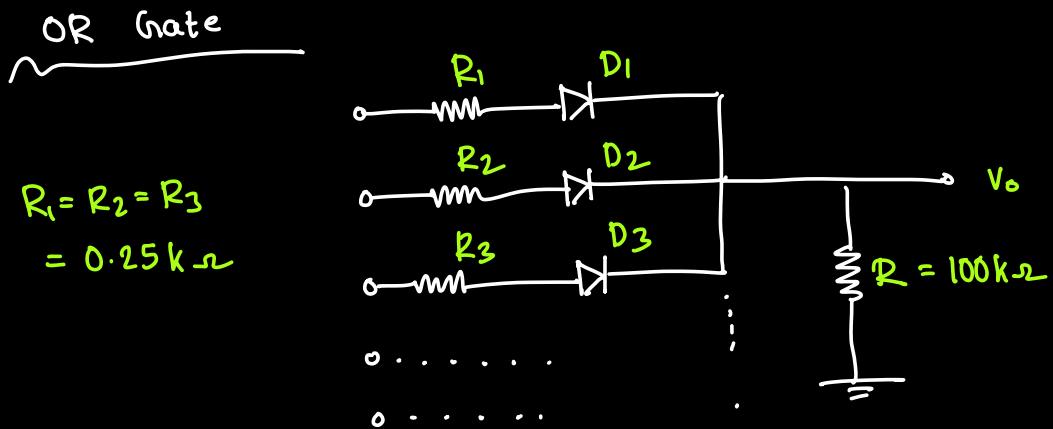
These gates are abstract → represent logical operations

Digital logic families distinguishes different ways of constructing logic



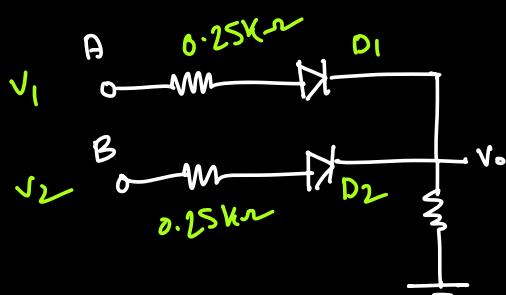
We can use diff electronic devices to construct logic gates

Diode logic (also in first lab 350)



"Beware of shorts" - Shahnewaz Bhai 2022

→ Consider constant voltage drop model



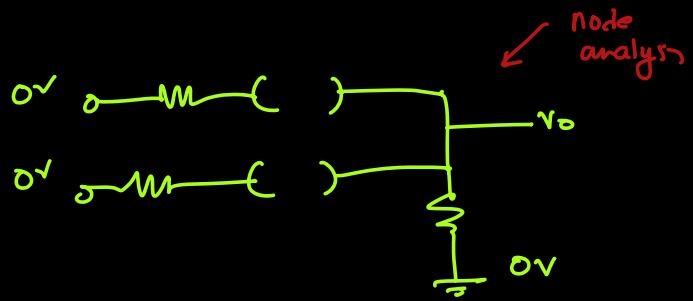
logic 1 → 5V
logic 0 → 0V

Case	A	B	V_1	V_L	V_0	C
i	0	0	0	0	0	0
ii	0	1	0	5	4.289	1
iii	1	0	5	0	4.289	1
iv	1	1	5	5	4.294	1

FACT: each diode needs atleast 0.6V to turn on

case I

D₁, D₂ off



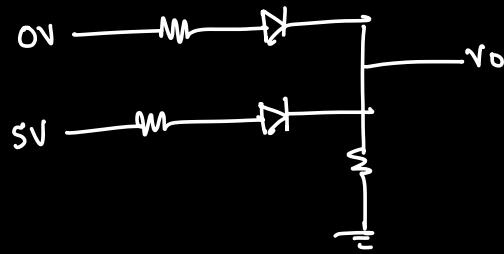
$$\frac{v_o - 0}{R} + \frac{v_o - 0}{R} + \frac{v_o - 0}{R} = 0$$

$$\frac{3v_o}{R} = 0$$

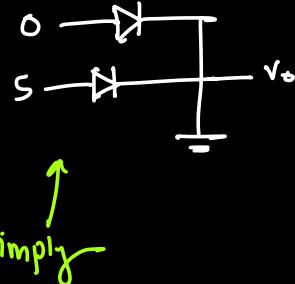
$$v_o = 0$$

no current

II

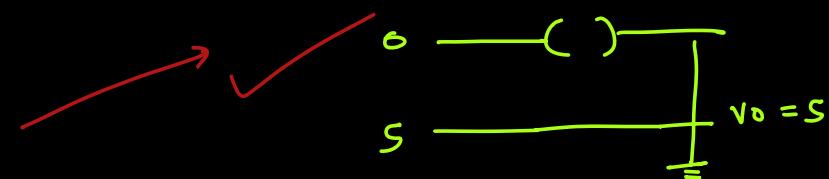


Simple model
≈

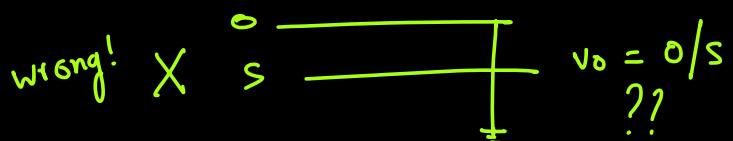


Step ①

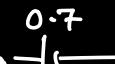
— simple analysis

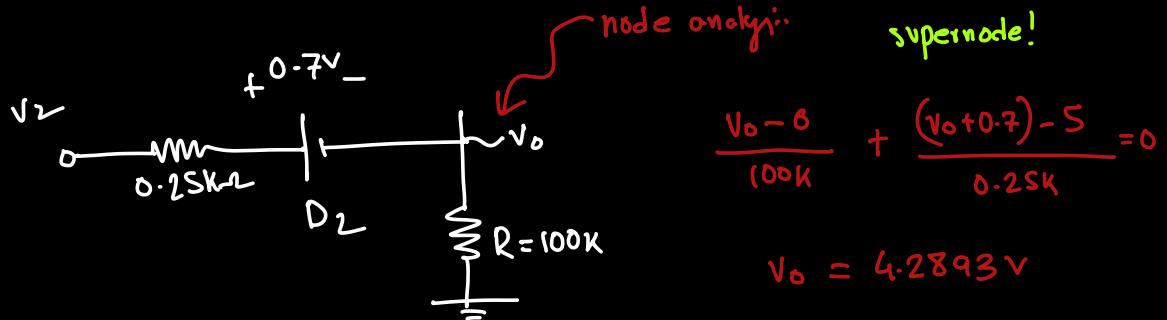


if



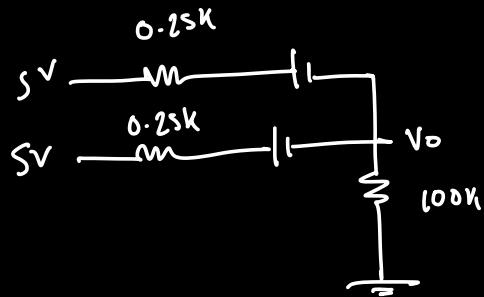
Step ②

- analysis \rightarrow constant V-drop model \rightarrow replace on D \rightarrow  off D \rightarrow 



case III same as II

case IV

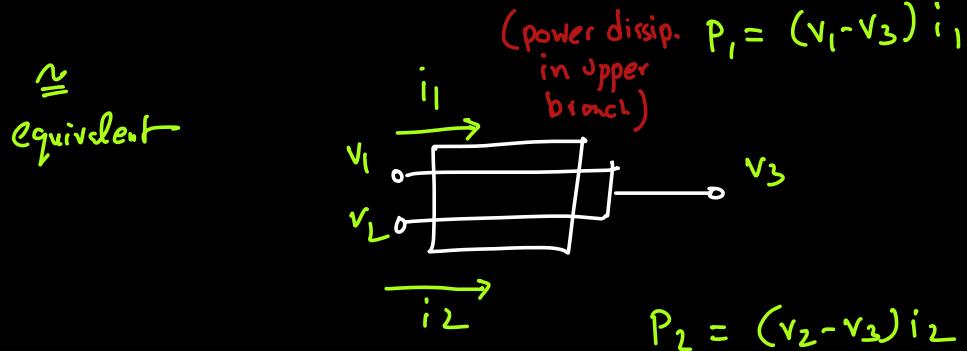
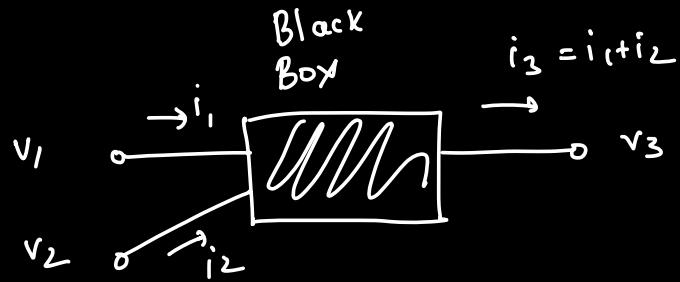


$$\frac{V_o + 0.7 - 5}{0.25k} + \frac{V_o + 0.7 - 5}{0.25k} + \frac{V_o - 0}{100k} = 0$$

choose smallest Vo value \rightarrow logical high (4.28 V)
 \therefore if $V > 4.28 \therefore$ Logical high otherwise Low

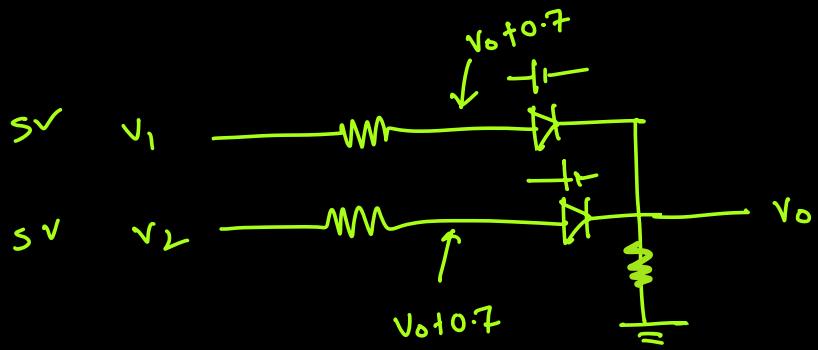
Power dissipation calculation

Theory



$P = P_1 + P_2 \quad (\text{total Power dissipation})$

among our 4 cases in previous example, which one
will cause P_{\max} dissipation.

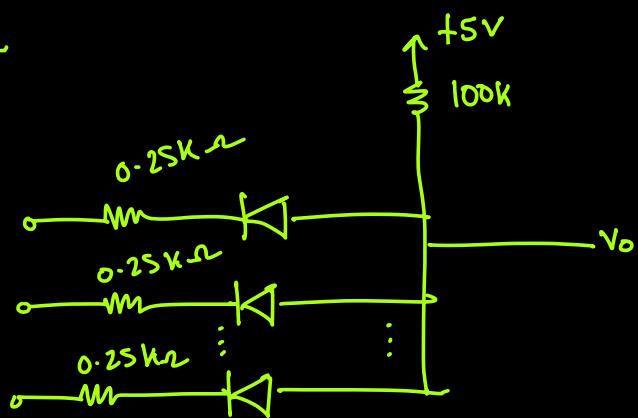


$$i_1 = \frac{5 - (4.2946 + 0.7)}{0.25 k}$$

$$i_2 = i_1$$

$$\left. \begin{array}{l} P_1 = (5 - 6) \times i_1 \\ P_2 = (5 - 6) \times i_2 \end{array} \right\} \quad p = P_1 + P_2$$

AND GATE



Do case analysis!

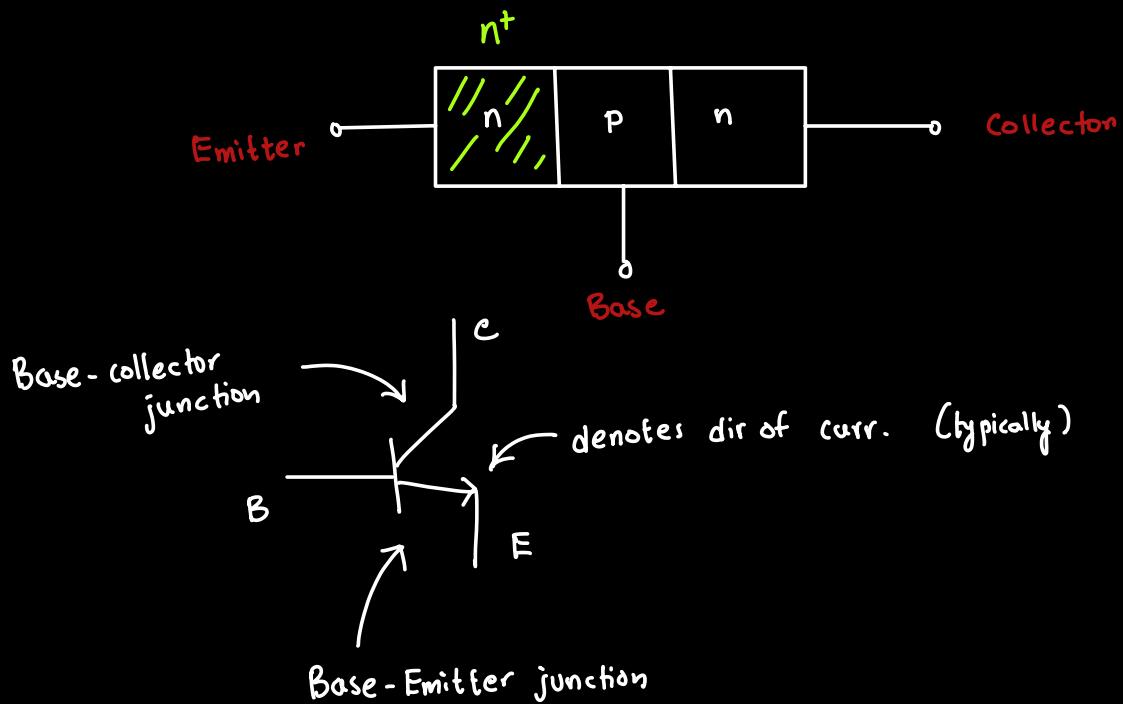
Set logic low voltage here \rightarrow set highest as logic low. $\therefore V_o < V_{low(highest)}$ \rightarrow logic low

Transistor

Lecture 3

- Will be used as a switch
- NOT as an amplifier

only n-p-n in this course

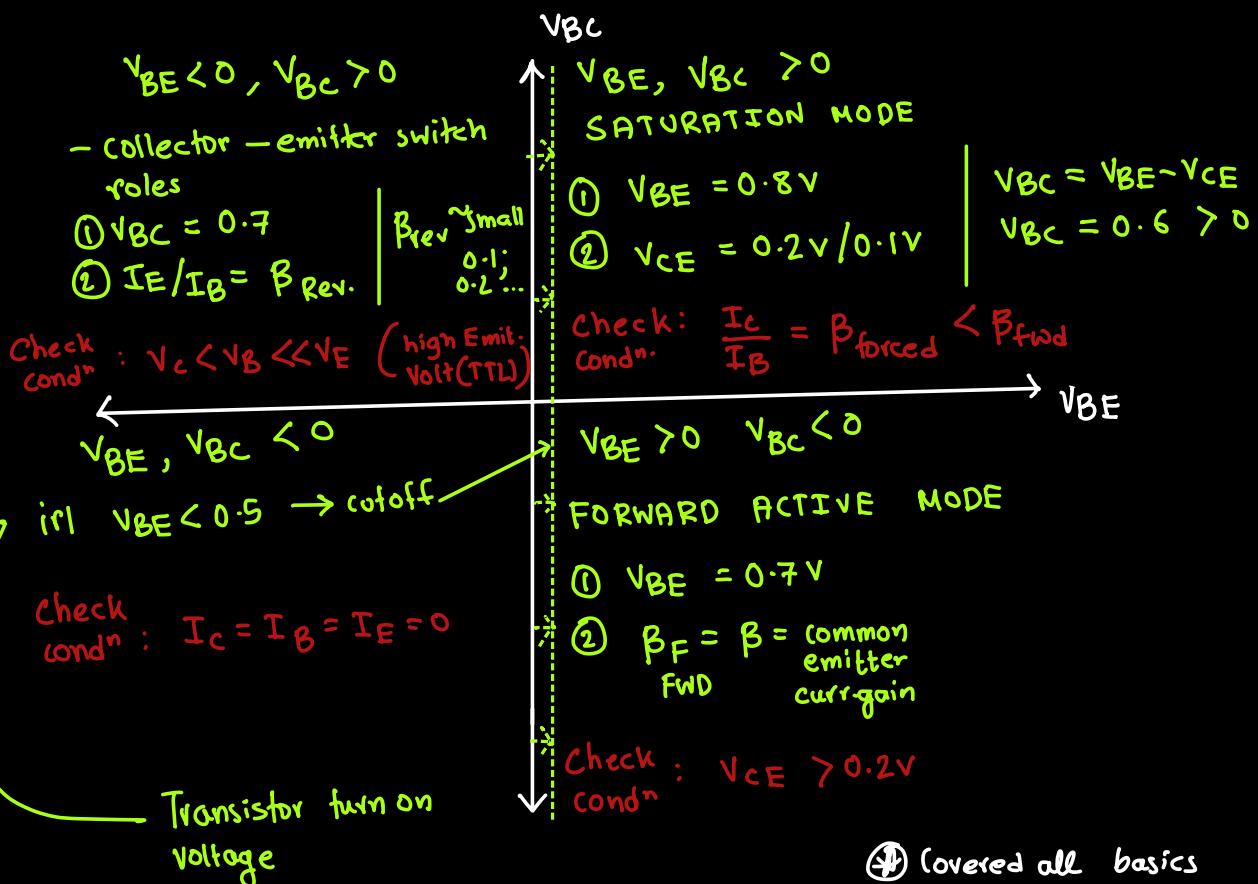


3-terminal device → e, h both used to carry current
∴ Bipolar device

Bipolar Junction Transistor (BJT)

4 modes of operation acc. to V_{BE} & V_{BC}

BE junction	BE junction	Mode
R	F	Forward active
F	F	Saturation
R	R	Cutoff
F	R	Reverse active

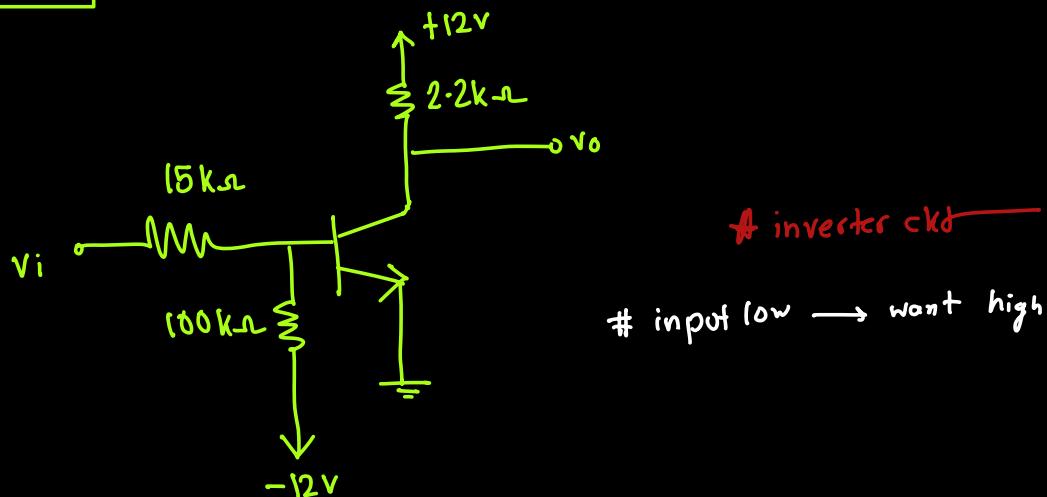


⊕ Covered all basics needed for this course

Register Transistor Logic (RTL)

{ saturated logic family:
logic transistors connected
to the output terminal }

NOT GATE



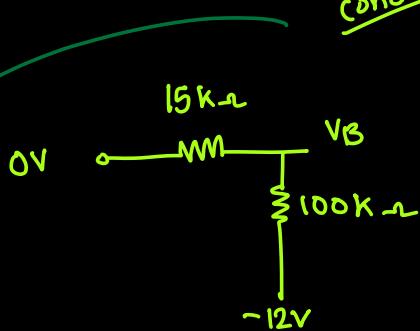
input low → want high

case (I)

$$\overline{Vi} = 0$$

assume cutoff

cond'n ① $V_{BE} < 0.5 \text{ V}$



cond'n ② $I_C = I_B = I_E = 0$

$$\frac{V_B - 0}{15k} + \frac{V_B - -12}{100k} = 0$$

$$V_B = -1.565 \text{ V}, V_B = 0$$

check $V_{BE} = -1.565 \text{ V} \quad \checkmark$

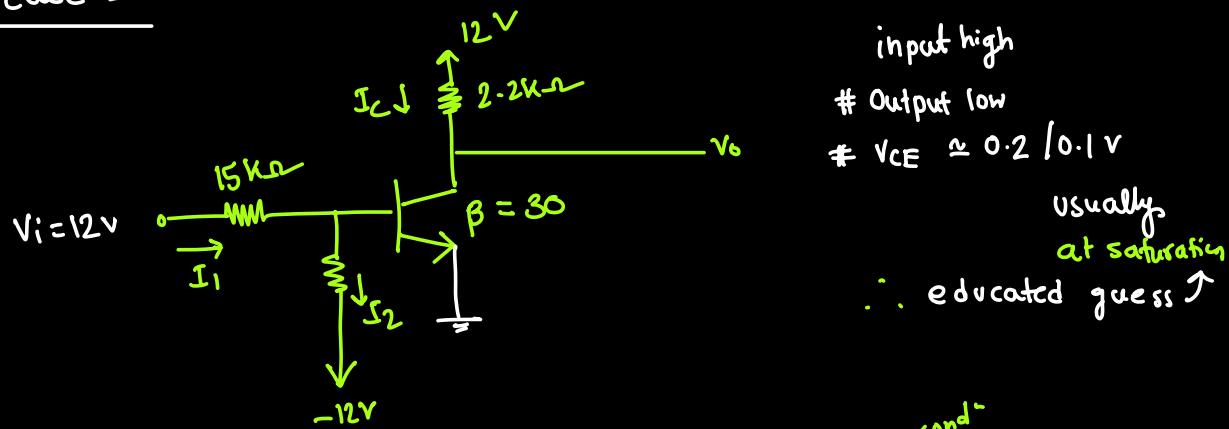
$$< 0.5 \text{ V}$$

For cutoff : $I_B = I_C = I_E = 0$

$$I_C = 0 = \frac{12 - V_C}{2.2k}$$

$$V_C = 12 = V_O \text{ high //}$$

Case 2



sat:

$$\textcircled{1} \quad v_{BE} = 0.8 \text{ V}$$

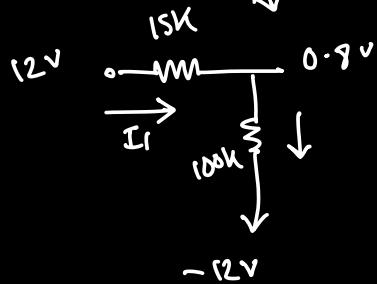
$$\textcircled{2} \quad v_{CE} = 0.2 \text{ V}$$

$$I_C = \frac{12 - v_C}{2.2 \text{ k}}$$

$$I_C = 5.3 \text{ mA}$$

(cond)
2
 $v_{CE} = v_C = 0.2$

$$\textcircled{1} \quad v_{BE} = 0.8 \text{ V}$$



$$I_1 = \frac{12 - 0.8}{15 \text{ k}} = 0.746 \text{ mA}$$

$$I_2 = \frac{0.8 - (-12)}{100 \text{ k}} = 0.128 \text{ mA}$$

case check

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = 8.659 < \beta_{\text{FWD}}$$

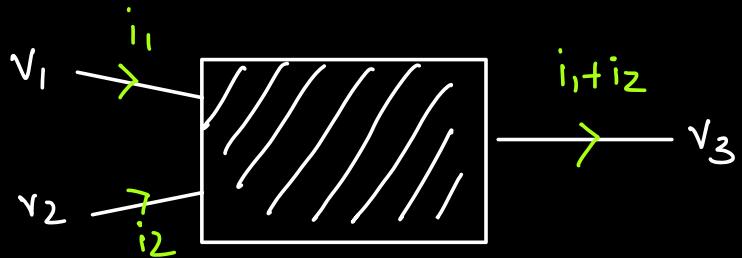
assumption ✓

$$I_B + I_2 - I_1 = 0$$

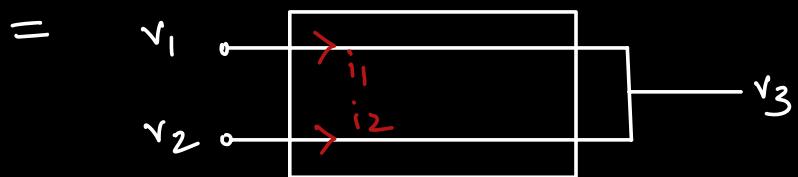
$$I_B = I_1 - I_2 = 0.619 \text{ mA}$$

Power dissipation

Lecture 4



$$P_1 = (v_1 - v_3) i_1$$



$$P_2 = (v_2 - v_3) i_2$$

$$P_{\text{dissipation}} = P_1 + P_2 = (v_1 - v_3) i_1 + (v_2 - v_3) i_2$$

maximum power dissipation \rightarrow ① Look at the cases of the gates

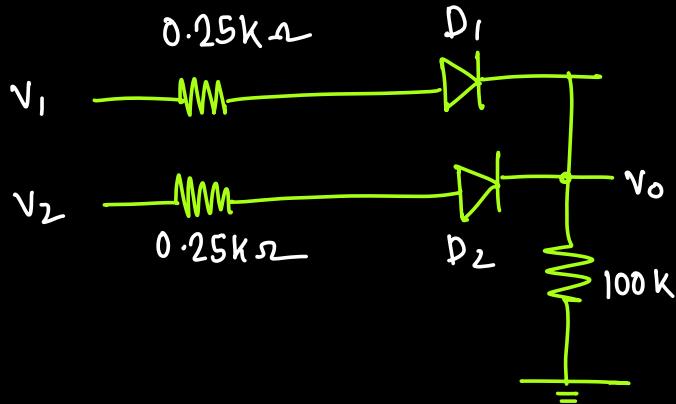
- ④ If in doubt, find the power dissipation (for cases in doubt)

P_{\max} = "jeta boro habe of the cases"

- ② Notice where max current flows

- ③ Calc. power for that case

from prev. ckt



for Diode Logic Ckt

Remember the case ...

(I) $V_1 \quad V_2 \quad D_1 \quad D_2$
0 0 off off

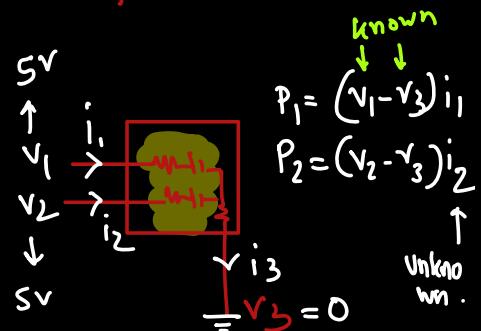
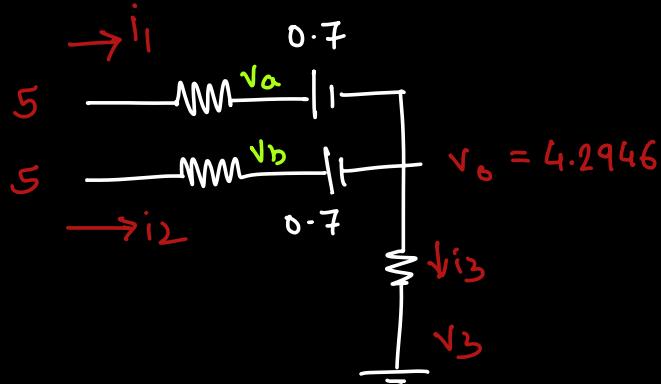
(II) $V_1 \quad V_2 \quad D_1 \quad D_2$
0 5 off on

(III) $V_1 \quad V_2 \quad D_1 \quad D_2$
5 0 on off

(IV) $V_1 \quad V_2 \quad D_1 \quad D_2$
5 5 on on

most current for this case

$\therefore P_{\max}$ pow dissipation!



To find maximum power dissipation \rightarrow find currents i_1, i_2, i_3 .

$$V_a - V_3 = 0.7 \quad \text{--- (1)}$$

$$\therefore V_a = 0.7 + 4.2946$$

$$V_a = 4.9946 \text{ V}$$

} similarly

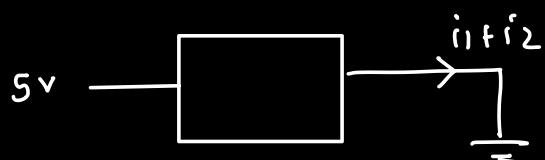
$$V_b = 4.9946 \text{ V}$$

$$v_1 \downarrow \quad v_3 \downarrow$$

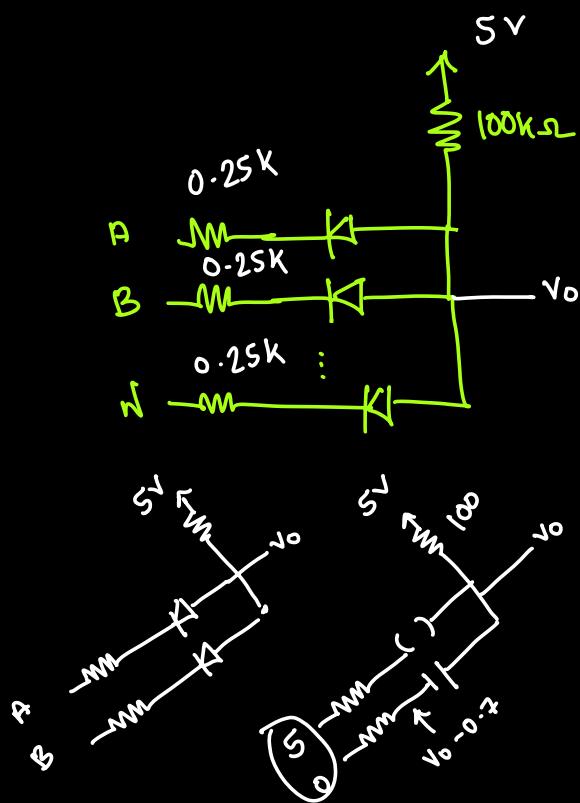
$$P_1 = (5 - 0) \times i_1$$

$$P_2 = (5 - 0) \times i_2$$

$$P_{\text{tot}}^{\text{(max)}} = P_1 + P_2 = 0.215 \text{ mA}$$



Do this for and gate too!

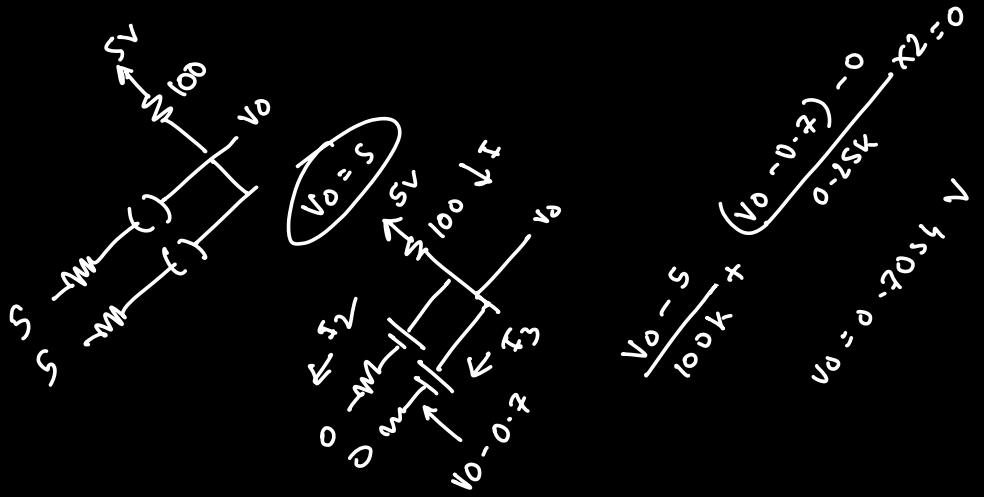


PRACTICE!

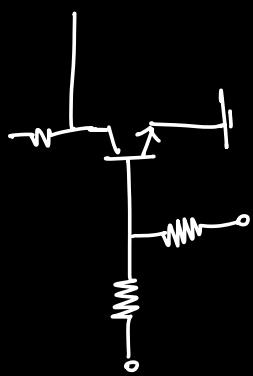
$N = 2, 3$

$$\frac{v_o - 5}{100k} + \frac{v_o - 0.7}{0.25k} = 0$$

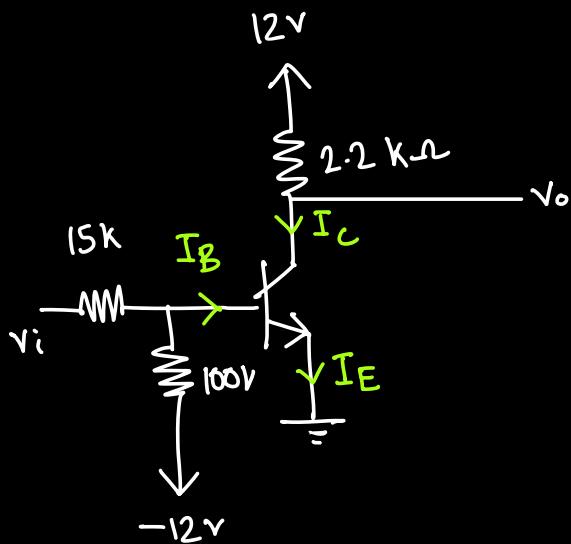
$$v_o = 0.710V$$



$$\begin{aligned}
 & \text{Power during max} \\
 & P_{\text{out}} = \frac{I^2 \cdot 0.7054}{100k} \\
 & = \\
 & P_1 = \frac{(S - 0) I_2}{100k} \\
 & + P_2 = \frac{(S - 0) I_3}{100k} \\
 & P_1 + P_2 = P_{\text{max}}
 \end{aligned}$$



For RTL inverters



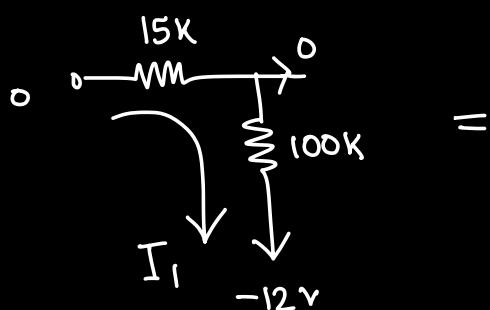
Same method

figure cases

Case ① $V_i = 0$ cutoff

$$I_B = I_C = I_E = 0$$

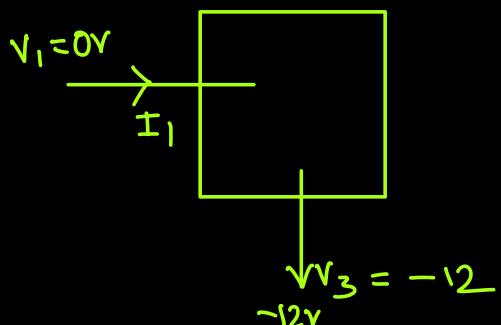
only current flow in ckt



$$\frac{0 - -12}{(15 + 100)k} = I_i$$

$$I_i = 0.104 \text{ mA}$$

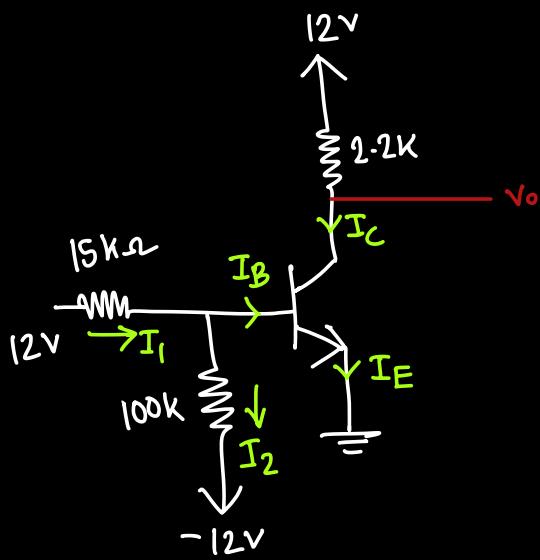
power dissip.



$$P_i = (0 - -12) \times I_i$$

$$P_i = 1.2521 \text{ mW}$$

Case 11



Saturation mode:

$$\textcircled{1} \quad V_{BE} = 0.8V$$

$$\textcircled{2} \quad V_{CE} = 0.2V$$

$$V_E = 0 \quad \text{in ckt}$$

$$\therefore V_C = 0.2$$

$$\therefore V_B = 0.8$$

$$\frac{12 - V_C}{2.2k} = I_C = \frac{12 - 0.2}{2.2k}$$

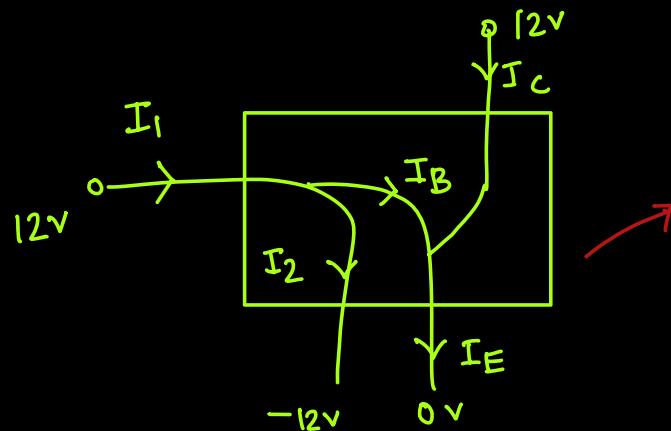
$$= 5.364 \text{ mA}$$

$$I_1 = \frac{12 - 0.8}{15k} = 0.7466 \text{ mA}$$

$$I_2 = \frac{0.8 - -12}{100k} = 0.128 \text{ mA}$$

$$I_B = I_1 - I_2 = 0.6186 \text{ mA}$$

Power dissip.



$I_B, I_2 \rightarrow$ create two outputs

I_1 does not flow through two lines
but divides into I_2 & I_B .

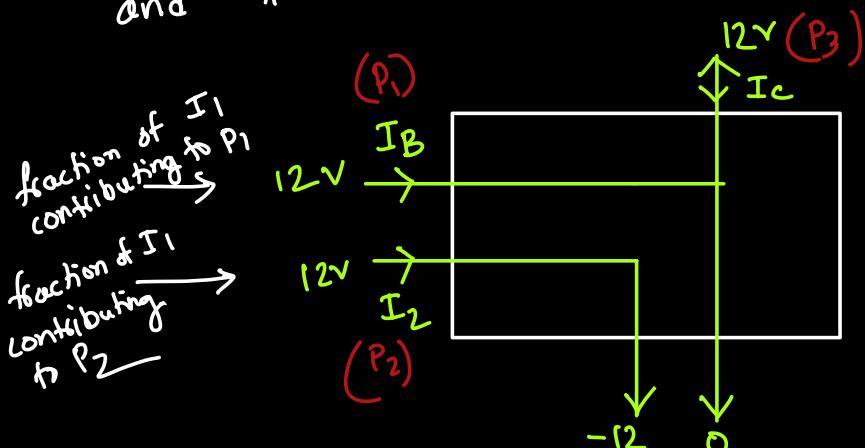
if we write

$$P_1 = I_1 (12V - (-12))$$

$$P_2 = I_1 (12V - 0)$$

wrong! I_1 cannot be considered in two power values. P_1 & P_2 here are not indep. pow. values.
(as if I_1 flows through both lines. wrong)

→ separate $I_1 \rightarrow I_2$ & I_B ($I_1 = I_2 + I_B$) → know that I_1 actually divides into 2 terminals



$$P_1 = (12 - (-12)) \times 0.128 \text{ mW}$$

$$= 3.072 \text{ mW}$$

$$P_2 = (12 - 0) \times 0.6186$$

$$= 7.4323 \text{ mW}$$

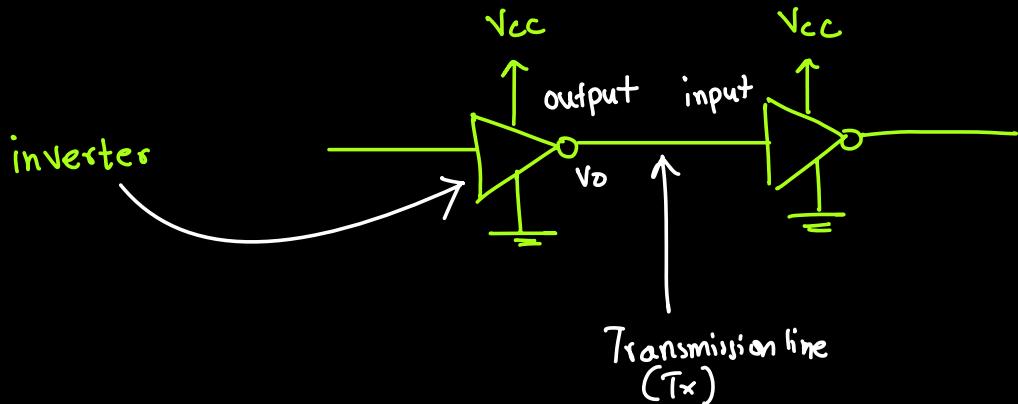
$$P_3 = (12 - 0) \times 5.3636$$

$$= 64.3632 \text{ mW}$$

$$P_{\text{tot.}} = P_1 + P_2 + P_3 = 74.8584 \text{ mW}$$

(max!)

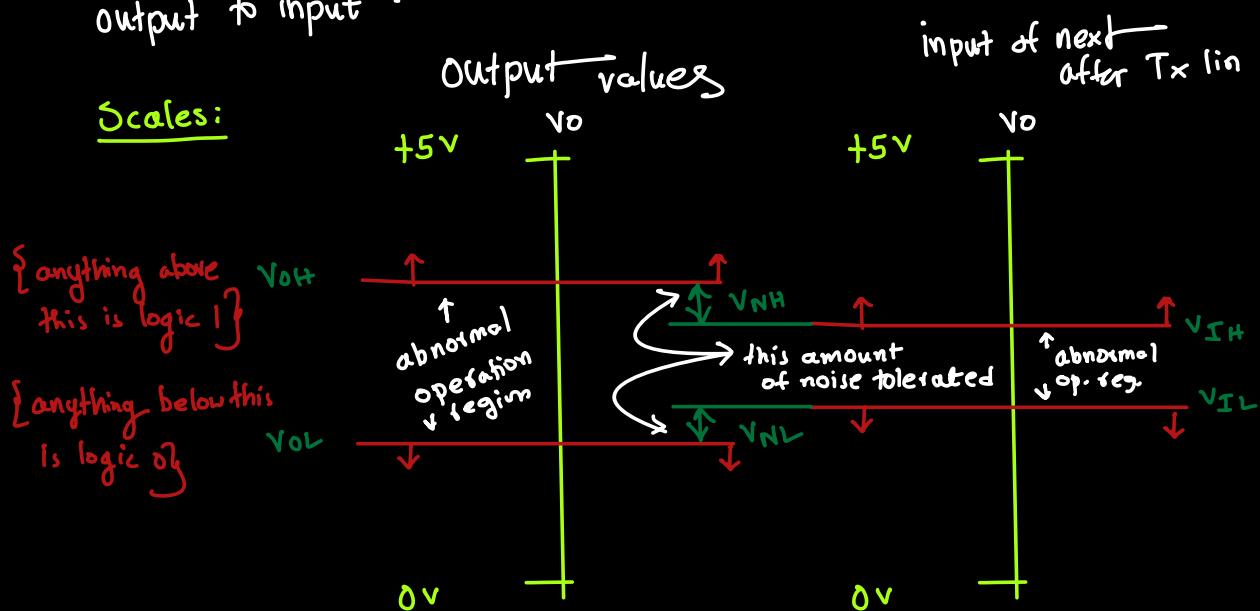
Noise Margin



external interference, noise can hamper signal transmission.

- What is noise margin?

The max. amount of noise voltage that can be tolerated by a circuit while completing a successful transmission from output to input.



V_{NH} = high state noise margin

V_{NL} = Low " " "

even if noise in Tx line is added in the extra noise
decreases V_{OH} by $\leq V_{NH}$ system will work

even if noise in Tx line is added in the extra noise
increase V_{OL} by $\leq V_{NL}$ system will work

$\rightarrow \therefore$ high state noise margin: $V_{NH} = V_{OH} - V_{IH}$

Low state noise margin: $V_{NL} = V_{IL} - V_{OL}$

defn

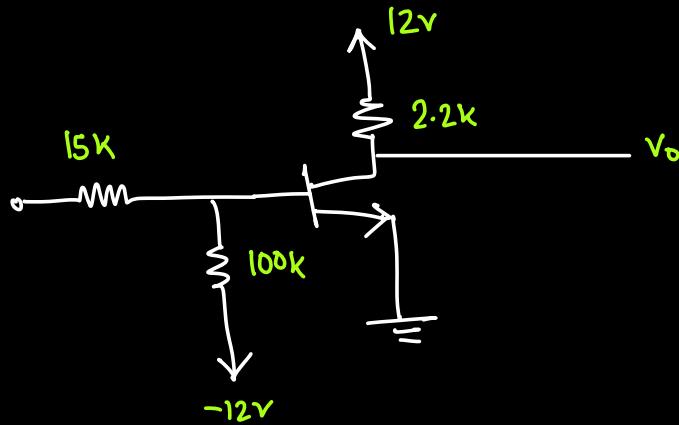
V_{OH} : min Volt. level at output in a logical 1 state
under defined load condition

V_{OL} : max Volt. level at an output in the logical 0 state
under defined load condition.

V_{IL} : Same as V_{OL} except input \swarrow

V_{IH} : " " V_{OH} " input \swarrow

Example using RTL



in saturated logic families : $V_{OL} = 0.2V$
 $V_{OH} = \text{will be given}$

e.g. Given

"The output voltage might drop 0.5V from max. V"

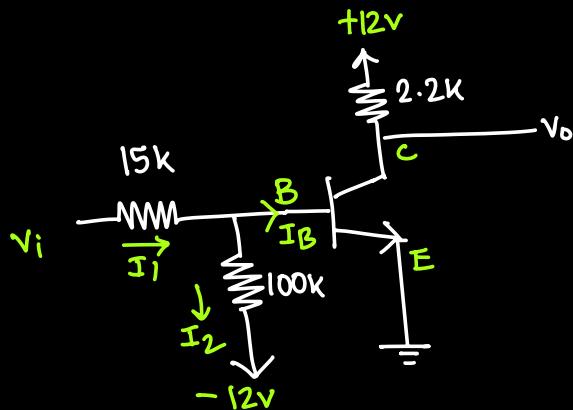
$$V_{O\max} = 12V$$

$$\therefore V_{OH} = 12 - 0.5 = 11.5V \quad (\text{now you know!})$$

V_{IL} , V_{IH} will not (usually) be given, and maybe asked to be found in a question.

V_{IL} calculation: "max V we can apply at input keeping Transistor off & V_o at high (NOT gate)"

Think at input when calculating V_{IL} or V_{IN} .



- $V_{BE} = 0.5V$ (as $V_{BE} \leq 0.5V$ cut-off, $V_{BE} = 0.5V$ verge of being on)

Cutoff

$$\textcircled{1} \quad I_B = I_C = I_E = 0$$

~~KCL~~ $\therefore I_1 = I_2 \quad (\text{as } I_B = 0)$

$$V_{BE} = 0.5V$$

$$\& V_E = 0 \text{ (gnd)}$$

$$\therefore V_B = 0.5V$$

$$I_2 = \frac{V_B - -12}{100k}$$

$$I_2 = \frac{0.5 - (-12)}{100k} = 0.125mA$$

$$I_1 = \frac{V_i - 0.5}{15k} = 0.125mA$$

$$V_i = 0.5 + 15 \times 0.125 = 2.375V$$

* This voltage is max. we can apply to the inverter without turning on T

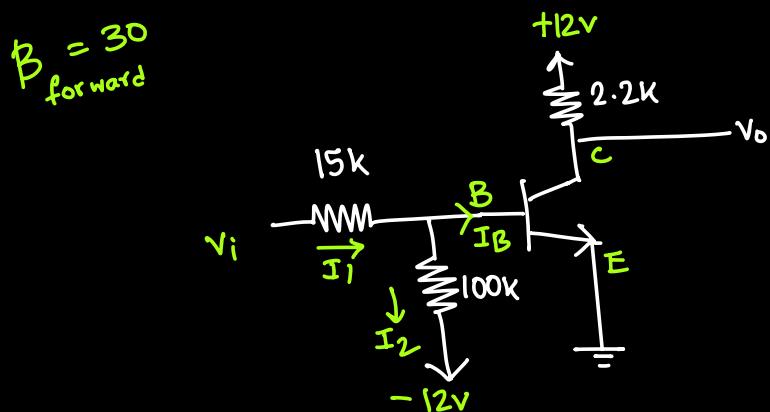
$\therefore V_{IL} = 2.375$ (max V to be considered as input low!)

- even if noise is $0V < \text{noise} < 2.375$ for a $0V$ ideal input
the system will operate correctly.
- $\text{noise} > 2.375$ will disrupt and erroneously flip output to
a wrong state.

V_{IH} Calculation

The min. high voltage that we can apply to the input so that transistor is still in saturation mode

x make sure it does not → change modes : Forward active for e.g.



→ Locate boundary point, decrease V_i such that it is at the verge of moving from saturation to forward active!

$$\text{i.e } \beta_{\text{forced}} = \frac{I_C}{I_B} \approx B_{\text{FORWARD}}$$

$$I_C = \frac{12 - 0.2}{2.2k} = 5.3636 \text{ mA}$$

$$\beta_{\text{forced}} \approx \beta_{\text{FWD}} = 30$$

$$\therefore 30 = \beta_{\text{forced}} = \frac{I_C}{I_B}$$

$$I_B = 0.1788 \text{ mA}$$

$$I_2 = \frac{0.8 - 12}{100k} = 0.128 \text{ mA}$$

$$\frac{V_i - 0.8}{15k} = I_1 = 0.3068$$

$$\therefore V_i = 0.8 + 0.3068 \times 15 = 5.4018 \text{ V}$$

$$V_{IH} = 5.4018 \text{ V}$$

- even if noise decreases V_i to 5.4018 V from 12 V (ideal) Transistor will still be in sat. mode and input still high.
- But if noise decreases V_i to less than 5.4018 V from 12 V (ideal) Transistor will no longer be in cutoff and input → will be such that output state will be wrong.
(abnormal op. region)
- Now since we know V_{IH} , V_{IL}

$$V_{NH} = 11.5 - 5.4018 = 6.0982 \text{ V} \leftarrow \text{high noise margin}$$

$$V_{NL} = 2.375 - 0.2 = 2.175 \text{ V} \leftarrow \text{low noise margin}$$

$$\text{Noise Margin} = \min(V_{NH}, V_{NL}) = 2.175V$$

Take minimum this means the gap for that between output - input as if that is the noise level, both V_{NH} , V_{NL} will not be violated.

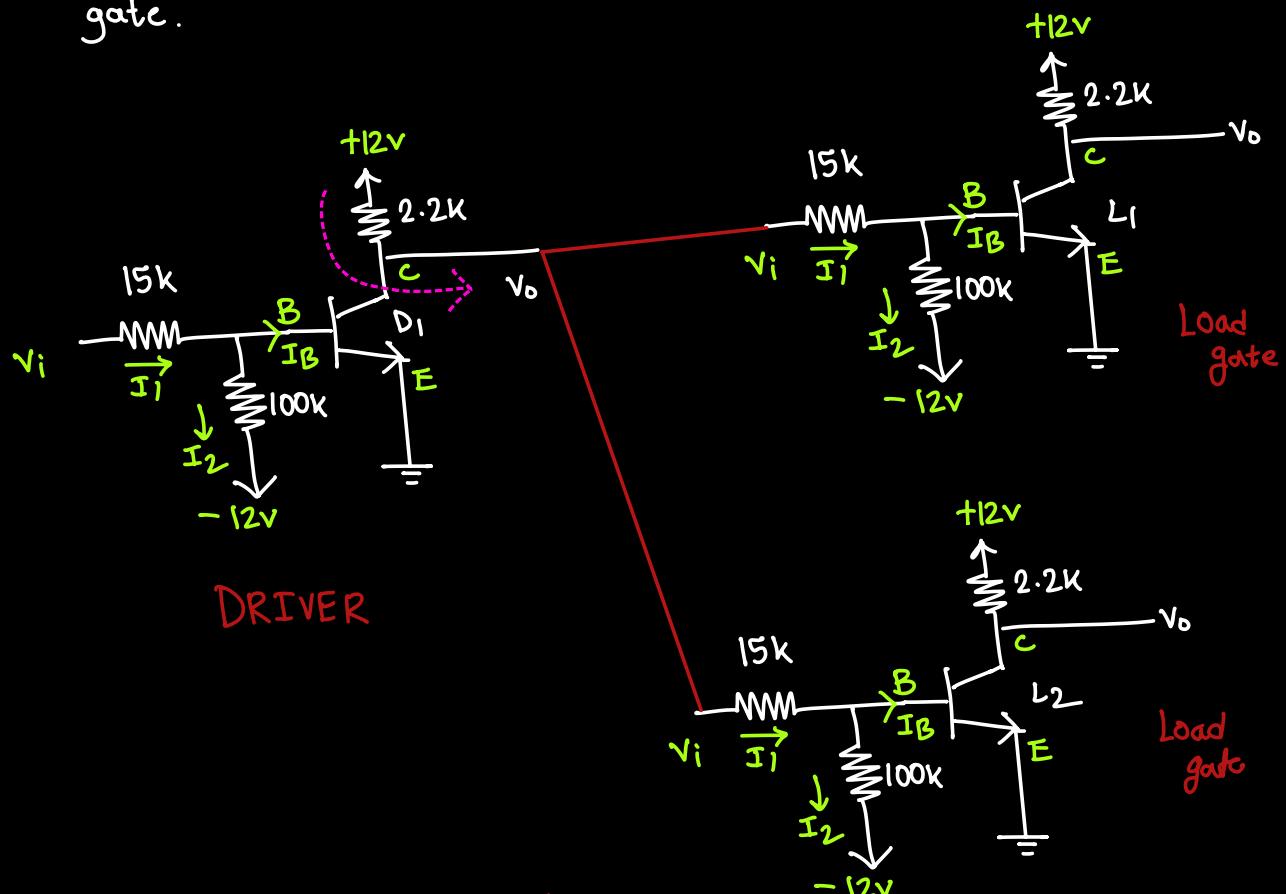
If the larger margin taken then the other "smaller" margin will be violated.

Fanout

maximum number of logic input (of same logic family) that an output can drive reliably is called maximum fanout

calc. fanout \longrightarrow max fanout

fanin : how many input terminals are there in a logic gate.



maximum load gates this driver can drive, reliably \longrightarrow fanout

Driver gate : supplies current

Load gate : consume "

Calculations of fan-out varies with Logic families

Constraints

individual demand (current) from each load circuit/gate.

max. current that can be supplied by driver

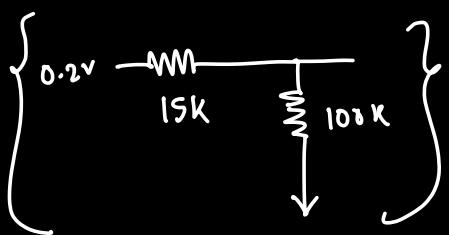
case I

Driver output low $V_{OL} = 0.2V$

$$\times \text{Max. total supply} = \frac{V_C - V_O}{2.2k} = \frac{12 - 0.2}{2.2k} = 5.3636 \text{ mA}$$

why?
- input low
x individual load current demand. $= \frac{0.2 - 12}{115k} \approx 0.106 \text{ mA}$

(Load ckt in cut-off)



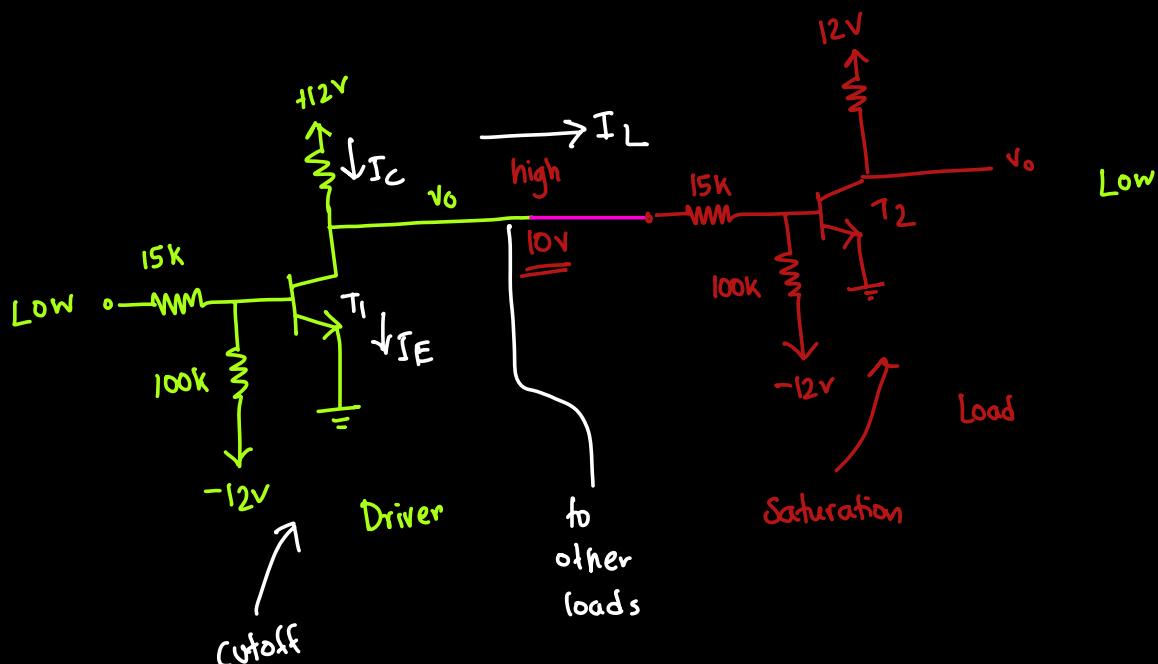
\therefore max no. of load cks that our driver can support

$$= \frac{\text{individual load demand}}{\text{max driver load supplied}}$$

$$= \frac{5.3636}{0.106} = \lfloor 50.6 \rfloor \rightarrow \text{we use floor! } 50!$$

case (II)

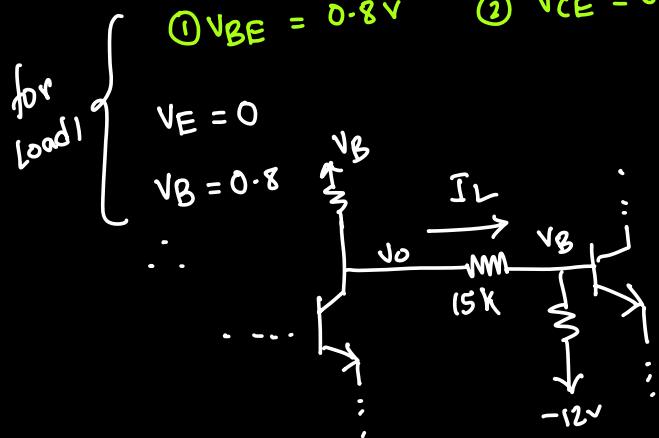
Driver output high $V_{OH} = 10V$



$$\text{Maximum Supply current} = \frac{12-10}{2.2k} = 0.909 \text{ mA}$$

Load transistors are all in saturation mode:

$$① V_{BE} = 0.8V \quad ② V_{CE} = 0.2V$$



$$I_L = \frac{v_o - v_B}{15k} = \frac{10 - 0.8}{15k}$$

$$I_L = 0.6133 \text{ mA}$$

$$\begin{aligned} \text{Max. fanout} &= \frac{0.909}{0.6133} = \boxed{1.48} \\ &= 1 \text{ load only!} \end{aligned}$$

Only 1 Load possible, otherwise V_{OH} will fall.

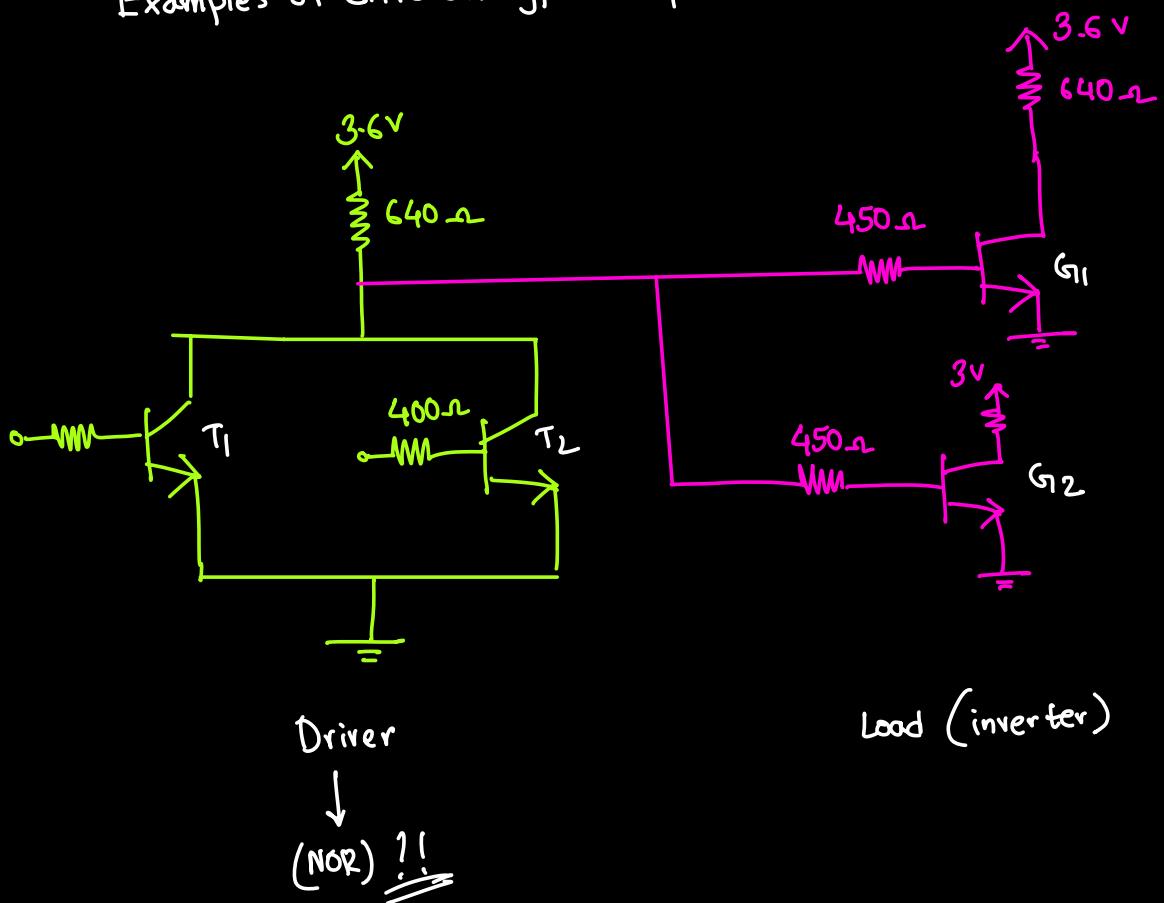
Now

Overall maximum fanout must be calculated by considering worst case scenario.

To prevent malfunction of driver circuit, we need to take the minimum of two cases

$$\text{in this case maximum fanout} = \min(50, 1) = 1$$

Examples of different types of problems from this part



Both are RTL circuits → from saturated Logic families

How to detect RTL?

① Resistor connected to input terminal

② That resistor is also connected to the transistor

if both fulfilled → RTL (sat.-logic family member)

→ Once RTL detected :

- switch transistors will operate at

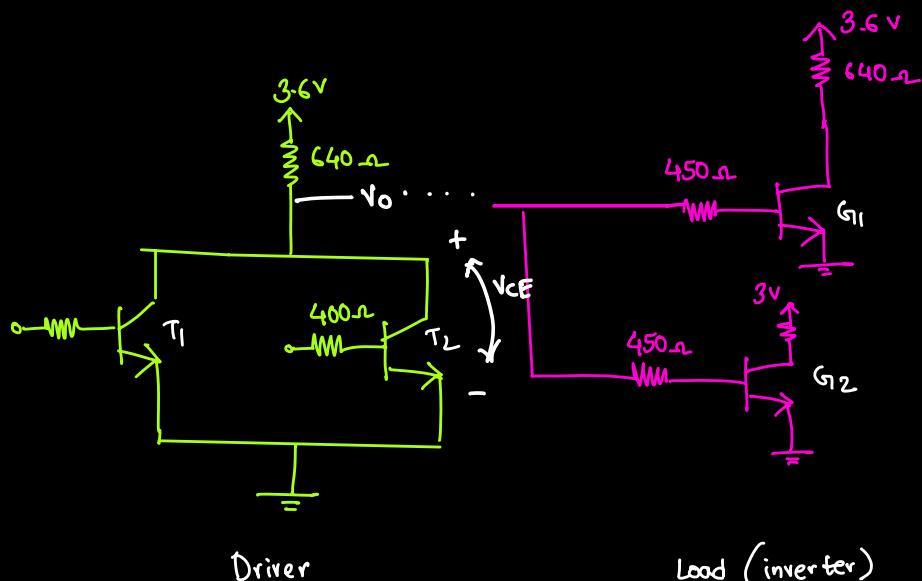
- ① set for input high
- ② cutoff for input low

Question

Given no. of fanout is 5.

Find the minimum value of B_{forced} , so that these ckts operate as NOR gate.

Assume all transistors have same B values.



Disconnect driver from load. Consider driver separately.

A Logic	B Logic	A A	B B	T ₁	T ₂	V _O (=V _{CE})	V _O Logic	
1	1	3.6	3.6	Sat.	Sat.	0.2	0	$V_{CE}(\text{sat}) = 0.2V$
1	0	3.6	0	Sat.	C.	0.2	0	Driver
0	1	0	3.6	C.	Sat.	0.2	0	acting as NOR Gate!
0	0	0	0	C	C	3.6	1	

Q1. Why didn't we verify sat./cutoff modes?

Here B_{forward} is not given.

We have to make this ckt work as a NOR gate.

\therefore We need them to work at saturation/cutoff.

We will find B_{forced} and say for example B_{forward} for the Transistors used MUST be larger so that sat. mode exist

$\&$ this ckt acts as an NOR GATE.

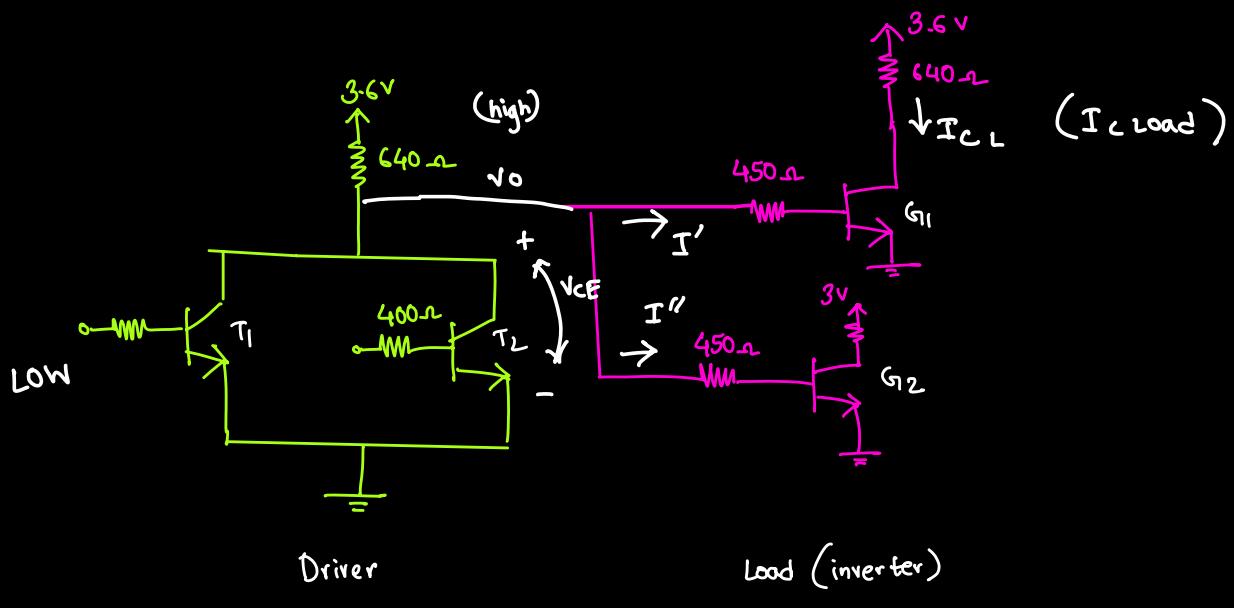
\therefore This is a design problem \rightarrow we determine what Transistor (as in what B valued Transistor we need) to make this act like a NOR gate.

Now connecting V_o to load part... (driver-load connection)

- For $V_o = 0.2V$ (Low), $V_{CE} = 0.2V$ @ sat. so that

does not change.

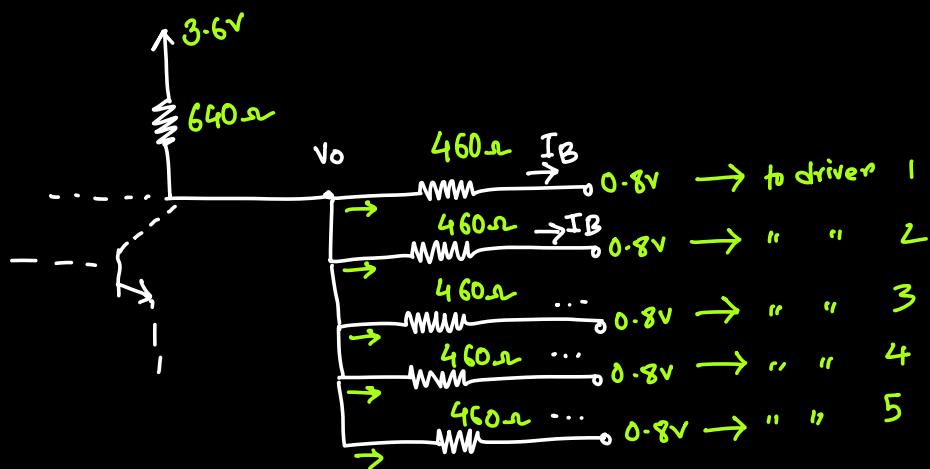
- For $V_o = 3.6V$ (high), Load ckt_s will draw some current and thus reduce the ideal 3.6V of V_o .



$\Rightarrow T_1 \text{ & } T_2$ both off at input low, \therefore driver $G_1 - G_5$ saturated

Since fan-out = 5 $G_1 - G_5$ exists (although we showed $G_1 \text{ & } G_2$)

$$\text{(collector current of load)} \quad I_{CL} = \frac{3.6 - 0.2}{0.64K} = 5.3125 \text{ mA} \quad \checkmark$$



Perform node-analysis at V_o .

$$\frac{V_o - 0.8}{460} \times 5 + \frac{V_o - 3.6}{640} = 0$$

$$V_o = 1.1452 \text{ V}$$

individual base current for Load, $I_{BL} = \frac{V_o - 0.8}{0.46k}$ for each load

$$I_{BL} = 0.767 \text{ mA}$$

$$\beta_{\text{forced}} = \frac{I_{CL}}{I_{BL}} \text{ for load} = \frac{5.3125}{0.767} = 6.9263$$

Answer

We will need β_{Forward} of the used transistors to be larger than 6.9263 .

\therefore Load circuits will remain at saturation ($\beta_{\text{Fwd}} \gg \beta_{\text{forced}}$)

\therefore our ckt will act as a NOR gate.

$$\therefore \beta_{\text{min}} = 6.9263$$

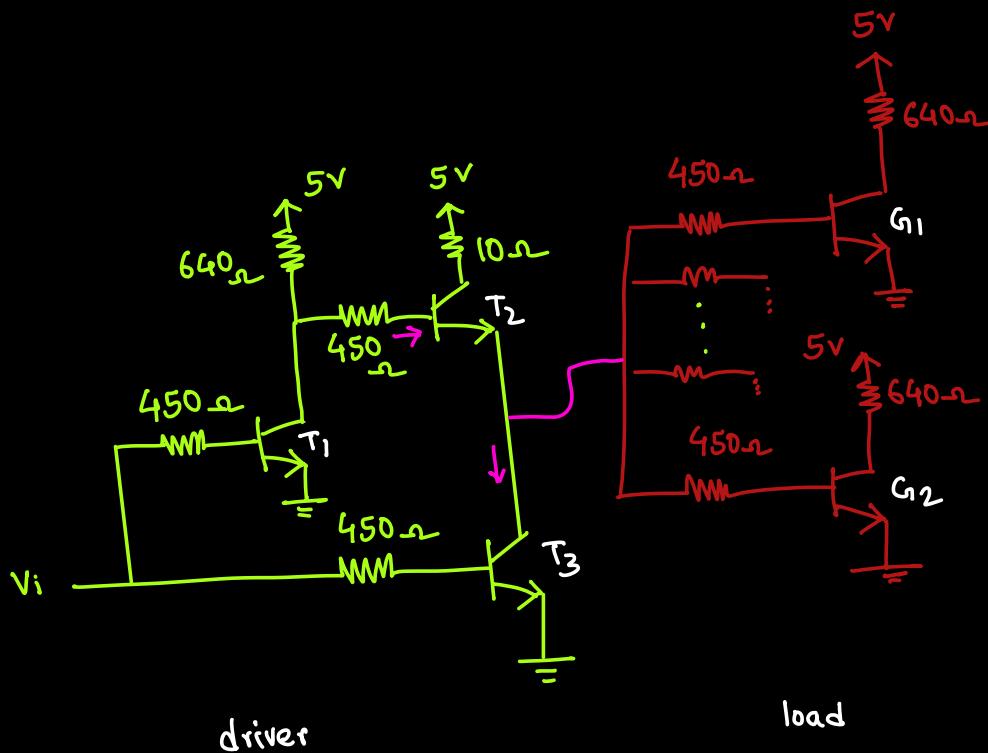
(forward)

Example Problem

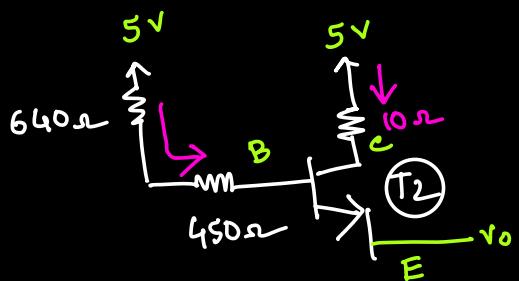
important for tests!

- ④ The following circuit "boosts" the value of maximum fanout for regular RTL inverters.

"Buffer ckt" : alternative name



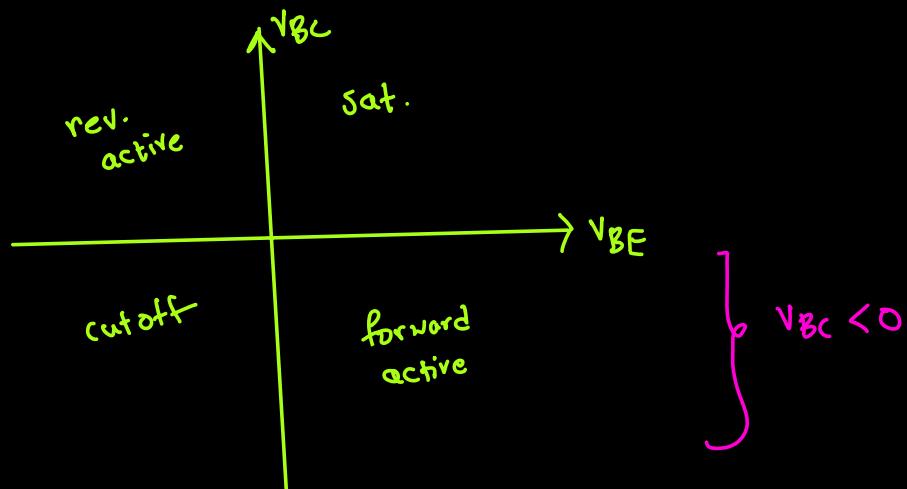
Hints: $V_i = 0V$ $T_1, T_3 \rightarrow \text{cutoff}$, But $T_2 = ?$



as collector resistance small
 $V_C \approx 5V$ (Low drop across Resistor)
 $\therefore V_C > V_B$
 as $V_B < 5V$ as $(640 + 450)\Omega$ is a substantial resistance will high potential drop

$$\therefore V_B - V_C < 0 \quad \therefore V_{BC} < 0$$

remember the quadrant for V_{BC} & V_{BE} .



Thus T_2 will be in forward active mode.

$$\therefore \text{for } T_2 \quad I_c = \beta_F \cdot I_B$$

$$I_E = (I_B + I_c) = (\beta_F + 1) I_B$$

$$I_B = \frac{5 - (10 + 0.7)}{640 + 450}$$

$$I_E = (\beta_F + 1) I_B = \text{supply curr.}$$

Then find fan-out—