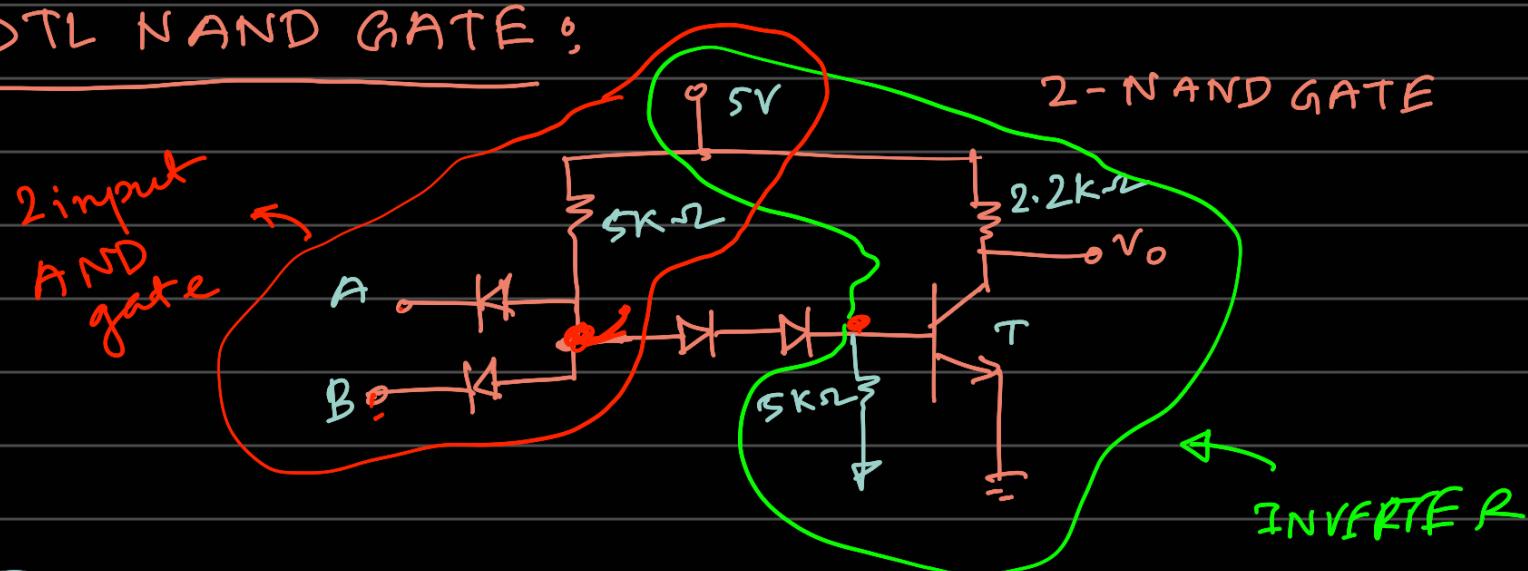


## # DTL (Diode Transistor Logic)

\* Bipolar  $\rightarrow$  Saturated (switching) transistor will be operating in cutoff or saturation.

\* [Input terminals connect through diodes to the <sup>v</sup> switching terminal.]

### DTL NAND GATE:



### BASIC OPERATION:



This is the basic structure.

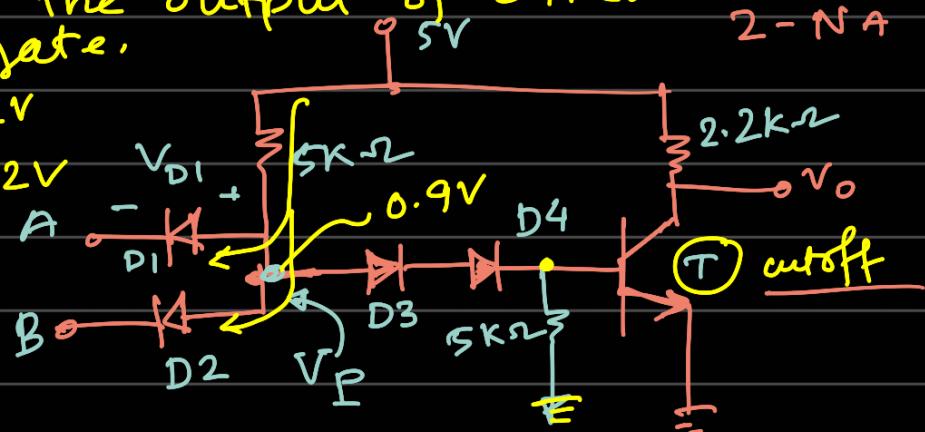
# Calculate the currents and node voltages for the following DTL gate. Verify it is a NAND gate. Input stages might be

Ans: Connected to the output of other DTL NAND gate.

Case ①.  $V_A = \text{Low} = 0.2V$

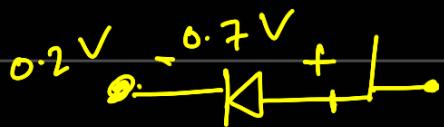
$$V_B = \text{Low} = 0.2V$$

Assume, the anode voltage  $V_p$  might be higher



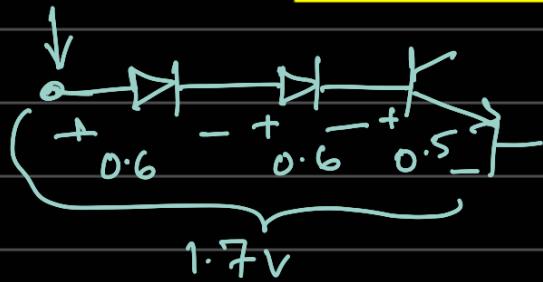
than the cathode voltages of D1 and D2 diode.

So, D1 and D2 are conducting. Thus.  $V_{D1} = 0.7V$



Therefore, according to the assumption  $V_p = 0.2 + 0.7 = 0.9V$

(#) In order for T transistor to turn on we need to have  $V_{BE} \approx 0.5V$  (cut-in voltage of transistors), we also need to have  $V_{D3} = V_{D4} \approx 0.6V$  (cut-in voltage for diodes). As a total we require  $V_{D3} + V_{D4} + V_{BE} \approx 1.7V$  at P mode to



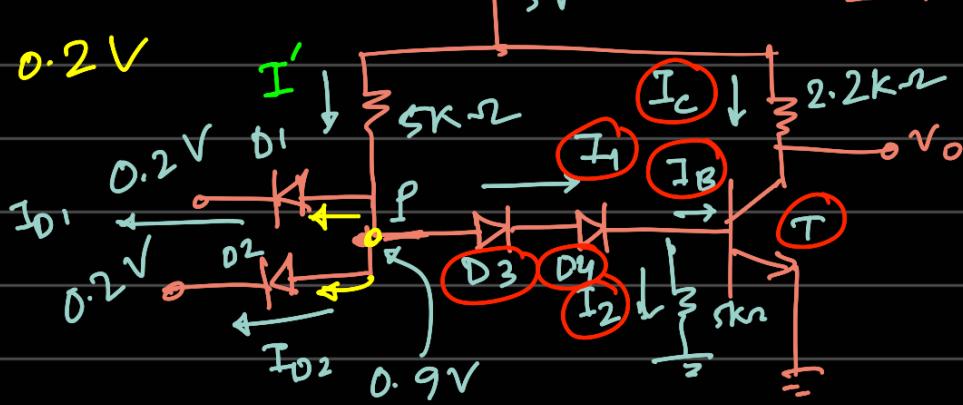
turn on the right side of the circuit.

If  $V_p = 0.9V$ , then T could not turn on. This justifies our assumption.

Now we can calculate the current and voltages.

Case ①

$$V_A = V_B = 0.2V$$

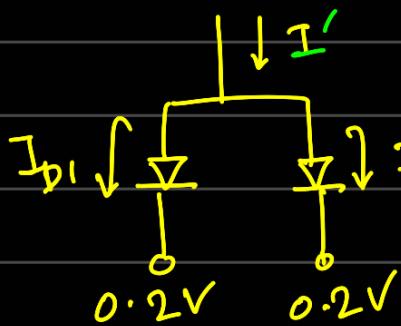


2-NA

$T \rightarrow$  cutoff.  $D_1, D_2 \rightarrow$  conducting.  $D_3, D_4 \rightarrow$  off

$$V_p = 0.9V. \quad I_c = I_b = 0. \Rightarrow V_o = 5V$$

$$I'_p = 0, \quad I_{D2} = 0, \quad I' = \frac{5 - 0.9}{5k} = \frac{4.1}{5k} = 0.82mA$$



$I_{D1} = I_{D2}$  because both of the branches are identical.

$$I_{D1} = \frac{I'}{2} = 0.41mA = I_{D2}$$

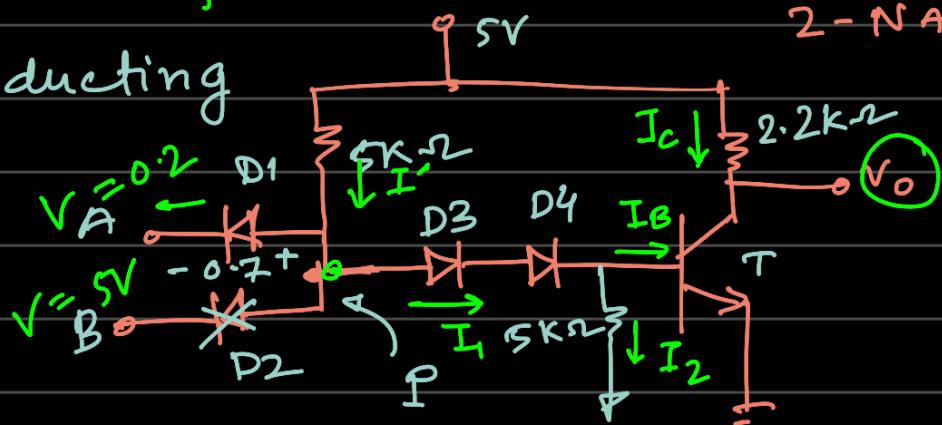
Case ②

$$\begin{array}{l|l} V_A = 0.2V & V_B = 0.2V \\ \hline V_B = 5V & V_A = 5V \end{array} \left. \begin{array}{l} \\ \end{array} \right\} \text{Similarly.}$$

Assume,  $D_1$  is conducting  
and  $D_2$  is off.

This implies.

$$V_p = 0.9V$$



2-NA

# we need at least  $V_p \geq 1.7V$  to turn on  $T$

transistor. It again justifies our assumption

#

$$I_c = I_b = I_1 = I_2 = 0mA,$$

$$I' = 0.82mA$$

$$I_{D2} = 0mA, \quad I_{D1} = 0.82mA, \quad V_o = 5V, \quad V_B = 0V$$

Case 3  $V_A = V_B = 5V$

Assume  $D_1, D_2$  are off.

$$I_{D1} = I_{D2} = 0 \text{ mA}$$

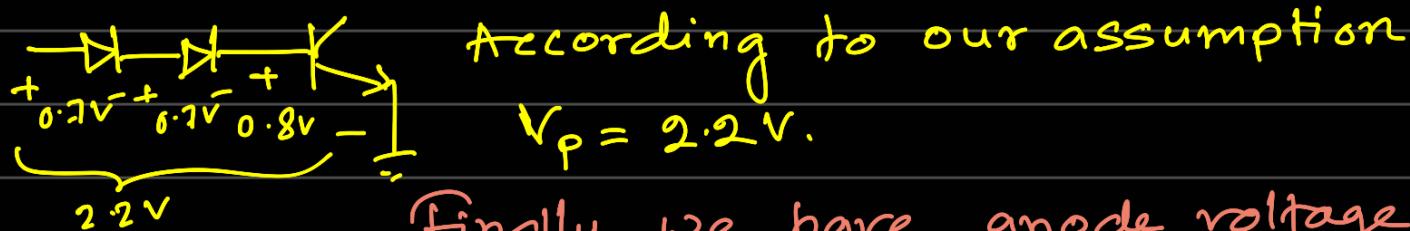
Therefore,

$D_3, D_4$  and

$T$  must be ON.

Because it is a DTL circuit. The switching transistor must operate in saturation mode when it is turned on.  $V_{CE} = 0.2V, V_{BE} = 0.8V$

$$V_{D3} = V_{D4} = \underline{\underline{0.7V}} \quad [\text{Conduction voltage of diode}]$$



Finally we have anode voltage of  $D_1$  and  $D_2$  is smaller than cathode voltage. This justifies our assumption.

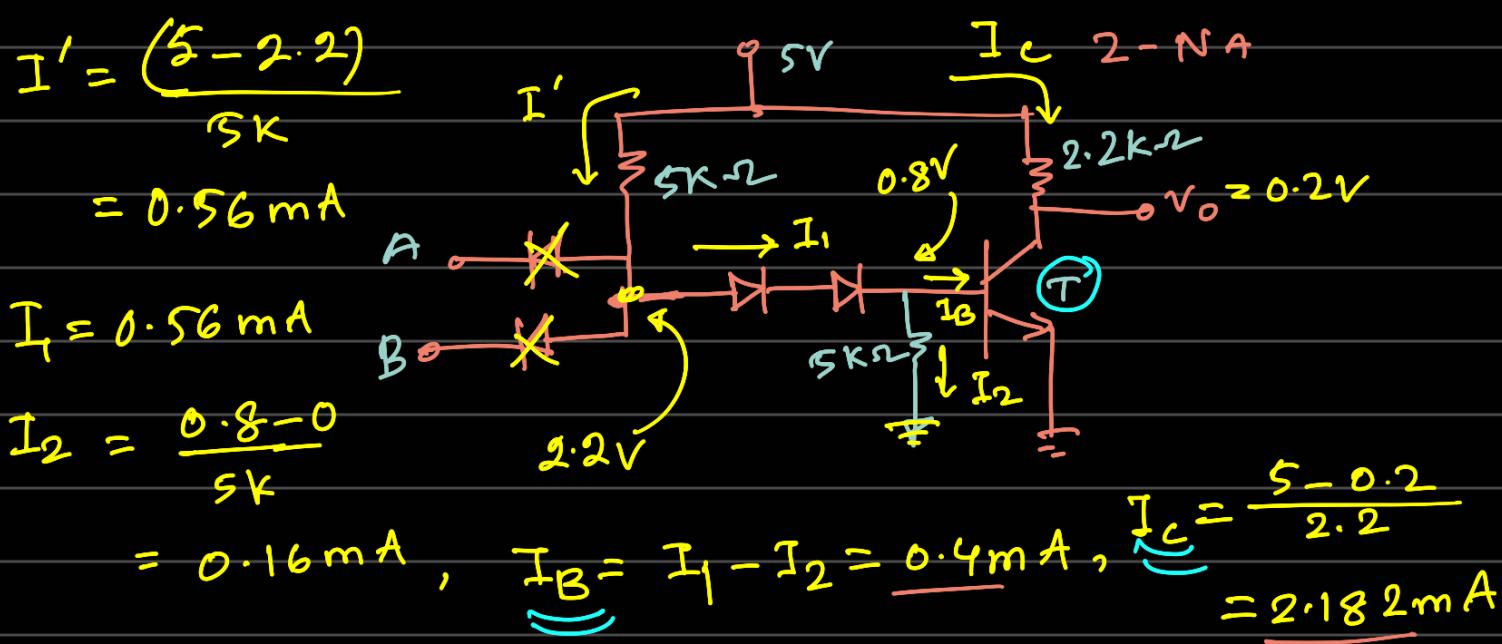
# Current calculation :-

$$I' = \frac{(5 - 2.2)}{5K} = 0.56 \text{ mA}$$

$$I_1 = 0.56 \text{ mA}$$

$$I_2 = \frac{0.8}{5K} = 0.16 \text{ mA}$$

$$I_B = I_1 - I_2 = 0.4 \text{ mA}, I_C = \frac{5 - 0.2}{2.2} = 2.182 \text{ mA}$$



From analyzing the cases we can clearly conclude this circuit is a NAND gate.

Lecture 6: DTL Noise margin, Fanout and modified DTL and HTL circuits.

$\beta_{min}$  = the minimum value of  $\beta_F$  of the switching transistor T, that will keep the circuit operation error free.

# Case ① and ② will not help us to determine the  $\beta_{min}$ , because in both of those cases transistor is turn off.

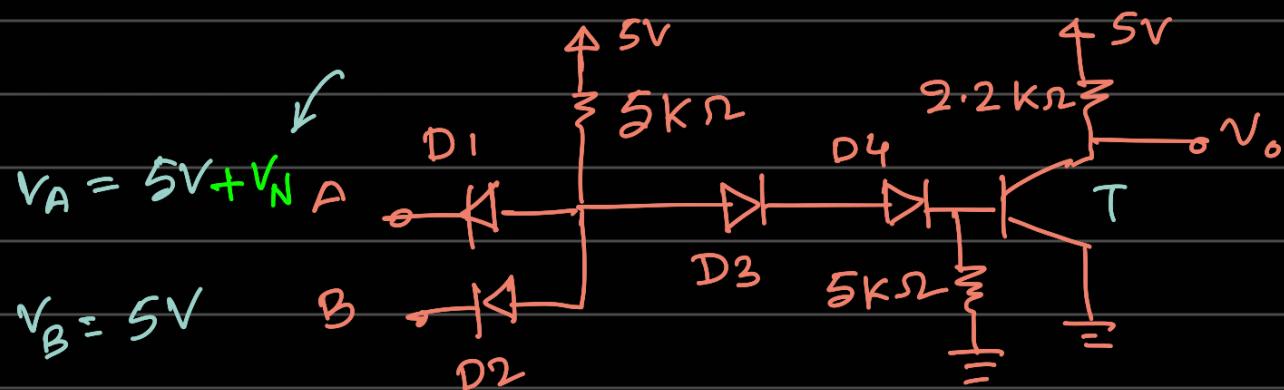
However, for case ③, transistor is on and operates in saturation mode. Therefore, to maintain correct operating we must choose a value of  $\beta_F$  that is higher than  $\beta_{forced}$ .

minimum value allowed for  $\beta_F = \beta_{forced} = \beta_{min}$

$$\beta_{min} = \frac{I_c}{I_B} (\text{sat}) = \frac{2 \cdot 182}{0.4} = 5.46$$

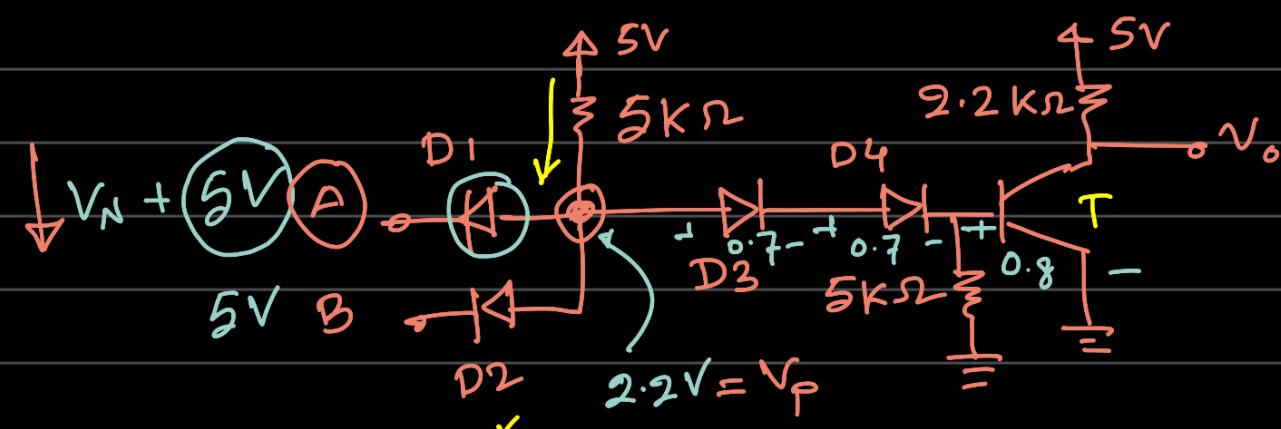
IV Noise margin Calculation:

\* NM calculation for DTL is not similar to the RTL circuit.

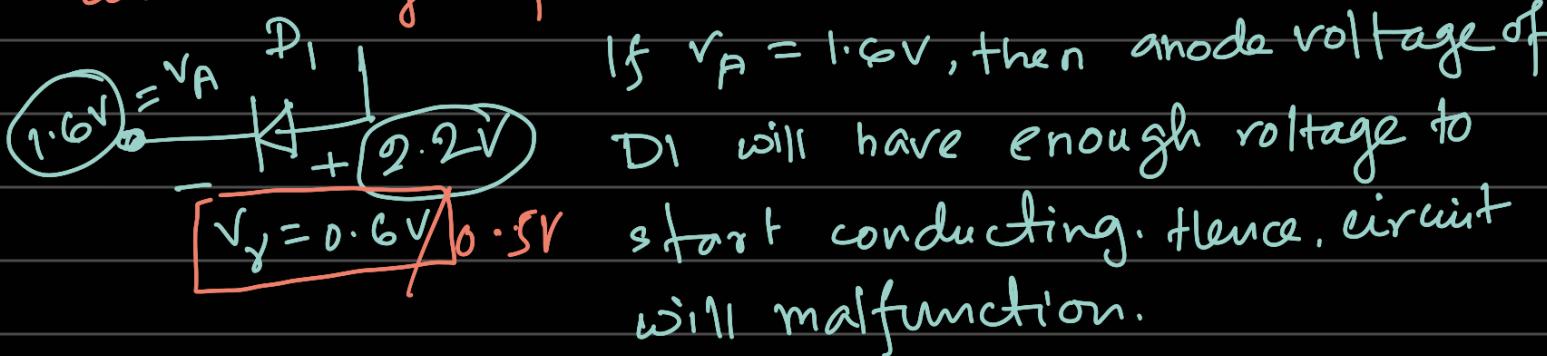


- ⑧ If all the inputs are high, what is the magnitude of noise voltage which will cause the gate to malfunction?
- noise voltage can be positive or negative
- # Correct operating condition when all inputs are high. Case ③. D<sub>1</sub>, D<sub>2</sub> off. D<sub>3</sub>, D<sub>4</sub> on. T  $\rightarrow$  sat.
  - # The circuit will malfunction if it starts operating in case ② conditions.  
D<sub>1</sub>, D<sub>2</sub> on, D<sub>3</sub>, D<sub>4</sub>, T off.

If D<sub>1</sub> and D<sub>2</sub> start conducting, they will have precedence over D<sub>3</sub>, D<sub>4</sub> and T because of lower resistance at that direction.

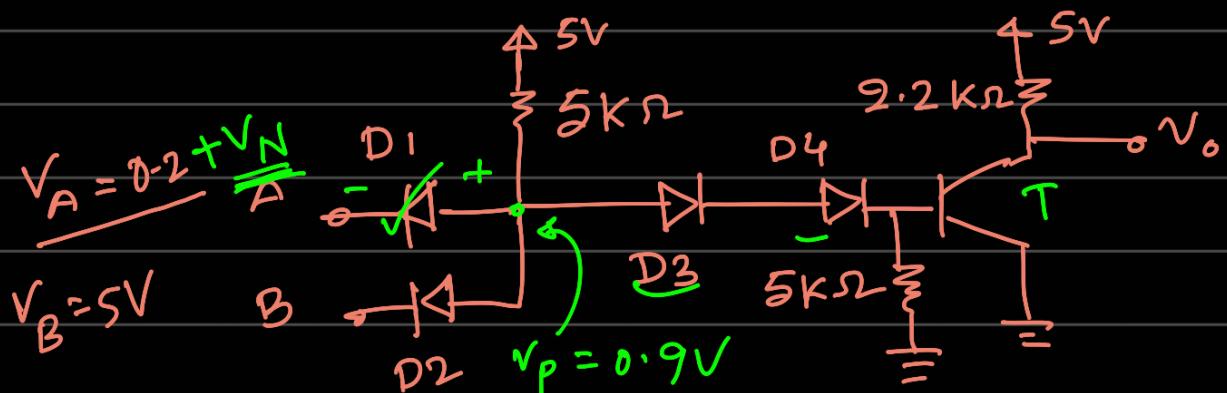


So the circuit will malfunction when the voltage difference V<sub>A</sub> and V<sub>P</sub> is equal to cut-in voltage of diode.



$$V_N + 5 = 1.6 \Rightarrow V_N = -3.4V, V_N = |3.4|V = 3.4V = V_{NH}$$

Q: If one of the inputs is low and others are high, then what magnitude of noise voltage at low input terminal will cause the transistor to malfunction?



# Valid operation: Case ②.  $D_1$  on,  $D_2$ ,  $D_3$ ,  $D_4$ ,  $T$  off.

# The circuit will malfunction if  $D_3$ ,  $D_4$  and  $T$  start conducting or turned on.

# As long as  $D_1$  is on any increment in noise voltage at node A will also increase the voltage at  $V_p$ . Because, the difference between anode and cathode terminal should be 0.7V for conducting diode  $D_1$ .

# If we increase  $V_p$  upto  $1.7V$ , then  $D_3$ ,  $D_4$  and  $T$  will turn on.

$$V_p + V_N = 1.7 \Rightarrow V_N = 1.7 - 0.9 = 0.8 \text{ V}$$

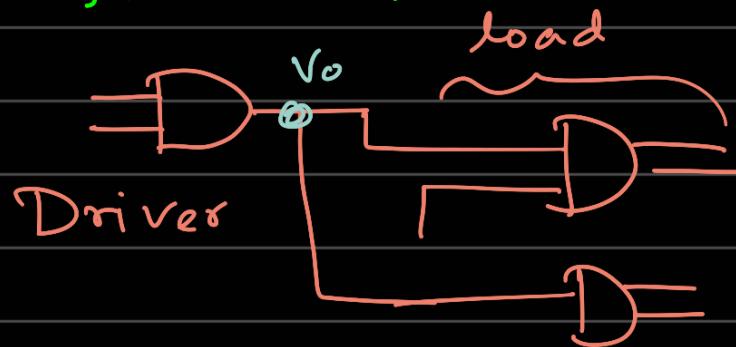
Low noise margin = 0.8V.

Finally, total noise margin,  $NM = \min(NM_L, NM_F) = \min(0.8, 3.4)$

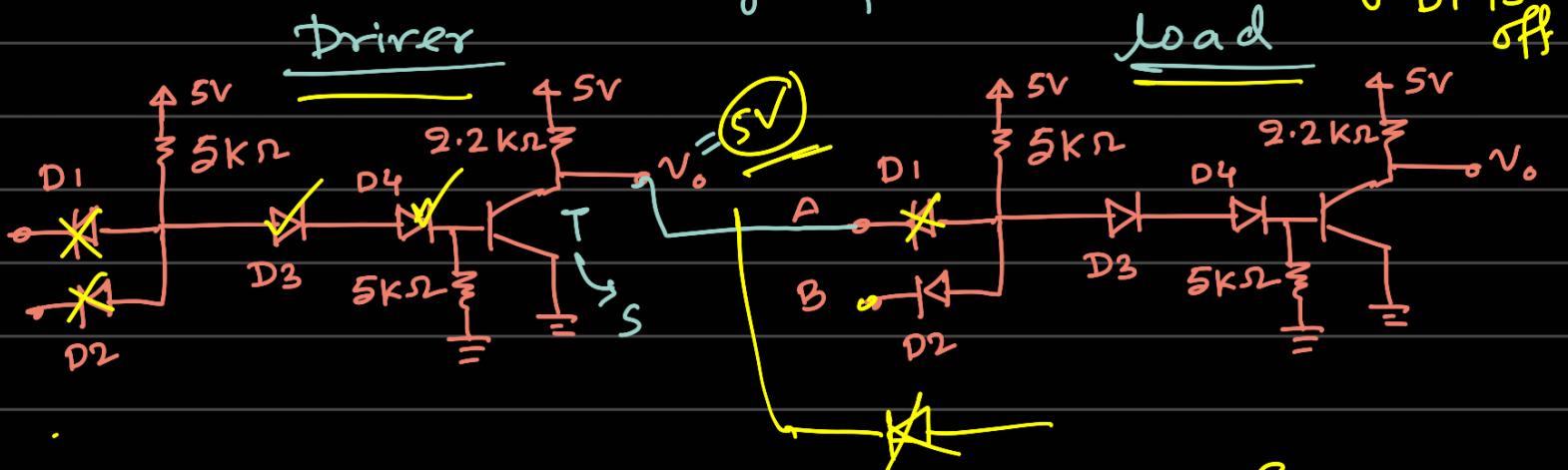
$$NM = 0.8 \text{ V}$$

## Fanout Calculation:

Different from RTL.



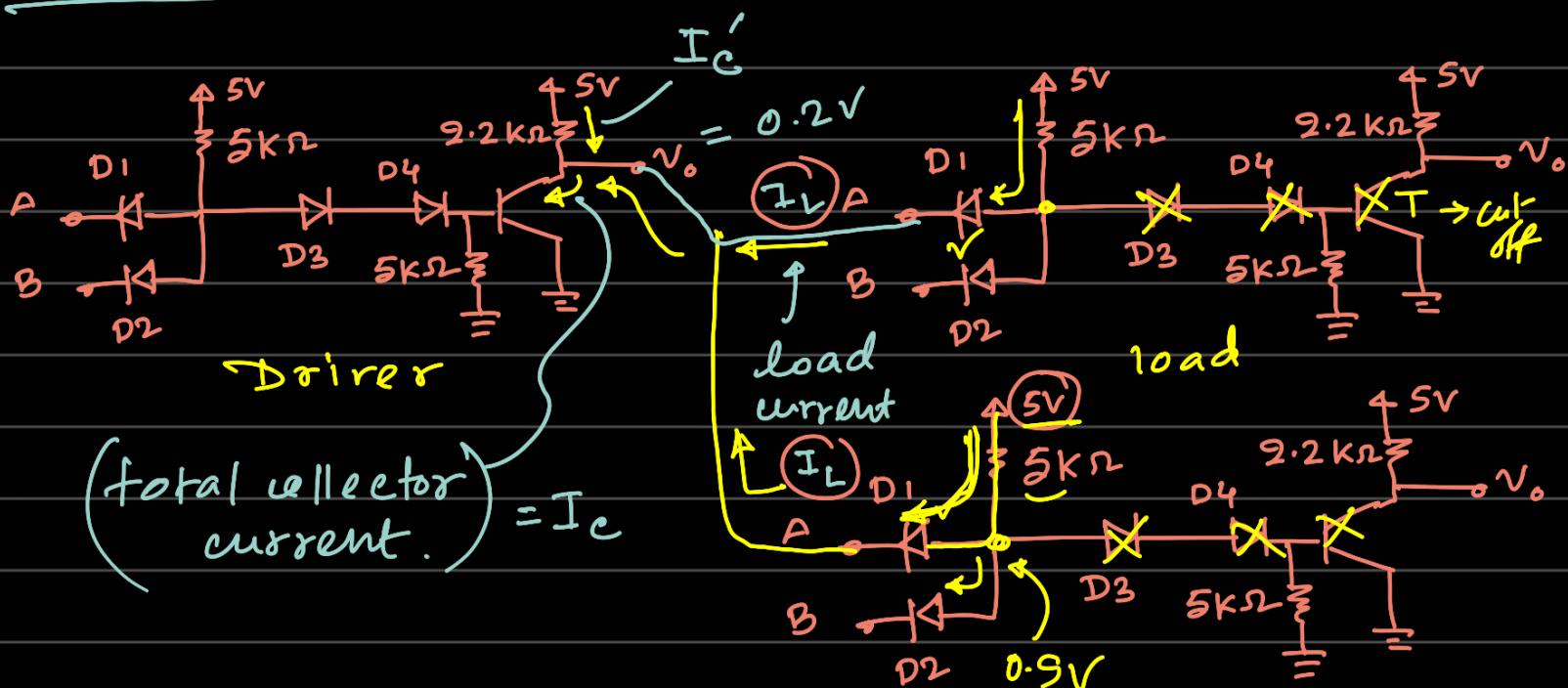
Case ① Output voltage of drivers is high, load  $D_1$  is off.



If  $V_o = 5V$ , then the demand current of the load circuit is zero. Therefore, we can connect as many load circuit as we wish for this case.

$$\text{maximum Fanout} = \infty$$

Case ②  $V_o = 0.2V$



individual load circuit delivers  $I_L$  current.

$I_L$  = standard load

$I_c'$  = no-load collector current

$I_c$  = total collector current.

If the number of fanout =  $N$ ,

$$\text{total collector current } I_c = I_c' + N I_L$$

Constraint: Since the transistor T in driver circuit is saturation mode, the collector current can not cross a certain value.

That will push the transistor T from saturation to forward active mode.

~~⊗~~  $\beta_{\text{forced}} > \beta_F$  [Not in saturation]

①  $\beta_{\text{forced}} \approx \beta_F$  (Edge of sat. and F.A.).

$$I_{c,\max} = \beta_F \times I_B \quad [\beta_{\text{forced}} \approx \frac{I_c}{I_B} \leq \beta_F]$$
$$= 30 \times 0.4 \quad I_c' = 2.182 \text{ mA}$$
$$= 12 \text{ mA}$$

$$I_{c,\max} = I_c' + N \times I_L \quad [N = \max \text{ fanout}]$$

$$\text{Standard load, } \frac{5 - 0.9}{5 \text{ k}\Omega} = 0.82 \text{ mA}$$

$$12 = 2.182 + N \times 0.82$$

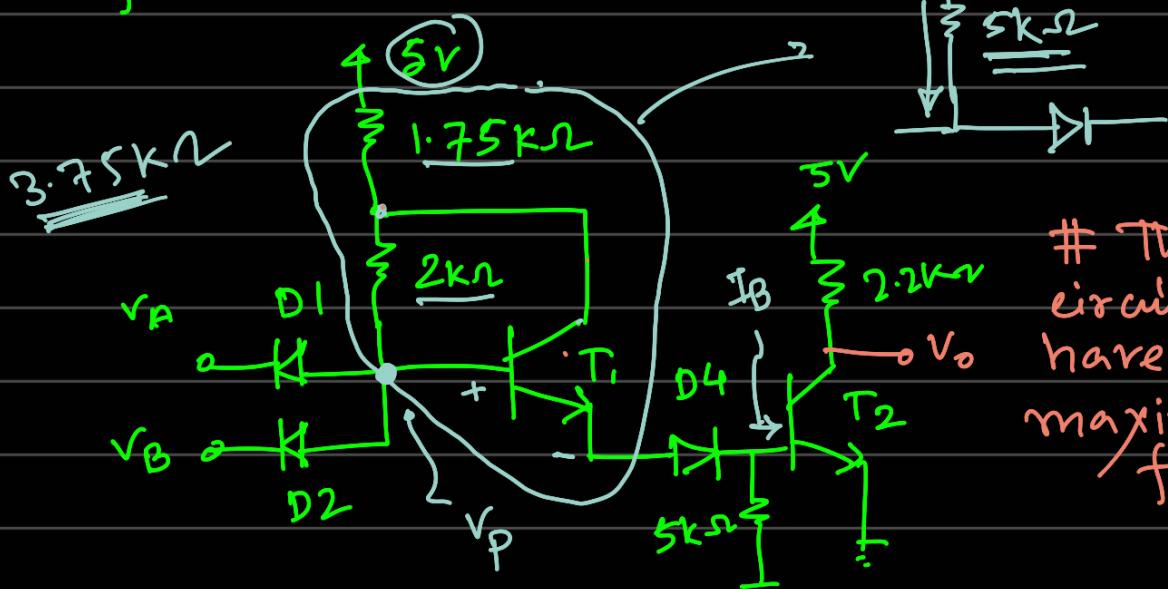
$$\Rightarrow N = 11.97 \approx \cancel{12}$$

We can not choose 12, because in that case collector current will overflow and make transistor T to operate in F.A.

$$\text{So maximum fanout } [11.97] = 11$$

$$\text{Finally, maximum fanout, } \min(11, \infty) \\ = 11.$$

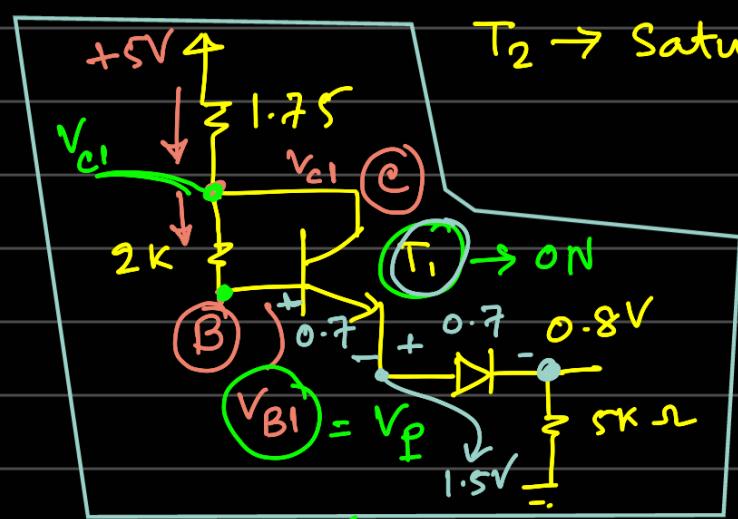
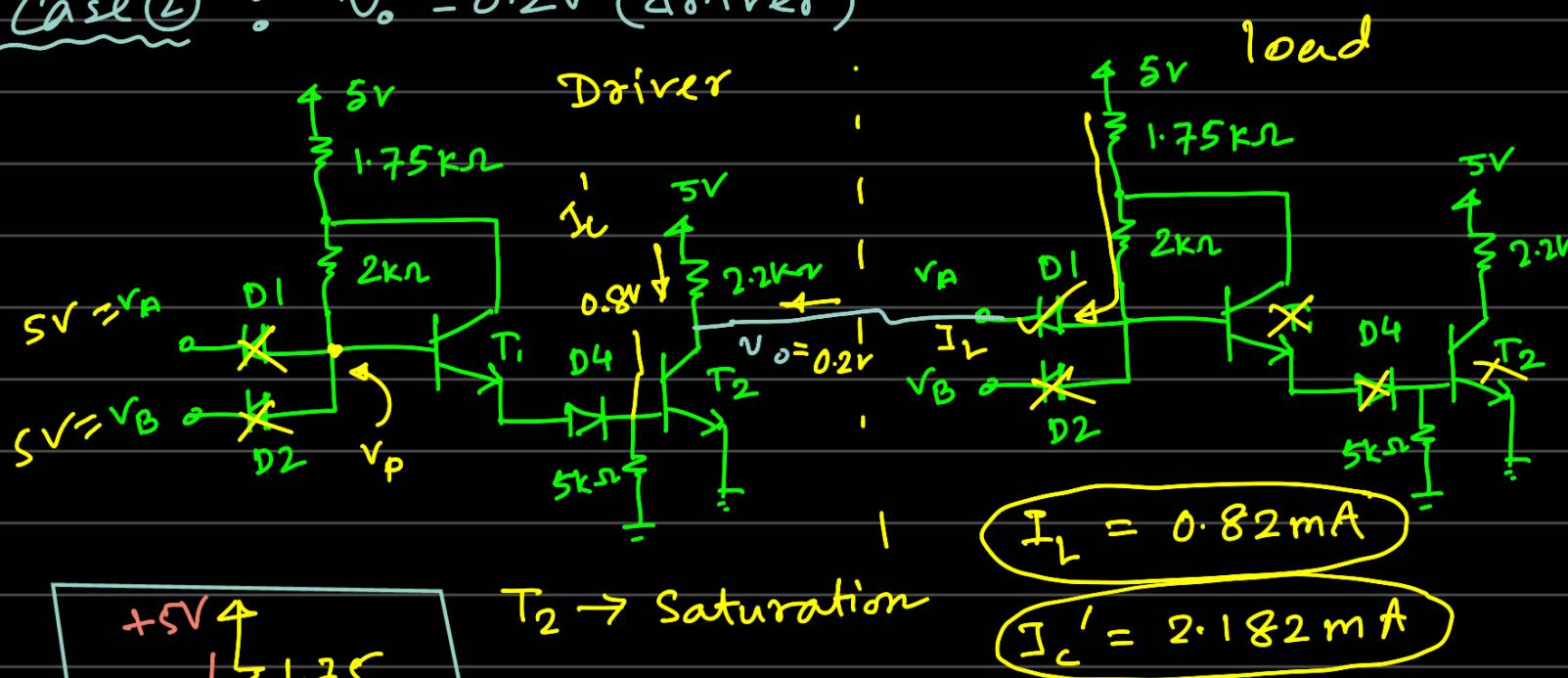
## Modified DTL circuit. :-



# This circuit will have higher maximum fanout.

Case ①: Trivial.  $V_o = 5V$  (driver circuit). Fanout = 2.

Case 2 :  $V_o = 0.2V$  (driver)



# Current will flow from higher voltage to lower voltage.

Therefore,  $V_{el} > V_{Bi}$

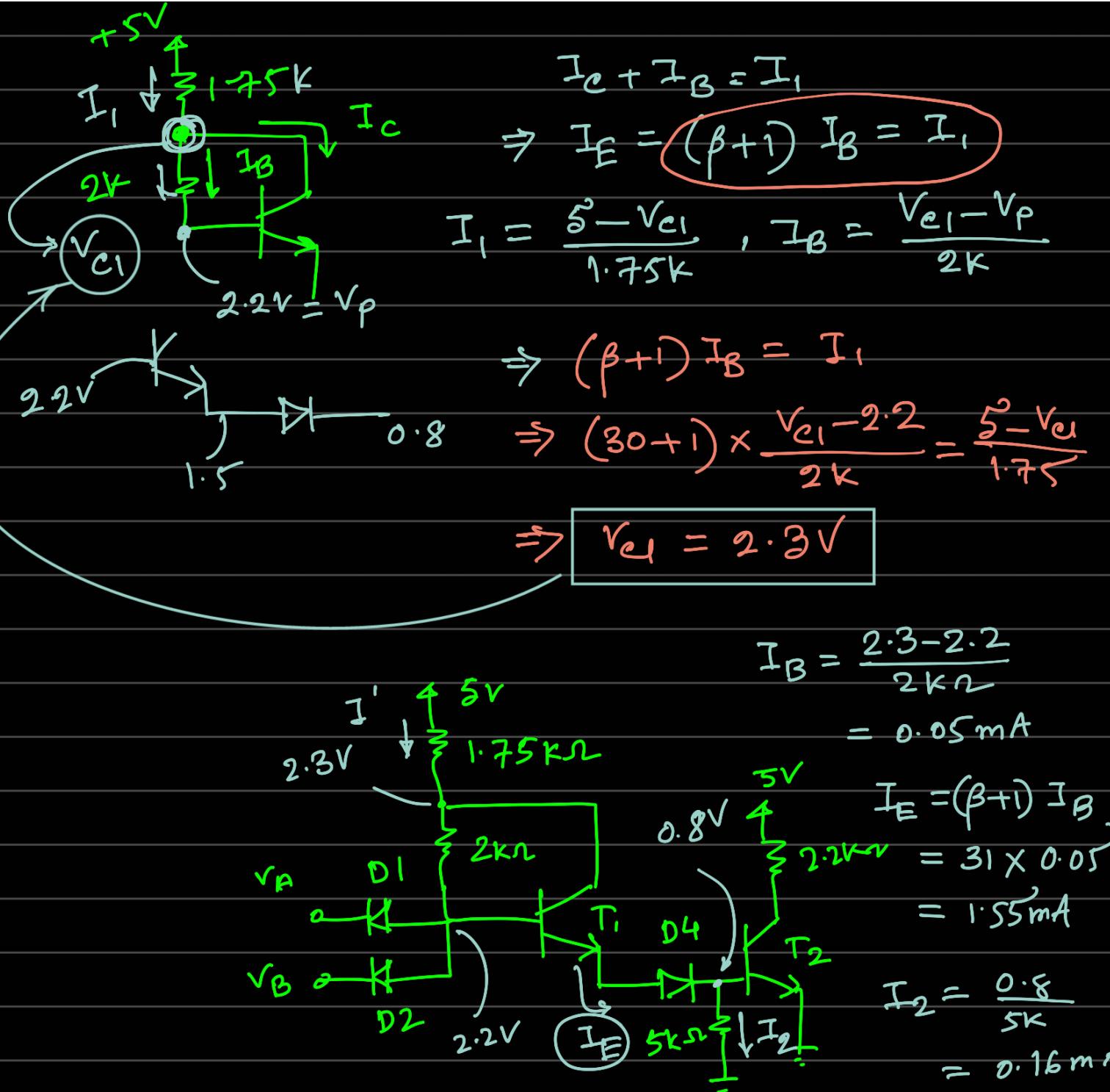
$$\Rightarrow V_{B1} - V_{C1} < 0$$

$$\Rightarrow V_{BC_1} < 0$$

$T_i \rightarrow ON \Rightarrow V_{BEi} > 0.5V$   
 So  $T_i$  must be in forward active.

$$V_{BE} = 0.7V$$

(for forward active)



$$I_B = I_E - I_2 = 1.39mA$$

↗ fomout  
no load  
collector current

$$I_{c,max} = \beta_F \times I_B = \underbrace{I_{c'}}_{\substack{\text{standard} \\ \text{load}}} + N \times \underbrace{I_L}_{\substack{\text{standard} \\ \text{load}}}$$

$$1.39 \times 30 = 2.182 + N \times 0.82$$

$$\lfloor N \rfloor = \lfloor 35. \dots \rfloor$$

Maximum fomout = 35.

