

Review of CSE 251 : Electronic Circuits & devices

electronics: method or process used to control the flow of electrons using external electric field.

examples : spintronics , photonics ...

\downarrow \downarrow
control control optical wave
spin by by E field
 E field

→ Material classification in three categories: depending on conductivity

1. Metal	$10^{-13} \Omega m$
2. Insulators	$10^1 - 10^{-4} \Omega m$
3. Semiconductors	$10^{-10} \Omega m$

Concept of bands: → collection of discrete energy levels \nearrow conduction band \searrow valence band

- Electronic Band gap theorem

valence band: energy band formed by a series of energy levels containing valence electrons .

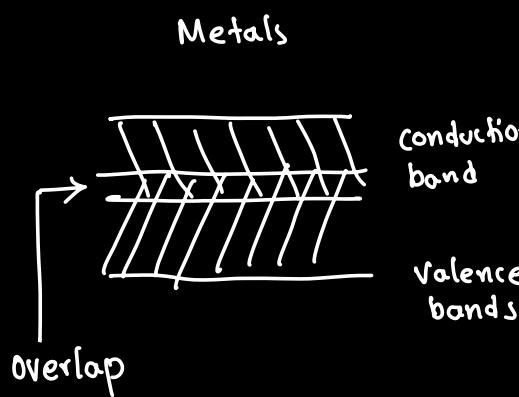
Low energy state , below fermi level

conduction band: when energized e^- may move from valence to conduction band.

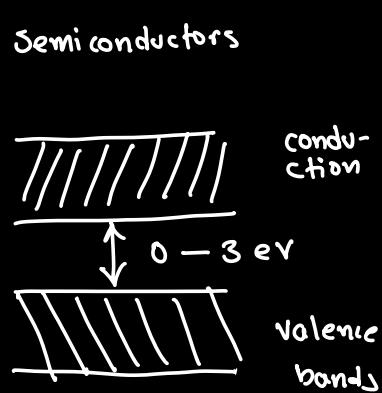
- Band of e^- orbitals that e^- bounce up into from valence band
- collection of energy bands above the fermi level
- e^- in conduction band are free to move
- current flow due to these e^- in conduction band

Fermi level: highest energy level which can be occupied by an e^- at 0K

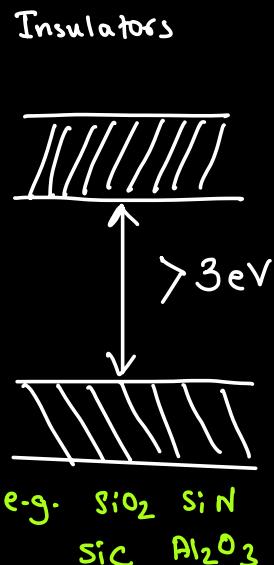
Energy levels in the 3 categories:



e.g.
Al, Ag, Cu, Na, Mg



e.g.
Si, Ge, GaAs, GaN



e.g. SiO_2 Si_3N_4
 SiC Al_2O_3

Silicon most widely used semi-conductor material in electronic devices

→ Semiconductors

1. Intrinsic semiconductor : Pure semiconductor material
(limited use → e.g. PIN diodes in LED)

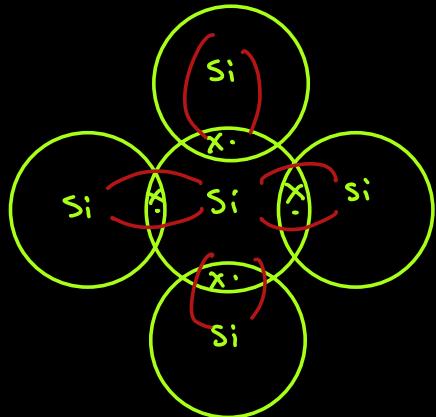
2. Extrinsic semiconductor : Impurity introduced here
(possibilities & applications → boundless!)

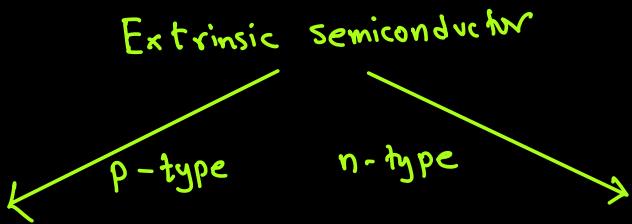
Visualizations

Si electron configuration : $1s^2 2s^2 2p^4$ 3s² 3p²

valence e^-

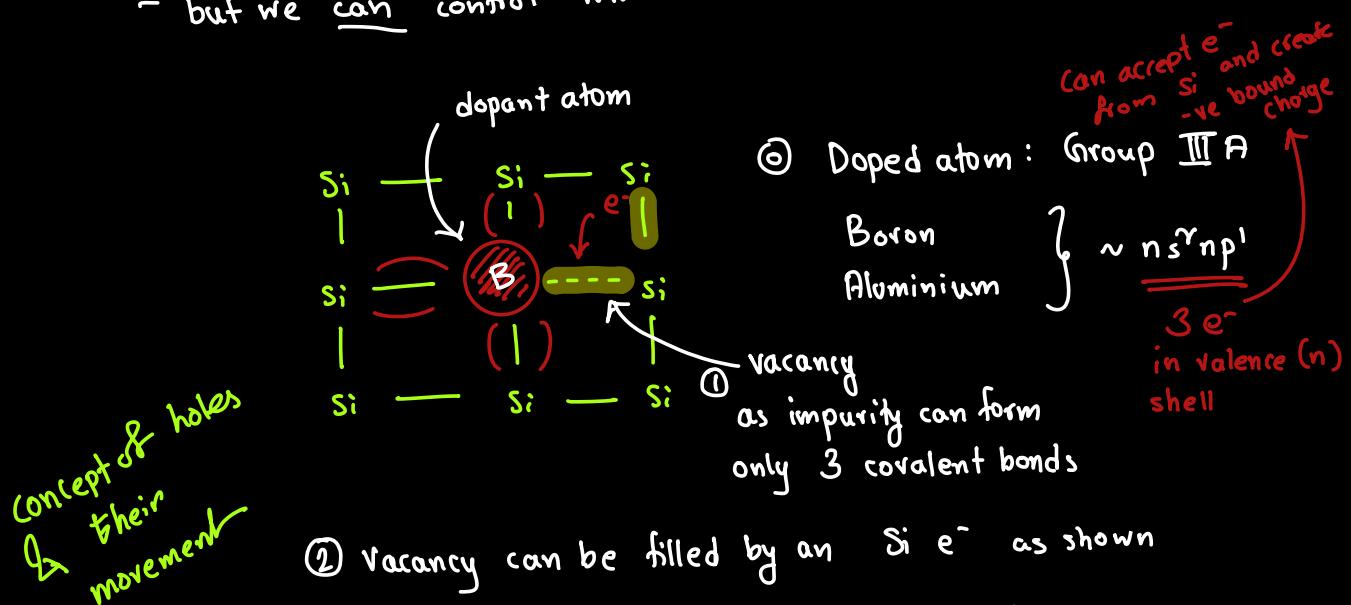
pure crystal → intrinsic semiconductor





① P type semiconductor

- we cannot control where we place the impurity atoms
- but we can control where we can place them



② Vacancy can be filled by an $Si e^-$ as shown

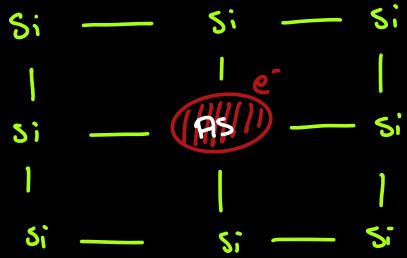
③ Vacancy \rightarrow absence of $e^- \rightarrow$ holes

④ movement of vacancies \rightarrow movement of holes

⑤ Majority charge carrier : hole

⑥ Boron can accept an e^- & form -ve bound charge

② N-type semiconductor

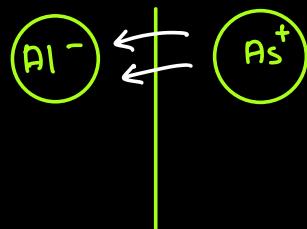
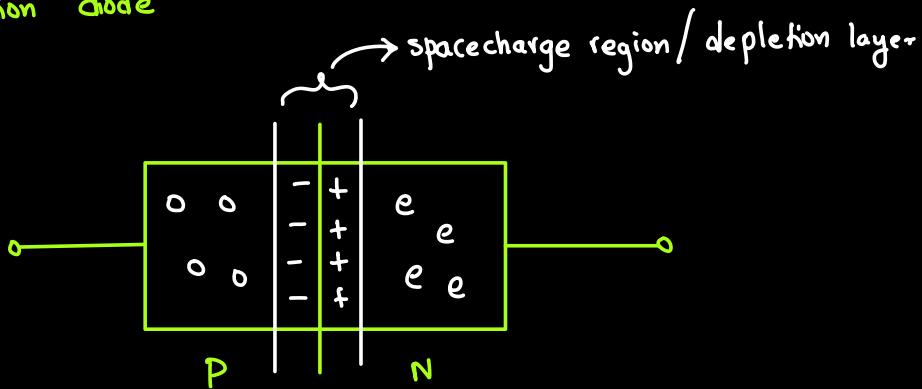


⑥ Dopant atom: Group VA
P, Sb, As $ns^2 np^3$

① Majority charge carrier is
 e^-

② As can just release an e^-
and form five bound charge

→ p-n junction diode



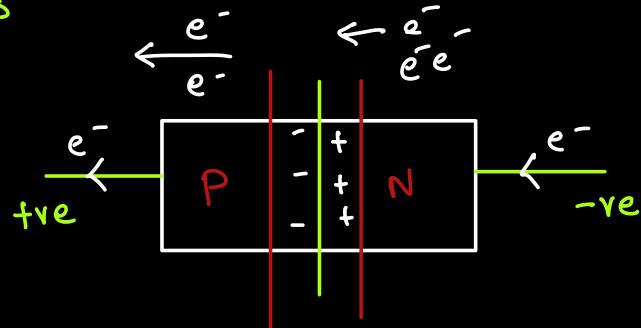
diffusion process

junction is fundamental to electronics
electronics would not be possible without it

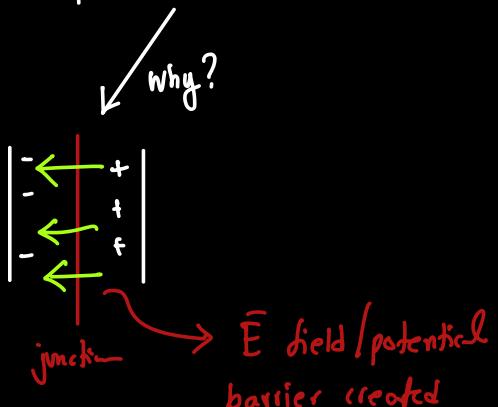
Two modes



Forward Bias



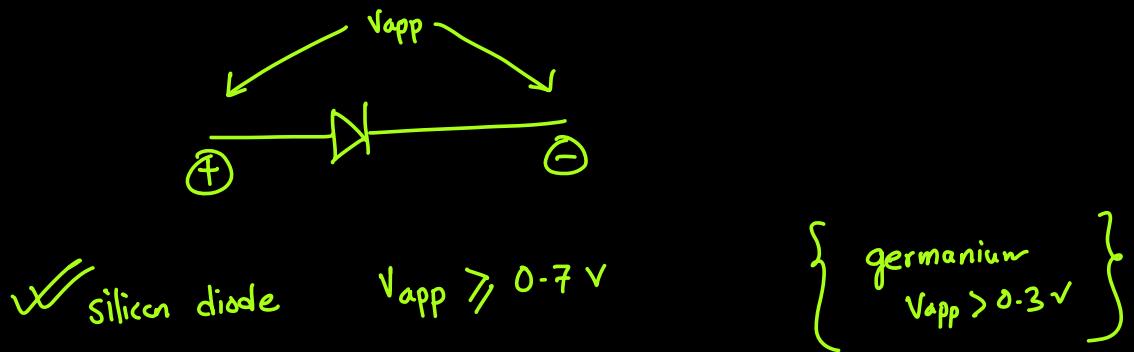
- ① high enough voltage applied
- ② e^- will move from N \rightarrow P side and out
- ③ voltage not high enough
- ④ e^- will not be able to cross depletion region
- ⑤ in space charge region



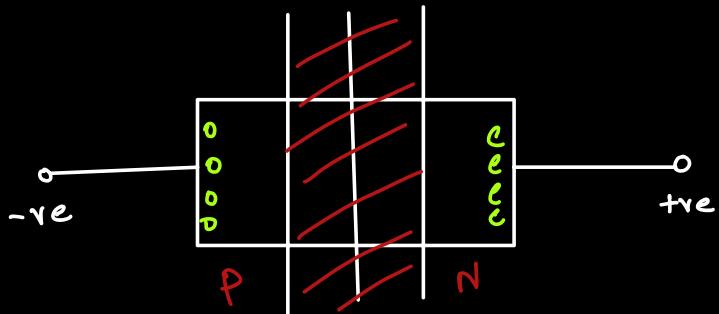
If field direction is \leftarrow , e^- pushed in \rightarrow direction

considering cases ①, ②,

⑥ e^- move N \rightarrow P, holes P \rightarrow N against barrier



Reverse bias

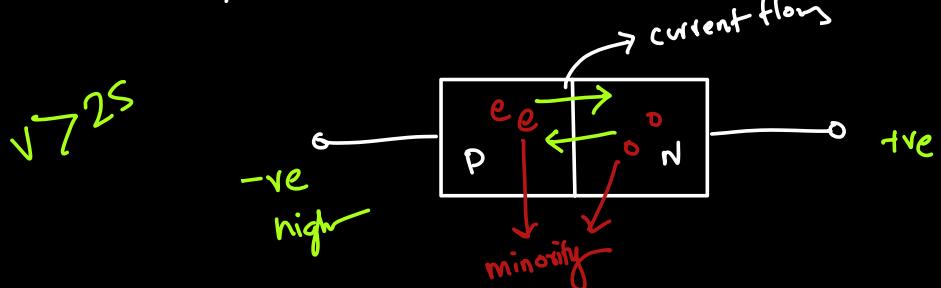


- ① increase in width of depletion region
- ② more diffusion needed to balance out and so more space charge formed ③ → not imp. for this course



→ # Breakdown

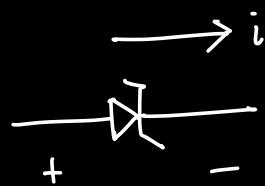
if reverse bias voltage is high \rightarrow diode may conduct



- ① Voltage (rev.) high enough to cause minority carriers to move to the other junction.

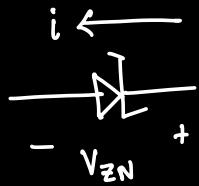
Zener diode

Breakdown mode is utilized in application



Forward conduction

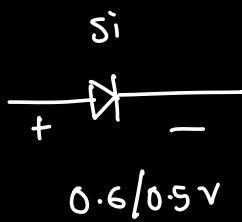
0.7V



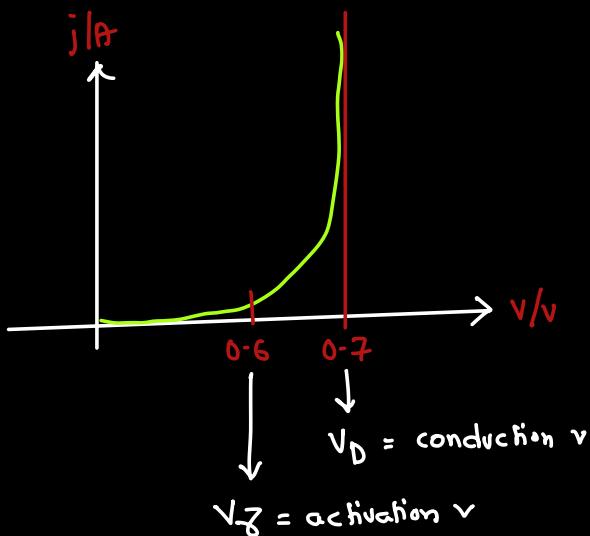
Zener Voltage

V_{reverse} > V_{ZN} → conduction

Activation voltage / Turn on voltage



0.6/0.5V



Conduction Voltage Drop model:

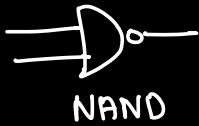
$$\textcircled{1} \quad \xrightarrow{\text{Zener Diode}} = \xrightarrow{\text{Voltage Drop} V_D = 0.7V}$$

$$\textcircled{2} \quad \xrightarrow{\text{Zener Diode}} = \xrightarrow{\text{Current i}}$$

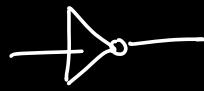
* In Question → see if activation voltage mentioned
if not → ignore use conduction voltage

Review of 251 ends (for diodes)

Introduction to Digital logic families



NAND



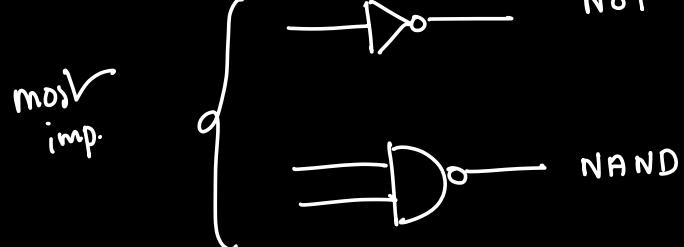
NOT



NOR

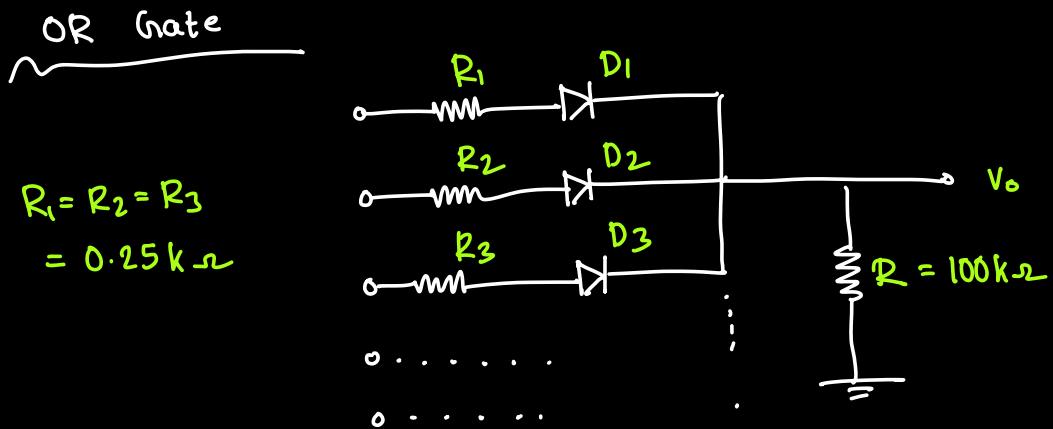
These gates are abstract → represent logical operations

Digital logic families distinguishes different ways of constructing logic



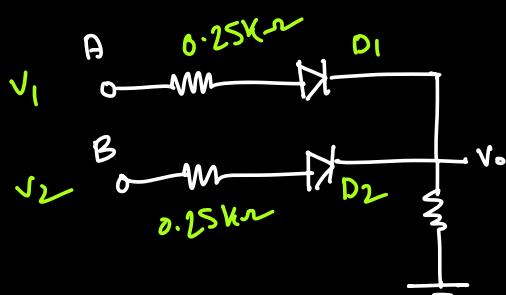
We can use diff electronic devices to construct logic gates

Diode logic (also in first lab 350)



"Beware of shorts" - Shahnewaz Bhai 2022

→ Consider constant voltage drop model



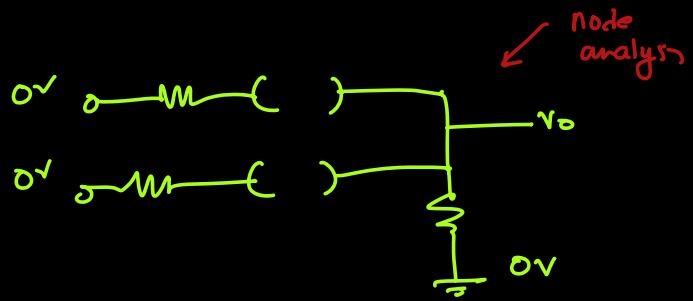
logic 1 → 5V
logic 0 → 0V

Case	A	B	v_1	v_L	v_o	C
i	0	0	0	0	0	0
ii	0	1	0	5	4.289	1
iii	1	0	5	0	4.289	1
iv	1	1	5	5	4.294	1

FACT: each diode needs atleast 0.6V to turn on

case I

D₁, D₂ off



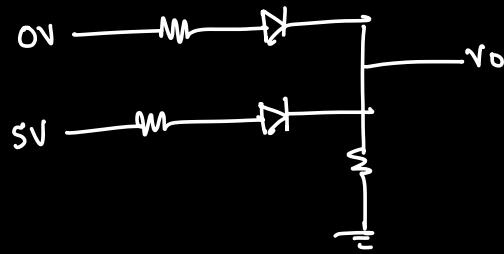
$$\frac{v_o - 0}{R} + \frac{v_o - 0}{R} + \frac{v_o - 0}{R} = 0$$

$$\frac{3v_o}{R} = 0$$

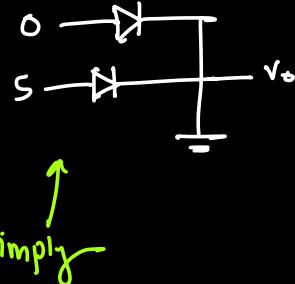
$$v_o = 0$$

no current

II

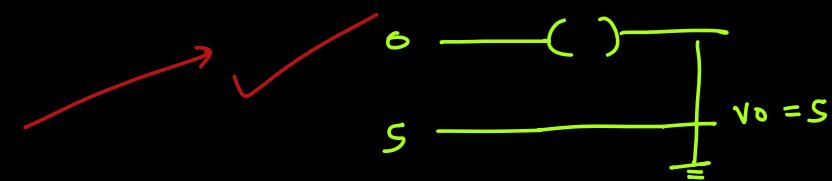


Simple model
≈

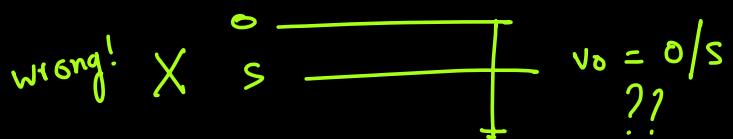


Step ①

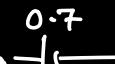
— simple analysis

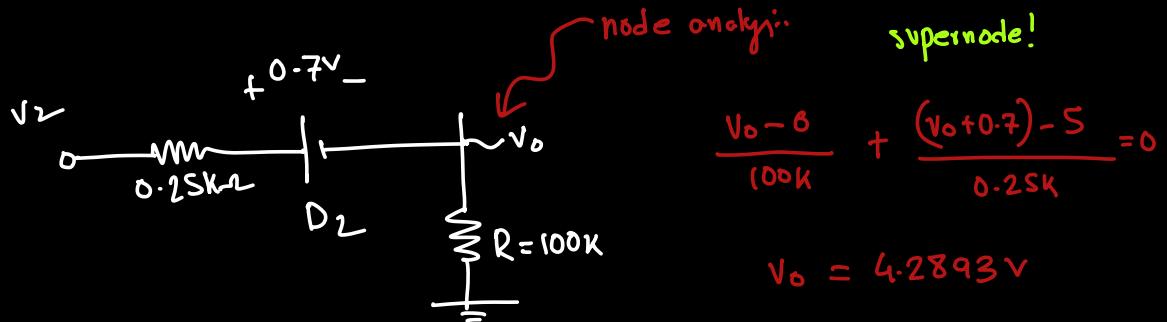


if



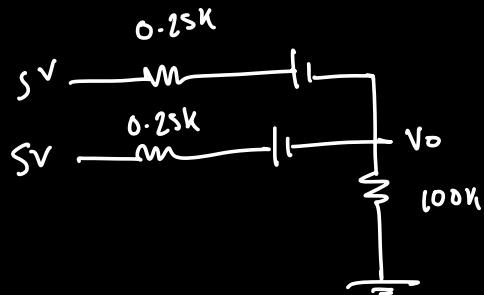
Step ②

- analysis \rightarrow constant V-drop model \rightarrow replace on D \rightarrow  off D \rightarrow 



case III same as II

case IV

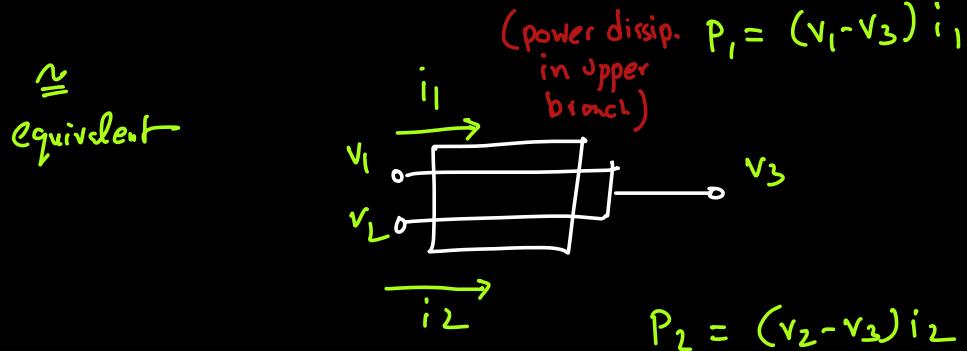
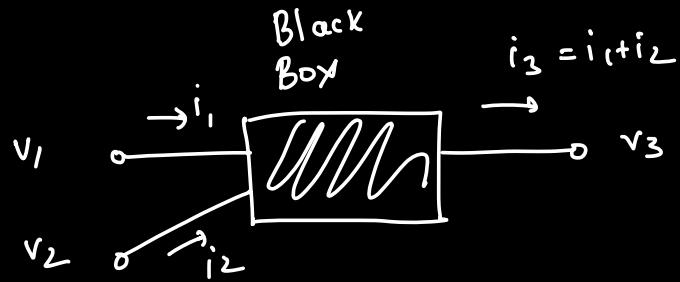


$$\frac{V_o + 0.7 - 5}{0.25k} + \frac{V_o + 0.7 - 5}{0.25k} + \frac{V_o - 0}{100k} = 0$$

choose smallest V_o value \rightarrow logical high (4.28 V)
 \therefore if $V > 4.28 \therefore$ Logical high otherwise Low

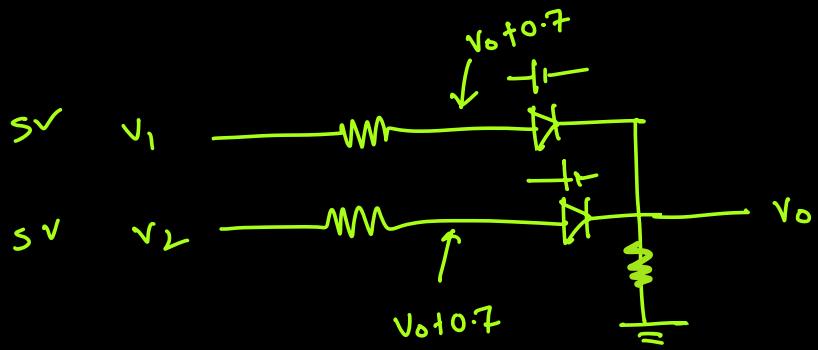
Power dissipation calculation

Theory



$$P = P_1 + P_2 \quad (\text{total Power dissipation})$$

among our 4 cases in previous example, which one
will cause P_{\max} dissipation.

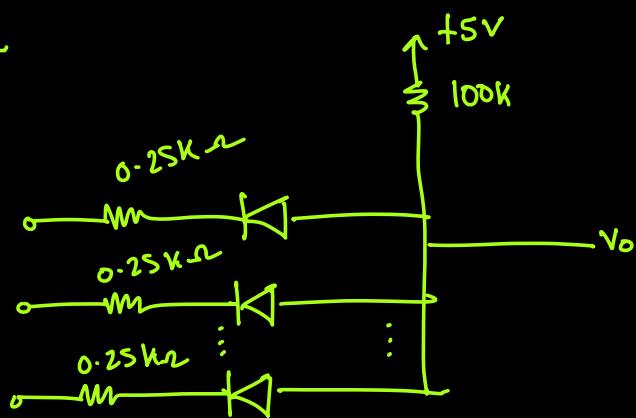


$$i_1 = \frac{5 - (4.2946 + 0.7)}{0.25 k}$$

$$i_2 = i_1$$

$$\left. \begin{array}{l} P_1 = (5 - 6) \times i_1 \\ P_2 = (5 - 6) \times i_2 \end{array} \right\} \quad p = P_1 + P_2$$

AND GATE



Do case analysis!

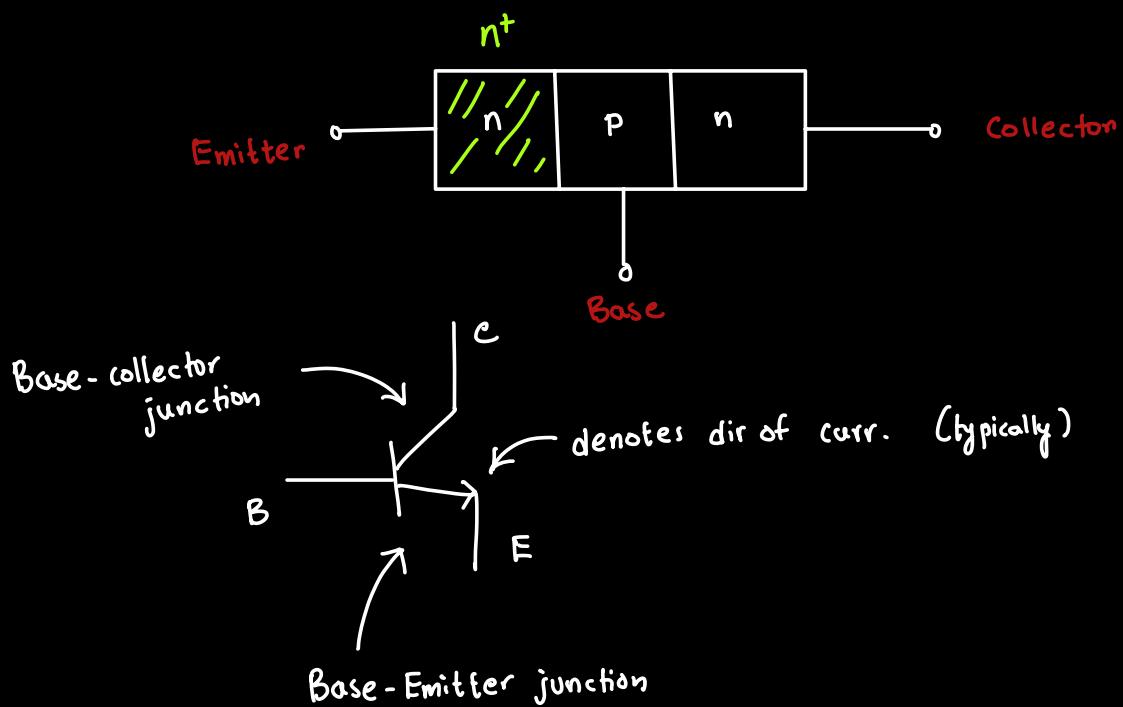
Set logic low voltage here \rightarrow set highest as logic low. $\therefore V_o < V_{low(highest)}$ \rightarrow logic low

Transistor

Lecture 3

- Will be used as a switch
- NOT as an amplifier

only n-p-n in this course

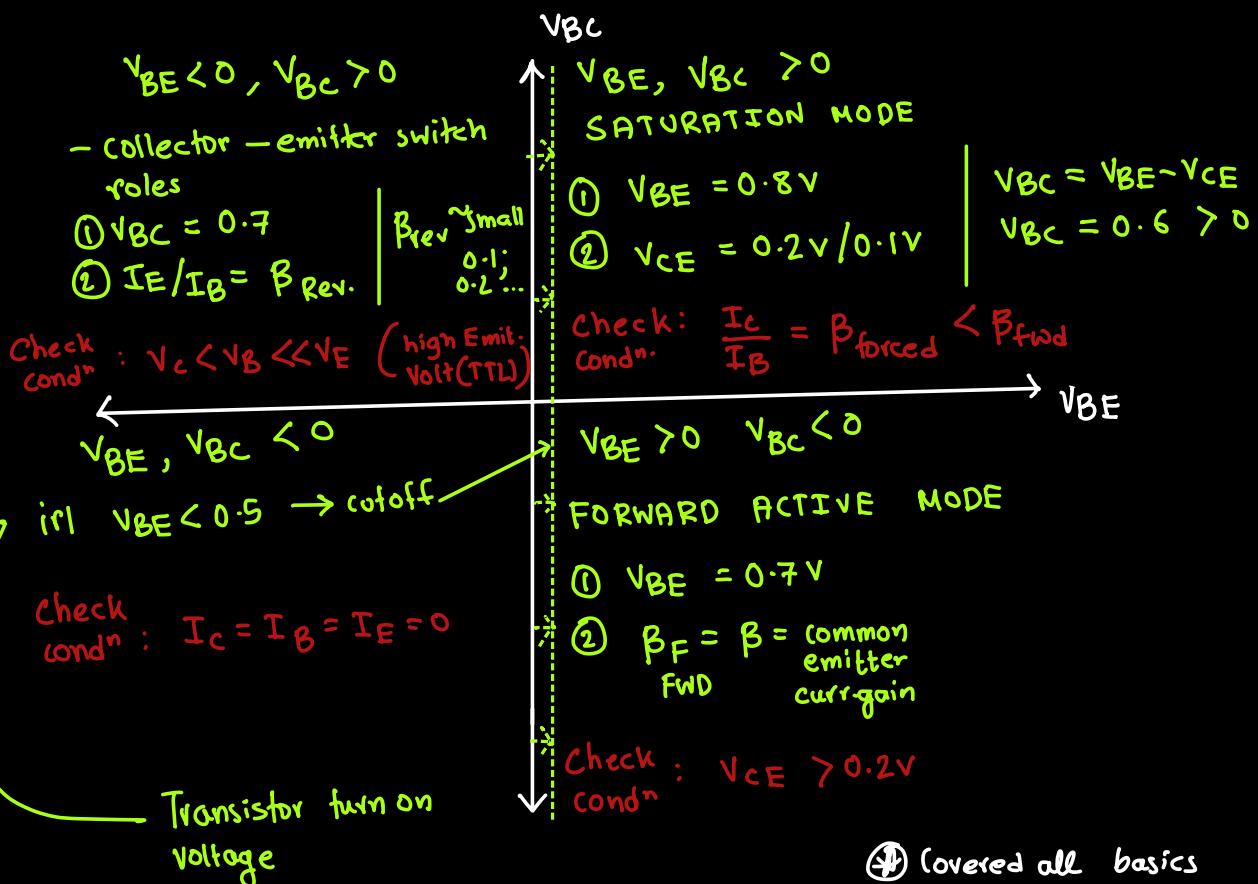


3-terminal device → e, h both used to carry current
∴ Bipolar device

Bipolar Junction Transistor (BJT)

4 modes of operation acc. to V_{BE} & V_{BC}

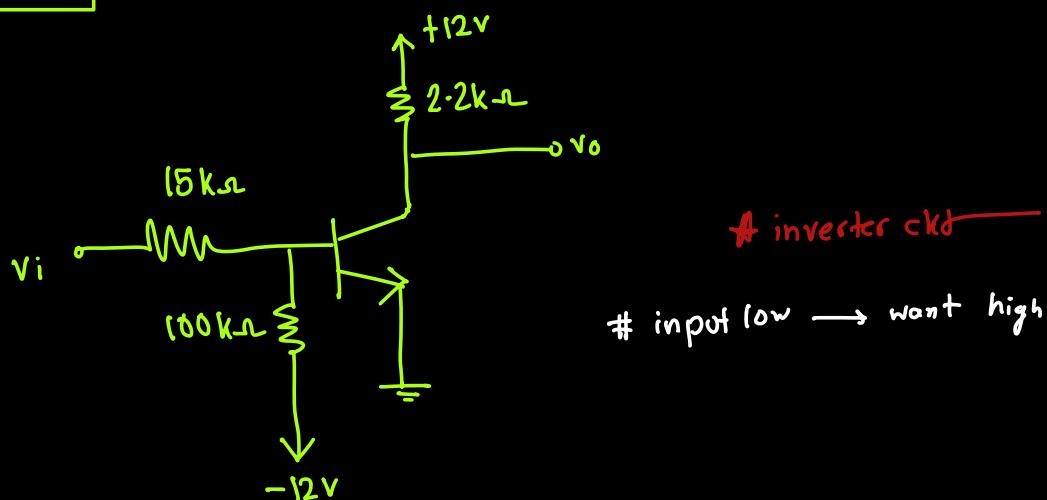
BE junction	BE junction	Mode
R	F	Forward active
F	F	Saturation
R	R	Cutoff
F	R	Reverse active



Register Transistor Logic (RTL)

{ saturated logic family:
logic transistors connected
to the output terminal }

NOT GATE



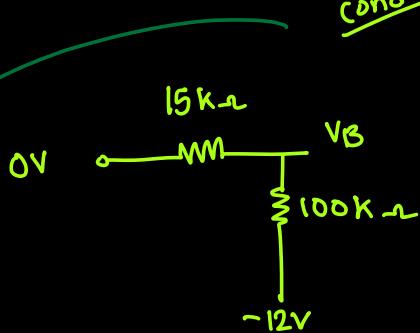
input low → want high

case (I)

$$\overline{Vi} = 0$$

assume cutoff

cond'n ① $V_{BE} < 0.5\text{ V}$



cond'n ② $I_C = I_B = I_E = 0$

$$\frac{V_B - 0}{15k} + \frac{V_B - -12}{100k} = 0$$

$$V_B = -1.565\text{ V}, V_B = 0$$

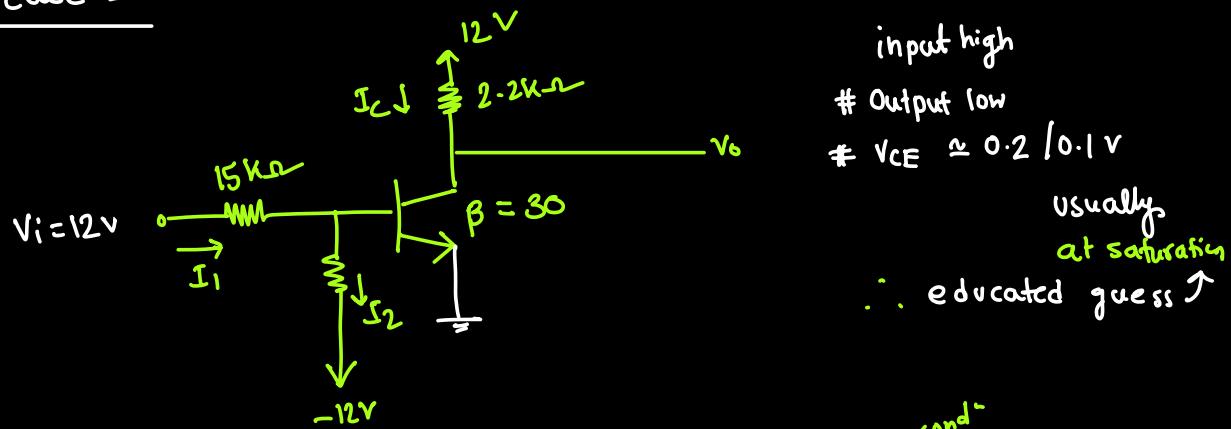
check $V_{BE} = -1.565\text{ V}$ ✓
 $< 0.5\text{ V}$

For cutoff : $I_B = I_C = I_E = 0$

$$I_C = 0 = \frac{12 - V_C}{2.2k}$$

$$V_C = 12 = V_O \text{ high //}$$

Case 2



sat:

$$\textcircled{1} \quad v_{BE} = 0.8 \text{ V}$$

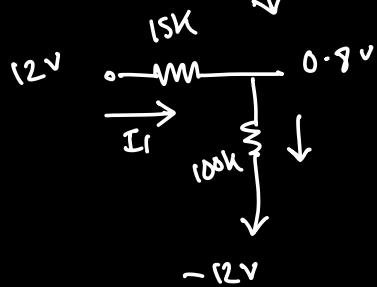
$$\textcircled{2} \quad v_{CE} = 0.2 \text{ V}$$

$$I_C = \frac{12 - v_C}{2.2 \text{ k}}$$

$$I_C = 5.3 \text{ mA}$$

(cond)
2
 $v_{CE} = v_C = 0.2$

$$\textcircled{1} \quad v_{BE} = 0.8 \text{ V}$$



$$I_1 = \frac{12 - 0.8}{15 \text{ k}} = 0.746 \text{ mA}$$

$$I_2 = \frac{0.8 - (-12)}{100 \text{ k}} = 0.128 \text{ mA}$$

case check

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = 8.659 < \beta_{\text{FWD}}$$

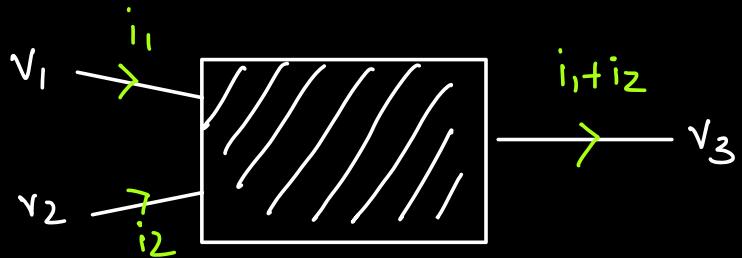
assumption ✓

$$I_B + I_2 - I_1 = 0$$

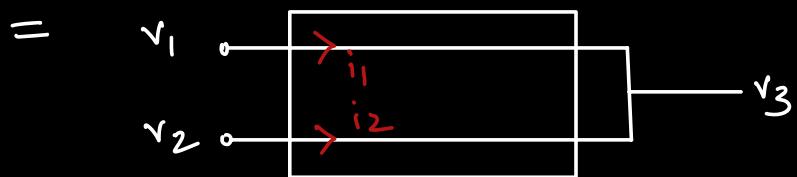
$$I_B = I_1 - I_2 = 0.619 \text{ mA}$$

Power dissipation

Lecture 4



$$P_1 = (v_1 - v_3) i_1$$



$$P_2 = (v_2 - v_3) i_2$$

$$P_{\text{dissipation}} = P_1 + P_2 = (v_1 - v_3) i_1 + (v_2 - v_3) i_2$$

maximum power dissipation \rightarrow ① Look at the cases of the gates

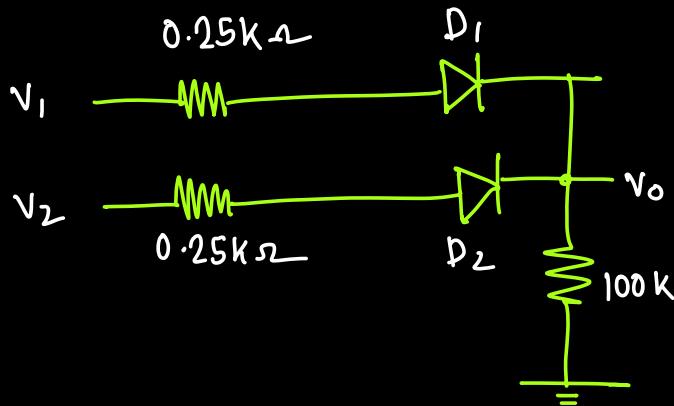
- ④ If in doubt, find the power dissipation (for cases in doubt)

P_{\max} = "jeta boro habe of the cases"

- ② Notice where max current flows

- ③ Calc. power for that case

from prev. ckt



for Diode Logic Ckt

Remember the case ...

(I) $V_1 \quad V_2 \quad D_1 \quad D_2$
0 0 off off

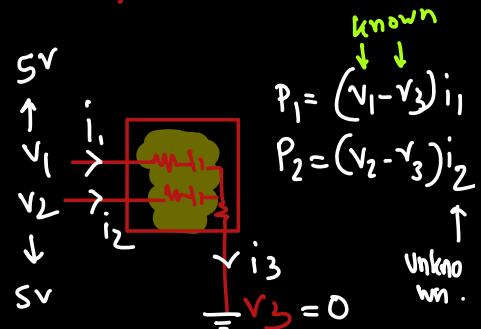
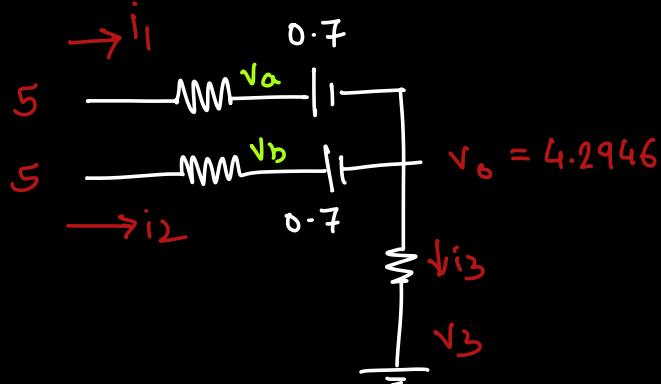
(II) $V_1 \quad V_2 \quad D_1 \quad D_2$
0 5 off on

(III) $V_1 \quad V_2 \quad D_1 \quad D_2$
5 0 on off

(IV) $V_1 \quad V_2 \quad D_1 \quad D_2$
5 5 on on

most current for this case

$\therefore P_{\max}$ pow dissipation!



To find maximum power dissipation \rightarrow find currents i_1, i_2, i_3 .

$$V_a - V_3 = 0.7 \quad \text{--- (1)}$$

$$\therefore V_a = 0.7 + 4.2946$$

$$V_a = 4.9946 \text{ V}$$

} similarly

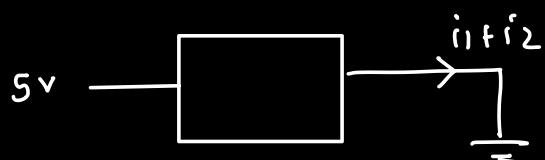
$$V_b = 4.9946 \text{ V}$$

$$v_1 \downarrow \quad v_3 \downarrow$$

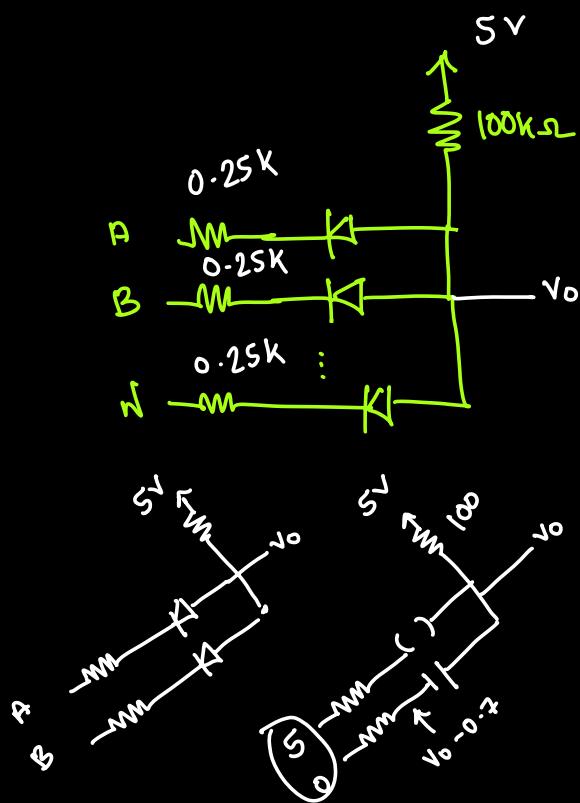
$$P_1 = (5 - 0) \times i_1$$

$$P_2 = (5 - 0) \times i_2$$

$$P_{\text{tot}}^{\text{(max)}} = P_1 + P_2 = 0.215 \text{ mA}$$



Do this for and gate too!

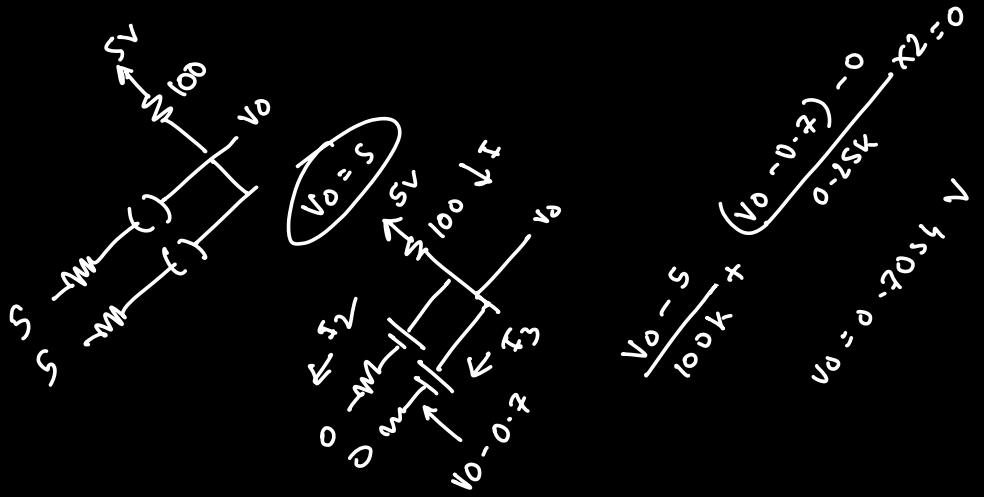


PRACTICE!

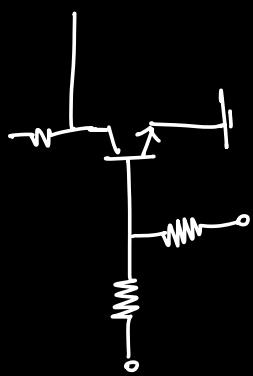
$N = 2, 3$

$$\frac{V_o - 5}{100k} + \frac{V_o - 0.7}{0.25k} = 0$$

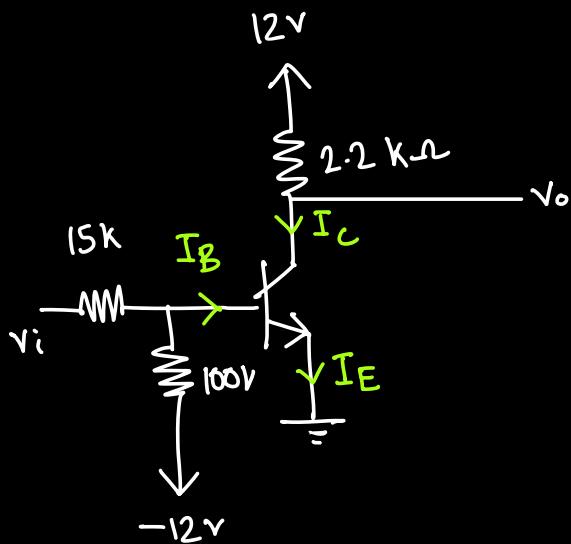
$$V_o = 0.710V$$



$$\begin{aligned}
 & \text{Power during max} \\
 & P_{\text{out}} = \frac{I^2 \cdot 0.7054}{100k} \\
 & = \\
 & P_1 = \frac{(S - 0) I_2}{100k} \\
 & + P_2 = \frac{(S - 0) I_3}{100k} \\
 & P_1 + P_2 = P_{\text{max}}
 \end{aligned}$$



For RTL inverters



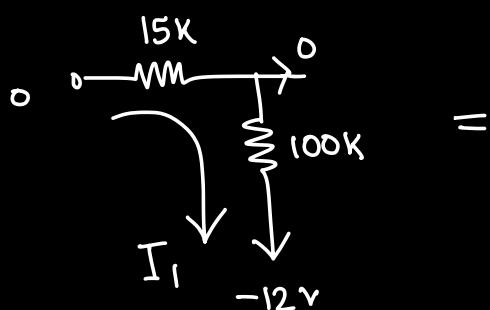
Same method

figure cases

Case ① $V_i = 0$ cutoff

$$I_B = I_C = I_E = 0$$

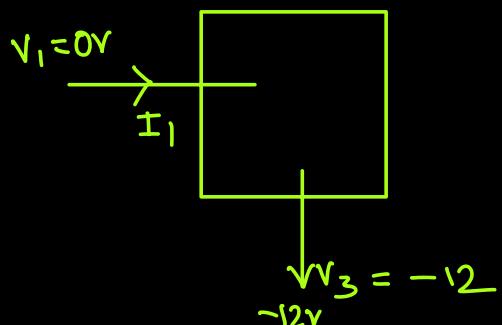
only current flow in ckt



$$\frac{0 - -12}{(15 + 100)k} = I_1$$

$$I_1 = 0.104 \text{ mA}$$

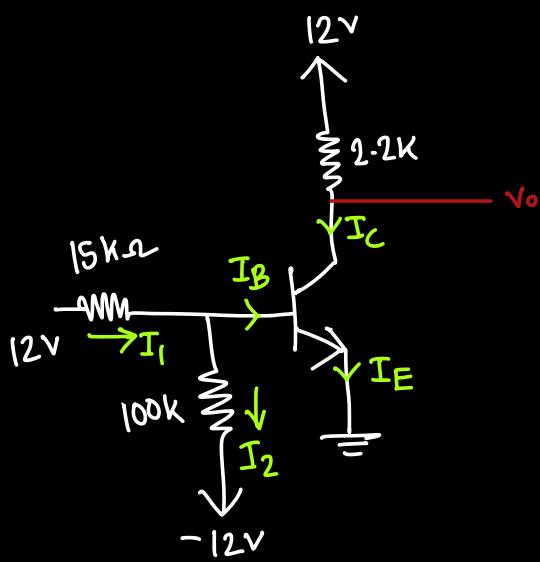
power dissip.



$$P_1 = (0 - -12) \times I_1$$

$$P_1 = 1.2521 \text{ mW}$$

Case 11



Saturation mode:

$$\textcircled{1} \quad V_{BE} = 0.8V$$

$$\textcircled{2} \quad V_{CE} = 0.2V$$

$$V_E = 0 \quad \text{in ckt}$$

$$\therefore V_C = 0.2$$

$$\therefore V_B = 0.8$$

$$\frac{12 - V_C}{2.2k} = I_C = \frac{12 - 0.2}{2.2k}$$

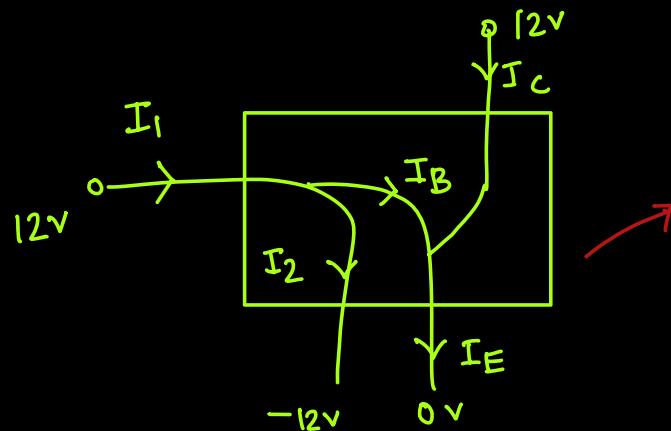
$$= 5.364 \text{ mA}$$

$$I_1 = \frac{12 - 0.8}{15k} = 0.7466 \text{ mA}$$

$$I_2 = \frac{0.8 - -12}{100k} = 0.128 \text{ mA}$$

$$I_B = I_1 - I_2 = 0.6186 \text{ mA}$$

Power dissip.



$I_B, I_2 \rightarrow$ create two outputs

I_1 does not flow through two lines
but divides into I_2 & I_B .

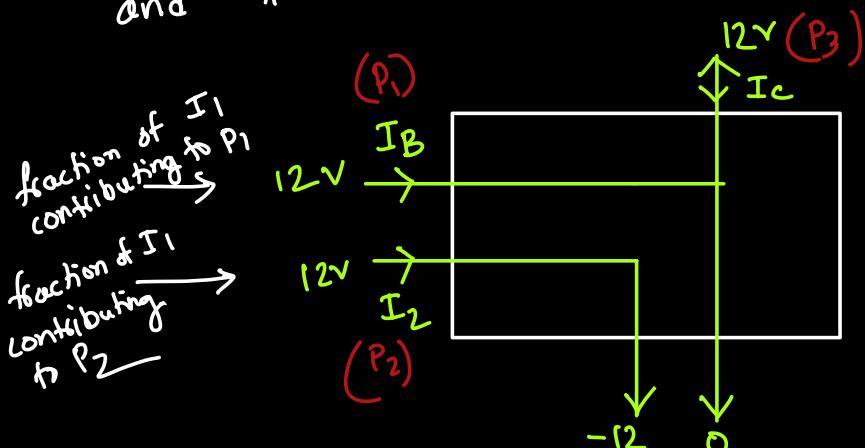
if we write

$$P_1 = I_1 (12V - (-12))$$

$$P_2 = I_1 (12V - 0)$$

wrong! I_1 cannot be considered in two power values. P_1 & P_2 here are not indep. pow. values.
(as if I_1 flows through both lines. wrong)

→ separate $I_1 \rightarrow I_2$ & I_B ($I_1 = I_2 + I_B$) → know that I_1 actually divides into 2 terminals



$$P_1 = (12 - (-12)) \times 0.128 \text{ mW}$$

$$= 3.072 \text{ mW}$$

$$P_2 = (12 - 0) \times 0.6186$$

$$= 7.4323 \text{ mW}$$

$$P_3 = (12 - 0) \times 5.3636$$

$$= 64.3632 \text{ mW}$$

$$P_{\text{tot.}} = P_1 + P_2 + P_3 = 74.8584 \text{ mW}$$

(max!)