**BRAC UNIVERSITY**

**Department of Computer Science & Engineering**

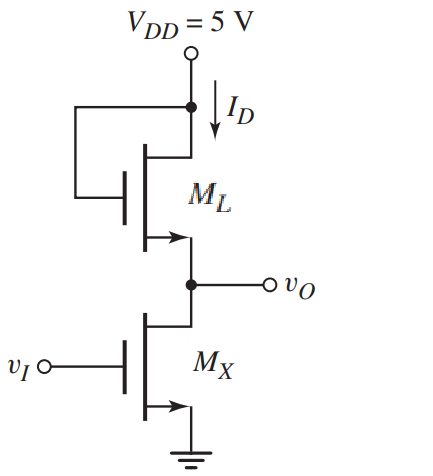
**Practice Problem sheet (Week8)**

**CSE 350: Digital Electronics and Pulse Technique** 

# Question 1

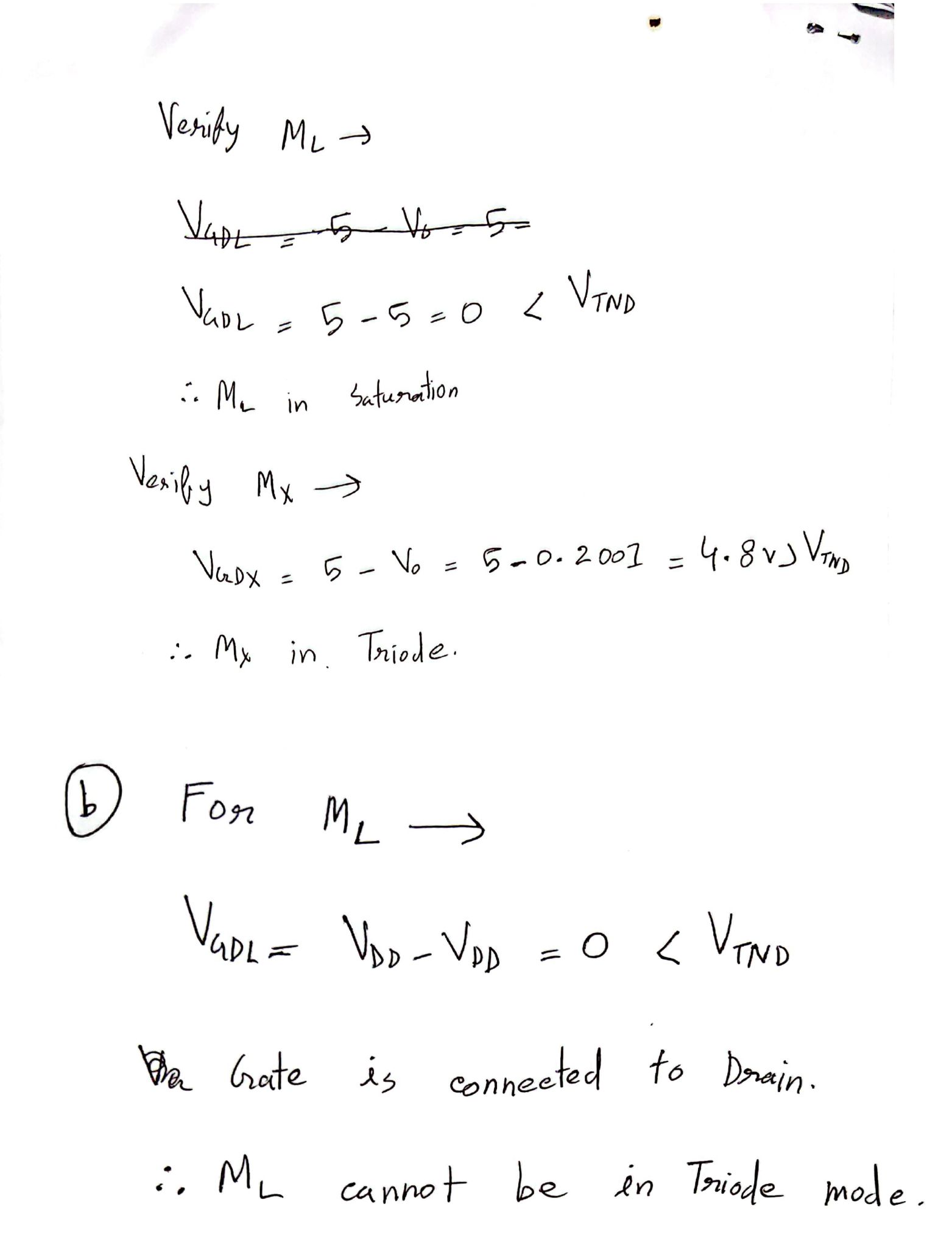
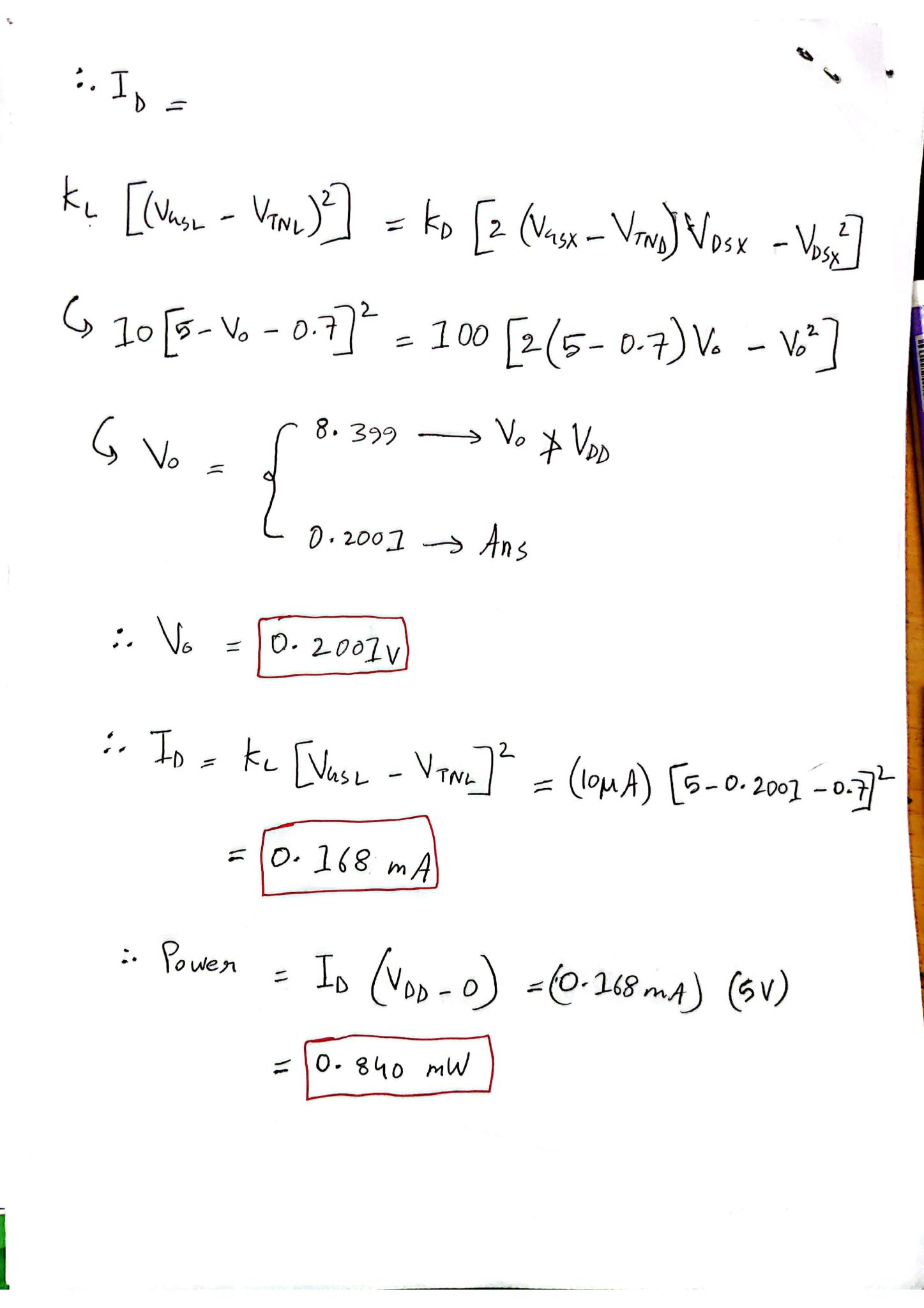
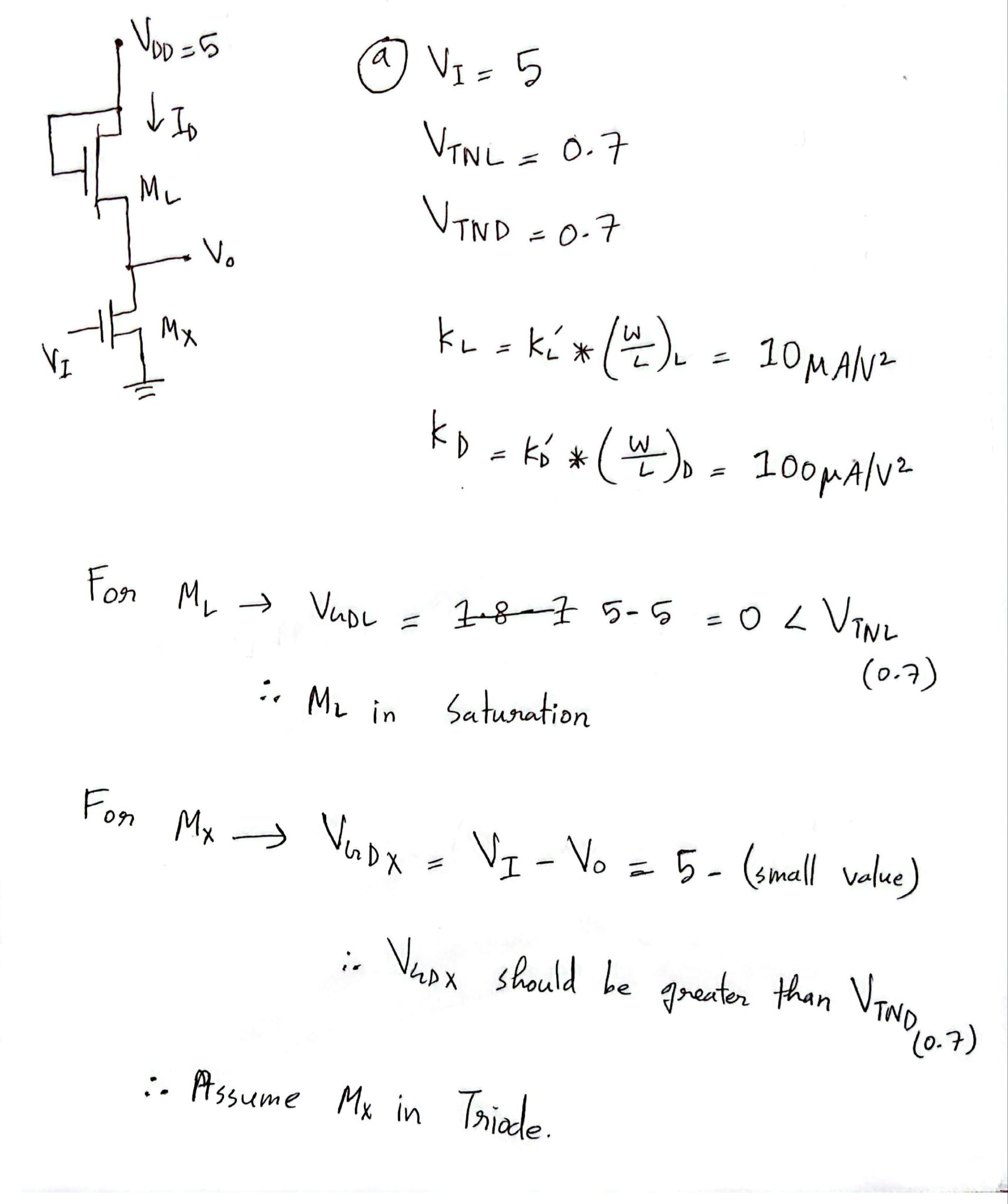
For the circuit below (enhancement Load Inverter), assume these parameters,

MOSFET process parameter for ML is **K’L= 5 μA/V2**, **(W/L)L = 2** and threshold voltage, **VTNL = 0.7V**. MOSFET process parameter for MX is **K’D= 25 μA/V2**, **(W/L)D = 4** and threshold voltage, **VTND = 0.7V**.



| (a) | Assume **VI = 5 V**. Find value of **Vo** in volt. Find **ID** and Power Dissipation. Verify the operating mode of **ML** and **MX**. |
| --- | --- |
| (b) | What should be the value of **VI**  if we want **ML** to operate in the triode region? |

## Solution:

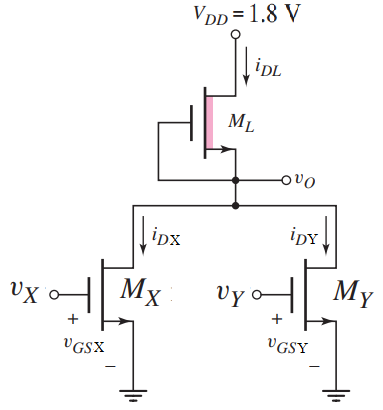


# Question 2

For the circuit below (Depletion Load NOR), assume these parameters,

MOSFET process parameter for ML is **K’L= 50 μA/V2**, **(W/L)L = 2** and threshold voltage, **VTNL = −0.6V**. MOSFET process parameter for both MX and MY is **K’D= 33.25 μA/V2**, **(W/L)D = 4** and threshold voltage, **VTND = 0.4V**.

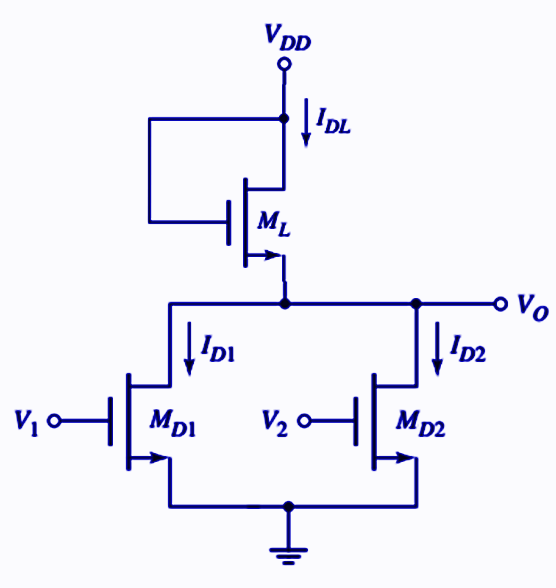
| (a) | Assume **VX = VY = 1.8 V**. Find value of **Vo** in volt. Find **IDX, IDY, IDL** and Power Dissipation. Verify the operating mode of **ML**. |
| --- | --- |
| (b) | Now, assume **VX = VY = 0.1 V**. Find value of **Vo**, **IDX, IDY, IDL.** |
| (c) | What should be the operating mode of **MX** and **MY** if **VX = 1.8V and VY = 0 V**? (Use logical reasoning, no need for calculation) |



# 

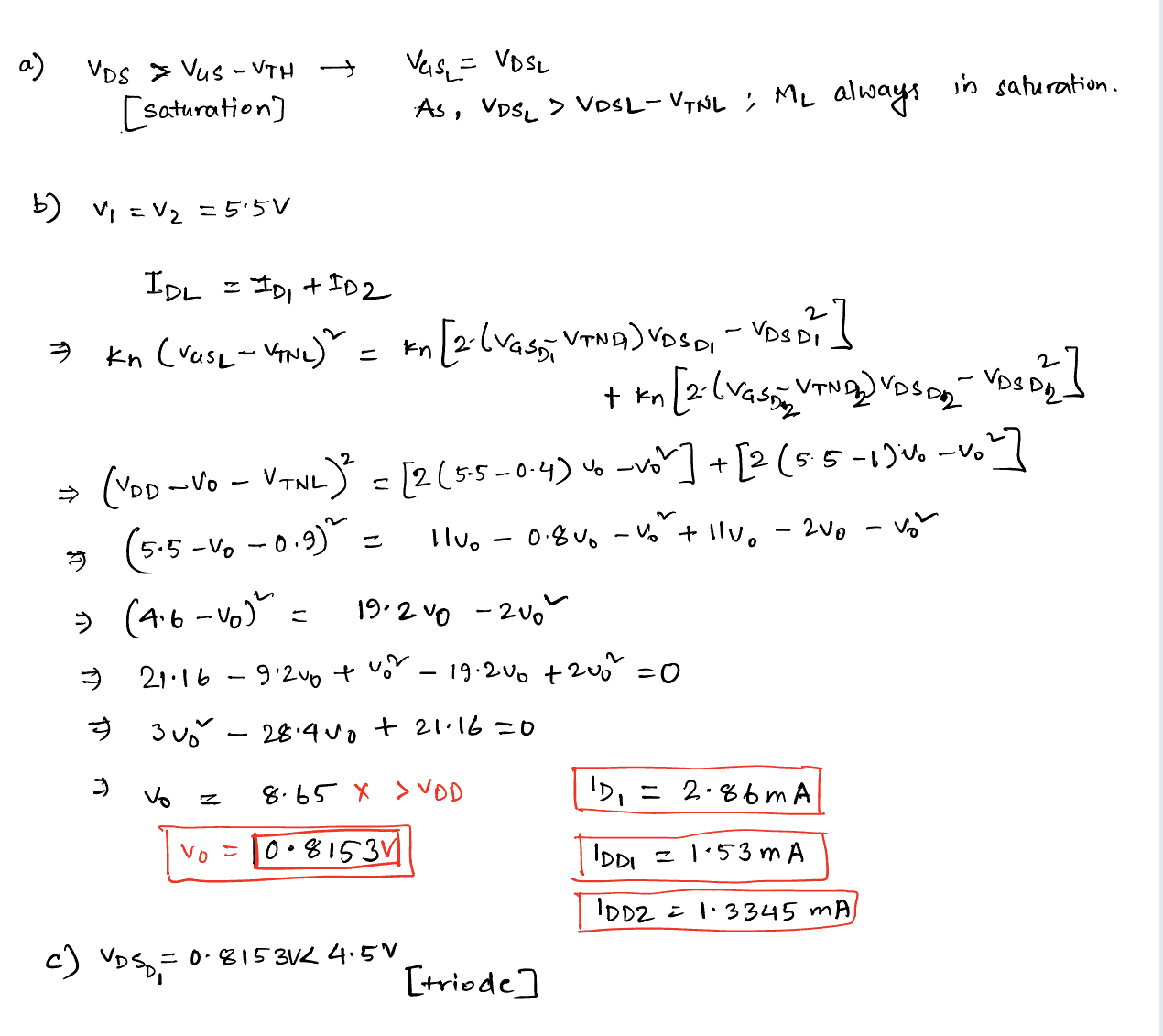
# Question 3

**The enhancement-load NMOS NOR gate in the figure is biased at VDD = 5.5 V. The transistor parameters are Kn = 0.2mA/V2 , VTN1 = 0.4 V, VTN2 = 1 V, VTN L = 0.9 V.**



| (a) | Find the operating mode of the load NMOS transistor. |
| --- | --- |
| (b) | Find the value of ***v*o in V and IDL, ID1, ID2 in *mA*** for ***vI*= 5.5V, *v2*= 5.5V** |
| (c) | Find the operating mode of the transistor **MD1.** |

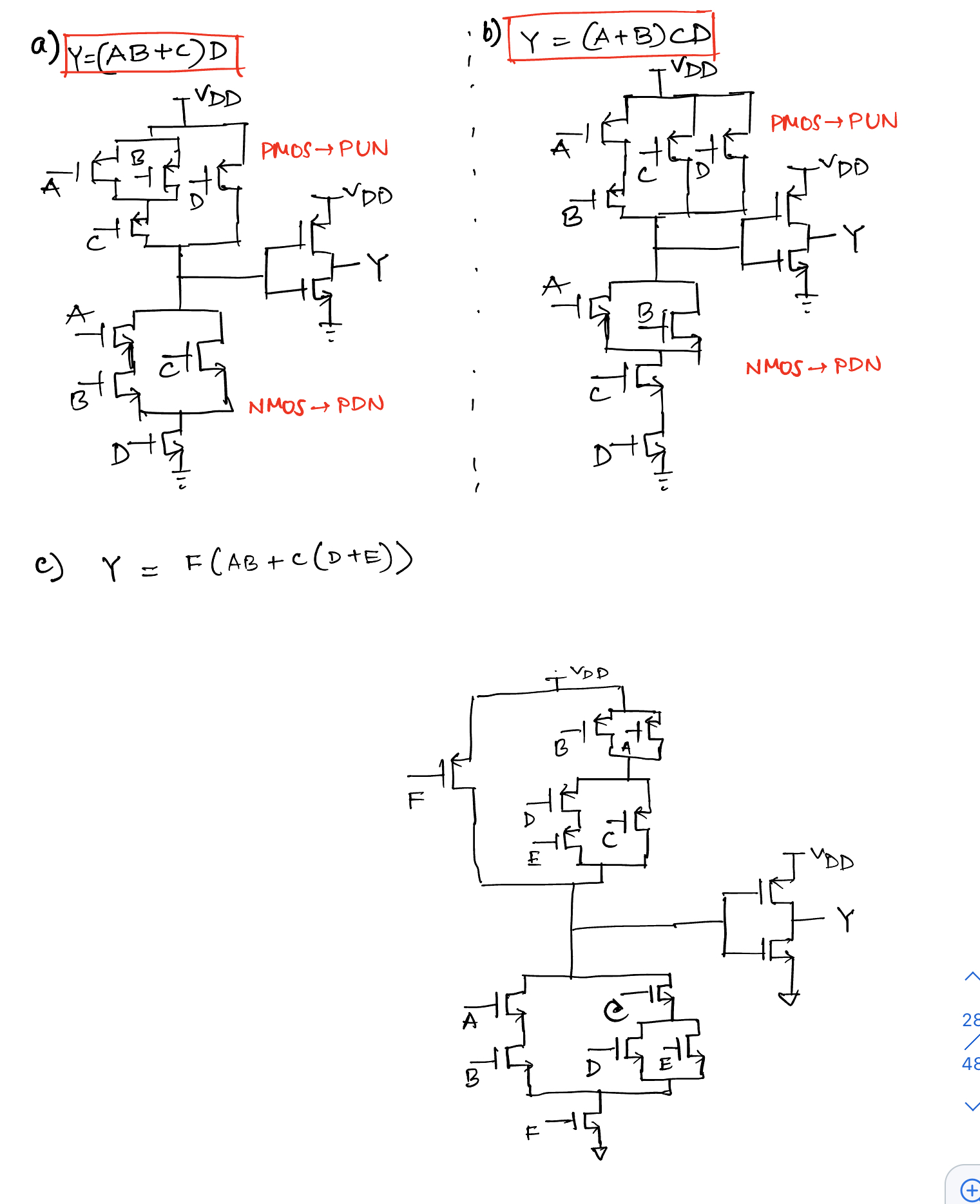
Solution:



# Question 4

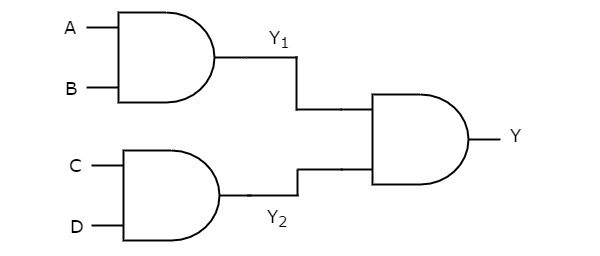
| (a) | Design a static CMOS logic circuit that implements the logic function ***Y= (AB+C)D*** |
| --- | --- |
| (b) | Design a static CMOS logic circuit that implements the logic function ***Y= (A+B)CD*** |
| (c) | Design a static CMOS logic circuit that implements the logic function ***Y= F(AB+C(D+E))*** |

Solution:



# Question 5

Design a CMOS logic circuit to implement the given compound gate in Figure below. First derive the logical expression of output Y and then design the CMOS network.



Solution:

