Organization of Digital Computer Lab
EECS112L/CSE 132L

Assignment 1
Working with CAD tools

Student name:
Mario Ruiz
Student ID:
46301389

EECS Department
Henry Samueli School of Engineering
University of California, Irvine

January, 10, 2016

1 What you've learned

I learned how to use the MentorGraphics Questasim toolset through the UCI Linux servers such as zuma.eecs.uci.edu in order to simulate and test VHDL code. We can also simulate and test our VHDL code using the Cadence Incisive toolset, however we need to use the UCI sun SPARC servers because the Linux servers don't support the Cadence toolset.

2 MentorGraphics QuestaSim toolset

2.1 Description

First we load the setup.csh and pre_compile.csh files into the command prompt.

```
zuma% source setup.csh
zuma% source pre_compile.csh
QuestaSim-64 vmap 10.4c Lib Mapping Utility 2015.07 Jul 19 2015
vmap work questa/work
Copying /home/linware/mentor/questa/questasim/linux_x86_64/../modelsim.ini to modelsim.ini
Modifying modelsim.ini
** Warning: (vlib-34) Library already exists at "questa/work".
QuestaSim-64 vmap 10.4c Lib Mapping Utility 2015.07 Jul 19 2015
vmap -c mtiUvm questa/work
Modifying modelsim.ini
** Warning: vmap will not overwrite local modelsim.ini.
QuestaSim-64 vmap 10.4c Lib Mapping Utility 2015.07 Jul 19 2015
vmap work questa/work
Modifying modelsim.ini
```

Next we compile the VHDL file for the alu.

```
zuma% vcom -64 -f rtl.cfg
QuestaSim-64 vcom 10.4c Compiler 2015.07 Jul 19 2015
Start time: 17:08:20 on Jan 10,2016
vcom -64 -f rtl.cfg
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package NUMERIC_STD
-- Compiling entity ALU_32
-- Compiling architecture Behavioral of ALU_32
End time: 17:08:20 on Jan 10,2016, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

Then we compile the System Verilog file for the test bench.

```
zuma% vlog -64 -sv -f tb.cfg
QuestaSim-64 vlog 10.4c Compiler 2015.07 Jul 19 2015
Start time: 17:09:34 on Jan 10,2016
vlog -64 -sv -f tb.cfg
-- Compiling module alu_32_tb

Top level modules:
        alu_32_tb
End time: 17:09:34 on Jan 10,2016, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
zuma%
```

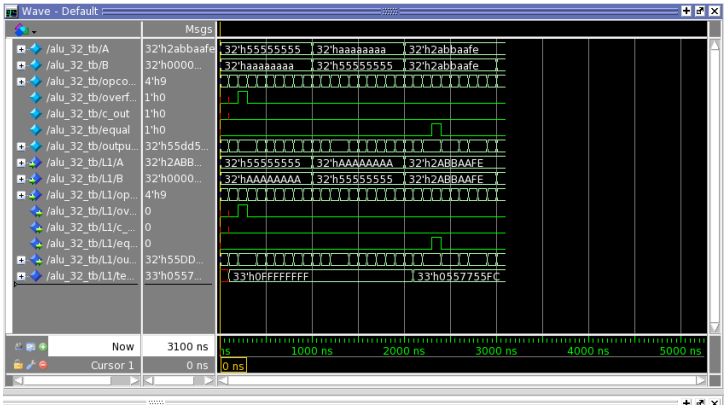
Then we optimize the VHDL design for the alu.

```
zuma% vopt -64 alu_32_tb +acc=mpr -o alu_32_tb_opt
QuestaSim-64 vopt 10.4c Compiler 2015.07 Jul 19 2015
Start time: 17:11:03 on Jan 10,2016
vopt alu_32_tb "+acc=mpr" -o alu_32_tb_opt

Top level modules:
       alu_32_tb

Analyzing design...
-- Loading module alu_32_tb
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package NUMERIC_STD
-- Loading entity ALU_32
-- Loading architecture Behavioral of ALU_32
Optimizing 2 design-units (inlining 0/1 module instances, 0/0 UDP instances):
-- Optimizing module alu_32_tb(fast)
-- Optimizing architecture Behavioral of ALU_32
Optimized design name is alu_32_tb_opt
End time: 17:11:03 on Jan 10,2016, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
zuma%
```

Finally, we simulate the alu using the testbench.

```
zuma% vsim -64 -l simulation.log -do sim.do -c alu_32_tb_opt
Reading pref.tcl

# 10.4c

# vsim -l simulation.log -do "sim.do" -c alu_32_tb_opt
# Start time: 17:12:12 on Jan 10,2016
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCIAL
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECTION 552.
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UNDER
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.alu_32_tb(fast)
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.alu_32(behavioral)#1
# do sim.do
# .
# waveform.wlf
# ** Warning: (vsim-151) NUMERIC_STD.TO_INTEGER: Value -1431655766 is not in bounds of subtype NATURAL.
#    Time: 800 ns  Iteration: 1  Instance: .alu_32_tb.L1
# End time: 17:12:13 on Jan 10,2016, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
```

2.2 Simulation waveform



3 Cadence Incisive toolset

3.1 Description

First, compile the vhdl code for the orgate and the tb.

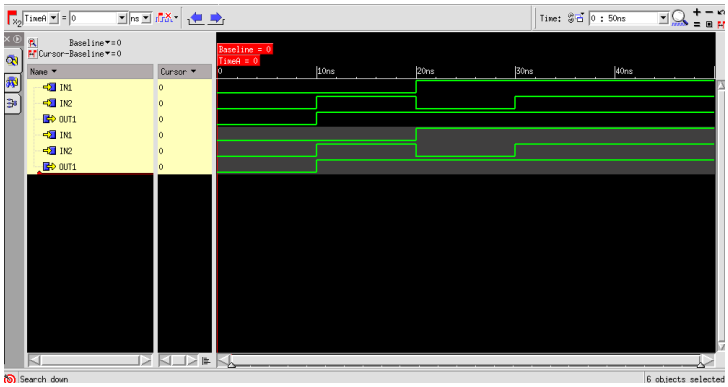
```
ncvhdl: 06.20-s015: (c) Copyright 1995-2009 Cadence Design Systems, Inc.
TOOL:   ncvhdl  06.20-s015: Started on Jan 10, 2016 at 23:19:11 PST
ncvhdl
    -messages
    orgate.vhd

orgate.vhd:
        errors: 0, warnings: 0
WORK.ORGATE (entity):
        streams: 4, words: 18
WORK.ORGATE:BEHAVIORAL (architecture):
        streams: 1, words: 23
TOOL:   ncvhdl  06.20-s015: Exiting on Jan 10, 2016 at 23:19:11 PST  (total:
 00:00:00)
```

Next elaborate and run the simulation in order for it to make the appropriate waveforms.

```
ncsim: 06.20-s015: (c) Copyright 1995-2009 Cadence Design Systems, Inc.
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm -all -variables -depth all
Created probe 1
ncsim> run 50 ns
Ran until 50 NS + 0
ncsim> simvision
ncsim: *E,TCLERR: SimVision process terminated before a connection was estab
lished..
ncsim> simvision &
ncsim: *E,TCLERR: SimVision process terminated before a connection was estab
lished..
ncsim> exit
```

3.2 Simulation waveform

Simulation Waveform is as follows:



4 Conclusion

I would prefer to use the MentorGraphics Questasim toolset for the 112L course because the Cadence Incisive toolset needed a lot more steps to work properly. For example we need to set up a project folder with many other file for each new project. Also there was more work needed in order to view the waveforms in Cadence. On the other hand, the MentorGraphics toolset did not need any new files created other then the actual files for the assignment. Also the waveform was easily viewed compared to the Cadence toolset. Overall my experience with the MentorGraphics toolset was a lot less tedious.