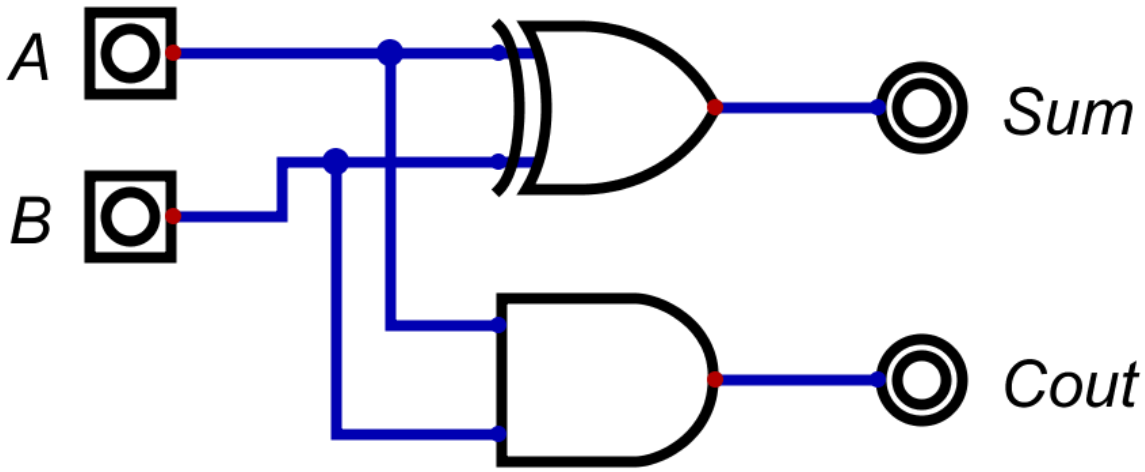
Problem:
Build CPU based on following requirements:

1. **Word Size of CPU = 6**
2. **ALU Operations = XOR,ADD,SHR**
3. **Register Number = 6**
4. **Size of RAM = 7**
5. **Word size of ISA and RAM = 15**
6. **CPU Instructions = Register Mode, Immediate Mode, JMP, JG**

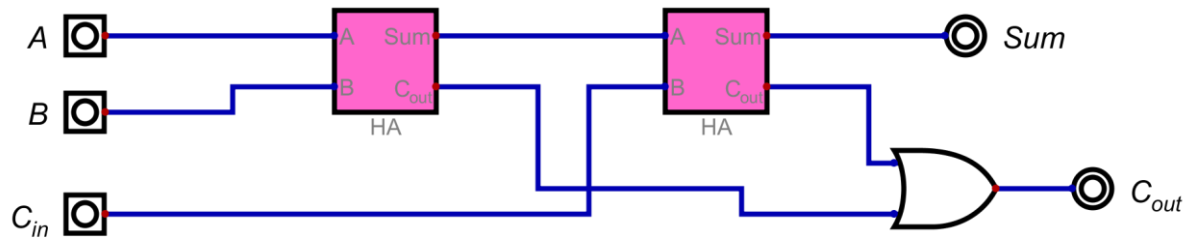
Solution:
Simulator Design:

1. **ALU Circuit (Top to Bottom all circuits):**

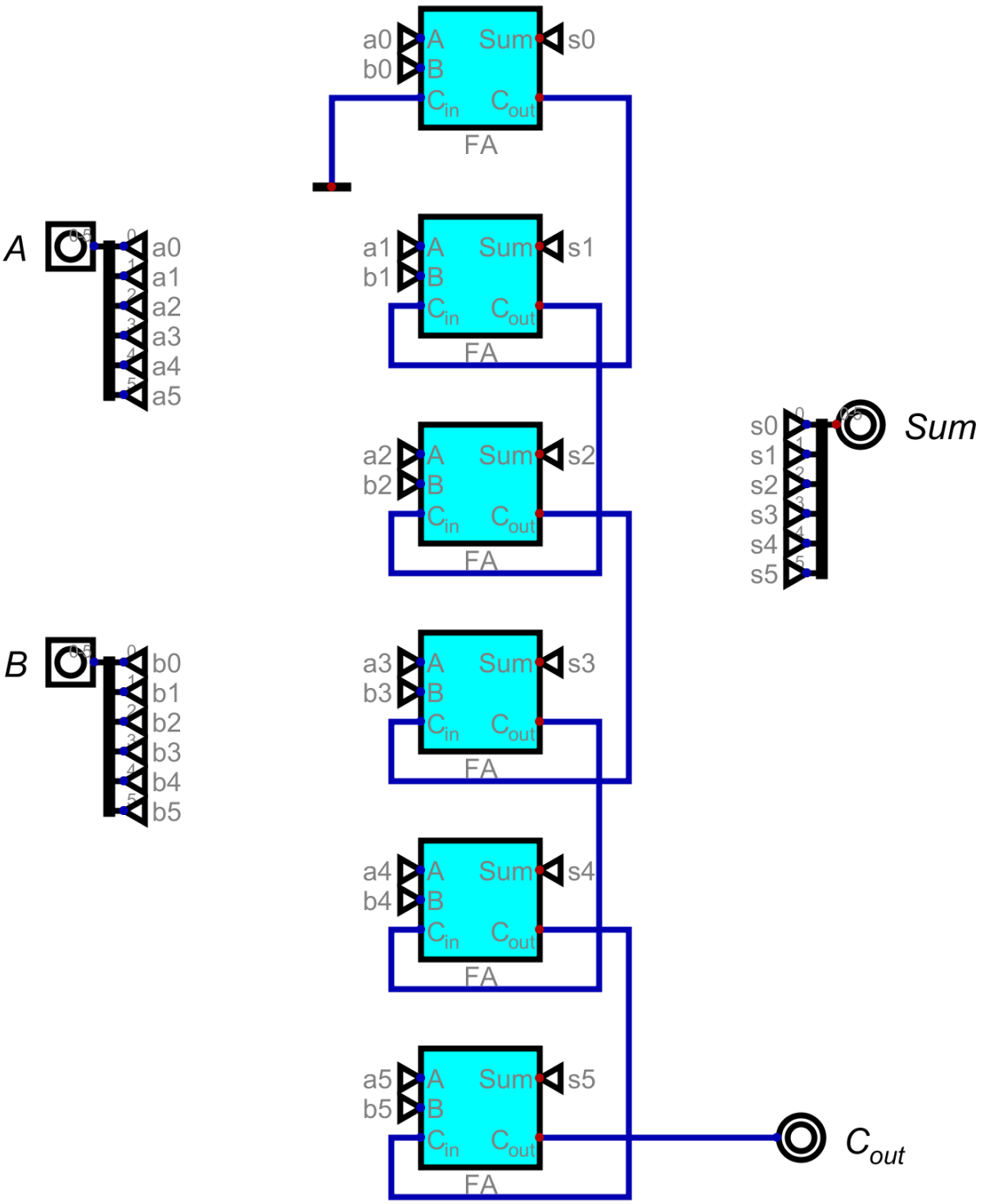
Half Adder



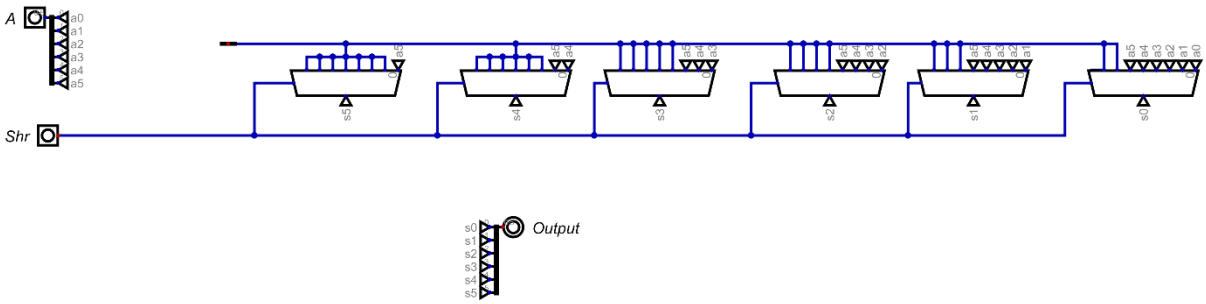
Full Adder



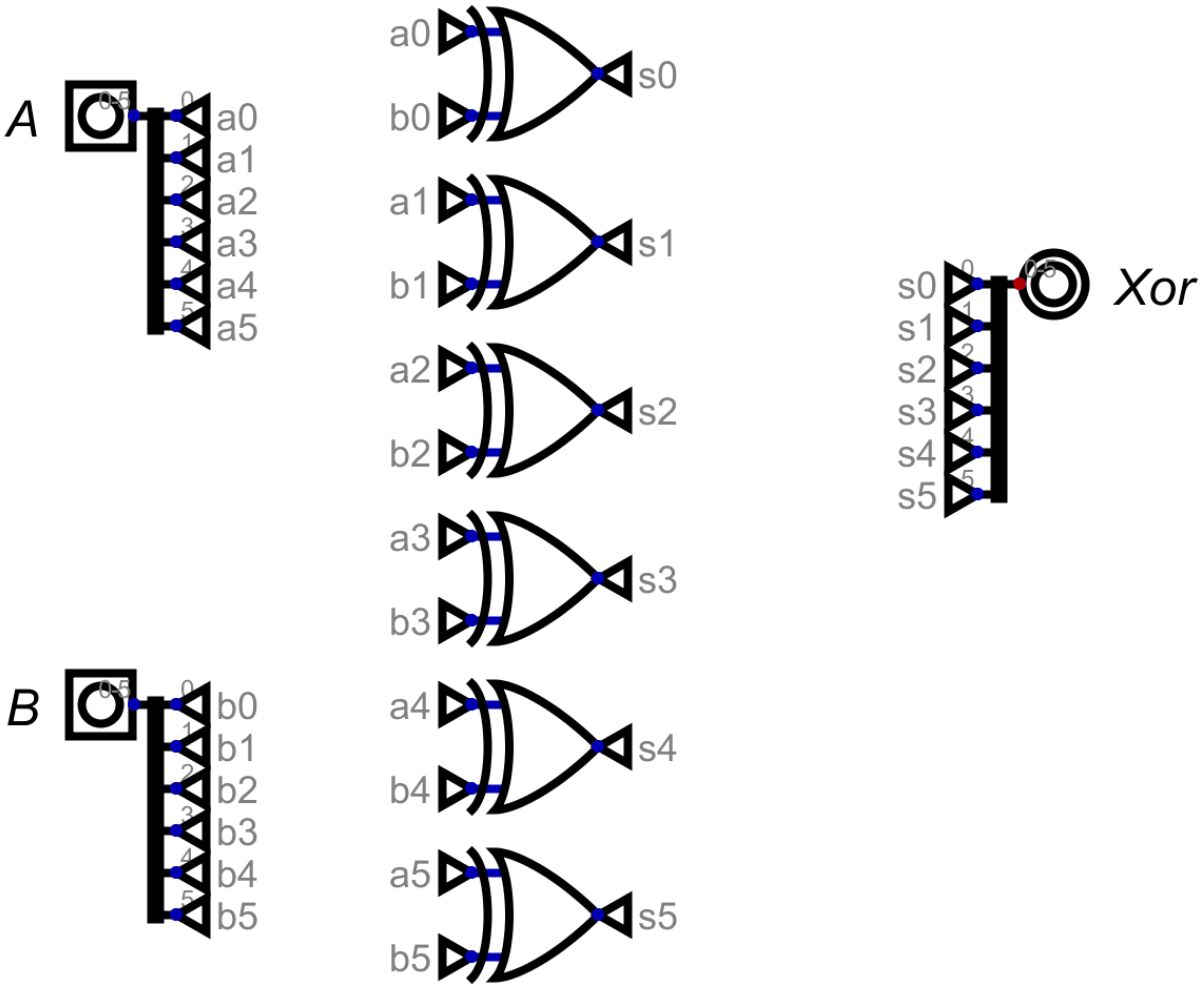
6-bit Adder


A
a0
a1
a2
a3
a4
a5
B
b0
b1
b2
b3
b4
b5
a0
b0
A
B
Sum
s0
Cin
Cout
FA
a1
b1
s1
a2
b2
s2
a3
b3
s3
a4
b4
s4
a5
b5
s5
s0
s1
s2
s3
s4
s5
Sum
Cout

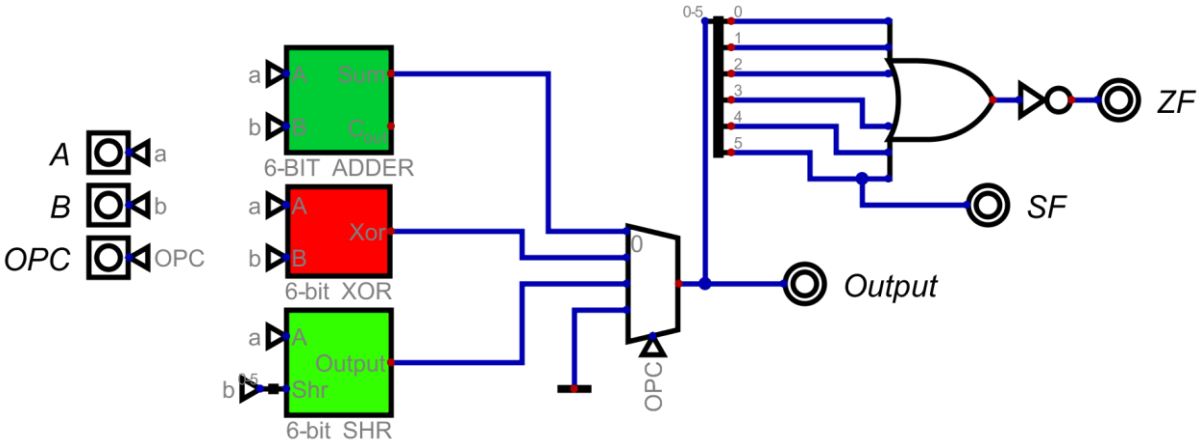
6-bit SHR



6-bit XOR

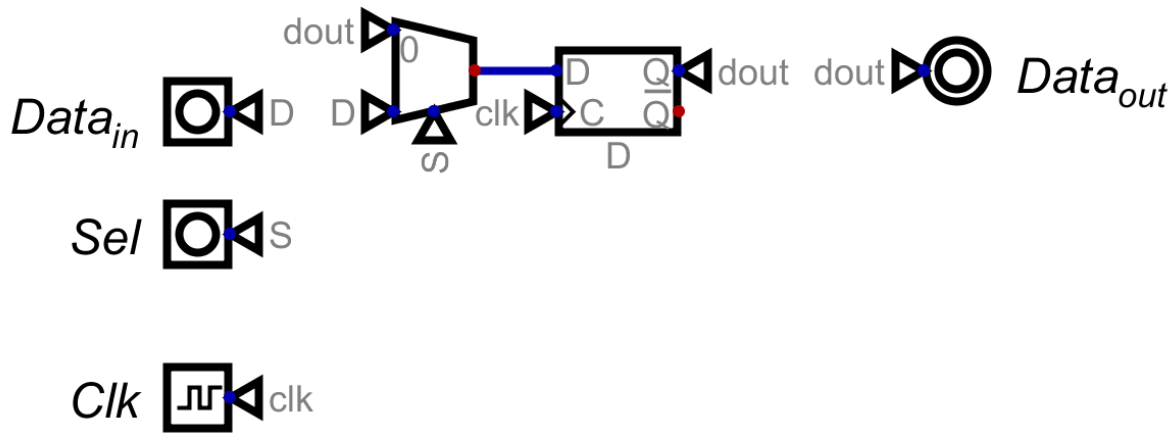


Arithmetic Logic Unit

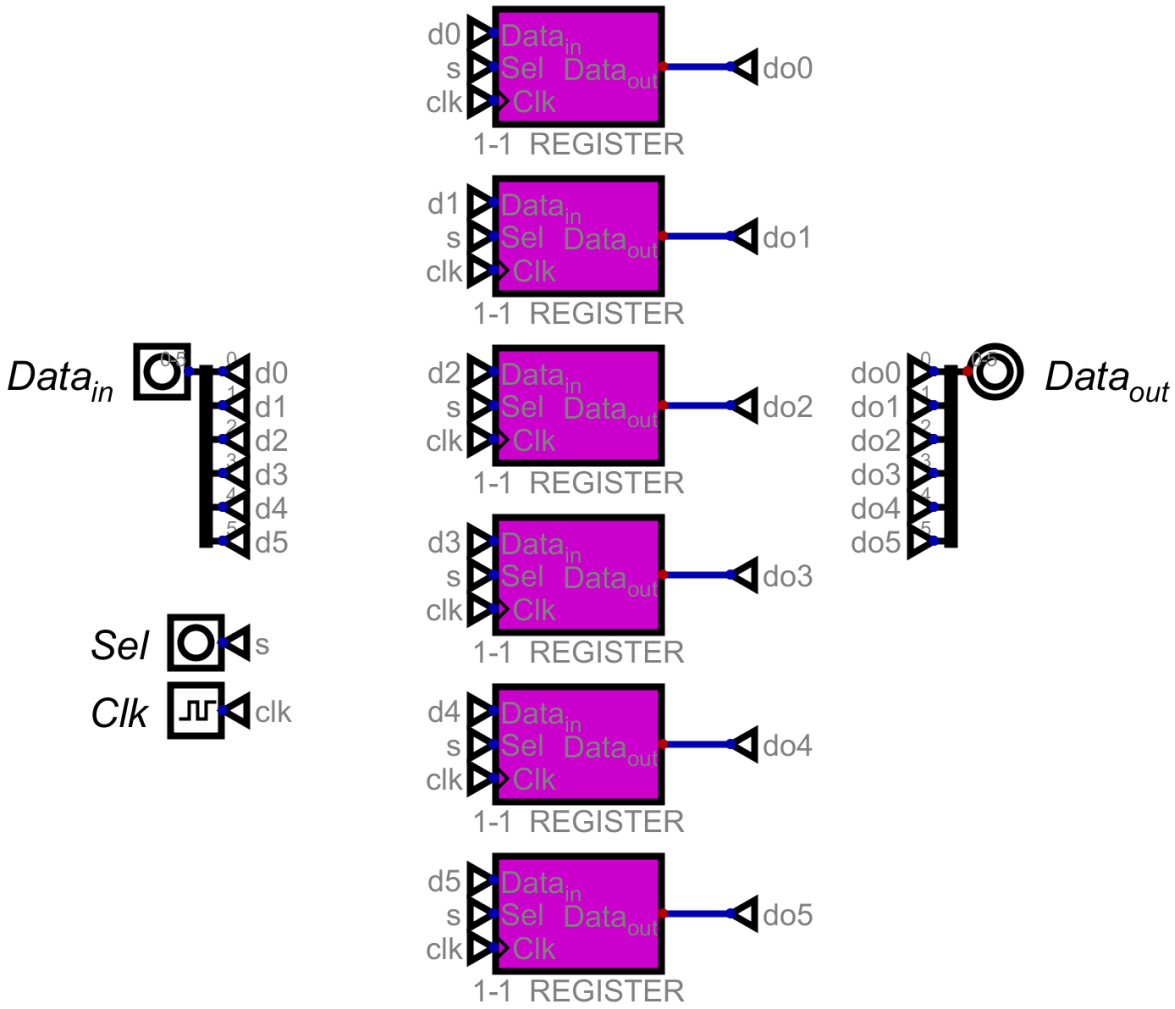


2. **Register Set Circuit (Top to Bottom all circuits):**

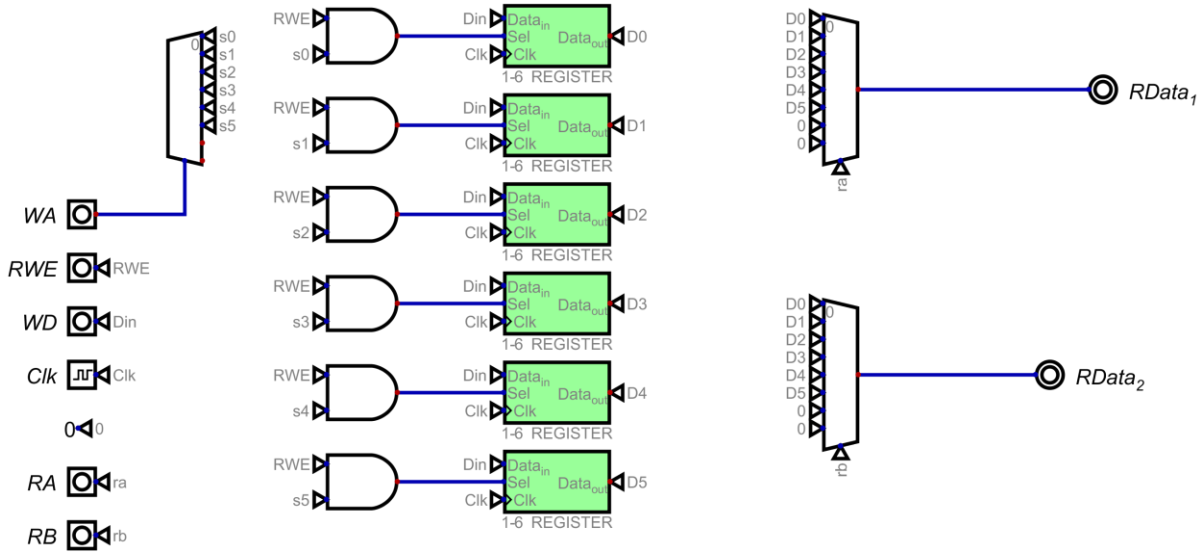
1-1 Register



1-15 Register

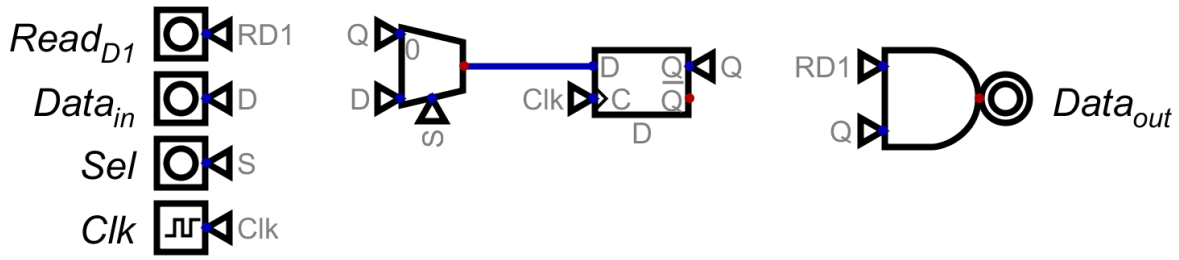


6-15 Register

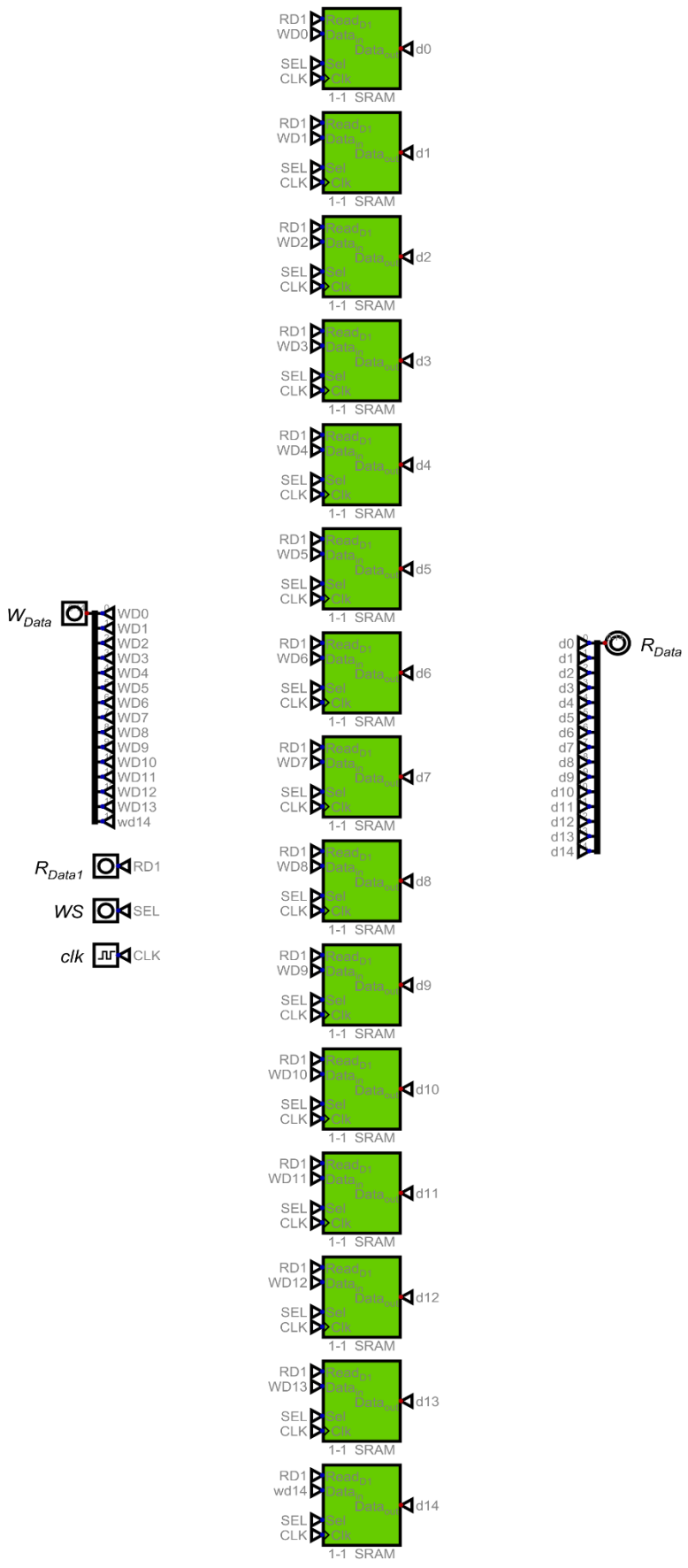


3. RAM Circuit (Top to Bottom all circuits):

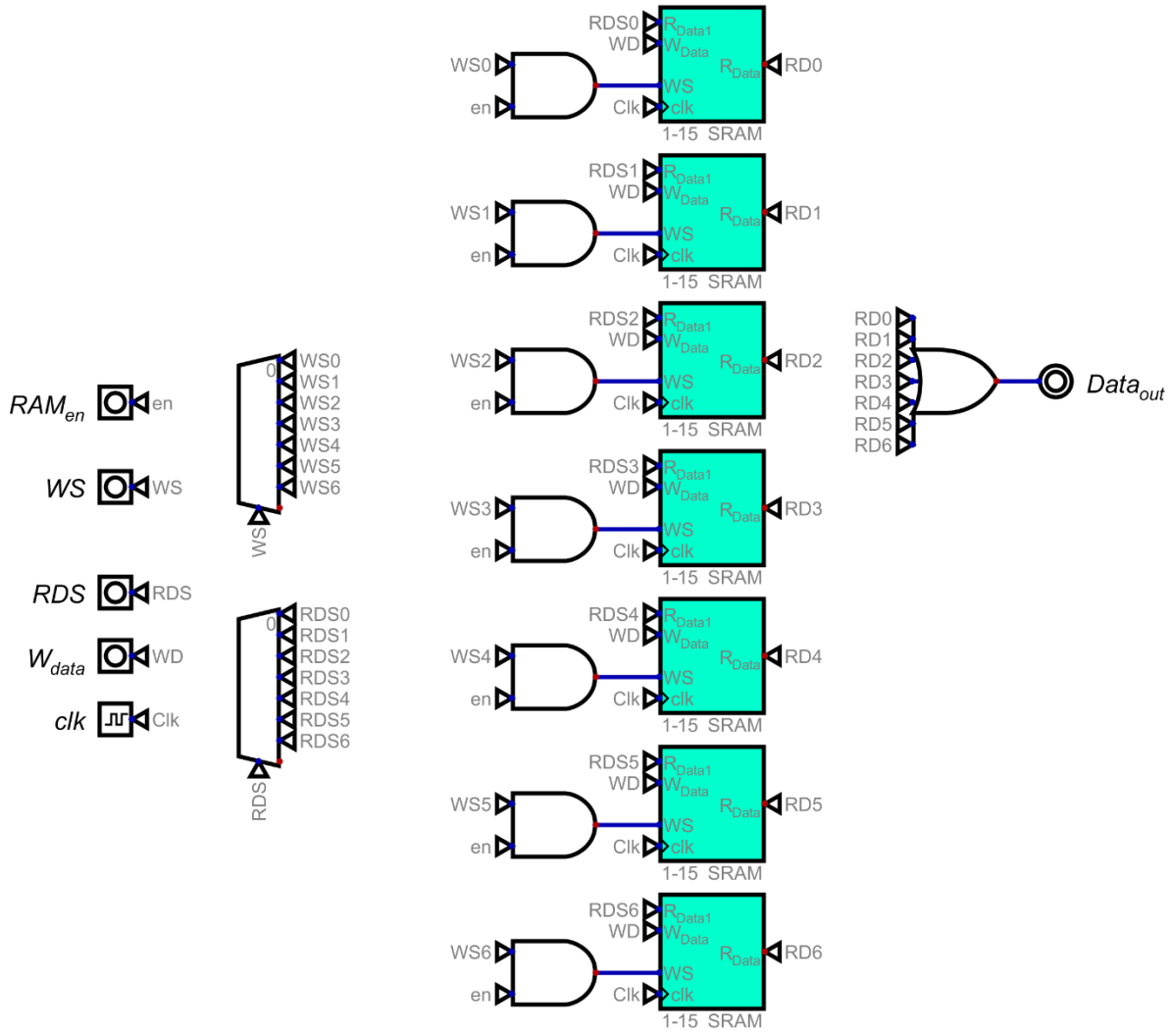
1-1 SRAM



1-15 SRAM


W_{Data}
WD0
WD1
WD2
WD3
WD4
WD5
WD6
WD7
WD8
WD9
WD10
WD11
WD12
WD13
wd14
R_{Data1}
RD1
WS
SEL
clk
CLK
RD1
WD0
SEL
CLK
d0
1-1 SRAM
RD1
WD1
SEL
CLK
d1
1-1 SRAM
RD1
WD2
SEL
CLK
d2
1-1 SRAM
RD1
WD3
SEL
CLK
d3
1-1 SRAM
RD1
WD4
SEL
CLK
d4
1-1 SRAM
RD1
WD5
SEL
CLK
d5
1-1 SRAM
RD1
WD6
SEL
CLK
d6
1-1 SRAM
RD1
WD7
SEL
CLK
d7
1-1 SRAM
RD1
WD8
SEL
CLK
d8
1-1 SRAM
RD1
WD9
SEL
CLK
d9
1-1 SRAM
RD1
WD10
SEL
CLK
d10
1-1 SRAM
RD1
WD11
SEL
CLK
d11
1-1 SRAM
RD1
WD12
SEL
CLK
d12
1-1 SRAM
RD1
WD13
SEL
CLK
d13
1-1 SRAM
RD1
wd14
SEL
CLK
d14
1-1 SRAM
d0
d1
d2
d3
d4
d5
d6
d7
d8
d9
d10
d11
d12
d13
d14
R_{Data}

7-15 SRAM



4. Instraction Set Architecture

1.Register Mode:

0-1 bits→mode of operation

- **00 for Register Mode**

2-3 bits → Type of operation

- **00 for ADD**
- **01 for XOR**
- **10 for SHR**

4-6 bits → Register 1

7-9 bits → Register 2

10-14 bits → Unused

2.Immediate Mode:

0-1 bits→mode of operation

- **01 for Immediate Mode**

2-3 bits → Type of operation

- **00 for ADD**
- **01 for XOR**
- **10 for SHR**

4-6 bits → Register 1

7-12 bits → Value of B

13-14 bits → Unused

3. JUM Mode:

0-1 bits→mode of operation

- **10 for JUMP Mode**

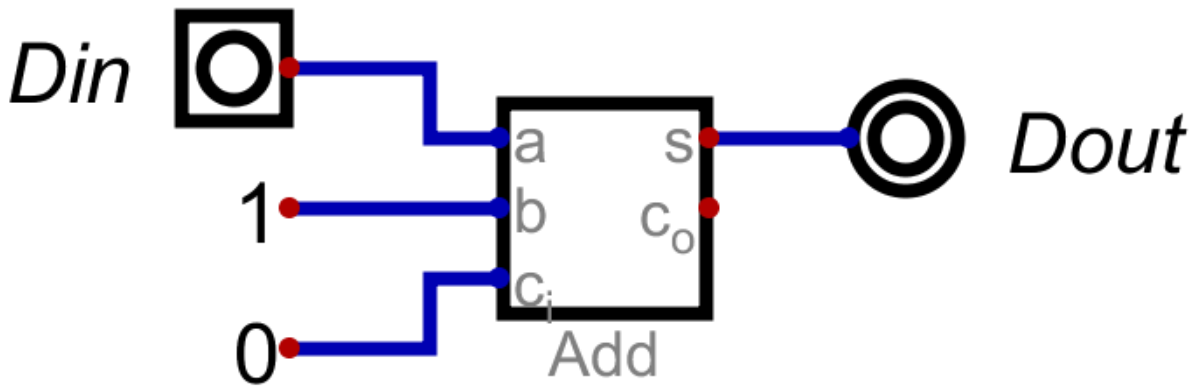
2 bits → type of JUMP

- **0 for JUM**
- **1 for JG**

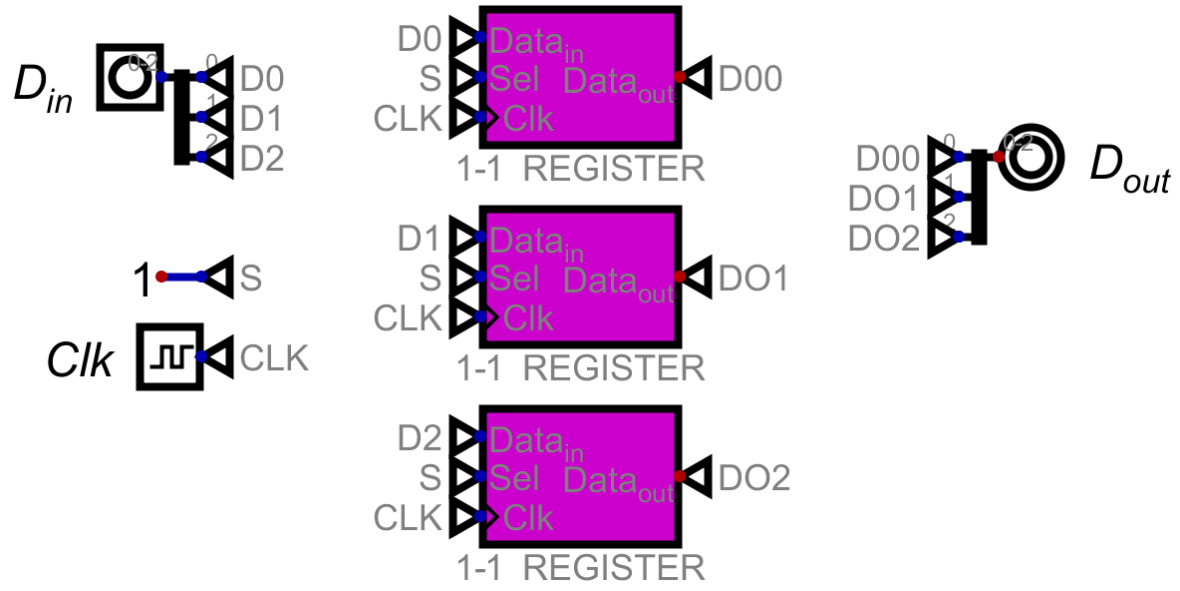
3-5 bits → Jump address

5. CPU (Top to Bottom all circuits):

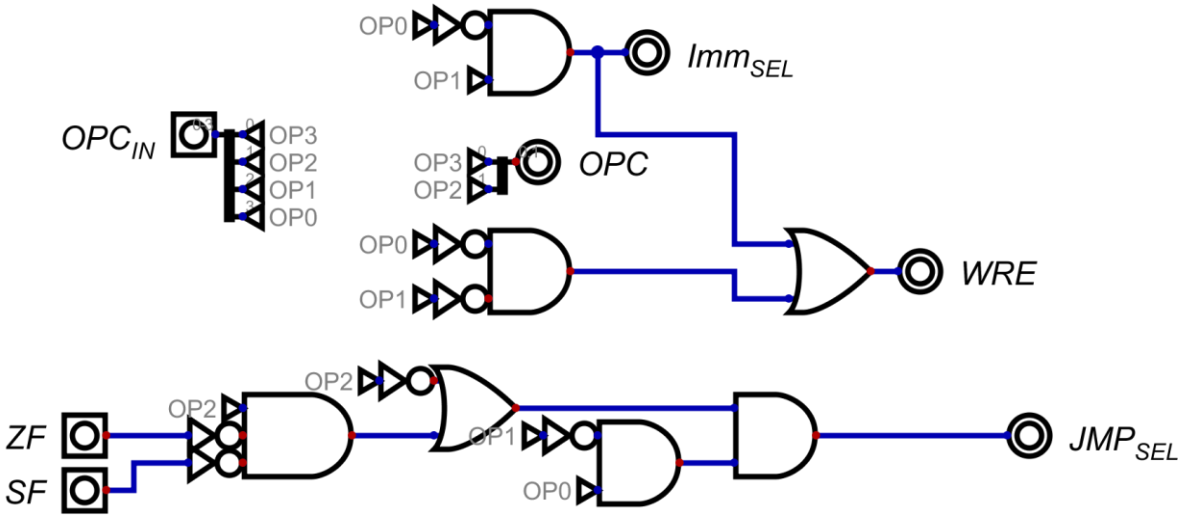
Plus 1



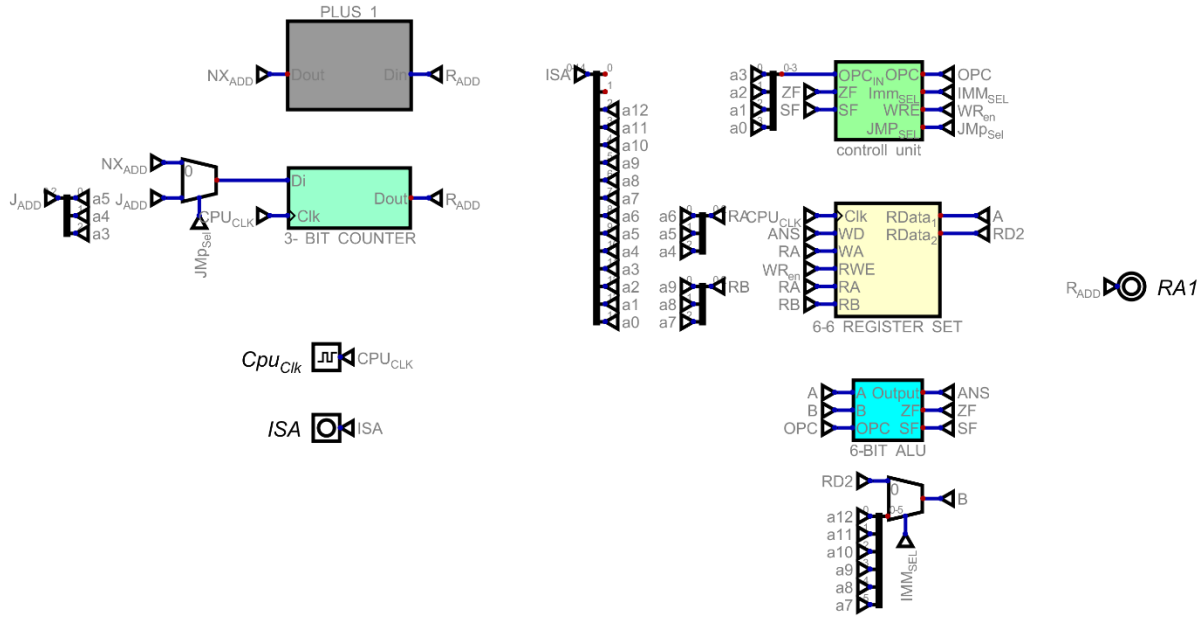
3-Bit Program Counter:



Control Unit



6-bit CPU


PLUS_1
NXADD
Dout
Din
RADD
NXADD
JADD
a5
a4
a3
JADD
0
1
CPUCLK
JMPSel
Di
Clk
Dout
RADD
3- BIT COUNTER
CpuClk
CPUCLK
ISA
ISA
ISA
a12
a11
a10
a9
a8
a7
a6
a5
a4
a3
a2
a1
a0
a3
a2
a1
a0
0-3
ZF
SF
OPCIN
ZF
SF
OPC
ImmSEL
WRE
JMPSel
OPC
IMMSEL
WRen
JMPSel
controll unit
a6
a5
a4
RA
a9
a8
a7
RB
CPUCLK
ANS
RA
WRen
RA
RB
Clk
WD
WA
RWE
RA
RB
RData1
RData2
A
RD2
6-6 REGISTER SET
RADD
RA1
A
B
OPC
A Output
B
OPC
ANS
ZF
SF
6-BIT ALU
RD2
0
1
B
a12
a11
a10
a9
a8
a7
IMMSEL