Integer-only Quantized Transformers for Embedded FPGA-based Time-series Forecasting in AIoT

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Abstract—This paper presents the design of a hardware accelerator for Transformers, optimized for on-device time-series forecasting in AIoT systems. It integrates integer-only quantization and Quantization-Aware Training with optimized hardware designs to realize 6-bit and 4-bit quantized Transformer models, which achieved precision comparable to 8-bit quantized models from related research. Utilizing a complete implementation on an embedded FPGA (Xilinx Spartan-7 XC7S15), we examine the feasibility of deploying Transformer models on embedded IoT devices. This includes a thorough analysis of achievable precision, resource utilization, timing, power, and energy consumption for on-device inference. Our results indicate that while sufficient performance can be attained, the optimization process is not trivial. For instance, reducing the quantization bitwidth does not consistently result in decreased latency or energy consumption, underscoring the necessity of systematically exploring various optimization combinations. Compared to an 8-bit quantized Transformer model in related studies, our 4-bit quantized Transformer model increases test loss by only 0.63%, operates up to 132.33 \times faster, and consumes 48.19 \times less energy.

Index Terms—AIoT, Time-series Forecasting, Transformer, Integer-only Quantization, Embedded FPGAs

I. INTRODUCTION

The integration of Artificial Intelligence with Internet of Things (IoT) devices, commonly referred to as AIoT, is revolutionizing interaction mechanisms with environments, driving innovative solutions in domains such as smart cities and smart homes [1]. In these sectors, deploying Deep Learning (DL) models on IoT devices to process sensor data locally offers significant benefits, including reduced data transmission costs and greater independence from network conditions [2].

Among DL models, Transformer-based architectures excel in effectively handling long data sequences and capturing global dependencies in fields such as Natural Language Processing (NLP) [3], Computer Vision (CV) [4], and Time-series (TS) analysis [5]. Despite efforts to simplify these models [6], optimized Transformer models are still challenging to deploy on IoT devices due to limited resources and processing power.

To address these challenges, this study aims to refine Transformer models for compact IoT devices while maintaining precision. We adopt a heterogeneous architecture by leveraging embedded Field Programmable Gate Arrays (FPGAs) as hardware accelerators for model inference, specifically targeting time-series forecasting tasks.

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Our Transformer model is tailored for the computational constraints of embedded FPGAs by streamlining layers and fine-tuning hyperparameters. Additionally, we employ integer-only quantization and Quantization-Aware Training (QAT) techniques to reduce the numerical bitwidth from 8-bit to 4-bit, optimizing resource utilization and accelerator performance on FPGAs while preserving model precision. Our co-design methodology seamlessly integrates software implementations in PyTorch with optimized hardware components on FPGAs, ensuring smooth accelerator generation and reliable performance. The main contributions of this paper are as follows:

- We design an FPGA-friendly Transformer model, quantized to 8 bits, that surpasses existing benchmarks by 8.47% on a traffic flow dataset and by 33.47% on an air quality dataset.
- We provide reusable, resource-optimized, and pipeline-enabled hardware components as VHDL templates, enabling developers to seamlessly translate a trained quantized model with 8, 6, or 4 bits into an FPGA-friendly hardware accelerator without requiring a deep understanding of FPGA development.
- We analyze the feasibility of our approach by deploying our generated accelerators on a Xilinx Spartan-7 XC7S15 FPGA. This FPGA is too small to deploy larger variants of our Transformer models, forcing us to compromise between precision and size, similar to a real IoT system. Our results show that we can deploy a 4-bit quantized Transformer model that increases test loss by only 0.63% but is 132.33× faster and consumes 48.19× less energy.

The paper is structured as follows: Section II explores our FPGA-friendly Transformer architecture. Section III outlines our approach to integer-only quantization. Section IV details the software-hardware co-design. Section V presents experimental results. Section VI reviews related literature, and Section VII concludes the paper and suggests future work.

II. FPGA-FRIENDLY TRANSFORMER

This section introduces our proposed FPGA-friendly Transformer model for single-step ahead time-series forecasting, adapted from prior work [7], [8]. As illustrated in Figure 1, the model comprises an input module, an encoder layer, and an output module. It processes the input X, a sequence of n data points, each with m dimensions, and is suitable for both univariate and multivariate time-series.

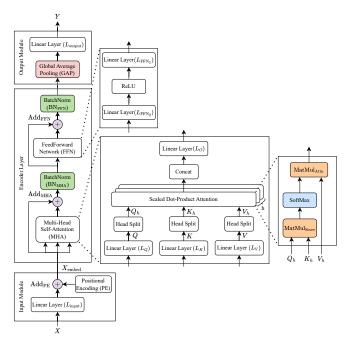


Fig. 1: The Architecture of the Transformer Model

TABLE I: Operations & Parameters of the Transformer Model

Modules			Operations	Parameters		
Input]	Linear Layer (L_{input})	$(m+1) \times d_{\text{model}}$		
		Po	sitional Encoding (PE)	-		
			Addition (Add _{PE})	-		
	МНА		Linear Layer (L_Q)	$(d_{\text{model}} + 1) \times d_{\text{model}}$		
			Linear Layer (L_K)	$(d_{\text{model}} + 1) \times d_{\text{model}}$		
			Linear Layer (L_V)	$(d_{\text{model}} + 1) \times d_{\text{model}}$		
			MatMul (MatMul _{Score})	-		
		SDA	Softmax	-		
			MatMul (MatMul _{Attn})	-		
Encoder			tput Linear Layer (L_O)	$(d_{\text{model}} + 1) \times d_{\text{model}}$		
Layer	Addition (Add _{MHA})			-		
Layer	BatchNorm (BN _{MHA})			$2d_{ m model}$		
	FFN	I	Linear Layer (L_{FFN_1})	$4(d_{\text{model}} + 1) \times d_{\text{model}}$		
			ReLU	-		
			Linear Layer (L_{FFN_2})	$(4d_{\text{model}} + 1) \times d_{\text{model}}$		
	Addition (Add _{FFN})			-		
	BatchNorm (BN _{FFN})			$2d_{\mathrm{model}}$		
Outr	Output		al Average Pooling (GAP)	-		
Output		I	Linear Layer (L_{output})	$d_{\text{model}} + 1$		

A. Parameters Simplification

To simplify the architecture and reduce training complexity, we standardized key dimensions. As detailed in Table I, we set the dimensions of the query (Q), key (K), value (V), and output vectors of the Multi-Head Self-Attention (MHA) module to d_{model} . Based on prior experience, the Feedforward Network (FFN) module dimension is set to four times d_{model} . Furthermore, we reduced the head count h in the MHA to 1. Thus, the total number of model parameters is calculated as shown in Equation 1.

$$Params_{Total} = 12d_{model}^2 + (15 + m) \times d_{model} + 1$$
 (1)

B. Encoder Enhancements

To optimize the encoder layer, we focused on two key enhancements:

1) Scaling Integration: In conventional Scaled Dot-product Attention (SDA) within the MHA module (See Equation 2¹), a scaling factor is applied after matrix multiplication (MatMul_{Score}) between Q and the transpose of K (K^T). This scaling, typically dividing by $\sqrt{d_{\text{model}}/h}$, ensures stable gradients during training by keeping the Softmax function within appropriate gradient regions. We directly integrated this scaling operation into the MatMul_{Score} (as detailed in Section IV), thereby eliminating additional computational overhead.

$$Attention(Q, K, V) = Softmax\left(\frac{QK^{T}}{\sqrt{d_{\text{model}}/h}}\right)V \tag{2}$$

2) Batch Normalization: The original Transformer model proposed in [7], [8] utilizes Layer Normalization (LN), which requires the computation of mean and standard deviation during inference. This computation, involving division and square root operations, is computationally expensive for embedded FPGAs. To address this, we replaced LN with Batch Normalization (BN) in our Transformer model, leveraging BN's ability to pre-compute statistics across entire batches during training, thus reducing computational overhead compared to LN's per-feature real-time computation [9]. Our empirical findings revealed that replacing LN with BN improves precision by 2.78% and 15.86% on the selected datasets, respectively, without compromising model performance.

III. INTEGER-ONLY QUANTIZATION

In addition to optimizing the model architecture, we utilize integer-only quantization to reduce data complexity, which is crucial for efficient deployment on embedded FPGAs. As detailed in [10], integer-only quantization maps continuous real numbers from the domain \mathbb{R} to discrete equivalents within a finite set \mathbb{Q} . This process converts a tensor X to its quantized counterpart X_q using a scale factor S and a zero point Z. The scale factor S is a floating-point value, while the zero point Z is an integer, which is crucial for rounding X to the nearest integers and clamping the results within the range of b-bit signed integers $(-2^{b-1}, 2^{b-1} - 1)$ as described in Equation 3. De-quantization reverts X_q to an approximate realvalued tensor X', using the same quantization parameters Sand Z, as illustrated in Equation 4.

$$\begin{split} X \mapsto X_q &\approx \text{clamp}(\text{round}\left(\frac{X}{S}\right) + Z, -2^{b-1}, 2^{b-1} - 1) \\ X_q \mapsto X' &= S \cdot (X_q - Z) \end{split} \tag{3}$$

$$X_a \mapsto X' = S \cdot (X_a - Z) \tag{4}$$

The quantization parameters S and Z are dynamically determined during QAT to adapt to the statistical distribution of each tensor [11]. This customization enhances model precision with lower-bit quantization compared to Post-training Quantization. Specifically, the scale factor S and the zero point Z are computed based on the observed minimum α and maximum β values of the tensor, as detailed in Equations 5 and 6, ensuring accurate representation of the original data distribution.

$$S = \frac{\alpha - \beta}{2^b - 1} \tag{5}$$

¹In this paper, the adjacency of two matrices indicates matrix multiplication.

$$Z \approx \text{clamp}\left(\text{round}((2^{b-1}-1) - \frac{\alpha}{S}), -2^{b-1}, 2^{b-1} - 1\right)$$
 (6)

In this study, all model parameters (as detailed in Table I), along with model inputs, outputs, and inter-layer activations, are designated as quantization objects. This comprehensive quantization ensures that every computation within the model utilizes integer-only operations, facilitating efficient deployment on FPGA platforms. We implemented an asymmetric quantization scheme for all quantization targets, except biases and offsetS in BN, which are quantized using a symmetric scheme. While our framework supports mixed-precision quantization, in this paper, we use a uniform quantization bitwidth across all quantization objects for simplicity and consistency.

IV. SOFTWARE-HARDWARE CO-DESIGN

A software-hardware co-design is essential for deploying the Transformer model on resource-constrained FPGAs. Our approach merges integer-only quantization with custom hardware optimizations at the register transfer level (RTL), creating VHDL templates that enhance computational efficiency and reduce resource utilization. We adapted the linear layer and ReLU components from prior work [10] on Multilayer Perceptron to handle multiple input dimensions. By processing these dimensions sequentially rather than duplicating logic circuits, we avoid excessive resource consumption on FPGAs. The following subsections detail the co-design for Transformerspecific operations.

A. Addition Component

The addition operation is described in Equation 7, where two floating-point inputs, A^1 and A^2 , are added to produce a floating-point output A^3 . In our Transformer model, there are three addition instances labeled Add_{PE} to Add_{FEN} in Table I. For integer-only addition, as outlined in Section III, A^3 can be approximated using Equation 8. To obtain the integer output S_{q}^{13} , Equation 8 is transformed into Equation 9. The terms $S_{A^{1}}$ and $\frac{S_{A^2}}{S_{A^2}}$ are the remaining floating-point values, which can be approximated using a precomputed positive integer M by right-shifting by n bits, as shown in Equation 10 (using $\frac{S_{A1}}{S_{A2}}$ as an example). This process, referred to as ApproxMul, ensures that all operations remain within the integer domain. Notably, the Add_{PE} operation in the input module uses precomputed positional information from a look-up table.

$$A^3 = A^1 + A^2 (7)$$

$$A^{3} \approx S_{A^{1}} \cdot (A_{a}^{1} - Z_{A^{1}}) + S_{A^{2}} \cdot (A_{a}^{2} - Z_{A^{2}})$$
 (8)

$$\begin{split} A_q^3 \approx \left(\frac{S_{A^1}}{S_{A^3}} \cdot (A_q^1 - Z_{A^1}) + \frac{S_{A^2}}{S_{A^3}} \cdot (A_q^2 - Z_{A^2}) \right) + Z_{A^3} & \quad (9) \\ \frac{S_{A^1}}{S_{A^3}} \approx 2^{-n} \cdot M & \quad (10) \end{split}$$

(10)

B. Matrix Multiplication Component

The co-design of the matrix multiplication component follows similar principles to the linear layer component but replaces static weights with dynamic inputs and excludes bias terms. This component involves two instances, denoted as MatMul_{Score} and MatMul_{Attn}, in Table I. As mentioned in Section II, MatMul_{Score} computes the dot product between matrices Q and K^T . We integrate the scaling factor $\sqrt{d_K/h}$ into the quantization scaling factor (see Equation 11), eliminating the need for adjustments at the RTL level and streamlining the hardware implementation process.

$$A_q^3 \approx \frac{S_{A^1} \cdot S_{A^2}}{S_{A^3} \cdot \sqrt{d_{\text{model}}/h}} \left((A_q^1 - Z_{A^1}) (A_q^2 - Z_{A^2}) \right) + Z_{A^3} \tag{11}$$

While matrix transposition of K is easily handled in the PyTorch framework with a call to transpose ()², it poses significant challenges on resource-constrained FPGAs due to its high time and memory requirements. To mitigate these costs, we implement an address-mapping mechanism that enables direct data retrieval from the non-transposed input buffer, avoiding extra time and memory for matrix transposition. This component also serves $MatMul_{Attn}$ by deactivating the address mapping block.

C. Softmax Component

Although many quantization approaches for the Softmax function have been proposed [12]-[14], our experiments revealed that none could meet our precision criteria for regression tasks. Inspired by prior work [15], we adopt a Softmax implementation based on lookup tables for computing exp () for all possible inputs. This approach relies on two lookup tables: NLUT for numerators and DLUT for denominators. As is customary, we constrain the output of the exp() function to the interval (0, 1] by offsetting all potential integer inputs X_q by the maximum value, yielding \hat{X}_q . Subsequently, the exponential values E are derived through $E = \exp(\hat{X}_q)$. To ensure effective quantization, we introduce a scaling factor S_E and a zero point Z_E as defined in Equations 12 and 13, accommodating the dynamic range within the constraints of integer precision. The DLUT and NLUT are calculated using Equations 14 and 15, respectively, ensuring bitwidths of 2bfor DLUT and 3b for NLUT to maintain sufficient precision. The integer output A_q is computed by retrieving the quantized numerators and denominators and performing the division as outlined in Equation 16, where $i, j \in [1, n]$.

$$S_E = \frac{1}{((2^{(2b-1)} - 1) - (-2^{(2b-1)}))/(n^2 \cdot h)}$$
(12)

$$Z_E = 2^{(2b-1)} - \frac{1}{S_E} \tag{13}$$

$$DLUT(\hat{X}_q) = clamp(round(\frac{E}{S_E}), -2^{2b-1}, 2^{2b-1} - 1)$$
 (14)

$$\text{NLUT}(\hat{X}_q) = \text{clamp}(\text{round}(\frac{E}{S_E \cdot S_A}), -2^{3b-1}, 2^{3b-1}-1) \tag{15}$$

$$A_q \approx \frac{\text{NLUT}(\hat{X}_q(i,j))}{\sum_{i=1}^n (\text{DLUT}(\hat{X}_q(i,j)) - Z_E)} + Z_A \tag{16}$$

Our Softmax implementation on FPGA involves three phases, as detailed in Algorithm 1. In the first phase (Lines 2-5), the algorithm iteratively scans each row to identify the maximum value (\max_i). In the second phase (Lines 6-11), all

²https://pytorch.org/docs/stable/generated/torch.transpose.html

inputs are normalized by subtracting \max_i . The resulting x_q values are then passed through NLUT and DLUT to prepare the numerators and denominators, respectively. The outputs from NLUT are stored in $X_{\rm numerators}$, while those from DLUT are summed up. In the third phase (Lines 12-13), element-wise division is performed to produce the final output.

However, this division operation is resource-intensive on FPGAs. Our evaluation of the default divider in Vivado synthesis revealed a 23 ns logic latency, limiting the system's clock frequency to below 43 MHz. Recognizing that higher clock frequencies enhance the energy efficiency of Spartan-7 FPGAs [16], we employ a *Radix-2* non-restoring divider [17], enabling the system to operate at higher clock frequencies. Although each division operation may require more clock cycles, it constitutes only a small portion of the total cycles required for one model inference. Thus, this optimization can significantly reduce overall inference time.

Algorithm 1 Softmax Implementation on FPGA

D. Batch Normalization Component

BN operates on input X with dimensions (n, d_{model}) to normalize the data using Equation 17, where μ_i and σ_i^2 represent the mean and variance of feature $j \in [1, d_{\text{model}}]$ across all samples in the batch. The scaling factor γ_i and offset β_i adjust the normalized values, while ϵ prevents division by zero. By transforming, Equation 17 can be expressed as Equation 18 with new a scaling factor $\hat{\gamma}_j$ (equals to $\frac{\gamma_j}{\sqrt{\sigma_j^2 + \epsilon}}$), and a new offset $\hat{\beta}_j$ (represents $\beta_j - \frac{\mu_j}{\sqrt{\sigma_j^2 + \epsilon}}$). Following a similar principle adopted in linear layer component, the integer output $A_q(i,j)$ can be obtained using Equation 19. Notably, we approximate the offset term $S_{\hat{\beta}_i} \cdot \beta_{j_q}$ as $S_{\hat{\gamma}_j} \cdot S_X \cdot \beta^*_{j_q}$ to streamline the calculation. Thus, the hardware implementation focuses on designing an efficient pipeline to perform elementwise dot products concurrently during data fetching. The newly computed products are then scaled using the ApproxMul operation to obtain the integer output.

$$A(i,j) = \gamma_j \cdot \frac{X(i,j) - \mu_j}{\sqrt{\sigma_j^2 + \epsilon}} + \beta_j \tag{17}$$

$$A(i,j) = \hat{\gamma_i} \cdot X(i,j) + \hat{\beta_i} \tag{18}$$

$$A_{q}(i,j) \approx \frac{S_{\hat{\gamma}_{j}} \cdot S_{X}}{S_{A}} \cdot (\hat{\gamma}_{j_{q}} - Z_{\hat{\gamma}_{j}})((X_{q}(i,j) - Z_{X}) + \hat{\beta}_{j_{q}}^{*}) + Z_{A}$$
(19)

E. Global Average Pooling Component

Given the input X with dimensions (n, d_{model}) , the GAP operation computes the average over dimension n, producing the quantized output A_q , as shown in Equation 20. To circumvent division operations and considering the fixed sequence length n, we incorporate the division factor 1/n into the quantization scaling factor. Thus, the FPGA implementation requires only a summation operation followed by an ApproxMul operation.

$$A_{q}(j) = \frac{S_{X}}{S_{A} \cdot n} \cdot \sum_{i=1}^{n} (X_{q}(i, j) - Z_{X}) + Z_{A}, \quad j \in [1, d_{\text{model}}]$$
 (20)

V. EXPERIMENTS AND RESULTS

This section outlines our experimental setup, including dataset details and processing methods. We discuss model precision, resource utilization, inference time, and power and energy consumption on a Spartan-7 XC7S15 FPGA across various model configurations.

A. Datasets and Data Processing

We used two datasets for our case studies: the *PeMS*³ dataset, which captures univariate traffic flow data from 11,160 sensor measurements over four weeks. Each series samples data at 5-minute intervals, yielding 8,064 time points. We selected a single series with sensor index 4192 to facilitate a fair comparison with [16]. The *AirU*⁴ dataset contains multivariate air quality records from 19,380 observations, featuring seven variables with Ozone as the target variable. After removing discontinuous records, the dataset was reduced to 15,258 feature-target pairs. Observations overlapping with the test set period used in [8] were split into 14,427 training samples and 831 testing samples. All data were normalized using the MinMax method to ensure uniformity in training and testing inputs.

B. Experiments Setup

Each model configuration underwent 50 training sessions consisting of 100 epochs, with early stopping implemented to prevent overfitting. We used a batch size of 256 and the Adam optimizer with standard parameters ($\beta_1 = 0.9$, $\beta_2 = 0.98$, $\epsilon = 10^{-9}$). The learning rate was initialized at 0.001, with a scheduler having a step size of 3 and a decay factor γ of 0.5 for dynamic adjustment during training. These training sessions were conducted on an NVIDIA GeForce RTX 2080 SUPER GPU, utilizing CUDA 11.0 and PyTorch 3.11 within the Ubuntu 20.04.6 LTS. The objective metric for training was the minimization of the Mean Squared Error. The Mean Squared Loss function guided the training process. Post-training, we applied an inverse transformation to the model's outputs and normalized target values to compute the Root Mean Square Error (RMSE) on the test data as the evaluation metric.

³https://doi.org/10.5281/zenodo.3939793

⁴https://dx.doi.org/10.21227/aeh2-a413

PeMS AirU Configs. RMSE RMSE Params Params FP32 4-bit FP32 n 8-bit 6-bit 8-bit 6-bit 4-bit $d_{\rm model}$ 897 0.1609 0.1809 0.2227 0.4224 945 4.055 4.791 4.696 6.616 3329 0.1988 3425 16 0.1615 0.1685 0.3117 3.726 3.858 4.004 6 32 12801 0.1652 **0.1563** 0.1971 0.3300 12993 3.799 3.665 4.095 5.731 64 50177 0.1666 0.1621 0.1855 0.4084 50561 4.236 3.506 3.923 5.699 8 897 0.1692 0.1847 0.2107 0.4226 945 3.846 5.274 6.229 6.406 0.1582 3320 0.1596 0.1922 0.3979 3425 3.878 4.804 4.675 5.853 12 12993 32 12801 0.1568 0.1617 0.1848 0.4030 3.723 4.116 64 50177 0.1586 0.1809 50561 4.071 3.518 **3.763** 5.494 0.1571 0.3279 0.5258 8 897 0.1645 0.2008 0.2158 945 3.917 5.419 6.757 3329 0.1838 0.3297 0.1593 3425 4.974 16 0.1607 3.662 4.614 5.866 18 32 12801 0.1567 0.1581 0.1918 0.3162 12993 3.603 3.796 4.012 64 50177 0.1600 0.1583 0.1845 0.3462 50561 4.055 3.518 3.897 5.286 8 897 0.1664 0.2229 0.2436 0.4841 945 4.129 5.377 7.160 6.795 0.1595 0.1673 0.1988 0.3856 16 3329 3425 3.899 4.929 5.776 5.881 24 4.019 | 4.380 | 5.700 32 12801 0.1574 0.1591 0.1943 0.4158 12993 3.867 64 0.1604 0.1573 0.1874 0.3787 50561 3.988 3.619 3.840 5.456 50177

TABLE II: Parameter Count and Test RMSE Across Various Models Configurations

To generate the accelerator, Python scripts were used to translate the trained quantized model by passing its model and quantization parameters to VHDL templates, which resulted in corresponding VHDL files. We then used GHDL simulations to estimate the number of clock cycles required per inference. The accelerator design was synthesized using Vivado, generating comprehensive reports on resource utilization, timing, and power consumption. Finally, the accelerators were validated on real hardware to assess the effectiveness and efficiency of our FPGA implementation.

C. Model Precision Across Different Configurations

To investigate the impact of model complexity on precision, we conducted experiments on both datasets with varying numbers of input features (m). These experiments also explored different input lengths (n: 6, 12, 18, 24) and embedding dimensions $(d_{\text{model}}: 8, 16, 32, 64)$, evaluating the model at different precision levels: floating-point numbers (FP32), 8-bit integers (8-bit), 6-bit integers (6-bit), and 4-bit integers (4-bit).

1) Parameter Count and FP32 Models: The Params column in Table II displays the parameter count of each model. The variance in the number of input features (m) between datasets did not significantly affect the overall parameter count, as m only influences the parameter count of the linear layer L_{input} . Increasing the embedding dimension $(d_{\rm model})$ led to a notable rise in model parameters. However, this increase did not consistently improve the precision of FP32 models, indicating that larger $d_{\rm model}$ does not necessarily enhance performance on these datasets. Additionally, increasing the input length (n) did not consistently improve precision, suggesting that incorporating more historical data points does not linearly enhance precision.

Overall, the optimal configuration for minimizing test RMSE across both datasets was n=18 and $d_{\rm model}=32$. Notably, our FP32 model outperformed benchmarks reported in [18] for the PeMS dataset, demonstrating a 16.06% improvement. Similarly, compared to FP32 results on the AirU dataset documented by Becnel et al. [8] (where n=24 and $d_{\rm model}=64$), our model achieved a 3.20% enhancement.

2) Quantization and Model Precision: Figures 2 and 3 depict the RMSE variation of quantized models compared to FP32 models on the PeMS and AirU datasets, respectively. Smaller $d_{\rm model}$ models exhibited greater sensitivity to quantization across various datasets and bitwidths, as indicated by the taller blue bars in the figures. This suggests that higher-dimensional embeddings better preserve essential information even with reduced numerical precision. However, the impact of changes in n (input length) on model precision and quantization sensitivity remained uncertain.

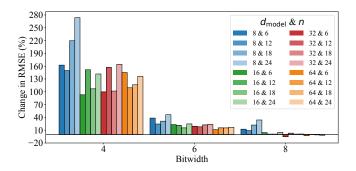


Fig. 2: PeMS Dataset: RMSE Variation

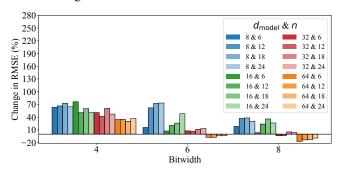


Fig. 3: AirU Dataset: RMSE Variation

The increase (at least 93.0%) in RMSE at 4-bit quantization is more pronounced on the PeMS dataset than on the AirU dataset, likely due to its univariate nature. In contrast, the multivariate nature of the AirU dataset provides enhanced

robustness against quantization effects, demonstrating up to a 76% increase in RMSE at 4-bit quantization. Notably, at $d_{\rm model}\!=\!64$, the 8-bit and 6-bit quantized models on the AirU dataset exhibited up to 17.23% and 7% lower RMSE, respectively, compared to their FP32 counterparts. On the PeMS dataset, however, only the 8-bit quantized model achieved 5.38% lower RMSE compared to FP32.

The optimal configuration of the FP32 model did not consistently yield the best precision under quantization. For instance, on the AirU dataset, the optimal configuration (with n = 6and $d_{\text{model}} = 64$) under 8-bit quantization resulted in 2.69% lower RMSE compared to the best FP32 model. Under 6-bit quantization, it (with n = 12 and $d_{\text{model}} = 64$) had 4.44% higher RMSE than the best FP32 model. For 4-bit quantization, n=18 and $d_{\rm model}=64$ provided the best outcomes, with RMSE 46.71% higher than the best FP32 model. Notably, on the PeMS dataset, our 8-bit quantized model outperformed the 8-bit quantized model reported in [18] by 8.47%. Even our 6-bit quantized model delivered comparable performance. In addition, on the AirU dataset, our 8-bit quantized model surpassed the 8-bit quantized model reported in [8] by 33.47%. Remarkably, even our 4-bit quantized model outperformed their 8-bit counterpart by 2.83%.

D. Resource Utilization

Due to space constraints, this section focuses on the AirU dataset and evaluates resource utilization, including Lookup Tables (LUTs), Block RAM (BRAM), and Digital Signal Processing Slices (DSPs), for various model configurations and quantization bitwidths on the XC7S15 FPGA. As illustrated in Table III, even when quantized to 4-bit, the largest configuration (n=24 and $d_{\rm model}=64$) exceeded the FPGA's resource capacity, hence could not be deployed (denoted by "-"). Conversely, the smallest configuration (n=6 and $d_{\rm model}=8$) fit easily within the FPGA's constraints across different quantization bitwidths, with consistent BRAM utilization at 10%. LUTs and DSPs utilization increase with bitwidth, indicating higher logic resource demand with greater numeric precision.

TABLE III: Resource Utilization on AirU Dataset

Configs.		AirU								
n	$d_{ m model}$	LUTs(%)			BRAM(%)			DSPs(%)		
		8-bit	6-bit	4-bit	8-bit	6-bit	4-bit	8-bit	6-bit	4-bit
6	8	55.6	42.0	34.2	10.0	10.0	10.0	100.0	90.0	65.0
	16	57.1	47.0	37.3	40.0	30.0	30.0	100.0	95.0	65.0
	32	62.7	50.5	41.1	55.0	55.0	40.0	100.0	95.0	65.0
	64	89.5	57.2	47.4	100.0	100.0	75.0	100.0	90.0	60.0
12	8	58.0	46.0	36.5	20.0	10.0	10.0	100.0	95.0	65.0
	16	65.1	51.5	42.7	45.0	35.0	35.0	100.0	95.0	60.0
	32	74.3	58.9	46.8	60.0	55.0	40.0	100.0	95.0	65.0
	64	-	75.3	58.2	-	100.0	75.0	-	95.0	65.0
18	8	63.4	49.9	40.8	20.0	15.0	15.0	100.0	95.0	55.0
	16	71.0	55.8	45.8	45.0	35.0	35.0	100.0	95.0	65.0
	32	85.3	67.0	53.0	60.0	55.0	40.0	100.0	95.0	65.0
	64	-	-	-	-	-	-	-	-	-
24	8	67.8	52.7	39.2	20.0	20.0	15.0	100.0	90.0	50.0
	16	77.4	60.7	48.7	45.0	40.0	40.0	100.0	95.0	65.0
	32	-	73.7	58.3	-	60.0	45.0	-	95.0	65.0
	64	-	-	-	-	-	-	-	-	-

As discussed in Section V-C, the configuration with n=6and $d_{\text{model}} = 64$ under 8-bit quantization achieved optimal RMSE. According to Table III, this configuration barely fit the FPGA, utilizing at least 89.5% of all types of resources. For 6-bit quantization, the optimal RMSE was attained with the configuration of n=12 and $d_{\text{model}}=64$. Although its test RMSE is 7.33% higher than our best 8-bit quantized model, its LUTs utilization is 14.2% lower, while DSPs utilization increases by 5%. Among all 4-bit quantized models, the two most precise ones were too large to be deployed. We chose the model with the third-best RMSE performance (5.474), which has a 56.13% higher RMSE than our best 8-bit quantized model. However, its RMSE is only 0.63% higher than that of the 8-bit quantized model in [8]. This model, with the configuration of n=12 and $d_{\text{model}}=32$, consumes only 46.8% LUTs, 40% BRAM, and 65% DSPs. It represents a feasible compromise between resource utilization and precision, making it suitable for resource-constrained applications.

E. Timing Analysis

Focusing on the three candidate configurations identified in Section V-D, we analyzed the timing performance of these FPGA-deployable models. As detailed in the third column of Table IV, the clock frequency of the 8-bit quantized model was limited to 100 MHz. In contrast, models with lower bitwidths operate at frequencies up to 25% higher, supporting the expectation that fewer bits expedite computation due to simplified logic. However, decreasing the bitwidth from 6-bit to 4-bit did not increase the frequency, likely due to reduced DSPs engagement and subsequent increases in logic delay.

The fourth column of Table IV presents the number of clock cycles required per inference, which is influenced by model configuration (n, $d_{\rm model}$). Comparing Rows 2 and 3, doubling n resulted in $2.03\times$ more clock cycles per inference. Similarly, comparing Rows 3 and 4, halving $d_{\rm model}$ led to $3.46\times$ fewer clock cycles per inference. The fifth column of Table IV outlines the model inference time, which depends on the clock frequency and the number of clock cycles. Notably, our 4-bit quantized model demonstrated the shortest inference time, while the 6-bit quantized model exhibited the longest.

F. Power and Energy Consumption

The power estimates from Vivado are also summarized in Table IV. Interestingly, the 6-bit quantized model exhibited slightly higher power consumption than the 8-bit quantized model, likely due to its increased clock frequency. However, reducing the bitwidth of computation is generally expected to conserve power, a theory validated by the 4-bit quantized model, which demonstrated the lowest total power consumption at 63 mW among the three configurations.

Energy consumption, as shown in the last column of Table IV, is calculated based on power usage and inference time. The 4-bit quantized model was the most energy-efficient, owing to its shorter inference time and lower power consumption. In contrast, the 6-bit quantized model underperformed the others, incurring the highest costs in both power and time.

TABLE IV: Performance Comparison on Spartan-7 XC7S15 FPGA

Configs.	RMSE	Clock	Clock	Time(ms) [†]	Power(mW) [†]			Energy(mI)
(n, d_{model}, b)		Frequency(MHz)	Cycles	Time(ms)	Static	Dynamic	Total	Energy(mJ)
(6, 64, 8)	3.506	100	282974	2.82	31	44	75	0.212
(12, 64, 6)	3.763	125	575696	4.61	31	48	79	0.364
(12, 32, 4)	5.474	125	166394	1.33	31	32	63	0.084

[†] The numerical estimates obtained from GHDL and Vivado exhibit 2% variance in time, and 5% variance in power when compared to the actual hardware measurements.

Notably, despite the 4-bit quantized model exhibiting a 56.13% higher RMSE than the 8-bit model, it is 2.12 times faster and $2.52\times$ more energy-efficient. This efficiency highlights the potential advantages of deploying the 4-bit quantized model on smaller FPGAs, where resource constraints are more pronounced. Conversely, our 8-bit quantized model remains a suitable choice when precision is paramount.

VI. RELATED WORK

Research on quantizing Transformer-based architectures has been extensive, particularly in the domains of NLP [13] and CV [14]. These models, known for their substantial computational demands, are primarily deployed on cloud-based servers and edge servers equipped with GPUs. However, relevant studies in TS, especially time-series forecasting, remain underexplored. Becnel et al. [8] implemented an 8-bit quantized Transformer on a low-power microcontroller unit (MCU) for time-series forecasting, achieving a power consumption of 23 mW but with an inference time of 176 ms. In contrast, our 4-bit quantized Transformer accelerator on an embedded FPGA achieves up to 132.33× faster inference with only a 0.63% increase in test loss. Despite a 2.74× increase in power consumption, it consumes 48.19× less energy, indicating that integrating an FPGA-based accelerator with the MCU could be beneficial.

Previous works [19], [20] have explored implementing Transformer models on FPGAs for time-series applications, but their target platforms are server-grade or edge-grade FPGAs, which are unsuitable for embedding into IoT devices. In contrast, we chose the Xilinx Spartan-7 FPGA as our target platform. Although resource-constrained, it offers a balanced solution in terms of speed and energy efficiency for deploying Transformer models.

VII. CONCLUSION AND FUTURE WORK

In this study, we implemented an FPGA-friendly Transformer model using software-hardware co-design to balance model precision, resource utilization, timing, power and energy. We adopted QAT in the PyTorch framework to ensure model precision and conducted low-bit integer-only inference simulations prior to accelerator generation. Furthermore, our approach utilized VHDL templates and automatic generation scripts to facilitate the seamless translation of trained quantized models into FPGA-ready accelerators. Through hardware validation, we confirmed the effectiveness of our approach.

In future work, we plan to extend our approach to mixedprecision quantization. Additionally, we aim to optimize the hardware implementation further to improve energy efficiency, thereby advancing the sustainability of Transformer models for time-series forecasting in AIoT systems.

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