CS 530, Fall 2014 **Computer Architecture** Homework #2
Due Date: 22 Sep 2014

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1. H&P Problem 2.4, parts a-d
2. H&P Problem 2.8, parts a-b
3. H&P Problem B.1, parts a-c
4. H&P Problem B.9
5. H&P Problem B.12
6. For a direct cache of size 8kB, a word size of 32 bits, and a block size of 8 words, answer the following:
    a. Number of lines in the cache?
    b. Number of bits per tag?
    c. Total number of bits required for the cache?
7. For a 4-way set associative cache of size 8kB, a word size of 32 bits, and a block size of 8 words, answer the following:
    d. Number of lines in the cache?
    e. Number of bits per tag?
    f. Total number of bits required for the cache?
8. Assume a computer with a virtual address space of 32 bits and a physical address space of 24 bits. Assuming a page is 4KB, then how many bits are required for the page table? (Assume all virtual pages are being used.)
9. Assume a 2-way set associative cache using LRU with a total of 16 words and a block size of 4 words. For the following word addresses, tell whether each is a hit or a miss. Give the final contents of the cache. Word addresses: 4, 7, 15, 11, 13, 2, 9, 32, 45, 1, 9, 7, 8, 52, 21, 12
10. Assume a direct cache with a total of 16 words and a block size of 4 words. For the following word addresses, tell whether each is a hit or a miss. Give the final contents of the cache. Word addresses: 4, 7, 15, 11, 13, 2, 9, 32, 45, 1, 9, 7, 8, 52, 21, 12