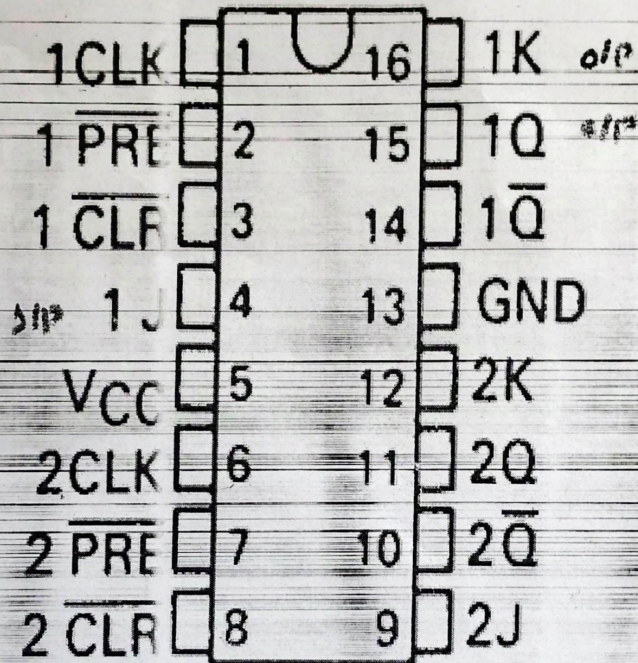


SN5476, SN54LS76A . . . J PACKAGE

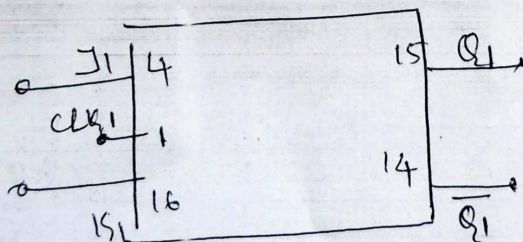
SN7476 . . . N PACKAGE

SN74LS76A . . . D OR N PACKAGE

(TOP VIEW)



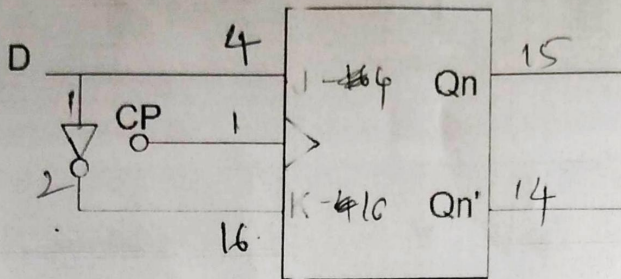
J K Flip Flop.



Truth Table

J	K	CLK	Q_1
0	0	\uparrow	Q_0 (no change)
1	0	\uparrow	1
0	1	\uparrow	0
1	1	\uparrow	$\overline{Q_0}$ (toggle)

JK-D

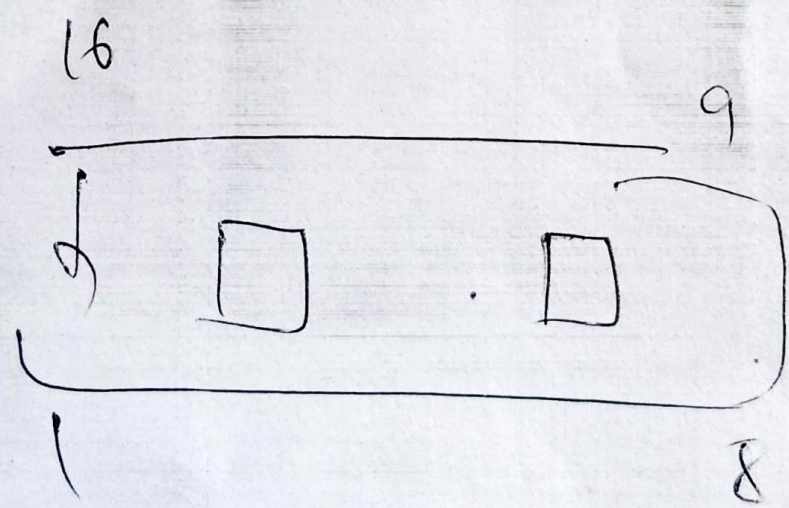


D	Qn	Qn+1	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

2. Flip-flop

clock	D	Qn	Qn+1
0	x	0/1	Qn
1	0	0/1	0
1	1	0/1	1

1	1	$\overline{Q_n}$
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$J_1 - 4$ { I/P PRE

$K_1 - 16$ }

$Q_1 - 15$

$\overline{Q_1} - 14$

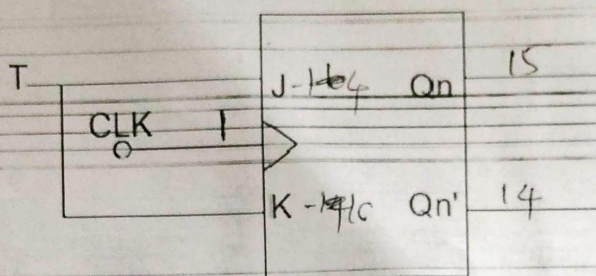
$\overline{CLK} - 1$

I/P clc

pin *

ground

JR-T



✓	T	Qn	Qn+1	J	K
	0	0	0	0	x
	0	1	1	x	0
	1	0	1	1	x
	1	1	0	x	1

Clock	T	Qn	Qn+1
0	x	0/1	Qn
1	0	0/1	Qn
1	1	0	1
1	1	1	0