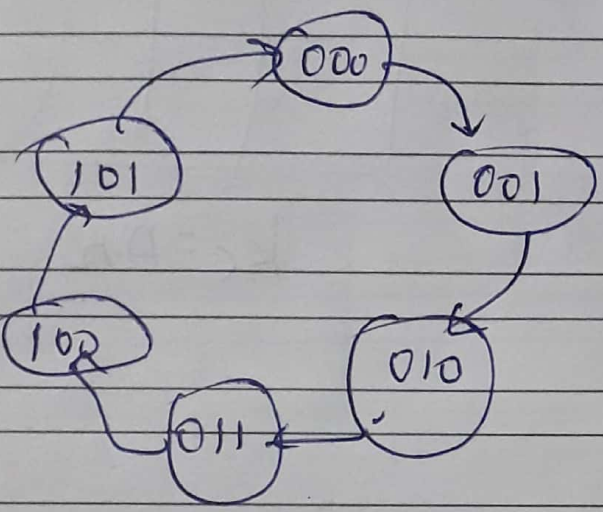
PAGE NO:
DATE: / /

10.7 Counter Design as a Synthesis Problem

Design of modulo-6 counter for the sequence given below.



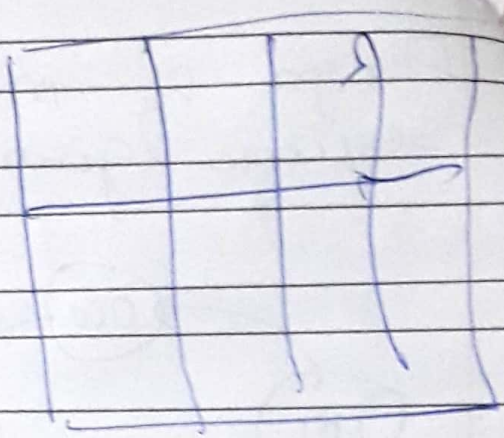
state sequence.

C_n	B_n	A_n	C_{n+1}	B_{n+1}	A_{n+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X				
0	0	1	0	1	0	0	X				
0	1	0	0	1	1	0	X				
0	1	1	1	0	0	1	X				
1	0	0	1	0	1	X	0				
1	0	1	0	0	0	X	0				

Excitation table of JK

$Q_n \to B_{n+1}$	J	K
0 0	0	X
0 1	1	X
1 0	X	1
1 1	X	0

C_n \ $B_n A_n$	00	01	11	10
0	0	0	1	0
1	x	x	x	x

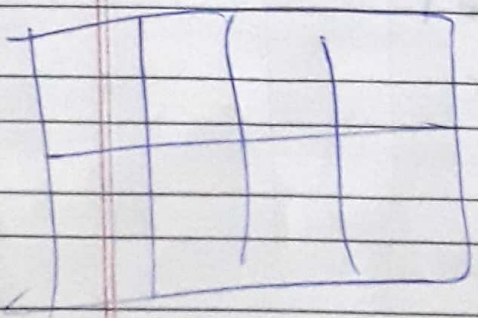


$J_C = B_n A_n$

$K_C = A_n$

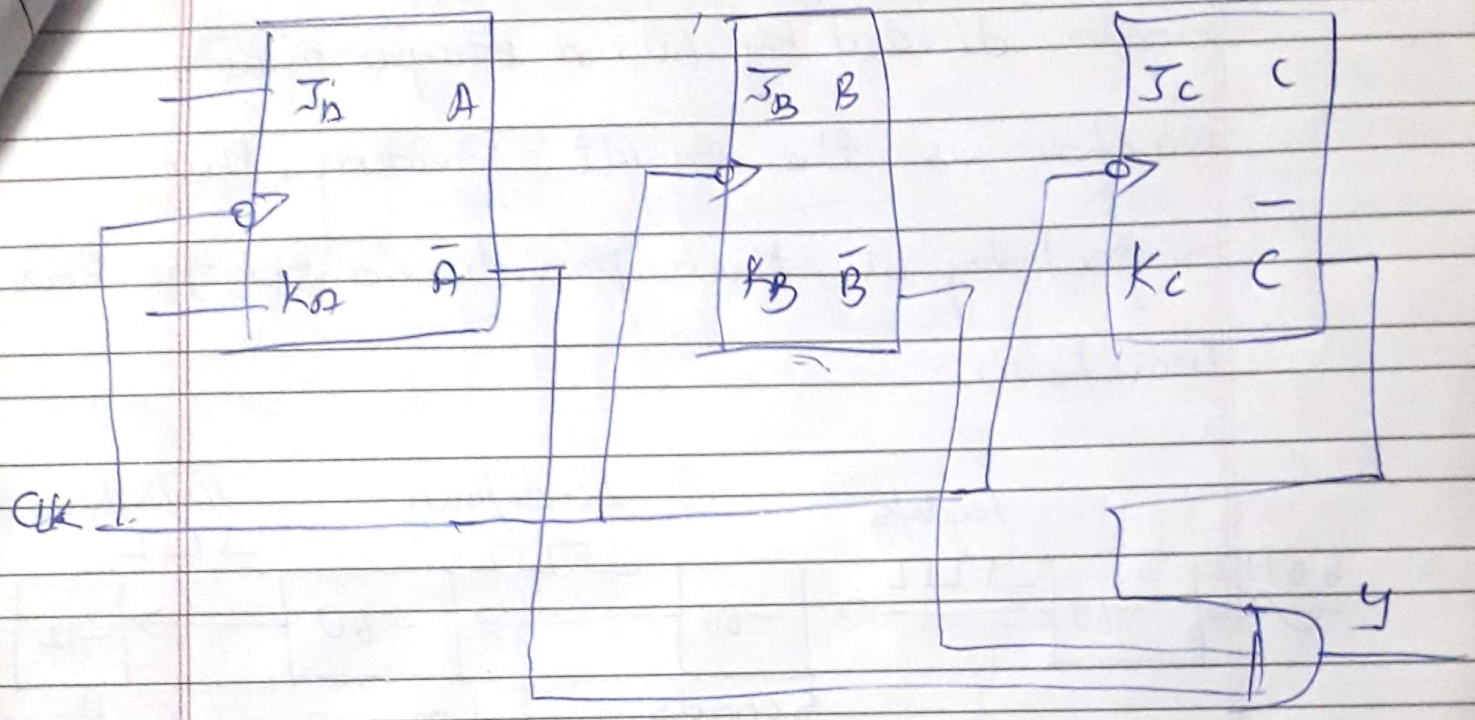
$J_B = \bar{C}_n \bar{A}_n$

$K_B = A_n$



$J_A = 1$

$K_A = 1$

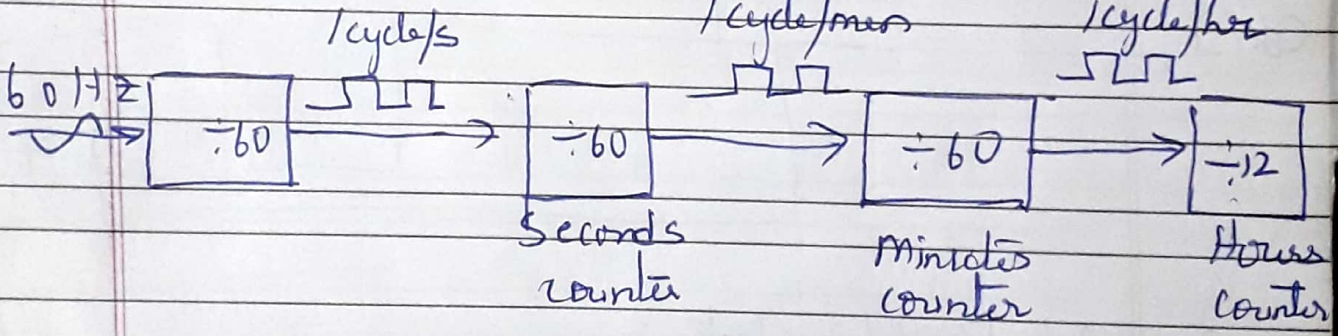


10.8 A Digital clock.

A very interesting application of counters and decoding arises in the design of a digital clock. The power supply for this system is usual 60Hz.

In order to obtain pulses occurring at a rate of one each second, it is necessary to divide the 60-Hz power source by 60.

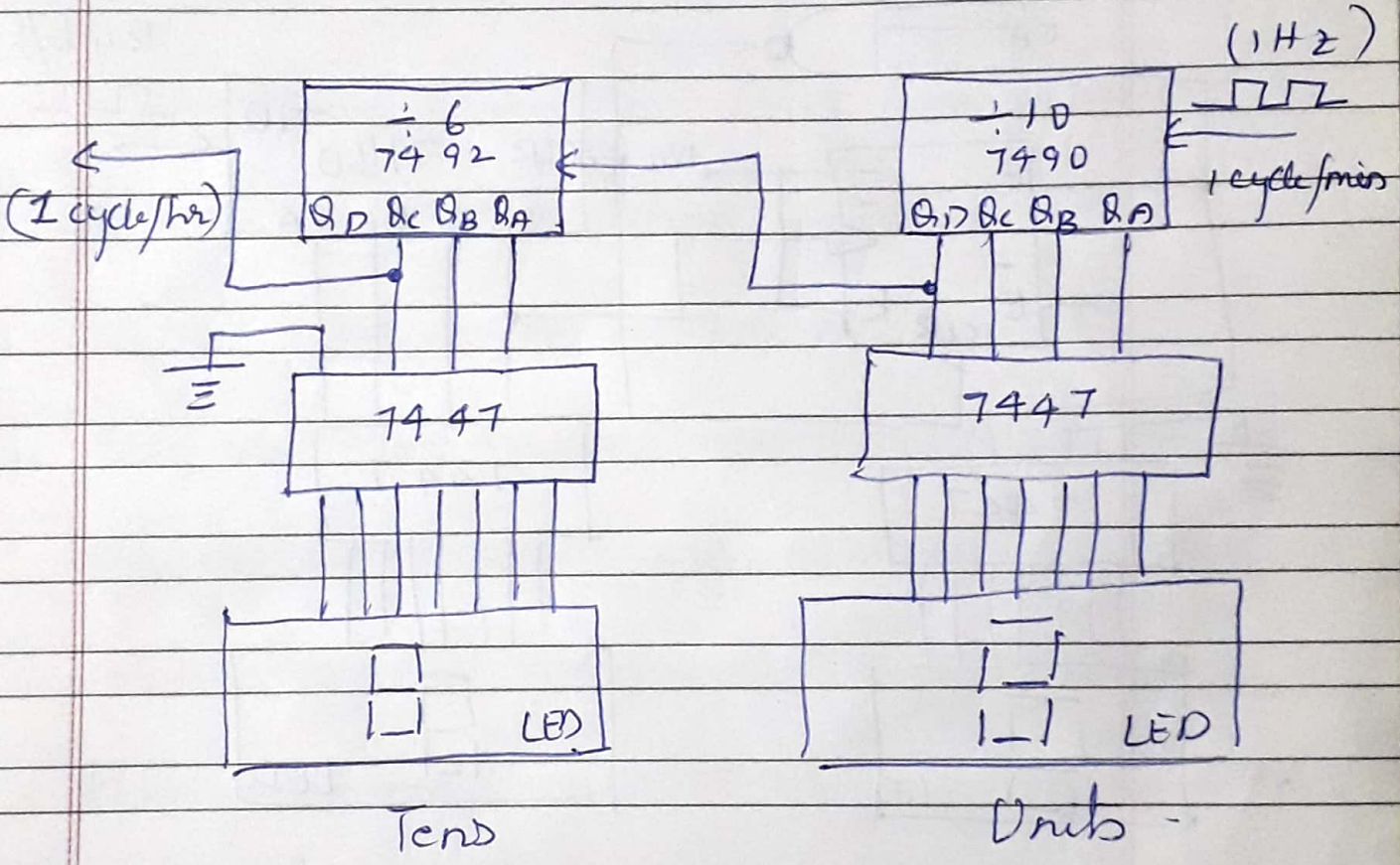
If the resulting 1-Hz waveform is again divided by 60, a one-per-minute waveform is the result. Dividing this signal by 60 then provides a one-per-hour waveform.



1011
1100
$Q_A Q_B$

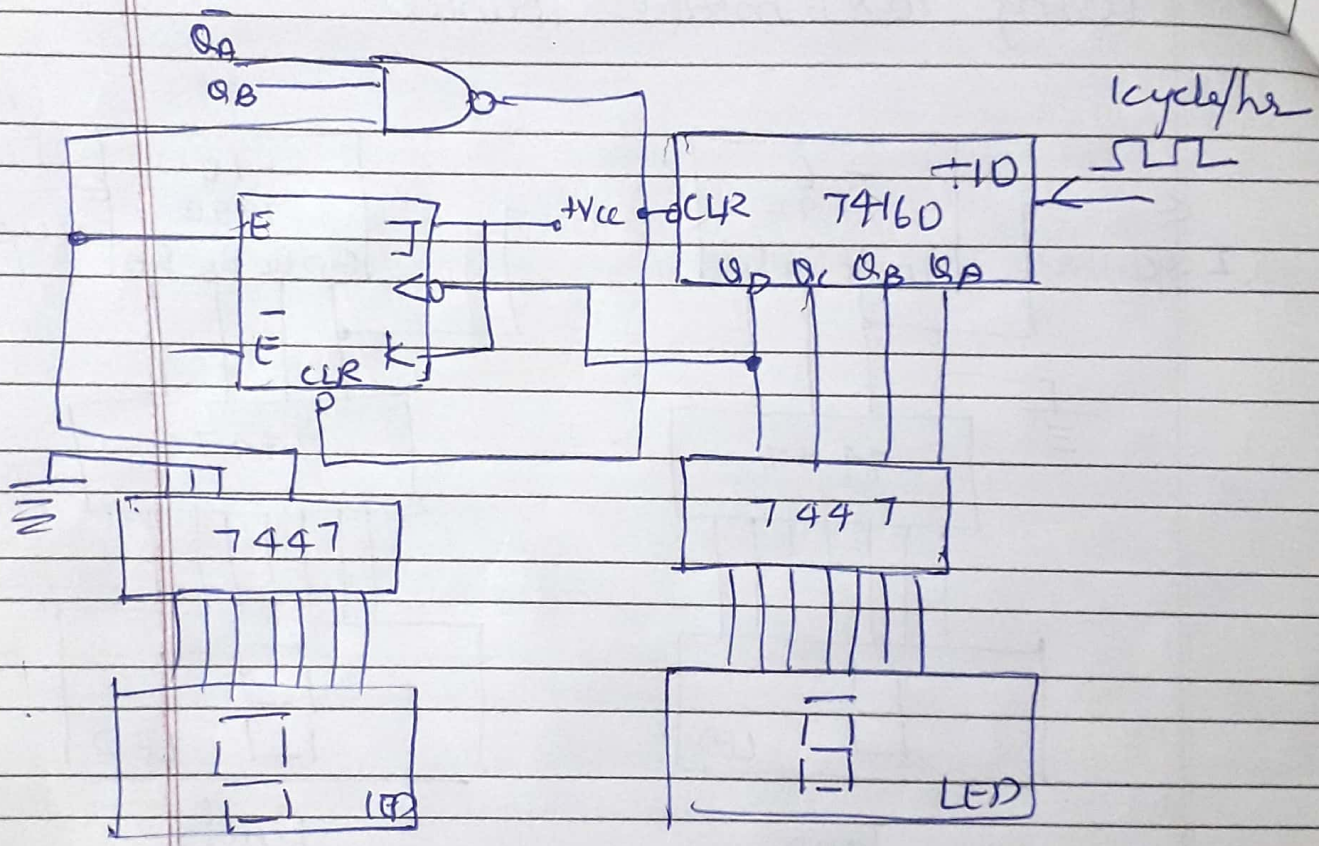
The last counter changes state once each 60 minutes (once each hour) ∴ divide-by-12 counter, helps to display the correct hour.

Design of seconds and minutes counter using 10 × 6 mod-60 counter



Both 7492 and 7490 count in straight 8421 binary & 7447 decoder-drivers to drive 7-segment indicators.

Design of an hour counter



Tens

Units

	Q_B	Q_A
10	0	0
11	0	1
12	1	0