

Delay Routine (Delay Loop)

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1) What is the delay produced by the following delay program, if the frequency of MP is 5MHz?

MOV BL, OFFH
 BACK: DEC BL
 JNZ BACK
 RET

FF \Rightarrow 255 in decimal
 38 300 (hex)
 2048 sat
 T3A

Instructions	T States / instruction	Total T States
MOV BL, OFFH	4	4
DEC BL	2	2
JNZ BACK	16	$(16+2) = 18 \times 255 = 4590$
RET	8	$\frac{4590}{12} = 382.5$
		$\text{Total} = 4602 \text{ T States}$

$$\text{Delay} = \frac{\text{Total T States}}{\text{Frequency}} = \frac{4602}{5 \text{ MHz}} = \frac{4602}{5 \times 10^6} = 0.0009204$$

$$= \frac{0.9204 \times 10^{-3}}{81} = 0.9204 \text{ ms}$$

In the above delay program, 8 bit register BL

Used so maximum value that can be stored is FF.

maximum delay that can be obtained using 8 bit register is 0.9204 ms.

2) Write a ALP to generate a delay of 0.5ms for 8086 UP that runs at 5MHz frequency

Soln
Assume x is the value to be loaded to an 8 bit register, then the delay routine is

DELAY PROC	T States/instn	
MOV BL, x	4	total T States
BACK: DEC BL	2	total 4t
jmp BACK	16 }	(16+2)*x
RET	8	

DELAY ENDP

delay = $\frac{\text{Total T States}}{\text{Frequency}}$

$$0.5\text{ms} = \frac{12 + 18x}{5\text{MHz}}$$

$$0.5\text{ms} = \frac{12 + 18x}{5 \times 10^6}$$

$$0.5 \times 10^{-3} = \frac{12 + 18x}{5 \times 10^6}$$

$$12 + 18x = (0.5 \times 10^{-3})(5 \times 10^6)$$

$$x = \frac{(0.5 \times 10^{-3})(5 \times 10^6) - 12}{18}$$

$$0.0005 \times 5000000 - 12$$

$$= \frac{2488}{18} = 138 = 8AH$$

$$\boxed{x = 8AH}$$

3) Write an ALP to generate a delay of 100ms
for 8086 CPU that runs at 5MHz frequency

$$0.5 \text{ ms} = 138$$

$$1 \text{ ms} = 138 \times 2 = 276$$

$$10 \text{ ms} = 2760$$

$$100 \text{ ms} = 27600$$

Point

As we have seen in Problem 1

that, Using 8 bit register we can

Generate a delay of maximum 0.9204 ms. So to generate a delay higher than this requires 16 bit register.

∴ Assume x is the 16 bit value to be loaded to 16 bit register, the delay routine is as follows

<u>Instructions</u>	<u>T States/instr</u>	<u>Total T States</u>
MOV BX, x	4	4
BACK: DEC BX	2	
JNZ BACK	16	$(16+2)x^8$
RET		

$$\text{delay} = \frac{\text{Total T States}}{\text{Frequency}}$$

$$100 \text{ ms} = \frac{12 + 18x}{\frac{5 \times 10^6}{8}}$$

$$100 \times 10^{-3} = \frac{12 + 18x}{5 \times 10^6}$$

$$(100 \times 10^{-3}) (5 \times 10^6) = 12 + 18x$$

$$\therefore x = \frac{(100 \times 10^{-3}) (5 \times 10^6) - 12}{18} =$$

$$X = \frac{(0.1) * (5000000) - 12}{18} = 27,777$$

$$X = 27,777 \text{ or } \underline{\underline{6C81H}}$$

delay routine to generate 100ms in 8086 that runs on 5MHz frequency

Delay PROC

MOV BX, 6C81H

BACK: DEC BX

JNZ BACK

RET

Delay EndP

endp T wait . endp wait T

4) Write a program to generate a delay of 0.2 sec in 8086 UP that runs at 5MHz frequency

MOV BX, X

$$4 \text{ states} \times 4 = 16$$

BACK: Dec BX

$$2 \text{ states}$$

JNZ BACK

$$16 + 2 = 18$$

RET

$$8 \text{ states}$$

$$\text{Total} = 12 + 18 \times T \text{ states}$$

delay = Total T states

$$8814.4 = \frac{(18)(T)}{5000000} \times 12 + 18 \times T$$

$$8814.4 = (18)(T) \times (5000000)$$

$$8814.4 = 90000000(T)$$

$$0.2 \text{ sec} = \frac{12 + 18x}{5 \text{ MHz}}$$

$$0.2 \text{ sec} = \frac{12 + 18x}{5 \times 10^6} \quad \text{MAP 283} = \text{MAP 136}$$

$$(0.2) * (5 * 10^6) - 12$$

$$x = \frac{1}{18}$$

$$x = 55,555 \quad \text{or} \quad D_{903H}$$

$$\begin{array}{r} 16 \longdiv{55555} \\ \hline 3472 - 3 \\ \hline 217 - 0 \\ \hline \end{array}$$

∴ delay you're

∴ delay routine
call to wait at beginning of message (i) 35113 — 9
At Delay proc

MOV BX, D903H

BACK: DEC BX

fruz BACK : . 23A S.0 di

P R T

Delay EndP.9001 Upgrade CANNLIC

5) What is the maximum delay produced if $BX = R1; FFFFFFFF$

running on 8086 MP operating at 5MHz frequency

Mov	BX, FFFFH	4	{ d1	Lx)A8	SUB
cx; DEC BX		2	{ s	4	XA > 30
JNZ BACK		16	} - d1	18 * FFFF = 18 * 65535	18 * 65535
RET		8	8	8	T38

$$\text{Delay} = \frac{\text{Total } T \text{ States}}{\text{Frequency}} = \frac{1179642}{5 \times 10^6} = \frac{1179642}{5000000} = 0.2359 \text{ sec}$$

$$\boxed{\text{Delay} = 0.2359 \text{ sec}}$$

Or

$$\text{Delay} = 235.9 \times 10^{-3}$$

$$\boxed{\text{Delay} = 235.9 \text{ ms}}$$

\therefore The maximum delay that can be obtained with 16 bit register is 0.2 sec

6) Write a program to generate a delay of 1 sec.

Soln:- Maximum delay obtained by 16 bit register is 0.2 sec. \therefore To generate delay of 1 sec, we require nested loops.

MOV AX, X
AGAIN: MOV BX, FFFF
BACK: DEC BX
JNZ BACK
DEC AX
JNZ AGAIN
RET

delay = $4 + (2^2 + 1.8 \times 65,535) \times 8 \times 10^6$

$$\text{delay} = 4 + (2^2 + 1.8 \times 65,535) \times 8 \times 10^6$$

$$= 1 \text{ Sec} = \frac{4 + 22x + 1179630x + 8}{5000000}$$

$$5000000 = 12 + 1179652x + 8$$

$$5000000 = 20 + 1179652x$$

$$x = \frac{5000000 - 20}{1179652} =$$

$$x = 4.238 \approx 5$$

\therefore delay routine to generate 1 Sec is
~~Delay PROC~~ \rightarrow MOV AX, 15

gain: MOV BX, FFFF $\frac{3 + 0.238711 + 1}{8 - 8(31 + 0.238711 + 1) + 1} =$

JACK: DEC BX

JNZ BACK

DEC AX

JNZ AGAIN

RET

Delay EndP

$\frac{\text{Blanks} + 1000T}{\text{Program}} = 4000b$

$\frac{31 - (0000002)}{0000002} = 300000$

$\frac{31 - (0000002)(0002)}{0000002} = *$

7) Write a delay routine to generate a delay of

10 minutes $\frac{600000}{60} = 10000$ $\frac{10000}{1000} = 10$

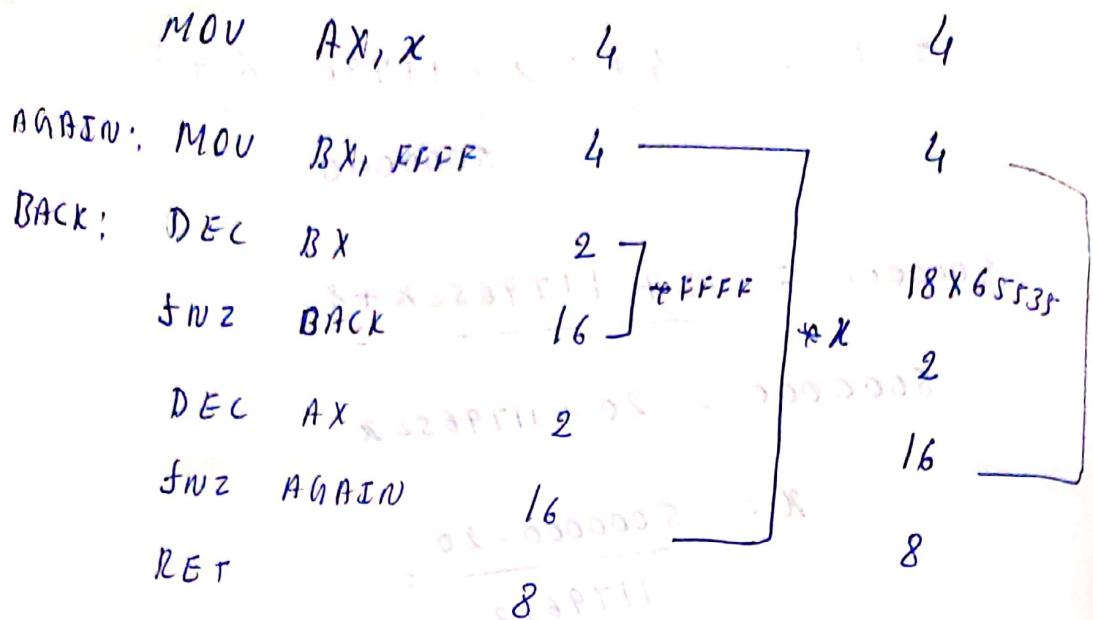
\therefore SOLN $10 \text{ minutes} = 10 \times 60 \text{ sec} = 600 \text{ sec}$

\therefore maximum delay with 16 bits loaded to 16 bit register

is 0.2 sec.

HASP XA 0000

\therefore required number of loops = $\frac{600000}{200000} = 30$



$$T = 38.5 \times K$$

\therefore Total T States

$$= 4 + (22 + 18 \times 65535)K + 8$$

delay = $\frac{\text{Total T States}}{\text{Frequency}}$

$$600 \text{ sec} = \frac{12 + 1179652K}{5000000}$$

$$K = \frac{(600)(5000000) - 12}{1179652} = 2543$$

$$K = 2543 \text{ or } 0909EFH$$

$$\begin{array}{r} 2543 \\ 16 \end{array}$$

9-E

\therefore Delay routine to generate 600 sec or 10 minutes

IS delay proc of assembly language

MOV AX, 9EFH

AGAIN: MOV BX, FFFFH

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BACK: DEC BX
      JNZ BACK
      DEC AX
      JNZ AGAIN
      RET
Delay Endp

```

8) Write a delay routine to calculate a delay of 4 sec for 8086 MP that operates at 10MHz frequency

Soln \therefore 4 Sec means requires nested loop \Rightarrow 0.2 Sec

```

MOV AX, X
AGAIN: MOU BX, FFFF
BACK: DEC BX
      JNZ BACK
      DEC AX
      JNZ AGAIN
      RET

```

\therefore Total T States = $4 + (2^2 + (18 * 65535)) \times 8$

delay = $\frac{\text{Total T States}}{\text{frequency}}$

$$4 \text{ sec} = 228281 \text{ T states} \therefore$$

$\frac{228281}{10 \text{ MHz}}$

$16/34$
 $2-2$

$$X = \frac{4 * 10^6 - 12}{1179652} = \frac{4 * 1000000 - 12}{1179652} = 33.9 \approx 34 = 22H$$

∴ delay routine to generate 4 sec delay

Delay proc

MOV AX, 22H

AGAIN: MOV BX, FFFF

BACK! DEC BX

turn BACK

DEC AX

JNZ AGAIN

RET

Delay End.p

9) Write a delay procedure to generate a delay of

1 Dec for 8086 MP working at 10MHz

Soln

1 Sec \Rightarrow nested loop
 MOU AX, X 8
 AGAIN: MOU BX, FFFF 16
 BACK: DEC BX 8
 fnz BACK 16] + FFFF
 $8 + ((AX + 8) + 16) + 1 = \text{width T width T width T}$
 fnz AGAIN 16
 RET 8

$$\therefore \text{Total T States} = 4 + (22 + 18 * 65535)x + 8$$

$$= 12 + 1179652x$$

$$\text{delay} = \frac{\text{Total T States}}{\text{Frequency}}$$

$$1 \text{ Sec} = \frac{12 + 1179652x}{10 * 10^6}$$

$$x = \frac{1000000 - 12}{1179652} = 8.4 \approx 8.5$$

∴ Delay routine needs to wait
for 8.5 sec to generate 1 sec

(Subroutine) **DELAY PROC**

MOV AX, 9
AGAIN: MOV BX, FFFF

BACK: DEC BX

JNZ BACK

DEC AX

JNZ AGAIN

RET

ENDP **DELAY END**

⇒ In assembly code delay is

converted to loops

⇒ Assembly H is now used to

convert to loops

and loops need to remove first 10 loops

and then it depends on the maximum value

and it depends on how many loops need to

remove A and B = n² - 10² = n² - 100

Instruction Template Radeshwari, B.S
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A 8086 Assembler converts an 8086 language program into machine codes. Consider the instruction MOV CX, Source. The source can be any of the 8 16-bit registers (AX, BX, CX, DX, SP, BP, SI + DI), Any of the memory location specified by any of 24 addressing modes ([BX], [SI], [DI], [BX] + [SI], [BX] + [DI], [BP] + [SI], [BP] + [DI], [BX] + [SI] + d₈, [BX] + [DI] + d₈, etc.). Therefore there are 32 ways to specify source operand in an instruction with CX as destination. Similarly there are 32 ways to specify destination operand in an instruction with CX as source. Therefore there are 64 different codes for mov instruction with CX register as a source or destination.

64 different codes with CL register as a source or destination.

64 different codes with CH register as a source or destination.

Because of large number of possible codes for an 8086 instruction, it is impossible to take it from the table, instead assembler uses a template for each basic instruction type & fill in the bits to generate

Machine Codes. The instruction template for an 8086 processor is as shown below

Case I : Instruction template for an instruction, which moves data from register to register, register to memory & memory to register.			
Byte 1	Byte 2	Byte 3	Byte 4
1 0 0 0 1 0	D/W MOD Reg R/M	Low displacement	High displacement

- * The upper 6 bits are opcode.
- * D bit in the first byte indicates direction, whether the data is being moved to the register or data is being moved from the register. If the data is being moved to the register, then $D=1$. If the data is being moved from the register, then $D=0$.
- * W bit in the first byte indicates whether word data or byte data

for byte movement, $W=0$
for word movement, $W=1$

- * 3, 4, + 5th bits of the second byte specifies the register. 2 Mod bit & 3 R/M bits of the second byte specifies the addressing modes of the other operand.

The following table shows MOD & R/M for each of the possible 32 addressing modes.

R/M \ MOD	00	01	10	11
000	$[BX] + [SI]$	$[BX] + [SI] + d_8$	$[BX] + [SI] + d_{16}$	$[BX] + [SI] + d_{16}$
001	$[BX] + [DI]$	$[BX] + [DI] + d_8$	$[BX] + [DI] + d_{16}$	$[BX] + [DI] + d_{16}$
010	$[BP] + [SI]$	$[BP] + [SI] + d_8$	$[BP] + [SI] + d_{16}$	$[BP] + [SI] + d_{16}$
011	$[BP] + [DI]$	$[BP] + [DI] + d_8$	$[BP] + [DI] + d_{16}$	$[BP] + [DI] + d_{16}$
100	$[SI]$	$[SI] + d_8$	$[SI] + d_{16}$	$[SI] + d_{16}$
101	$[DI]$	$[DI] + d_8$	$[DI] + d_{16}$	$[DI] + d_{16}$
110	(Direct address) d_{16}	$[BP] + d_8$	$[BP] + d_{16}$	$[BP] + d_{16}$
111	$[BX]$	$[BX] + d_8$	$[BX] + d_{16}$	$[BX] + d_{16}$

d_8 :- 8 bit displacement

d_{16} :- 16 bit displacement

$d = 8$

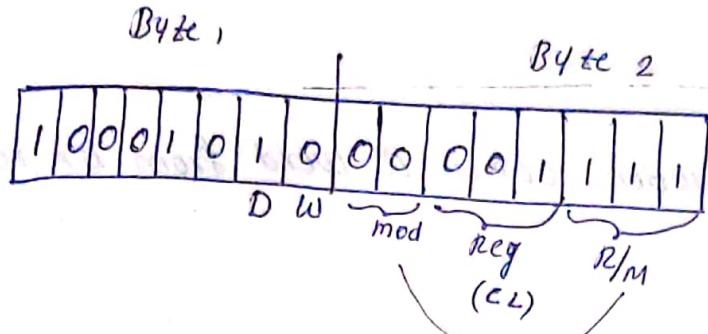
Segment Reg	CODE
CS	01
DS	11
ES	00
SS	10

Eg:

Generate opcode for the following instruction

MOV CL, [BX]

This instruction copies a byte from the location whose effective address is find BX reg into CL reg



$$[BX] \Rightarrow \text{mod} = 00$$

10001010 00000111

Code for MOV CL, [BX] is 8A0F1H (1388)

②

MOV 43H [SI], DH

8 bit displacement

10001000

01 110 100
mod R/M R/M
DH

8874431H

This instn copies a byte from 10001000 register in memory location pointed by SI with displacement 43H

0100 0011

4 3

displacement

③

MOV CX, [437AH]

This instruction copies Content

into CX register

10010001

of two memory locations

10001011 00 001 110
mod reg R/M

01111010 01000011

7A

43

$\Rightarrow 8B0E7A431H$

4) $MOV SP, BX$

This instruction copies a word from BX register to SP register.

Since this is register to register operation, 2 registers are involved in the instruction. The move operation can be either to SP or from BX . When it is to SP , $D=1$. When it is from BX , $D=0$.

Case (i) To SP

When it is to SP , $D=1$

$MOV D \text{ with } 10001011$
mod Reg R/M
 $= EBE3H$

Case (ii)

from BX

When it from BX , $D=0$

10001001

mod Reg R/M
 $= 89DC H$

(5)

$MOV CS:[BX], DL$

This instruction copies ~~one byte~~ from DL register into memory location in Code Segment.

The Segment register CS in an instruction

is called as Segment override prefix. The Segment override prefix has the format

001 XX110

In place two bit code for segment registers in place of XX.

∴ The Segment override prefix byte for CS register is

Code for CS	001	01110	= 2EH	111100011
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Segment override prefix is put in memory before the m/c code of an instruction.

10001000 DW 00 H3E = 01111 100
mod Reg R/M

⇒ 2E 8814H

Template to move immediate data to register

Byte 1	Byte 2	Byte 3
1011 W	H3E	

Eg: ① mov AX, 1234H

This instruction moves immediate data 1234 to Ax register.

1011 1000 upper byte first
W AX 3 4 lower byte next
0011 0100 0001 0010 ⇒ B83412H

Eg. ② MOV CL, 0F2H

10110 w 001 1111 0010 \Rightarrow B1F2H

III. Template to move immediate data to memory location

Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
1100011.W	mod	000	R/M	011	

Eg. MOV DS: F246H [BP], 1234H

Segment override prefix for DS register is

001 11110 = 3EH 00010001
DS code 11000000 00010001

for inst

11000111 $\stackrel{w}{\text{mod}}$ 10 000-110 0100 0110 11110010
 R/M 4 6 F 2
 00110100 00010010
 3 4 1 2

\Rightarrow 3E C7 86 46 F2 34 12 H

IV. Template to move data to accumulator using direct addressing

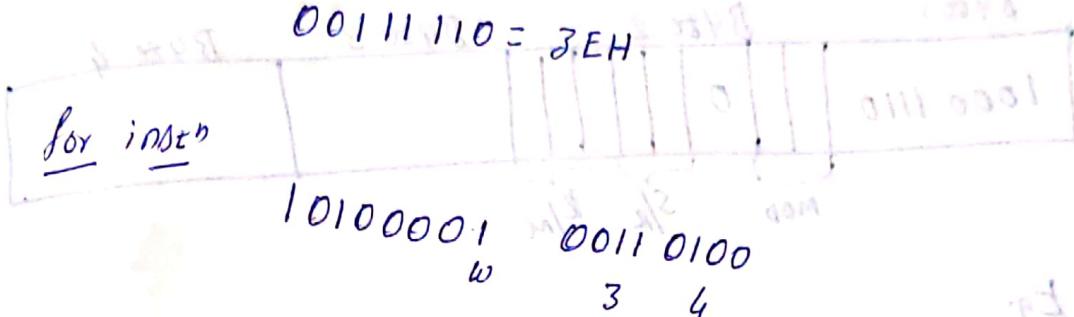
Byte 1	Byte 2	Byte 3
1010000W		

Eg. MOV AX, DS: 34

This instruction moves the word from the location 0034 in data segment to AX register.

Segment override prefix for DS register is

0011110 = 3EH.

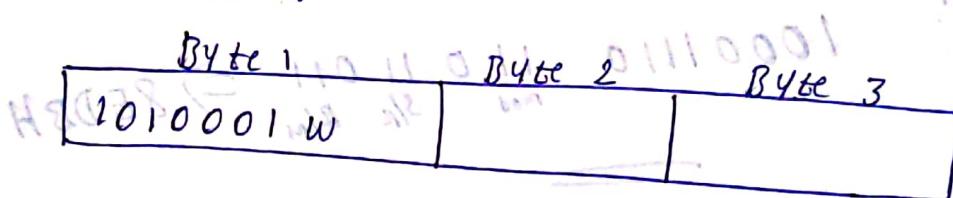


3E A1 34

Segment
Override
Prefix

10.2A WM ①

V Template to move data from accumulator to using direct addressing



Eg:

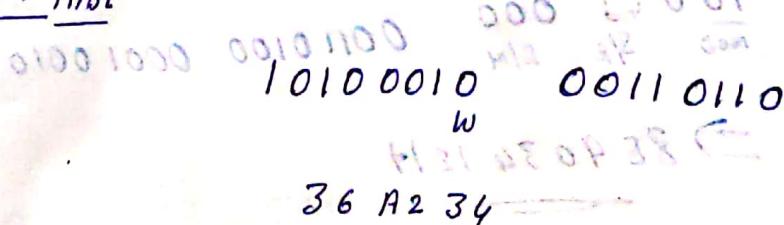
MOV SS:34H, AL

This instruction moves the byte from AL register to location 34H in the Stack Segment.

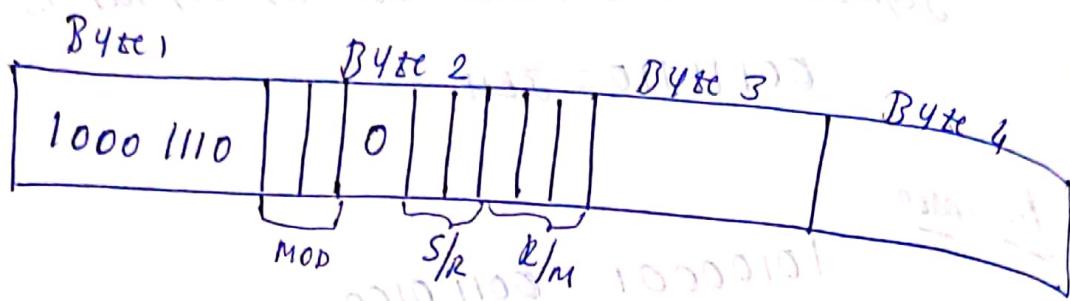
Segment and override prefix for stack segment is

segment SS + 16 00110110 \Rightarrow 36

for inst^b



VI Template to move data to segment register from register or memory location

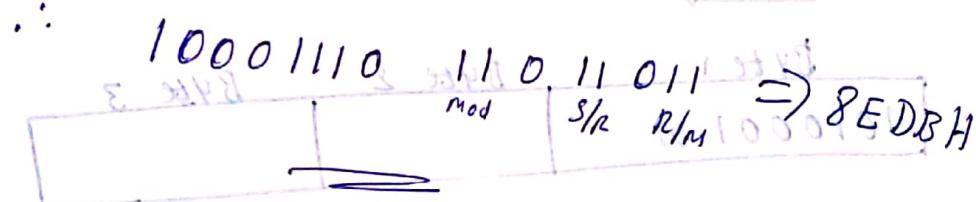


Eg:-

① $MOV DS, BX$

This instruction moves data from BX register to DS register.

For DS register, Segment register code is 1.

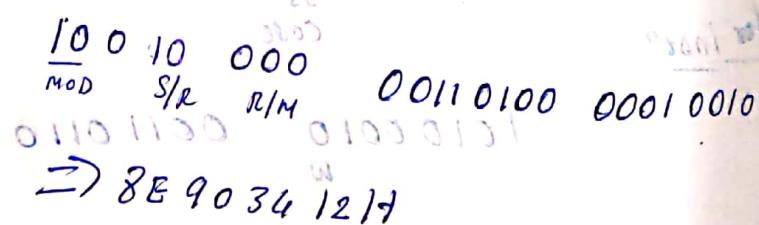


②

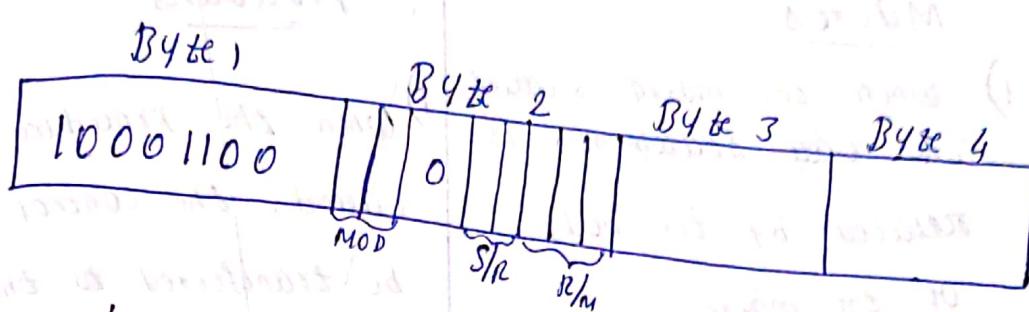
$MOV SS, 1234H [BX + SI]$

This instruction moves to SS from location, whose effective address is the sum of 16 bit displacement 1234 & content of BX & SI register.

10001110



VII Template to move data from segment register to register or memory location



Eg: ① $MOV BX, DS$

10001100

11 0 11 011 \Rightarrow 8C DBH

for BX reg

② $MOV 1234H[BX][SI], SS$

10001100

10010000

0011 0100 0001 0010 (3)

\Rightarrow 8C 90 34 12 H

NOTE

Templates

① Register to Register

Register to memory

Memory to register

② Immediate data to register

③ Immediate data to memory

④ To move data to accumulator

⑤ To move data from accumulator

⑥ To move data to segment reg from reg/memory

⑦ To move data from segment reg to reg/memory

Difference b/w Macros + Procedures

Macros

- 1) When the macro is called, the call statement is replaced by the body of the macro.
- 2) More memory is required, because code will be expanded at the place of call.
- 3) Stack is not required.
- 4) Speed of execution of the program increases.
- 5) Macros are called as open subroutine, because macro is replaced at the place of call.
- 6) Macro is replaced during assembly time.

Procedures

- 1) When the procedure is called, the control will be transferred to the beginning of the procedure.
- 2) Less memory is required, because code will not be expanded at the place of call, instead control will be transferred to procedure block.
- 3) Stack is required to store the return address of the program.
- 4) Speed of execution of the program is less, because control has to be transferred to/from procedure.
- 5) Procedures are called as closed subroutine.
- 6) Control is transferred to procedure during run time.

7) Macro is defined using
directives

MACRO & ENDM

for defining its code (instructions)

8) Eg: Disp Macro msg
MOV AH, 09H
LEA DX, msg

INT 21H

EndM

7) Procedures

are defined
Using the directives
& ENDP

8) Eg: Disp Proc

LEA DX, msg
MOV AH, 09

INT 21H
Disp
ENDP

a number of lines (5)

newline character