Interrupts

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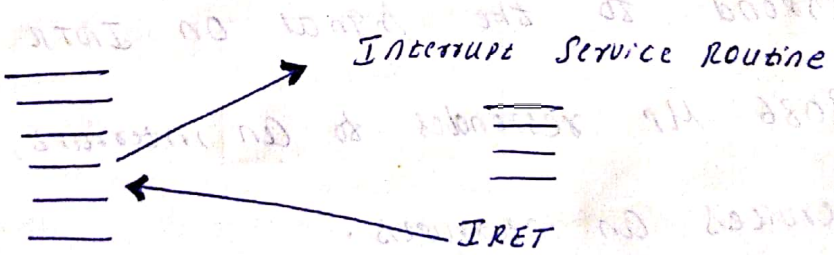
An interrupt is a signal that is given by some external device or due to the execution of some instructions within the program that informs the CPU to temporarily halt its current activities & to transfer the control to the special routine called as Interrupt Service Routine (ISR) or Interrupt Handler to service an interrupt. An IRET instruction at the end of the ISR returns the control back to interrupted program & execution resumes. The concept of interrupt is as shown below



Based on the source of the interrupt, it is broadly classified into 3 types

1) External Hardware Interrupt
2) Software Interrupt
3) Exception Interrupt

Hardware Interrupt:- If external device applies a signal on INTR or NMI interrupt input pin of 8086 MP, then it is referred to as an hardware interrupt.

Hardware Interrupt
- Maskable Interrupt
- Non maskable Interrupt

Maskable Interrupt:- An external interrupt signal, which can accept or ignore by 8086 processor depending upon the content of interrupt flag (IF) is called as maskable interrupt. This signal is applied on INTR Pin of 8086 processor. If IF=0, then 8086 MP does not respond to the signal on INTR pin. If IF=1, then 8086 MP responds to an interrupt, accepts an interrupt, services an interrupts.

Non maskable Interrupt:- An external interrupt signal, which cannot be ignored by 8086 MP is called as non maskable interrupt. This signal is applied on NMI pin of 8086 processor. The signal on NMI pin is serviced even when all other interrupts are disabled. The content of IF has no effect on signal on NMI pin. The NMI is used to signal

emergencies such as memory failure or power failure etc.

Software Interrupts:- If an interrupt generated by the execution of interrupt instructions is called as Software Interrupt.

for eg:.

INT N ; where N is an interrupt number

INT 21H ; 21H is an interrupt to access DOS Services.

These instructions are used as a regular instructions in the program. Software interrupt instructions are used to call system services.

Exception Interrupt:- Interrupt, which is generated by 8086 processor by the execution of some instructions in the program.

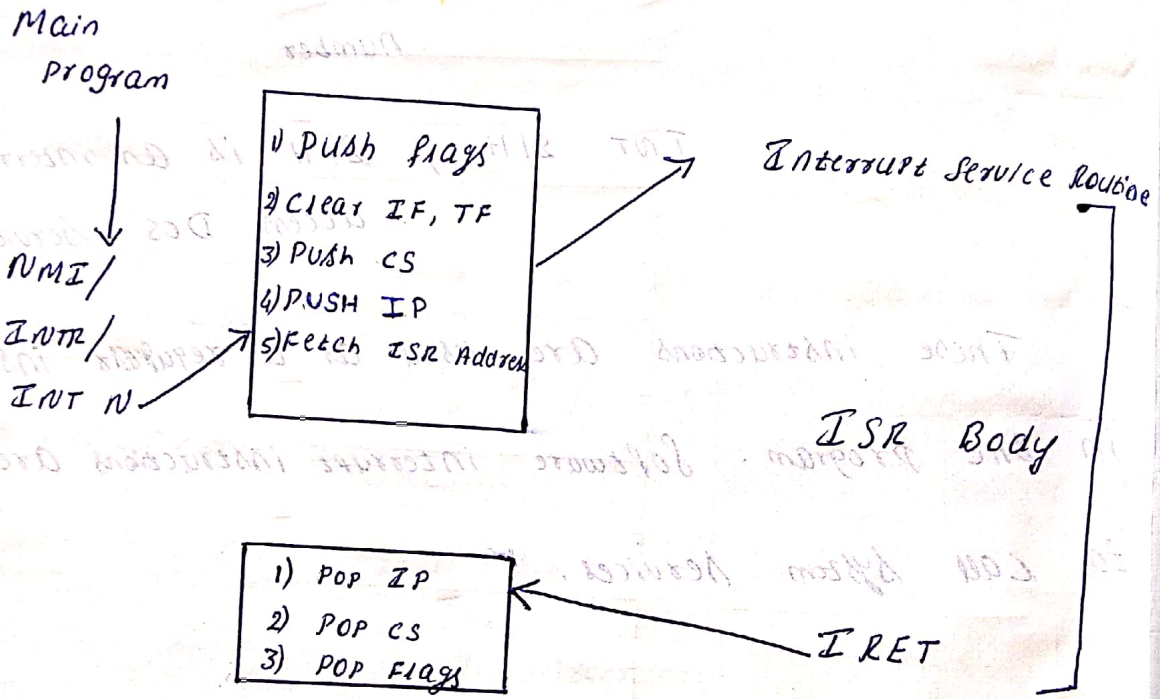
for eg:. ① Divide by zero interrupt; If an operand is divided by 0, then 8086 processor automatically interrupt currently executing program.

② Illegal memory reference ; for eg: MOV AX, [238688]
24 bit address

③ Arithmetic overflow

Interrupt Actions

At the end of each instruction execution, µp checks to see if any interrupts have be requested on INTR pin & NMI pin. If any interrupt have been requested, then processor takes series of actions as shown below



1) Decrements the stack pointer (SP) by 2 & saves flag register content onto the stack

SP ← SP-2 , [SP] ← flags

2) Clears the interrupt flag IF in the flag register to 0 to disable INTR interrupt

IF ← 0

3) Clears the trap flag TF in the flag register to 0 to stop single step execution

TF ← 0

4) Decrements stack pointer SP by 2 & saves CS register content onto the stack (ie, return address)

SP ← SP-2 , [SP] ← CS

5) Decrements stack pointer SP by 2 again & saves instruction pointer IP content onto the stack (ie, return address offset value)

SP ← SP-2, [SP] ← IP

6) Loads the CS register with the base address of ISR (Interrupt Service routine)

CS ← Base address of ISR

7) Loads the IP register with the offset address of ISR within the segment

IP ← offset address of ISR

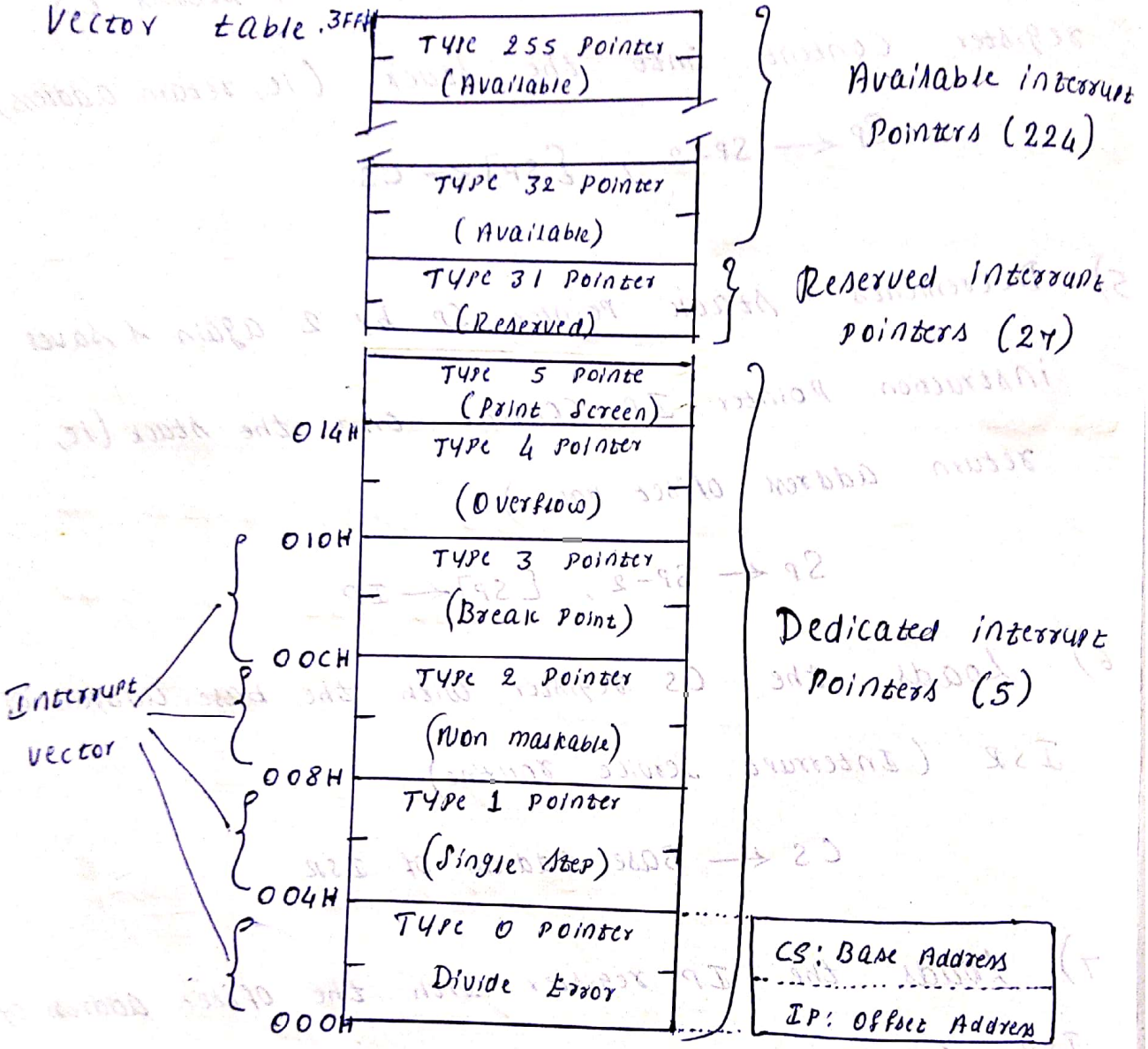
⇒

Interrupt Vector Table (IVT)

8086 processor can recognize 256 different interrupts. The lowest 1024 bytes of memory locations is reserved for a table, which contains base address & offset address of Interrupt Service routine called

as Interrupt vector table (IVT)

The below figure shows interrupt



The address of an ISR stored in interrupt vector table for each interrupt type, which contains 2 bytes CS address & 2 byte IP address is called as Interrupt vector or Interrupt pointer.

INT N, whose ISR address is stored in IVT at the location N*4

for eg. INT 2 ⇒ Address of non maskable

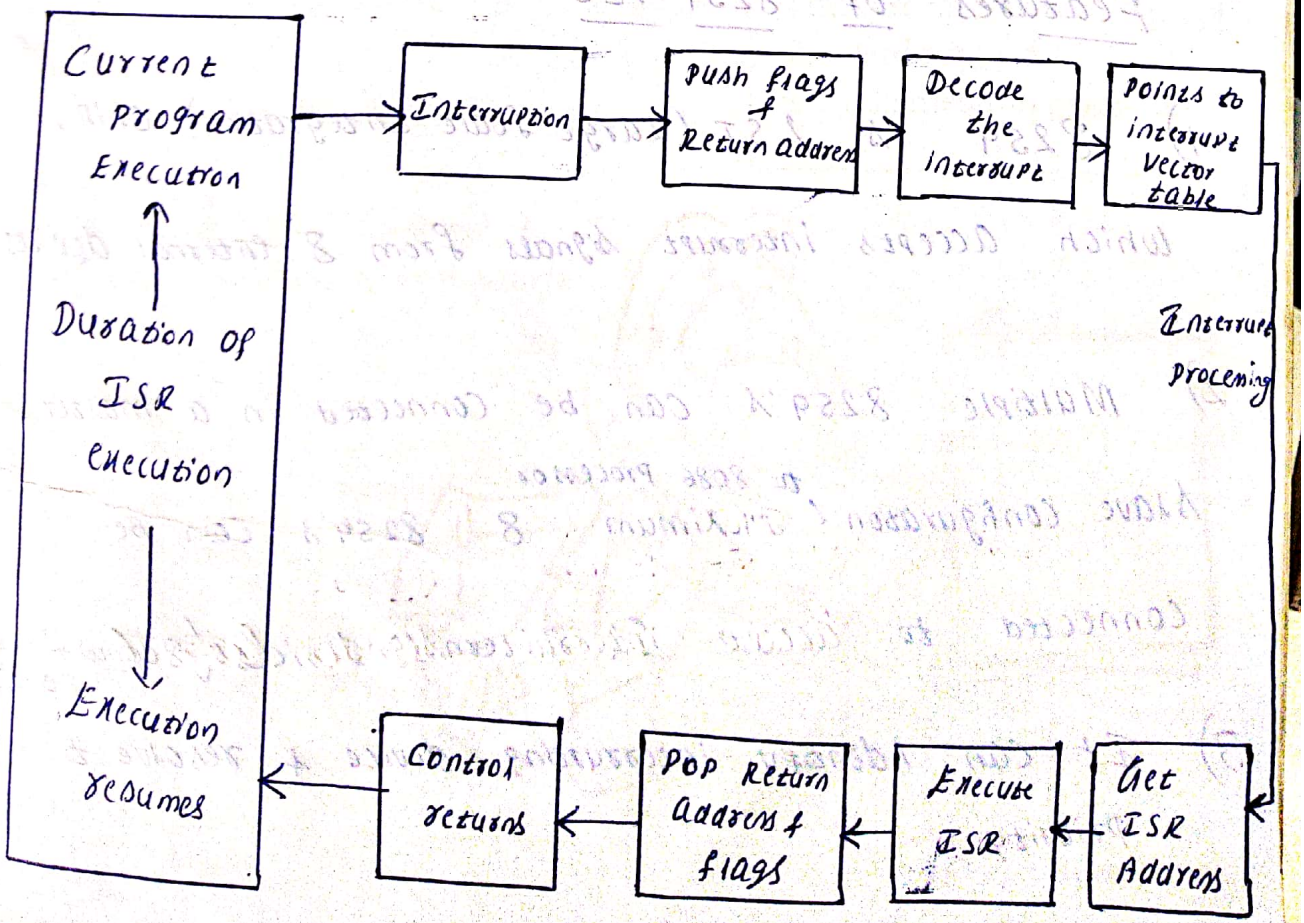
Service routine is stored in the location $2*4=8^{th}$ location of IVT. 0008 & 0009H contains CS value 000AH & 000BH contains IP value.

The lowest 5 types of interrupts are dedicated interrupt dedicated to specific functions like divide by zero, overflow etc

Interrupt from 6 to 31 are reserved by Intel

Interrup from 32 to 255 are available for u/s to use for hardware or software interrupts.

The concept of interrupt servicing by the microprocessor is shown below



8259 Programmable Interrupt Controller (PIC)

In 8086 processor, there is a problem for an interrupt for an different application, because 8086 has only two interrupt pins NMI & INTR pins. If NMI pin is saved for power failure interrupt, that leaves only one INTR pin for all other applications. To overcome this problem, we can have an external device called programmable Interrupt controller (PIC) to funnel the interrupt signals from multiple external device into single interrupt input to 8086 processor.

Features of 8259 PIC

1) 8259 is LSI (Large Scale Integration) chip, which accepts interrupt signals from 8 external devices

2) Multiple 8259's can be connected in a master slave configuration to 8086 processor / maximum 8 8259's can be connected to handle 64 external devices (8 devices * 8 pins each 8259)

3) It can identify interrupting device & resolve their priority