ECE 3300L

California State Polytechnic University, Pomona

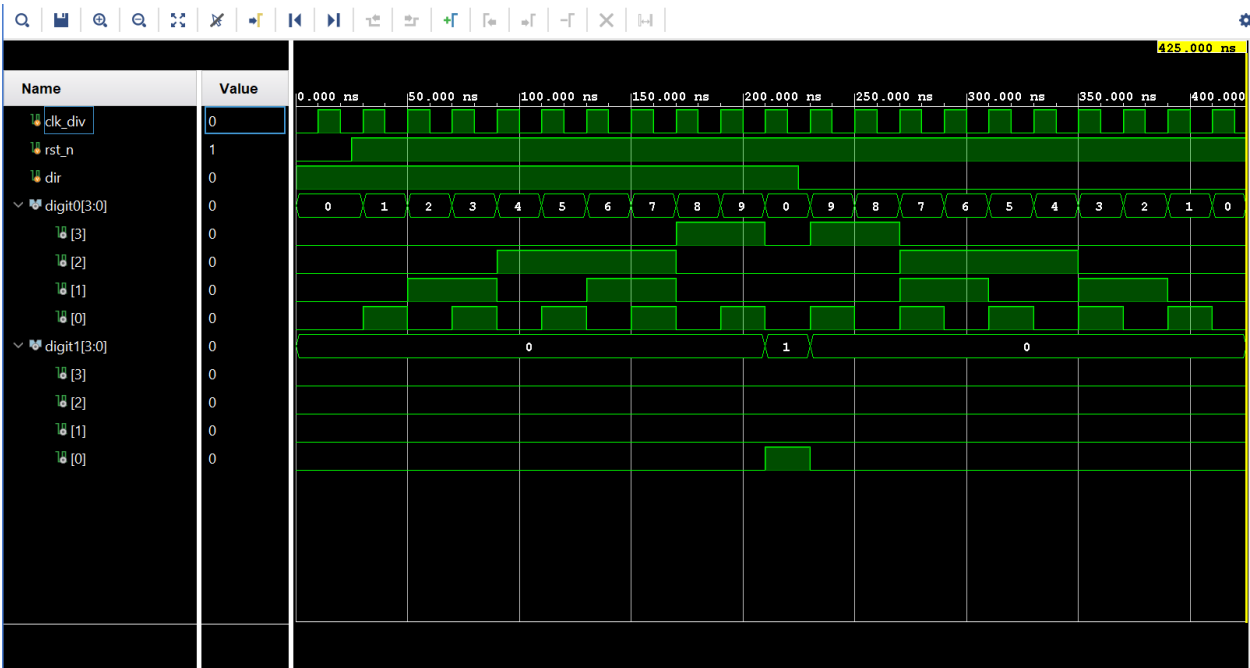# Group G

Nathaniel Garcia and Mikael Parsmyan

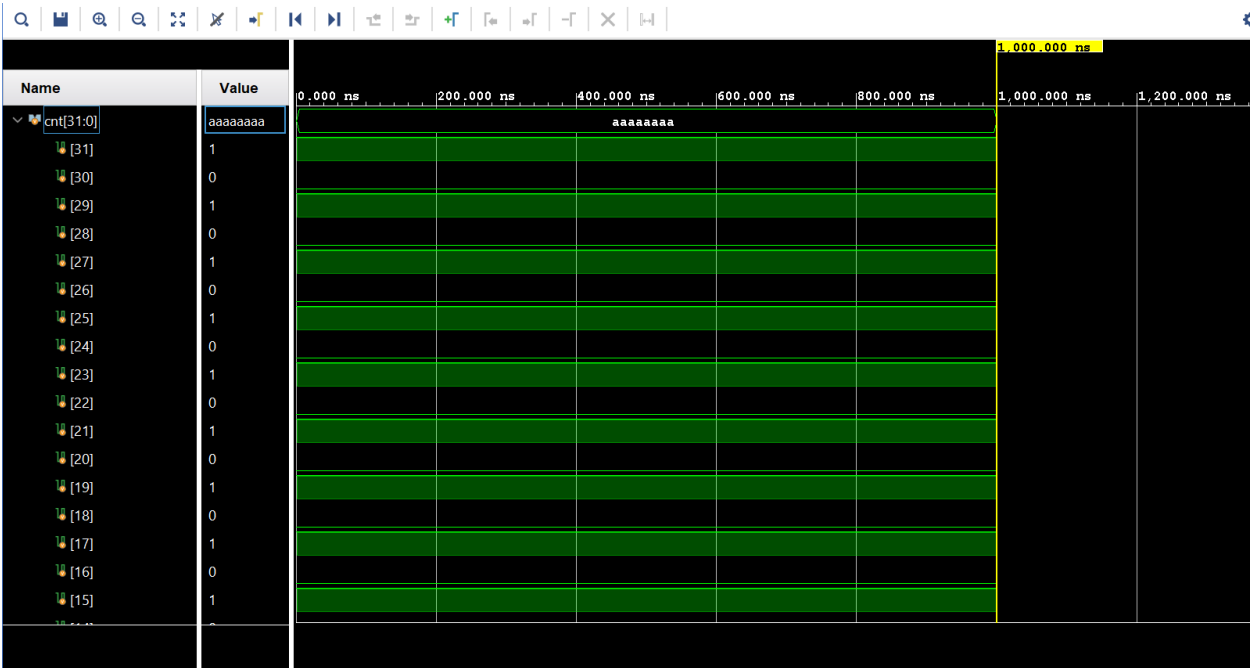# Lab Report #4
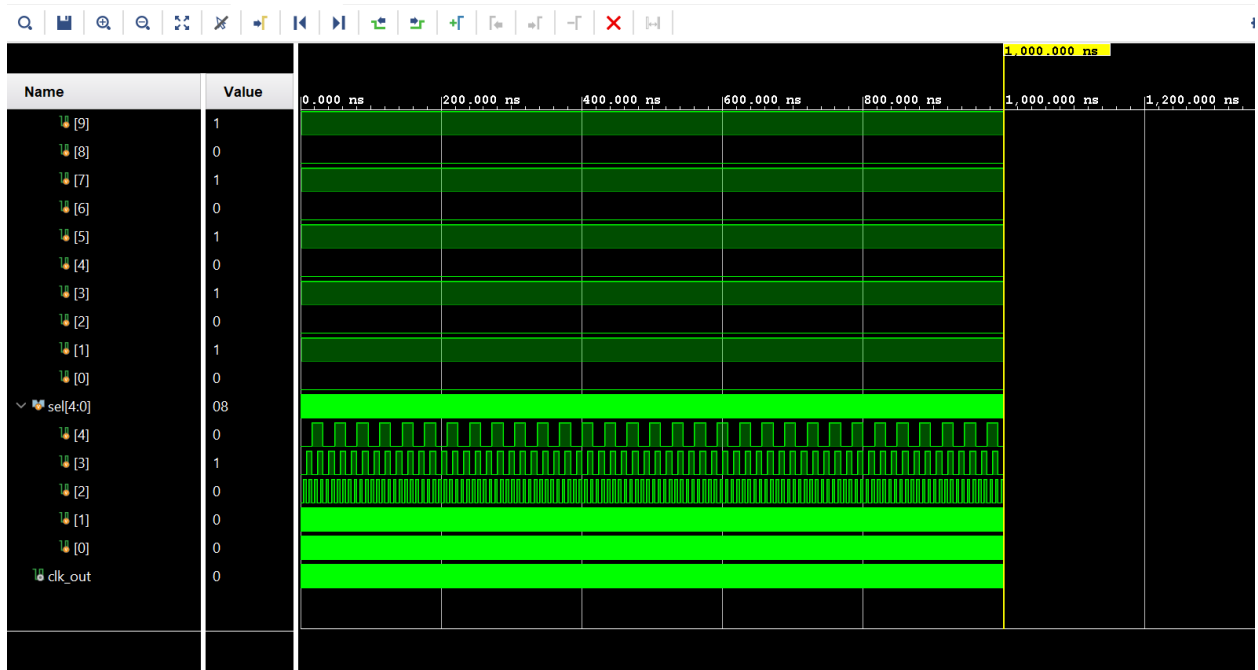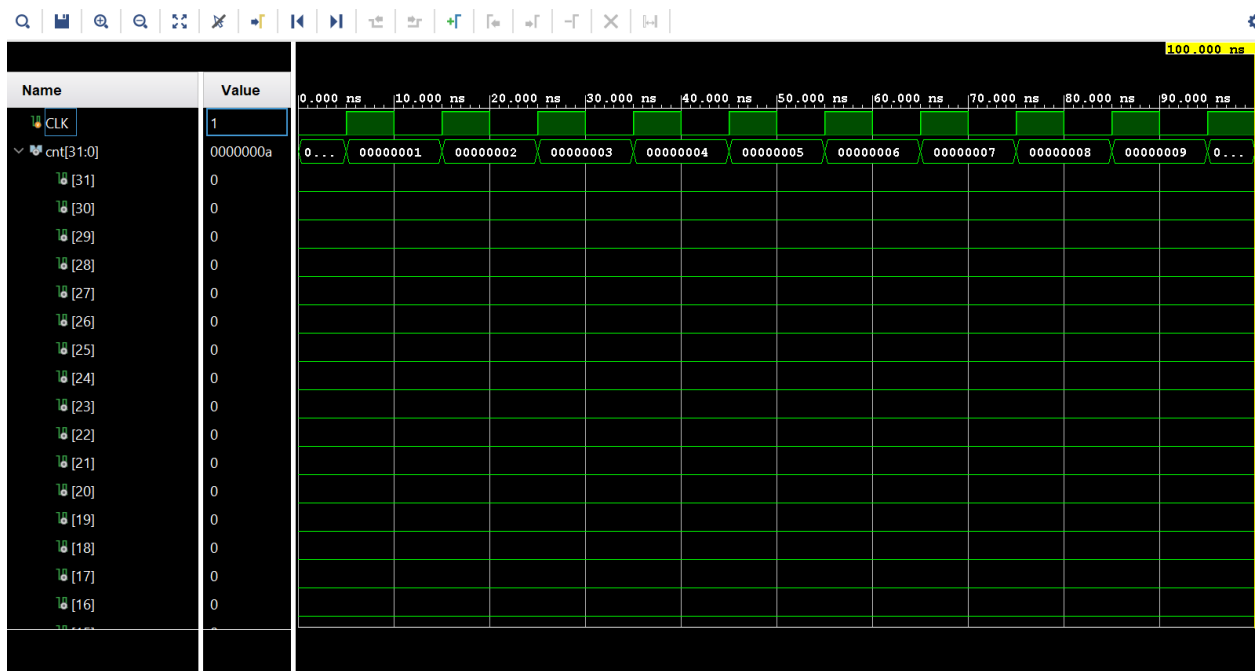
07/10/2025

Top_Lab5:

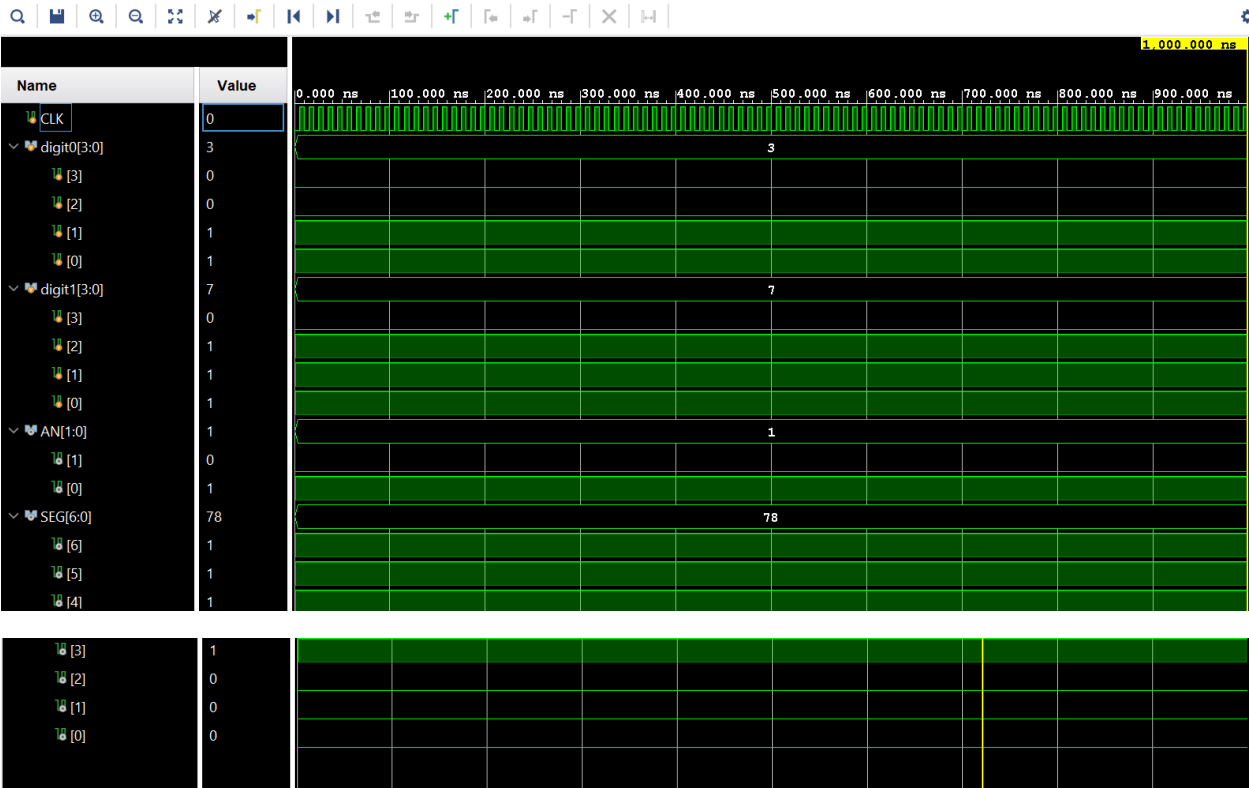## BCD_up_down_counter:
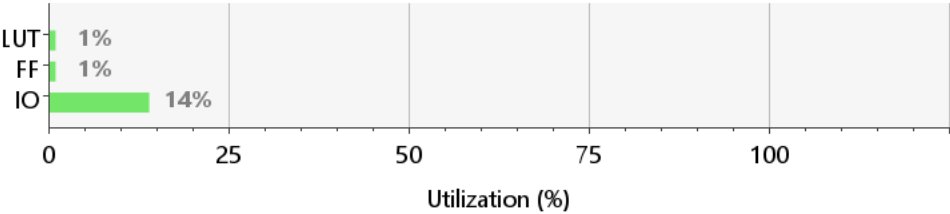

Mux32x1:

Clock_divider:

Seg7_scan:

Hardware Results:

Name		Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
∨ N top_lab5		26	59	4	24	26	30	1
	counter (bcd_up_down_counter)	14	8	0	6	14	0	0
	display (seg7_scan)	2	18	0	6	2	0	0
	div (clock_divider)	10	32	4	12	10	0	0

Summary

Resource	Utilization	Available	Utilization %
LUT	26	63400	0.04
FF	59	126800	0.05
IO	30	210	14.29

LUT 1%
FF 1%
IO 14%

Utilization (%)

Contributions:

Both worked on the report

Nathaniel: Testbench files, Xdc files and Demo

Mikael: Source files, simulation testing