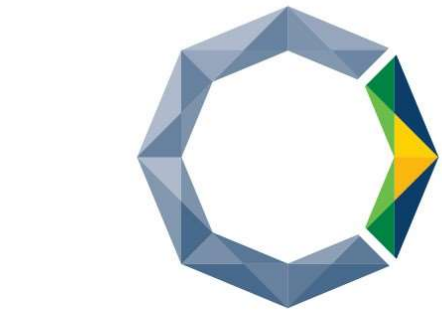

CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #1

Experiment #1

Presented By: Michelle Lau & Edwin Estrada

Presented to Mohamed Aly

June 18th, 2025

Synthesis Screenshot:

The following is our LUT and FF count for our project. The full utilization report has been included in our Github.

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	0	0	0	63400	0.00
LUT as Logic	0	0	0	63400	0.00
LUT as Memory	0	0	0	19000	0.00
Slice Registers	0	0	0	126800	0.00
Register as Flip Flop	0	0	0	126800	0.00
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

Group Video Link: https://youtu.be/G-naOk_Qv2U

Reflections:

In this week's lab, we are introduced to the Vivado Design Suite from AMD/Xilinx and Verilog. We directly connected a 16-bit input bus to a 16-bit output bus. From there, we wrote our constraint file such that the 16-bit input represents the 16 slide switches and the 16-bit output

represents the 16 LED's directly above the switches. By doing this, when sliding a switch up, the LED above it will turn on and stay at that state until the switch is slid back down. It's important to be clear when writing the Verilog program and constraint file to make sure no unknown behavior/error occurs. Overall, lab 1 gives the foundation of FPGA design, from synthetization to generating the bitstream, and describing hardware in Verilog.