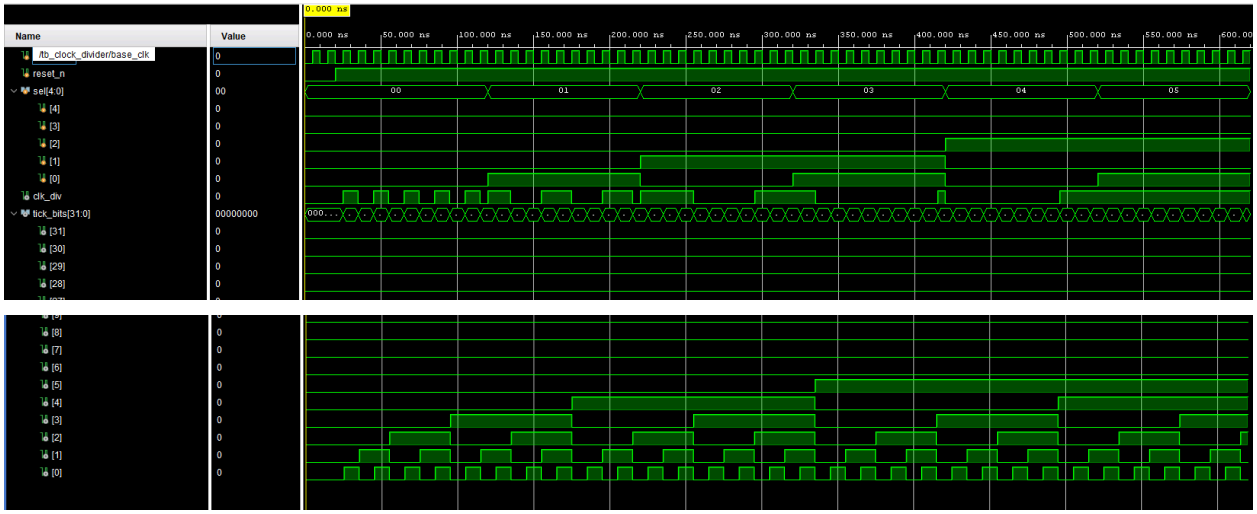
ECE 3300 Lab 6 Group J

Introduction

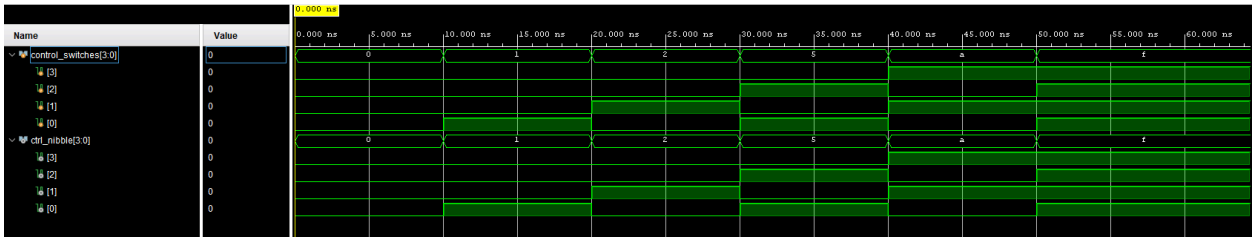
In this experiment, we designed and implemented a complete digital system on the Nexys A7 FPGA board that integrates dual BCD up/down counters, a 4-bit ALU, and a three-digit seven-segment display. The objective was to design independent counters for the units and tens digits, each with separate direction controls (SW7 and SW8), and perform arithmetic operations using an ALU controlled by switches SW5 and SW6. A clock divider module enabled speed control of the counters via SW0–SW4, while BTN0 provided a global reset function. The ALU's 8-bit result and a control nibble formed from the switch settings were displayed using a three-digit seven-segment scan driver, and the raw BCD values of the counters were mirrored on LEDs for debugging. This lab emphasized modular hardware design, clock control, and real-time visual feedback, reinforcing key digital design principles such as arithmetic logic, control signal bundling, and multiplexed display systems on FPGA platforms.

Testbench Waveform

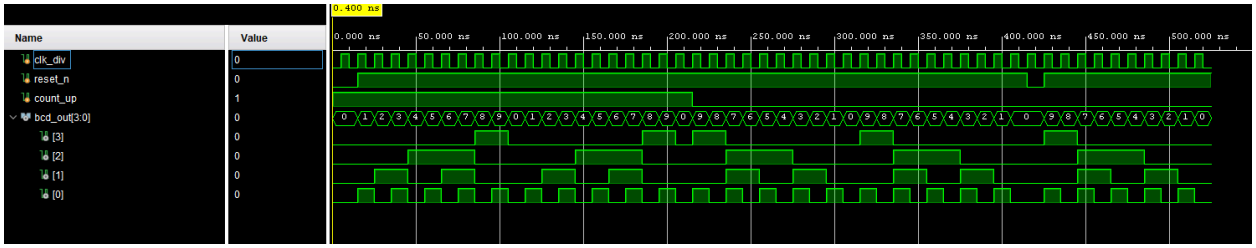
clock_divider_tb



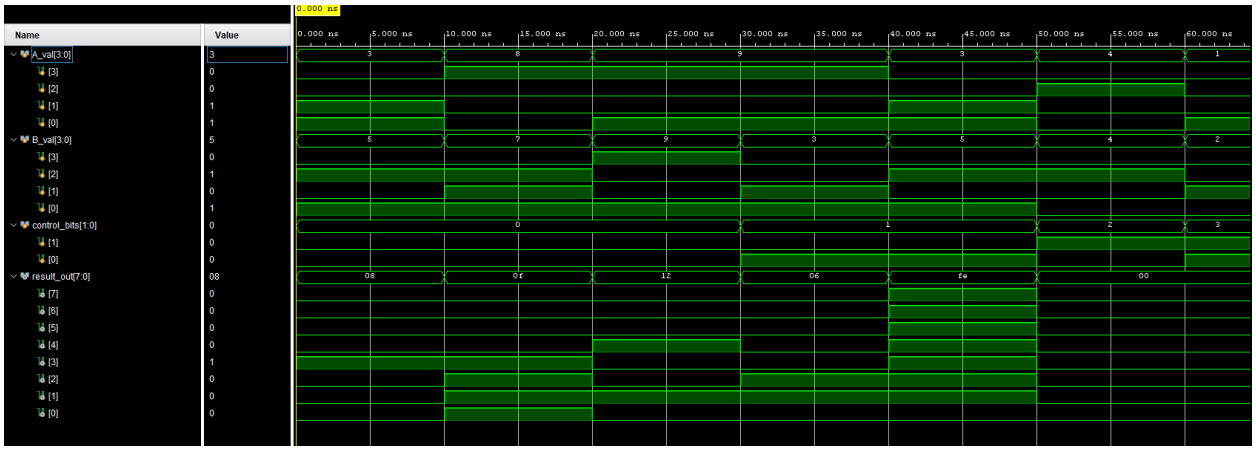
control_decoder_tb



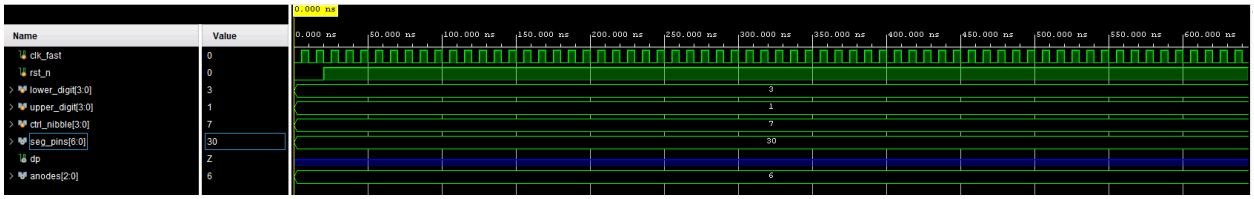
bcd_counter_tb



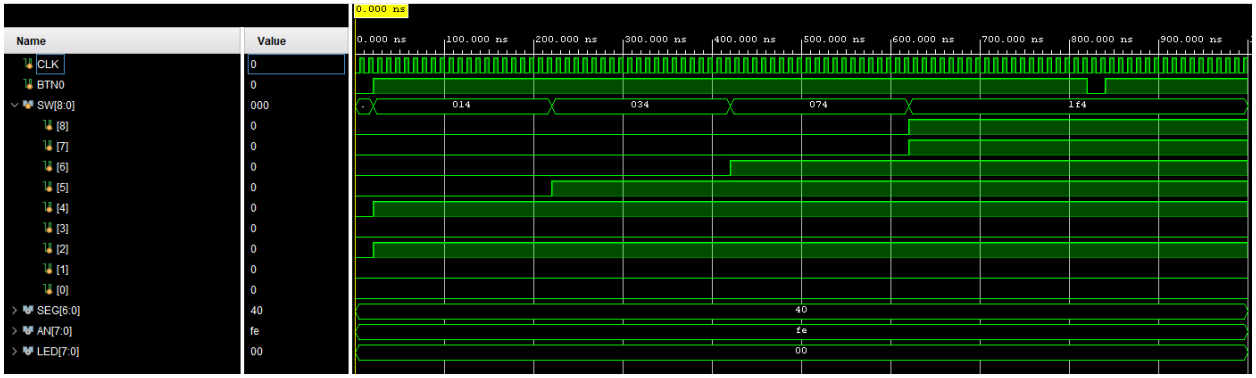
alu_tb



seg7_scan_tb



top_lab6_tb



Group Video Link

https://www.youtube.com/watch?v=VsWrkE1q018

Reflection

This lab highlighted the complexity and value of integrating multiple hardware modules into a cohesive FPGA system. Working with two independent BCD counters introduced challenges in managing separate direction controls and ensuring accurate synchronization between them.

Implementing the ALU required careful handling of 4-bit arithmetic and interpreting control signals to select the correct operation. Displaying both the ALU result and control nibble on a multiplexed seven-segment display added another layer of design consideration, especially in coordinating digit selection and segment encoding. Debugging was made more manageable by visualizing counter outputs through LEDs before verifying the full display output. Additionally, adjusting the clock speed using a switch-controlled clock divider helped reinforce our understanding of clock domain interactions. This lab strengthened our proficiency in Verilog, modular design, and hardware validation, while also enhancing our ability to troubleshoot and fine-tune a system composed of interdependent digital components.

Partner Contribution

Sean Go - code, lab report, video demonstration
Ryan Tran - code, lab report