California Polytechnic State University Pomona

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Digital Circuit Design Verilog

ECE 3300L

Report #2

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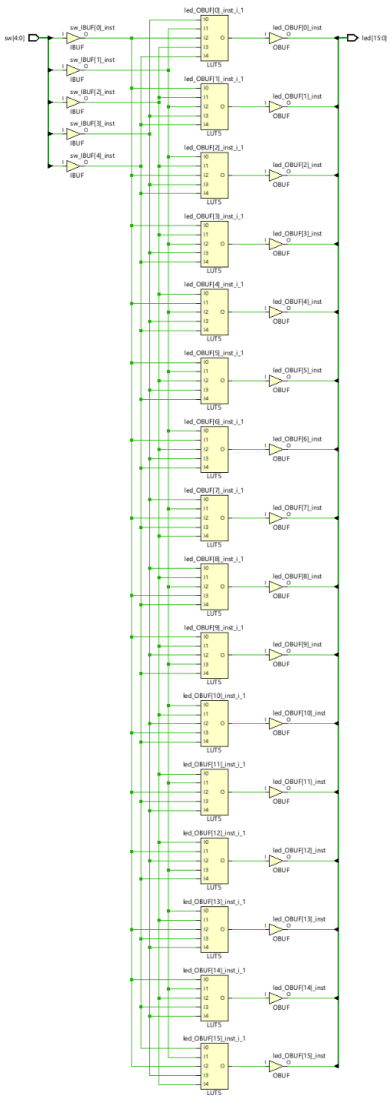
Objective: In Lab 2, students will design, simulate, and implement a 4-to-16 decoder with an enable input. When the decoder is enabled, exactly one of its 16 outputs will be HIGH depending on the 4-bit input value. When disabled, all outputs remain LOW. Students will experience both gate-level (structural) and behavioral Verilog coding, write a self-checking testbench, and analyze Vivado's resource utilization and timing reports.

Demo Video:

https://youtu.be/V1SjWwjWFRs

Design - Gate Level vs. Behavioral Snippets:

Schematic:



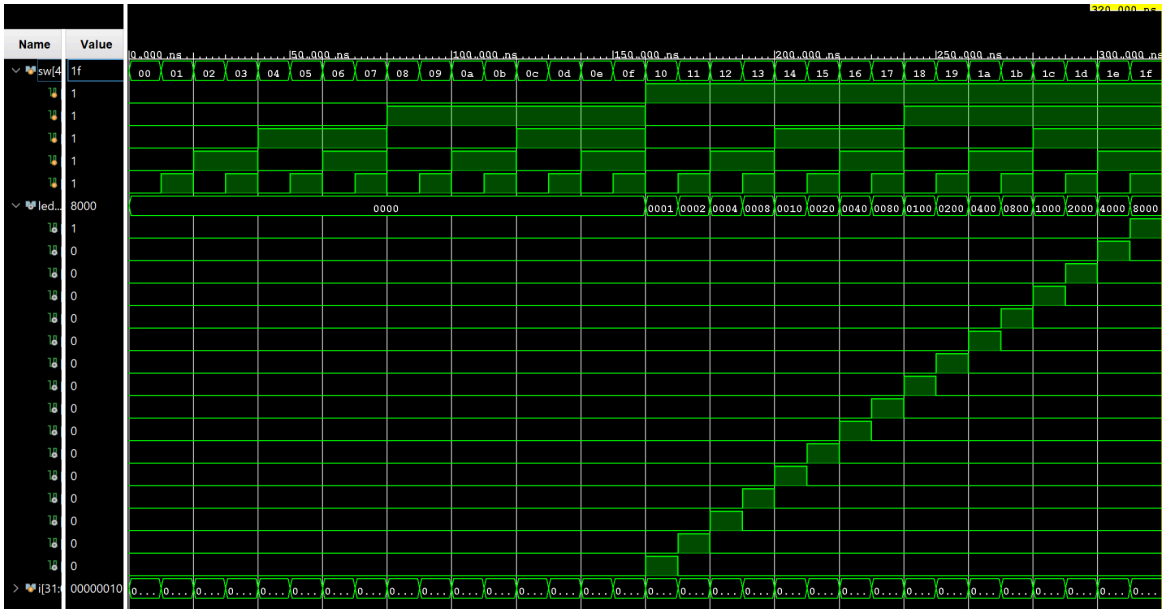
Simulation - Testbench Description/Waveform:

Description: The testbench automatically verifies that all combinations in the decoder are working correctly. To do this, the decoder module is instantiated inside the testbench through either the behavioral or gate-level implementation. Then the two main signals are declared and a loop cycles from 0 to 15 to test all input values. If the enable is 0 output is LOW, and if the enable is 1, only one output is HIGH.

Testbench Output:

```
Time resolution is 1 ps
Starting testbench...
PASS: sw[4]=0, sw[3:0]=0000 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=0001 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=0010 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=0011 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=0100 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=0101 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=0110 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=0111 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1000 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1001 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1010 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1011 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1100 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1101 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1110 → led=0000000000000000
PASS: sw[4]=0, sw[3:0]=1111 → led=0000000000000000
PASS: sw[4]=1, sw[3:0]=0000 → led=0000000000000001
PASS: sw[4]=1, sw[3:0]=0001 → led=0000000000000010
PASS: sw[4]=1, sw[3:0]=0010 → led=0000000000000100
PASS: sw[4]=1, sw[3:0]=0011 → led=0000000000001000
PASS: sw[4]=1, sw[3:0]=0100 → led=0000000000010000
PASS: sw[4]=1, sw[3:0]=0101 → led=0000000000100000
PASS: sw[4]=1, sw[3:0]=0110 → led=0000000001000000
PASS: sw[4]=1, sw[3:0]=0111 → led=0000000010000000
PASS: sw[4]=1, sw[3:0]=1000 → led=0000000100000000
PASS: sw[4]=1, sw[3:0]=1001 → led=0000001000000000
PASS: sw[4]=1, sw[3:0]=1010 → led=0000010000000000
PASS: sw[4]=1, sw[3:0]=1011 → led=0000100000000000
PASS: sw[4]=1, sw[3:0]=1100 → led=0001000000000000
PASS: sw[4]=1, sw[3:0]=1101 → led=0010000000000000
PASS: sw[4]=1, sw[3:0]=1110 → led=0100000000000000
PASS: sw[4]=1, sw[3:0]=1111 → led=1000000000000000
Tests Successful
$finish called at time : 320 ns : File "C:/Users/Sean/Documents/Summer 25 CPP/ECE3300L/Lab 2/Lab 2.srcs/sim 1/new/tb_decoder4x16.v" Line 41
```

Testbench Waveform:



Implementation - Resource Utilization Table & Timing Summary:

Resource Utilization Table:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	8	0	0	63400	0.01
LUT as Logic	8	0	0	63400	0.01
LUT as Memory	0	0	0	19000	0.00
Slice Registers	0	0	0	126800	0.00
Register as Flip Flop	0	0	0	126800	0.00
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.
Warning! LUT value is adjusted to account for LUT combining.
Warning! For any ECO changes, please run place_design if there are unplaced instances

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	21	0	0	210	10.00
Bonded IPADs	0	0	0	2	0.00
PHY_CONTROL	0	0	0	6	0.00
PHASER_REF	0	0	0	6	0.00
OUT_FIFO	0	0	0	24	0.00
IN_FIFO	0	0	0	24	0.00
IDELAYCTRL	0	0	0	6	0.00
IBUFDS	0	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	300	0.00
ILOGIC	0	0	0	210	0.00
OLOGIC	0	0	0	210	0.00

Timing Summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	16	Total Number of Endpoints:	16	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Contribution:

Heba - Created Code Foundation and Lab Report. 50%

Sean - Debugged Code, Connected Hardware, and Edited Video. 50%

Reflections:

Along the way, we dealt with a couple of issues. As we are still getting familiar with the software, we didn't properly put in the constraint files. Then, within the code, we had to fix the input and output definitions in the gate code. Finally, when it came to the case statements in the behavioral code initially, we were referencing all 5 bits, so the statements were never true. In order to fix this, we had to change the code to reference only the 3 relevant bits.