ECE 3300L

Lab Report #7

Group E

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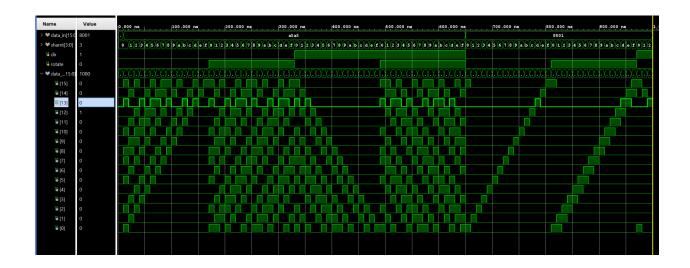
August 06, 2025

Design:

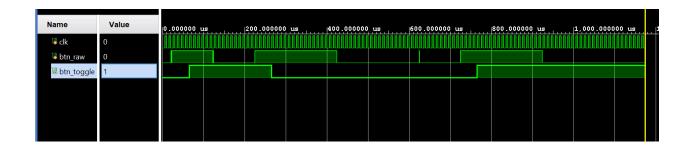
- a) clock_divider_fixed.v Divides 100 MHz into 1 kHz for display scanning and 2 Hz for demo using cascaded counters.
- b) debounce_toggle.v Debounces a button at 1 kHz and toggles output on each clean press.
- c) shamt.v 2-bit counter that increments on each debounced BTNC press to generate shamt[3:2].
- d) barrel_shifter16.v Performs logical or rotate left/right shifts on a 16-bit input in one cycle based on dir, rotate, and shamt.
- e) hex_to_7seg.v Converts a 4-bit value to a 7-segment display pattern.
- f) seg7_scan8.v Cycles through 8 digits at 1 kHz, outputting the active-low digit enable and segment pattern.
- g) top_lab7.v Integrates all modules to read switches/buttons, shift the input, and display the result with debug LEDs.

Simulation:

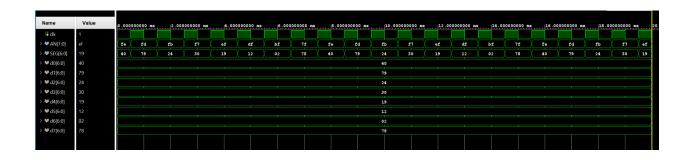
barrel_shifter16_tb:



debounce_toggle_tb:



seg7_scan8_tb:



Implementation:

+	-+		+-		+-		+		4.	+
Site Type				Fixed	İ	Prohibited	İ	Available	Ī	Util%
Slice LUTs*	-+	33		0		0	Ť	63400		
LUT as Logic		33	I	0	I	0		63400		0.05
LUT as Memory	-	0	Ī	0	Ī	0	I	19000	Ī	0.00
Slice Registers	-	67	I	0	I	0	I	126800	I	0.05
Register as Flip Flop	-	67	I	0	I	0	I	126800	I	0.05
Register as Latch	-	0	Ī	0	Ī	0	Ī	126800	Ī	0.00
F7 Muxes		0	Ī	0	Ī	0	I	31700	Ī	0.00
F8 Muxes	I	0	I	0	I	0	I	15850	I	0.00
+	-+		+-		+-		+		+-	+

Contributions:

Paul Kim - Source Codes, Testbench, Simulation - 50% contribution

Winson Zhu - Source Codes, Implementation, Hardware Demo - 50% contribution