Department of Electrical and Computer Engineering

ECE 3300L Section 1

Lab 4 – Switch-to-7-Segment Display Interface on Nexys A7

Bryan Liu ID: 016695471

Jaden Yeremenko ID: 016414528

July 9, 2025

Design:

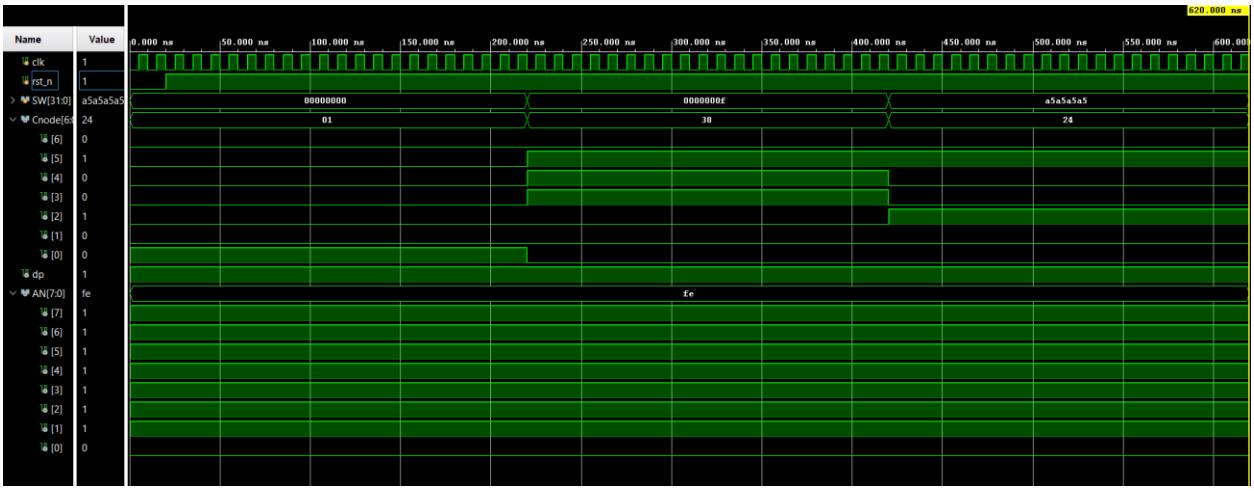
Src code:

```
`timescale 1ns/1ps
module seg7_driver(
  input        clk,
  input        rst_n,
  input  [15:0] SW,        // Eight 4-bit values
  output reg [6:0] Cnode, // Segments a-g (active low)
  output       dp,         // Decimal point (tie-off)
  output  [7:0] AN,         // Digit enables (active low)
  output  [15:0] LED
);

  // 1. Scan counter for ~200 Hz digit rate
  reg [19:0] cnt;
  always @(posedge clk or negedge rst_n)
    if (!rst_n) cnt <= 0;
    else        cnt <= cnt + 1;
  wire [2:0] scan = cnt[19:17];

  // 2. Pick the current 4-bit nibble
  reg [3:0] digit;
  always @(*) begin
    case (scan)
      3'd0: digit = SW[3:0];
      3'd1: digit = SW[7:4];
      3'd2: digit = SW[11:8];
      3'd3: digit = SW[15:12];
      3'd4: digit = SW[3:0];
      3'd5: digit = SW[7:4];
      3'd6: digit = SW[11:8];
      3'd7: digit = SW[15:12];
      default: digit = 4'd0;
    endcase
  end

  // 3. 4-bit → 7-segment (common-anode, active-low)
  always @(*) begin
    case (digit)
      4'd0:  Cnode = 7'b0000001;
      4'd1:  Cnode = 7'b1001111;
      4'd2:  Cnode = 7'b0010010;
```

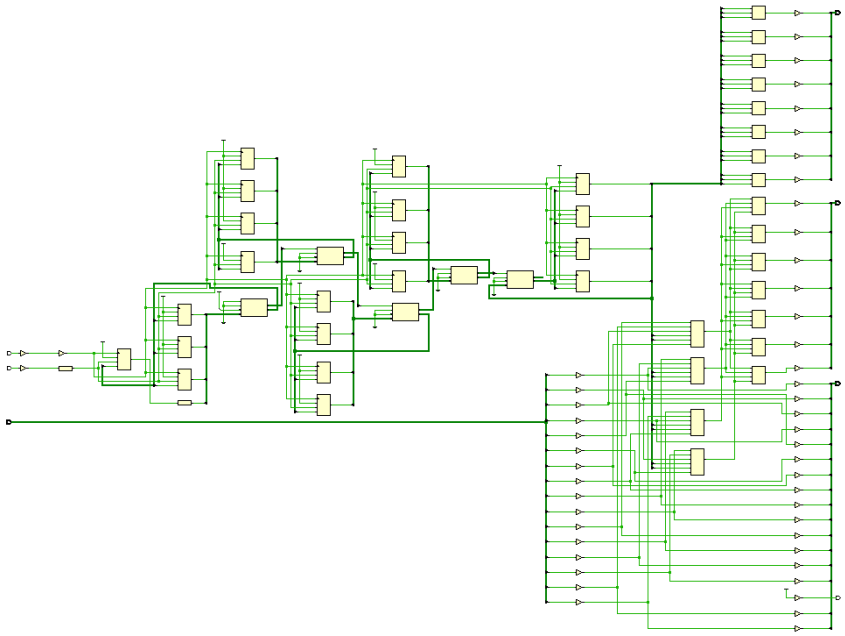
```
      4'd3:  Cnode = 7'b0000110;
      4'd4:  Cnode = 7'b1001100;
      4'd5:  Cnode = 7'b0100100;
      4'd6:  Cnode = 7'b0100000;
      4'd7:  Cnode = 7'b0001111;
      4'd8:  Cnode = 7'b0000000;
      4'd9:  Cnode = 7'b0001100;
      4'd10: Cnode = 7'b0001000;
      4'd11: Cnode = 7'b1100000;
      4'd12: Cnode = 7'b0110001;
      4'd13: Cnode = 7'b1000010;
      4'd14: Cnode = 7'b0110000;
      4'd15: Cnode = 7'b0111000;
      default: Cnode = 7'b1111111;
    endcase
  end

  // 4. Decimal point always off
  assign dp = 1'b1;

  // 5. Enable one AN at a time (active-low)
  reg [7:0] AN_tmp;
  always @(*) begin
    AN_tmp = 8'hFF;
    AN_tmp[scan] = 1'b0;
  end
  assign AN = AN_tmp;
  assign LED = SW;
endmodule
```

Simulation:

Waveform:



Schematic:



Implementation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.437 ns	Worst Hold Slack (WHS):	0.324 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	20	Total Number of Endpoints:	20	Total Number of Endpoints:	21

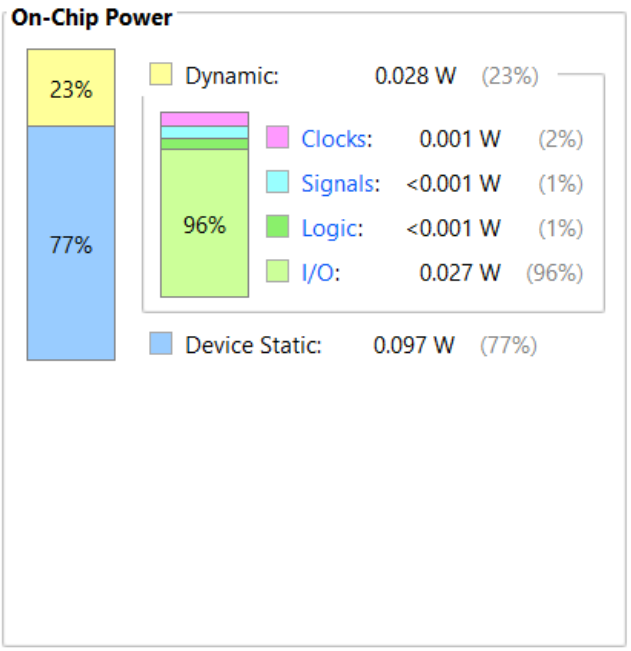
All user specified timing constraints are met.

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

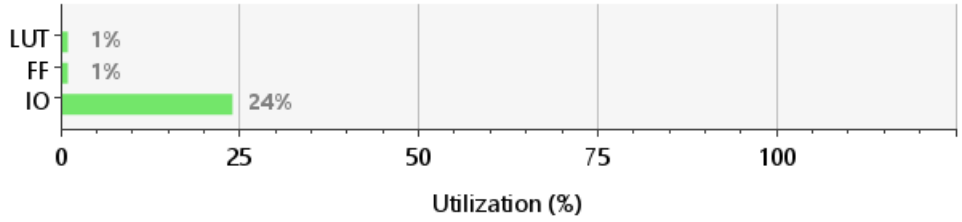
Total On-Chip Power:	**0.126 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (12.9 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Summary

Resource	Utilization	Available	Utilization %
LUT	14	63400	0.02
FF	20	126800	0.02
IO	50	210	23.81



Contributions:

Bryan Liu: Src code + Testbench code + xdc constraint file: 50%

Jaden Yeremenko: Synthesis + Implementation +Testing and Debugging: 50%