3300 Lab 1 Report

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1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	0	0	0	63400	0.00
LUT as Logic	0	0	0	63400	0.00
LUT as Memory	0	0	0	19000	0.00
Slice Registers	0	0	0	126800	0.00
Register as Flip Flop	0	0	0	126800	0.00
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.
Warning! LUT value is adjusted to account for LUT combining.
Warning! For any ECO changes, please run place_design if there are unplaced instances

Video Link: https://youtu.be/cUUGZgiRYvU

Reflections:

In the lab, we learned how to connect switches and LEDs on the Nexys A7-100T FPGA board using Verilog and a constraints file. We started by designing a simple Verilog module that directly maps each switch to its corresponding LED. Then we applied a constraints file to match the physical pins on the board to the signals in our code. This process helped us become more comfortable with writing HDL code and gave us a better understanding of verilog and the Nexys board.