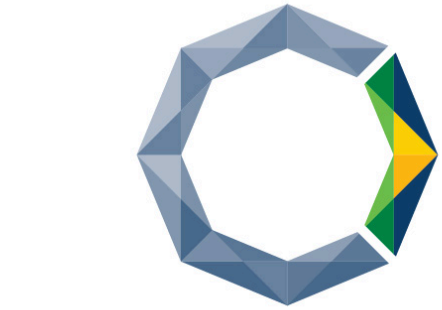

CalPolyPomona

College of Engineering

# California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #4

**Experiment #4**

Presented By: Kobe Aquino (StudentID: 015266433)

& Daniel Mondragon Xicotencatl (StudentID: 012803856)

Presented to Mohamed Aly

July 10, 2025

## Simulation:

### TestBench Log Description:


### Sample Waveform Picture: