California Polytechnic State University Pomona

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Dgtl Circuit Dsgn Verilog Lab

ECE 3300L Section E01

Report # 7

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Group H

Presented to

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DESIGN OVERVIEW:

In Lab 7, we built a 16-bit combinational barrel shifter/rotator capable of performing either a logical shift or a rotate operation in left or right direction by any shift amount k ∈ [0–15]. The design used BTNU, BTND, BTNL, BTNR as latched toggle controls and BTNC as asynchronous reset.

The shift amount SHAMT[3:0] is configured via:

- SHAMT[1:0] from toggled buttons (BTNL, BTNR)
- SHAMT[3:2] from a 2-bit up-counter incremented by BTNC

The 16-bit result is displayed as four hexadecimal nibbles across the rightmost four 7-segment digits (AN0–AN3), with AN4–AN7 blanked. We used a fixed clock divider to produce:

- A ~2 Hz clock for visual shifting
- A ~1 kHz clock for 7-segment scanning

We also added optional debug visibility for DIR, ROT, and SHAMT on LED[7:0].

MODULE HIERARCHY:

- **top_lab7.v**
    - clock_divider_fixed
    - debounce_toggle (x4 for BTNU, BTND, BTNL, BTNR)
    - shamt_counter
    - barrel_shifter16
    - hex_to_7seg (x4)
    - seg7_scan8

Top Module:

Explanation:
The top-level module instantiates all submodules and wires together to control inputs, display logic, and data outputs.

- **SW[15:0]** provides the 16-bit input word
- **BTNU** toggles DIR (0 = Left, 1 = Right)
- **BTND** toggles ROT (0 = Logical, 1 = Rotate)
- **BTNL/BTNR** toggle SHAMT[1:0]
- **BTNC** resets the design and increments the 2-bit shift counter for SHAMT[3:2]
- **LED[7:0]** displays current DIR, ROT, and SHAMT
- **AN0–AN3** display the barrel shifter output in hex
- **AN4–AN7** are blank

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clock_divider_fixed Module:

Explanation:
Uses two cascaded counters to derive:

- clk_2Hz (for demo timing)
- clk_1kHz (for scanning display and button debouncing)

Parameter: DIV_VALUE = 26'd50_000_000 (to get ~1 Hz base)

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debounce_toggle Module:

Explanation:
Debounces raw button inputs (BTNU, BTND, BTNL, BTNR).
Each clean press toggles an internal signal used for control (DIR, ROT, and SHAMT[1:0]).

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shamt_counter Module:

Explanation:
Implements a 2-bit counter that increments on each **BTNC press**.
This forms the upper bits of the shift amount: SHAMT[3:2].

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barrel_shifter16 Module:

Explanation:
Performs the 16-bit shift/rotate operation.

- Input: data_in[15:0], dir, rotate, shamt[3:0]
- Output: data_out[15:0]
  Uses four stages of generating loops ($\log_2 16 = 4$), 16 muxes per stage.

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hex_to_7seg Module:

Explanation:
Same lookup module from Lab 6, reused here to display each nibble of the 16-bit result.

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seg7_scan8 Module:

Explanation:
Drives the 7-segment display with 1-of-8 digit scanning at 1kHz.
We only enable AN0–AN3 and leave AN4–AN7 off.

TEST BENCH:

barrel_shifter16_tb.v

- Tested with various patterns (16'hA5A5, 16'h8001, etc.)
- Confirmed proper behavior for all 16 shift amounts, both directions, and both modes (logical/rotate)

debounce_toggle_tb.v

- Verified proper glitch filtering
- Output toggled only on clean edges

shamt_counter_tb.v

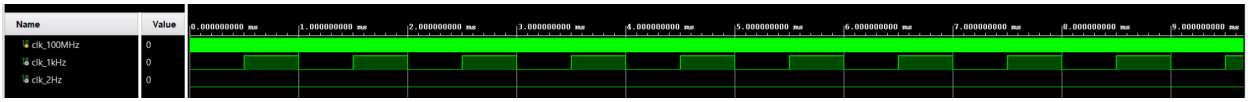
- Checked incrementing behavior on simulated BTNC pulses

seg7_scan8_tb.v

- Verified digit enable cycling and segment output for hex display

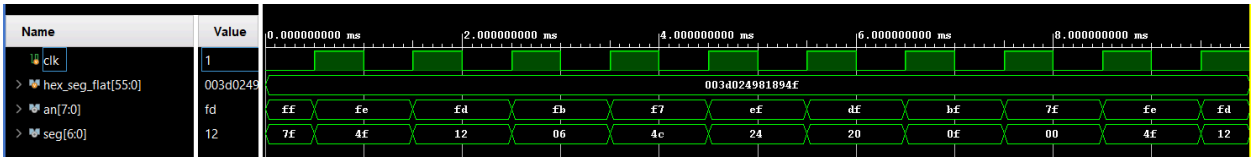
SIMULATION:

Clock Divider Fixed TB:

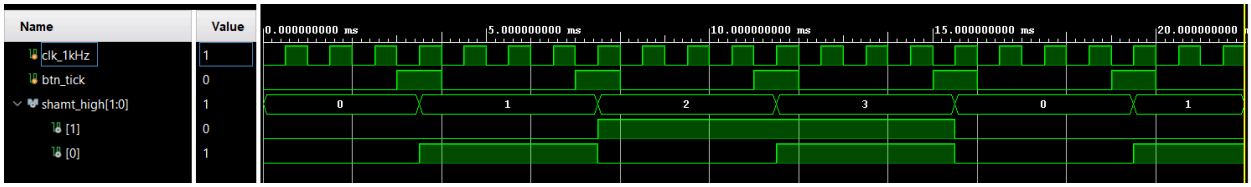


Hex_to_7seg_TB:

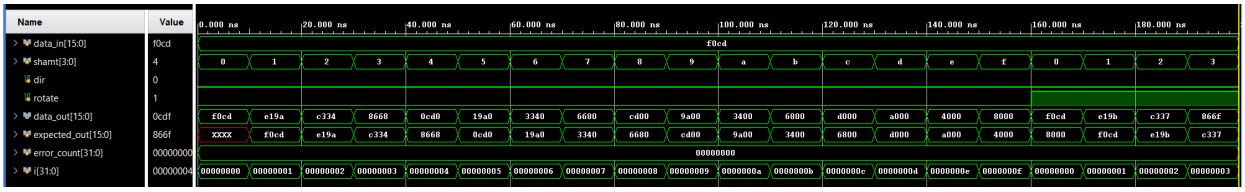
Seg7_scan8_TB:



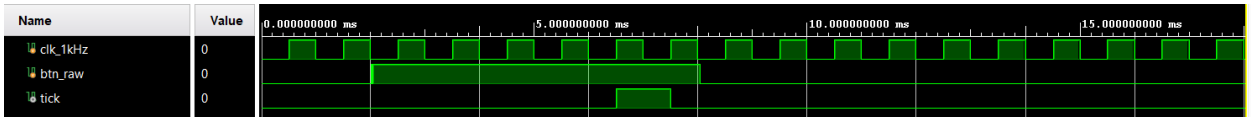
Shamt_counter_TB:



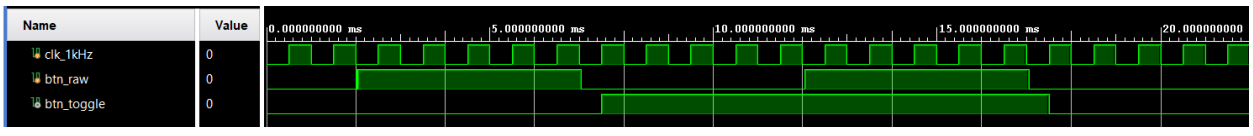
Barrel_shifter16_TB:



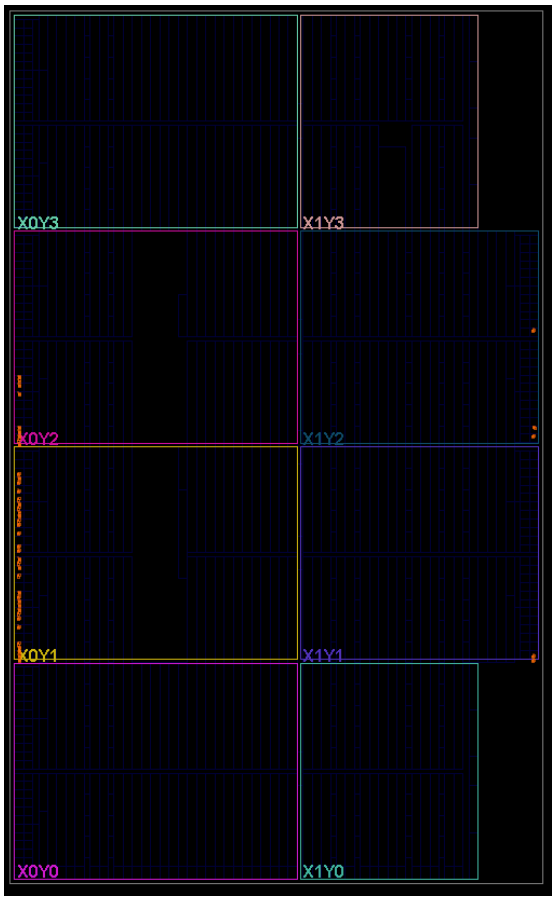
Debounce_tick_TB:



Debounce_toggle_TB:



SYNTHESIS SCHEMATIC:



RESOURCE UTILIZATION:

Name	Slice LUTs (63400)	Slice Registers (126800)	Bonded IOB (210)	BUFGCTRL (32)
top_lab7	107	71	45	2
db_s0 (debounce_toggle_1)	85	7	0	0

CONTRIBUTIONS:

Arvin Ghaloosian (50%)

- Implemented barrel_shifter16, clock_divider_fixed, and shamt_counter
- Led hardware demo and testing
- Verified LED display and shift logic

Vittorio Huizar (50%)

- Designed and tested debounce_toggle and seg7_scan8 modules
- Ran simulations and testbenches
- Integrated and debugged top-level system

REFLECTION:

This lab helped reinforce the value of combinational design using generate-for structures, especially for variable-shift logic. Implementing a barrel shifter deepened our understanding of mux tree structures. One challenge was tuning the toggle logic to ensure consistent behavior with physical buttons, which was resolved using clean debounce and edge-toggle modules. The shift counter and 7-segment scanning brought together many past lab skills into one cohesive system.

Link to demo video:

https://youtube.com/shorts/Cis5tRyRet4