3300 Lab 5
Switch-to-7-Segment Display Interface on Nexys A7

Group C
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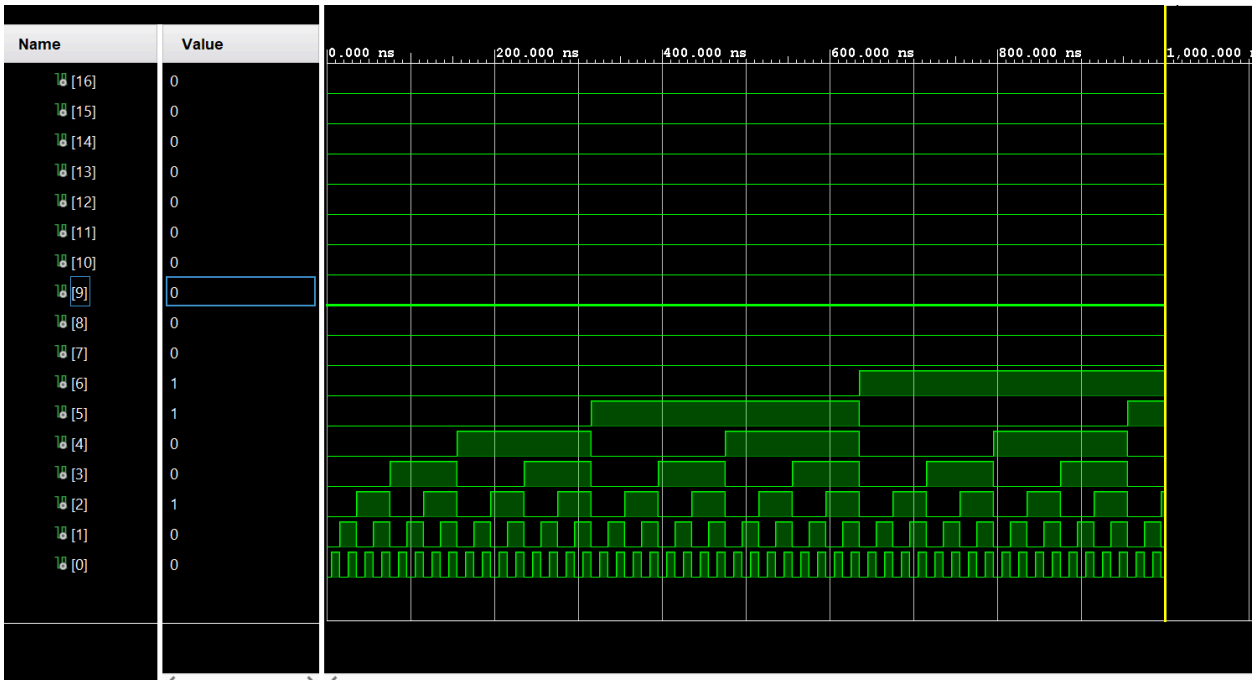
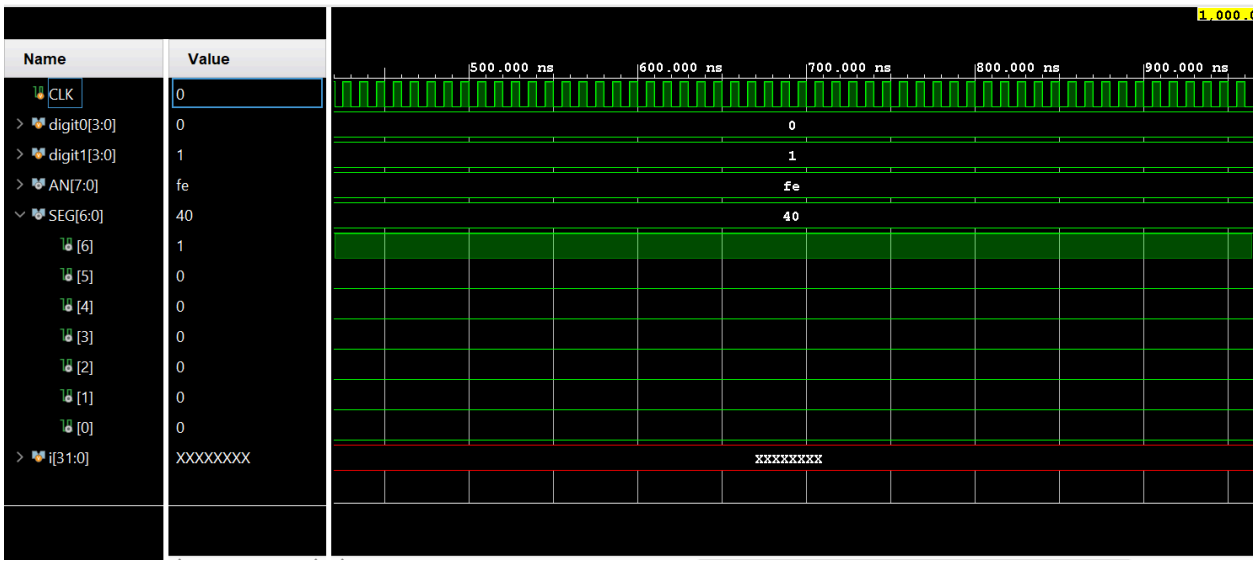
7/20/25

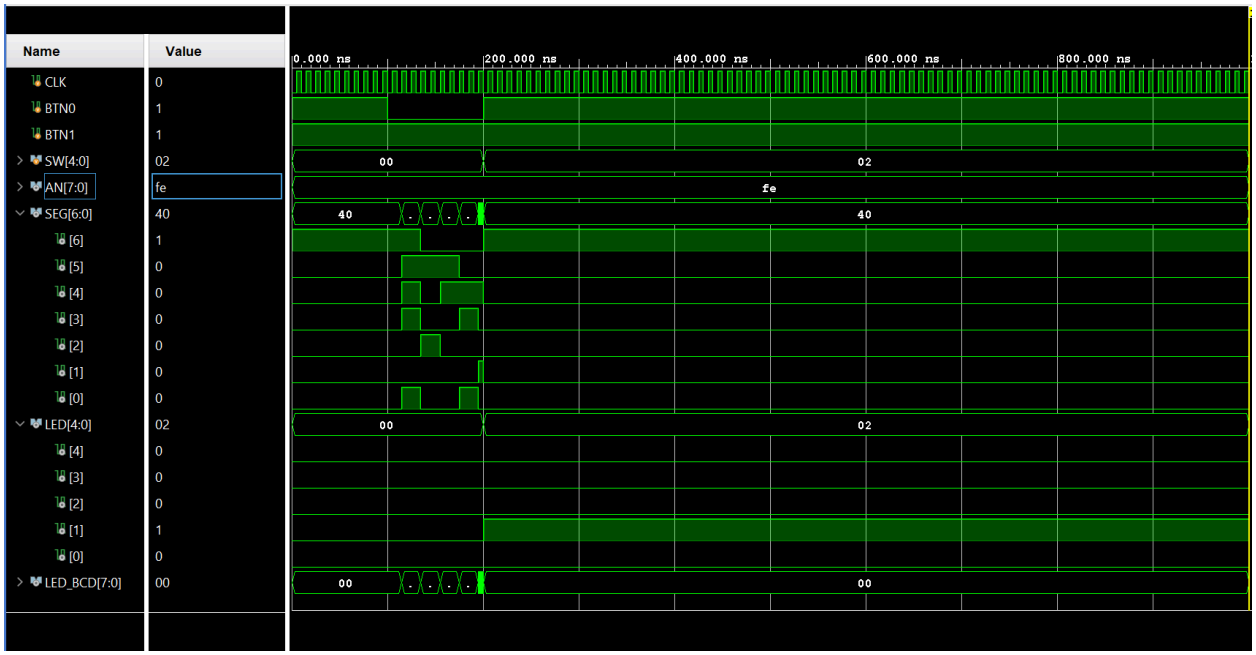
Waveform screenshot
clock_divider



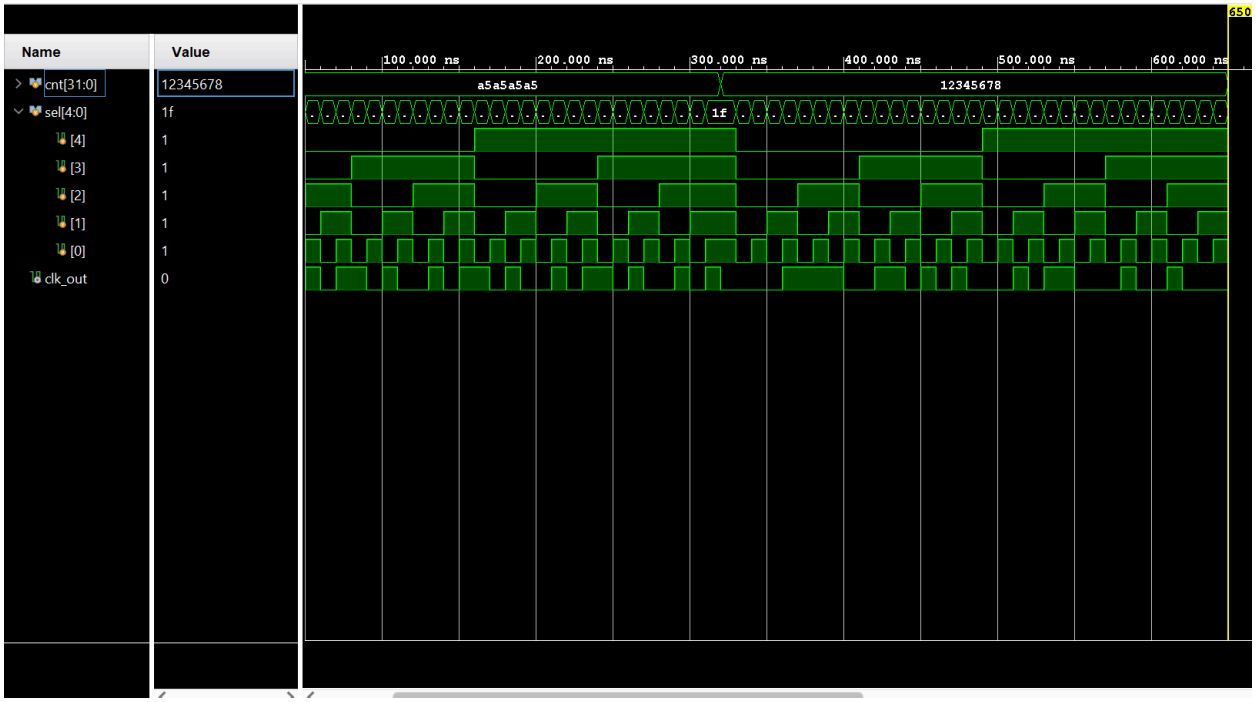
Seg7scan



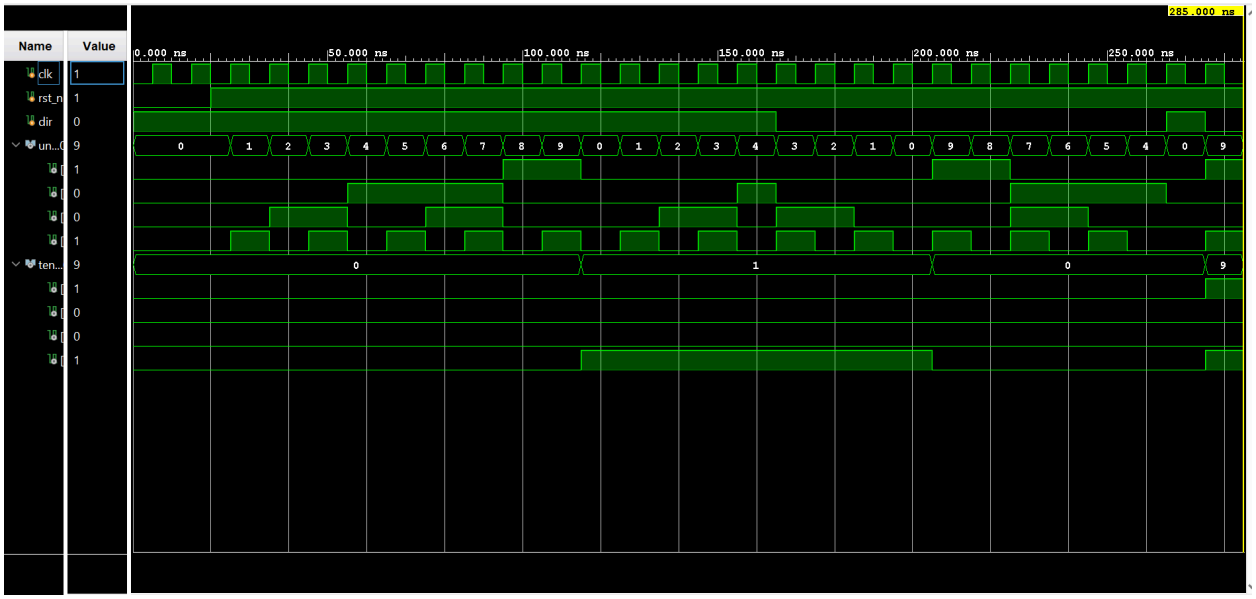
Top module



Mux32x1

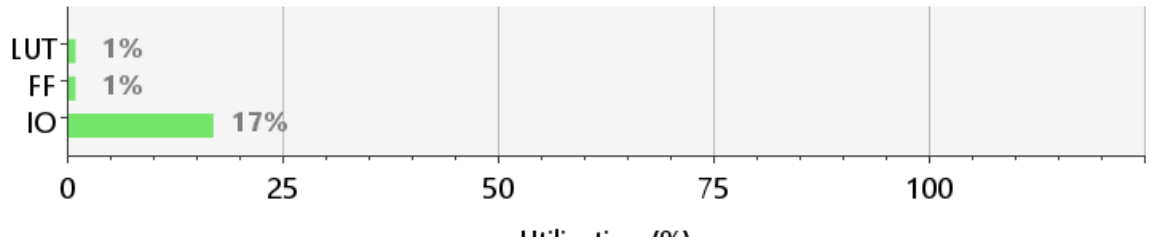


Bcd_up_down_counter



LUTs and FF screenshot:

Resource	Utilization	Available	Utilization %
LUT	26	63400	0.04
FF	59	126800	0.05
IO	36	210	17.14



Timing screenshot:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.621 ns	Worst Hold Slack (WHS):	0.249 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	51	Total Number of Endpoints:	51	Total Number of Endpoints:	52

All user specified timing constraints are met.

Contribution:
Rohan Walia (50%): Implementation, demo, verilog, report
Parsa Ghasemi (50%): testbench code, testing, report

Demo link: https://youtu.be/wobXr7kfy68

Reflections: This lab gave us practical experience building a functional BCD counter. We learned how clock division and proper synchronization are crucial when working with physical hardware and debugging the display multiplexing and counter rollover behavior improved our understanding of sequential logic implementation.