ECE 3300L

California State Polytechnic University, Pomona

Group G

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Lab Report #8

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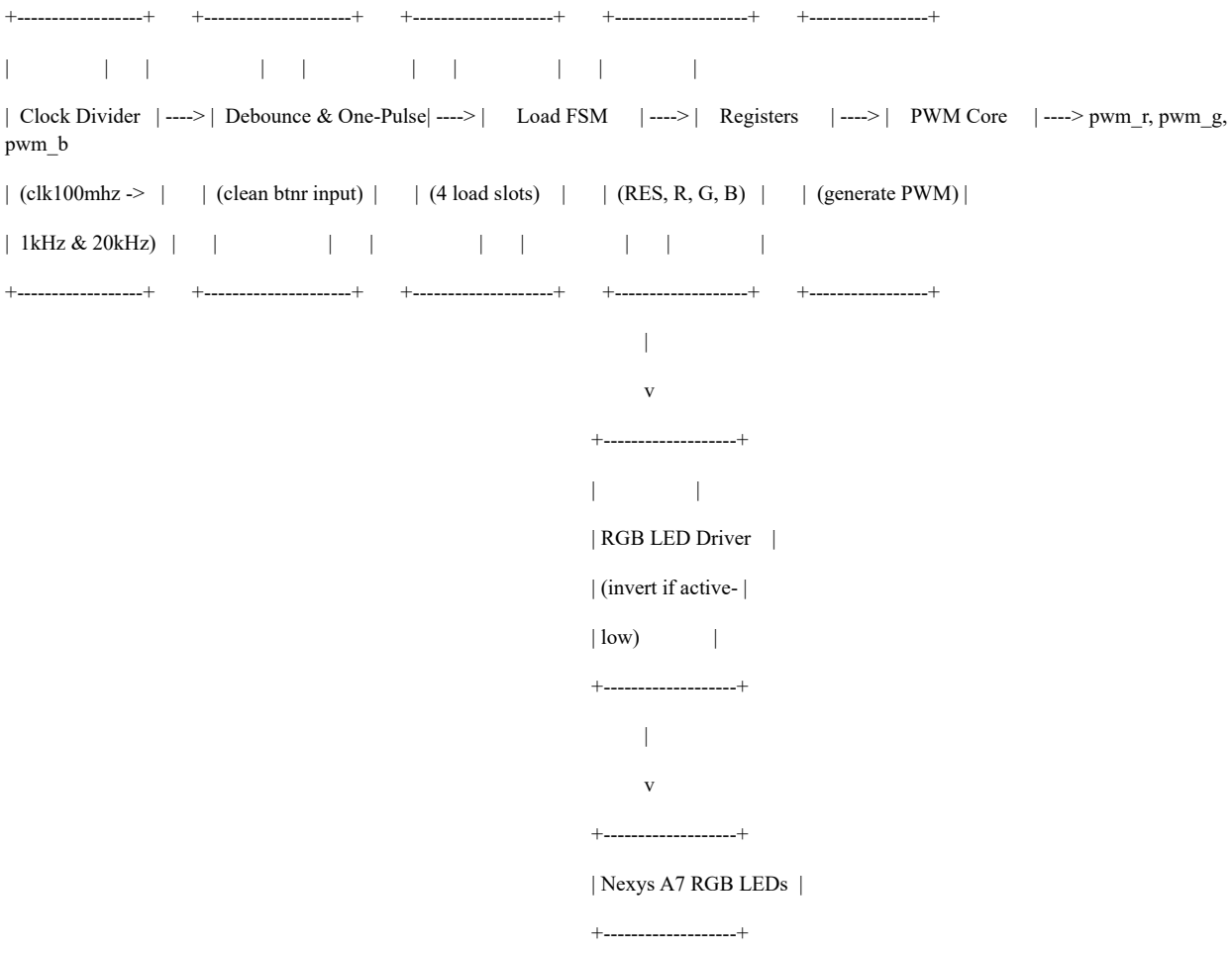
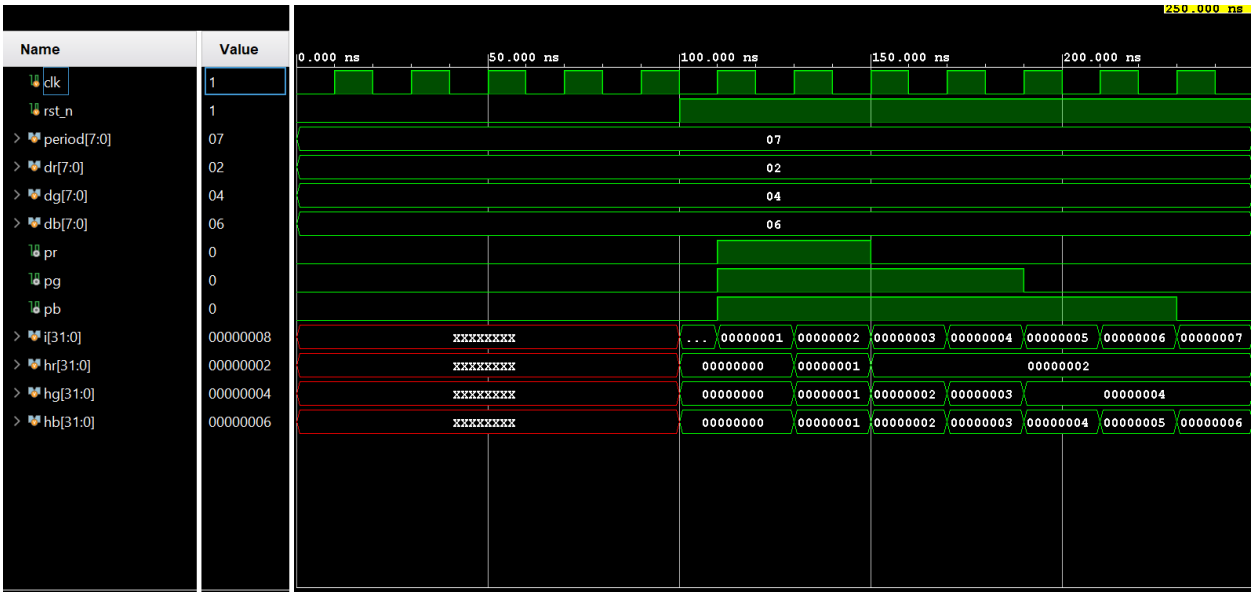
Explanation:

We have a simple 4-slot system that allows you to load four different values, one at a time, with the LOAD button. You load values into the slots in this way: PWM resolution (RES) followed by the brightness levels for the Red, Green, and Blue LEDs. You simply press the input button each time to load each value into the next slot, allowing you to change each value independently. The RES defines how many steps the PWM has to use to control the brightness; in code, it is actually RES + 1 because the PWM counts from 0 up to that number making the brightness of the LED smoother and more likely darker.

Block Diagram:



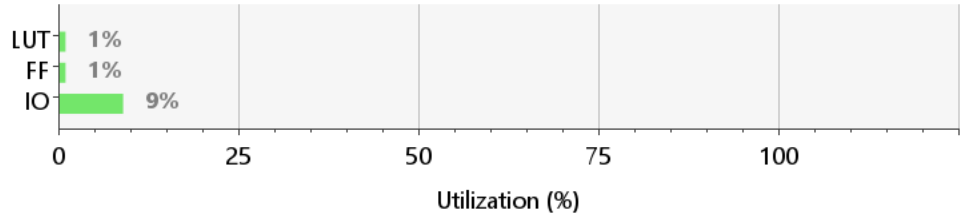
Pwm_core_tb:



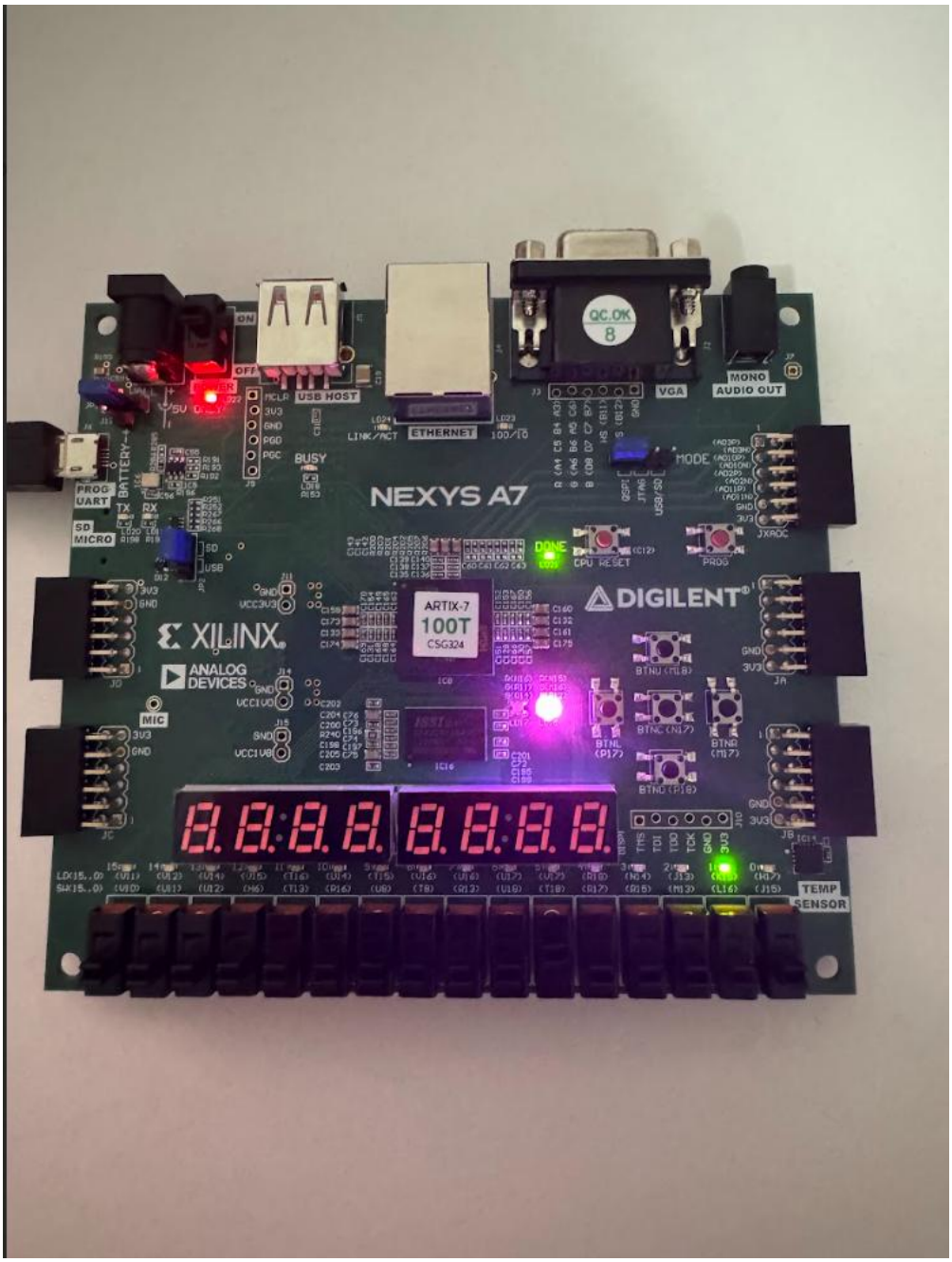
Hardware Utilization:

Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
top_lab8	113	152	62	113	18	3
u_db (debounce_onepulse)	7	10	3	7	0	0
u_div (clock_divider_fixed)	37	32	19	37	0	0
u_fsm (load_fsm)	5	2	2	5	0	0
u_pwm (pwm_core)	64	12	22	64	0	0

Resource	Utilization	Available	Utilization %
LUT	113	63400	0.18
FF	152	126800	0.12
IO	18	210	8.57



Board Picture:



Contributions:

Both worked on the Lab documents

Mikael: Verilog source files, Testbench file

Nathaniel: Simulations, Xdc file and Demo