ECE 3300L.01 - Lab 2

4x16 Decoder

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June 25th, 2025

Objective: You will design, simulate, and implement a 4-to-16 decoder with an enable input. When enabled, exactly one of 16 outputs goes HIGH based on the 4-bit input; when disabled, all outputs are LOW.

Design:

Gate-level vs. behavioral: The gate level uses gate logic and focuses on the physical gates to get things to work as intended. Meanwhile, behavioral uses conditional statements like if's and else's to get intended results. The gate level can be easier to understand and more precise when it comes to controlling hardware, but it is not easy to debug. Meanwhile, the behavioral level can be easy to write but harder to understand.

Simulation

```
# run 1000ns
Passed0
Passed1
Passed2
Passed3
Passed4
Passed5
Passed6
Passed7
Passed8
Passed9
Passed10
Passed11
Passed12
Passed13
Passed14
Passed15
$finish called at time : 180 ns : File "C:/Users/thisi/Desktop/project_2/project_2.srcs/sim_1/new/simulation.v" Line 152
INFO: [USF-XSim-96] XSim completed. Design snapshot 'testben_decoder4x16_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

Implementation

Utilization Table:

1. Slice Logic

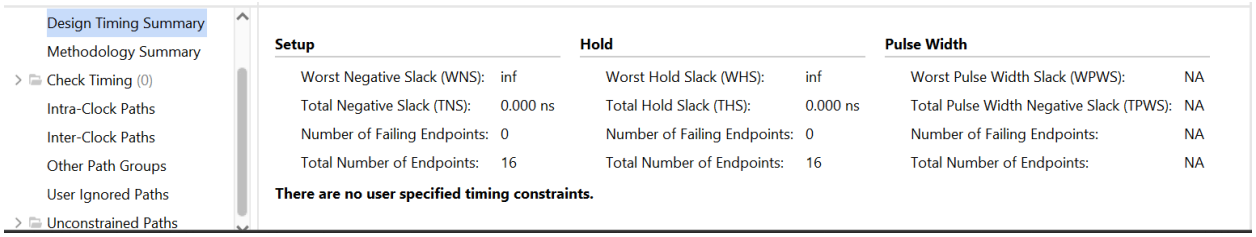
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	8	0	0	63400	0.01
LUT as Logic	8	0	0	63400	0.01
LUT as Memory	0	0	0	19000	0.00
Slice Registers	0	0	0	126800	0.00
Register as Flip Flop	0	0	0	126800	0.00
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

* Warning! LUT value is adjusted to account for LUT combining.

5. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	21	21	0	210	10.00
IOB Master Pads	8				
IOB Slave Pads	13				
Bonded IPADs	0	0	0	2	0.00
PHY_CONTROL	0	0	0	6	0.00
PHASER_REF	0	0	0	6	0.00
OUT_FIFO	0	0	0	24	0.00
IN_FIFO	0	0	0	24	0.00
IDELAYCTRL	0	0	0	6	0.00
IBUFDS	0	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	300	0.00
ILOGIC	0	0	0	210	0.00
OLOGIC	0	0	0	210	0.00

Time Summary:



Group Video

https://youtube.com/shorts/ahBljr9ykkk

Reflection

In this lab we learned the differences between gate-level and behavior-level, and how to use both. We tested the lab through a test bench to see a chart of all possible inputs and their outputs. We also tested this through the fpga board, turning different switches to see the output.

Contributions:

Kevin Tang (50%) - decoder4x16_bev code, test bench code.
Jared Mocling (50%)- board demo, decoder4x16_gate code.
We both worked on the lab report together.