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Group I

Session E02

Lab 4

Switch to 7 Segment Display Interface on NEXYS A7

Friday

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Objective:

In this lab we will be showing number system conversions and FPGA design using Verilog and the Nexys A7 board. By implementing slide switches, 7-segment displays, and mirror LEDS, we will translate 4-bit binary inputs into their corresponding hex and decimal values on the 7-segment displays. Also we utilize the decoderm multiplexer, and testbench verilog modules to verify that it works as intended.

Design(Code):

- This code initializes the input and outputs to allow for the later implementation.

```
module seg7_driver(
    input clk,
    input rst_n,
    input [15:0] SW,
    output reg [6:0] Cnode,
    output dp,
    output [15:0] LED,
    output [7:0] AN
);
```

- This segment initializes the clk function and uses case statements to allow each switch to control the specific digit being displayed.

```
always@(posedge clk or negedge rst_n)
    if(!rst_n) tmp<=0;
    else tmp<=tmp+1;

wire [2:0] s = tmp[19:17];

always@(s, SW)
    case (s)
        3'd0:digit=SW[3:0];
        3'd1:digit=SW[7:4];
        3'd2:digit=SW[11:8];
        3'd3:digit=SW[15:12];
        3'd4:digit=SW[3:0];
        3'd5:digit=SW[7:4];
        3'd6:digit=SW[11:8];
        3'd7:digit=SW[15:12];
        default:digit=4'b0000;
    endcase
```

- This final block also uses a case statement to set the specific binary numbers to the 7-segment display

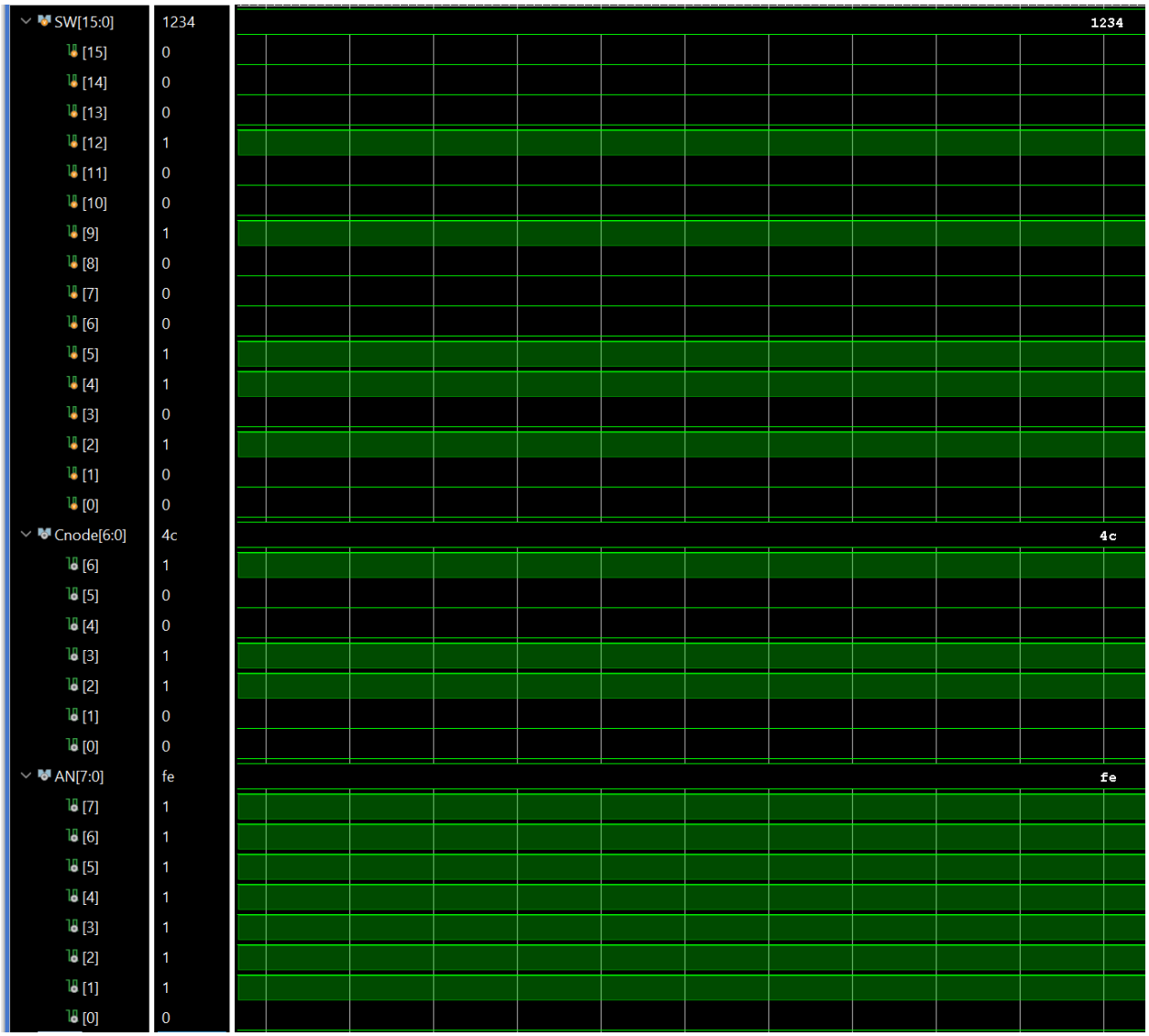
```
always@(s)
    case(s)
        3'd0:AN_tmp=8'b11111110;
        3'd1:AN_tmp=8'b11111101;
        3'd2:AN_tmp=8'b11111011;
        3'd3:AN_tmp=8'b11110111;
        3'd4:AN_tmp=8'b11101111;
        3'd5:AN_tmp=8'b11011111;
        3'd6:AN_tmp=8'b10111111;
        3'd7:AN_tmp=8'b01111111;
        default:AN_tmp=8'b11111111;
    endcase
assign AN=AN_tmp;
endmodule
```

Testbench and Waveform:

This is for SW = 0x1234

For the first 7-Segment Display

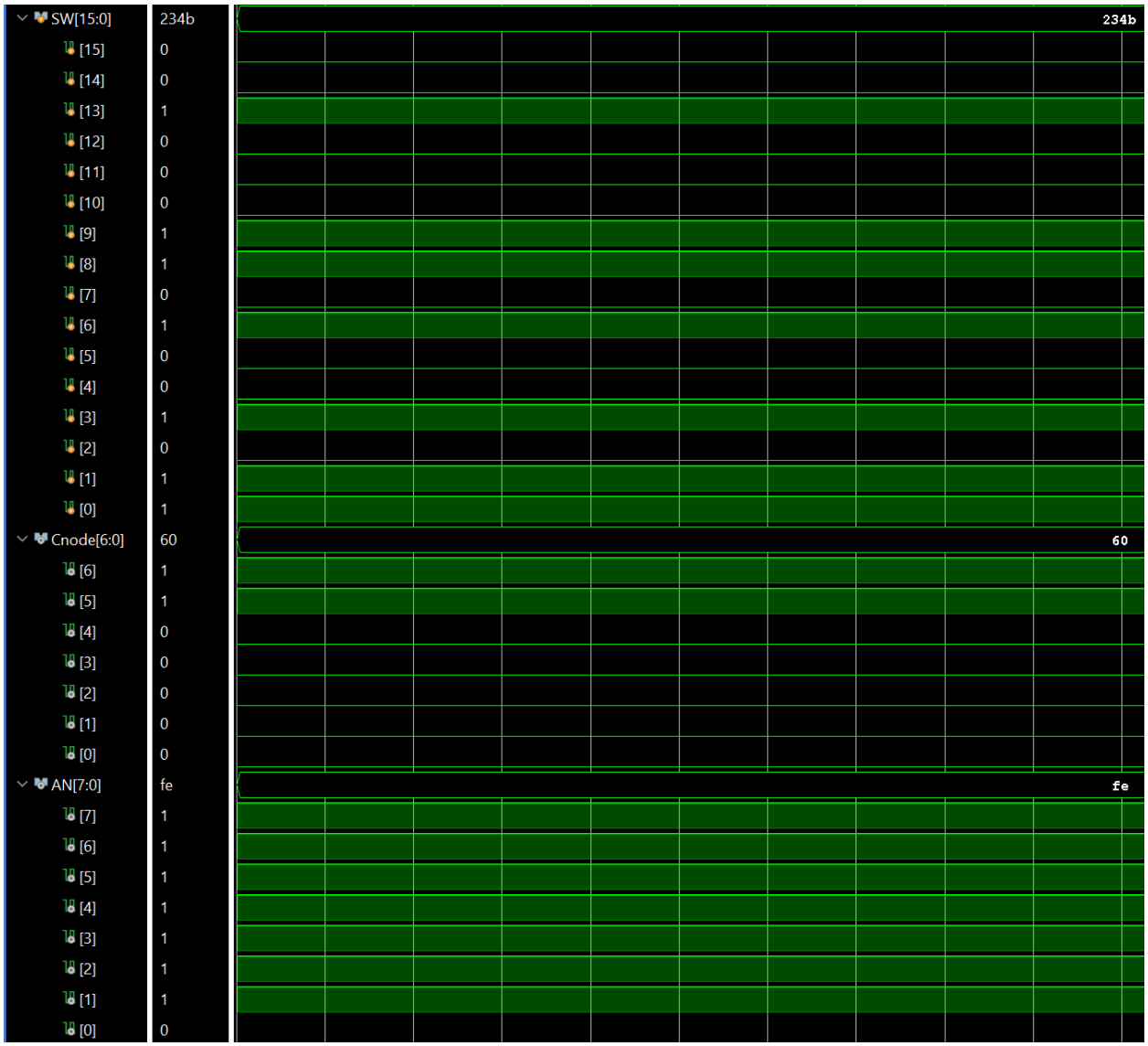
Cnode is showing 4



This is for SW = 0x234B

For the first 7-Segment Display

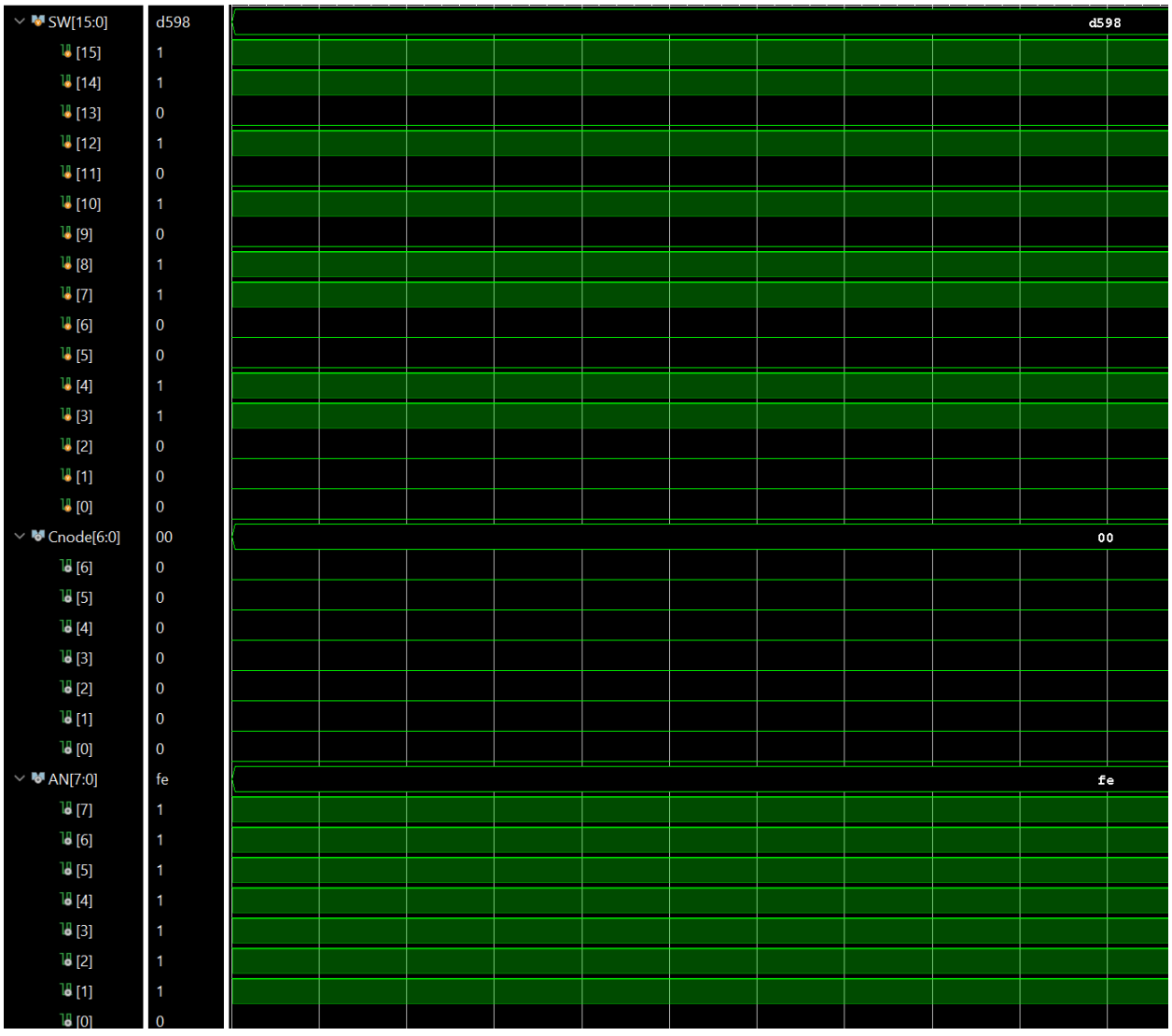
Cnode is showing b



This is for SW = 0xD598

For the first 7-Segment Display

Cnode is showing 8



- These testbenches show 3 examples which are digit “4”, letter “b”, and finally digit “8”. We can verify that the code is working correctly by checking the CNODE to check what segment is on(0) or off(1) corresponding to the digit or letter imputed by the switches.

Implementation:

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	14	0	0	63400	0.02
LUT as Logic	14	0	0	63400	0.02
LUT as Memory	0	0	0	19000	0.00
Slice Registers	20	0	0	126800	0.02
Register as Flip Flop	20	0	0	126800	0.02
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

Contributions:

Julio Flores: 50% - Verilog Code (Testbench Code) and Test demo and report

Victor Perez : 50% - Verilog Code (Constraints Code) and Waveform and report

Reflection:

This lab provided valuable hands-on experience with digital design concepts and FPGA development. Working with binary, decimal, and hexadecimal conversions showed an understanding of number systems and how they relate to hardware representation.