



CalPolyPomona

College of
Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #2

Experiment #2

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Presented to Mohamed Aly

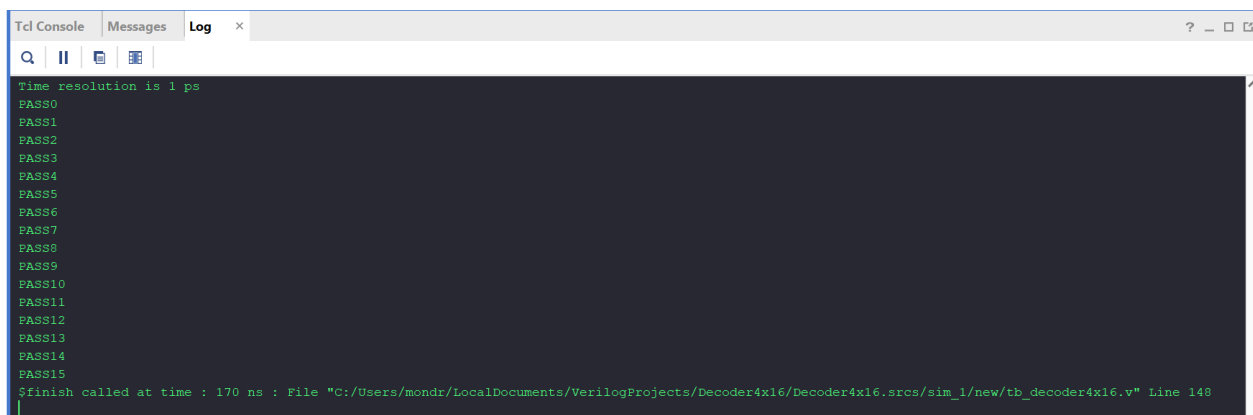
June 25th, 2025

Design:

Gate-level design involves defining the circuit using basic logic gates like AND, OR, and NOT, which closely represents the physical hardware layout. Meanwhile, behavioral design describes what the circuit should do using conditional statements, making it more easy to understand at a foundational level. Gate-level design is more complex, providing insight into the circuit's physical structure, but it is more time consuming and less productive as the designs get more complex. Behavioral design is more consistent in more complex systems due to its simplicity.

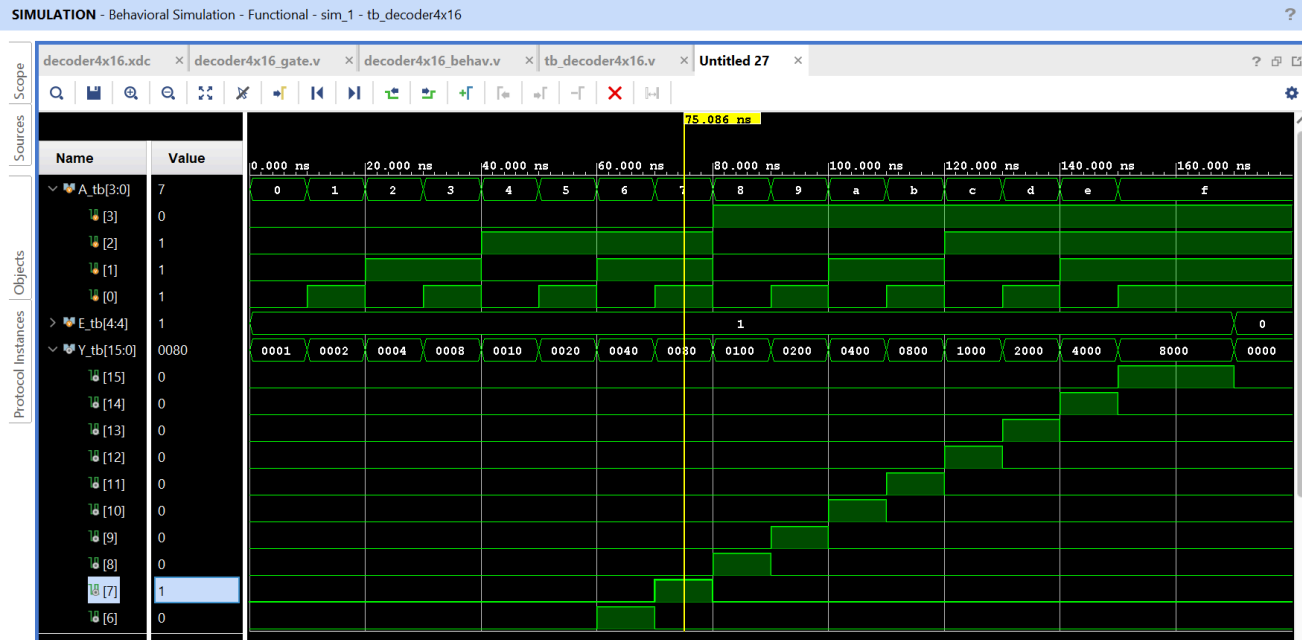
Simulation:

TestBench Log Description: shows that all cases passed.



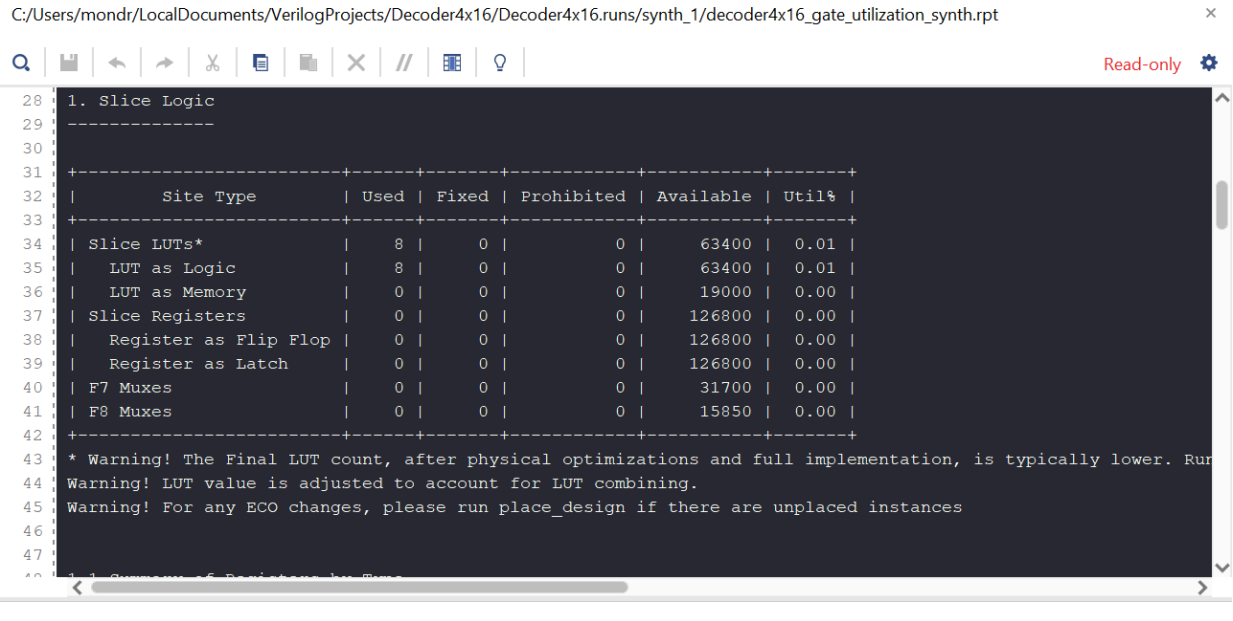
```
Tcl Console Messages Log x
Time resolution is 1 ps
PASS0
PASS1
PASS2
PASS3
PASS4
PASS5
PASS6
PASS7
PASS8
PASS9
PASS10
PASS11
PASS12
PASS13
PASS14
PASS15
$finish called at time : 170 ns : File "C:/Users/mondr/LocalDocuments/VerilogProjects/Decoder4x16/Decoder4x16.srcs/sim_1/new/tb_decoder4x16.v" Line 148
```

Sample Waveform Picture: We also tested for $E = 0$, at the end, the test bench confirms that all outputs stay LOW



Implementation:

Utilization Table:



Utilization - Synth Design - synth_1

C:/Users/mondr/LocalDocuments/VerilogProjects/Decoder4x16/Decoder4x16.runs/synth_1/decoder4x16_gate_utilization_synth.rpt

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	21	0	0	210	10.00
Bonded IPADs	0	0	0	2	0.00
PHY_CONTROL	0	0	0	6	0.00
PHASER_REF	0	0	0	6	0.00
OUT_FIFO	0	0	0	24	0.00
IN_FIFO	0	0	0	24	0.00
IDELAYCTRL	0	0	0	6	0.00
IBUFDS	0	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	300	0.00
ILOGIC	0	0	0	210	0.00
OLOGIC	0	0	0	210	0.00

Timing Summary:

Tcl Console Messages Log Reports Design Runs DRC Power Timing Utilization

Design Timing Summary

General Information	Setup	Hold	Pulse Width
Timer Settings	Worst Negative Slack (WNS): inf	Worst Hold Slack (WHS): inf	Worst Pulse Width Slack (WPWS): NA
Design Timing Summary	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): NA
Methodology Summary	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: NA
Check Timing (0)	Total Number of Endpoints: 16	Total Number of Endpoints: 16	Total Number of Endpoints: NA
Intra-Clock Paths	There are no user specified timing constraints.		
Inter-Clock Paths			
Other Path Groups			
User Ignored Paths			
Unconstrained Paths			

Timing Summary - impl_1 (saved) Timing Summary - timing_1

Contributions:

Daniel Mondragon + 50% effort

Kobe Aquino + 50% effort

Group Video Link: Here is the following link to our Lab 2 Group Demonstration Video:

<https://youtu.be/5IJdcM6cmcl>