California Polytechnic State University Pomona

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Dgtl Circuit Dsgn Verilog Lab

ECE 3300L Section E01

Report # 8

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Presented to

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DESIGN OVERVIEW:

In this lab, we designed and implemented a hardware-controlled RGB LED system using Pulse Width Modulation (PWM) on the Nexys A7 FPGA board. The design allows independent control of the resolution (PWM period) and duty cycles for the Red, Green, and Blue LED channels, enabling adjustable brightness and color mixing.

The entire system is controlled with a single LOAD button to sequentially store:

1. Resolution (PWM Period)
2. Red Duty Cycle
3. Green Duty Cycle
4. Blue Duty Cycle

The design uses:

- **BTNC** (Center Button) as active-high reset.
- **BTNR** (Right Button) as the load control to advance the 4-slot FSM.
- **SW[7:0]** to input 8-bit values for resolution and duty cycle settings.
- **LED[3:0]** to display the active load slot (one-hot encoded).
- Two on-board RGB LEDs (LD16, LD17) to display the generated colors.

MODULE HIERARCHY:

- **top_lab8.v**
    - clock_divider_fixed
    - debounce_onepulse
    - load_fsm

- pwm_core
- rgb_led_driver (x2 for both RGB LEDs)

Top Module: Explanation

The top-level module integrates all subsystems:

- Clock Generation: clock_divider_fixed produces a 1 kHz clock for debouncing and FSM control, and a 20 kHz clock for flicker-free PWM.
- Debouncing & One-Pulse: `debounce_onepulse` ensures a clean single-cycle load pulse from BTNR.
- Load FSM: `load_fsm` cycles through the 4 load slots, generating write-enable signals for the resolution and RGB duty registers.
- Register Storage: Four 8-bit registers store the resolution and duty values.
- Clock Domain Crossing: Two-stage synchronizers transfer values from the 1 kHz domain to the PWM clock domain.
- PWM Generation: `pwm_core` compares counters to duty values, producing high-frequency PWM signals.
- LED Driving: `rgb_led_driver` inverts PWM outputs (active-low) and drives the on-board RGB LEDs.

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clock_divider_fixed Module: Explanation

Generates two clocks from the 100 MHz input:

- 1 kHz clock (`clk_1k`) for debouncing and FSM timing.
- 20 kHz clock (`clk_pwm`) for PWM output.
  Uses separate counters for each output frequency with toggle-on-terminal-count logic.

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debounce_onepulse Module: Explanation

Filters mechanical switch bounce on BTNR and outputs a single-cycle `pulse` signal for each valid press.

- Synchronizes input to `clk_1k`.
- Requires a stable signal for a set number of ticks (`STABLE_TICKS = 20`).
- Detects a rising edge and outputs a one-cycle pulse.

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load_fsm Module: Explanation

Implements a 2-bit state machine that cycles through four load slots on each `load_pulse`. Outputs one-hot encoded slot indicators to drive LED[3:0] and corresponding write-enable signals (`wr_res`, `wr_r`, `wr_g`, `wr_b`).

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pwm_core Module: Explanation

Generates PWM signals for the three color channels:

- `period` (RES register) defines the PWM resolution (`eff_period = RES + 1`).
- Each duty value is clamped to avoid exceeding `eff_period`.
- A counter runs from 0 to `eff_period − 1` and compares against each duty value to produce `pwm_r`, `pwm_g`, `pwm_b`.

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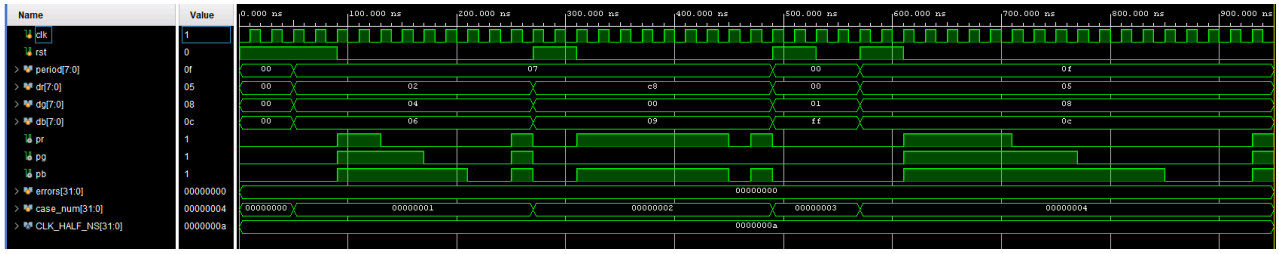
rgb_led_driver Module: Explanation

Accepts PWM inputs and outputs LED drive signals. If `ACTIVE_LOW` is set, inverts each PWM output for active-low LED hardware.

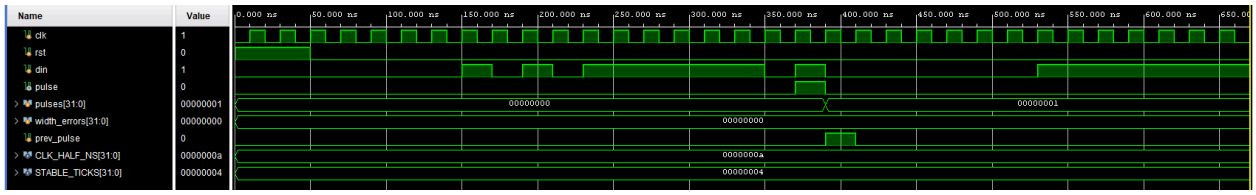
TEST BENCHES

- pwm_core_tb.v



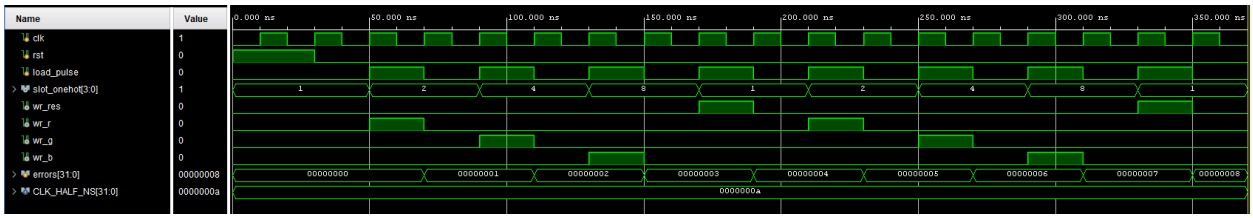
  - Verified correct PWM ratios for various duty values and resolutions.
  - Confirmed RES + 1 period behavior and duty clamping at maximum values.

- debounce_onepulse_tb.v



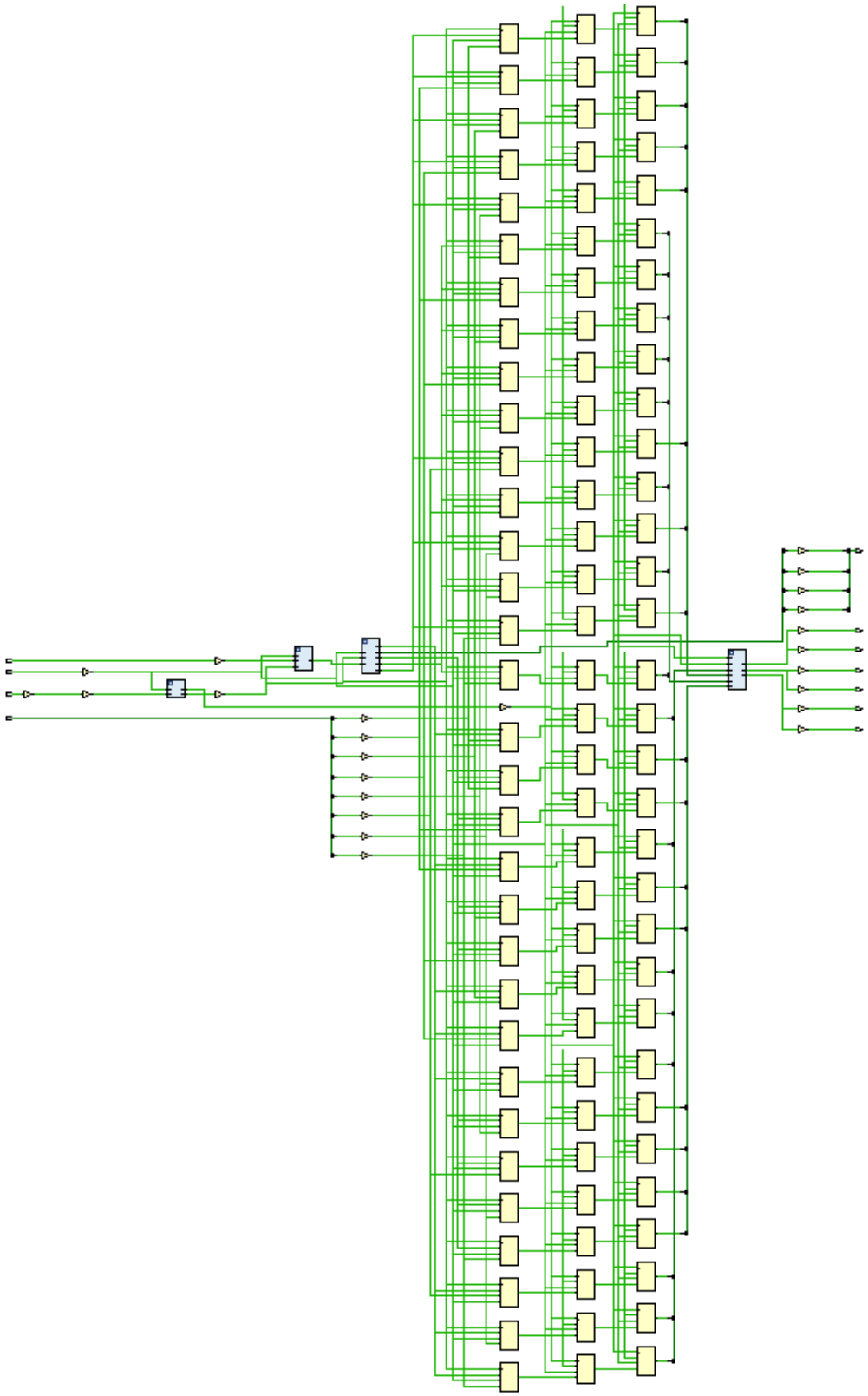
  - Verified single-pulse generation and proper noise filtering.

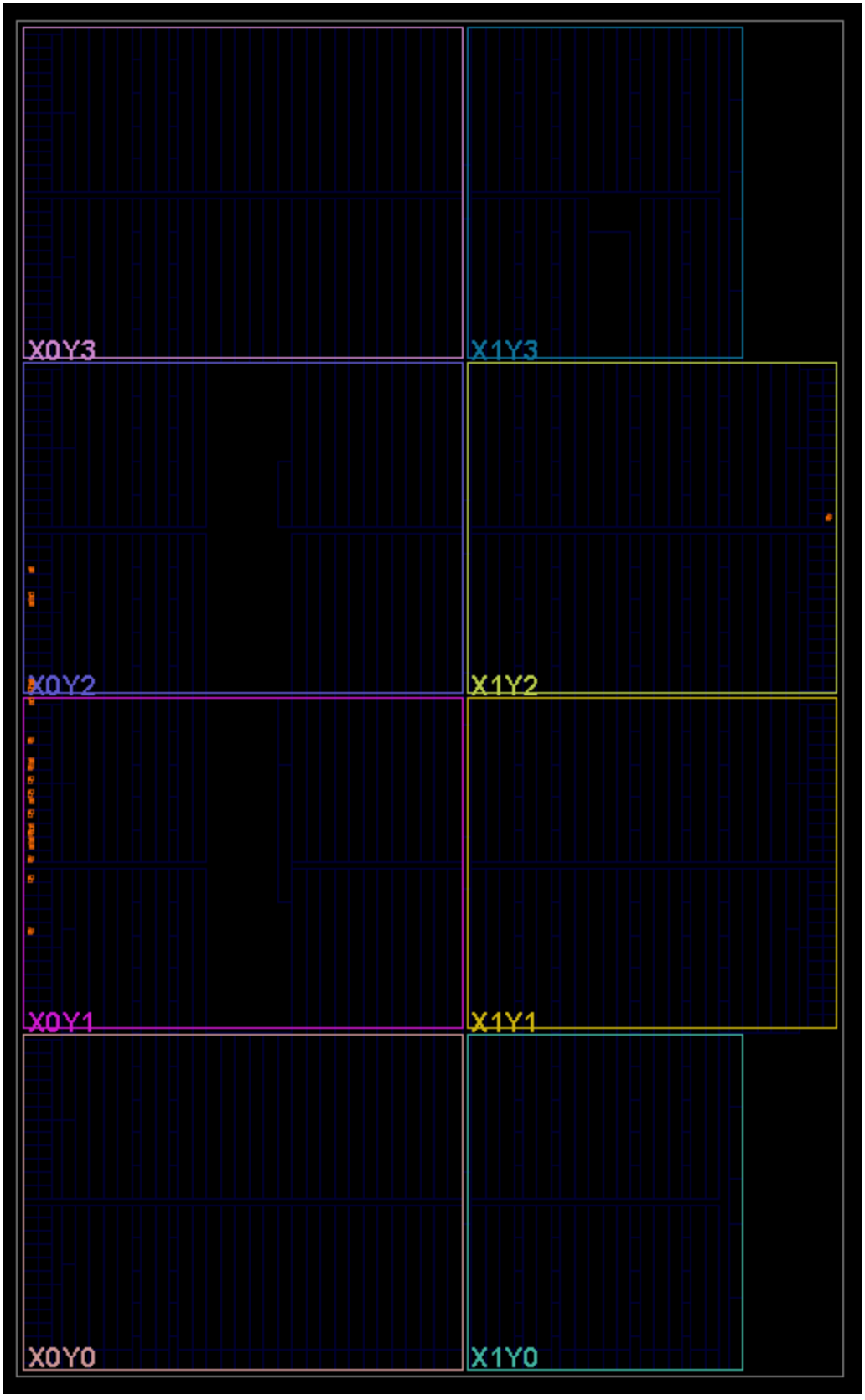
- load_fsm_tb.v



  - Checked correct slot sequencing and one-hot LED output.

SYNTHESIS SCHEMATIC:




X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0

RESOURCE UTILIZATION:

Name	Slice LUTs (63400)	Slice Registers (126800)	Bonded IOB (210)	BUFGCTRL (32)
top_lab8	116	152	21	3
u_pwm (pwm_core)	67	12	0	0

CONTRIBUTIONS:

Arvin Ghaloosian (50%)

- Implemented `pwm_core`, `clock_divider_fixed`, and `load_fsm`.
- Integrated top-level design and performed hardware bring-up.
- Verified PWM accuracy and LED output behavior.

Vittorio Huizar (50%)

- Developed `debounce_onepulse` and `rgb_led_driver`.
- Created and ran simulation testbenches.
- Debugged and validated full system operation.

REFLECTION:

This lab provided hands-on experience with PWM-based digital control for RGB LEDs, demonstrating how adjusting resolution and duty cycles affects brightness and perceived color. The four-slot loading FSM allowed efficient use of limited input controls.

One challenge was ensuring stable PWM operation without flicker, which was solved by using a 20 kHz clock and proper two-stage synchronization between clock domains. Implementing the RES + 1 period and duty clamping also improved accuracy and avoided over-duty saturation.

The project reinforced the importance of careful clock domain crossing, signal debouncing, and modular design for complex FPGA systems.

Link to demo video:

https://youtu.be/sxtLGnraEL0