



CalPolyPomona

College of
Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #4

Experiment #4

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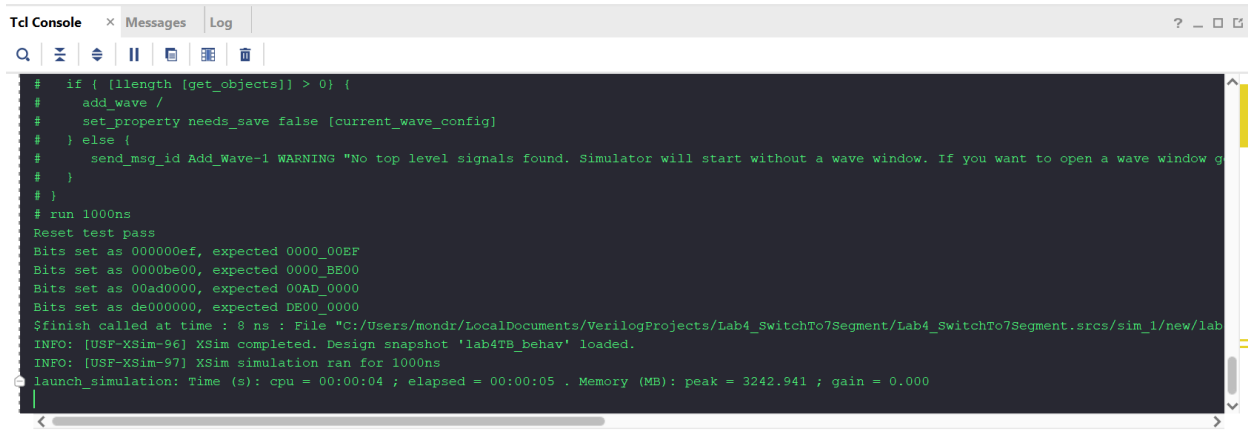
& Daniel Mondragon Xicotencatl (StudentID: 012803856)

Presented to Mohamed Aly

July 10, 2025

Simulation:

TestBench Log Description:



The screenshot shows the Tcl Console window with the following text:

```
# if { [length [get_objects]] > 0 } {  
#   add_wave /  
#   set_property needs_save false [current_wave_config]  
# } else {  
#   send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window g  
# }  
# }  
# run 1000ns  
Reset test pass  
Bits set as 000000ef, expected 0000_00EF  
Bits set as 0000be00, expected 0000_BE00  
Bits set as 00ad0000, expected 00AD_0000  
Bits set as de000000, expected DE00_0000  
$finish called at time : 8 ns : File "C:/Users/mondr/LocalDocuments/VerilogProjects/Lab4_SwitchTo7Segment/Lab4_SwitchTo7Segment.srsc/sim_1/new/lab  
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab4TB_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:04 ; elapsed = 00:00:05 . Memory (MB): peak = 3242.941 ; gain = 0.000
```

Sample Waveform Picture:

