Cal Poly Pomona

College of Engineering

California Polytechnic State University, Pomona

ECE3300L

Experiment #7

GROUP K
Hoang, Dalton - 016062800
Siu, Andy - 016205137

August 5th, 2025

Introduction:

In Lab 7 of ECE 3300L, we designed and implemented a 16-bit combinational barrel shifter and rotator, integrated with a 4-digit 7-segment display. The goal of this experiment is to establish logical or rotational shifting of a 16-bit word in either direction, based on control inputs from debounced push buttons. The result is displayed in real time on the board's hexadecimal display, offering a clear visual representation of the shifting behavior.

Design:

Clk_divider: This module implements a fixed clock divider using two cascaded counters to produce two slower clock signals: ~1 kHz for scanning the 7-segment display and ~2 Hz for visibly stepping the barrel shifter output.

Denounce_toggle: This module debounces mechanical push-button signals to filter out glitches and bouncing. It toggles a clean output (btn_toggle) each time a button press is detected with a clean rising edge, using the ~1 kHz clock.

Barrel_shifter16: This is the core combinational logic module that performs 16-bit logical or rotational shifts either left or right, based on the dir, rotate, and 4-bit shift amount shamt.

Shamt_counter: This module generates the upper two bits (shamt[3:2]) of the shift amount using a 2-bit counter.

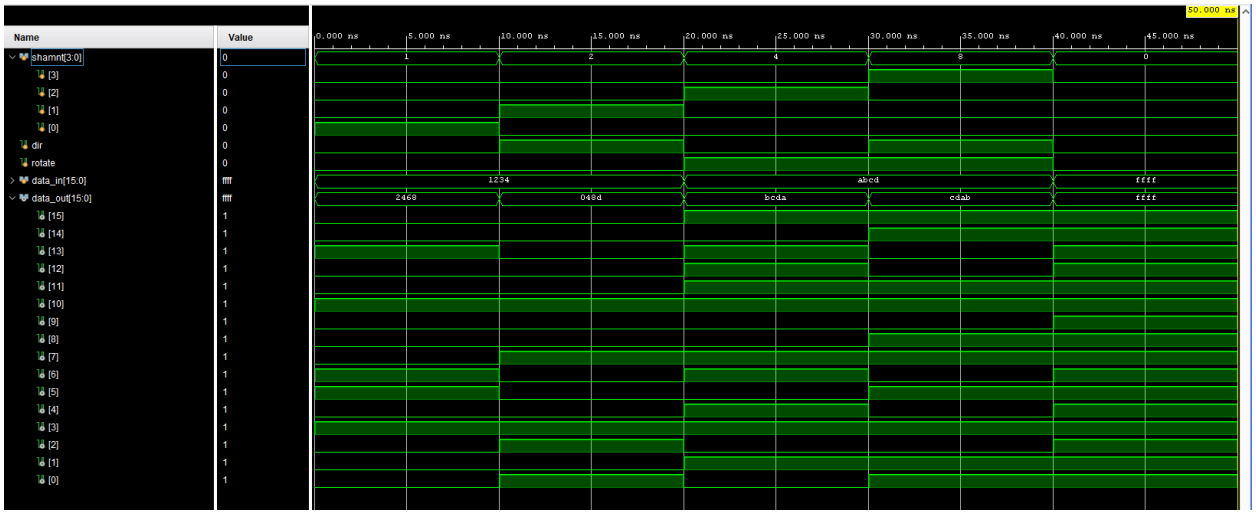
Hex_to_7seg: This module converts 4-bit binary inputs (hex digits) into corresponding 7-segment display patterns. It contains a lookup table mapping values 0–F to the appropriate 7-segment codes.

Seg7_scan8: This module manages time-multiplexed scanning of up to 8 digits on a 7-segment display. In this lab, only AN0–AN3 are used to show the 16-bit barrel shifter output as 4 hex digits.

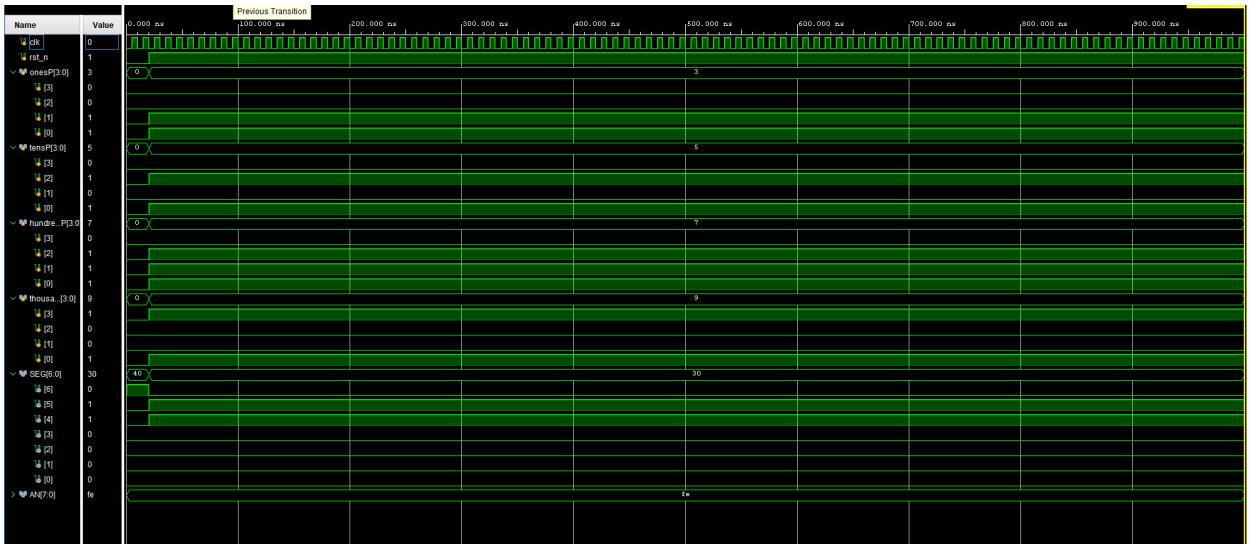
Top_lab7: This is the top-level module that instantiates and connects all other modules. It wires up the input switches, debounced buttons, control logic, barrel shifter, 7-segment encoders, and display scanner to produce the final system behavior.

Simulation:

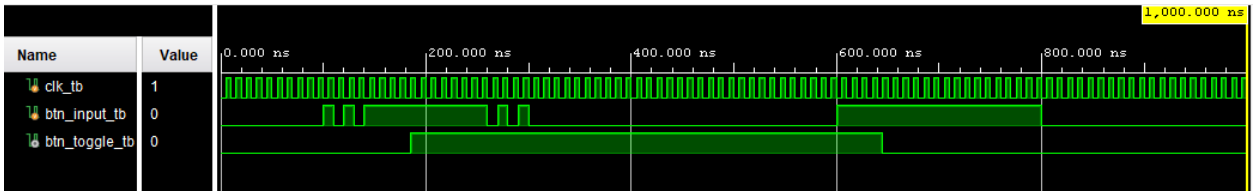
barrel_shifter_tb.v: verifies logical and rotational left/right shifting for a 16-bit barrel shifter by applying a variety of shamnt, dir, and rotate combinations and monitoring the output.



Seg7scan8_tb.v: verifies seg7scan8 cycles through 4 digits (onesP, tensP, hundredsP, thousandsP) and activates the correct AN bits and 7-segment output values (SEG).



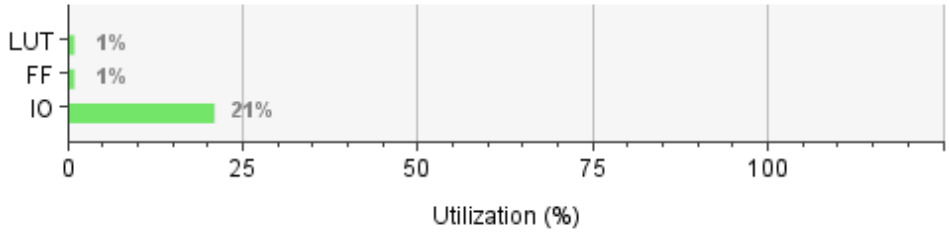
Debounce_toggle_tb.v: verifies that noisy, bouncing button inputs are correctly filtered by the debounce logic, resulting in clean, single toggles on the output signal.



Implementation:

Summary

Resource	Utilization	Available	Utilization %
LUT	60	63400	0.09
FF	71	126800	0.06
IO	45	210	21.43



Design Timing Summary

Setup

Worst Negative Slack (WNS):	5.919 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	72

Hold

Worst Hold Slack (WHS):	0.265 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	72

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	48

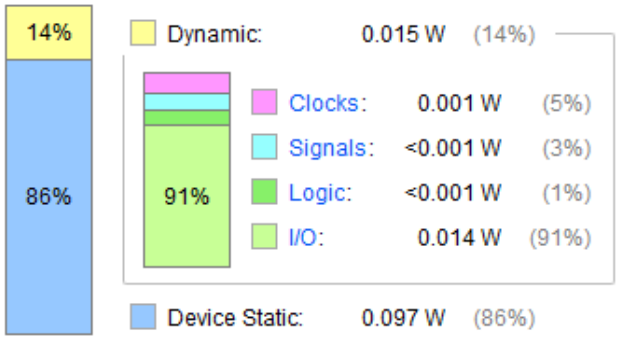
All user specified timing constraints are met.

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.112 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.5°C**
Thermal Margin:	59.5°C (12.9 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power



Video Link:

https://youtu.be/4higxxSDsZA

Contributions:

Andy Siu: 50% source files, testbench files, demo, report

Dalton Hoang: 50% source files, testbench files, simulation, report, implementation