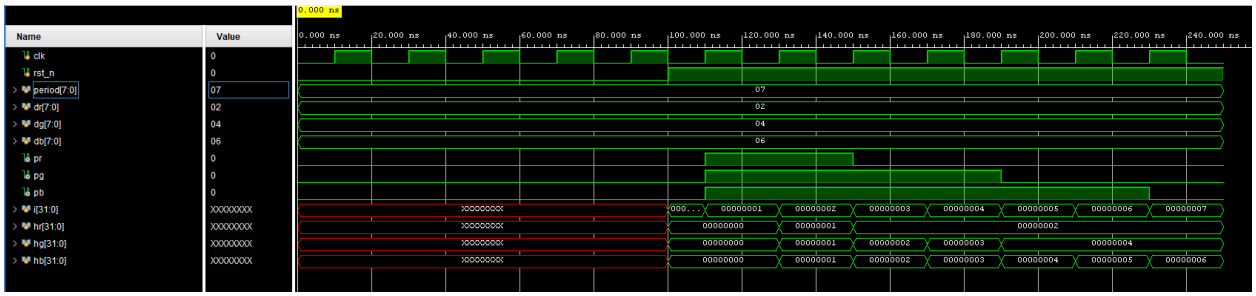
ECE 3300 Lab 8 Group J

Introduction

In this lab, we designed and implemented an RGB LED controller on the Nexys A7 FPGA using Pulse Width Modulation (PWM) to control the brightness and blending of colors. The project incorporated multiple hardware modules, including a clock divider to generate appropriate frequencies, a debouncing and one-pulse circuit to ensure clean button inputs, a finite state machine (FSM) to manage the loading of resolution and duty cycle values, and a PWM core to generate precise timing signals for the red, green, and blue channels. By cycling through four load slots with a single button, we were able to store and update the resolution period and individual color duty cycles, enabling smooth and flicker-free LED control. This lab emphasized modular digital design, clock domain crossing, and real-time signal control to achieve a fully functional hardware-driven RGB lighting system.

Testbench Waveform



pwm_core_tb

Group Video Link

https://youtube.com/shorts/I9h_hGgQQC8

Reflection

This lab was a valuable exercise in applying digital design principles to a practical, visually interactive system while exploring efficient user input handling. Implementing the RGB LED controller reinforced my understanding of modular Verilog development, as each stage played a critical role in the final functionality. The 4-slot loading system allowed a single button to cycle through four distinct storage registers: resolution (RES), red duty cycle, green duty cycle, and blue duty cycle, with the current slot indicated by an LED pattern. The PWM period was based on RES + 1 to ensure the counter covered the full intended range, preventing off-by-one errors and enabling precise brightness control. Overall, this lab deepened my skills in hardware-based PWM control, FSM design, and system integration on an FPGA platform.

Partner Contribution

Sean Go - code, lab report, video demonstration
Ryan Tran - code, lab report