ECE3300L

Lab 4

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Objective

The objective of this lab is to design a Verilog-based system on the Nexys A7 FPGA that converts 4-bit binary inputs into hexadecimal and decimal formats and displays them on the 7-segment display.

Verilog Code:

```
case(digit)
4'd0: Cnode=7'b0000001; 4'd1: Cnode=7'b1001111; 4'd2: Cnode=7'b0010010;
4'd3: Cnode=7'b0000110; 4'd4: Cnode=7'b1001100; 4'd5: Cnode=7'b0100100;
4'd6: Cnode=7'b0100000; 4'd7: Cnode=7'b0001111; 4'd8: Cnode=7'b0000000;
4'd9: Cnode=7'b0001100; 4'd10:Cnode=7'b0001000;4'd11:Cnode=7'b1100000;
4'd12:Cnode=7'b0110001;4'd13:Cnode=7'b1000010;4'd14:Cnode=7'b0110000;
4'd15:Cnode=7'b0111000;default: Cnode=7'b1111111;
endcase
always@(posedge clk or negedge rst_n)
if(!rst_n) tmp<=0;
else tmp<=tmp+1;
wire [2:0] s = tmp[19:17];
always@(s, SW)
case (s)
3'd0:digit=SW[3:0]; 3'd1:digit=SW[7:4];
3'd2:digit=SW[11:8]; 3'd3:digit=SW[15:12];
//4-7 are the 2nd set of 7 segment displays
3'd4:digit=SW[3:0]; 3'd5:digit=SW[7:4];
3'd6:digit=SW[11:8]; 3'd7:digit=SW[15:12];
default:digit=4'b0000;
endcase
reg [7:0] AN_tmp;
always@(s)
case(s)
3'd0:AN_tmp=8'b11111110;3'd1:AN_tmp=8'b11111101;
3'd2:AN_tmp=8'b11111011;3'd3:AN_tmp=8'b11110111;
3'd4:AN_tmp=8'b11101111;3'd5:AN_tmp=8'b11011111;
3'd6:AN_tmp=8'b10111111;3'd7:AN_tmp=8'b01111111;
default:AN_tmp=8'b11111111;
endcase
assign AN=AN_tmp;
endmodule
```

The driver code converts 4 switches to hexadecimal, lights up LEDs according to the switch position, and displays a 7-segment hexadecimal number.

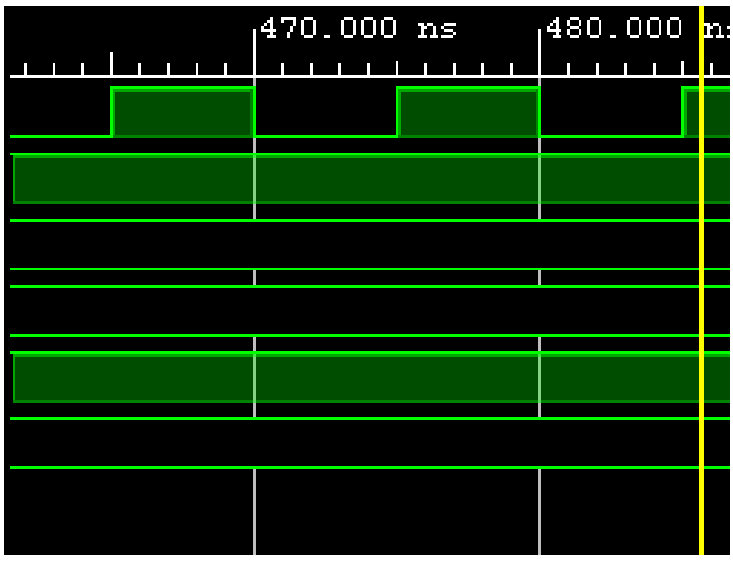
Test Bench Code

```
module seg7_driver_tb();

reg clk, rst_n;
reg [15:0] SW;
wire [6:0] Cnode;
wire dp;
wire [7:0] AN;
seg7_driver test (
                .clk(clk),
                .SW(SW),
                .rst_n(rst_n),
                .Cnode(Cnode),
                .dp(dp),
                .AN(AN)
                 );

always begin
 #5 clk = ~clk;
end
initial begin
SW = 32'h0000_A867;
clk = 0;
rst_n = 0;        // assert
#20 rst_n = 1;    // release
#10_000_000 $finish;
 end
endmodule
```

Simulation:



Implementation:

Utilization Table:

Resource	Utilization	Available	Utilization %
LUT	14	63400	0.02
FF	20	126800	0.02
IO	50	210	23.81

Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.440 ns	Worst Hold Slack (WHS):	0.324 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	20	Total Number of Endpoints:	20	Total Number of Endpoints:	21

Video:

https://youtu.be/vqPIlqdBZP0

Contributions:

Justin Wong: XDC, Driver Code, testbench code, report. 50% for all.
Hector Garibay: XDC, Driver Code, testbench code, report. 50% for all.