ECE 3300L

California State Polytechnic University, Pomona Group G

Nathaniel Garcia and Mikael Parsmyan Lab Report #6

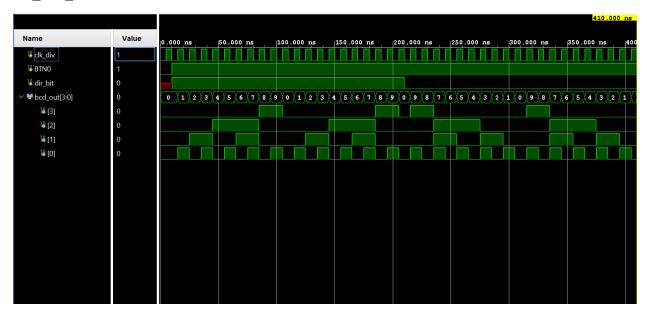
07/28/2025

Explanation:

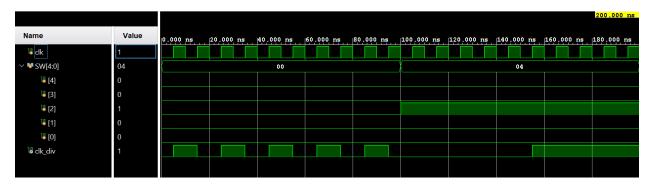
Tb_alu:

							30.00
Name	Value	0.000 ns	5.000 ns	10.000 ns	15 000 ns	20.000 ns	25 000 ns
∕ ™ A[3:0]	6		3		9	<u> </u>	6
¼ [3]	0						
¥ [2]	1						
¥ [1]	1						
₩ [0]	0						
₩ B[3:0]	7		5	<u> </u>	2	<u> </u>	7
¼ [3]	0						
¥ [2]	1						
⅙ [1]	1						
¥ [O]	1						
✓ ♥ ctrl[6:5]	2		0		1	<u> </u>	2
¼ [6]	1						
¥ [5]	0						
✓ ™ result[7:0]	00		08		07	<u> </u>	00
1 8 [7]	0						
Ta [6]	0						
1 ₀ [5]	0						
Ta [4]	0						
16 [4]	0						
16 [3]	0						
16 [2]	0						
18 [1]	0						
16 [0]	0						

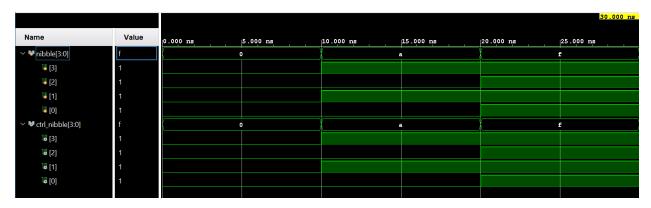
Tb_bcd_counter:



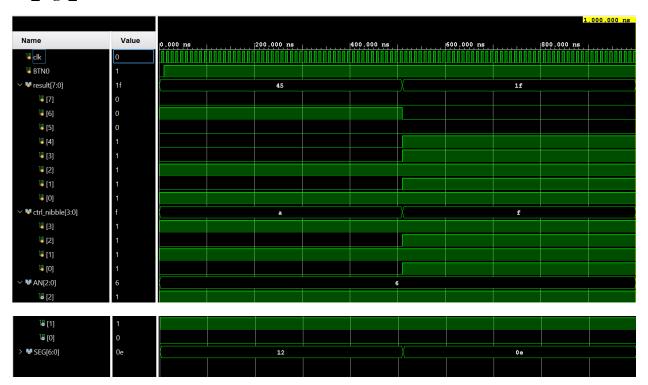
Tb_clock_divider:



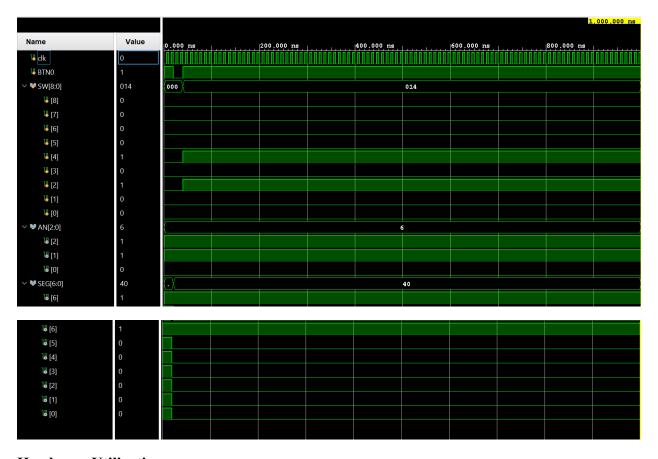
$Tb_control_decoder:$



Tb_seg7_scan:



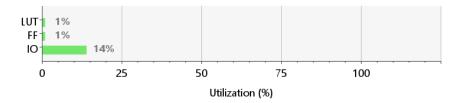
Tb_top_lab6:



Hardware Utilization:

Name 1	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
∨ N top_lab6	37	58	4	25	37	29	1
clkdiv_inst (clock_divider)	10	32	4	12	10	0	0
seg_inst (seg7_scan)	17	18	0	13	17	0	0
<pre>tens_inst (bcd_counter)</pre>	4	4	0	3	4	0	0
<pre>units_inst (bcd_counter_0)</pre>	6	4	0	4	6	0	0

Resource	Utilization	Available	Utilization %
LUT	37	63400	0.06
FF	58	126800	0.05
Ю	29	210	13.81



Contributions:

Both worked on the Lab document

Mikael: Verilog source files, Simulations

Nathaniel: Testbench files, Xdc file and Demo