ECE 3300 Lab 5 Group J

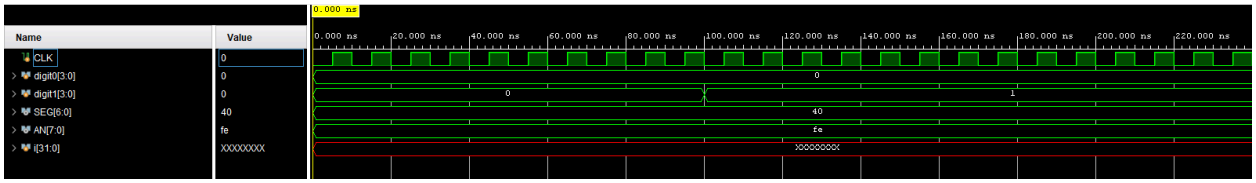
Introduction

In this experiment, we designed and implemented a two-digit BCD up-down counter on the Nexys A7 FPGA board using Verilog. The objective was to integrate multiple hardware components, including a 32-bit clock divider with selectable speed control, a dual-digit BCD counter, and a seven-segment display scan driver, into a complete digital system. User inputs such as counting direction (controlled by BTN1) and reset (BTN0) were used to interact with the system. The design required cascading two single-digit BCD counters to handle tens and units digits correctly, ensuring proper rollover and borrow behavior during counting. The final system displayed the counter values on a two-digit seven-segment display using multiplexing, with additional outputs mirrored on LEDs for debugging purposes. Through simulation, synthesis, and hardware testing, this lab emphasized modular design, clock domain control, and the practical integration of sequential logic on FPGA platforms.

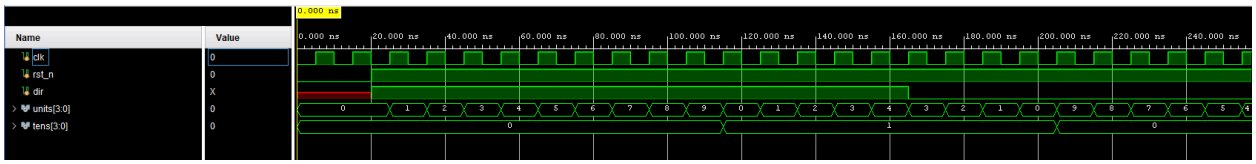
Testbench Waveform

mux32x1_tb

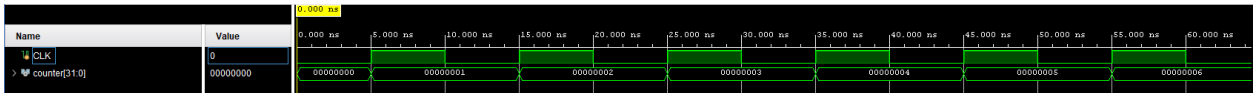
seg7_scan_tb

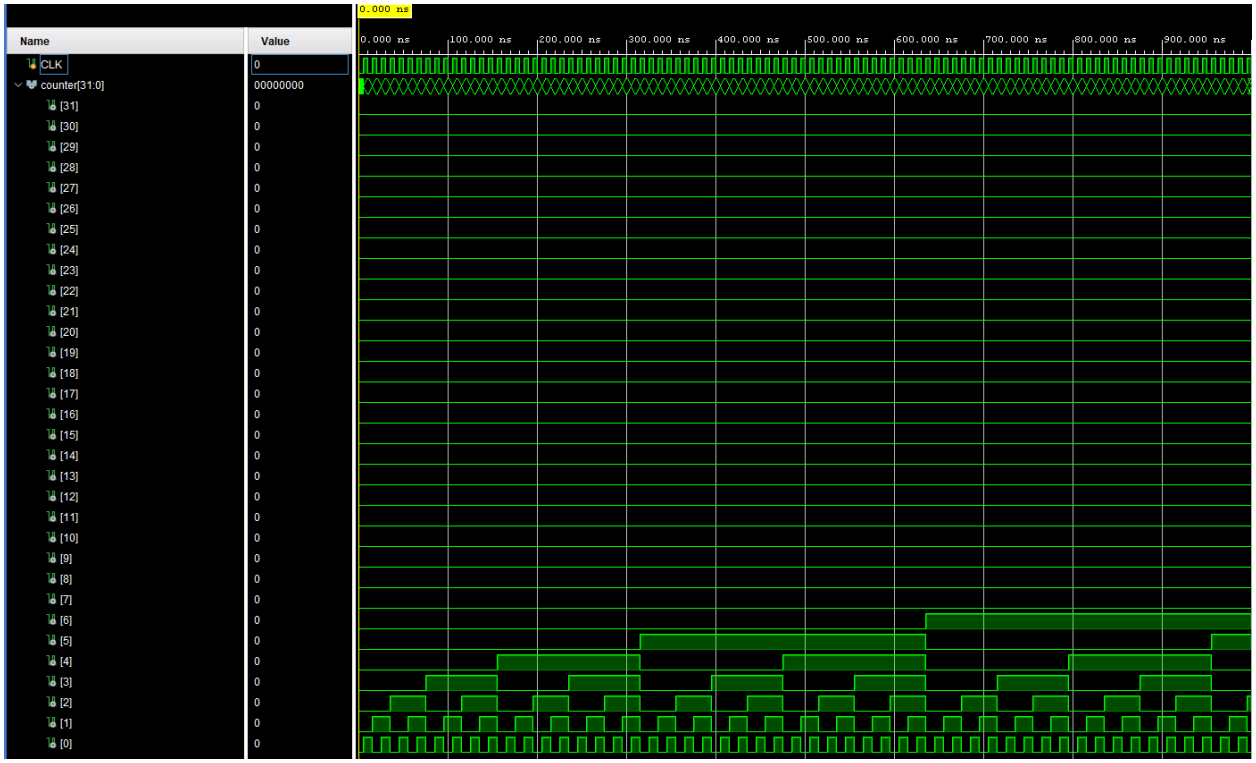


bcd_up_down_counter_tb



clock_divider_tb





Group Video Link

https://www.youtube.com/shorts/UqPRhE_WRYM

Reflection

This lab reinforced the importance of modular design and signal timing in FPGA-based digital systems. Implementing the BCD up-down counter required careful coordination between the clock divider, the counter logic, and the seven-segment scan driver. One of the key challenges we faced was ensuring the correct operation of the counters, particularly detecting the exact rollover and borrow conditions when transitioning between digits. Debugging with LEDs helped verify the internal logic before relying solely on the seven-segment display. Another critical aspect was understanding how clock division and multiplexing interact, especially when adjusting counting speeds using the switch-controlled multiplexer. Overall, this project deepened our skills in coding, simulating, and debugging Verilog designs and gave us practical experience with integrating hardware modules on the Nexys A7 FPGA.

Partner Contribution

Sean Go - code, lab report, video demonstration
Ryan Tran - code, lab report