Cal Poly
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ECE3300L

Experiment #2

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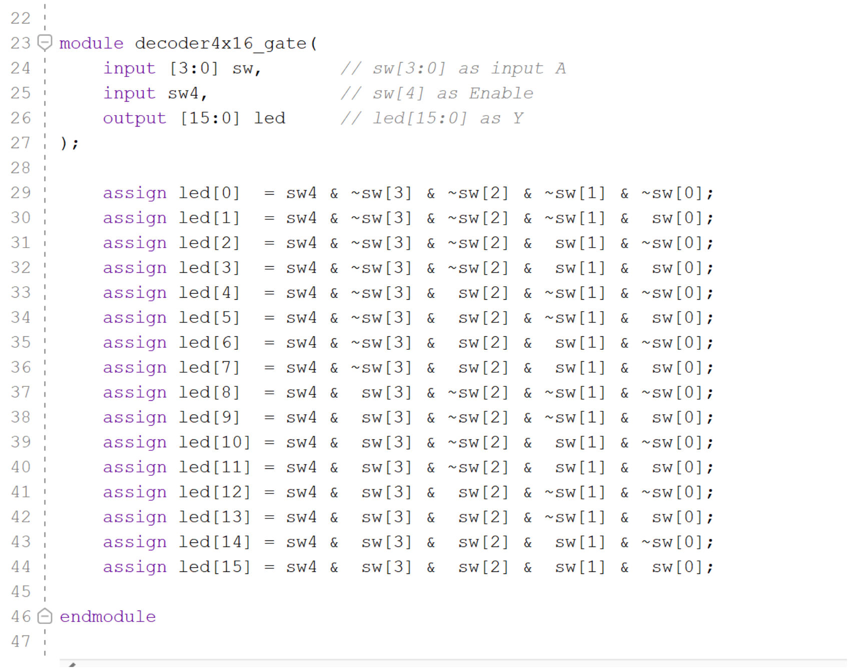
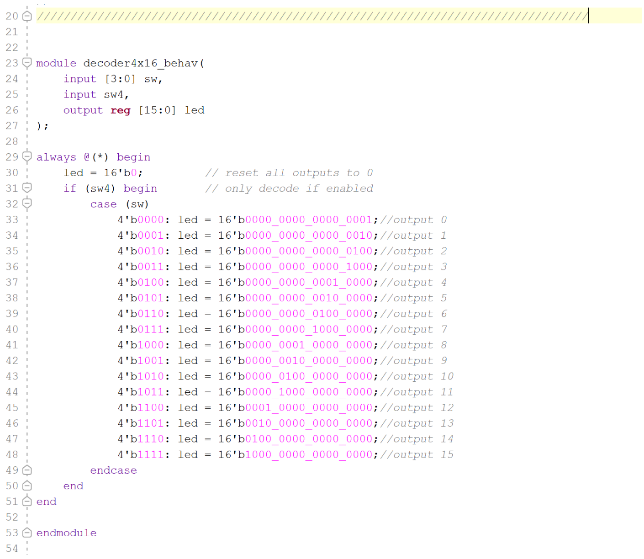
Introduction: The purpose of this lab is to design and implement a 4-to-16 line decoder with an enable signal using Verilog HDL on the Digilent Nexys A7-100T FPGA development board. When the enable input is active, the decoder asserts one of the sixteen outputs corresponding to the 4-bit binary input. When the enable input is disabled, all outputs remain low.

Design (Initializing Gates):



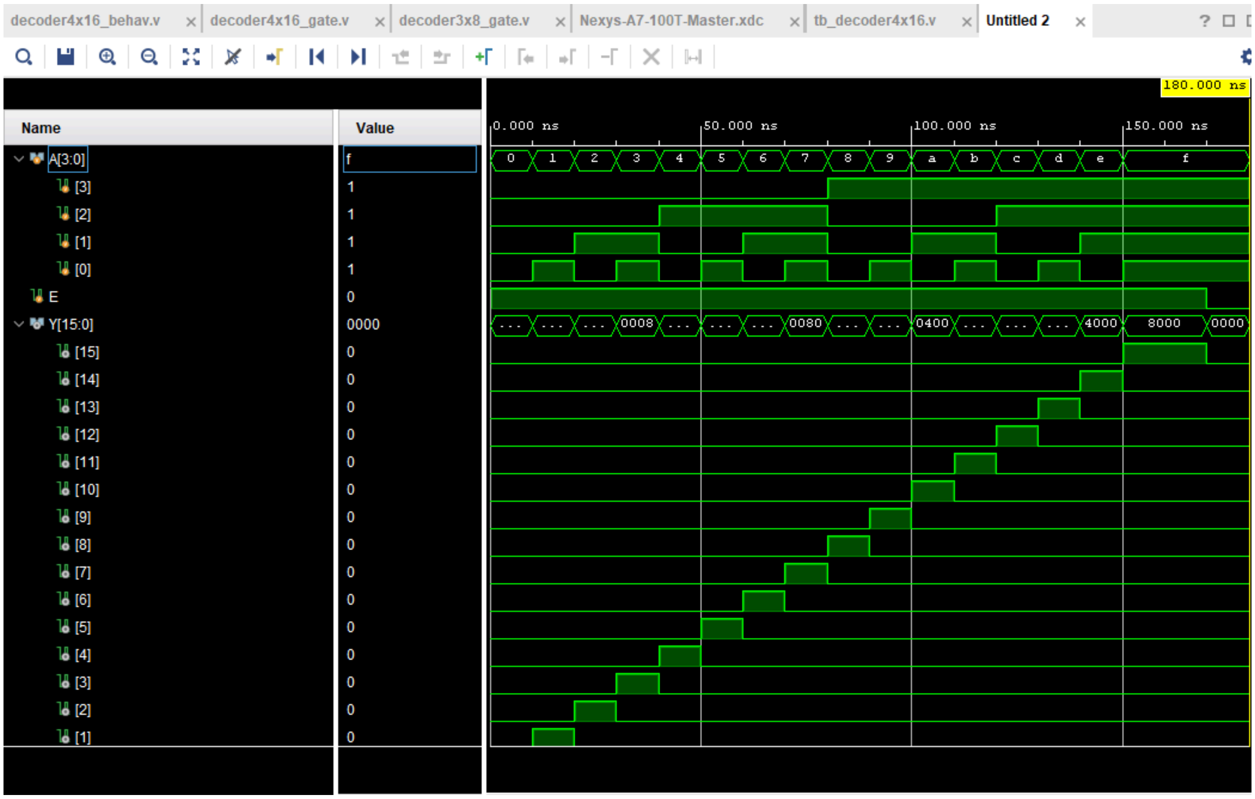
```

module decoder4x16_gate(
    input  [3:0] sw,        // sw[3:0] as input A
    input sw4,              // sw[4] as Enable
    output [15:0] led       // led[15:0] as Y
);

    assign led[0]  = sw4 & ~sw[3] & ~sw[2] & ~sw[1] & ~sw[0];
    assign led[1]  = sw4 & ~sw[3] & ~sw[2] & ~sw[1] &  sw[0];
    assign led[2]  = sw4 & ~sw[3] & ~sw[2] &  sw[1] & ~sw[0];
    assign led[3]  = sw4 & ~sw[3] & ~sw[2] &  sw[1] &  sw[0];
    assign led[4]  = sw4 & ~sw[3] &  sw[2] & ~sw[1] & ~sw[0];
    assign led[5]  = sw4 & ~sw[3] &  sw[2] & ~sw[1] &  sw[0];
    assign led[6]  = sw4 & ~sw[3] &  sw[2] &  sw[1] & ~sw[0];
    assign led[7]  = sw4 & ~sw[3] &  sw[2] &  sw[1] &  sw[0];
    assign led[8]  = sw4 &  sw[3] & ~sw[2] & ~sw[1] & ~sw[0];
    assign led[9]  = sw4 &  sw[3] & ~sw[2] & ~sw[1] &  sw[0];
    assign led[10] = sw4 &  sw[3] & ~sw[2] &  sw[1] & ~sw[0];
    assign led[11] = sw4 &  sw[3] & ~sw[2] &  sw[1] &  sw[0];
    assign led[12] = sw4 &  sw[3] &  sw[2] & ~sw[1] & ~sw[0];
    assign led[13] = sw4 &  sw[3] &  sw[2] & ~sw[1] &  sw[0];
    assign led[14] = sw4 &  sw[3] &  sw[2] &  sw[1] & ~sw[0];
    assign led[15] = sw4 &  sw[3] &  sw[2] &  sw[1] &  sw[0];

endmodule

```

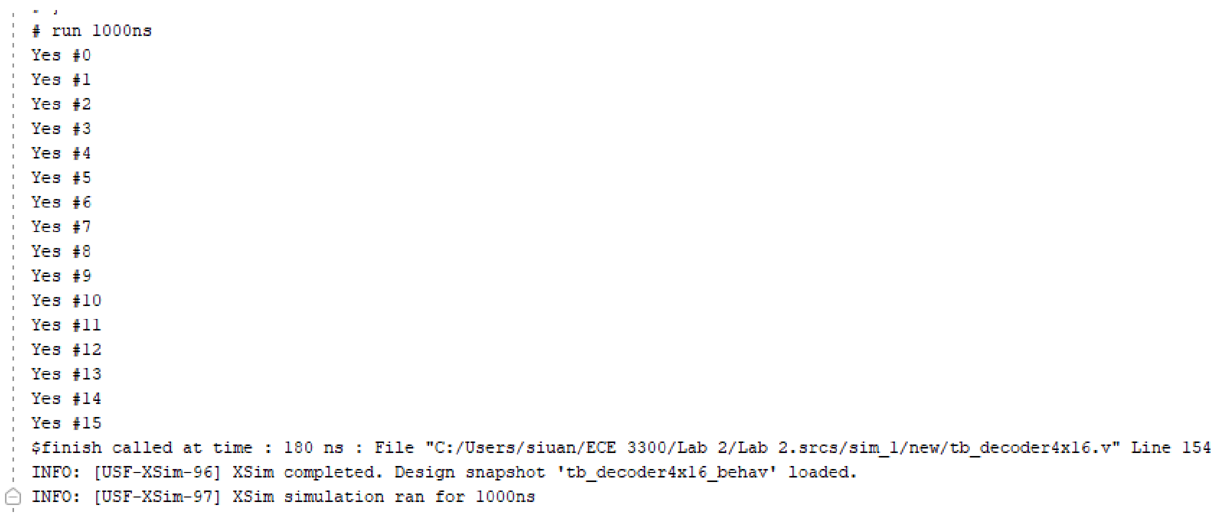
Design (Encoder Behavior):



```
////////////////////////////////////////////////////////////////////////////////


module decoder4x16_behav(
    input [3:0] sw,
    input sw4,
    output reg [15:0] led
);

always @(*) begin
    led = 16'b0;            // reset all outputs to 0
    if (sw4) begin          // only decode if enabled
        case (sw)
            4'b0000: led = 16'b0000_0000_0000_0001;//output 0
            4'b0001: led = 16'b0000_0000_0000_0010;//output 1
            4'b0010: led = 16'b0000_0000_0000_0100;//output 2
            4'b0011: led = 16'b0000_0000_0000_1000;//output 3
            4'b0100: led = 16'b0000_0000_0001_0000;//output 4
            4'b0101: led = 16'b0000_0000_0010_0000;//output 5
            4'b0110: led = 16'b0000_0000_0100_0000;//output 6
            4'b0111: led = 16'b0000_0000_1000_0000;//output 7
            4'b1000: led = 16'b0000_0001_0000_0000;//output 8
            4'b1001: led = 16'b0000_0010_0000_0000;//output 9
            4'b1010: led = 16'b0000_0100_0000_0000;//output 10
            4'b1011: led = 16'b0000_1000_0000_0000;//output 11
            4'b1100: led = 16'b0001_0000_0000_0000;//output 12
            4'b1101: led = 16'b0010_0000_0000_0000;//output 13
            4'b1110: led = 16'b0100_0000_0000_0000;//output 14
            4'b1111: led = 16'b1000_0000_0000_0000;//output 15
        endcase
    end
end

endmodule

```

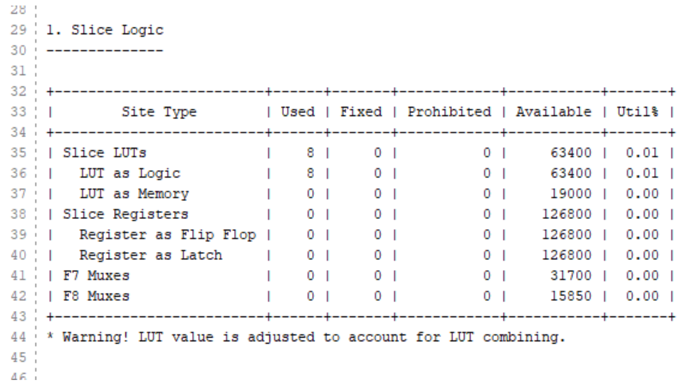
Simulation:



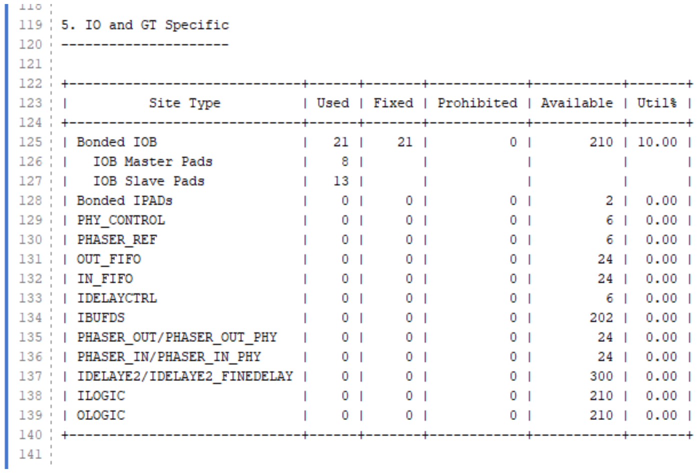


```
# run 1000ns
Yes #0
Yes #1
Yes #2
Yes #3
Yes #4
Yes #5
Yes #6
Yes #7
Yes #8
Yes #9
Yes #10
Yes #11
Yes #12
Yes #13
Yes #14
Yes #15
$finish called at time : 180 ns : File "C:/Users/siuan/ECE 3300/Lab 2/Lab 2.srcs/sim_1/new/tb_decoder4x16.v" Line 154
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_decoder4x16_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

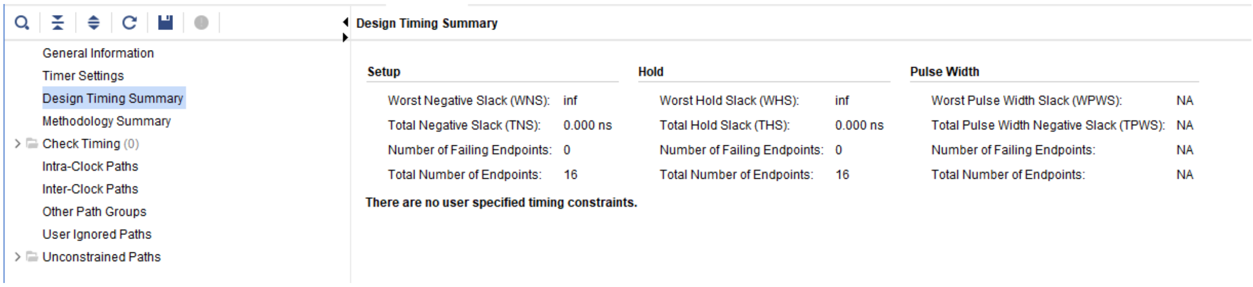
Implementation:



```
1. Slice Logic
--------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs              |    8 |     0 |          0 |     63400 |  0.01 |
|   LUT as Logic          |    8 |     0 |          0 |     63400 |  0.01 |
|   LUT as Memory         |    0 |     0 |          0 |     19000 |  0.00 |
| Slice Registers         |    0 |     0 |          0 |    126800 |  0.00 |
|   Register as Flip Flop |    0 |     0 |          0 |    126800 |  0.00 |
|   Register as Latch     |    0 |     0 |          0 |    126800 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     31700 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     15850 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
* Warning! LUT value is adjusted to account for LUT combining.
```



```
5. IO and GT Specific
--------------------

+-----------------------------+------+-------+------------+-----------+-------+
|          Site Type          | Used | Fixed | Prohibited | Available | Util% |
+-----------------------------+------+-------+------------+-----------+-------+
| Bonded IOB                  |   21 |    21 |          0 |       210 | 10.00 |
|   IOB Master Pads           |    8 |       |            |           |       |
|   IOB Slave Pads            |   13 |       |            |           |       |
| Bonded IPADs                |    0 |     0 |          0 |         2 |  0.00 |
| PHY_CONTROL                 |    0 |     0 |          0 |         6 |  0.00 |
| PHASER_REF                  |    0 |     0 |          0 |         6 |  0.00 |
| OUT_FIFO                    |    0 |     0 |          0 |        24 |  0.00 |
| IN_FIFO                     |    0 |     0 |          0 |        24 |  0.00 |
| IDELAYCTRL                  |    0 |     0 |          0 |         6 |  0.00 |
| IBUFDS                      |    0 |     0 |          0 |       202 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY   |    0 |     0 |          0 |        24 |  0.00 |
| PHASER_IN/PHASER_IN_PHY     |    0 |     0 |          0 |        24 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |    0 |     0 |          0 |       300 |  0.00 |
| ILOGIC                      |    0 |     0 |          0 |       210 |  0.00 |
| OLOGIC                      |    0 |     0 |          0 |       210 |  0.00 |
+-----------------------------+------+-------+------------+-----------+-------+
```



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	16	Total Number of Endpoints:	16	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Video Link: https://youtube.com/shorts/Re0NGSusW10 (51 seconds)

Contributions:

Andy Siu: 50%

Dalton Hoang: 50%