

ECE 3300L

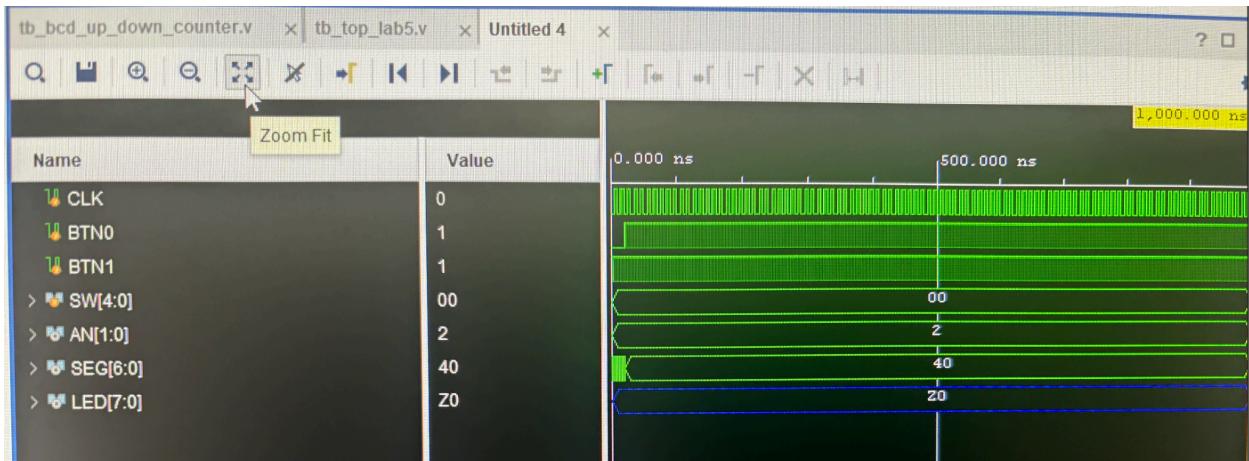
Lab 5 - BCD Up/Down Counter on 7-Segment Display

Raj Gokidi and Priyanka Ravinder

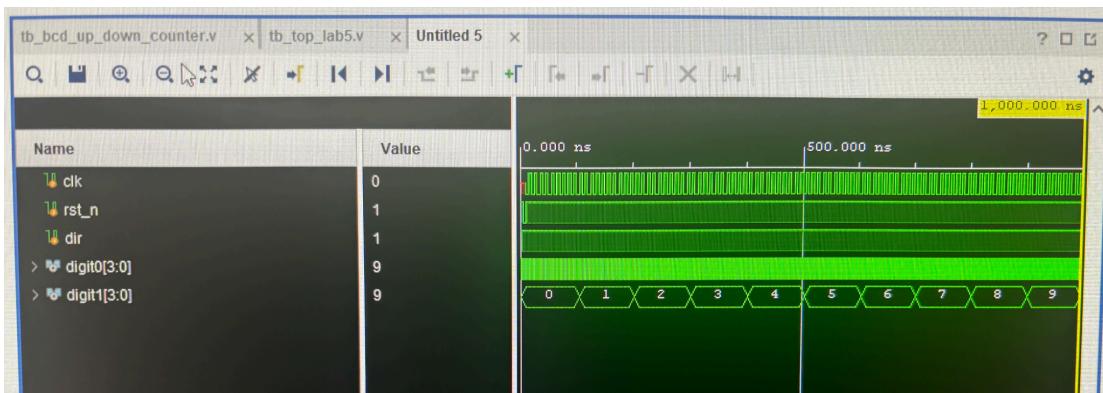
7/21/25

Waveforms

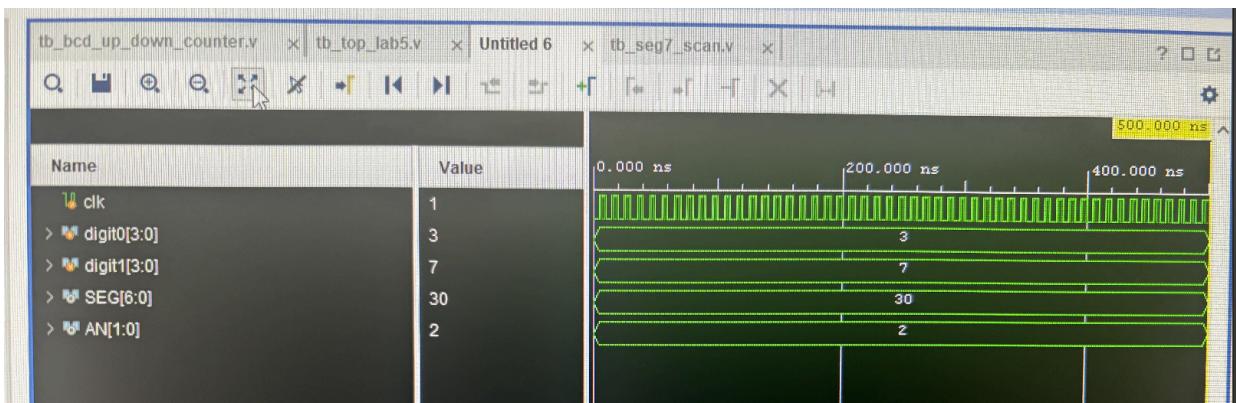
top_lab5 waveform



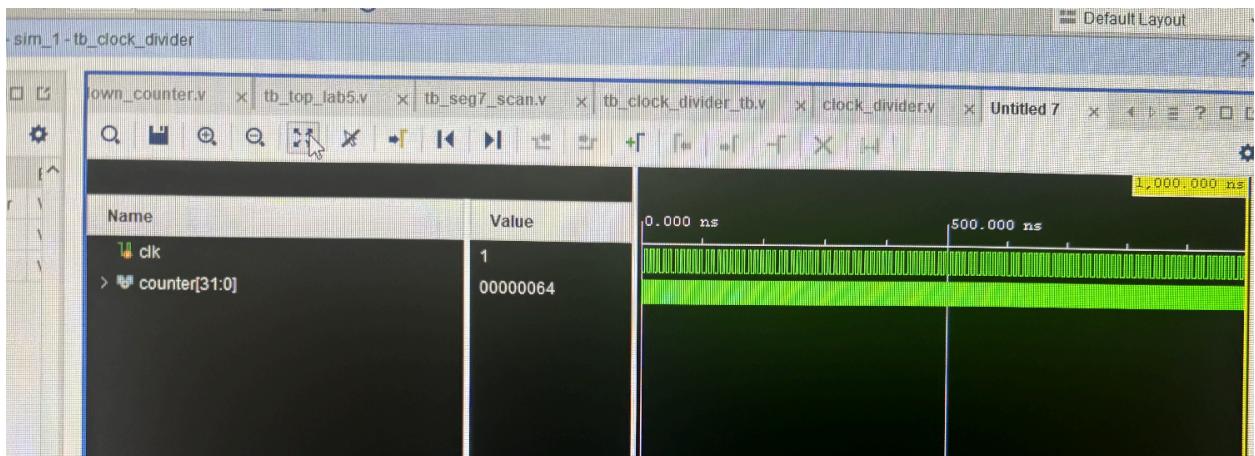
bcd_up_down_counter waveform



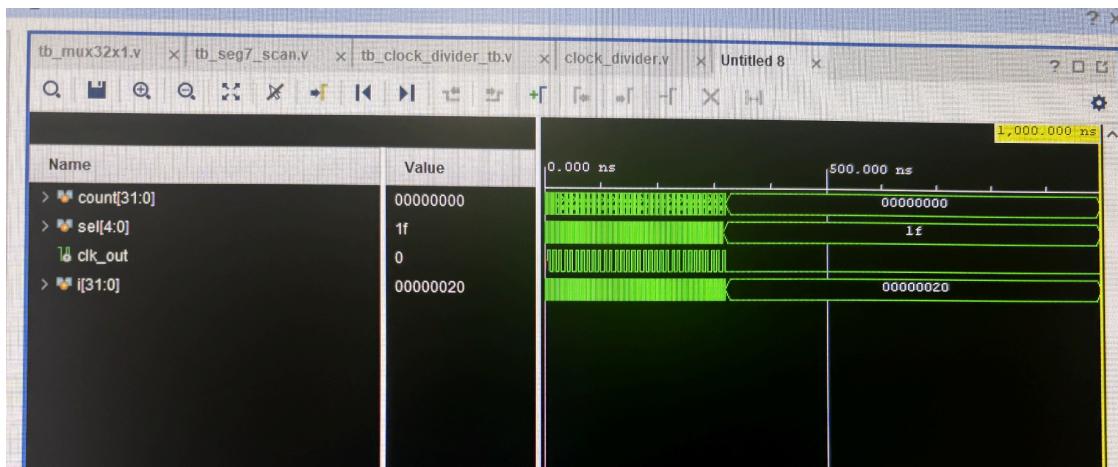
seg7_scan waveform



clock_divider waveform



mux32x1 waveform



LUT and FF

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27
28 1. Slice Logic
29 -----
30
31 +-----+-----+-----+-----+
32 | Site Type | Used | Fixed | Prohibited | Available | Util% |
33 +-----+-----+-----+-----+
34 | Slice LUTs* | 26 | 0 | 0 | 63400 | 0.04 |
35 | LUT as Logic | 26 | 0 | 0 | 63400 | 0.04 |
36 | LUT as Memory | 0 | 0 | 0 | 19000 | 0.00 |
37 | Slice Registers | 59 | 0 | 0 | 126800 | 0.05 |
38 | Register as Flip Flop | 59 | 0 | 0 | 126800 | 0.05 |
39 | Register as Latch | 0 | 0 | 0 | 126800 | 0.00 |
40 | F7 Muxes | 4 | 0 | 0 | 31700 | 0.01 |
41 | F8 Muxes | 0 | 0 | 0 | 15850 | 0.00 |
42 +-----+-----+-----+-----+
43 * Warning! The Final LUT count, after physical optimizations and full implementat
44 Warning! LUT value is adjusted to account for LUT combining.
45 Warning! For any ECO changes, please run place_design if there are unplaced ...
46

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Contributions:

Raj Gokidi (50%) - testbench code, demo, report

Priyanka Ravinder (50%) - verilog, implementation

Video link: <https://youtu.be/axOFM7bgF8Y>

Reflection:

This lab gave us hands-on practice building a BCD counter. We learned how key clock division and good sync are when working with real hardware. Fixing display multiplexing and counter rollover issues helped us better get sequential logic.