ECE3300L Lab 7

16-bit Barrel Shifter / Rotator &
4-Digit 7-Segment Display

Group X
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Objective:

The goal of this lab is to build a 16-bit barrel shifter and rotator displayed on four hexadecimal digits of a 7-segment display. It uses a fixed clock divider to generate both ~2 Hz for visible shifting and ~1 kHz for display scanning, and a tree of 2-to-1 multiplexers driven by a 4-bit shift-amount input to perform arbitrary left/right logical shifts or rotations . A push-button toggles the shift direction, another toggles between logical shift and rotate modes, and the center push-button resets the shifter. Debug LEDs LED7–LED0 light up to display the DIR, ROT, and SHAMT bits corresponding to the current shift settings.

Top Display Module:

```
`timescale 1ns / 1ps

module top_lab7(
                input wire clk,
                input wire [15:0] SW,
                input btnU, btnD, btnL, btnR, btnC,
                output wire [7:0] LED,
                output wire [6:0] seg,
                output wire [7:0] an
                );

                wire clk_2khz, clk_1khz;
                clock_divider_fixed clkdiv(.clk(clk), .clk_2khz(clk_2khz), .clk_1khz(clk_1khz));

                wire dir_toggle, rot_toggle, shamt0_toggle, shamt1_toggle;
                debounce_toggle dir(.clk_1khz(clk_1khz), .btn_raw(btnU), .toggle(dir_toggle));
                debounce_toggle rot(.clk_1khz(clk_1khz), .btn_raw(btnD), .toggle(rot_toggle));
                debounce_toggle shamt0(.clk_1khz(clk_1khz), .btn_raw(btnL), .toggle(shamt0_toggle));
                debounce_toggle shamt1(.clk_1khz(clk_1khz), .btn_raw(btnR), .toggle(shamt1_toggle));

                wire [1:0] shamt_high;
                shamt_counter count(.clk(clk_1khz), .btnc(btnC), .shamt_high(shamt_high));

                wire [3:0] shamt = {shamt_high, shamt1_toggle, shamt0_toggle};

                wire [15:0] barrel_out;
                barrel_shifter16 barrel(
                                        .DATA_IN(SW),
                                        .SHAMT(shamt),
                                        .DIR(dir_toggle),
                                        .ROTATE(rot_toggle),
                                        .DATA_OUT(barrel_out)
                                        );
```

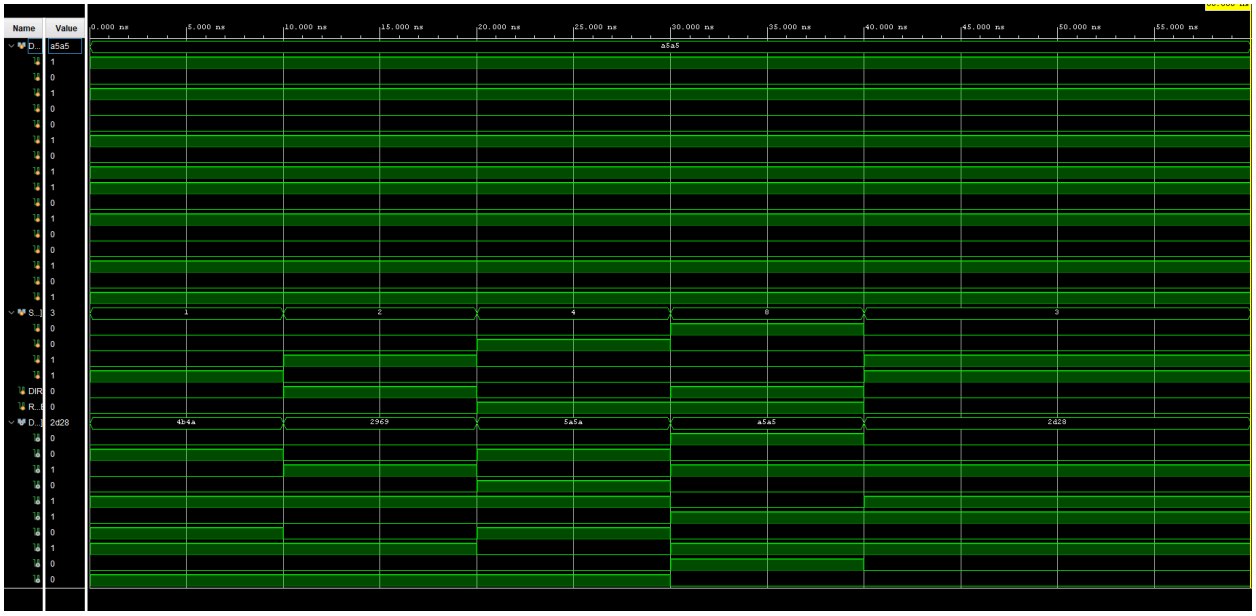
```
34
35                  wire [6:0] seg0, seg1, seg2, seg3;
36                  hex_to_7seg h0(.hex(barrel_out[3:0]), .seg(seg0));
37                  hex_to_7seg h1(.hex(barrel_out[7:4]), .seg(seg1));
38                  hex_to_7seg h2(.hex(barrel_out[11:8]), .seg(seg2));
39                  hex_to_7seg h3(.hex(barrel_out[15:12]), .seg(seg3));
40
41                  wire [6:0] blank = 7'b1111111;
42                  seg7_scan8 scanner(
43                                      .clk_1khz(clk_1khz),
44                                      .seg0(seg0),
45                                      .seg1(seg1),
46                                      .seg2(seg2),
47                                      .seg3(seg3),
48                                      .seg4(blank),
49                                      .seg5(blank),
50                                      .seg6(blank),
51                                      .seg7(blank),
52                                      .an(an),
53                                      .seg(seg)
54                                     );
55
56                   assign LED[7:0] = {2'b00, shamt, rot_toggle, dir_toggle};
57
58  endmodule
```

XDC File:

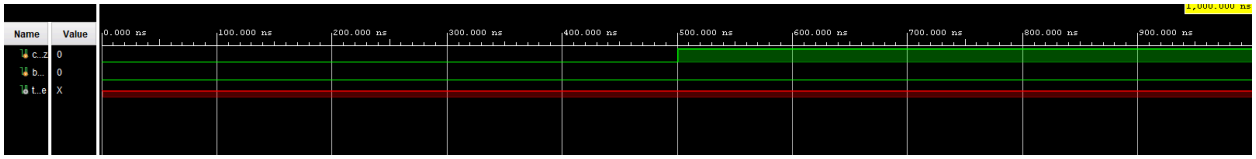
```
# Clock signal
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clk }]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {clk}];


##Switches

set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { SW[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { SW[1] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { SW[2] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { SW[3] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { SW[4] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { SW[5] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { SW[6] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { SW[7] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS18 } [get_ports { SW[8] }]; #IO_L24N_T3_34 Sch=sw[8]
set_property -dict { PACKAGE_PIN U8    IOSTANDARD LVCMOS18 } [get_ports { SW[9] }]; #IO_25_34 Sch=sw[9]
set_property -dict { PACKAGE_PIN R16   IOSTANDARD LVCMOS33 } [get_ports { SW[10] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[10]
set_property -dict { PACKAGE_PIN T13   IOSTANDARD LVCMOS33 } [get_ports { SW[11] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]
set_property -dict { PACKAGE_PIN H6    IOSTANDARD LVCMOS33 } [get_ports { SW[12] }]; #IO_L24P_T3_35 Sch=sw[12]
set_property -dict { PACKAGE_PIN U12   IOSTANDARD LVCMOS33 } [get_ports { SW[13] }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
set_property -dict { PACKAGE_PIN U11   IOSTANDARD LVCMOS33 } [get_ports { SW[14] }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { SW[15] }]; #IO_L21P_T3_DQS_14 Sch=sw[15]


## LEDs

set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports { LED[0] }]; #IO_L18P_T2_A24_15 Sch=led[0]
set_property -dict { PACKAGE_PIN K15   IOSTANDARD LVCMOS33 } [get_ports { LED[1] }]; #IO_L24P_T3_RS1_15 Sch=led[1]
set_property -dict { PACKAGE_PIN J13   IOSTANDARD LVCMOS33 } [get_ports { LED[2] }]; #IO_L17N_T2_A25_15 Sch=led[2]
set_property -dict { PACKAGE_PIN N14   IOSTANDARD LVCMOS33 } [get_ports { LED[3] }]; #IO_L8P_T1_D11_14 Sch=led[3]
set_property -dict { PACKAGE_PIN R18   IOSTANDARD LVCMOS33 } [get_ports { LED[4] }]; #IO_L7P_T1_D09_14 Sch=led[4]
set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports { LED[5] }]; #IO_L18N_T2_A11_D27_14 Sch=led[5]
set_property -dict { PACKAGE_PIN U17   IOSTANDARD LVCMOS33 } [get_ports { LED[6] }]; #IO_L17P_T2_A14_D30_14 Sch=led[6]
set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get ports { LED[7] }]; #IO L18P T2 A12 D28 14 Sch=led[7]

#7 segment display

set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports {  seg[0] }]; #IO_L24N_T3_A00_D16_14 Sch=ca
set_property -dict { PACKAGE_PIN R10   IOSTANDARD LVCMOS33 } [get_ports {  seg[1] }]; #IO_25_14 Sch=cb
set_property -dict { PACKAGE_PIN K16   IOSTANDARD LVCMOS33 } [get_ports {  seg[2] }]; #IO_25_15 Sch=cc
set_property -dict { PACKAGE_PIN K13   IOSTANDARD LVCMOS33 } [get_ports {  seg[3] }]; #IO_L17P_T2_A26_15 Sch=cd
set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCMOS33 } [get_ports {  seg[4] }]; #IO_L13P_T2_MRCC_14 Sch=ce
set_property -dict { PACKAGE_PIN T11   IOSTANDARD LVCMOS33 } [get_ports {  seg[5] }]; #IO_L19P_T3_A10_D26_14 Sch=cf
set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports {  seg[6] }]; #IO_L4P_T0_D04_14 Sch=cg

#set_property -dict { PACKAGE_PIN H15   IOSTANDARD LVCMOS33 } [get_ports { dp }]; #IO_L19N_T3_A21_VREF_15 Sch=dp

set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports { an[0] }]; #IO_L23P_T3_FOE_B_15 Sch=an[0]
set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports { an[1] }]; #IO_L23N_T3_FWE_B_15 Sch=an[1]
set_property -dict { PACKAGE_PIN T9    IOSTANDARD LVCMOS33 } [get_ports { an[2] }]; #IO_L24P_T3_A01_D17_14 Sch=an[2]
set_property -dict { PACKAGE_PIN J14   IOSTANDARD LVCMOS33 } [get_ports { an[3] }]; #IO_L19P_T3_A22_15 Sch=an[3]
set_property -dict { PACKAGE_PIN P14   IOSTANDARD LVCMOS33 } [get_ports { an[4] }]; #IO_L8N_T1_D12_14 Sch=an[4]
set_property -dict { PACKAGE_PIN T14   IOSTANDARD LVCMOS33 } [get_ports { an[5] }]; #IO_L14P_T2_SRCC_14 Sch=an[5]
set_property -dict { PACKAGE_PIN K2    IOSTANDARD LVCMOS33 } [get_ports { an[6] }]; #IO_L23P_T3_35 Sch=an[6]
set_property -dict { PACKAGE_PIN U13   IOSTANDARD LVCMOS33 } [get_ports { an[7] }]; #IO_L23N_T3_A02_D18_14 Sch=an[7]


##Buttons

#set_property -dict { PACKAGE_PIN C12   IOSTANDARD LVCMOS33 } [get_ports { CPU_RESETN }]; #IO_L3P_T0_DQS_AD1P_15 Sch=cpu_resetn

set_property -dict { PACKAGE_PIN N17   IOSTANDARD LVCMOS33 } [get_ports { btnC }]; #IO_L9P_T1_DQS_14 Sch=btnc
set_property -dict { PACKAGE_PIN M18   IOSTANDARD LVCMOS33 } [get_ports { btnU }]; #IO_L4N_T0_D05_14 Sch=btnu
set_property -dict { PACKAGE_PIN P17   IOSTANDARD LVCMOS33 } [get_ports { btnL }]; #IO_L12P_T1_MRCC_14 Sch=btnl
set_property -dict { PACKAGE_PIN M17   IOSTANDARD LVCMOS33 } [get_ports { btnR }]; #IO_L10N_T1_D15_14 Sch=btnr
set_property -dict { PACKAGE_PIN P18   IOSTANDARD LVCMOS33 } [get_ports { btnD }]; #IO_L9N_T1_DQS_D13_14 Sch=btnd
```

Test Benches:

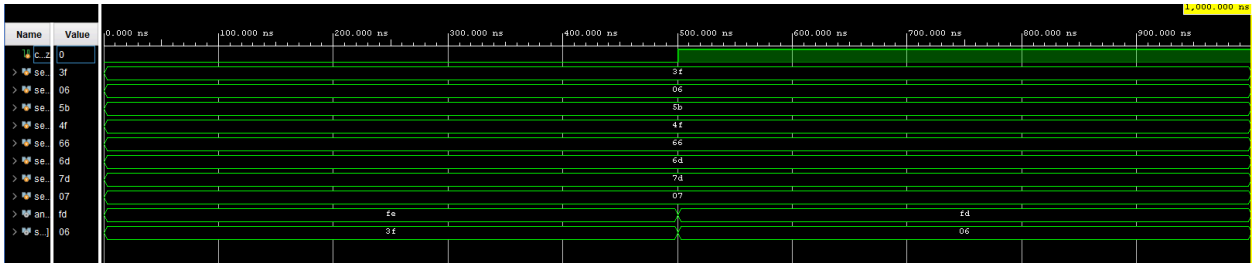
barrel_shifter16_tb:



debounce_toggle_tb:



seg7_scan8_tb:



Video Link:
https://youtube.com/shorts/k7fVS1Bpjj8?feature=share

Contributions:
Czyrone (50%) - Verilog code, Physical demo
Caleb (50%) - Testbenches
Both worked on the lab report together and troubleshooted code

Reflections:

This lab required more debugging than anticipated. The clock divider sometimes produced jittery pulses until fixing the reset synchronization. The button debounce occasionally mistoggled the direction and rotate signals, then we fixed the shift-register sampling depth. The 7-segment display showed faint ghost digits until they fixed the scan-timing logic and corrected pin assignments in the constraints file. Overall, these challenges reinforced the critical role of precise clock-domain isolation, debounce timing, and accurate pin mapping in FPGA design.