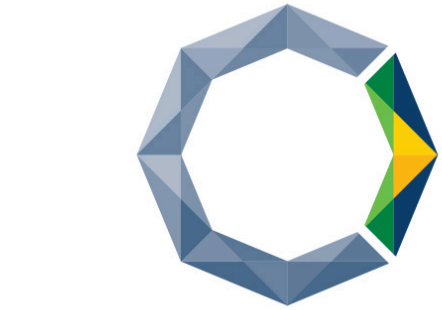


CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #8

Presented By: Kobe Aquino (StudentID: 015266433)

& Daniel Mondragon Xicotencatl (StudentID: 012803856)

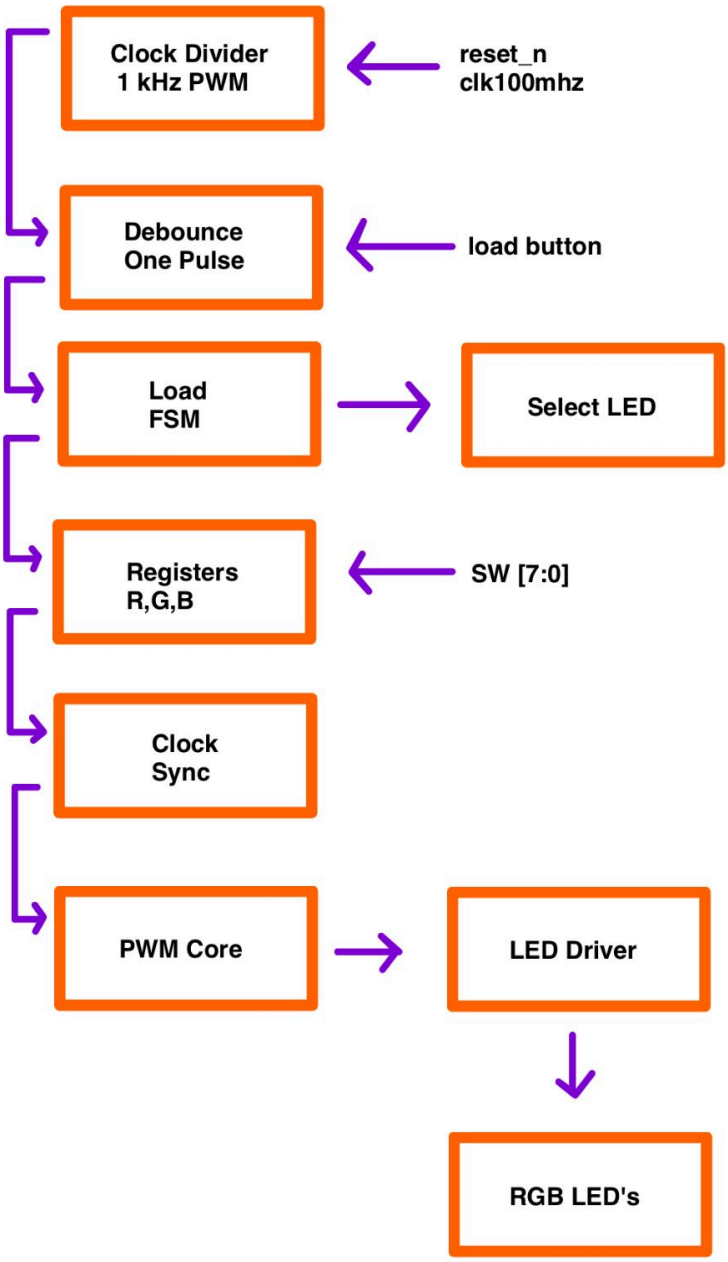
Presented to Mohamed Aly

August 14, 2025

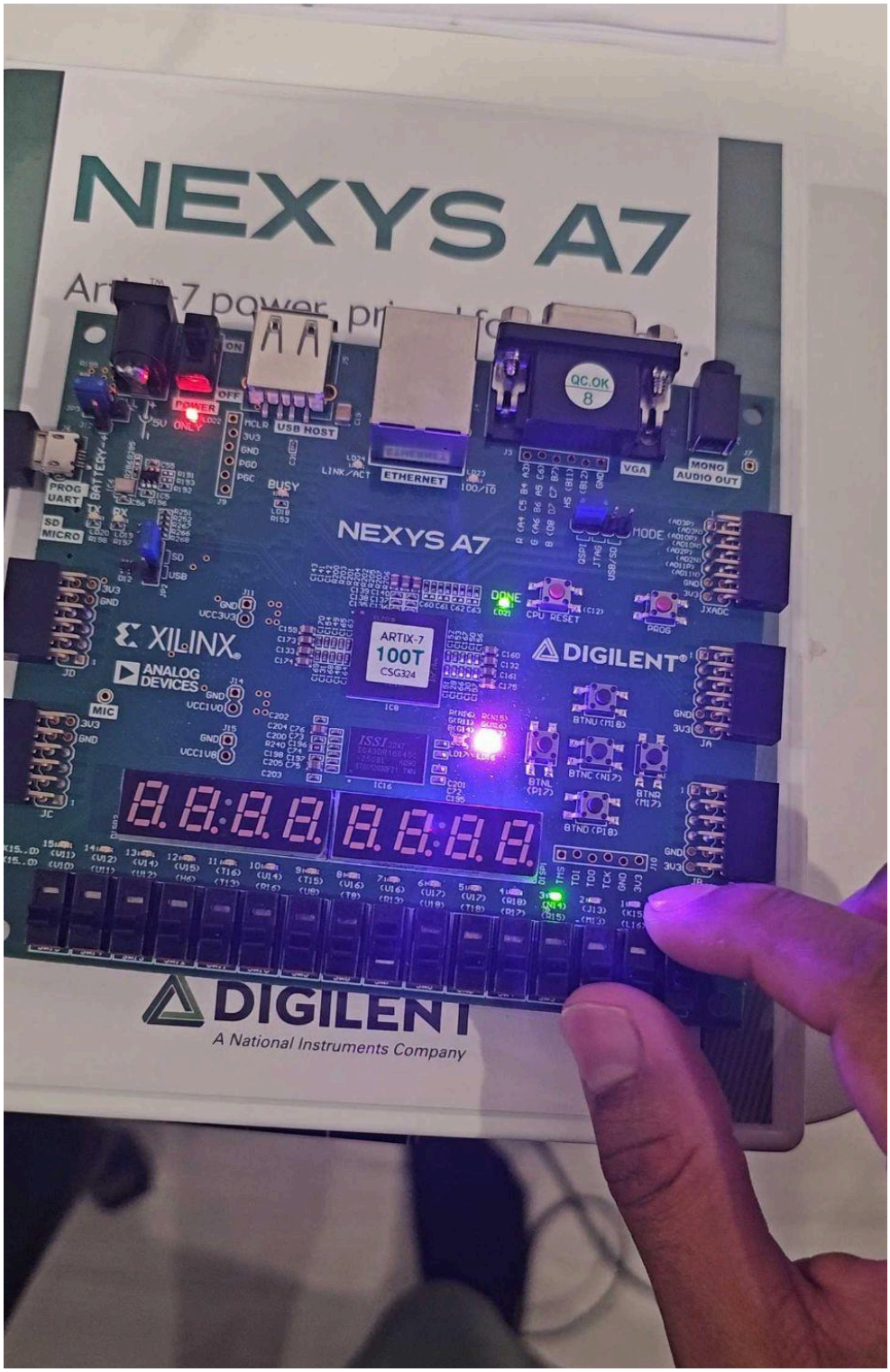
Short paragraph on 4-slot loading and RES + 1:

For this final lab we got the opportunity to delve into 4-slot loading and RES +1. We use one load button that has four different variations. The PWM Resolution that is labeled RES, and the cycles of Red, Green, and Blue. Each time we press the load button, the FSM rotates to the next option. Slot 0 is set as RES, Slot 1 is set as Red, Slot 2 as Green, and finally Slot 3 as blue. When it reaches Slot 3, it restarts and begins at Slot 0 creating an infinite loop. The RES+1 is needed because the actual value of RES is set as one lower than the real value period. So the +1 is needed to be set as the values to be considered in a cycle.

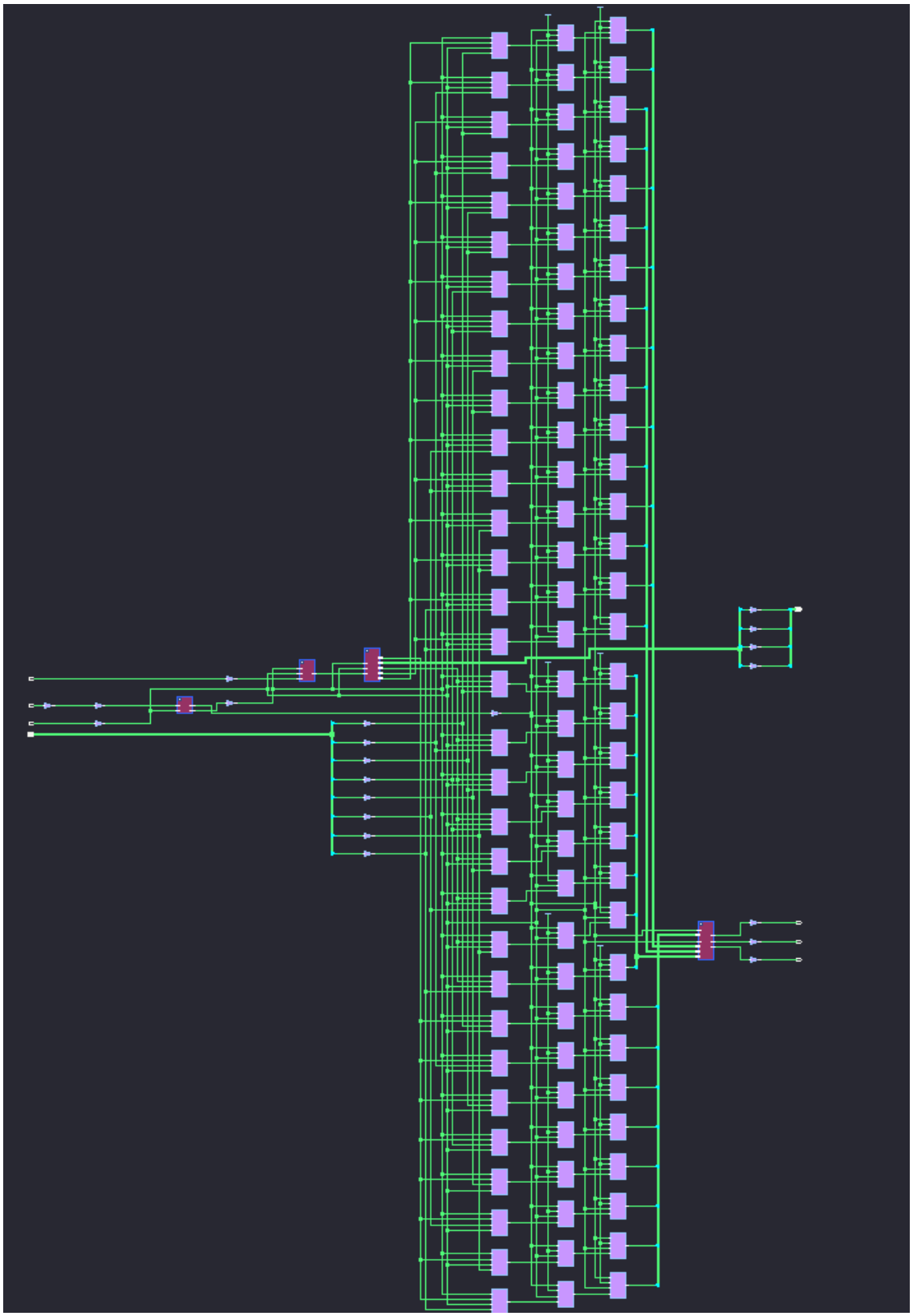
Block diagram:



Board photo:

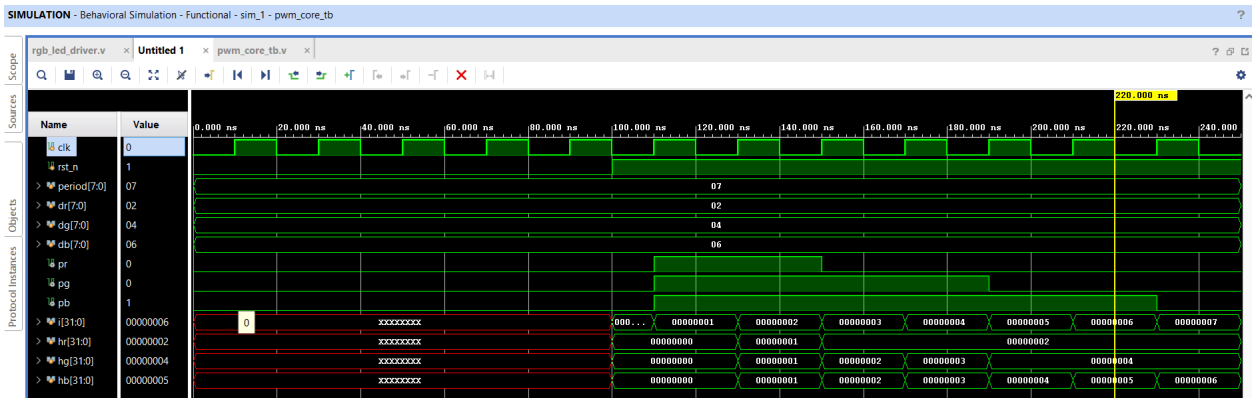

NEXYS A7
NEXYS A7
DIGILENT
A National Instruments Company
XILINX
ANALOG DEVICES
DIGILENT
ARTIX-7
100T
CSG324
ETHERNET
USB HOST
VGA
MONO AUDIO OUT
PROG UART
SD MICRO
MIC
CPU RESET
BTNU (M18)
BTNC (N17)
BTNL (P17)
BTND (M17)
BTND (P18)

Schematic:



Simulation:

pwm_core_tb.v



Team Contributions:

Daniel Mondragon Xicotencatl + 50%

Kobe Aquino + 50%

We both collaborated on the Verilog HDL code by troubleshooting the top_module to have it working correctly, as well as testing with simulations.