ECE 3300L

Lab Report #4

Group E

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Design:

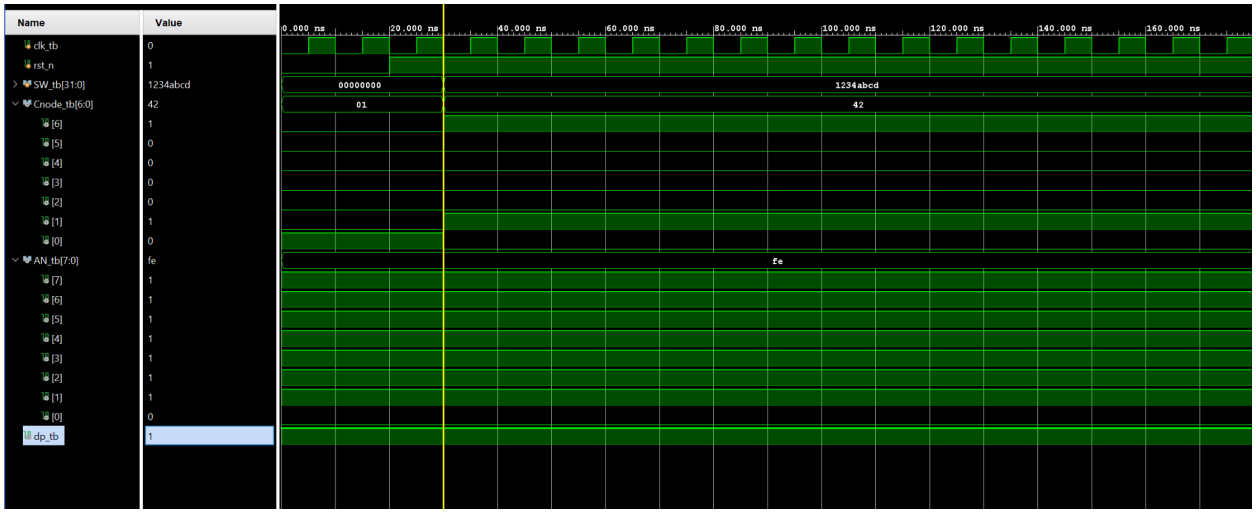
This lab uses the switches (SW[15:0]) as input and LEDs (LED[15:0]) to mirror their values. A Verilog source file (seg7_driver.v) is provided to control the 7-segment display through time-multiplexing. Each 4-bit chunk of the input is displayed as a corresponding hexadecimal digit.

Simulation:

We created a testbench file (seg7_driver_tb.v) to verify the design behavior. The test values used were: SW = 32'h1234ABCD, rst_n = 1, clk = toggled at 10ns.

```
module seg7_driver_tb;

  // Inputs
  reg clk_tb;
  reg rst_n;
  reg [31:0] SW_tb;

  // Outputs
  wire [6:0] Cnode_tb;
  wire [7:0] AN_tb;
  wire dp_tb;

  // Instantiate
  seg7_driver DUT (
    .clk(clk_tb),
    .rst_n(rst_n),
    .SW(SW_tb),
    .Cnode(Cnode_tb),
    .AN(AN_tb),
    .dp(dp_tb)
  );

  // 100 MHz clock (10 ns period)
  always #5 clk_tb = ~clk_tb;

  initial begin
    // Initialize signals
    clk_tb = 0;
    rst_n = 0;
    SW_tb = 32'h00000000;

    // Apply reset
    #20 rst_n = 1;

    // Apply switch input
    #10 SW_tb = 32'h1234ABCD;

    #100000;  // 100 us

    $display("Simulation finished.");
    $stop;
  end
endmodule
```

Waveform Screenshot:



Implementation:

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	14	0	0	63400	0.02
LUT as Logic	14	0	0	63400	0.02
LUT as Memory	0	0	0	19000	0.00
Slice Registers	20	0	0	126800	0.02
Register as Flip Flop	20	0	0	126800	0.02
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

Contributions:

Paul Kim - Testbench, Simulation - 50% contribution

Winson Zhu - Implementation, Hardware Demo - 50% contribution