ECE 3300L

California State Polytechnic University, Pomona

Group G

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Lab Report #4

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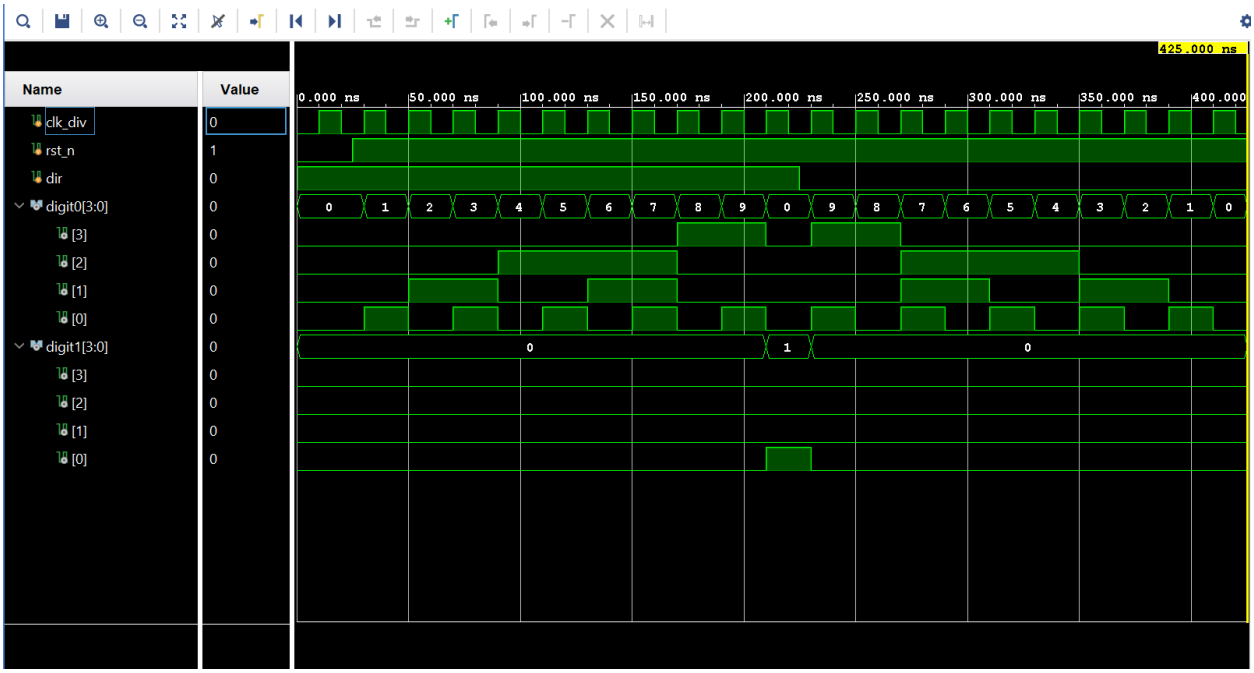
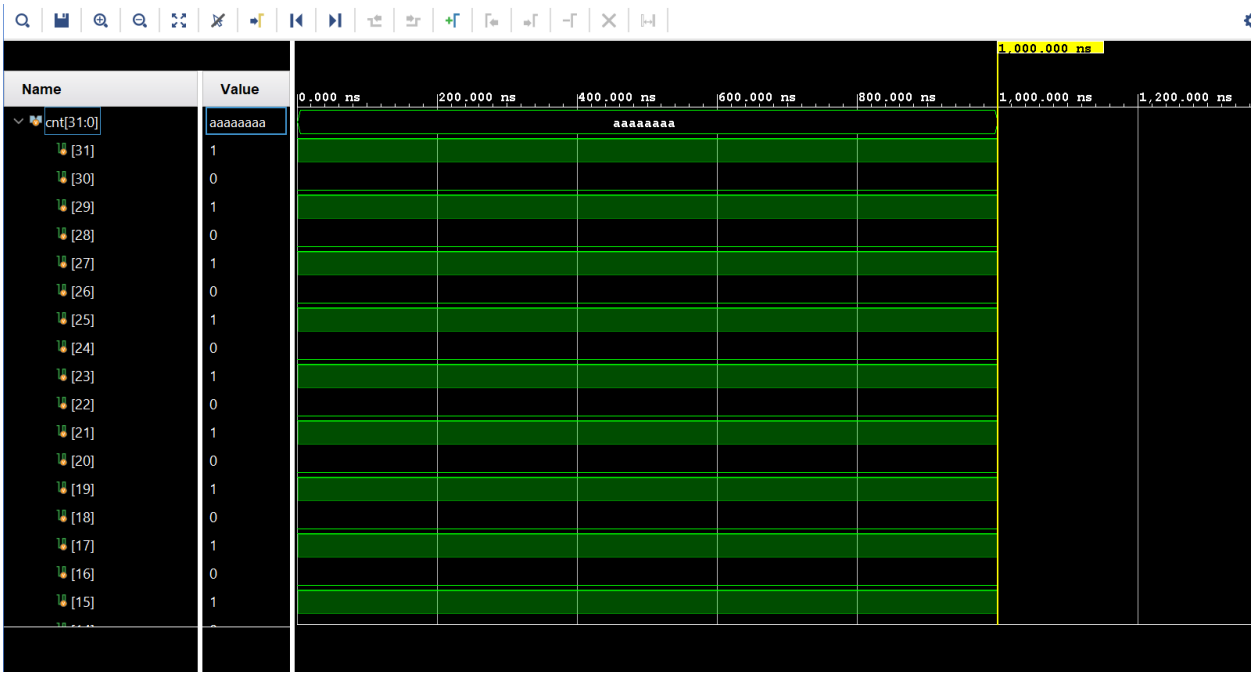
Explanation:

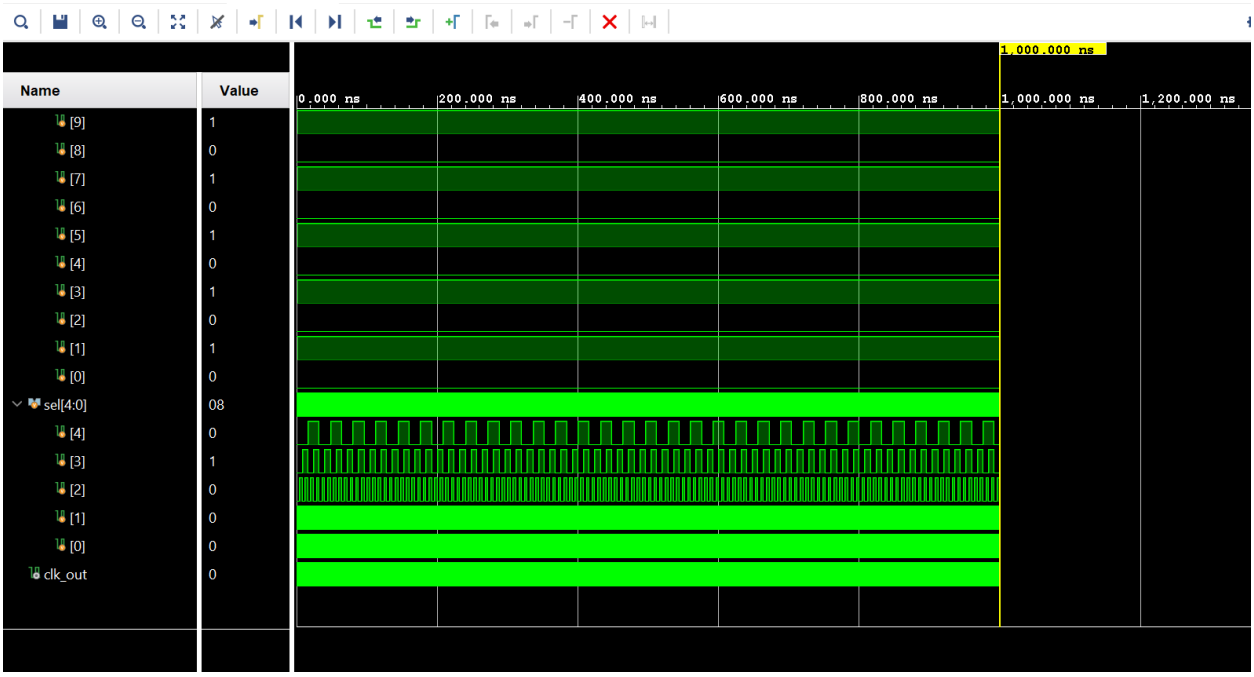
We designed a two-digit BCD up/down counter with the following modules. The clock_divider.v module implements a 32-bit free-running counter that increments on each positive edge of the 100 MHz clock. This makes a divided clock signal used to slow down the counting rate for the BCD counter. The mux32x1.v module is a 32-to-1 multiplexer that chooses one of the 32 bits from the clock divider counter based on the 5-bit switch input, where the selected bit is output as the divided clock used by the counter. The bcd_up_down_counter.v module holds a two-digit BCD up/down counter that uses cascading, which increments or decrements the digits based on the direction input and it also handles the carry/borrow between them. The seg7_scan.v module multiplexes the display of two BCD digits on a dual 7-segment display, which alternates enabling each digit and outputs the matching segment values.

BCD_up_down_counter:

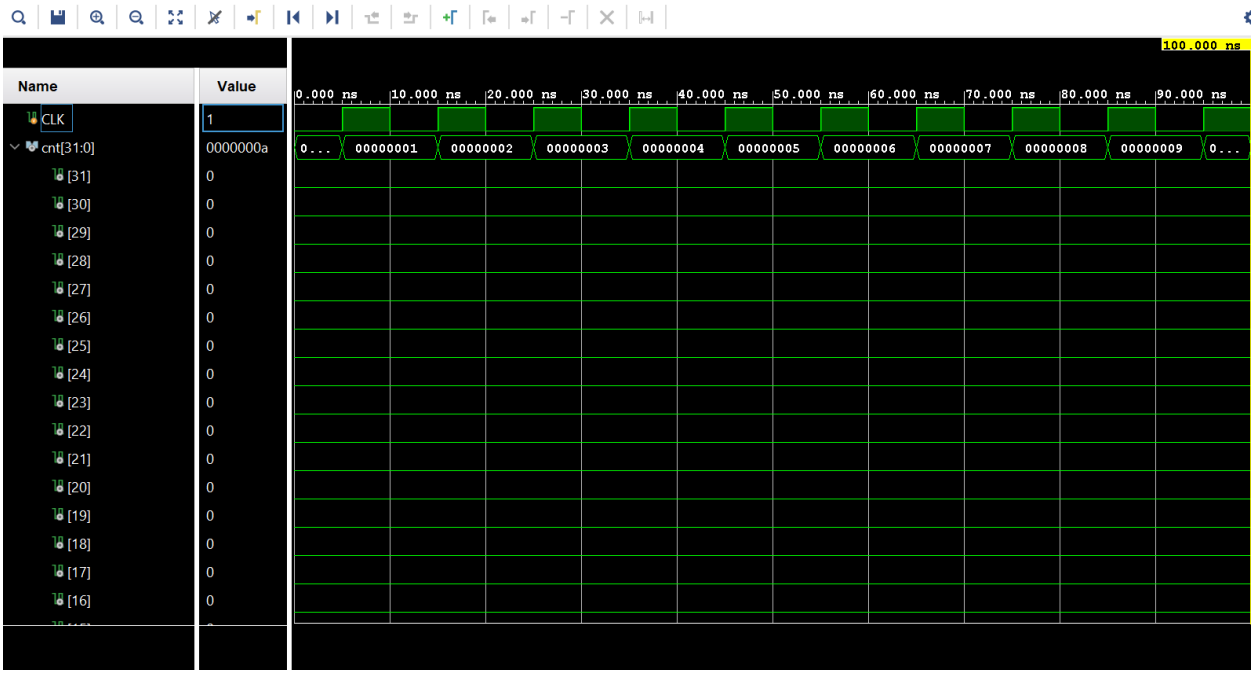


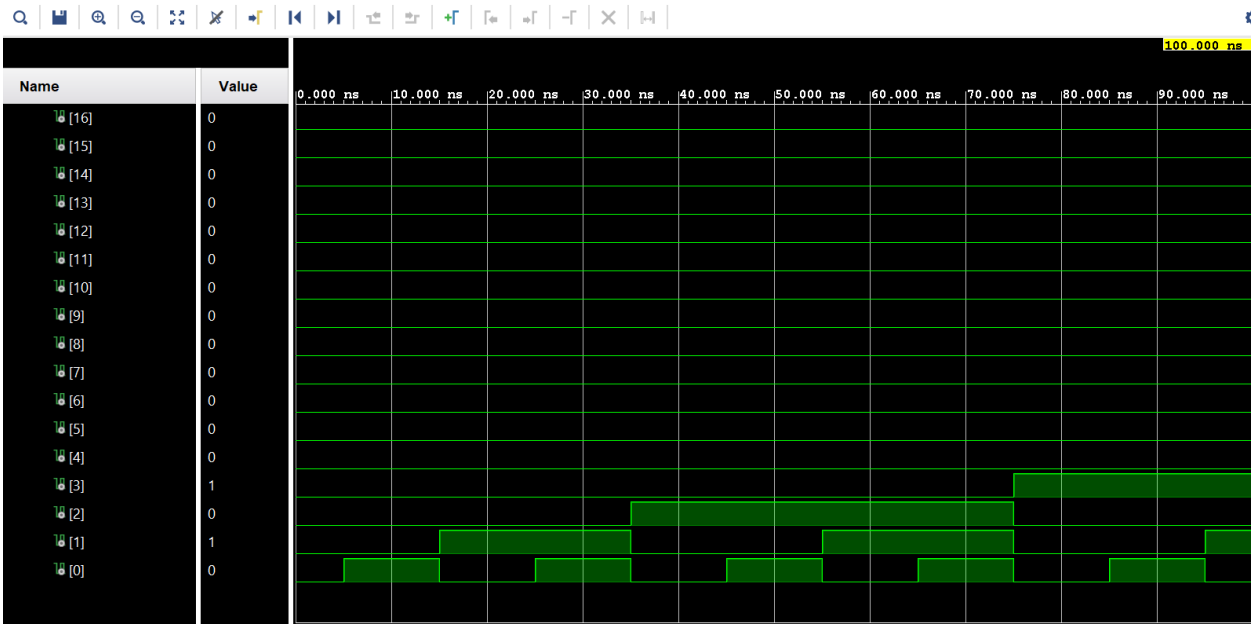
Mux32x1:



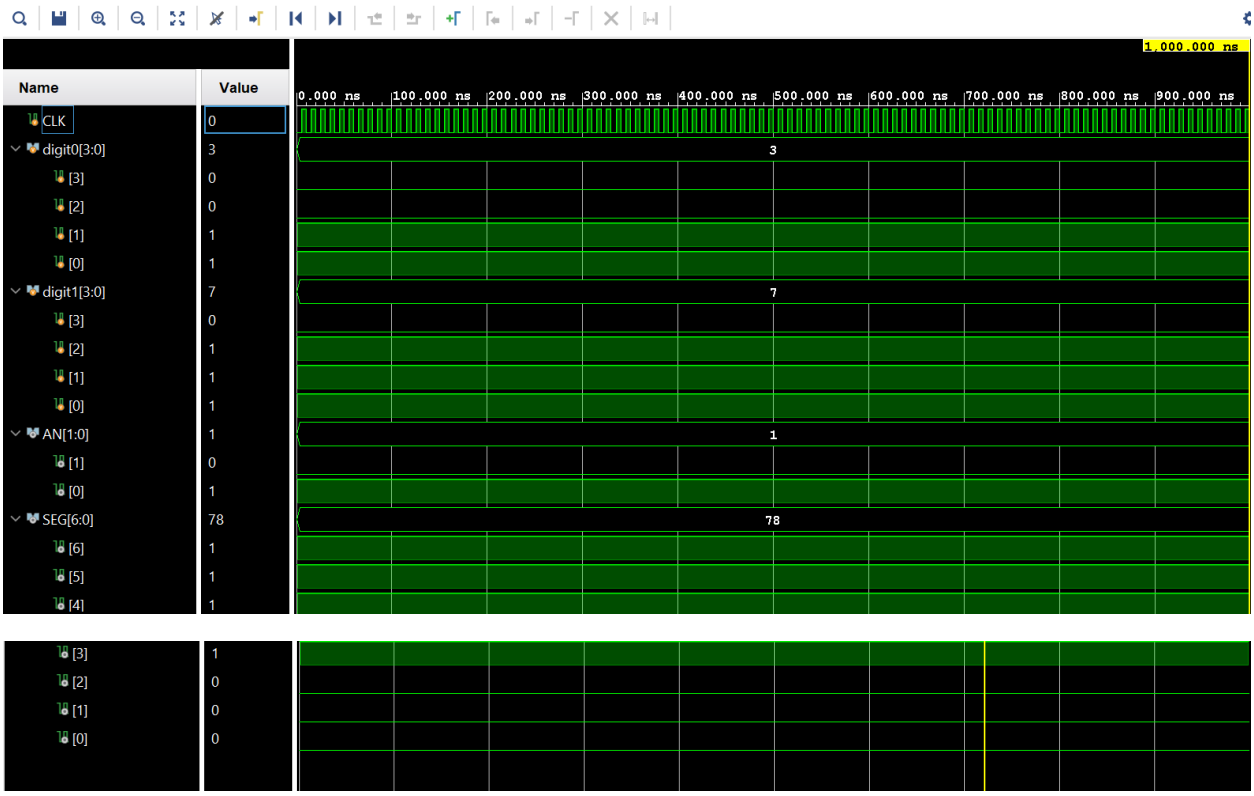


Clock_divider:


Name
Value
CLK
1
cnt[31:0]
0000000a
[31]
[30]
[29]
[28]
[27]
[26]
[25]
[24]
[23]
[22]
[21]
[20]
[19]
[18]
[17]
[16]
100.000 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
0...
00000001
00000002
00000003
00000004
00000005
00000006
00000007
00000008
00000009
0...


Name
Value
[16]
[15]
[14]
[13]
[12]
[11]
[10]
[9]
[8]
[7]
[6]
[5]
[4]
[3]
[2]
[1]
[0]
100.000 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns

Seg7_scan:

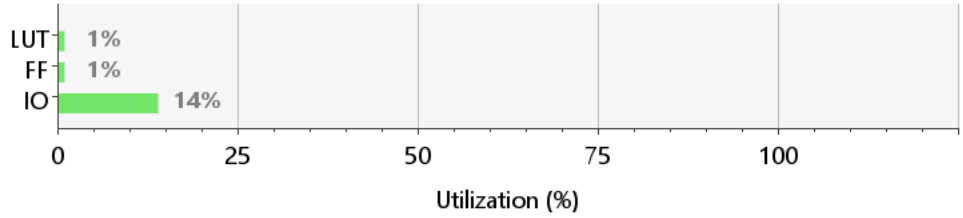


Hardware Results:

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
top_lab5	26	59	4	24	26	30	1
counter (bcd_up_down_counter)	14	8	0	6	14	0	0
display (seg7_scan)	2	18	0	6	2	0	0
div (clock_divider)	10	32	4	12	10	0	0

Summary

Resource	Utilization	Available	Utilization %
LUT	26	63400	0.04
FF	59	126800	0.05
IO	30	210	14.29



Contributions:

Both worked on the report

Nathaniel: Testbench files, Xdc files and Demo

Mikael: Source files, simulation testing