ECE 3300L

California State Polytechnic University, Pomona

Group G

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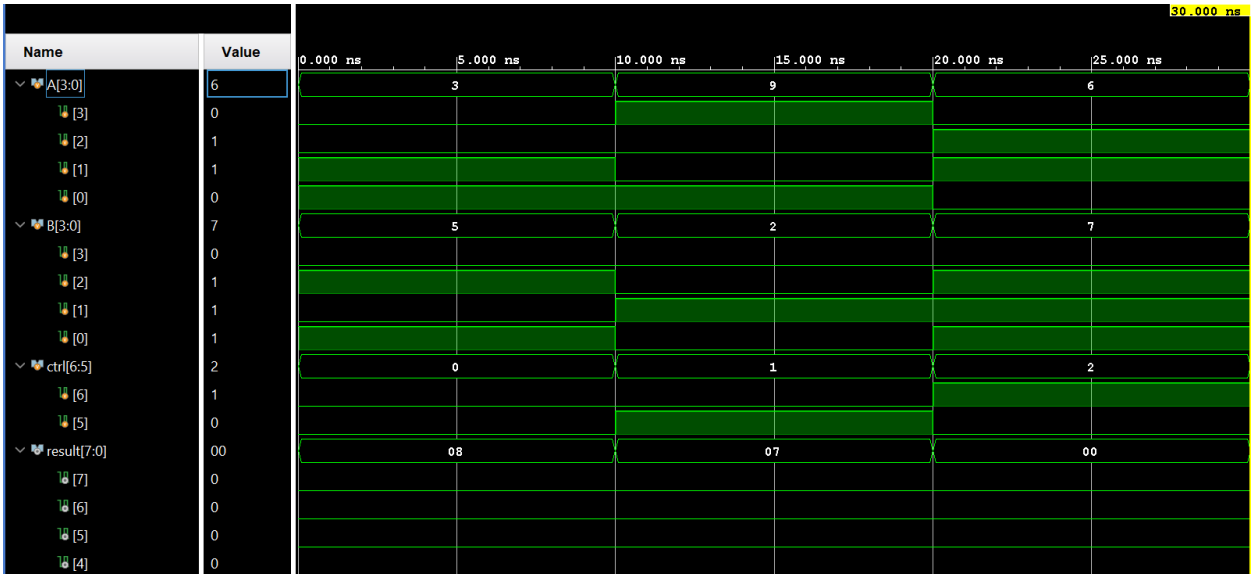
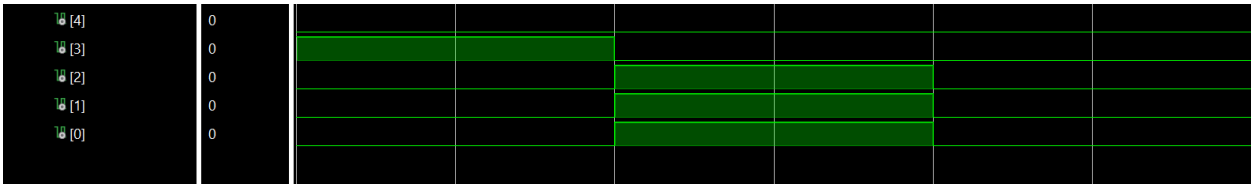
Lab Report #6

07/28/2025

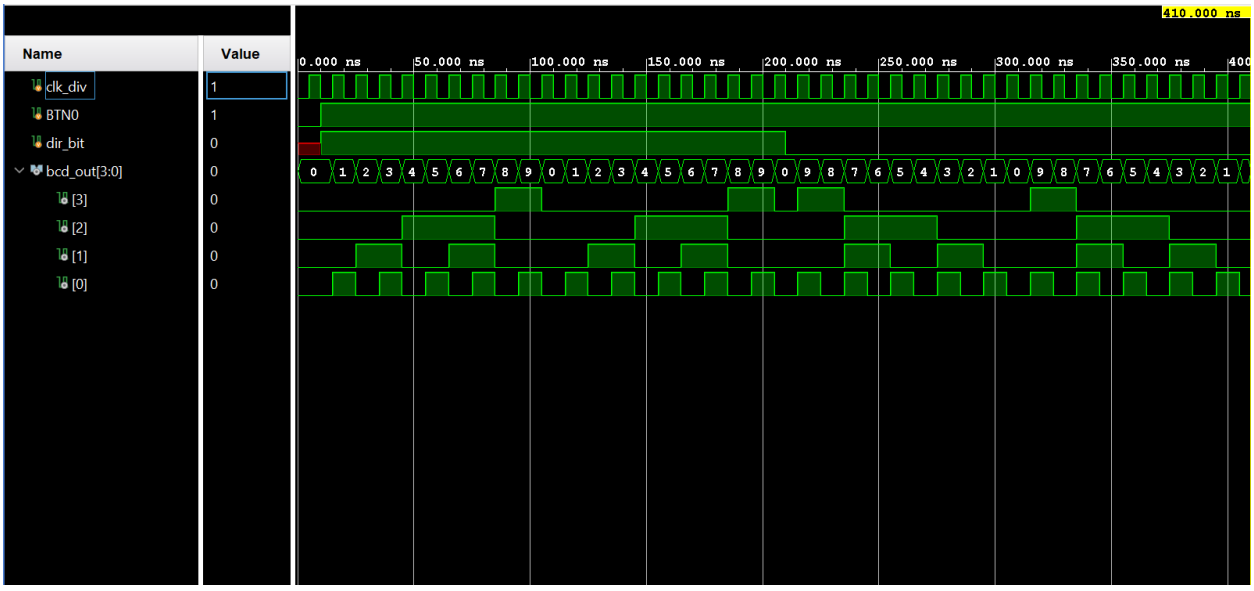
Explanation:

Tb_alu:

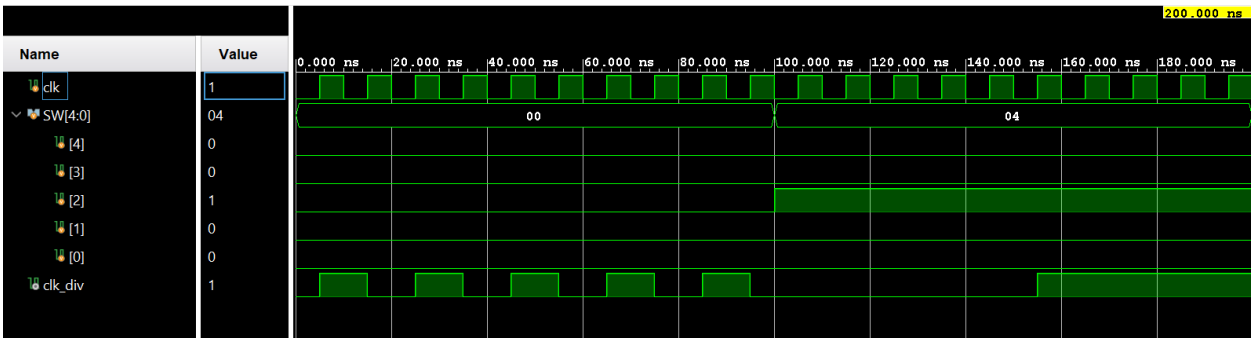




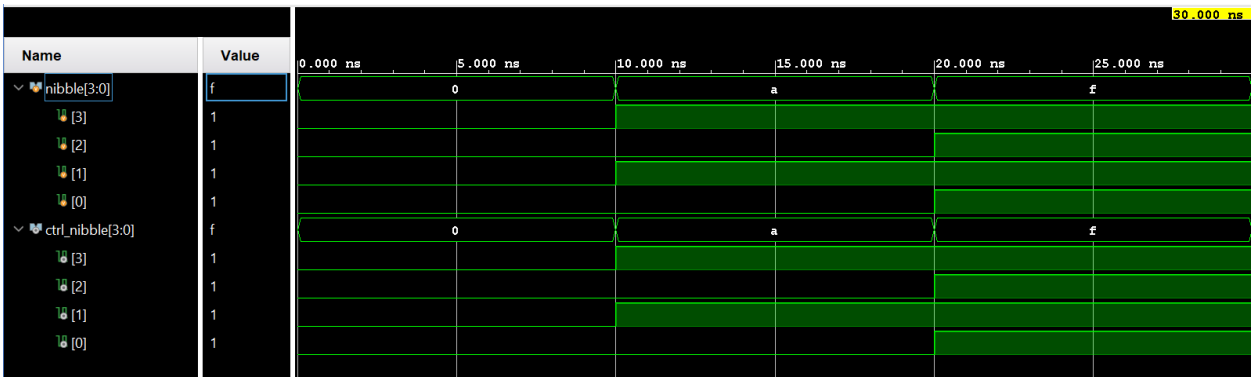
Tb_bcd_counter:



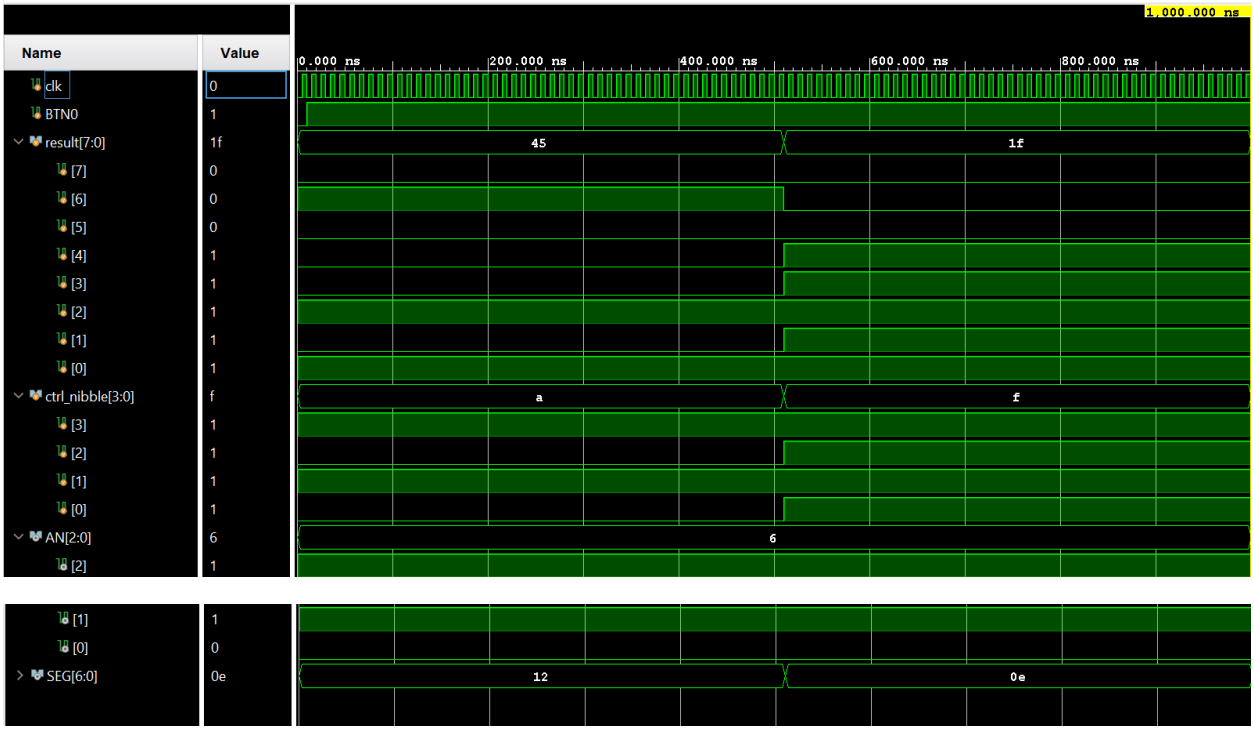
Tb_clock_divider:



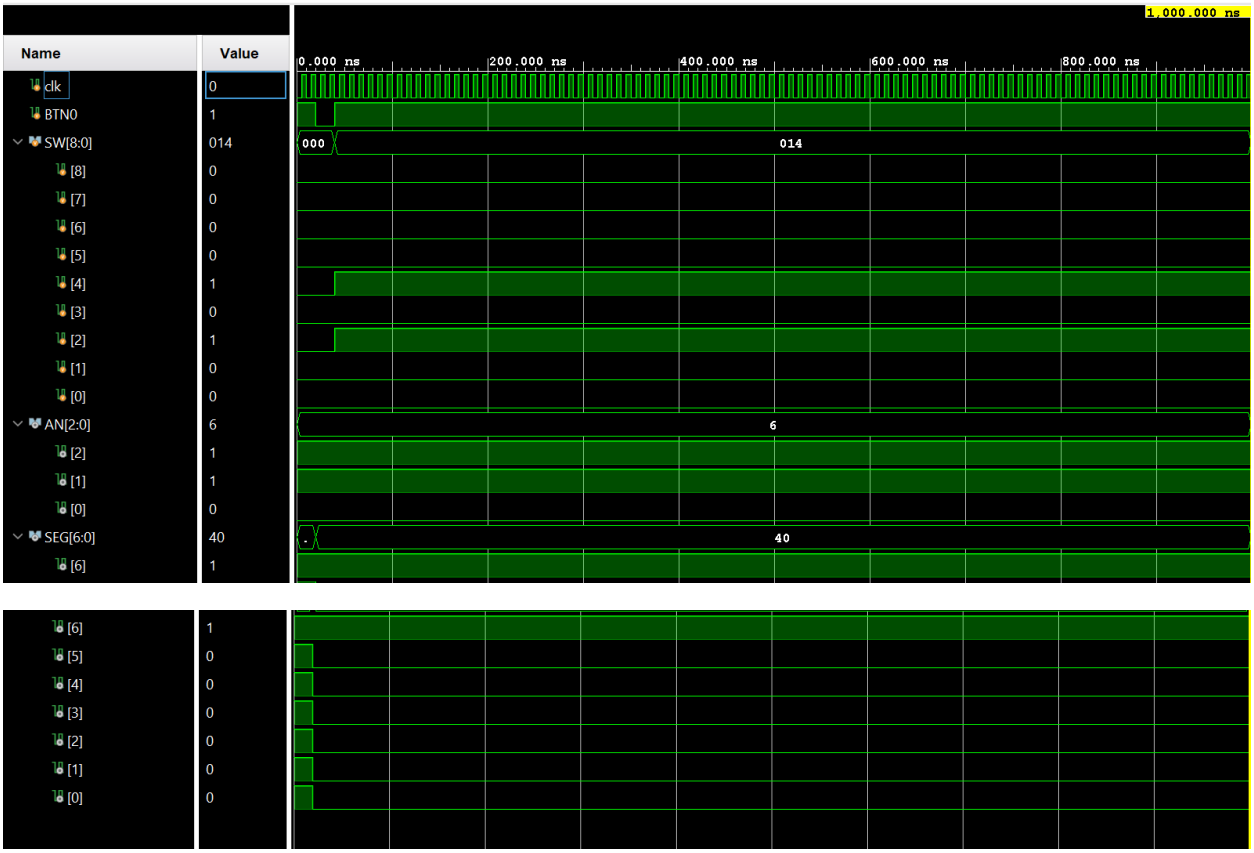
Tb_control_decoder:



Tb_seg7_scan:



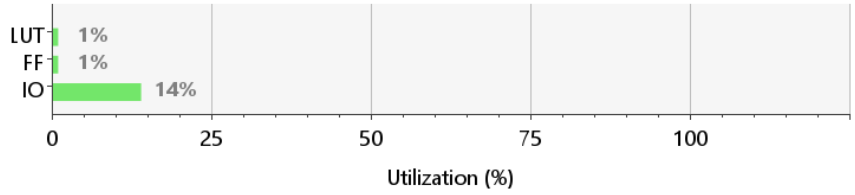
Tb_top_lab6:



Hardware Utilization:

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
top_lab6	37	58	4	25	37	29	1
clkdiv_inst (clock_divider)	10	32	4	12	10	0	0
seg_inst (seg7_scan)	17	18	0	13	17	0	0
tens_inst (bcd_counter)	4	4	0	3	4	0	0
units_inst (bcd_counter_0)	6	4	0	4	6	0	0

Resource	Utilization	Available	Utilization %
LUT	37	63400	0.06
FF	58	126800	0.05
IO	29	210	13.81



Contributions:

Both worked on the Lab document

Mikael: Verilog source files, Simulations

Nathaniel: Testbench files, Xdc file and Demo