ECE 3300L

Lab Report #5

Group E

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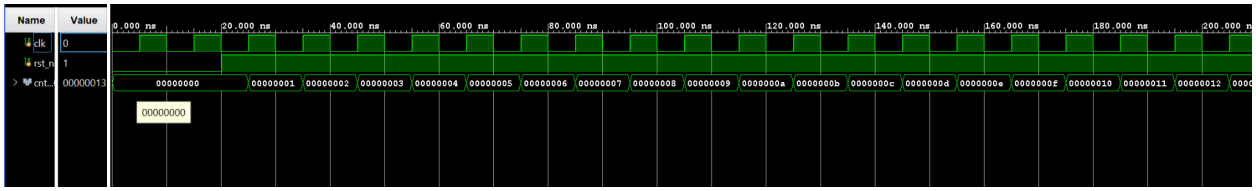
Design:

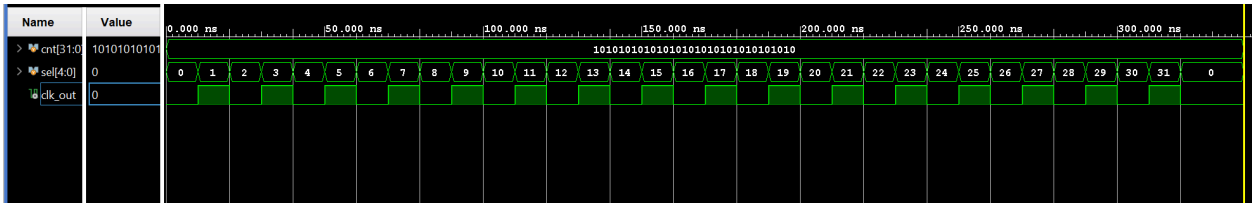
- **clock_divider.v -** Generates a 32-bit incrementing counter from the system clock.
- **mux32x1.v -** Selects one bit from the 32-bit counter using SW[4:0], outputting a divided clock.
- **bcd_up_down_counter.v -** A two-digit BCD counter. Handles up/down counting and cascading between digit0 and digit1.
- **seg7_scan.v -** Drives the 2-digit 7-segment display with time-multiplexed output.
- **top_lab5.v -** Integrates all submodules. Connects switches, buttons, LEDs, and 7-segment outputs.

Simulation:

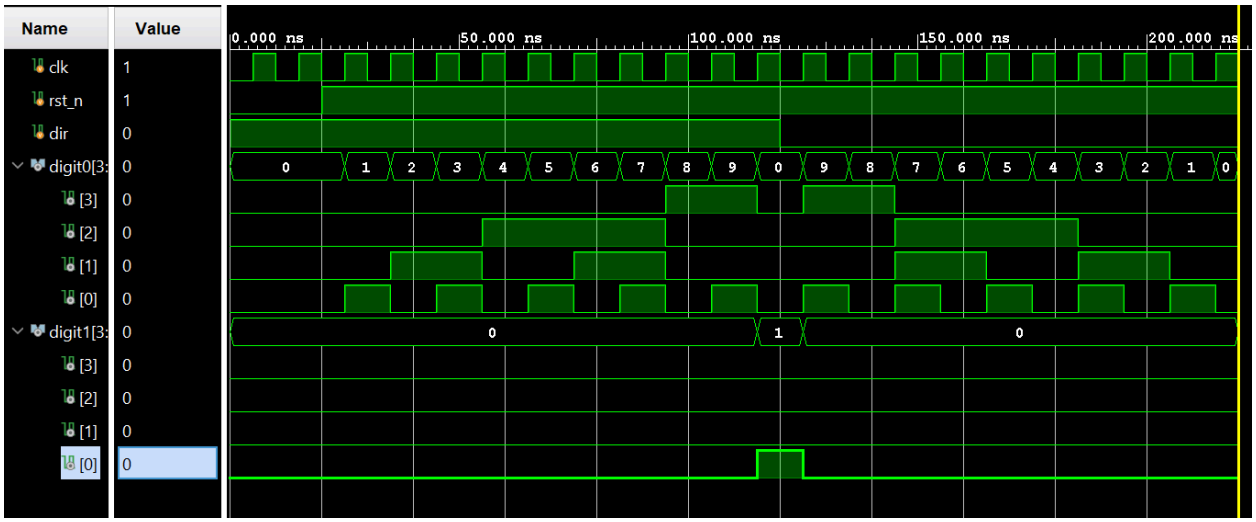
clock_divider_tb: Verify counter increments.



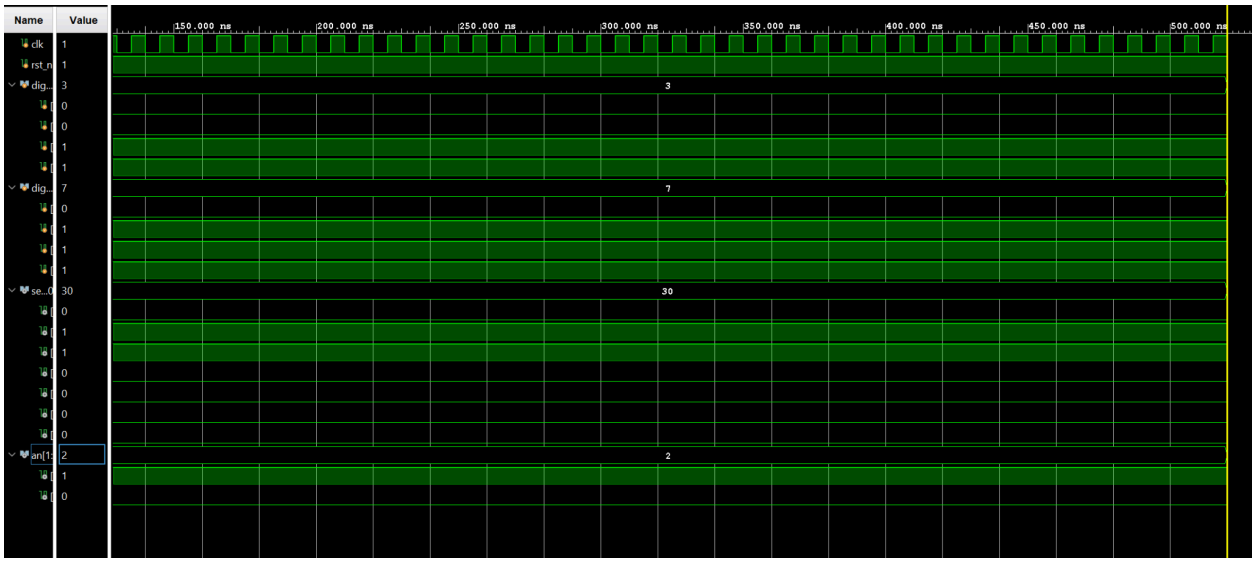
mux32x1_tb: Ensure correct bit selection for various sel.



bcd_up_down_counter_tb: Confirm up/down counting behavior with reset.



seg7_scan_tb: Verify multiplexing and segment decoding.



Implementation:

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	26	0	0	63400	0.04
LUT as Logic	26	0	0	63400	0.04
LUT as Memory	0	0	0	19000	0.00
Slice Registers	57	0	0	126800	0.04
Register as Flip Flop	57	0	0	126800	0.04
Register as Latch	0	0	0	126800	0.00
F7 Muxes	4	0	0	31700	0.01
F8 Muxes	0	0	0	15850	0.00

Contributions:

Paul Kim - Source Codes, Testbench, Simulation - 50% contribution

Winson Zhu - Source Codes, Implementation, Hardware Demo - 50% contribution