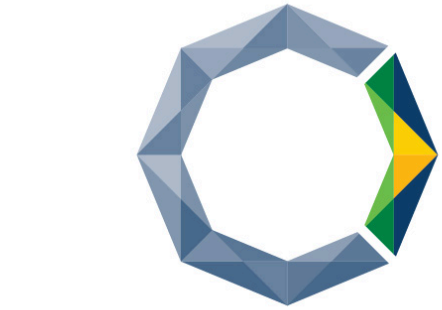

CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #7

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Presented to Mohamed Aly

August 6th, 2025

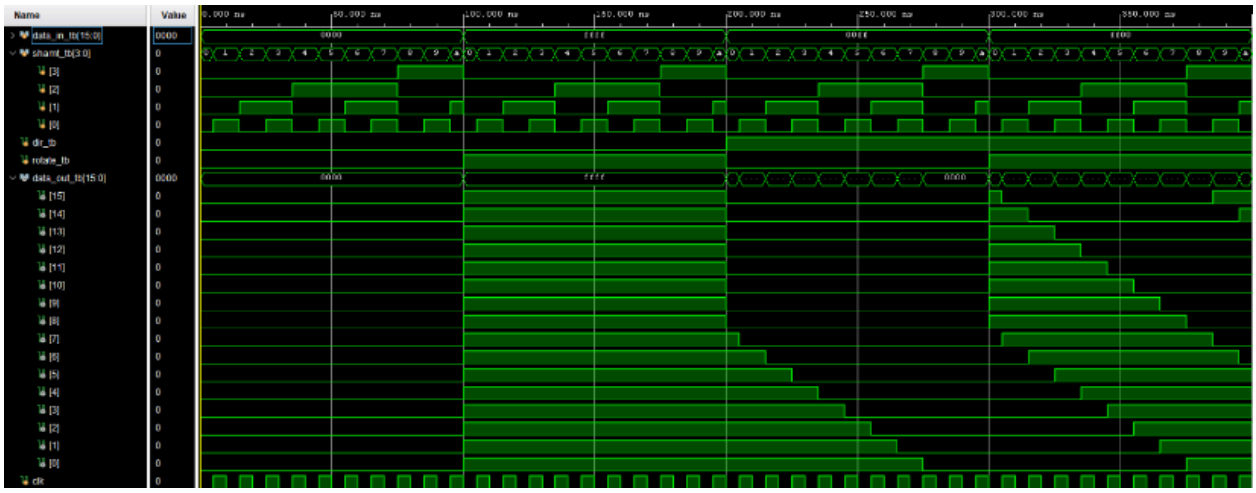
Objective: In this lab, we were tasked to build a 16-bit barrel shifter and rotator using the Nexys A7 FPGA. Our design takes a 16-bit input from the slide switches and can shift or rotate the bits left or right by any amount from 0 to 15. The direction and type of shift (logical or rotate) are controlled using debounced push buttons. The result shows up as four hex digits on the right side of the 7-segment display. Overall, this lab helped us get first hand experience with multiplexers, display control, and debouncing. It also shows how adding features can affect the complexity of a digital circuit.

Utilization:

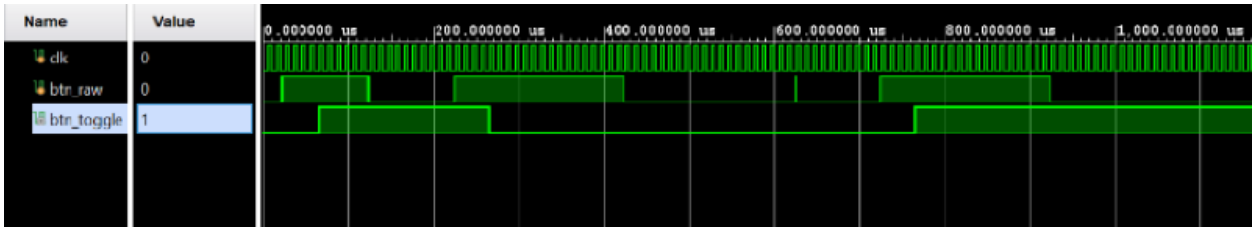
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	33	0	0	63400	0.05
LUT as Logic	33	0	0	63400	0.05
LUT as Memory	0	0	0	19000	0.00
Slice Registers	67	0	0	126800	0.05
Register as Flip Flop	67	0	0	126800	0.05
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

Simulation:

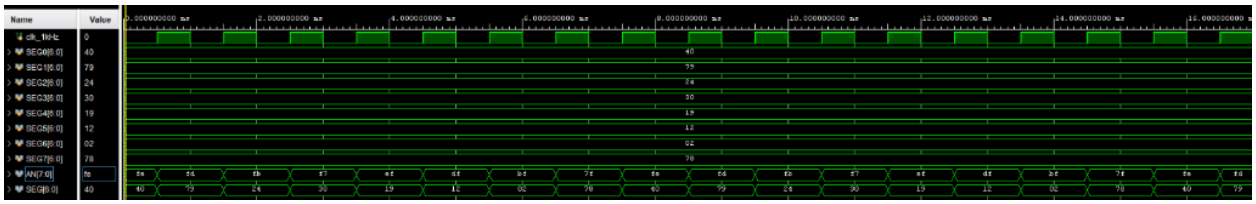
barrel_shifter16_tb



debounce_toggle_tb



seg7_scan8_tb



Team Contributions:

Daniel Mondragon Xicotencatl + 50%

Kobe Aquino + 50%

We both collaborated on the Verilog HDL by testing and modifying each other's modules, writing the test bench simulations together, and writing the report.

Reflection: This lab gave us some valuable first hand experience on designing a digital system with the function of being a 16 bit barrel shifter and rotator. We got experience on how hook up user inputs that implement push buttons and side switches can display the output on the seven segment display. One of the big takeaways was learning how a multi stage multiplexer can shift or rotate data instantly, which showed the usage of structural Verilog. We also learned how to debounce buttons properly and use a clock divider to make the controls reliable. Running simulations, generating bitstreams, and testing the circuit on hardware helped us understand how important it is to design things in a modular way and verify everything works. Overall, this final lab helped connect our class knowledge to real FPGA design skills.