ECE 3300L

California State Polytechnic University, Pomona

Group G

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Lab Report #6

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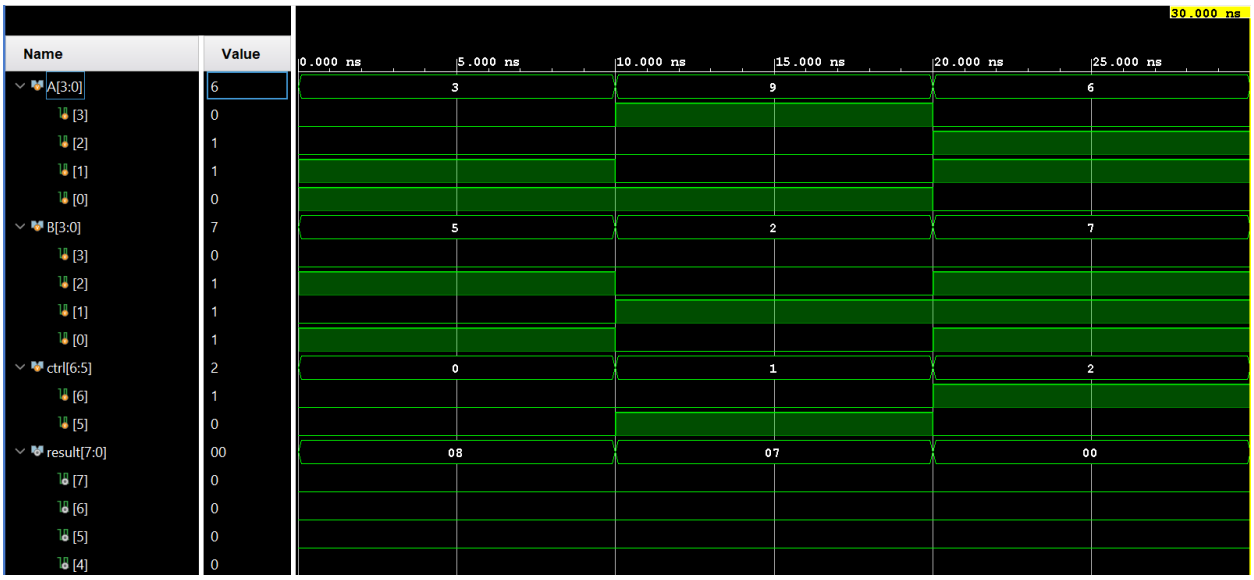
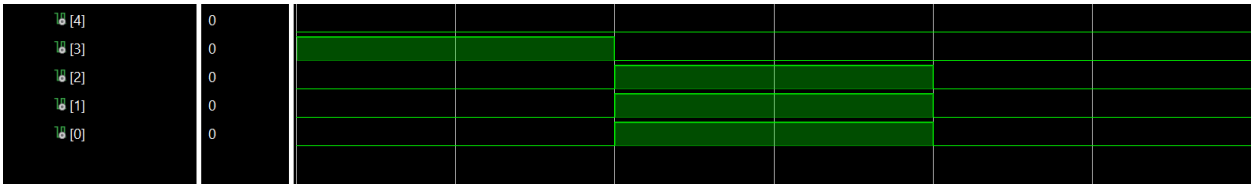
Explanation:

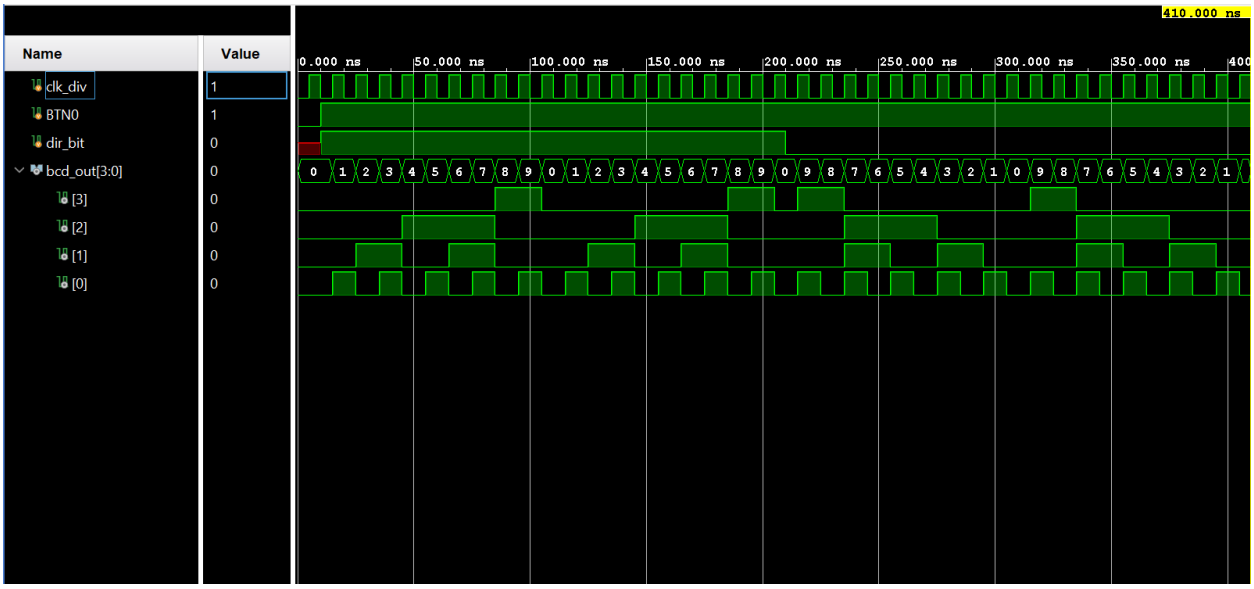
-The tb_top_lab6.v file is used for toggling switches and observing ALU operations and BCD counting. It does this by generating a clock, setting initial switch values, and simulating reset and control signals.
-The top_lab6.v file is the main module that connects all the components, consisting of the clock divider, BCD counters, ALU, control decoder, and 7-segment display. It describes the wiring and integrates the modules to handle the input switches, displaying the outputs on both the LEDs and the 7-segment display.
-The alu.v module is for calculating arithmetic operations between two 4-bit inputs depending on a 2-bit control signal. It outputs an 8-bit result and defaults to 0 if the control signal is undefined.
-The bcd_counter.v file defines a BCD counter that goes up or down based on a direction bit, which resets if the button is pressed. It makes sure that values stay within 0 to 9 by wrapping appropriately.
-The clock_divider.v module slows the input clock by dividing it based on a counter indexed by a switch value. It is useful for having observable timing for the counter and display operations.
-The control_decoder.v module passes a 4-bit slice of switch input as the control signal for the ALU. This allows the user to choose different ALU operations with the hardware switches.
-The seg7_scan.v module drives the 7-segment display using digit selection and a decoding process. It cycles through each digit and shows either ALU outputs or control signal values based on the current scan state.

Tb_alu:

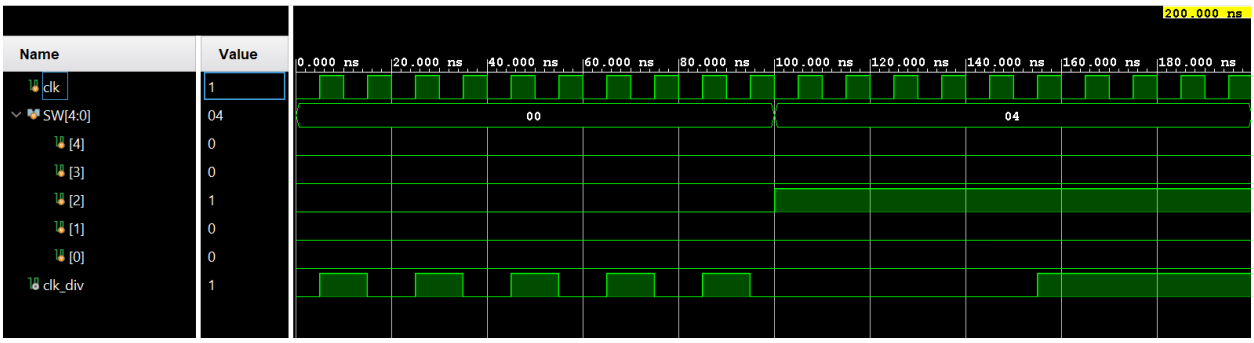




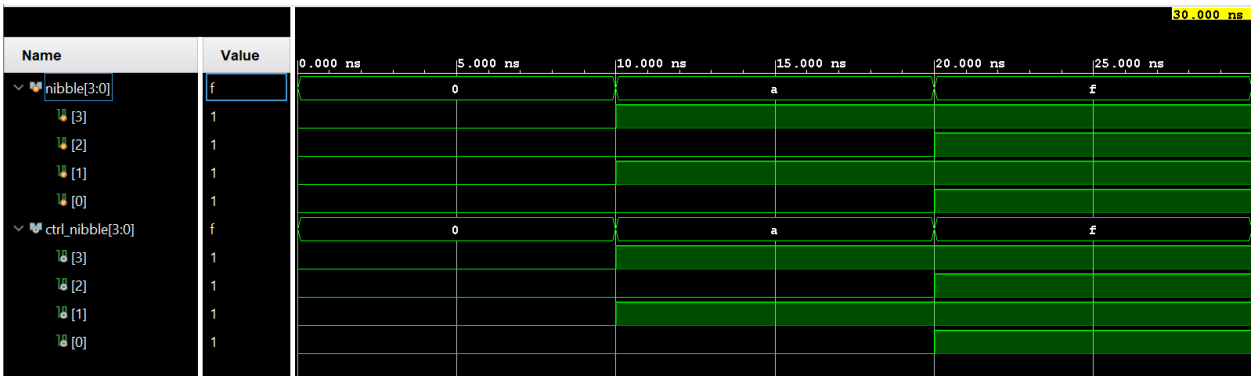
Tb_bcd_counter:



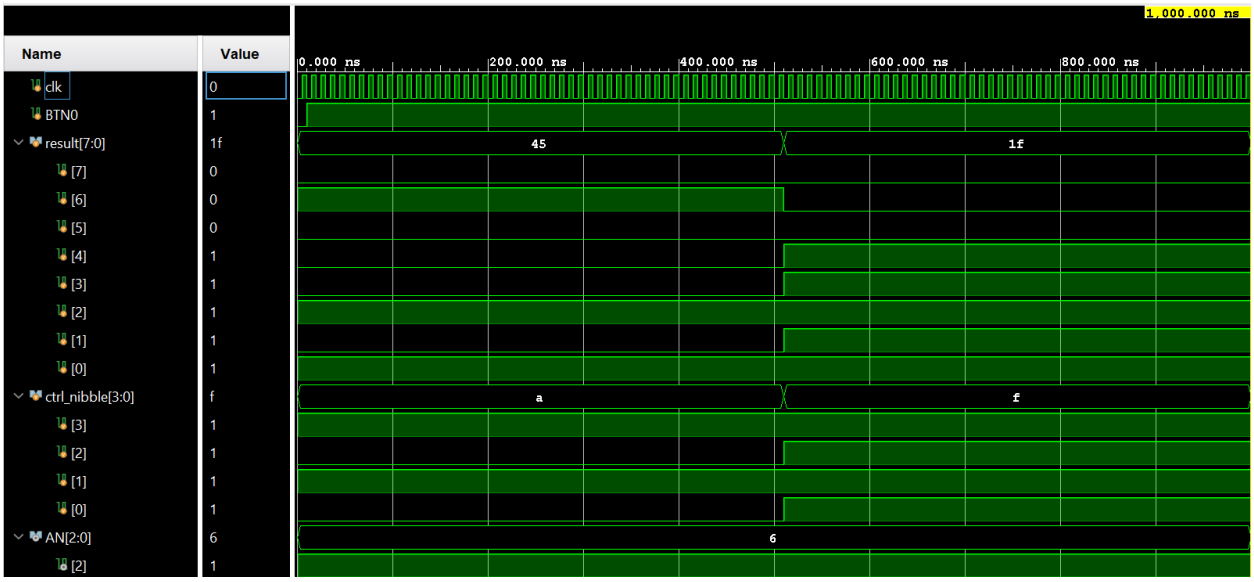
Tb_clock_divider:

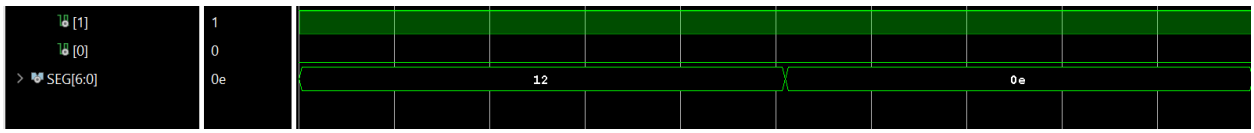


Tb_control_decoder:

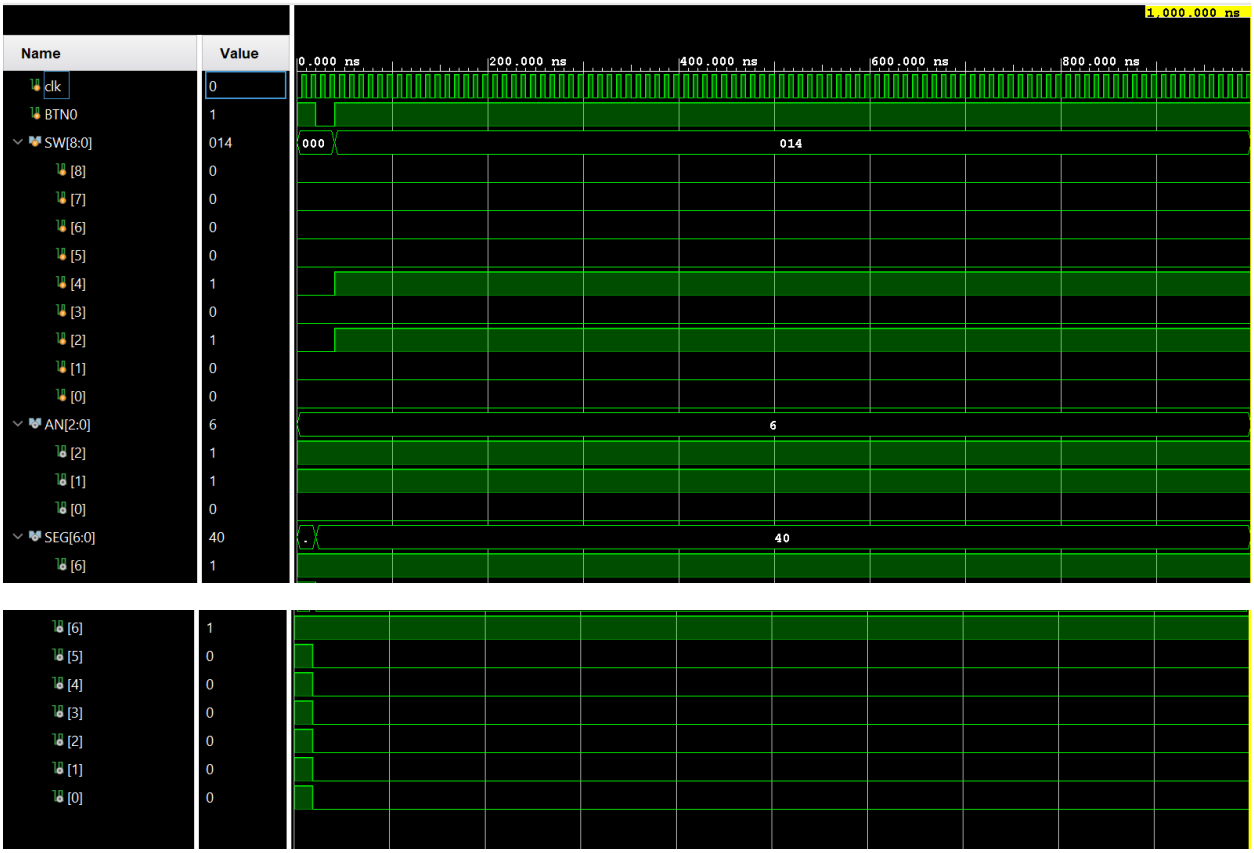


Tb_seg7_scan:





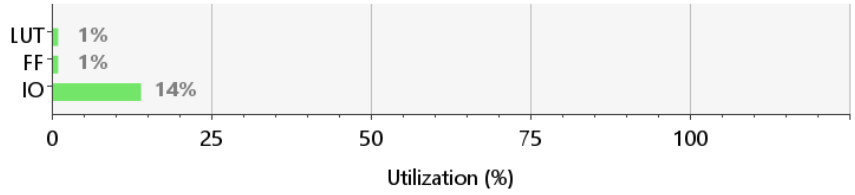
Tb_top_lab6:



Hardware Utilization:

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
top_lab6	37	58	4	25	37	29	1
clkdiv_inst (clock_divider)	10	32	4	12	10	0	0
seg_inst (seg7_scan)	17	18	0	13	17	0	0
tens_inst (bcd_counter)	4	4	0	3	4	0	0
units_inst (bcd_counter_0)	6	4	0	4	6	0	0

Resource	Utilization	Available	Utilization %
LUT	37	63400	0.06
FF	58	126800	0.05
IO	29	210	13.81



Contributions:

Both worked on the Lab document

Mikael: Verilog source files, Simulations

Nathaniel: Testbench files, Xdc file and Demo