ECE 3300L

California State Polytechnic University, Pomona

Group G

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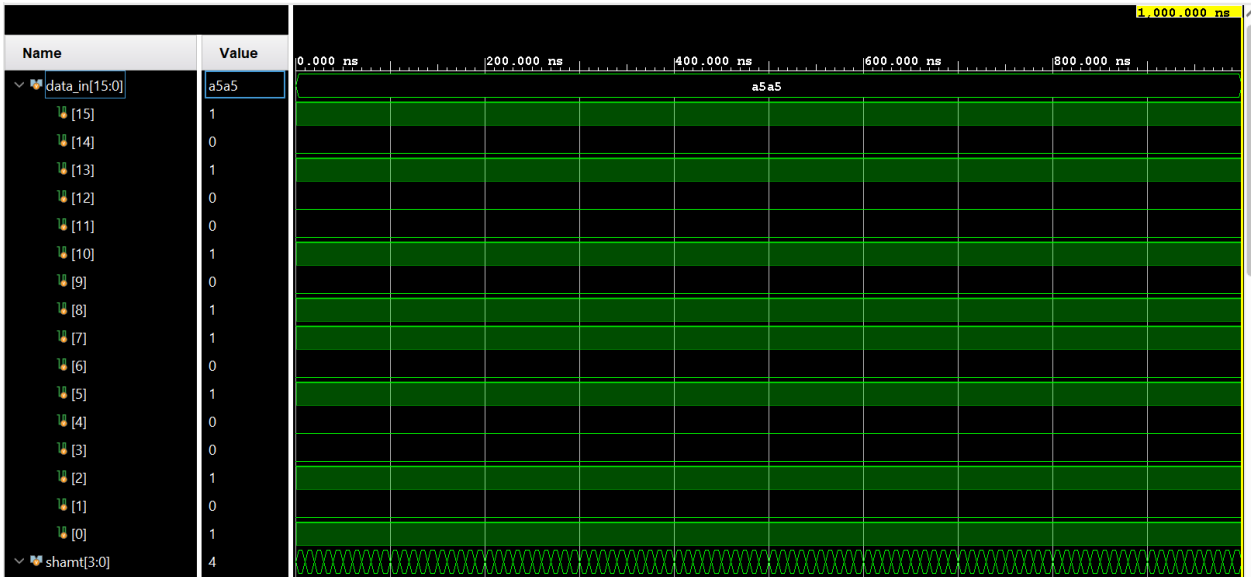
Lab Report #7

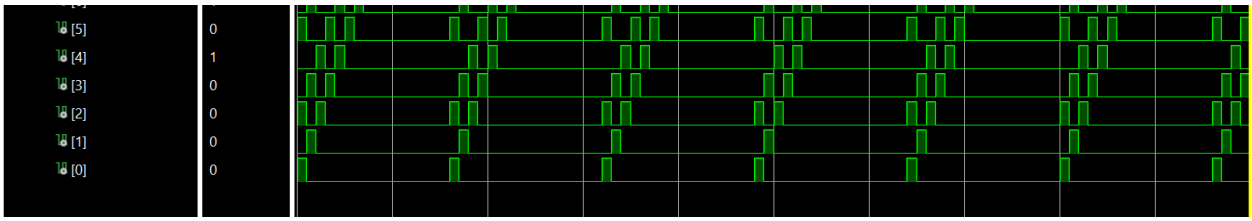
08/06/2025

Explanation:

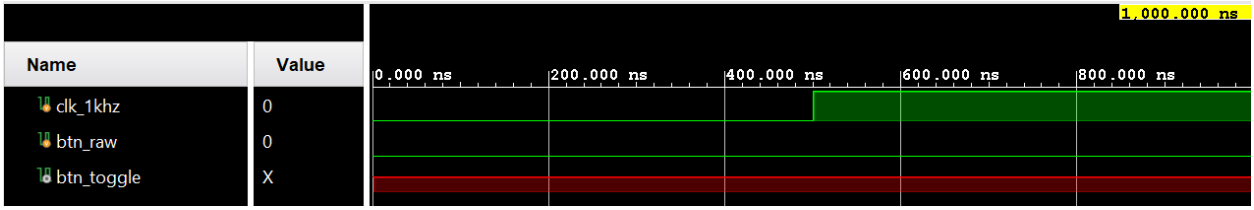
The Lab 7 Verilog project implements a 16-bit combinational barrel shifter/rotator circuit on the Nexys A7 FPGA. It features a MUX-based barrel_shifter16 module that shifts or rotates input data (SW[15:0]) left or right by a 4-bit amount, with direction and rotation control inputs. A clock_divider_fixed module creates slow clock pulses for display scanning and input control. Button inputs are processed by debounce_toggle modules to toggle DIR, ROTATE, and the lower 2 bits of the shift amount, with a shamt_counter cycling through the upper 2 bits. The result is shown on the lower four digits of the 7-segment display via hex_to_7seg and seg7_scan8, with debug LEDs showing control states. All is integrated in the top_lab7 module for the demonstration.

Barrel_shifter16_tb:

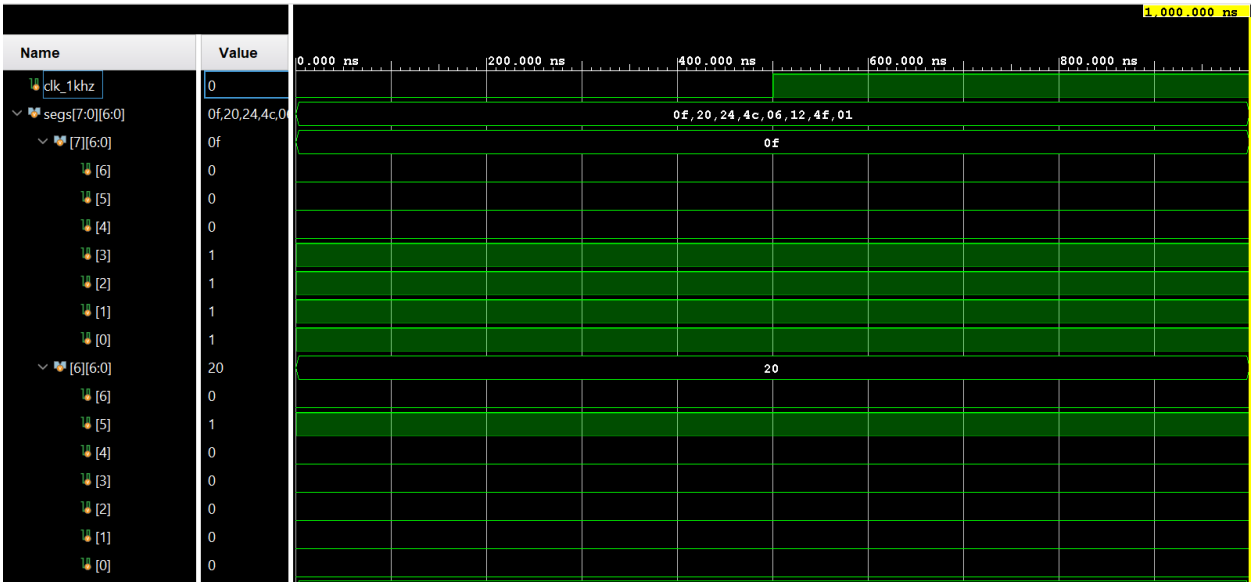


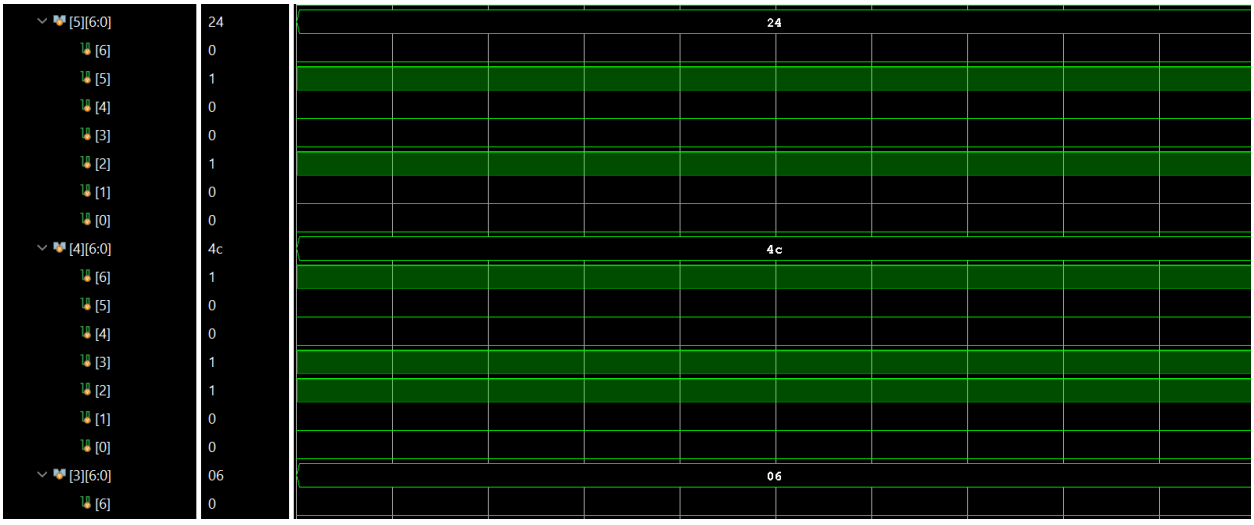


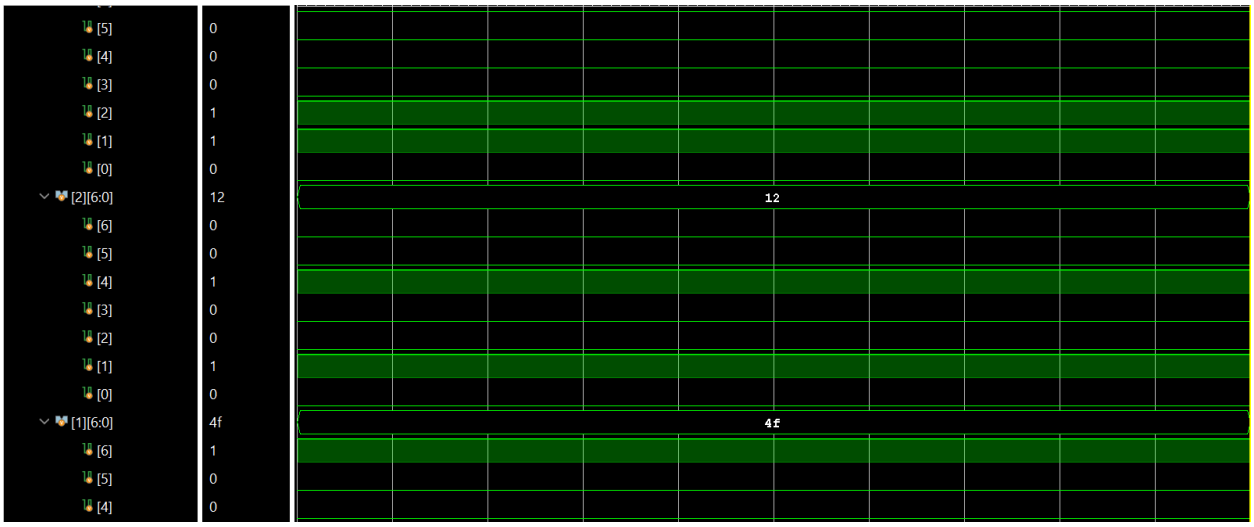
Debounce_toggle_tb:

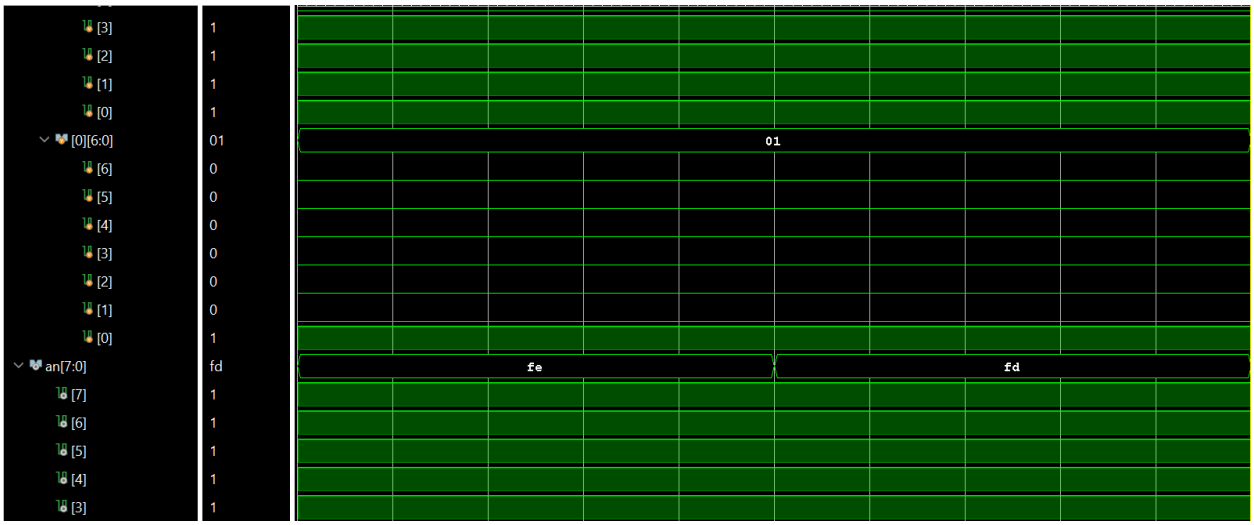


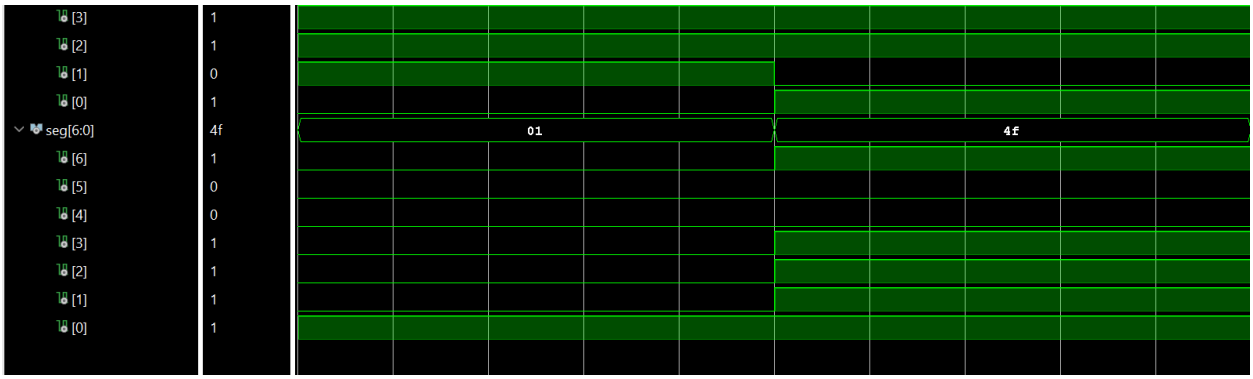
Seg7_scan8_tb:






[5] 0
[4] 0
[3] 0
[2] 1
[1] 1
[0] 0
[2][6:0] 12
12
[6] 0
[5] 0
[4] 1
[3] 0
[2] 0
[1] 1
[0] 0
[1][6:0] 4f
4f
[6] 1
[5] 0
[4] 0

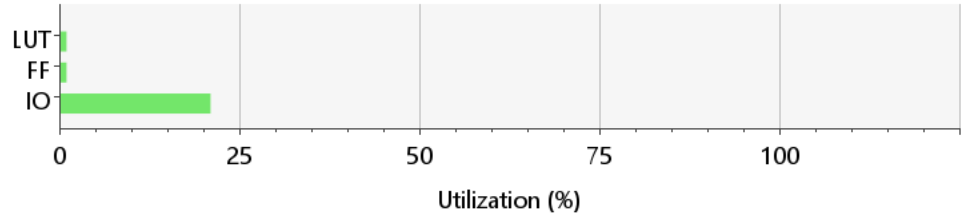

[3] 1
[2] 1
[1] 1
[0] 1
[0][6:0] 01
01
[6] 0
[5] 0
[4] 0
[3] 0
[2] 0
[1] 0
[0] 1
an[7:0] fd
fe
fd
[7] 1
[6] 1
[5] 1
[4] 1
[3] 1


[3] 1
[2] 1
[1] 0
[0] 1
seg[6:0] 4f
01
4f
[6] 1
[5] 0
[4] 0
[3] 1
[2] 1
[1] 1
[0] 1

Hardware Utilization:

Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
top_lab7	103	44	35	103	45	1
clkdiv (clock_divider_fixed)	5	18	6	5	0	0
cnt (shamt_counter)	1	3	1	1	0	0
deb_dir (debounce_toggle)	1	5	2	1	0	0
deb_rot (debounce_toggle_0)	5	5	6	5	0	0
deb_shamt0 (debounce_toggle_1)	84	5	27	84	0	0
deb_shamt1 (debounce_toggle_2)	1	5	2	1	0	0
scanner (seg7_scan8)	6	3	4	6	0	0

Resource	Utilization	Available	Utilization %
LUT	103	63400	0.16
FF	44	126800	0.03
IO	45	210	21.43



Contributions:

Both worked on the Lab document

Mikael: Verilog source files, Simulations

Nathaniel: Testbench files, Xdc file and Demo