ECE 3300L

Lab Report #1

Group E

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June 18, 2025

Synthesis Screenshots:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	0	0	0	32600	0.00
LUT as Logic	0	0	0	32600	0.00
LUT as Memory	0	0	0	9600	0.00
Slice Registers	0	0	0	65200	0.00
Register as Flip Flop	0	0	0	65200	0.00
Register as Latch	0	0	0	65200	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

Group Video Link:

https://youtu.be/7Gw7cZAkpMM

Reflection:

This lab was a basic introduction to designing FPGAs using Verilog on the Digilent Nexys A7-50T. In this lab, we connected all 16 switches on the FPGA board to the corresponding LEDs which turned them on and off individually. Although the design was simple, the lab emphasized the importance of precise pin mappings and how the XDC file is used for creating physical connections between peripherals on a board and the FPGA. Overall, this lab laid a solid foundation for future, more complex digital design projects.