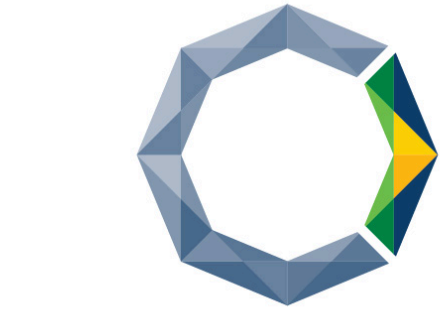


CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #6

Presented By: Kobe Aquino (StudentID: 015266433)

& Daniel Mondragon Xicotencatl (StudentID: 012803856)

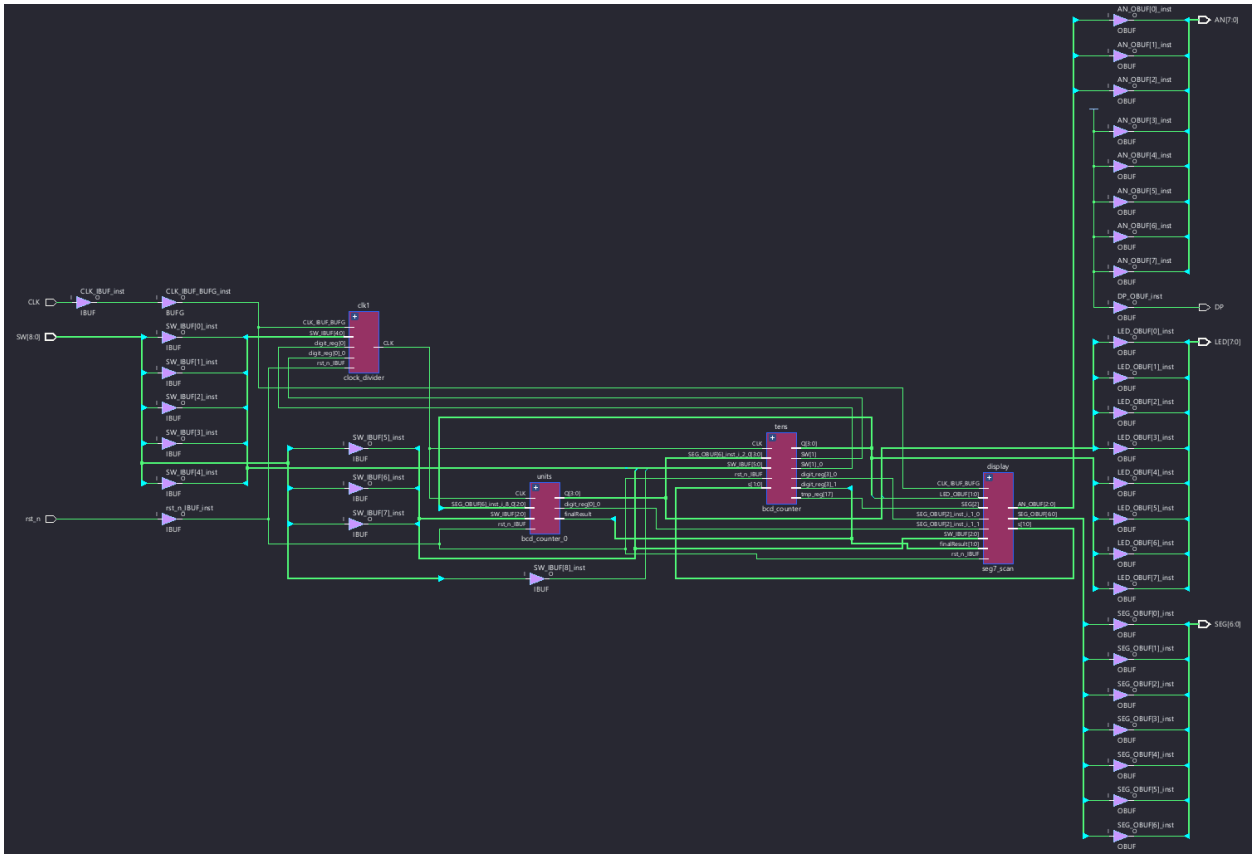
Presented to Mohamed Aly

July 28, 2025

Objective: So this week we took last week's lab of a BCD counter of a 2 7-segment display and modified it so that we can see each 7-segment counting up/down independently using LED's. In addition, we made an ALU module that adds/subtracts these 2 values which was shown in the 7-segment displays in HEX (0-18). We also added a new control module that displayed what settings were active in a third 7-seg display. We mapped the constraints file to the specifications below.

> Clock Divider: Use SW0–SW4 to slow down the 100 MHz clock for visible counting. Reset: BTN0 resets both counters to 0. Direction: SW7 & SW8 set up/down for each counter. ALU Operation: SW5 & SW6 select add or subtract. Display: Show result and control nibble on 7-seg; use LEDs for raw BCD debugging.

Schematic:



Utilization:

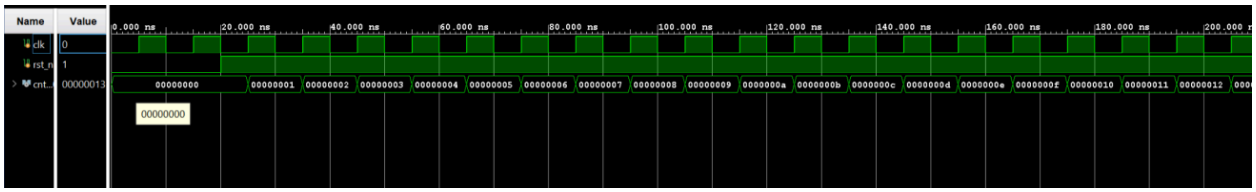
Tcl Console | Messages | Log | Reports | Design Runs | Methodology | DRC | Power | Timing

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	22	0	0	15850	0.14
SLICEL	14	0			
SLICEM	8	0			
LUT as Logic	34	0	0	63400	0.05
using O5 output only	0				
using O6 output only	23				
using O5 and O6	11				
LUT as Memory	0	0	0	19000	0.00
LUT as Distributed RAM	0	0			
using O5 output only	0				
using O6 output only	0				
using O5 and O6	0				
LUT as Shift Register	0	0			
using O5 output only	0				
using O6 output only	0				
using O5 and O6	0				
Slice Registers	59	0	0	126800	0.05
Register driven from within the Slice	59				
Register driven from outside the Slice	0				
Unique Control Sets	2		0	15850	0.01

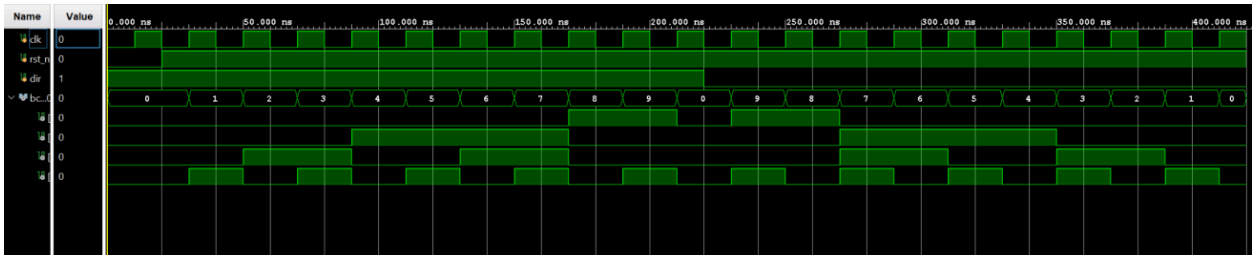
* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

Simulation:

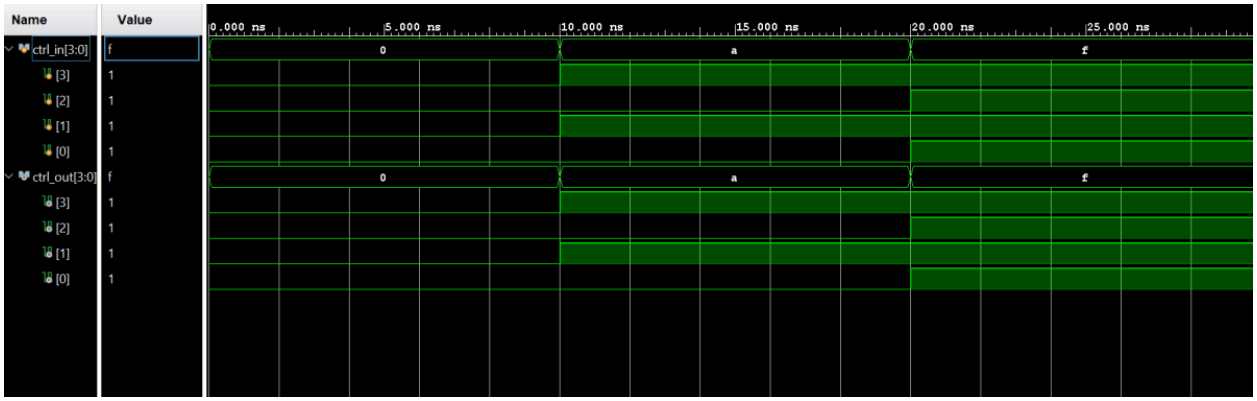
clock_divider_tb



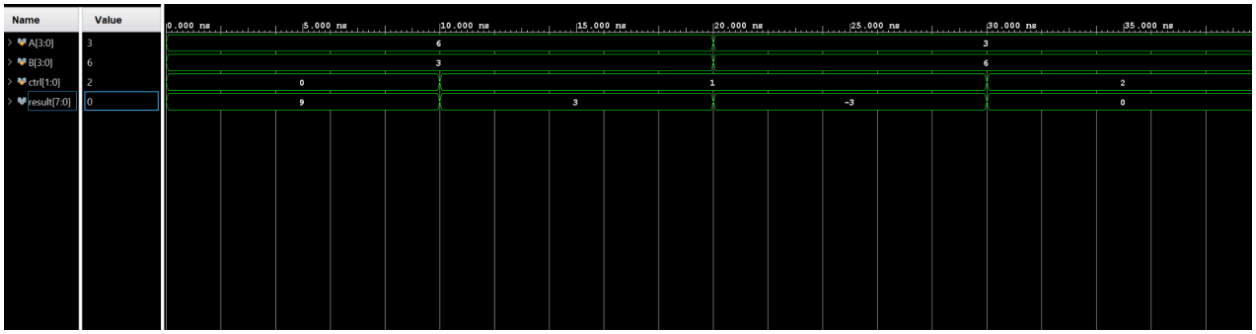
bcd_counter_tb



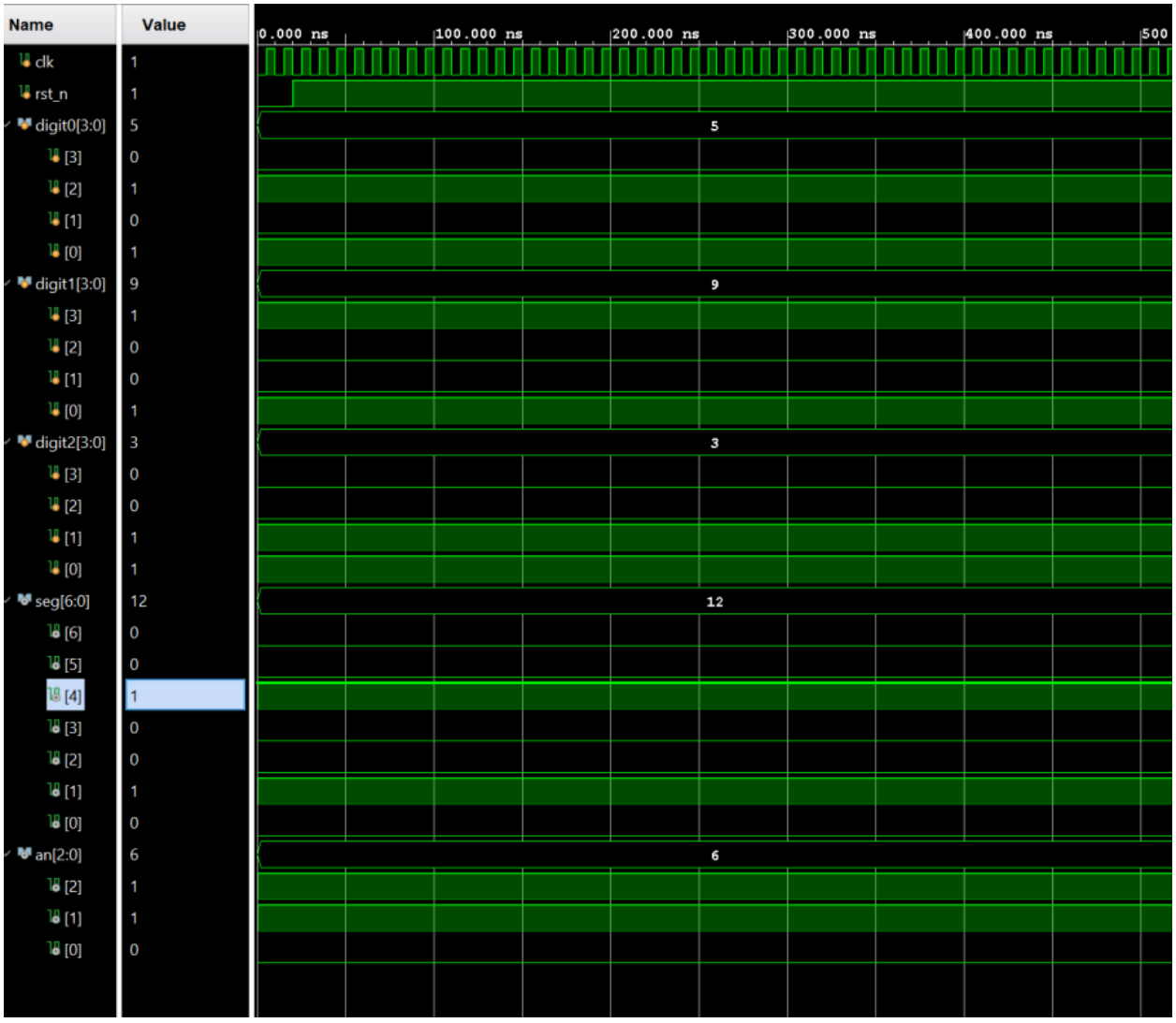
Control_decoder_tb



alu_tb



seg7_scan_tb



Team Contributions:

Daniel Mondragon Xicotencatl + 50%

Kobe Aquino + 50%

We both collaborated on the Verilog HDL by testing and modifying each other's modules, writing the test bench simulations together, and writing the report.