

Department of Electrical and Computer Engineering

ECE 3300L Section 1

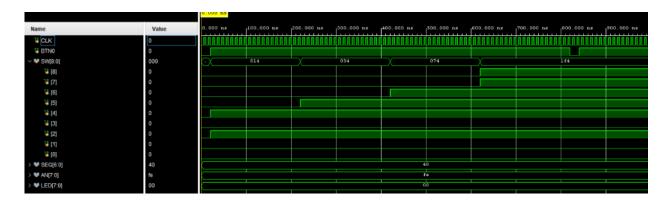
Lab 6 – Dual BCD Up/Down Counters, ALU, and Control Display on 7-Segment

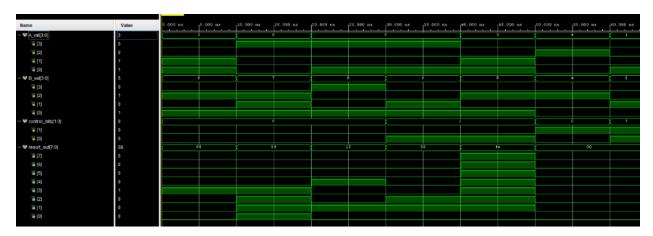
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July 28, 2025

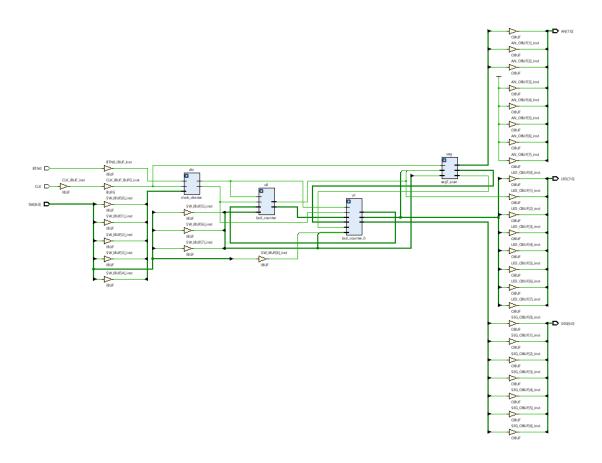
# Design:





# **Simulation:**

# Schematic:



### Implementation:

derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 0.131 W

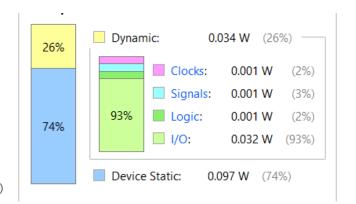
Design Power Budget: Not Specified

Process: typical

Power Budget Margin: N/A

Junction Temperature: 25.6°C

Thermal Margin: 59.4°C (12.9 W)



#### **Design Timing Summary**

Setup	Hold		Pulse Width	
Worst Negative Slack (WNS): 7.238 ns	Worst Hold Slack (WHS):	0.265 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints: 48	Total Number of Endpoints:	48	Total Number of Endpoints:	49
All user specified timing constraints are n	net.			

# **Contributions:**

Bryan Liu: Coding, Testbench, Simulations: 50%

Jaden Yeremenko: Simulations, Testbench, and Testing: 50%