Department of Electrical and Computer Engineering

ECE 3300L Section 1

Lab 5 – BCD Up/Down Counter on 7-Segment Display

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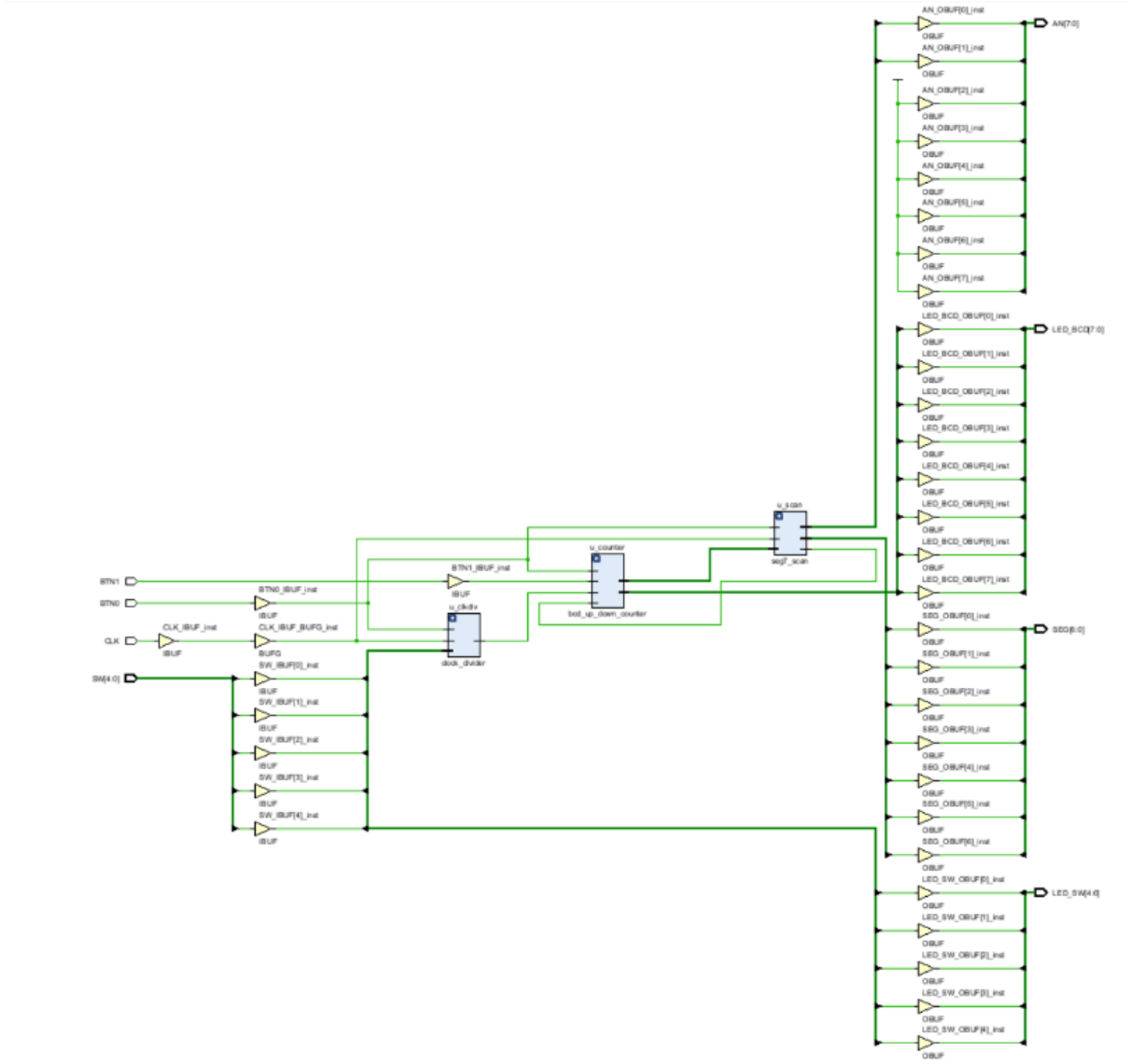
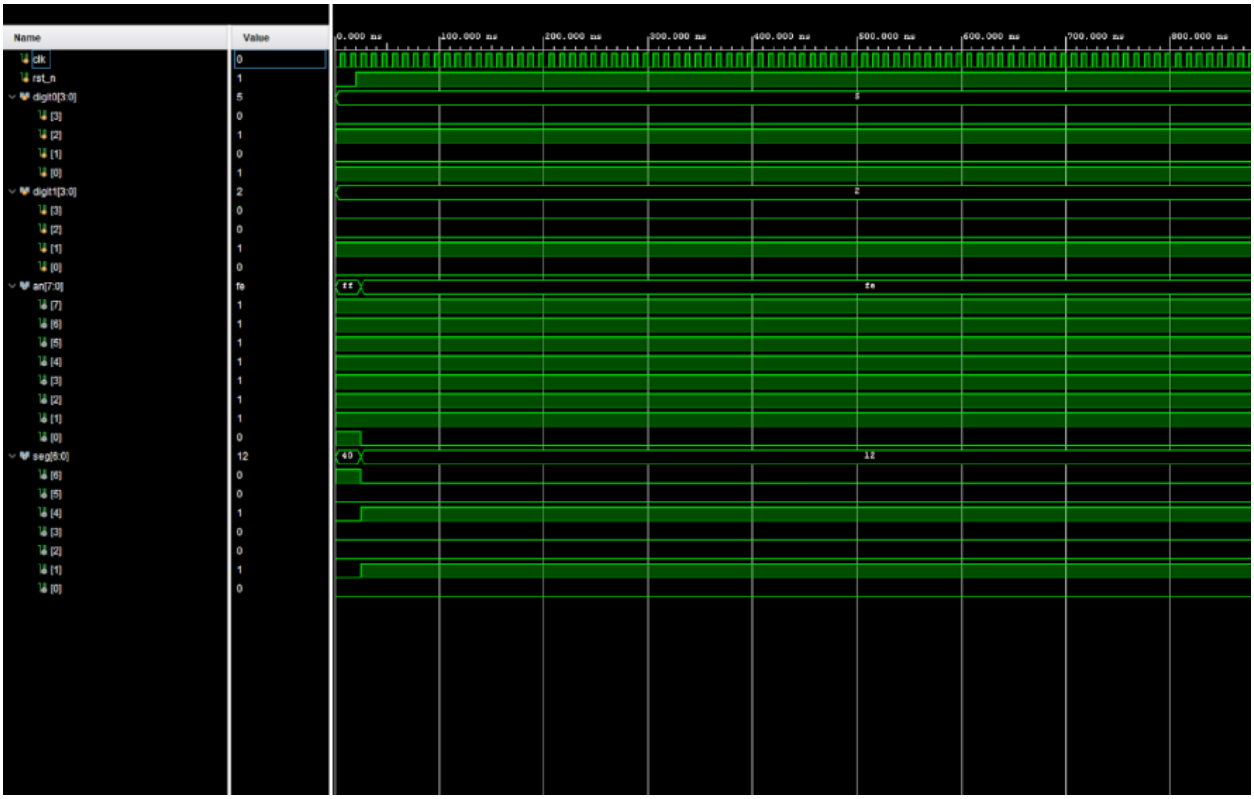
Design:


AN[7:0]
LED_BCD[7:0]
SEG[6:0]
LED_SW[4:0]
BTN1
BTN0
CLK
SW[4:0]
u_scan
seg7_scan
u_counter
bcd_up_down_counter
u_clkdiv
clock_divider

Simulation:


Name
Value
clk
0
rst_n
1
digit0[3:0]
5
[3]
0
[2]
1
[1]
0
[0]
1
digit1[3:0]
2
[3]
0
[2]
0
[1]
1
[0]
0
an[7:0]
fe
[7]
1
[6]
1
[5]
1
[4]
1
[3]
1
[2]
1
[1]
1
[0]
0
seg[6:0]
12
[6]
0
[5]
0
[4]
1
[3]
0
[2]
0
[1]
1
[0]
0
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
5
2
ff
fe
40
12

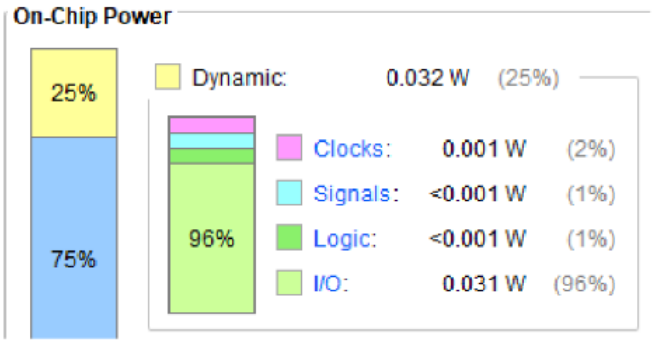
Implementation:

Utilization tables:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.338 ns	Worst Hold Slack (WHS):	0.252 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	58	Total Number of Endpoints:	58	Total Number of Endpoints:	59

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.129 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**



Contributions:

Bryan Liu: Some Verilog modules, testing, ultilization, schematic: 50%

Jaden Yeremenko: Testbench code, simulation, Some Verilog modules: 50%