ECE 3300L

Lab Report #6

Group E

Paul Kim (ID: 015236949)

Winson Zhu (ID: 016416790)

July 28, 2025

Design:

a) clock_divider.v - 100 MHz clock is divided based on SW[4:0]. 32-bit counter, output bit is selected by a 32×1 MUX.

b) bcd_counter.v - Counts 0–9 based on direction input (SW7/SW8). Resets on BTN0

c) alu.v - Accepts two 4-bit BCD values. Performs add or subtract based on SW[6:5]. Output is 8-bit result

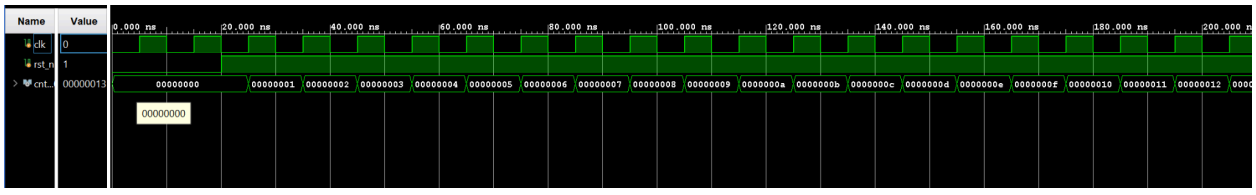
d) control_decoder.v - Takes {SW8, SW7, SW6, SW5}. Outputs as 4-bit control nibble for display

e) seg7_scan.v - 3-digit multiplexed display: AN0: result[3:0], AN1: result[7:4], AN2: control nibble

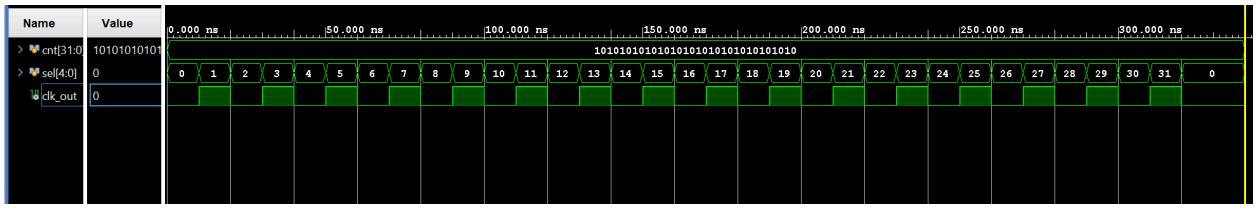
f) top_lab6.v - Instantiates all other modules

Simulation:

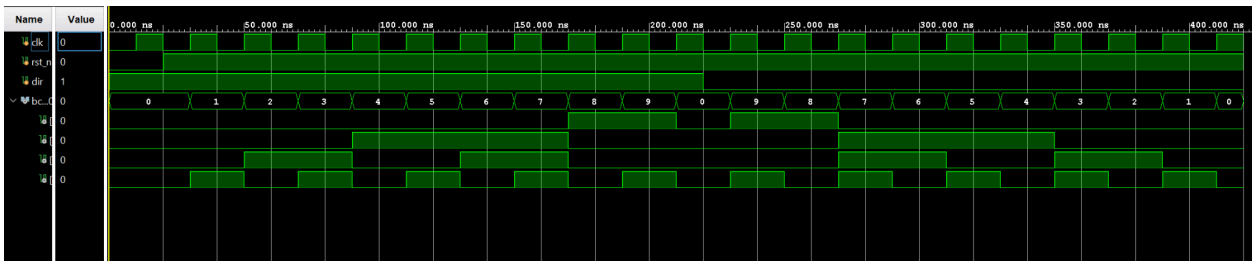
clock_divider_tb:



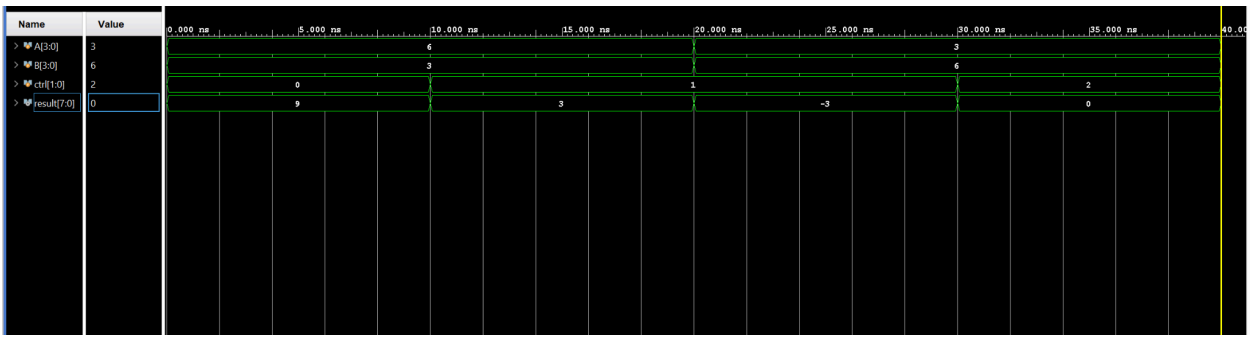
mux32x1_tb:



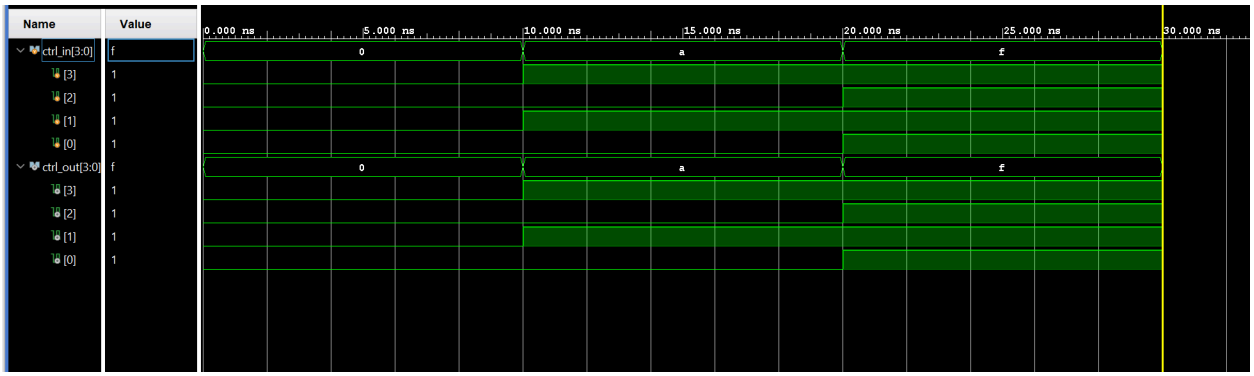
bcd_counter_tb:



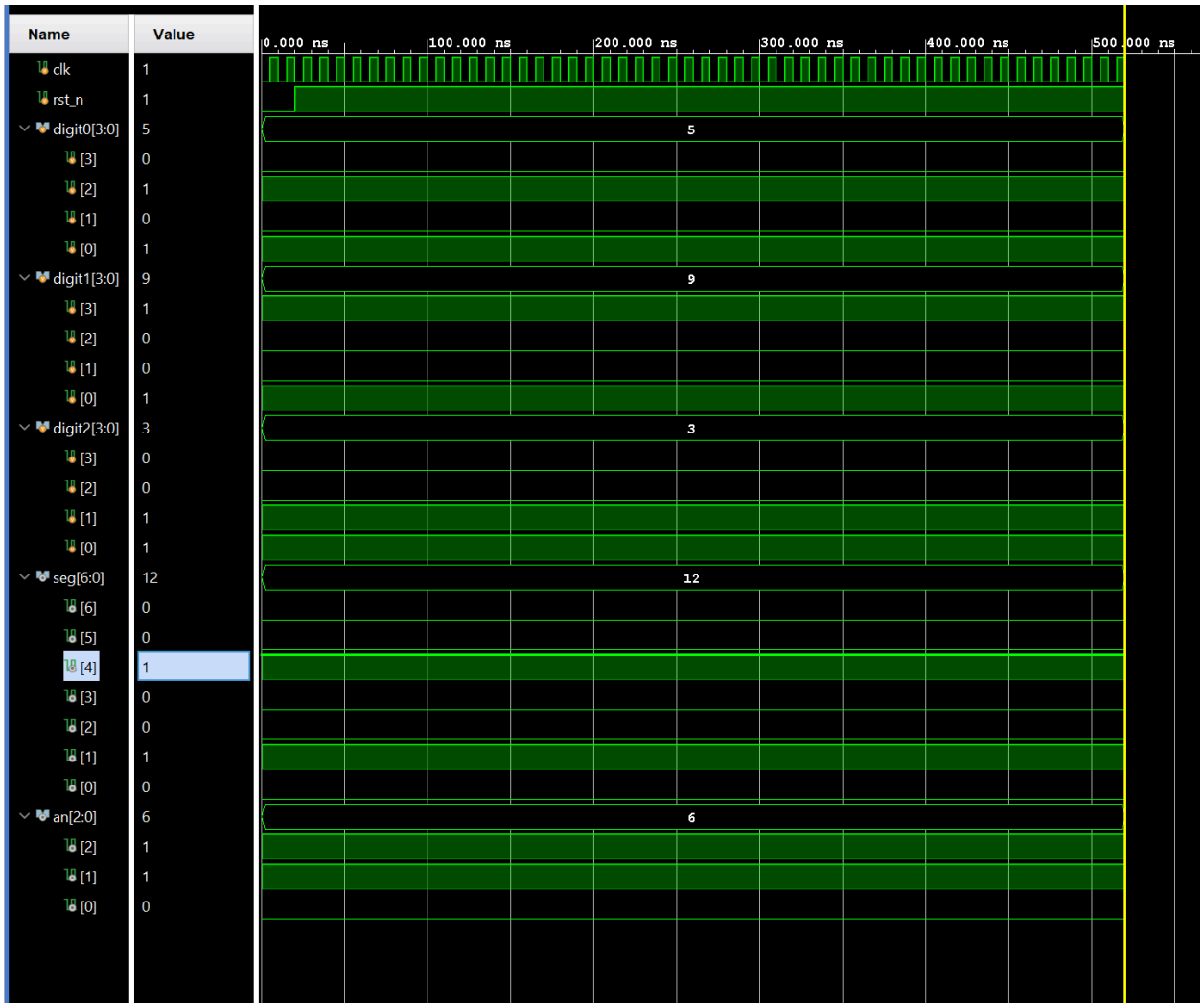
alu_tb:



control_decoder_tb:



seg7_scan_tb: Verify multiplexing and segment decoding.



Implementation:

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	37	0	0	63400	0.06
LUT as Logic	37	0	0	63400	0.06
LUT as Memory	0	0	0	19000	0.00
Slice Registers	58	0	0	126800	0.05
Register as Flip Flop	58	0	0	126800	0.05
Register as Latch	0	0	0	126800	0.00
F7 Muxes	4	0	0	31700	0.01
F8 Muxes	0	0	0	15850	0.00

Contributions:

Paul Kim - Source Codes, Testbench, Simulation - 50% contribution

Winson Zhu - Source Codes, Implementation, Hardware Demo - 50% contribution