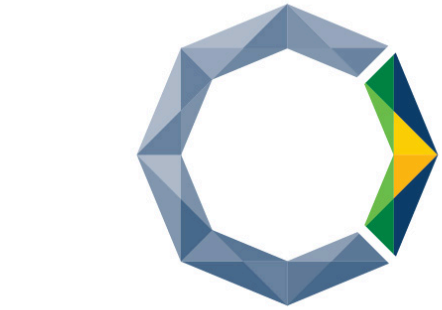

CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #2

Experiment #2

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& Daniel Mondragon Xicotencatl (StudentID: 012803856)

Presented to Mohamed Aly

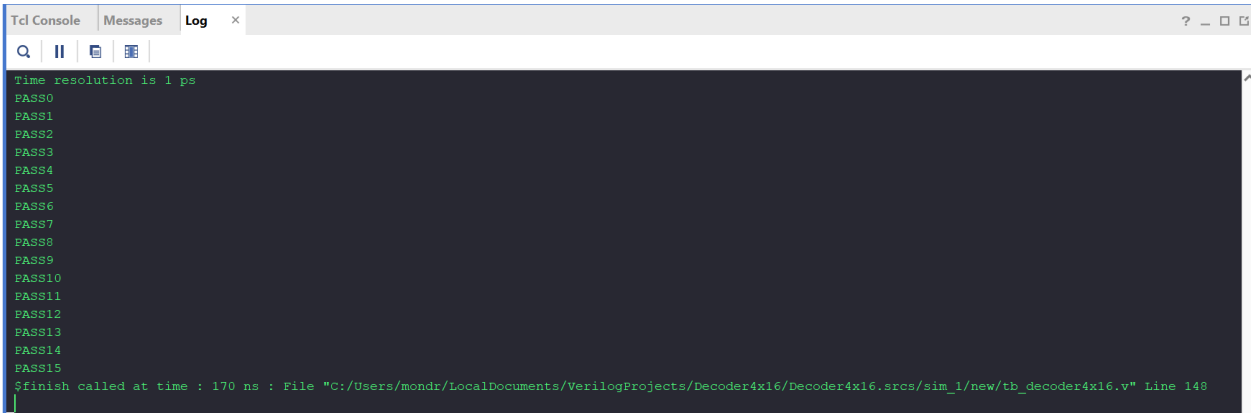
June 25th, 2025

Design:

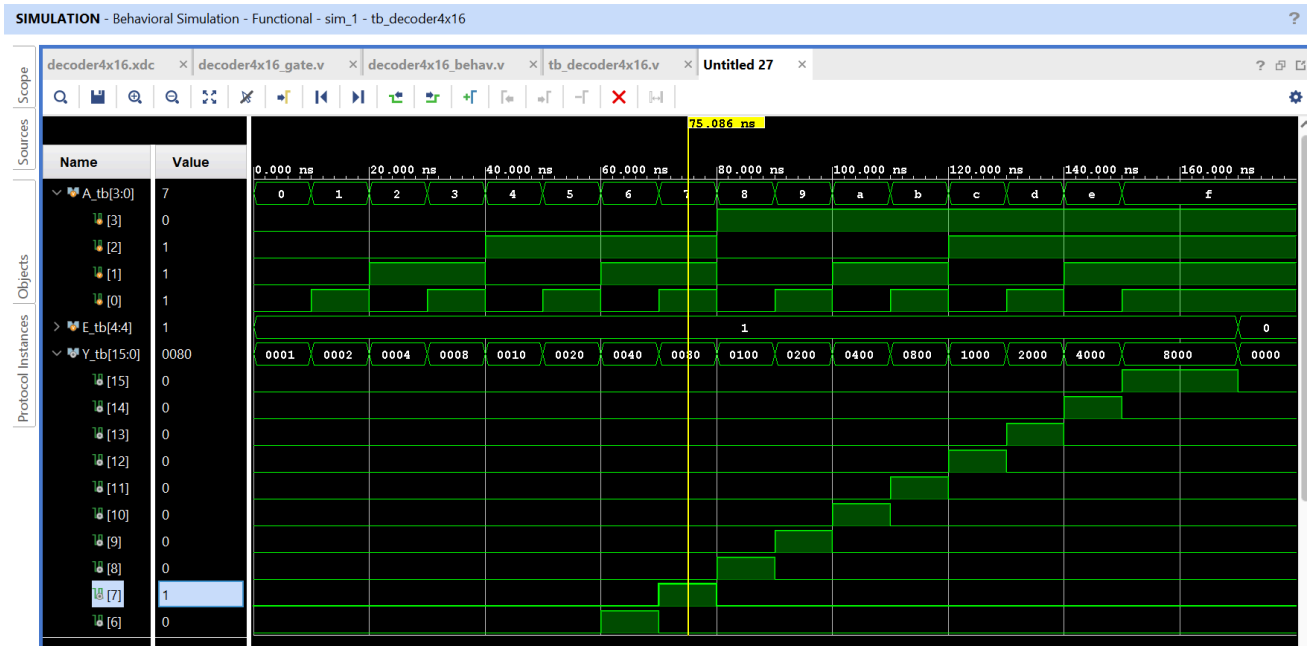
Gate-level design involves defining the circuit using basic logic gates like AND, OR, and NOT, which closely represents the physical hardware layout. Meanwhile, behavioral design describes what the circuit should do using conditional statements, making it more easy to understand at a foundational level. Gate-level design is more complex, providing insight into the circuit's physical structure, but it is more time consuming and less productive as the designs get more complex. Behavioral design is more consistent in more complex systems due to its simplicity.

Simulation:

TestBench Log Description: shows that all cases passed.



Sample Waveform Picture: We also tested for E = 0, at the end, the test bench confirms that all outputs stay LOW



Implementation:

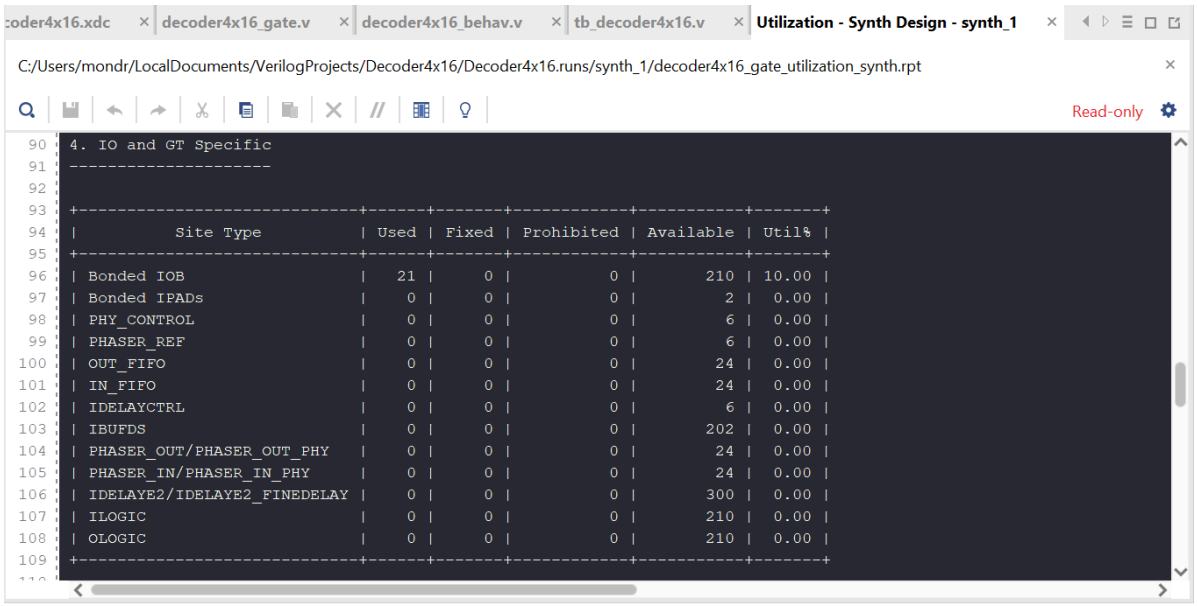
Utilization Table:

C:/Users/mondr/LocalDocuments/VerilogProjects/Decoder4x16/Decoder4x16.runs/synth_1/decoder4x16_gate_utilization_synth.rpt

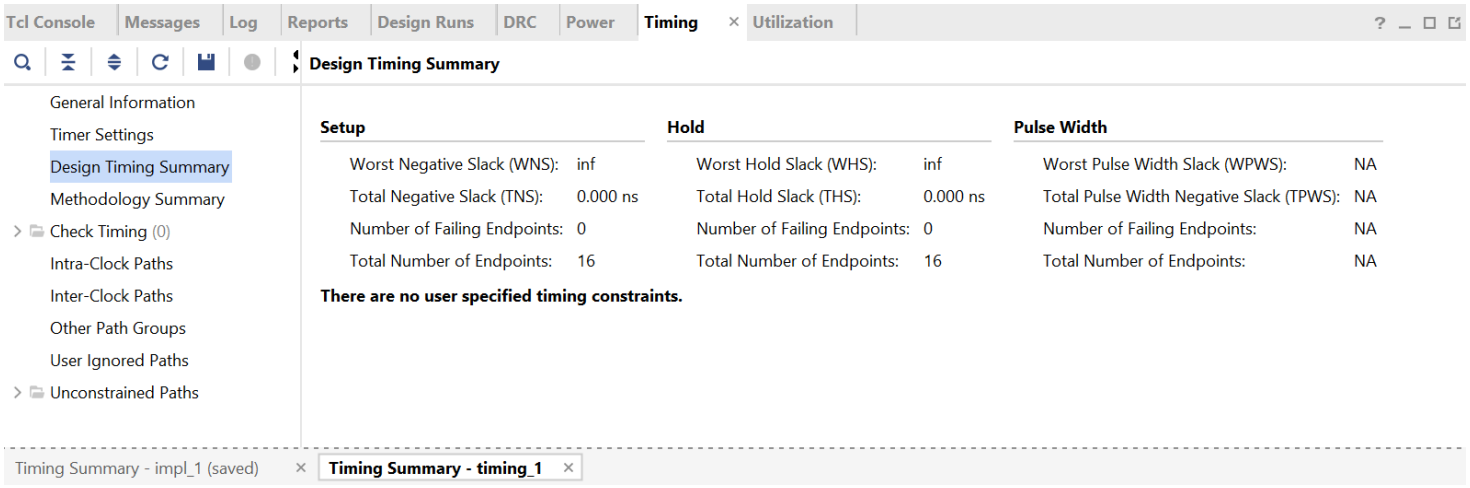
Read-only

```
1. Slice Logic
--------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |    8 |     0 |          0 |     63400 |  0.01 |
|   LUT as Logic          |    8 |     0 |          0 |     63400 |  0.01 |
|   LUT as Memory         |    0 |     0 |          0 |     19000 |  0.00 |
| Slice Registers         |    0 |     0 |          0 |    126800 |  0.00 |
|   Register as Flip Flop |    0 |     0 |          0 |    126800 |  0.00 |
|   Register as Latch     |    0 |     0 |          0 |    126800 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     31700 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     15850 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run
Warning! LUT value is adjusted to account for LUT combining.
Warning! For any ECO changes, please run place_design if there are unplaced instances
```



Timing Summary:



Contributions:

Daniel Mondragon + 50% effort

Kobe Aquino + 50% effort

Group Video Link: Here is the following link to our Lab 2 Group Demonstration Video:

https://youtu.be/5IJdcM6cmcI