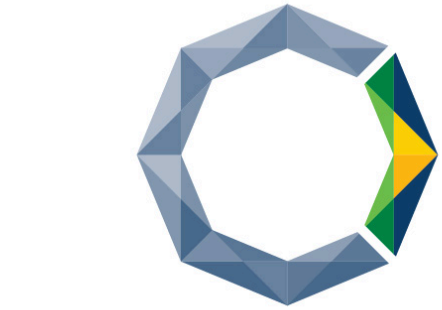


CalPolyPomona

College of Engineering

California Polytechnic State University Pomona

Department of Electrical & Computer Engineering

Digital Circuit Design Lab Verilog

ECE 3300L

Lab Report #5

Presented By: Kobe Aquino (StudentID: 015266433)

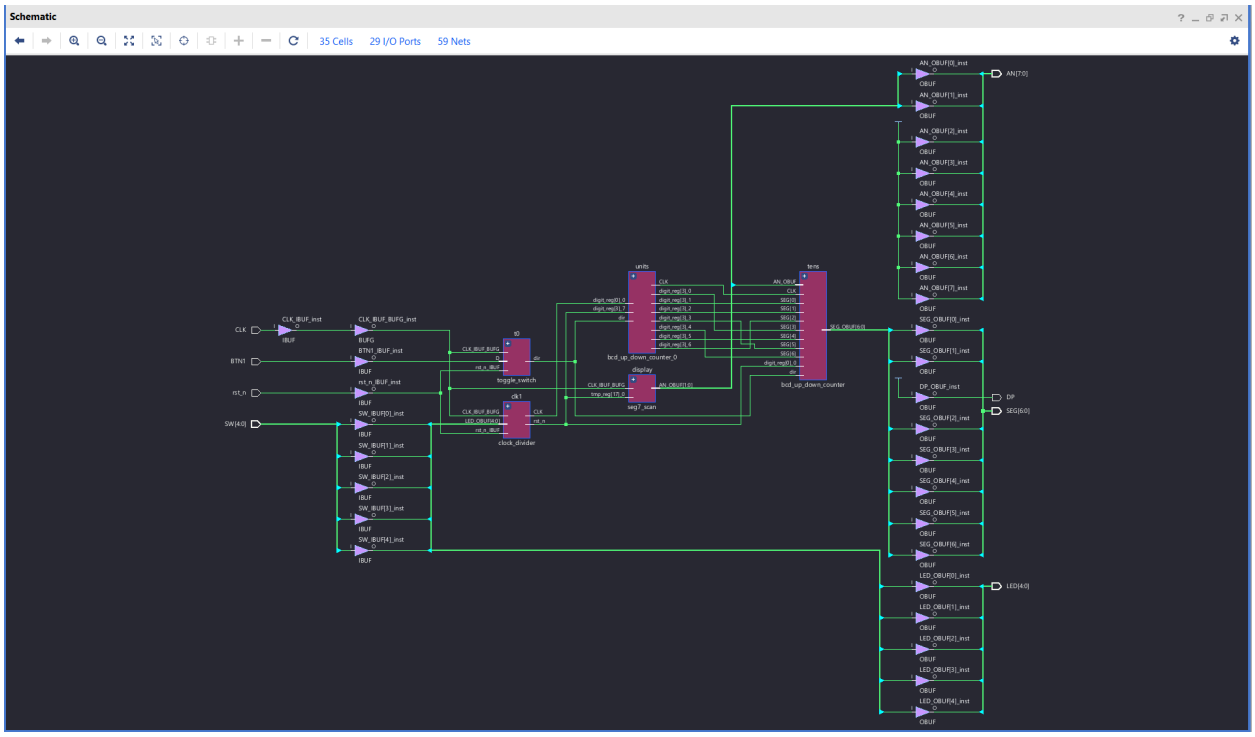
& Daniel Mondragon Xicotencatl (StudentID: 012803856)

Presented to Mohamed Aly

July 21, 2025

Objective: For this lab we designed a 2-digit BCD up/down counter in Verilog-HDL, by implementing a clock-divider that uses a 32-bit counter module with a 32x1 Mux module. The clock divider has 5 switch speed select, where 00000 is the slowest to 11111 being the fastest. We control the direction using Button C on the nexys A7, that when pressed reverses the direction. Naturally, the board starts at 0, then starts counting up, which also when the CPU Reset button is pressed, this is the state that resets it to. We modified HDL from last week's 7-segment driver to write the time multiplexer to drive the 2 7-segment displays.

Schematic:



Utilization:

Tcl Console | Messages | Log | Reports | Design Runs | DRC | Methodology | Power | Timing

```
9. Black Boxes
10. Instantiated Netlists

1. Slice Logic
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+----------------------------+------+-------+------------+-----------+-------+
|         Site Type          | Used | Fixed | Prohibited | Available | Util% |
+----------------------------+------+-------+------------+-----------+-------+
| Slice LUTs                 |   31 |     0 |          0 |     63400 |  0.05 |
|   LUT as Logic             |   31 |     0 |          0 |     63400 |  0.05 |
|   LUT as Memory            |    0 |     0 |          0 |     19000 |  0.00 |
| Slice Registers            |   64 |     0 |          0 |    126800 |  0.05 |
|   Register as Flip Flop    |   64 |     0 |          0 |    126800 |  0.05 |
|   Register as Latch        |    0 |     0 |          0 |    126800 |  0.00 |
| F7 Muxes                   |    4 |     0 |          0 |     31700 |  0.01 |
| F8 Muxes                   |    0 |     0 |          0 |     15850 |  0.00 |
+----------------------------+------+-------+------------+-----------+-------+
* Warning! LUT value is adjusted to account for LUT combining.
```
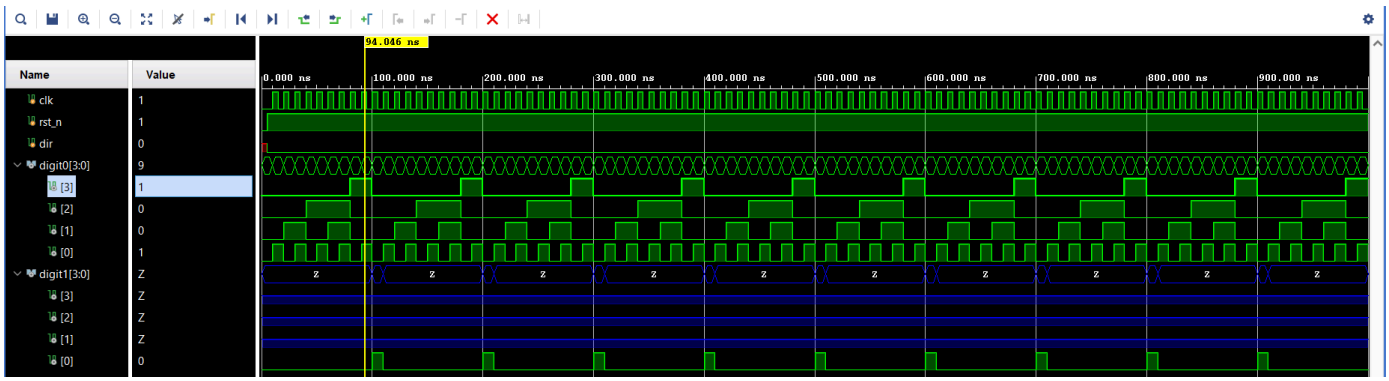
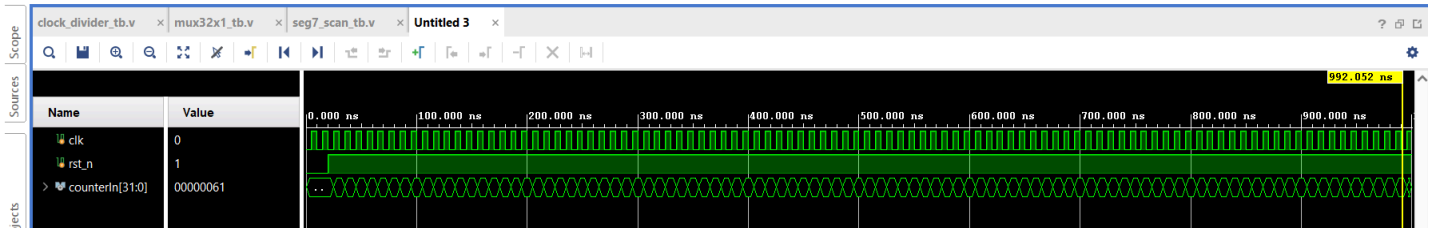

Simulation:

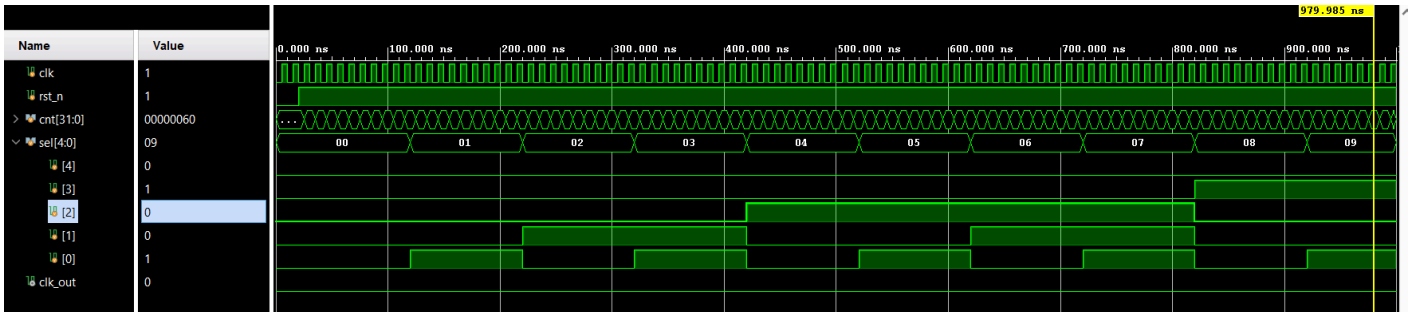
Bcd_up_down_counter_tb: Units properly counting 0-9, with the pulse correctly going 0-1 so that the tens count correctly from 0-9.



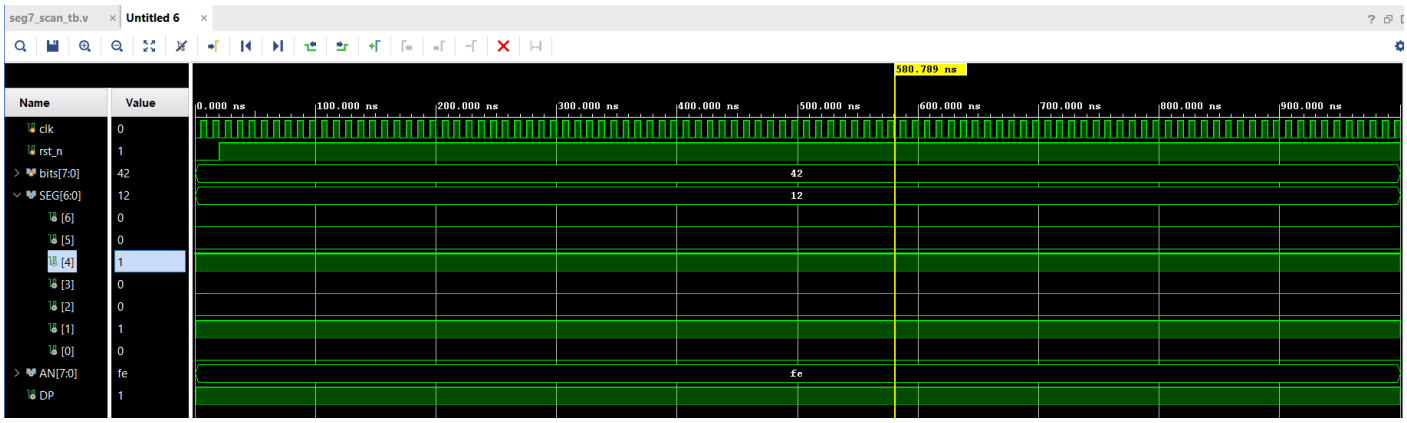
Clock_divider_tb:



mux32x1_tb:



seg7_scan_tb:



Team Contributions:

Daniel Mondragon Xicotencatl + 50%

Kobe Aquino + 50%

We both collaborated on the Verilog HDL by testing and modifying each other's modules, writing the test bench simulations together, and writing the report. Daniel uploaded to Github, and Kobe uploaded the demo to Youtube.