ECE 3300L.01 - Lab 5

BCD Up/Down Counter on 7-Segment Display

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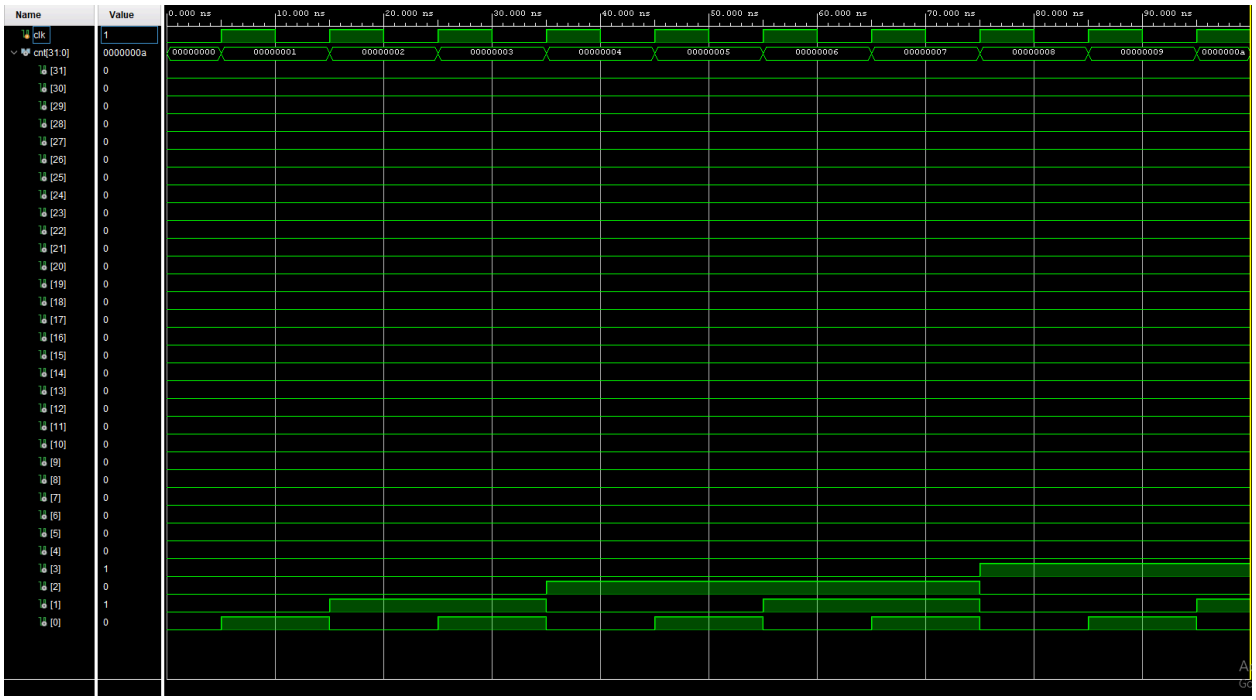
Objective:

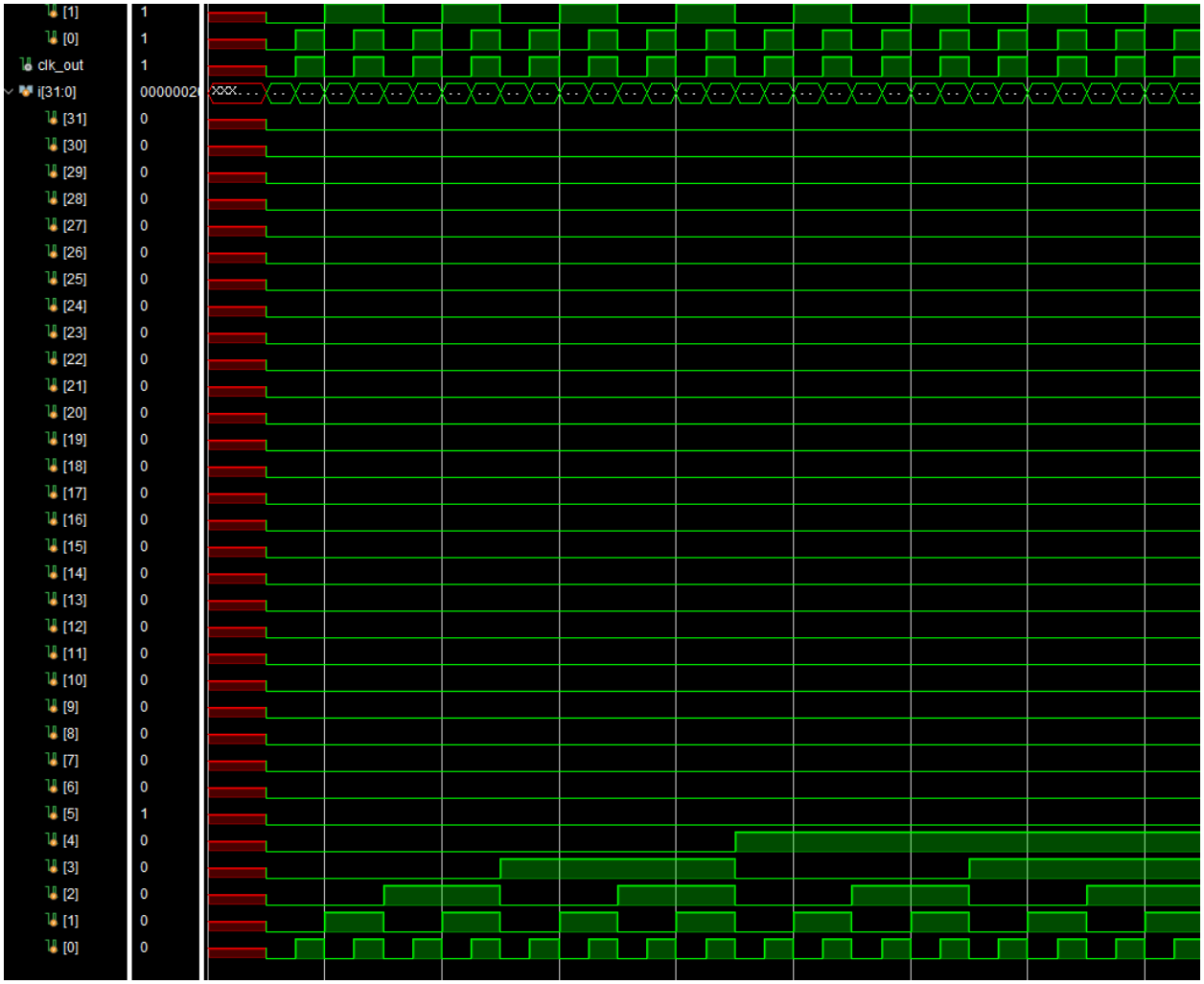
- Design a two-digit BCD up/down counter in Verilog-HDL.
- Implement a clock-divider with a 32-bit counter + 32×1 Mux and 5 SW speed select.
- Control counting direction via BTN1 (Up/Down) and reset via BTN0.
- Drive a dual-digit 7-segment display using multiplexing.
- Deploy on Nexys A7: simulate, synthesize, program, and test.

Testbench Waveform:

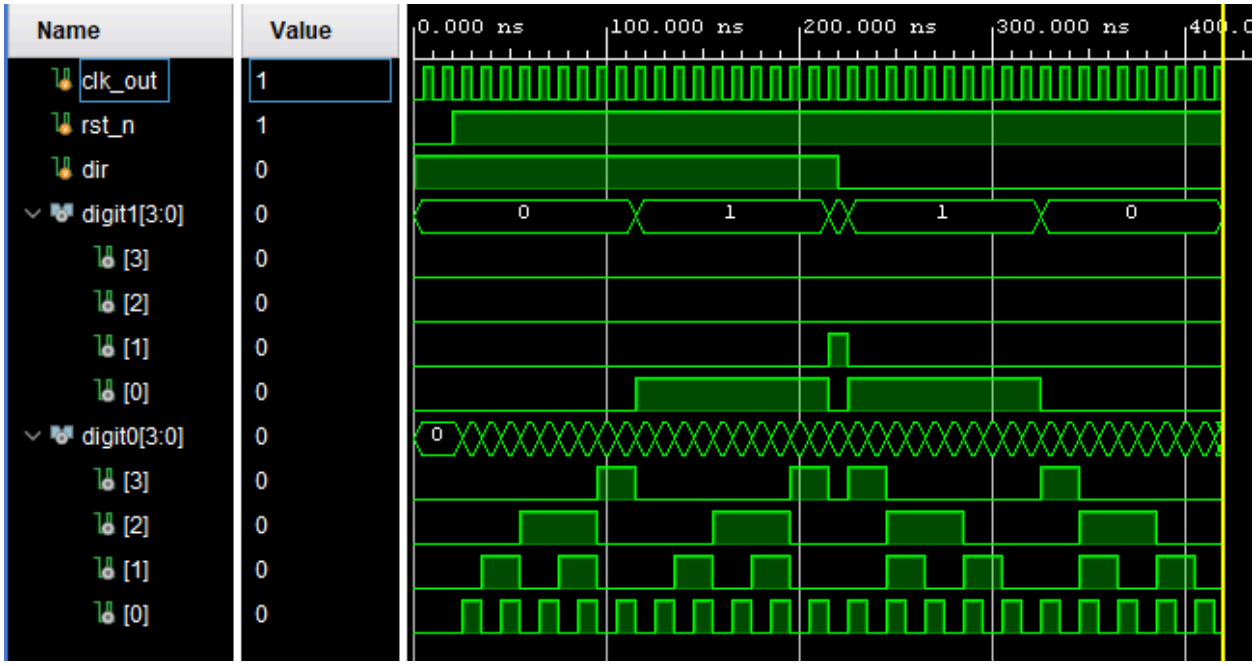
Clock Divider



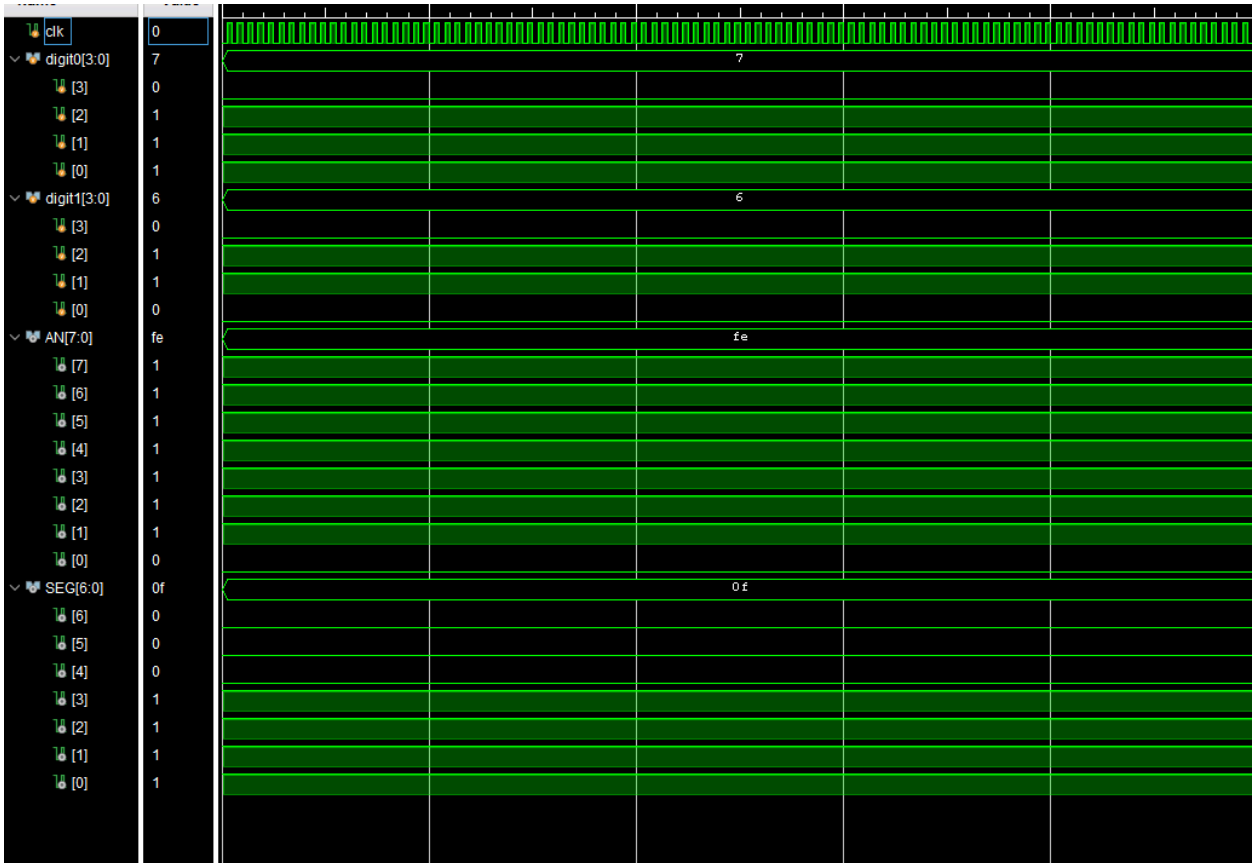
Mux 32x1


[1]
[0]
clk_out
i[31:0]
[31]
[30]
[29]
[28]
[27]
[26]
[25]
[24]
[23]
[22]
[21]
[20]
[19]
[18]
[17]
[16]
[15]
[14]
[13]
[12]
[11]
[10]
[9]
[8]
[7]
[6]
[5]
[4]
[3]
[2]
[1]
[0]

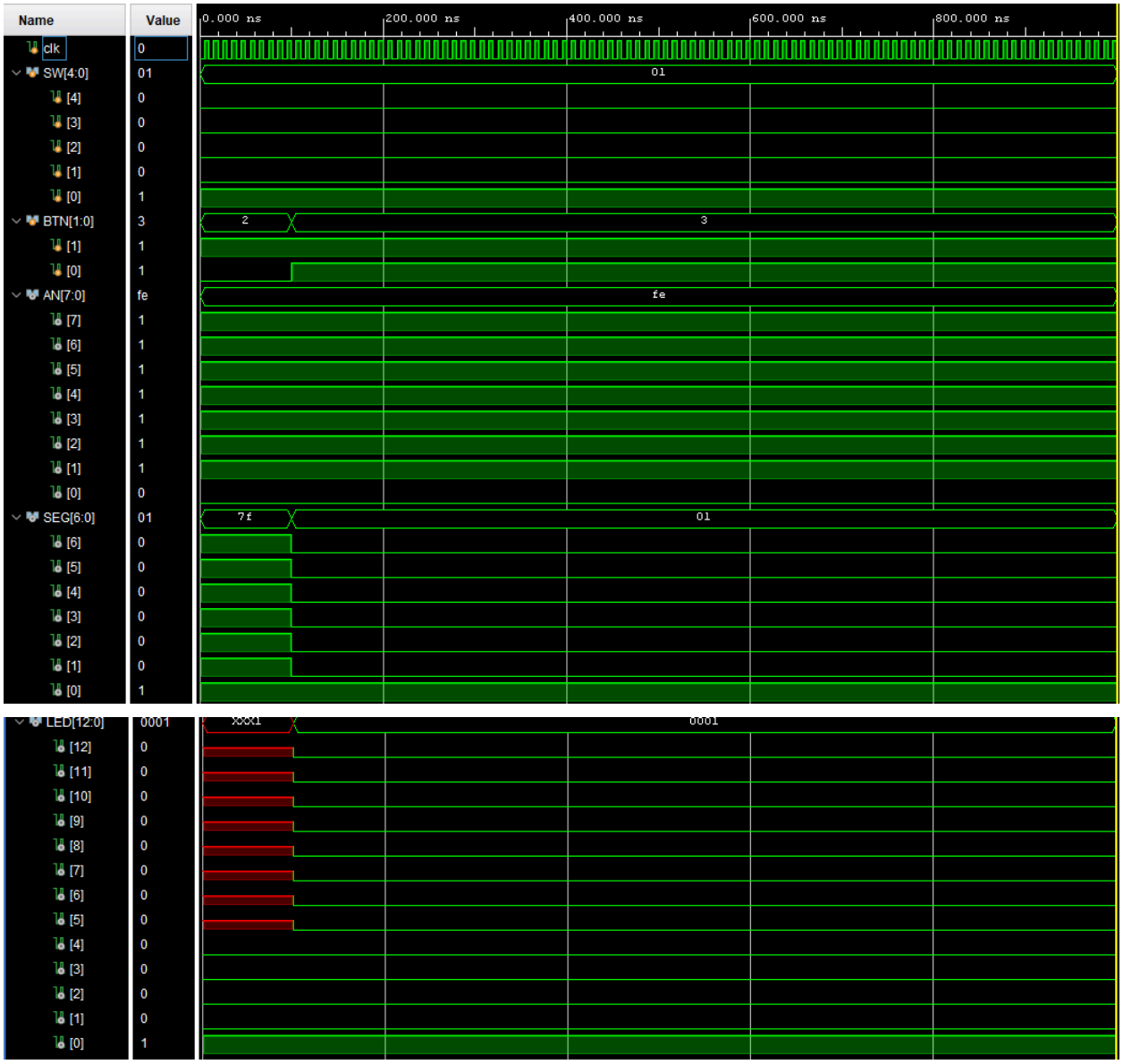
BCD Counter



7 Segment Display

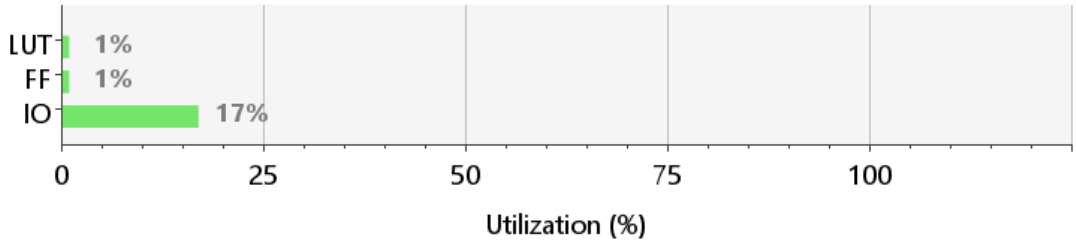


Top module


Name
Value
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
clk
0
SW[4:0]
01
[4]
0
[3]
0
[2]
0
[1]
0
[0]
1
BTN[1:0]
3
2
3
[1]
1
[0]
1
AN[7:0]
fe
fe
[7]
1
[6]
1
[5]
1
[4]
1
[3]
1
[2]
1
[1]
1
[0]
0
SEG[6:0]
01
7f
01
[6]
0
[5]
0
[4]
0
[3]
0
[2]
0
[1]
0
[0]
1
LED[12:0]
0001
XXX1
0001
[12]
0
[11]
0
[10]
0
[9]
0
[8]
0
[7]
0
[6]
0
[5]
0
[4]
0
[3]
0
[2]
0
[1]
0
[0]
1

Utilization/Implementation:

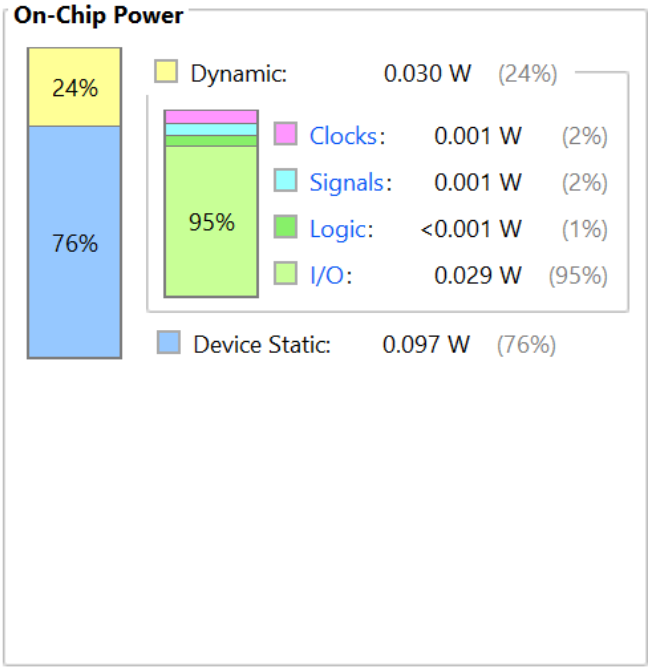
Resource	Utilization	Available	Utilization %
LUT	28	63400	0.04
FF	56	126800	0.04
IO	36	210	17.14



Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.127 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (12.9 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Contributions:

Jared Mocling (50%) - board demo, compiled code, report.
Kevin Tang (50%)- compiled code, simulation code, Synthesis reports, report