CALIFORNIA STATE POLYTECHNIC
UNIVERSITY, POMONA
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LAB 8

RGB LED PWM Controller

ECE 3300L Summer 2025

Digital Circuit Design using Verilog

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Objective

This project implements PWM-based control of an RGB LED, using switches to adjust the duty cycles for each color channel and set the overall resolution. To achieve this, clock division is employed to create a low-frequency signal for the debounce logic and a high-frequency clock for the PWM signal generation. User interaction is handled by debounced push buttons, which, combined with a one-pulse generator, provide clean inputs to a finite state machine that cycles through the color channels and resolution settings. The design is mapped to the specific hardware pins of a Nexys A7 board by matching the Vivado constraints for the LEDs, switches, pushbuttons, and clock. A key consideration is driving the active-low RGB LED (LED16), which requires ensuring the correct signal polarity is handled within the hardware driver.

Hardware Pin Mapping System

& Control:

- **clk100mhz:** Input, Pin E3, 100 MHz system clock
- **btnc_n:** Input, Pin N17, Center push button (active-low reset)
- **btnr:** Input, Pin M18, Right push button (FSM control)

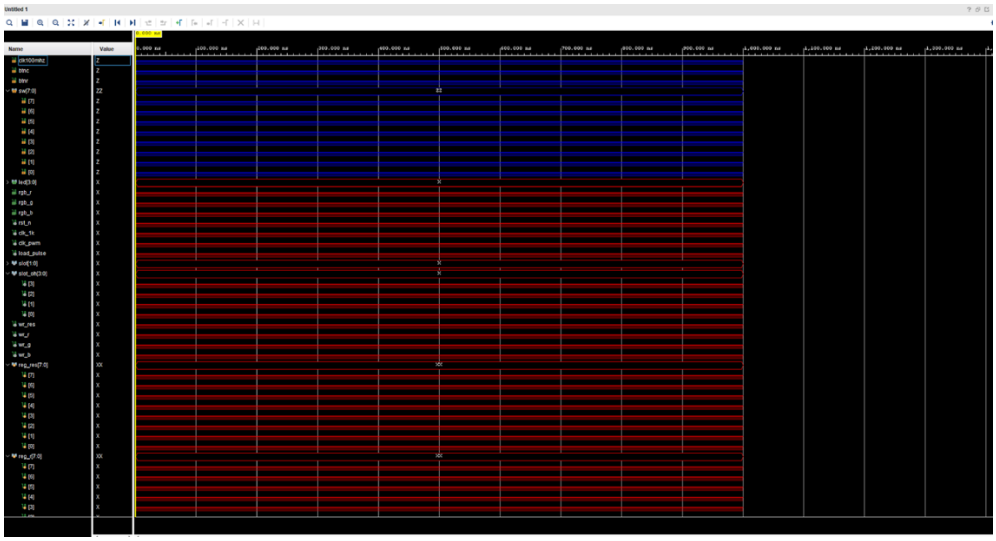
Switches:

- **sw[0]:** Input, Pin J15, Switch 0
- **sw[1]:** Input, Pin L16, Switch 1
- **sw[2]:** Input, Pin M13, Switch 2
- **sw[3]:** Input, Pin R15, Switch 3
- **sw[4]:** Input, Pin R17, Switch 4
- **sw[5]:** Input, Pin T18, Switch 5
- **sw[6]:** Input, Pin U18, Switch 6
- **sw[7]:** Input, Pin R13, Switch 7 **LED Outputs:**

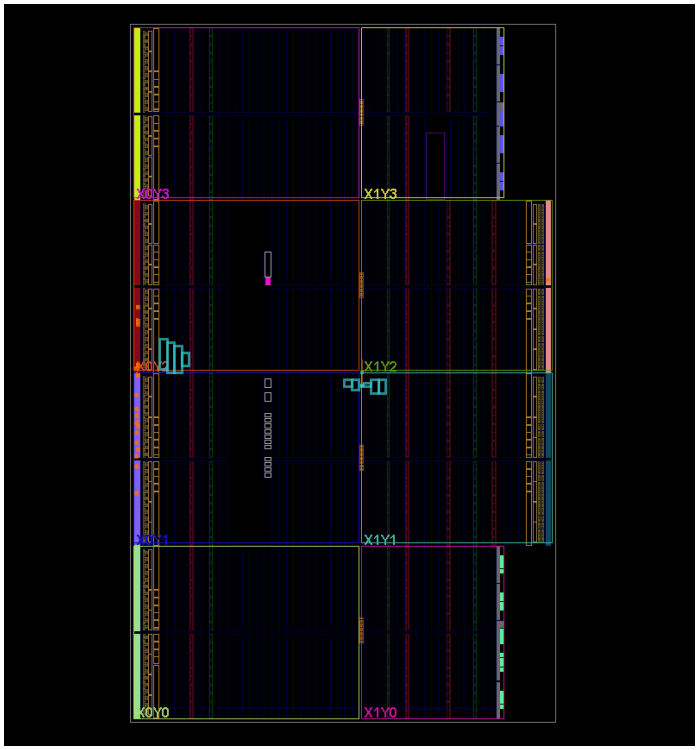
- **led[0]:** Output, Pin H17, Discrete LED 0
- **led[1]:** Output, Pin K15, Discrete LED 1 ● **led[2]:** Output, Pin J13, Discrete LED 2
- **led[3]:** Output, Pin N14, Discrete LED 3
- **rgb_r:** Output, Pin N15, LED16 Red (active-low)
- **rgb_g:** Output, Pin M16, LED16 Green (active-low)
- **rgb_b:** Output, Pin R12, LED16 Blue (active-low)

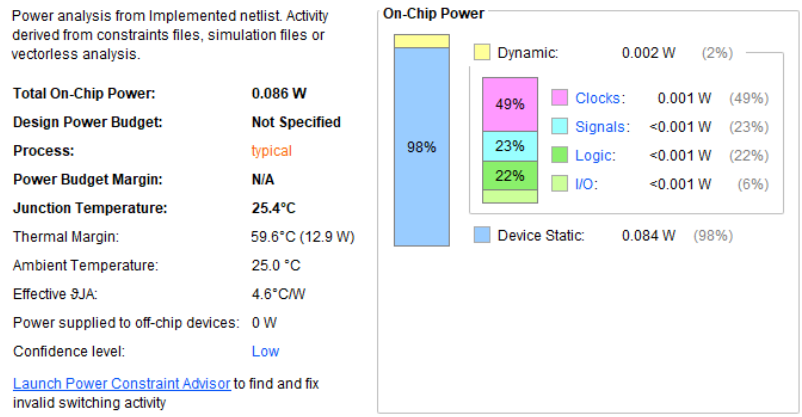
Synthesis and Implementation

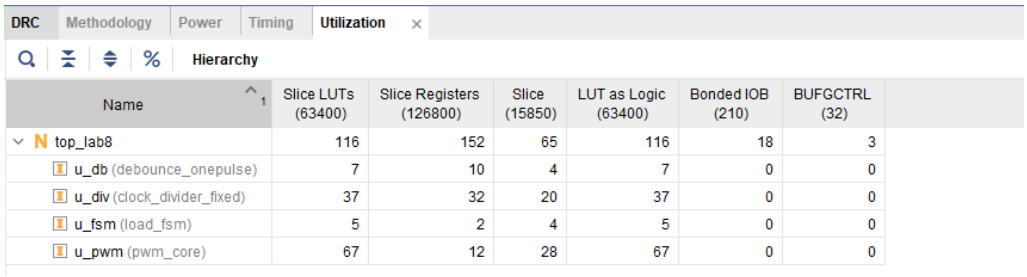
pwm_core_tb



Vivado Utilization







Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
top_lab8	116	152	65	116	18	3
u_db (debounce_onepulse)	7	10	4	7	0	0
u_div (clock_divider_fixed)	37	32	20	37	0	0
u_fsm (load_fsm)	5	2	4	5	0	0
u_pwm (pwm_core)	67	12	28	67	0	0

Partner Contribution

Clay Kim: Source Code and Implementation

Changwe Musonda: Testbench and Demonstration Video

Reflections

Reflecting on this project, several design choices were fundamental to achieving a stable and user-friendly outcome. A key takeaway was the absolute necessity of robust button debouncing. Initially, without a proper debounce and one-pulse circuit, the mechanical bounce from the push buttons caused multiple, unintended triggers of the finite state machine. Implementing a 1 kHz sampling clock for this logic proved to be the right solution. This highlighted the broader importance of clock domain separation—using a low-frequency clock for the user interface logic while driving the PWM with a high-frequency clock was critical for preventing any visual flicker and ensuring smooth color transitions on the LED. To maintain data integrity between these domains, especially when updating duty cycle or resolution values, two-stage register synchronization was essential to prevent glitches. Finally, small details in the hardware interface made a significant difference. Properly handling the active-low signal for the RGB LED was a simple but crucial step. Using the discrete LEDs to visually indicate which parameter was

selected for editing provided an intuitive and effective user feedback mechanism, making the entire system much easier to test and operate.