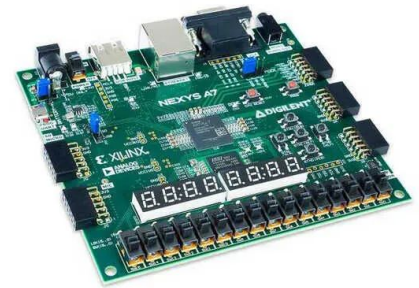

ECE 4301 Final Project

By Winson, Paul, Linus, Minh

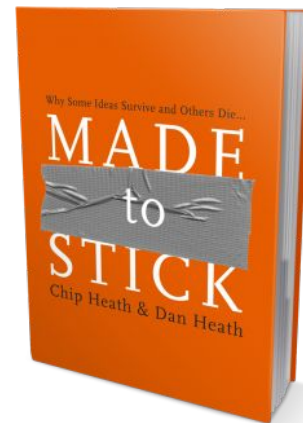
Project Vision + Deliverables

- Goal:
 - Complete performance benchmark between RSA and ECC algorithms running on RISC-V soft core inside Nexys A7 100T
- Deliverables:
 - Code (in rust?)
 - Tables + Charts comparing RSA vs ECC performance
 - Demo
 - Doc with final results of RSA and ECC performance



Roles + Milestones

1. Build RISC-V system
 - a. Get RISC-V soft-core running on FPGA
2. Benchmark RSA and ECC
3. Data Analysis



Toolchain/Hardware Plan

1. Vivado
 - a. Maps the RISC-V CPU and peripherals into FPGA logic cells
2. LiteX Framework
 - a. Python-based SoC builder that generates Verilog for a complete RISC-V system
3. VexRiscv
 - a. Soft processor (open source RISC-V CPU, runs any RV32I/M/C machine code), will execute Rust
4. Rust ToolChain + Crates
 - a. For crypto algorithms and implementing them
5. Python
 - a. For Data analysis, turning raw UART output into tables and plots