Laurel Electronics Co., Ltd.

LCD Module Specification

Model No.: LG240645-FFDWH6V-V33
LG240645-BMDWH6V-V33

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RECORD OF REVISION

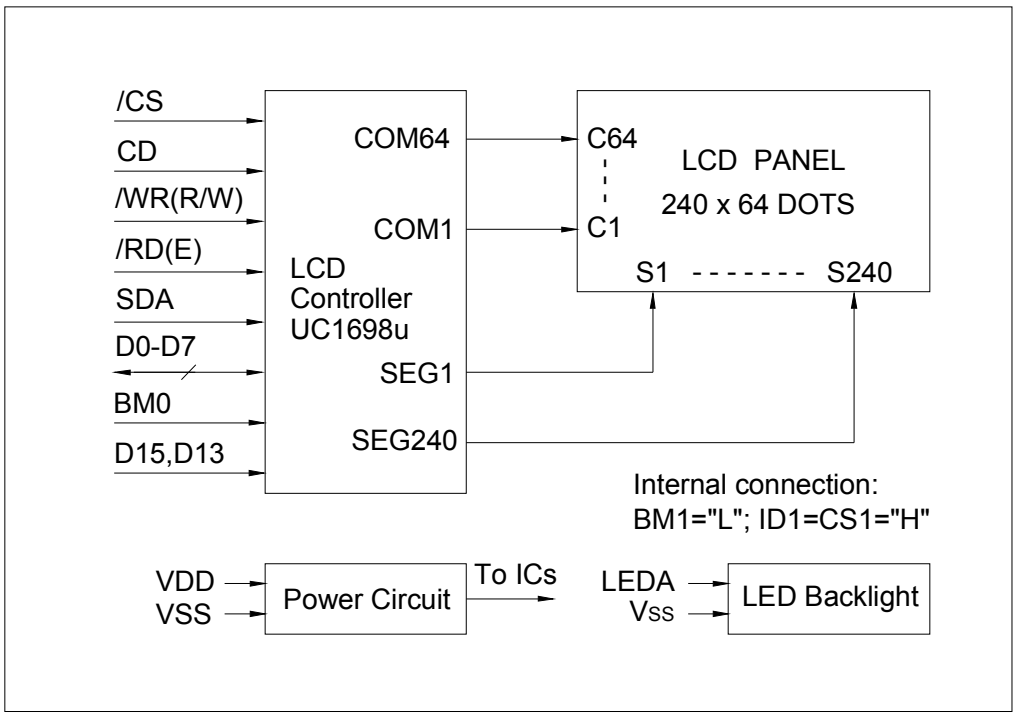
Rev.	Date	Page	Item	Description
0.1	2012/10/16	-	-	New release
0.2	2013/02/26	16	8	Update dimensional outline

1. BASIC SPECIFICATIONS

1.1 Features

Item		Specifications	Unit
Display Format		240 x 64	dot
LCD Type	FFDWH6V-V33	FSTN - Positive - Transflective Black characters on white background	-
	BMDWH6V-V33	STN - Blue - Negative - Transmissive White characters on blue background	-
Driving Method		1/64 Duty, 1/10 Bias	-
Viewing Direction		6	O'clock
Backlight & Color		LED, white color	-
Outline Dimension (WxHxT)		120.0 x 40.5 x 10.5	mm
Viewing Area (WxH)		91.0 x 27.2	mm
Active Area (WxH)		86.38 x 24.3	mm
Dot Pitch (WxH)		0.36 x 0.38	mm
Dot Size (WxH)		0.34 x 0.36	mm
Weight		48	g
Controller		UC1698u (COG)	-
Interface		8-bit parallel (8080 or 6800), 3/4-wire SPI	-
Power Supply (VDD)		3.0 to 3.3	V

1.2 Block Diagram



1.3 Terminal Functions (CN1: Thru Holes Terminals, CN2: FFC Terminals)

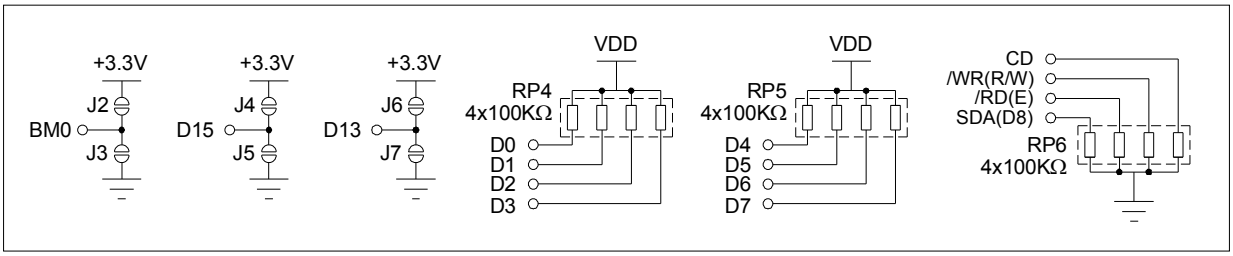
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Level</th><th>Function</th></tr>
<tr><td>1</td><td>VSS</td><td>0V</td><td>Ground</td></tr>
<tr><td>2</td><td>VDD</td><td>3V to 3.3V</td><td>Power supply for logic.</td></tr>
<tr><td>3</td><td>LEDA</td><td>3.3V</td><td>Power supply for LED backlight.
LEDK is connected to Vss on PCB.
Refer to section 3.6 to 3.7</td></tr>
<tr><td>4</td><td>CD</td><td>H/L</td><td>Data or instruction selection
CD=“L”: D0 to D7 are Instruction code;
CD=“H”: D0 to D7 are display data.
In S9 mode, CD pin is not used, connect it to VSS.</td></tr>
<tr><td>5</td><td>/CS</td><td>L</td><td>Chip selection signal. Active “L”.</td></tr>
<tr><td>6</td><td>SDA(D8)</td><td>H/L</td><td>Serial data input.</td></tr>
<tr><td>7</td><td>SCK(D0)</td><td rowspan="8">H/L</td><td rowspan="8">Bi-directional bus for parallel host interfaces. In serial modes, connect D0 to SCK, D8 to SDA and D[15,13] to VDD or VSS.
<table>
<tr><td></td><td>BM[1:0]=0x
8-bit parallel (ID1=1)</td><td>BM[1:0]=00
S8</td><td>BM[1:0]=00
S8uc</td><td>BM[1:0]=01
S9</td></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>D2</td><td>D2</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>D3</td><td>D3</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>D4</td><td>D4</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>D5</td><td>D5</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>D6</td><td>D6</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>D7</td><td>D7</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>D8</td><td>-</td><td>SDA</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D13</td><td>-</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>D15</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Connect unused pins to VDD or VSS.
BM1 is fixed to “0” and ID1 is fixed to “1” by internal connection.</td></tr>
<tr><td>8</td><td>D1</td></tr>
<tr><td>9</td><td>D2</td></tr>
<tr><td>10</td><td>D3</td></tr>
<tr><td>11</td><td>D4</td></tr>
<tr><td>12</td><td>D5</td></tr>
<tr><td>13</td><td>D6</td></tr>
<tr><td>14</td><td>D7</td></tr>
<tr><td>15</td><td>/WR
(R/W)</td><td>H/L</td><td>/WR signal for 8080 series MPU. Write data at rising edge of /WR.
R/W signal for 6800 series MPU. R/W=“H”: Read; R/W=“L”: Write.
In serial modes, /WR(R/W) is not used, connect it to VSS.</td></tr>
<tr><td>16</td><td>/RD(E)</td><td>H/L</td><td>/RD signal for 8080 series MPU. Read data when /RD is “L”
Enable signal for 6800 series MPU. Read data when E is “H”, write data at falling edge of E.
In serial modes, /RD(E) is not used, connect it to VSS.</td></tr>
</table>

Note: D0 to D7 signals are pulled to VDD by on-board 100KΩ resistors. SDA, CD, /WR and /RD signals are pulled to VSS by on-board 100KΩ resistors. Pin 8 to Pin 16 can be kept open in serial interface mode.

1.4 Set Bus Mode by on Board Jumpers

The interface bus mode is determined by BM[1:0] and D[15,13] levels. The relationship between jumper status, BM[1:0], D[15,13] levels and interface bus mode is below.

Jumper Status (C=Close; O=Open)								BM[1:0] Level	D[15,13] Level	Interface Bus Mode
J2	J3	J4	J5	J6	J7	J8	J9			
O	C	O	C	O	C	O	O	00	00	8080/8-bit **<Default>**
C	O	O	C	O	C	O	O	01	00	6800/8-bit
O	C	C	O	O	C	O	O	00	10	4-wire SPI (S8)
O	C	C	O	C	O	O	O	00	11	3/4-wire SPI (S8uc)
C	O	C	O	O	C	O	O	01	10	3-wire SPI (S9)



2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	-0.3	4.0	V
LCD Driving Voltage	VLCD	-0.3	19.8	V
Input Voltage	VIN	-0.4	VDD+0.5	V
Operating Temperature	Topr	-20	+70	°C
Storage Temperature	Tstg	-30	+80	°C

3. ELECTRICAL CHARACTERISTICS

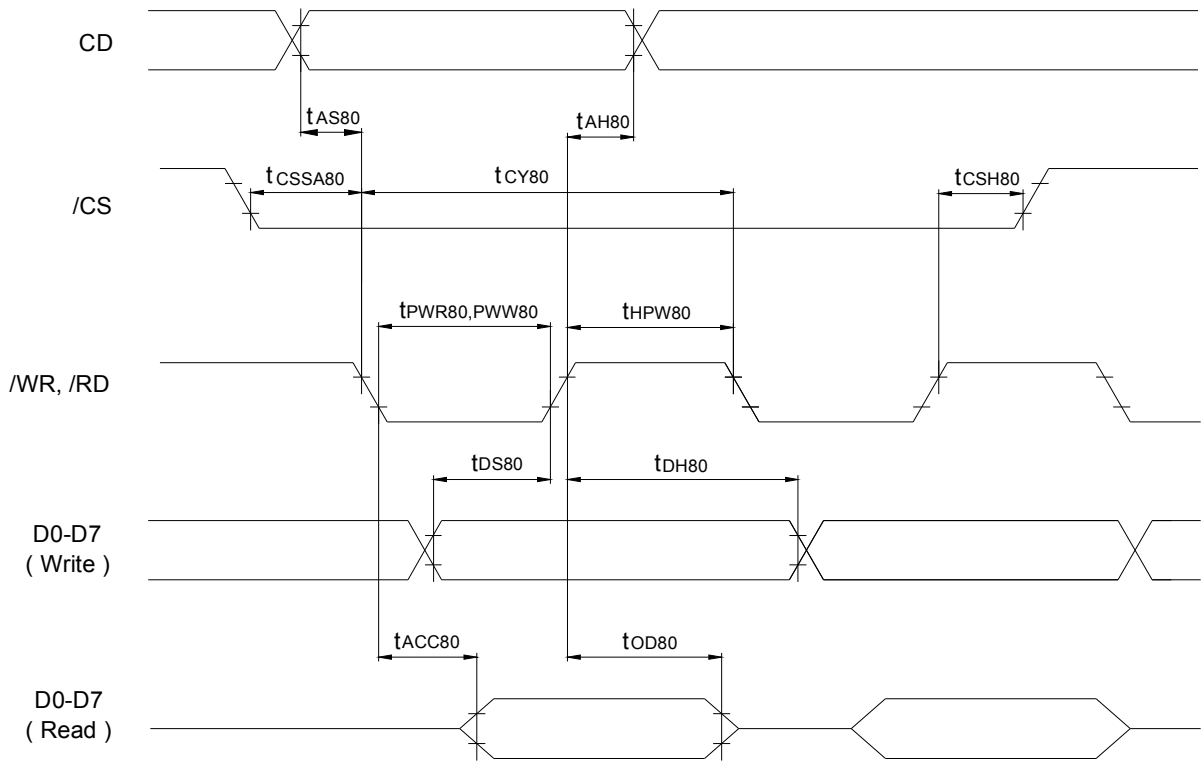
3.1 DC Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDD		3.0	-	3.3	V
Charge Pump Output	VLCD		-	13.2	-	V
Input Low Voltage	VIL		0	-	0.2VDD	V
Input High Voltage	VIH		0.8VDD	-	VDD	V
Output Low Voltage	VOL		0	-	0.2VDD	V
Output High Voltage	VOH		0.8VDD	-	VDD	V
Supply Current	IDD	VDD=3.3V VLCD=13.2V	-	2.0	2.5	mA

3.2 Parallel Bus Timing Characteristics (8080 Series MPU, VDD=3.0V to 3.3V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	CD	t_{AS80} t_{AH80}		0 0	-	ns
System cycle time 8 bits bus (read) (write)	/RD, /WR	t_{CY80}	 LC[7:6]=10b LC[7:6]=01b	 100 80 90	-	
Low pulse width 8 bits bus (read) (write)	/RD, /WR	t_{PWR80} t_{PWW80}	 LC[7:6]=10b LC[7:6]=01b	 50 40 45	-	
High pulse width 8 bits bus (read) (write)	/RD, /WR	t_{HPW80}	 LC[7:6]=10b LC[7:6]=01b	 50 40 45	-	
Data setup time Data hold time	D0 to D7	t_{DS80} t_{DH80}		30 0	-	
Read access time Output disable time	D0 to D7	t_{ACC80} t_{OD80}	CL=100pF	- 15	60 30	
Chip select setup time Chip select hold time	/CS	t_{CSSA80} t_{CSH80}		5 5	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

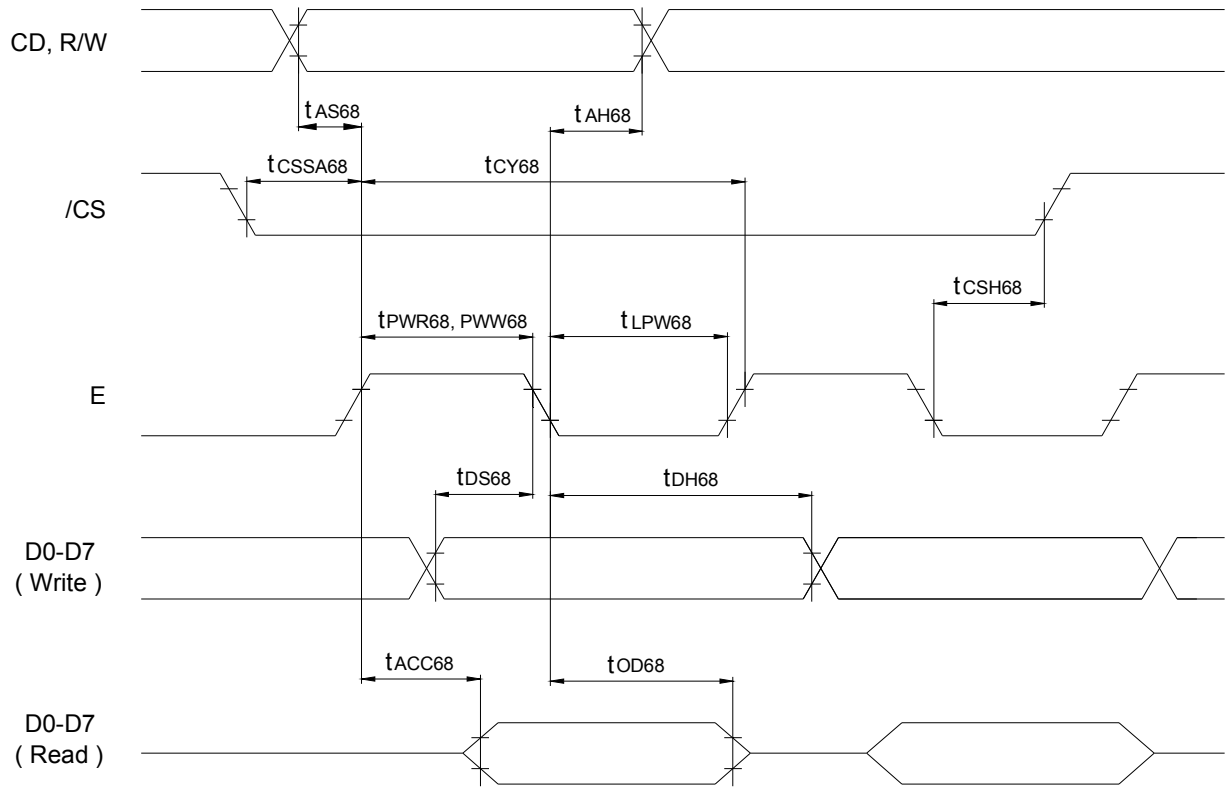


Parallel Bus Timing Characteristics (for 8080 MPU)

3.3 Parallel Bus Timing Characteristics (6800 Series MPU, VDD=3.0V to 3.3V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	CD, R/W	t_{AS68} t_{AH68}		0 0	-	ns
System cycle time 8 bits bus (read) (write)	E	t_{CY68}	 LC[7:6]=10b LC[7:6]=01b	100 80 90	-	
Pulse width 8 bits bus (read)	E	t_{PWR68}		50	-	
Pulse width 8 bits bus (write)	E	t_{PWW68}	LC[7:6]=10b LC[7:6]=01b	40 45	-	
Low pulse width 8 bits bus (read) (write)	E	t_{LPW68}	 LC[7:6]=10b LC[7:6]=01b	50 40 45	-	
Data setup time Data hold time	D0 to D7	t_{DS68} t_{DH68}		30 0	-	
Read access time Output disable time	D0 to D7	t_{ACC68} t_{OD68}	CL=100pF	- 15	60 30	
Chip select setup time Chip select hold time	/CS	t_{CSSA68} t_{CSH68}		5 5	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

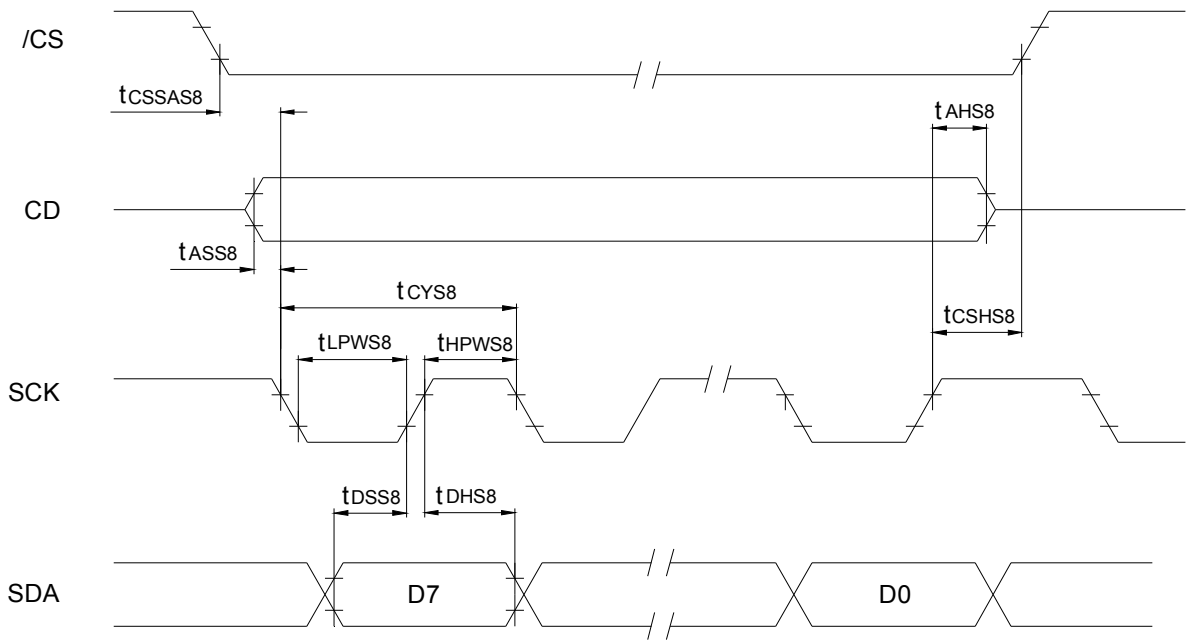


Parallel Bus Timing Characteristics (for 6800 MPU)

3.4 Serial Bus Timing Characteristics (for S8/S8uc, VDD=3.0V to 3.3V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	CD	t_{ASS8}		0	-	ns
Address hold time		t_{AHS8}		0	-	
System cycle time	SCK	t_{CYS8}		40	-	
Low pulse width		t_{LPWS8}		20	-	
High pulse width		t_{HPWS8}		20	-	
Data setup time Data hold time	SDA	t_{DSS8} t_{DHS8}		15 0	-	
Chip select setup time Chip select hold time	/CS	t_{CSSAS8} t_{CSHS8}		5 5	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

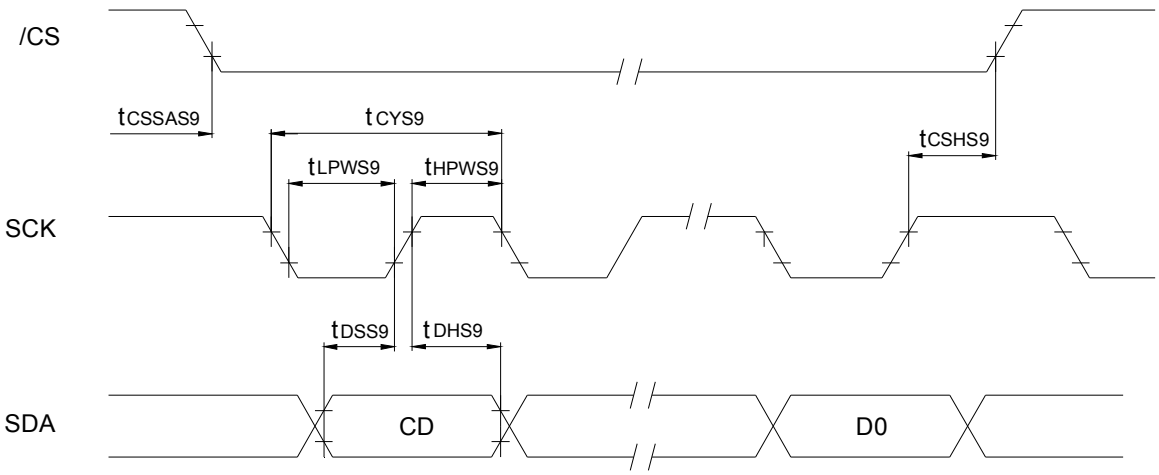


Serial Bus Timing Characteristics (for S8/S8uc)

3.5 Serial Bus Timing Characteristics (for S9, VDD=3.0V to 3.3V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time	SCK	t_{CYS9}		40	-	
Low pulse width		t_{LPWS9}		20	-	
High pulse width		t_{HPWS9}		20	-	
Data setup time Data hold time	SDA	t_{DSS9} t_{DHS9}		15 0	-	
Chip select setup time Chip select hold time	/CS	t_{CSSAS9} t_{CSHS9}		5 5	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

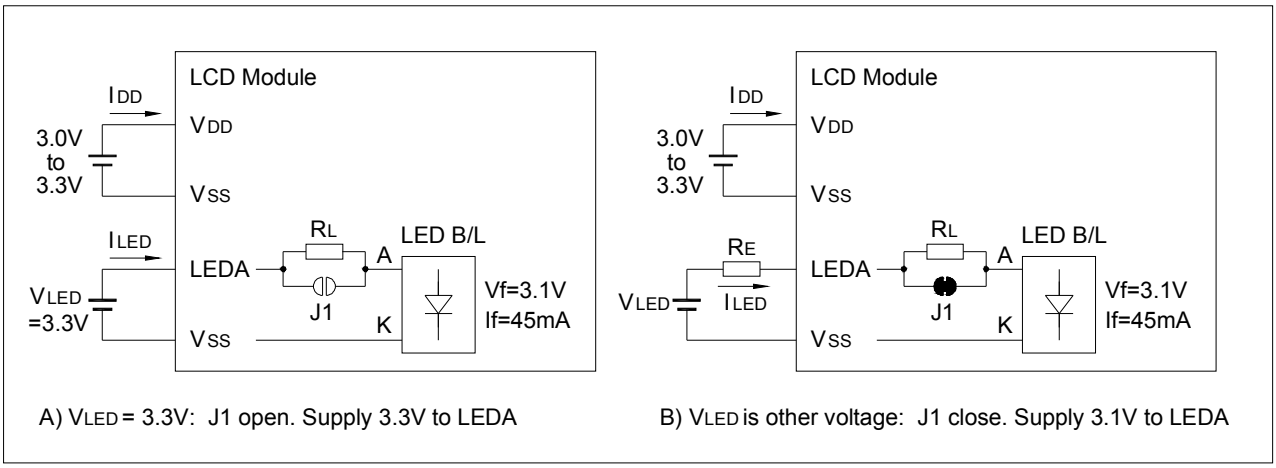


Serial Bus Timing Characteristics (for S9)

3.6 LED Backlight Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	Vf		2.9	3.1	3.3	V
Forward Current	If	Vf=3.1V	-	45	-	mA
Color	White					

3.7 Power Supply for Logic and LED Backlight



A) VLED = 3.3V: J1 open. Supply 3.3V to LEDA

B) VLED is other voltage: J1 close. Supply 3.1V to LEDA

* RL (internal) and RE (external) are the current limiting resistors for LED backlight

1) VLED=3.3V: J1 open. Supply 3.3V to LEDA (Pin 3) **<Default>**

2) VLED=5.0V: J1 open; RE=(5.0V-3.3V)/45mA=38Ω. Supply 3.3V to LEDA (Pin 3)

3) VLED=5.0V: J1 close; RE=(5.0V-3.1V)/45mA=43Ω. Supply 3.1V to LEDA (Pin 3)

4) VLED is other voltage: J1 close; RE=(VLED-3.1V)/45mA. Supply 3.1V to LEDA (Pin 3)

4. DISPLAY CONTROL COMMANDS

The following is a list of host commands supported by UC1698u.

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status&PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver	PMO[6:0]								
				Product Code(8h)				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R] [7:0] R=0 or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set V_{BIAS} Potentiometer (double-byte ommand)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H
		0	0	#	#	#	#	#	#	#	#		
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set{FLT,FLB}	0
		0	0	#	#	#	#	#	#	#	#		
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH
				-	-	-	#	#	#	#	#		
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0(BGR)
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A

Command Table (continued)

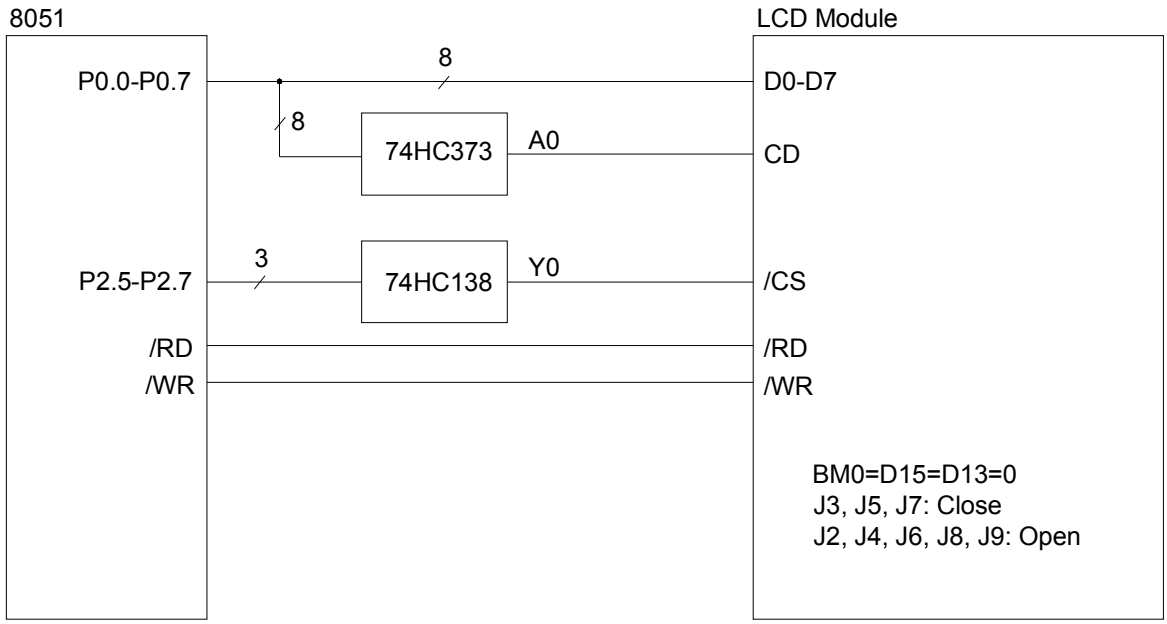
	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
25	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.		N/A
		0	0	#	#	#	#	#	#	#	#			
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]		11b:12
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]		159
		0	0	-	#	#	#	#	#	#	#			
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]		0
		0	0	-	#	#	#	#	#	#	#			
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]		159
		0	0	-	#	#	#	#	#	#	#			
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP Commands	Set WPC0	0
		0	0	-	#	#	#	#	#	#	#			
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1		Set WPP0	0
		0	0	#	#	#	#	#	#	#	#			
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0		Set WPC1	127
		0	0	-	#	#	#	#	#	#	#			
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1		Set WPP1	159
		0	0	#	#	#	#	#	#	#	#			
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Inside
35	Set MTP Operation Control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]		10H
		0	0	-	-	-	#	#	#	#	#			
36	Set MTP write mask	0	0	1	0	1	1	1	0	0	1	Set MTPM[6:0] MTPM1[1:0]		0
		0	0	-	#	#	#	#	#	#	#			
		0	0	-	-	-	-	-	-	#	#			
37	Set V_{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Shared with Window Program Commands	Set MTP1	N/A
		0	0	#	#	#	#	#	#	#	#			
38	Set V_{MTP2} Potentiometer	0	0	1	1	1	1	0	1	0	1		Set MTP2	N/A
		0	0	#	#	#	#	#	#	#	#			
39	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0		Set MTP3	N/A
		0	0	#	#	#	#	#	#	#	#			
40	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1		Set MTP4	N/A
		0	0	#	#	#	#	#	#	#	#			

Note: Please refer to UC1698u datasheet for details.

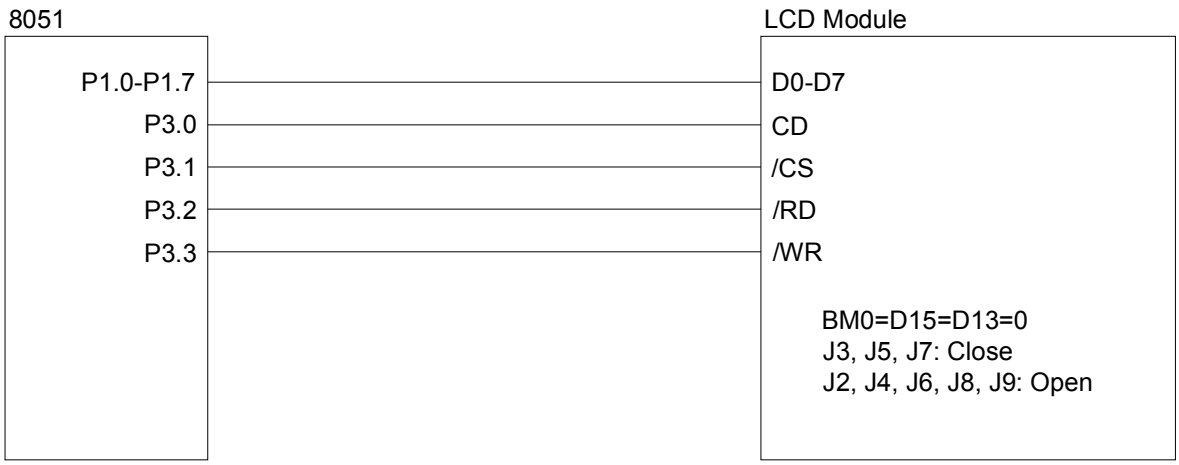
5. CONNECTION WITH MPU

This LCM supports two parallel bus protocols, 8080 or 6800 (in 8-bit bus width), and three serial bus protocols (4-wire, 3/4-wire and 3-wire SPI). Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to save the I/O terminals. The interface bus mode is determined by BM[1:0] and D[15,13] by the following relationship.

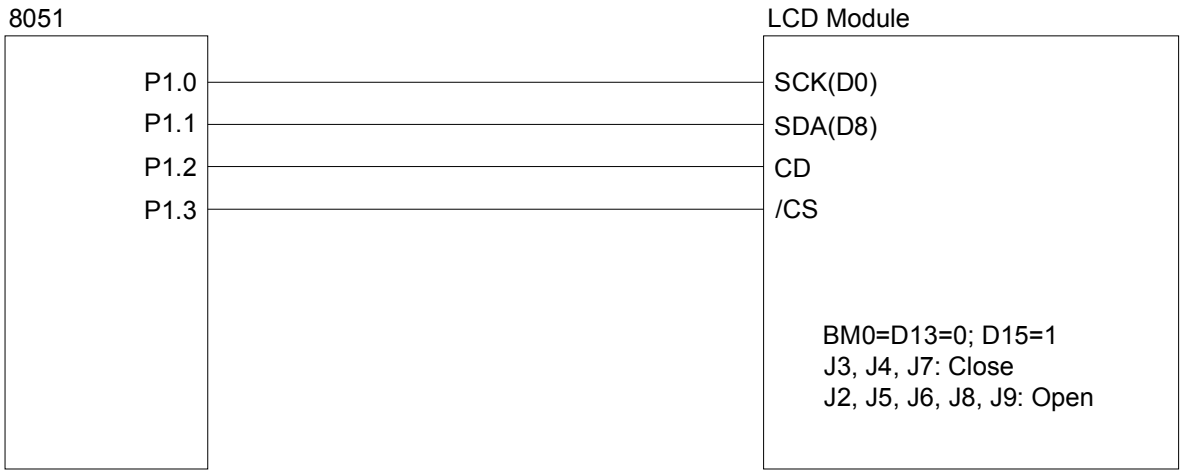
Bus type		8080	6800	S8	S8uc	S9
Width		8-bit	8-bit	4-wire	3/4-wire	3-wire
Access		Read/Write		Write Only		
Control & Data Pins	BM[1:0]	00	01	00	00	01
	D[15,13]	0x	0x	10	11	10
	/CS	Chip Select				
	CD	Control / Data				
	/WR(R/W)	/WR	R/W	0		
	/RD(E)	/RD	E	0		
	D8, D[7:0]	D[7:0]=Data	D[7:0]=Data	D8=SDA, D0=SCK		



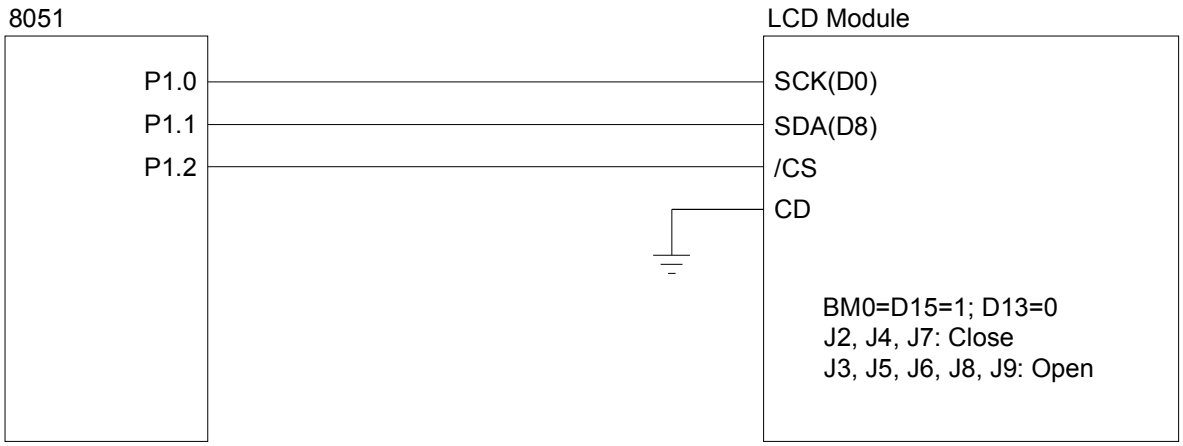
a. 8080 8-bit parallel interface



b. 8080 8-bit parallel interface



c. 4-wire SPI (S8) interface



d. 3-wire SPI (S9) interface

6. INITIALIZATION AND POWER OFF

6.1 Power on Initialization Sequence

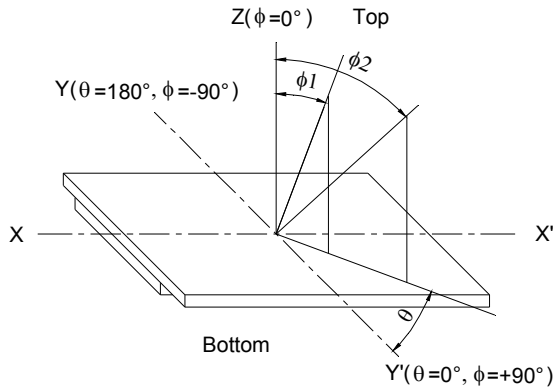
No.	Command	Operation
1	Power on	Power on
2	Automatic Power-On-Reset	There is built-in Power-On-Reset circuit in UC1698u. System reset will be activated automatically after VDD is stabilized. Delay 150ms, and then start the following initialization commands.
3	Set Power Control: 2AH	PC1=1b: Internal VLCD (x10) PC0=0b: LCD<=13nF
4	Set Temperature Compensation: 25H	TC[1:0]=01b: -0.05%/°C
5	Set Line Rate: A2H	LC[4:3]=10b: 12.6 Klps (On/Off Mode)
6	Set color Mode: D5H	LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K-color)
7	Set LCD Bias Ratio: E9H	BR[1:0]=01b: 1/10 bias
8	Set COM End: F1H, 3FH	CEN=3FH (64 pixel rows)
9	Set V_{BIAS} Potentiometer: 81H, 25H	PM[7:0]=00100101b: “00100101b ” is a reference value, modify this value to get the best display contrast. Because of the manufacturing dispersion of LCD modules, potentiometer (PM[7:0]) value may need be changed to match the driving voltage (VLCD) for different lot of LCD modules.
10	Set LCD Mapping Control: C4H	MY=1b: COM reverse MX=0b: SEG normal LC0=0b: Disable soft icon sections(2xFLT, 2xFLB)
11	Set RAM address control: 89H	AC[0]=1b: CA or RA (depends on AC[1]= 0 or 1) will restart AC[1]=0b: column increment (+1) first. AC[2]=0b: row address (RA) auto increment by +1
12	Set Color Pattern: D1H	<table><tr><td>LC[5]</td><td>SEG1</td><td>SEG2</td><td>SEG3</td><td>SEG4</td><td>SEG5</td><td>SEG6</td></tr><tr><td>1</td><td>R</td><td>G</td><td>B</td><td>R</td><td>G</td><td>B</td></tr></table>
13	Set Display Enable: AFH	DC[4:3]=11b: On/Off mode; Green Enhancing Mode disabled. DC2=1b: Normal mode
14	End of initialization	
15	Write display data	

6.2 Power off Sequence

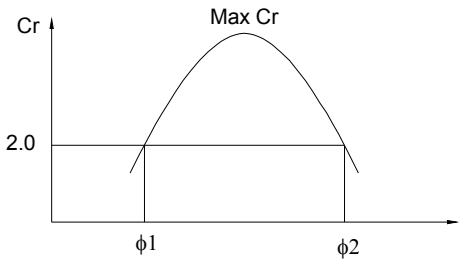
No.	Command	Description
1	Optional status	Normal operation
2	System Reset: E2H	Reset system, delay 2 ms.
3	Power off	Power off

7. ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

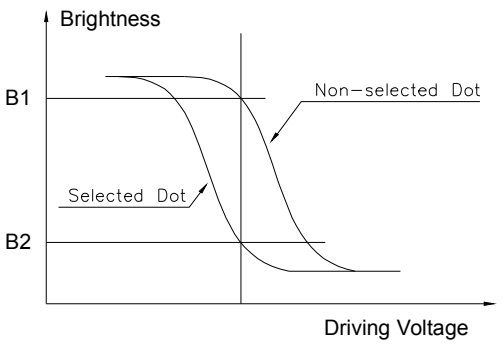
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
View Angle	Φ2-Φ1	Cr≥2 , θ=0°	-	70	-	Deg	Note1, Note2
Contrast Ratio	Cr	Φ=0°,θ=0°	3	-	-	-	Note3
Response Time	tr (rise)	Φ=0°,θ=0°	-	200	-	ms	Note4
	tf (fall)	Φ=0°,θ=0°	-	250	-	ms	



Note1: Definition of viewing angle ϕ, θ

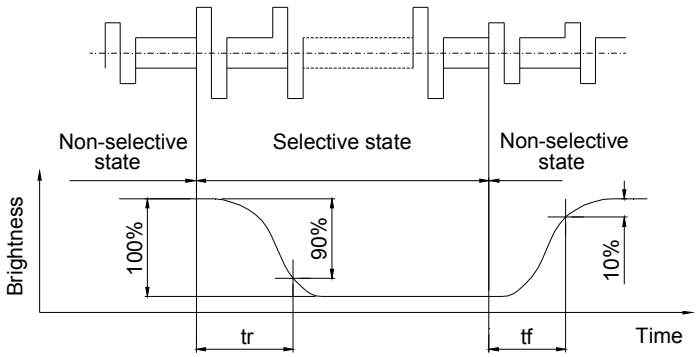


Note2: Definition of viewing angle range ϕ1, ϕ2



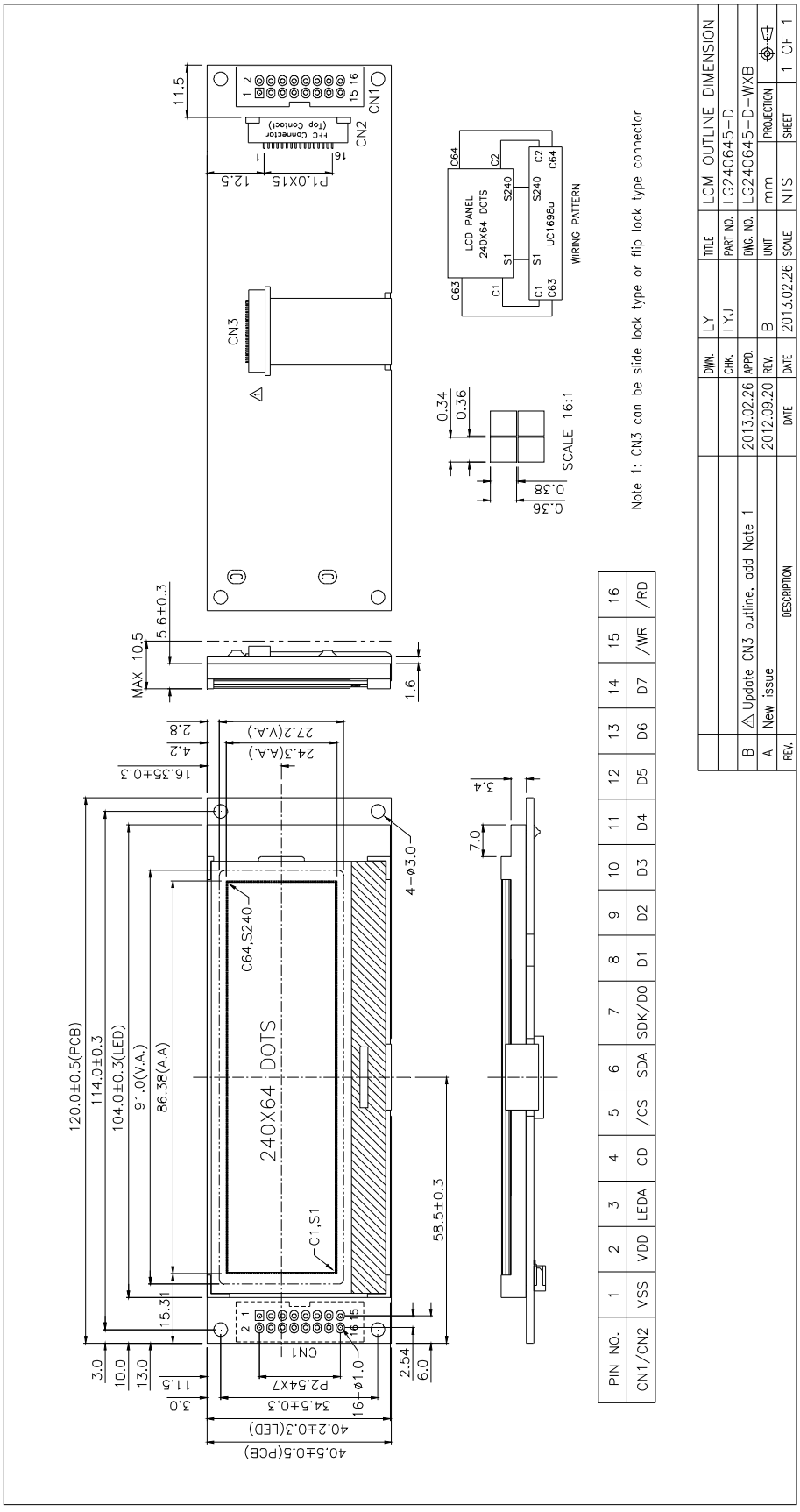
$$\text{Contrast Ratio} = \frac{\text{Brightness of non-selected dot (B1)}}{\text{Brightness of selected dot (B2)}}$$

Note3: Definition of contrast ratio (positive type)



Note3: Definition of response time

8. DIMENSIONAL OUTLINE



9. LCD MODULE NUMBERING SYSTEM

L	G	240	64	5	-	F	F	D	W	H	6	V	-	V33
(1)	(2)	(3)	(4)	(5)		(6)	(7)	(8)	(9)	(10)	(11)	(12)		(13)

(1) Brand

(2) Module type

C - Character module

G - Graphic module

(3) Display format

Character module : Number of characters per line, two digits XX

Graphic module : Number of columns, three digits XXX

(4) Display format

Character module : Number of lines, one digit X

Graphic module : Number of rows, two or three digits XX or XXX

(5) Development number : One or two digits X or XX

(6) LCD mode

T - TN Positive, Gray **N** - TN Negative, Blue

S - STN Positive, Yellow green **G** - STN Positive, Gray

B - STN Negative, Blue **F** - FSTN Positive, White

K - FSTN Negative, Black **L** - FSTN Negative, Blue

Q - FFSTN Negative, Black

(7) Polarizer mode

R - Reflective **F** - Transflective **M** - Transmissive

(8) Backlight type

N - Without backlight **L** - Array LED **D** - Edge light LED **E** - EL **C** - CCFL

(9) Backlight color

Y - Yellow green **B** - Blue **W** - White **G** - Green

A - Amber **R** - Red **M** - Multi color **Nil** - Without backlight

(10) Operating temperature range

S - Standard temperature (0 to +50 ^{o}C) **H** - Extended temperature (-20 to +70 ^{o}C)

(11) Viewing direction

3 - 3:00 **6** - 6:00 **9** - 9:00 **U** - 12:00

(12) DC-DC Converter

N or Nil - Without DC-DC converter **V** - Built in DC-DC converter

(13) Version code

V33 - 3.3V for VDD and LED backlight

10. PRECAUTIONS FOR USE OF LCD MODULE

10.1 Handing Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2) If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth. If the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3) Do not apply excessive force on the surface of display or the adjoining areas of LCD module since this may cause the color tone to vary.
4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
5) If the display surface of LCD module becomes contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents.
   · Isopropyl alcohol
   · Ethyl alcohol
   Solvents other than those mentioned above may damage the polarizer.
   Especially, do not use the following:
   · Water
   · Ketone
   · Aromatic Solvents
6) When mounting the LCD module make sure that it is free of twisting, warping, and distortion. Distortion has great influence upon display quality. Also keep the stiffness enough regarding the outer case.
7) Be sure to avoid any solvent such as flux for soldering never stick to Heat-Seal. Such solvent on Heat-Seal may cause connection problem of heat-Seal and TAB.
8) Do not forcibly pull or bend the TAB I/O terminals.
9) Do not attempt to disassemble or process the LCD module.
10) NC terminal should be open. Do not connect anything.
11) If the logic circuit power is off, do not apply the input signals.
12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
   · Be sure to ground the body when handling the LCD module.
   · Tools required for assembly, such as soldering irons, must be properly grounded.
   · To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
   · The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

1) When storing the LCD module, avoid exposure to direct sunlight or to the light of fluorescent lamps and high temperature/high humidity. Whenever possible, the LCD module should be stored in the same conditions in which they were shipped from our company.

2) Exercise care to minimize corrosion of the electrodes. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high humidity environment.

10.3 Design Precautions

1) The absolute maximum ratings represent the rated value beyond which LCD module can not exceed. When the LCD modules are used in excess of this rated value, their operating characteristics may be adversely affected.
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to satisfy VIL, VIH specification values, including taking the precaution of using signal cables that are short.
3) The liquid crystal display exhibits temperature dependency characteristics. Since recognition of the display becomes difficult when the LCD is used outside its designated operating temperature range, be sure to use the LCD within this range. Also, keep in mind that the LCD driving voltage levels necessary for clear displays will vary according to temperature.
4) Sufficiently notice the mutual noise interference occurred by peripheral devices.
5) To cope with EMI, take measures basically on outputting side.
6) If DC is impressed on the liquid crystal display panel, display definition is rapidly deteriorated by the electrochemical reaction that occurs inside the liquid crystal display panel. To eliminate the opportunity of DC impressing, be sure to maintain the AC characteristics of the input signals sent to the LCD Module.

10.4 Others

1) Liquid crystals solidify under low temperatures (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the LCD module is subjected to a strong shock at a low temperature.
2) If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
3) To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following sections when handling the module:
   · Terminal electrode sections.
   · Part of pattern wiring on TAB, etc.