HIGH-VOLTAGE MIXED-SIGNAL IC

UC1698u

160 x 128RGB C-STN LCD Controller-Driver
w/ 16-bit per RGB On-Chip SRAM
Optimized for VSTN (Video-CSTN)

MP Specifications
Revision 1.3

March 31, 2009

ULTRACHIP

The Coolest LCD Drive, Ever!!

TABLE OF CONTENT

UC1698u

Single-Chip, 160COM x128RGB Matrix Passive Color LCD Controller-Driver with VSTN Support

INTRODUCTION

UC1698u is an advanced high-voltage mixed-signal CMOS IC, specially designed for the display needs of low power hand-held devices.

In addition to low power COM and SEG drivers, UC1698u contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation, and graphics data memory.

UC1698u employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and LRM (Line Rate Modulation) gray-shade modulation scheme to achieve well balanced shading, vivid colors, and natural-looking images while supporting very fast Liquid Crystal material for video applications.

With UC1698u, LCD makers can now achieve TFT-like image quality, support video applications while maintaining the same STN advantages in power consumption, unit cost, ease of customization and production flexibility.

MAIN APPLICATIONS

- Cellular Phones and other battery operated hand held devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 160x128 matrix C-STN LCD with comprehensive support for input format and color depth:
  12-bit RGB: 4K-color
  16-bit RGB: 64K-color
- Support video rate CSTN applications.
- Window-write, window-skip functions to support flexible video applications such as OSD, dynamic service provider screen saver for cell phone and others.
- ID pin (ID1)-switched input data sets (D[7:0] or D[0, 2, 4, 6, 8, 10, 12, 14]) for 8-bit mode.
- One ID pin (ID0) plus two programmable ID flags, totally 4 software-readable ID bits to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 4-wire, 3/4-wire, and 3-wire serial buses (S8, S8uc, S9) and 16-bit/8-bit parallel buses (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Low power consumption under all display patterns.
- No power consumption or image quality penalty when used with video rate CSTN.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable temperature compensation coefficients.
- Software programmable, self-configuring 10x charge pump.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Pad layouts support COG applications.
- V_{DD} (digital) range (typical): 1.8 V ~ 3.3V
  V_{DD} (analog) range (typical): 2.8 V ~ 3.3V
  LCD V_{OP} range: 6.15V ~ 18V
- Available MTP trimming supports precise LCD contrast matching.
- Available in gold bump dies:
- COM/SEG bump information
  Bump pitch: 31 μM
  Bump gap: 13.5 μM
  Bump surface: 2013 μM^2

ORDERING INFORMATION

GOLD BUMPED DIE

Part Number	MTP	Description
UC1698uGAC	Yes	Gold bumped die, with MTP function.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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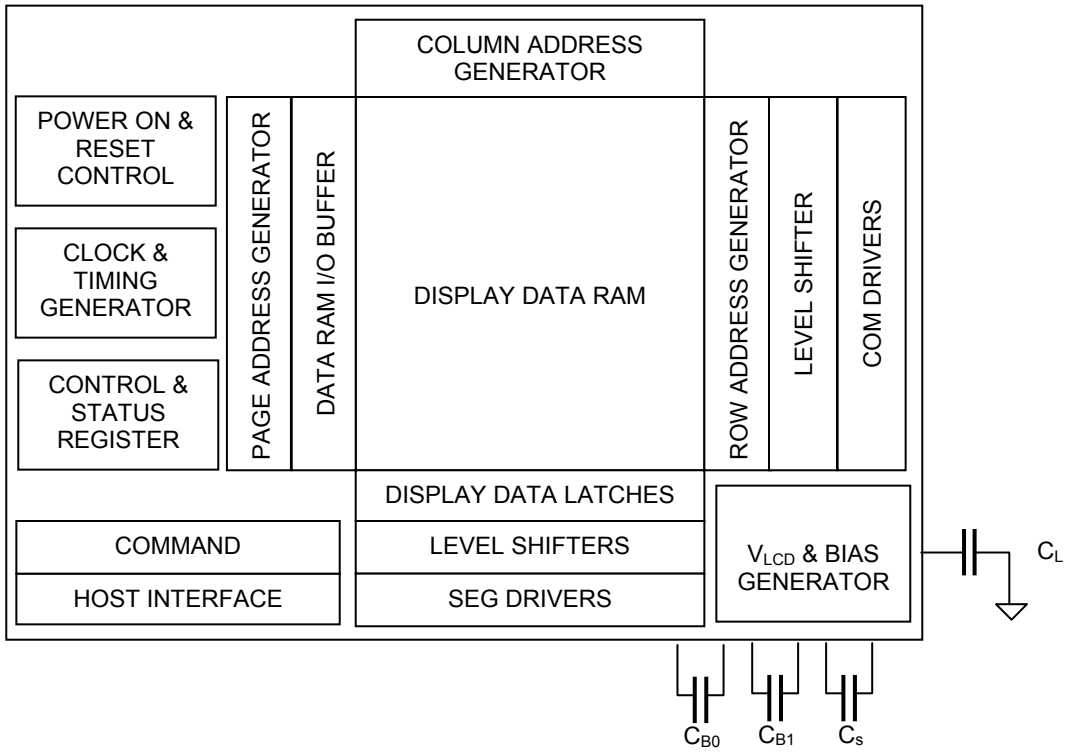
CONTACT INFORMATION

UltraChip Inc. (Headquarter)
2F, No. 70, Chowtze Street,
Nei Hu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	# of Pads	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	9 9 2	V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	12 12	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} , V_{B1-} V_{B0+} , V_{B0-} V_{S+} , V_{S-}	PWR	4, 4 4, 4 3, 3	LCD SEG driving voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}, and a capacitor of C_S value between V_{S+} and V_{S-}. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCD-IN} $V_{LCD-OUT}$	PWR	2 2	High voltage LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} source is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open. Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance around 20 Ω.

NOTE

- Recommended capacitor values:
  C_{Bx}: 2.2µF/5V or 300x LCD load capacitance, whichever is higher.
  C_S :150 ~ 220nF / 25V
  C_L :330nF/25V is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and {DB15, DB13} by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>{DB15, DB13}</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/16-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/16-bit</td></tr>
<tr><td>01</td><td>0x</td><td>6800/8-bit</td></tr>
<tr><td>00</td><td>0x</td><td>8080/8-bit</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
<tr><td>00</td><td>11</td><td>3/4-wire SPI w/ 8-bit token
(S8uc: Ultra-Compact)</td></tr>
<tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit taken
(S9: conventional)</td></tr>
</table></td></tr>
<tr><td>CS0
CS1</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[15:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1698u has built-in Power-ON reset and software reset commands, RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Selects Control data or Display data for read/write operation. In S9 mode, CD pin is not used. Connect to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID0</td><td>I</td><td>1</td><td>ID0 pin can be used for production control.
Connect ID0 pin to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>ID1</td><td>I</td><td>1</td><td>Selects Input Data set for 8-bit mode.
ID1=0 : 8-bit input data are D[0,2,4,6,8,10,12,14]
ID1=1 : 8-bit input data are D[0:7]
The wiring status of ID pins is available in PID[1:0] with command <code>Get Status</code>. Other than 8-bit mode, connect ID1 to V_{DD} for “H”, or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] control the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
</table>

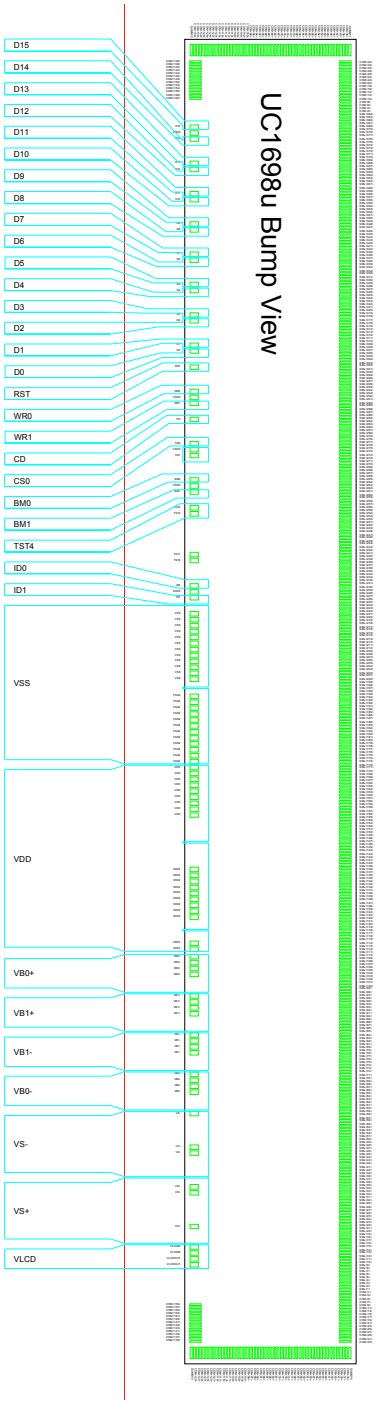
<table>
<tr><th>Name</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td colspan="4">DATA BUS</td></tr>
<tr><td>D0~D15</td><td>I/O</td><td>16</td><td>Bi-directional bus for parallel host interfaces.
In serial modes, connect DB[0] to SCK, DB[8] to SDA.
<table>
<tr><th></th><th>BM=1x
(16-bit)</th><th>BM=0x
(8-bit)
ID1=0</th><th>BM=0x
(8-bit)
ID1=1</th><th>BM=00
(S8/S8uc)</th><th>BM=01
(S9)</th></tr>
<tr><td>DB0</td><td>D0</td><td>D0/D8</td><td>D0/D8</td><td>SCK</td><td>SCK</td></tr>
<tr><td>DB1</td><td>D1</td><td>–</td><td>D1/D9</td><td>–</td><td>–</td></tr>
<tr><td>DB2</td><td>D2</td><td>D1/D9</td><td>D2/D10</td><td>–</td><td>–</td></tr>
<tr><td>DB3</td><td>D3</td><td>–</td><td>D3/D11</td><td>–</td><td>–</td></tr>
<tr><td>DB4</td><td>D4</td><td>D2/D10</td><td>D4/D12</td><td>–</td><td>–</td></tr>
<tr><td>DB5</td><td>D5</td><td>–</td><td>D5/D13</td><td>–</td><td>–</td></tr>
<tr><td>DB6</td><td>D6</td><td>D3/D11</td><td>D6/D14</td><td>–</td><td>–</td></tr>
<tr><td>DB7</td><td>D7</td><td>–</td><td>D7/D15</td><td>–</td><td>–</td></tr>
<tr><td>DB8</td><td>D8</td><td>D4/D12</td><td>–</td><td>SDA</td><td>SDA</td></tr>
<tr><td>DB9</td><td>D9</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB10</td><td>D10</td><td>D5/D13</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB11</td><td>D11</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB12</td><td>D12</td><td>D6/D14</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB13</td><td>D13</td><td>–</td><td>–</td><td>0:S8/1:S8uc</td><td>0</td></tr>
<tr><td>DB14</td><td>D14</td><td>D7/D15</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB15</td><td>D15</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table>
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
</table>

Name	Type	# of Pads	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG384	HV	384	SEG (column) driver outputs. Support up to 128xRGB pixels. Leave unused SEG drivers open-circuit.
COM1 ~ COM160	HV	160	COM (row) driver outputs. Support up to 160 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 160, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 160] open-circuit.
MISC. PINS			
V_{DDX}	O	5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus within the IC. These pads are provided to facilitate chip configurations in COG application. These pins should *NOT* be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I/HV	2	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50 Ω.
TST1 TST2	O	1 1	Test I/O pins. Leave these pins open during normal use.

NOTE:

Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value ranges for those index registers will be 0~159 for COM and 0~383 for SEG.

RECOMMENDED COG LAYOUT



Note for V_{DD} and V_{SS} with COG:

The operation condition $V_{DD} \geqslant 1.8V$ must be satisfied under all operating conditions. With its video capability, UC1698u peak current (I_{DD}) can be up to ~15mA range during high speed data write to UC1698u's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD}, V_{SS} ITO trances in COG glass modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1698u contains registers which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, starting with a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (159 – 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	8	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 10 10b: 11 **11b: 12**
TC	2	0H	Temperature Compensation (per ^{o}C) **00b: -0.00%** 01b: -0.05% 10b: -0.15% 11b: -0.25%
PM	8	40H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	7	00H	PM offset. PMO[6]=1b: The effective PM value, PMV = PM - PMO[5:0] PMO[6]=0b: The effective PM value, PMV = PM + PMO[5:0]
PC	2	2H	Power Control. PC[0]: **0b: LCD ⩽ 13nF** 1b: 13nF < LCD ⩽ 22nF PC[1]: 0b: External V_{LCD} **1b:** Internal V_{LCD} (10x charge pump)
AC	4	1H	Address Control. AC[0]: WA: Automatic column/row Wraparound (Default **1 : ON**) AC[1]: Auto-Increment order **0b : Column (CA) first** 1b : Row (RA) first AC[2]: RID: RA (row address) Auto Increment Direction (**L : +1** H : -1) AC[3] : Window Program Mode **0b : Inside Mode:** Write to SRAM within the window defined by (WPC0,WPP0) and (WPC1,WPP1) 1b : Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0) and (WPC1,WPP1)

Name	Bits	Default	Description
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray-shade Modulation mode. 0 : On/Off mode **1 : 32-shade Mode** DC[4]: Green Enhance Mode. *Only valid in 4K-color mode*. 0 : Enable. Allows an extra display bit for green color. **1 : Disable**
LC	9	090H	LCD Control: LC[0]: Enable the top FLTx2 and bottom FLBx2 lines in partial display mode (Default **0: OFF**). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **0: OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **0: OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 25.2. Klps 01b: 30.5 Klps **10b: 37.0 Klps** 11b: 44.8 Klps Line Rate (for On/Off mode) 00b: 8.5 Klps 01b: 10.4 Klps **10b: 12.6 Klps** 11b: 15.2 Klps (Line-Rate = Frame-Rate x Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode when DC[4]=1: 01b : 4K color mode. 4R-4G-4B (12-bit/RGB) **10b : 64K color mode**. 5R-6G-5B (16-bit/RGB) when DC[4]=0: 01b : 4K color mode. 4R-5G-3B (12-bit/RGB) 10b : 64K color mode. 5R-6G-5B (16-bit/RGB) LC[8] : Partial Display Control **0b: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	5	1DH	N-Line Inversion: NIV[2:0]: 000b: 11 lines 001b: 19 lines 010b: 21 lines 011b: 25 lines 100b: 29 lines **101b: 31 lines** 110b: 37 lines 111b: 43 lines NIV[3]: 0b: no-XOR **1b: XOR** NIV[4]: 0b: Disable NIV **1b: Enable NIV**
CSF	3	0H	COM Scan Function CSF[0]: Interlace Scan Function **0b: LRM sequence: AEBCD-AEBCD** 1b: LRM sequence: AEBCD-EBCDA CSF[1]: FRC function **0: Disable FRC** 1: Enable FRC CSF[2]: Shade-1 / Shade-30 option **0: Dither directly on input data (SRAM Change)** 1: PWM (Pulse-width modulation) on SEG output stage

Name	Bits	Default	Description
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
WPC0	7	00H	Window program starting column address. Value range: 0 ~127.
WPP0	8	00H	Window program starting row address. Value range: 0~159.
WPC1	7	7FH	Window program ending column address. Value range: 0~127.
WPP1	8	9FH	Window program ending row address. Value range: 0~159
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : **Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTP	7	--	Multiple-Time Programming. For V_{LCD} fine tune.
MTPID	2	--	Multiple-Time Programming. For LCM manufacturer's configuration.
MTPM	7	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
MTPM1	2	0H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded
ID	2	PIN	Access the connected status of ID pins.

COMMAND TABLE

The following is a list of host commands supported by UC1698u

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver	PMO[6:0]								
				Product Code (8h)				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H
		0	0	#	#	#	#	#	#	#	#		
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0
		0	0	#	#	#	#	#	#	#	#		
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH
				-	-	-	#	#	#	#	#		
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands: Set WPC0	0
		0	0	-	#	#	#	#	#	#	#		
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1	Set WPP0	0
		0	0	#	#	#	#	#	#	#	#		
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1	127
		0	0	-	#	#	#	#	#	#	#		
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1	Set WPP1	159
		0	0	#	#	#	#	#	#	#	#		
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H
		0	0	-	-	-	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
36	Set MTP Write Mask	0 0 0	0 0 0	1 - -	0 # -	1 # -	1 # -	1 # -	0 # -	0 # #	1 # #	Set MTPM[6:0] MTPM1[1:0]		0
37	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
38	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	N/A
39	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	N/A
40	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A

NOTE:

- All other bit patterns other than commands listed above may result in undefined behavior.
- The interpretation of commands (36)~(40) depends on the setting of register MTPC[3].
  - Commands (37)~(40) are shared with commands (30)~(33). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.
- Under 16-bit bus mode and CD=0, D[15:8] is ignored and only D[7:0] is used. As a result, the bus cycles for commands under 16-bit bus and 8-bit bus are the same, and double-byte commands still need two bus cycles under 16-bit bus mode.

  Example:

  8-bit bus mode:

  Set PL[1:0] = 2'b11 : D[7:0] = 0010 1011

  Set PM[7:0] = 8'h8b : 1st D[7:0] = 1000 0001

  2nd D[7:0] = 1000 1011

  16-bit bus mode:

  Set PL[1:0] = 2'b11: D[15:0] = 0000 0000 0010 1011

  Set PM[7:0] = 8'h8b: 1st D[15:0] = 0000 0000 1000 0001

  2nd D[15:0] = 0000 0000 1000 1011

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data written to SRAM							

UC1698u will convert input RAM data to 16-bit of RGB data. Please refer to command *Set Color Mode* for detail of data-write sequence.

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data read from SRAM							

Each RGB triplet is stored as 16-bit in the display RAM. Each 16-bit of RGB data takes 1 (/ 2) RAM read cycles for 16 (/ 8) –bit bus mode, respectively. The read out RGB data is *after-extension* for 64K color mode.

R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
1st 8-bit Read								2nd 8-bit Read							

Write/Read Data Byte (commands (1) and (2)) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing commands `Set Row Address` and `Set Column Address`. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

For 8-bit / 16-bit interface, the first 1 byte / 2 bytes of read, respectively, is a dummy read. Please ignore the data read out.

(3) GET STATUS & PM

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	GE	MX	MY	WA	DE	WS	MD	MS
	0	1	Ver	PMO[6:0]						
	0	1	Product Code				PID[1:0]		MID[1:0]	

Status1 definitions:
- *GE* : Green Enhancing enable flag. Green Enhance Mode is disabled when GE = 1.
- *MX* : Status of register LC[1], mirror X.
- *MY* : Status of register LC[2], mirror Y.
- *WA* : Status of register AC[0]. Automatic column/row wrap around.
- *DE* : Display enable flag. DE=1 when display is enabled
- *WS* : MTP Operation succeeded
- *MD* : MTP Option (1 for MTP version, 0 for non-MTP version)
- *MS* : MTP action status

Status2 definitions:
- *Ver* : IC Version Code. 0 or 1.
- *PMO[6:0]* : PM offset value.

Status3 definitions:
- *Product Code* : 1000b (8h)
- *PID[1:0]* : Provide access to ID pins connection status.
- *MID[1:0]* : LCM manufacturer's configuration.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	**0**	**0**	**0**	**1**	0	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~127**

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b = -0.00%/^{o}C 01b = -0.05%/^{o}C 10b = -0.15%/^{o}C 11b = -0.25%/^{o}C

(6) SET POWER CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[0] according to the capacitance loading of LCD panel.

Panel loading definition: **0b : LCD ⩽ 13nF** 1b : 13nF < LCD ⩽ 22nF

Set PC[1] to program the build-in charge pump stages. Before changing PC[1] value, always ensure the IC is in a RESET state. Avoid changing PC[1] when the display is enabled.

Pump control definition: 0b = External V_{LCD} **1b = Internal V_{LCD} (x10)**

(7) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
(Double-byte command)	0	0	APC register parameter							

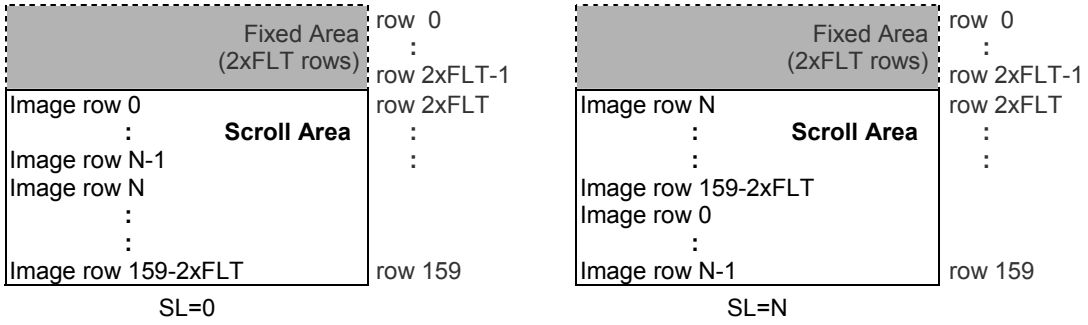
For UltraChip only. Please do NOT use.

(8) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	**0**	**1**	**0**	**1**	SL7	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 159-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by the `Set Fixed Lines` command.



(9) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address MSB RA [7:4]	0	0	**0**	**1**	**1**	**1**	RA7	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = **0~159**

(10) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section *LCD Voltage Setting* for more detail.

Effective range: **0 ~ 255**

(11) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC[8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**0**	LC8

This command is used to enable partial display function.

LC[8] : **0**b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
1b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0]x(FLT+FLB)x2

(12) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order
0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).
1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

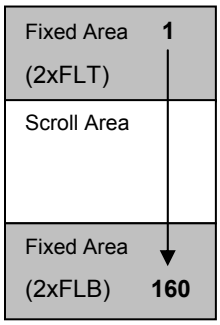
AC[2]: RID, row address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. For Window Program mode (AC[3]=ON), see section *Command Description* (32) ~ (35) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[3] is.

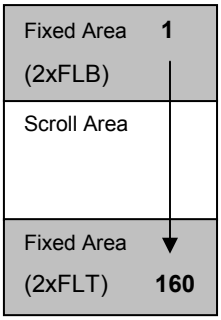
(13) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB}	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0



MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], ensure:

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(14) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 108, 80, 56, and 40.

The following are line rates at Mux Rate = 109 ~ 160.

00b: 25.2 Klps 01b: 30.5 Klps **10b: 37.0 Klps** 11b: 44.8 Klps

In On/Off Mode

00b: 8.5 Klps 01b: 10.4 Klps **10b: 12.6 Klps** 11b: 15.2 Klps

(Klps: Kilo-Line-per-second)

(15) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(16) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

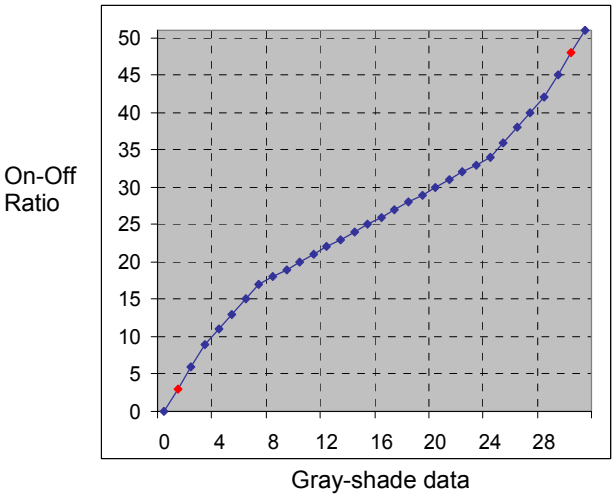
(17) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1698u will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1698u has two gray shade modulation modes: an On/Off mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



DC[4] Green Enhance Mode. Refer to command `Set Color Mode` for more information.

0b: Green Enhancing Mode enabled **1b: Green Enhancing Mode disabled**

NOTE:

1. For red and blue colors, when PWM is off, the shades mapped to data 1 and 30 (shown as red points above) are achieved by special dithering. When PWM is on, these shades are produced by PWM.
2. Green shades are created by combining FRC (default: Off) and special dithering. When PWM is off, six of the shades (1, 2, 3, 59, 60, and 61) are created by special dithering while they are created by PWM when PWM is on. Data 62 and 63 are mapped to the same shade.
3. When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1698u for 5~10mS after setting DC[2] to 1.

(18) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] to control COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by the MY action. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

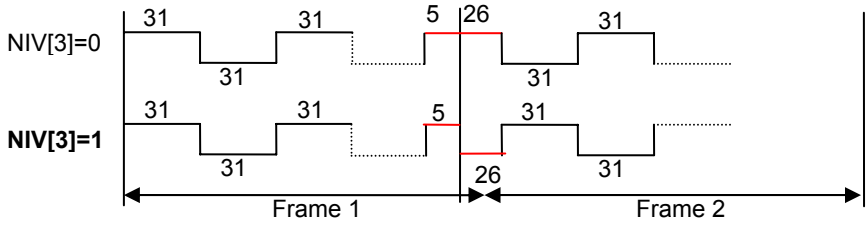
LC[0] controls whether soft icon sections (2xFLT, 2xFLB) are displayed during partial display mode.

(19) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line inversion NIV[3:0]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
(Double-byte command)	0	0	**-**	**-**	**-**	NIV4	NIV3	NIV2	NIV1	NIV0

N-Line Inversion:

NIV[2:0]: 000b: 11 lines; 001b: 19 lines; 010b: 21 lines; 011b: 25 lines; 100b: 29 lines; **101b: 31 lines**; 110b: 37 lines; 111b: 43 lines
NIV[3]: 0b: non-XOR; **1b: XOR**
NIV[4]: 0b: Disable NIV; **1b: Enable NIV**



(20) SET COLOR PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	LC5

UC1698u supports on-chip swapping of R⇔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG382	SEG383	SEG384
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in *`Set Color Mode`* below.

(21) SET COLOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Note: *For serial bus modes, please refer to 8-bit tables below.*

Green Enhance Mode disabled (DC[4]=1):

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K-color)

12 bits of input RGB data are stored to 16 RAM bits. No dither is performed. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	***D[7:0]***							
1st Write Data Cycle	R3	R2	R1	R0	G3	G2	G1	G0
2nd Write Data Cycle	B3	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G3	G2	G1	G0	B3	B2	B1	B0

Data Write Sequence (16-bit)	***D[15:0]***															
1st Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2nd Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

LC[7:6] = **10b** (RRRRR-GGGGGG-BBBBB, 64K-color)

16 bits of input data are stored to 16 RAM bits directly.

Data Write Sequence (8-bit)	***D[7:0]***							
1st Write Data Cycle	R4	R3	R2	R1	R0	G5	G4	G3
2nd Write Data Cycle	G2	G1	G0	B4	B3	B2	B1	B0

Data Write Sequence (16-bit)	***D[15:0]***															
1st Write Data Cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Green Enhance Mode enabled (DC[4]=0)**:**

LC[7:6] = 01b (RRRR-GGGGG-BBB, 4K-color)

12 bits of input data are extended and stored to 16 RAM bits. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	***D[7:0]***							
1st Write Data Cycle	R3	R2	R1	R0	G4	G3	G2	G1
2nd Write Data Cycle	G0	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G4	G3	G2	G1	G0	B2	B1	B0

Data Write Sequence (16-bit)	***D[15:0]***															
1st Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G4	G3	G2	G1	G0	B2	B1	B0
2nd Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G4	G3	G2	G1	G0	B2	B1	B0

LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color)

The behaviors of 8-bit input mode and 16-bit input mode do not change with DC[4] setting. Refer to previous section for more information on these two input modes.

(22) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[2:0]	0	0	**1**	**1**	**0**	**1**	**1**	CSF2	CSF1	CSF0

COM scan function

CSF[0]: Interlace Scan Function
- **0b: LRM sequence: AEBCD-AEBCD**
- 1b: LRM sequence: AEBCD-EBCDA

CSF[1]: FRC Function
- **0b: FRC Disable**
- 1b: FRC Enable

CSF[2]: Shade-1, Shade-30 option
- **0 : Dither directly on input data(SRAM Change)**
- 1 : PWM on SEG output stage

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	TT	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Do *NOT* use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b =5 01b = 10 10b = 11 **11b = 12**

***(27)* SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	**-**	*CEN* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 160 pixel rows, the LCM designer should set CEN to N-1 (where N is the number of pixel rows) and use COM1 through COM-N as COM driver electrodes.

***(28)* SET PARTIAL DISPLAY START**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	**-**	*DST* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

***(29)* SET PARTIAL DISPLAY END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double-byte command)	0	0	**-**	*DEN* register parameter						

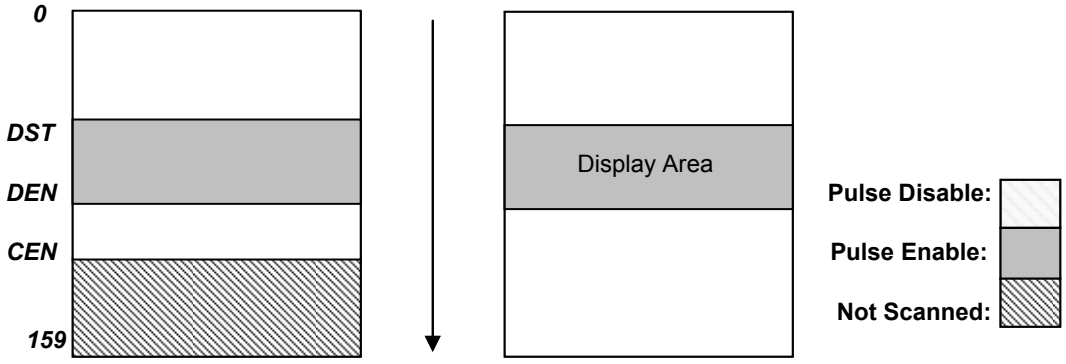
This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8]=1b, the Mux-Rate is narrowed down to DST-DEN+1+(FLT+FLB)xLC[0]x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

For minimum power consumption, set LC[8]=1b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On/Off mode, set PC[0]=0b, disable N-Line Inversion, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 40, it is recommended to set BR=5 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(Scan Method) (Display Result)

(30) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	**-**	*WPC0[6:0]* register parameter						

This command is to program the starting column address of RAM program window.

(31) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	*WPP0[7:0]* register parameter							

This command is to program the starting row address of RAM program window.

(32) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	**-**	*WPC1[6:0]* register parameter						

This command is to program the ending column address of RAM program window.

(33) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	*WPP1[7:0]* register parameter							

This command is to program the ending row address of RAM program window.

(34) SET WINDOW PROGRAM MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command controls the Window Program function.

AC[3]=0: Inside Mode

When Window Programming is under “Inside” mode , the CA and RA increment and wrap-around will be performed automatically around the boundaries as defined by registers WPC0, WPC1, WPP0, and WPP1, so that the CA/RA address will stay ***within*** the defined window of SRAM address, and therefore allow effective data update within the window.

AC[3]=1: Outside Mode

When Window Programming is under “Outside” mode, the CA and RA increment and wrap-around boundary will cover the entire UC1698u SRAM map (CA: 0~127, RA:0~159). However, when CA/RA points to a memory location within the window defined by registers WPC0, WPC1, WPP0, and WPP1, the SRAM data update operation will be suspended, the existing data will be retained and the input data will be ignored.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting.

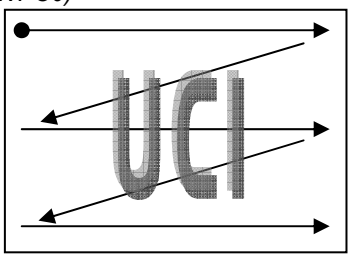
- WA (AC[0]) decides whether the program RAM address advances to next row / column after reaching the specified window column / row boundary.
- RID (AC[2]) controls the RAM address increasing from WPP0 toward WPP1 (RID=0) or the reverse direction (RID=1).
- Auto-increment Order (AC[1]) directs the RAM address increasing vertically (AC[1]=1) or horizontally (AC[1]=0).
- MX (LC[1]) results the RAM column address increasing from 127-WPC0 to 127-WPC1 (MX=1) or from WPC0 to WPC1 (MX=0).

By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the “window”, effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

Auto-increment order = 0 MX=0 RID = 0

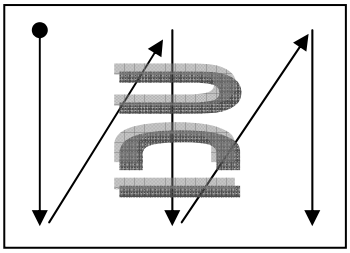
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=0 RID = 0

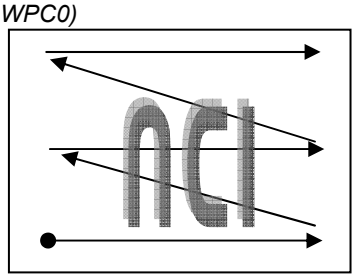
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=0 RID = 1

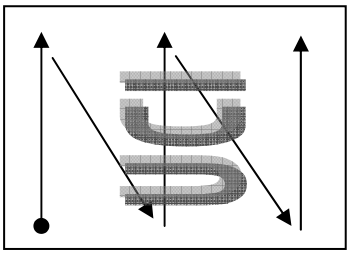
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=0 RID = 1

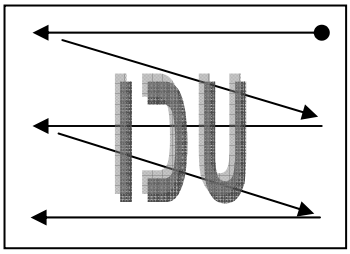
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=1 RID = 0

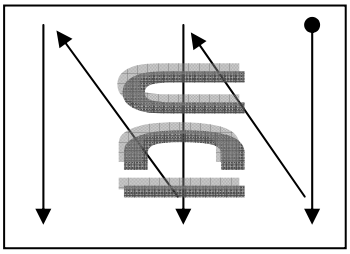
(WPP0,127-WPC0)



(WPP1,127-WPC1)

Auto-increment order = 1 MX=1 RID = 0

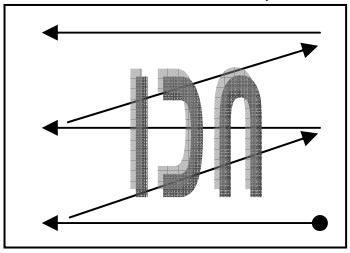
(WPP0,127-WPC0)



(WPP1,127-WPC1)

Auto-increment order = 0 MX=1 RID = 1

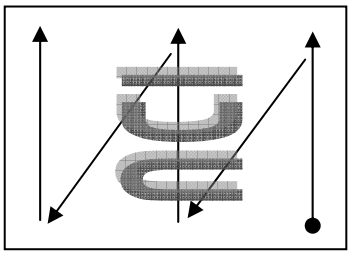
(WPP0,127-WPC0)



(WPP1,127-WPC1)

Auto-increment order = 1 MX=1 RID = 1

(WPP0,127-WPC0)



(WPP1,127-WPC1)

(35) SET MTP OPERATION CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	**-**	*MTPC* register parameter				

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Sleep
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

The following commands, (37) ~ (41), are used as MTP commands only when MTPC[3]=1.

(36) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (Triple-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	**-**	MTPM[6:0] register parameter						
	0	0	**-**	**-**	**-**	**-**	**-**	**-**	MTPM1 [1:0]	

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to “1”. MTPM[x]=0 means no Write action for x-th bit. And the content of this bit will not change.

The amount of “programming current” increases with the number of 1’s in MTPM. If the “programming current” appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1’s evenly into these cycles.

MTPM[6:0] : Set PMO value
MTPM1[1:0]: Set MID value

This command is only valid when MTPC[3]=1.

(37) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{MPT1} setting (use with BR=00) and is only valid when MTPC[3]=1.

(38) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} PM setting (use with BR=01) and is only valid when MTPC[3]=1.

(39) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(40) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1698u via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 6, UC1698u can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD} / V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=160), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1698u supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	11	12

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	-0.00	-0.05	-0.15	-0.25

Table 2: Temperature Compensation

V_{LCD} AND CONTRAST FINE TUNING

Color STN LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the V_{OP} of LCD. It is very difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to precisely match the actual V_{OP} of each LCD.

For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH FOR COG

The power supply circuit of UC1698u is designed to handle LCD panels with loading up to ~18nF using 7-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.8V$. For larger LCD panels, use lower resistance ITO glass.

Due to crosstalk consideration, ~18nF is also the recommended maximum LCD panel loading for COG applications. Using 4.5-Ω/Sq low resistance ITO glass will help improve image quality and operation tolerance.

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[1].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

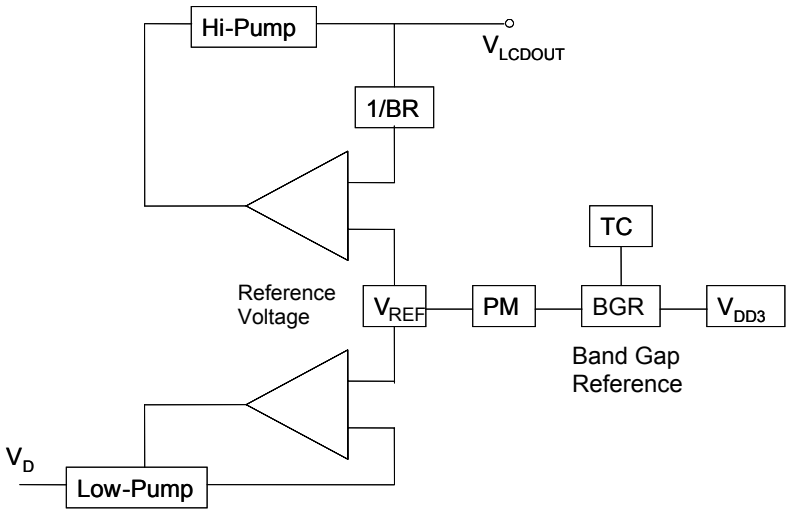
where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

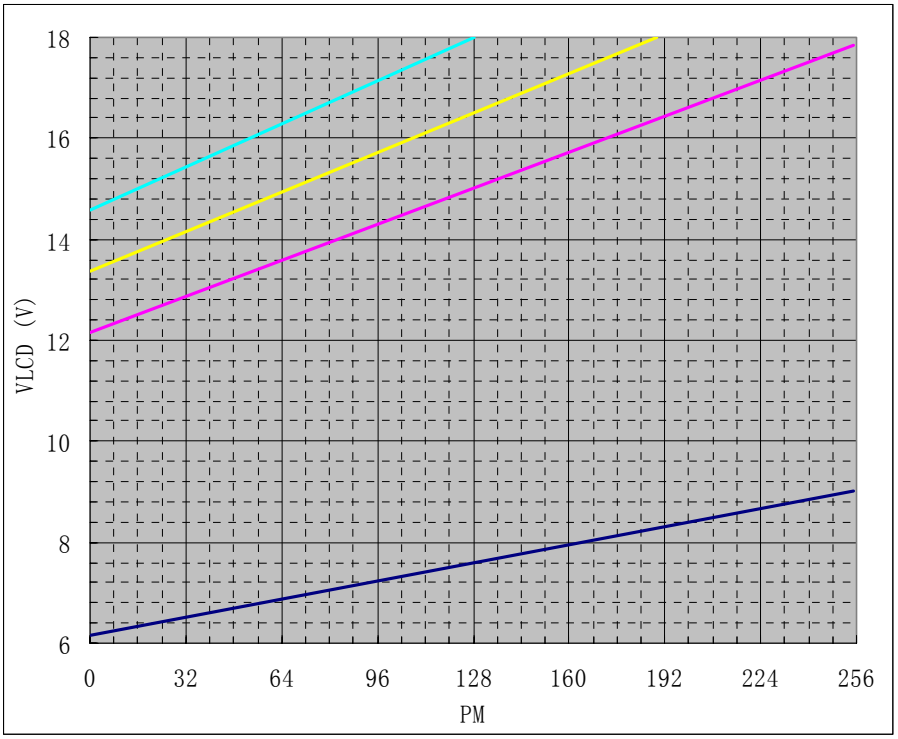
PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.



V_{LCD} QUICK REFERENCE



BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
5	6.154	11.22	0	6.154
			255	9.015
10	12.157	22.26	0	12.157
			255	17.833
11	13.369	24.45	0	13.369
			189	17.991
12	14.580	26.61	0	14.580
			128	17.986

V_{LCD}-PM-BR relationship at 25°C

NOTE:

1. For good product reliability, please keep V_{LCD} under **18V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

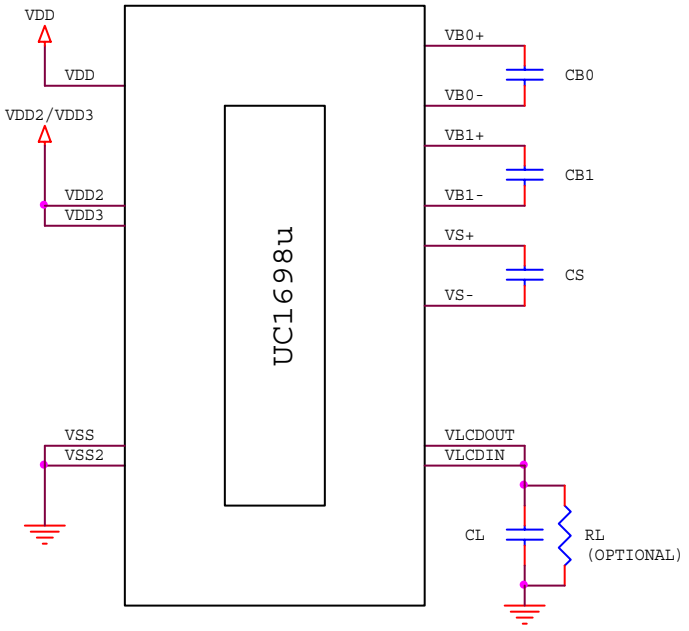


FIGURE 1: Sample circuit using internal Hi-V generator circuit

NOTE:
Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

$C_{B0\sim1}$: 2.2 µF/5V or 300x LCD load capacitance, whichever is higher.

C_L : 330nF(25V) is appropriate for most applications.

C_S : 150 ~ 220nF / 25V.

R_L: 3.3 ~ 10 MΩ to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1698u contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 109, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 108, 80, 56 and 40, line rate will be scaled down automatically by 1.5, 2, 3 and 4 times to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Line rate 37.0 Klps or higher is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to On/Off Mode, line rate will be scaled down automatically to reduce power.

Under most situations, flicker behavior is similar between these two modulation schemes. However, it is recommended to test each mode to make sure the result is as expected.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming convention is COM(X), where X =1~160, referring to the COM driver for the X-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1698u will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1698u will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FLT and FLB specify two regions of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. FLT and FLB registers can be used to implement fixed regions when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1698u provides flexible control of Mux Rate and active display area. Please refer to commands `Set COM End`, `Set Partial Display Start`, and `Set Partial Display End` for more detail.

GRAY-SHADE MODULATION MODE

UC1698u has two gray-shade modulation modes: 32-shade and On/Off Mode.

The On/Off mode will consume roughly 40~45% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between On/Off mode and 32-shade mode.

INPUT COLOR FORMATS

UC1698u supports the following two different input color formats.

4KC (12-bit/RGB): In this color mode, R/G/B will be extended and the input data will be converted into 5R-6G-5B format before they are stored to display RAM.

64KC (16-bit/RGB): This is the native color mode. Data will be stored directly to on-chip SRAM in 5R-6G-5B (16-bit) format (except shade1 and shade30, which are achieved by special dithering. See command Set Display Enable for more details). This is the default input format mode.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can mix several color modes together and switch among them in real time.

For example, the menu portion can be painted in 4K-color mode for fast update speed, and then switch to 64K-color mode, together with window programming function to effectively produce smooth graphics images.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1698u can be as short as 13µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 0.8\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} – RC_{MIN} | < 0.15\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.3\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / #_column, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast and color saturation will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/160	1/12	7.93%	6.3%	5.7%
1/160	1/11	7.77%	6.2%	5.6%

VIDEO CSTN & COG

UC1698u can support very fast CSTN for video rate applications. For LCM with t_r+t_f = 180mS ~ 200mS or smaller, it is recommended to set the line rate higher such that the frame rate is 260Hz or higher. For such applications, special attentions are necessary for COG design to minimize crosstalk and to ensure plenty of power is available to drive the LCM at such high speed.

- At this fast scan rate, the SEG/COM trace RC decay minimization will be very critical in minimizing crosstalk.
- MPU will perform frequent high speed update to the on-chip video RAM for video applications. Make sure the ITO does not cause on-chip V_{DD}-V_{SS} to fall below 1.7V, and V_{SS} bounce is under 7% x V_{DD}.

For VSTN (video CSTN) applications, it is recommended to use low resistance ITO glass to help reducing SEG signal RC decay, minimizing V_{DD}, V_{SS} noise, and ensuring sufficient V_{DD2}, V_{SS2} supply for on-chip DC-DC converter.

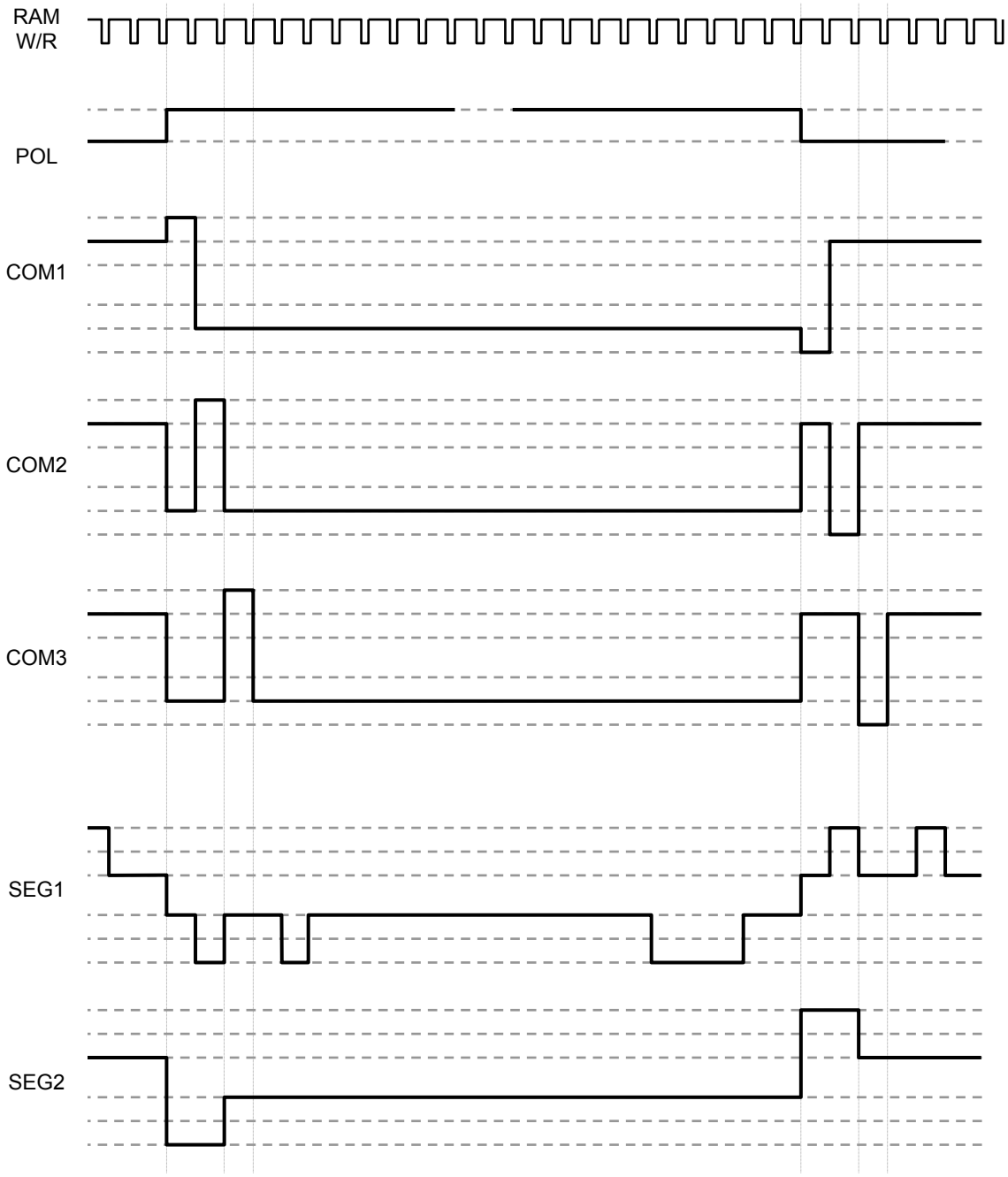


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1698u supports two parallel bus protocols, in either 8-bit or 16-bit bus width, and three serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

		Bus Type						
		8080		**6800**		**S8 (4wr)**	**S8uc (3/4wr)**	**S9 (3WR)**
Width		16-bit	8-bit	16-bit	8-bit	Serial		
Access		Read/Write				Write Only		
Control & Data Pins	BM[1:0]	10	00	11	01	00	00	01
	{DB[15], DB[13]}	Data	0x	Data	0x	10	11	10
	CS[1:0]	Chip Select						
	CD	Control / Data						0
	WR0	$\overline{WR}$		R/$\overline{W}$		0		
	WR1	$\overline{RD}$		EN		0		
	DB[1,3,5,7,9,11]	Data	–	Data	–	–		
	DB[0,2,4,6,8,10,12, 14]	Data	Data	Data	Data	DB[8]=SDA, DB[0]=SCK		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Interface	CS Init bus state	CD 1⇔0 Init bus state	CD 1⇨0 init color mapping	RESET Init bus state	RESET init color mapping
16-bit	✓	–	–	✓	✓	✓
8-bit	✓	–	–	✓	✓	✓
S8	✓	✓	–	✓	✓	✓
S8uc	✓	–	✓	✓	✓	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS Sync / RESET can be used to initialize bus state machine (like 8-bit / S8 / S9).
- RESET can be pin reset / soft reset / power on reset.
- CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1698u internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 16-bit mode, by either *Set CA,* or *Set RA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

16-BIT & 8-BIT BUS OPERATION

UC1698u supports both 8-bit and 16-bit bus width. The bus width is determined by pin BM[1].

8-bit bus operation exactly doubles the clock cycles of 16-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 8-bit mode is reset each time CD pin changes state (when CS is active).

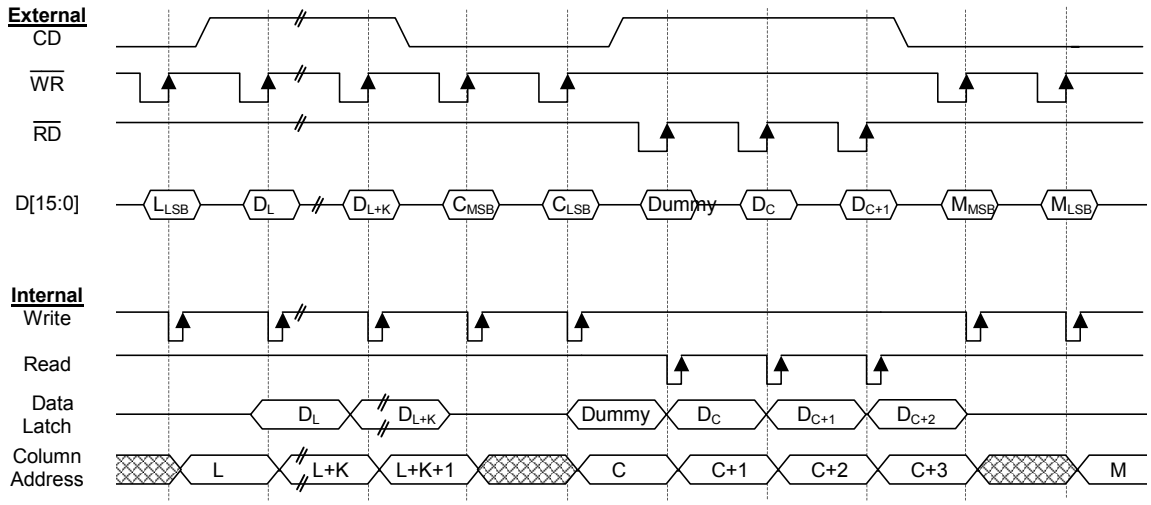


FIGURE 3: 16-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1698u supports three serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc), and one 3-wire mode (S9) . Bus interface mode is determined by the wiring of the BM[1:0], D[15] and D[13]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

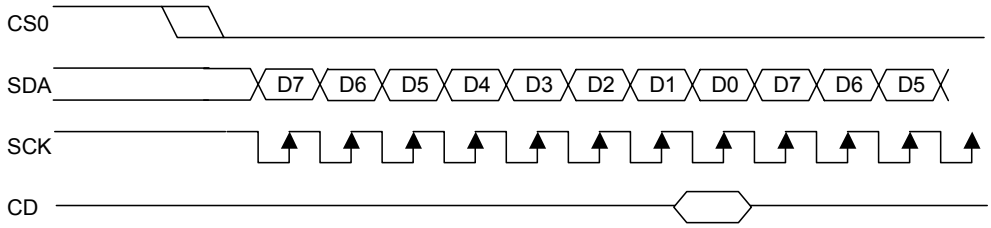


FIGURE 4.a: 4-wire Serial Interface (S8)

S8UC (3/4-WIRE) INTERFACE

Only write operations are supported in this 3/4-wire serial mode. The data format is identical to S8. The CD pin transitions will reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

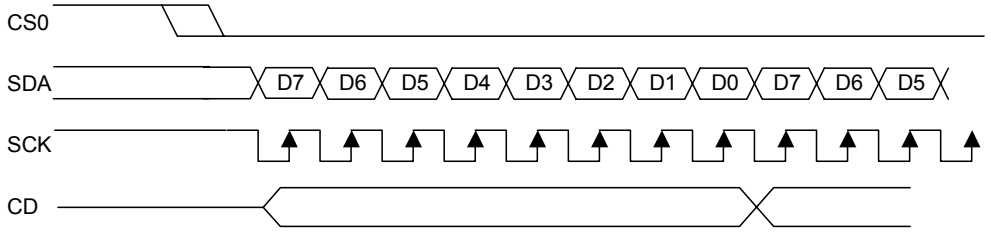


FIGURE 4.b: 3/4-wire Serial Interface (S8uc)

S9 (3-WIRE) INTERFACE

Only Write operation is supported in this 3-wire serial mode. Pins CS[1-0] are used for chip select and bus cycle reset. On each Write cycle, the first bit is CD, which determines the interpretation of the following 8 bits of data, MSB first. These 8 command/data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the following byte will be decoded as command.

If CD=1, the following byte will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

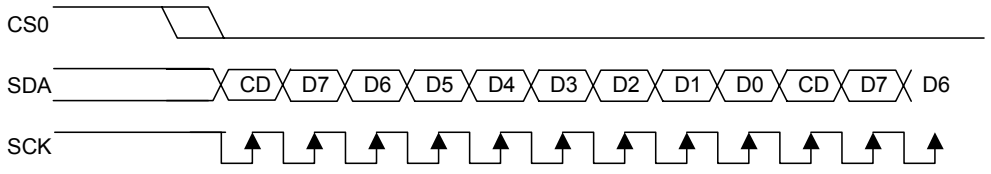


FIGURE 4.c: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

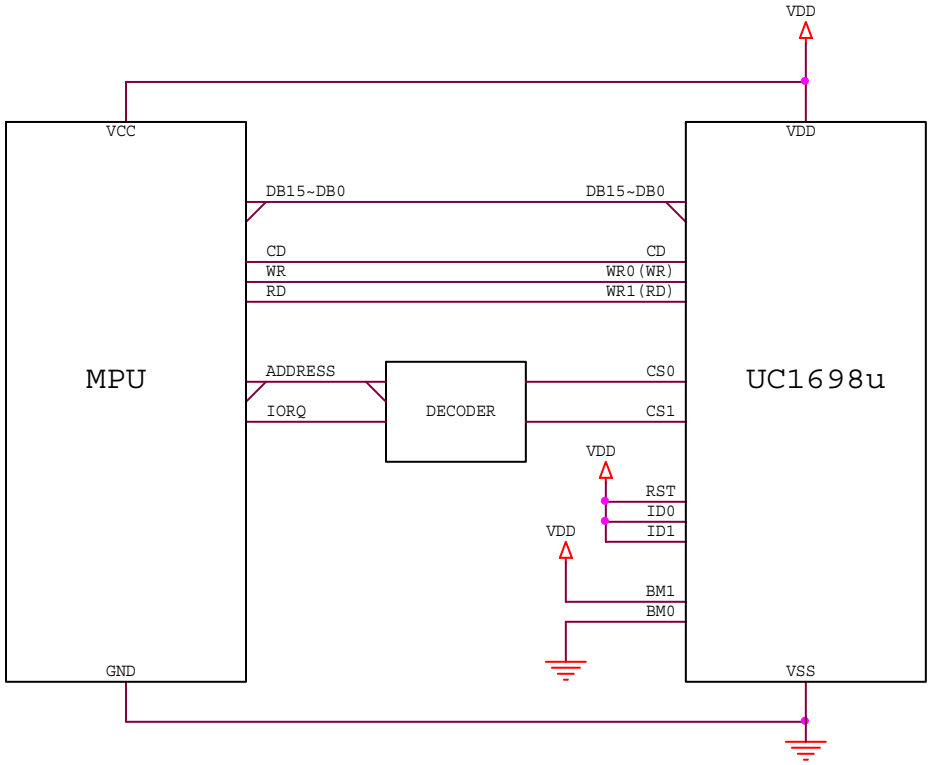


FIGURE 5: 8080/16-bit parallel mode example

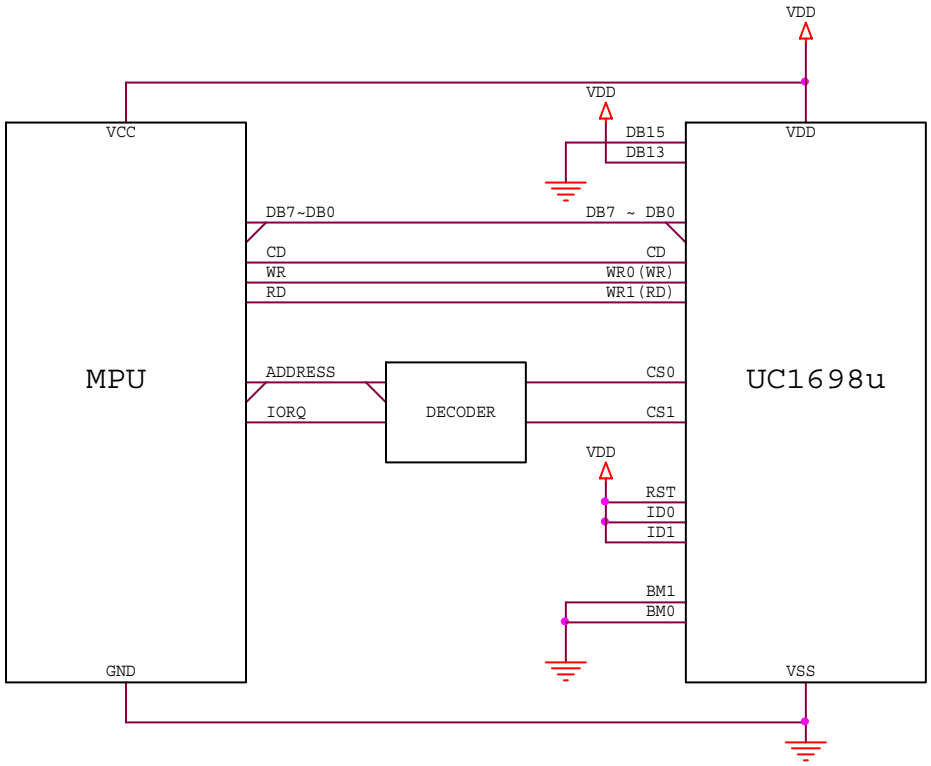


FIGURE 6: 8080/8-bit parallel mode example

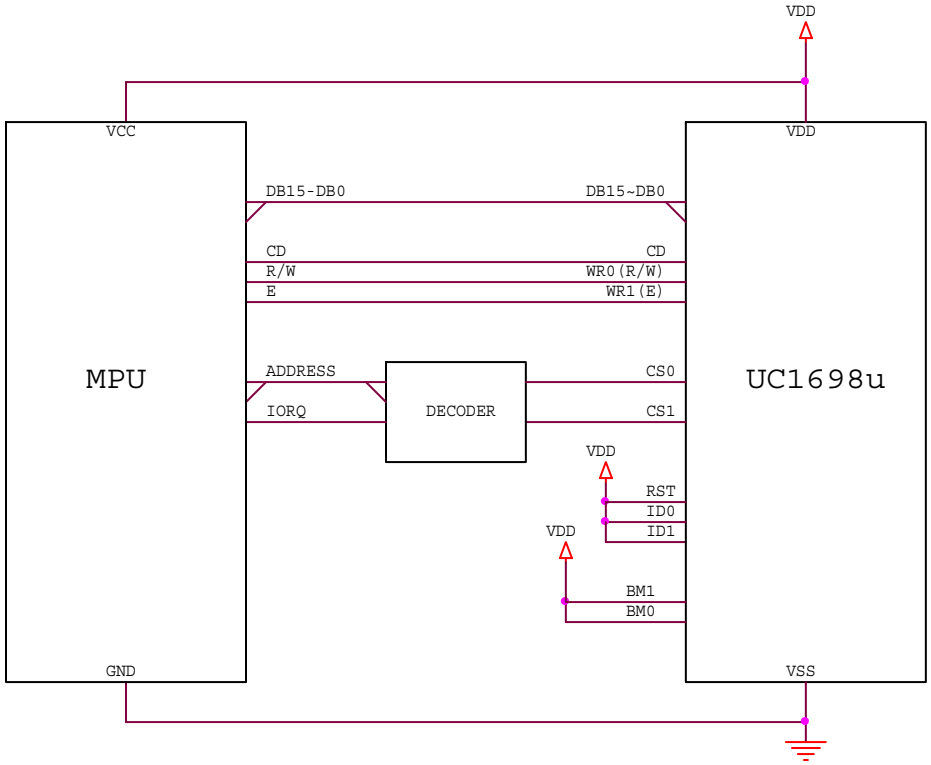


FIGURE 7: 6800/16-bit parallel mode example

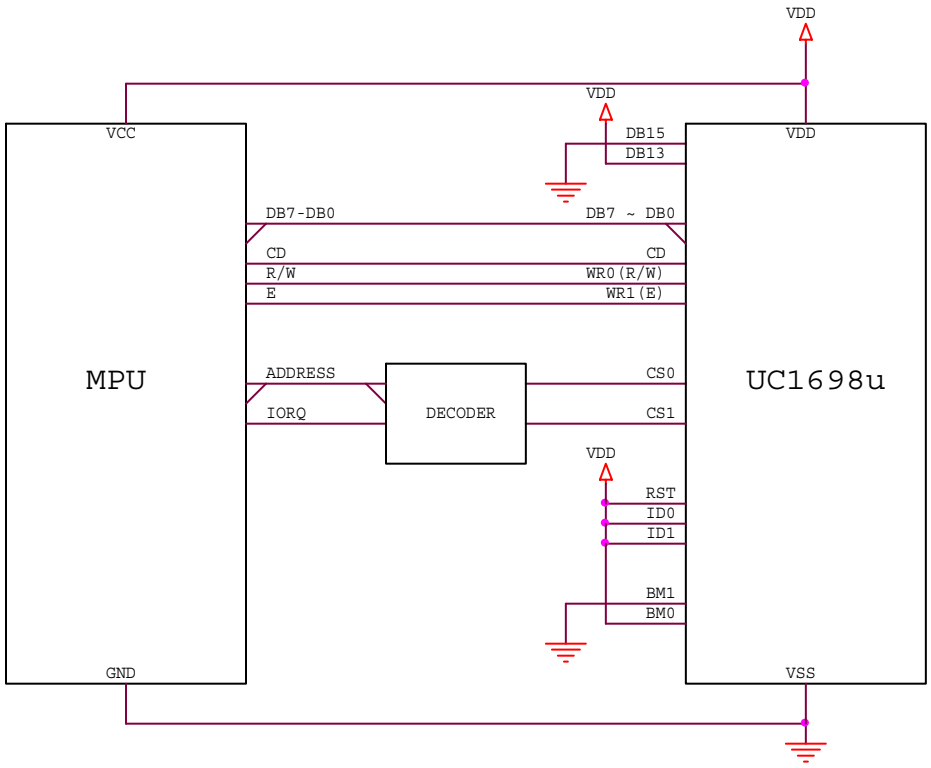


FIGURE 8: 6800/8-bit parallel mode example

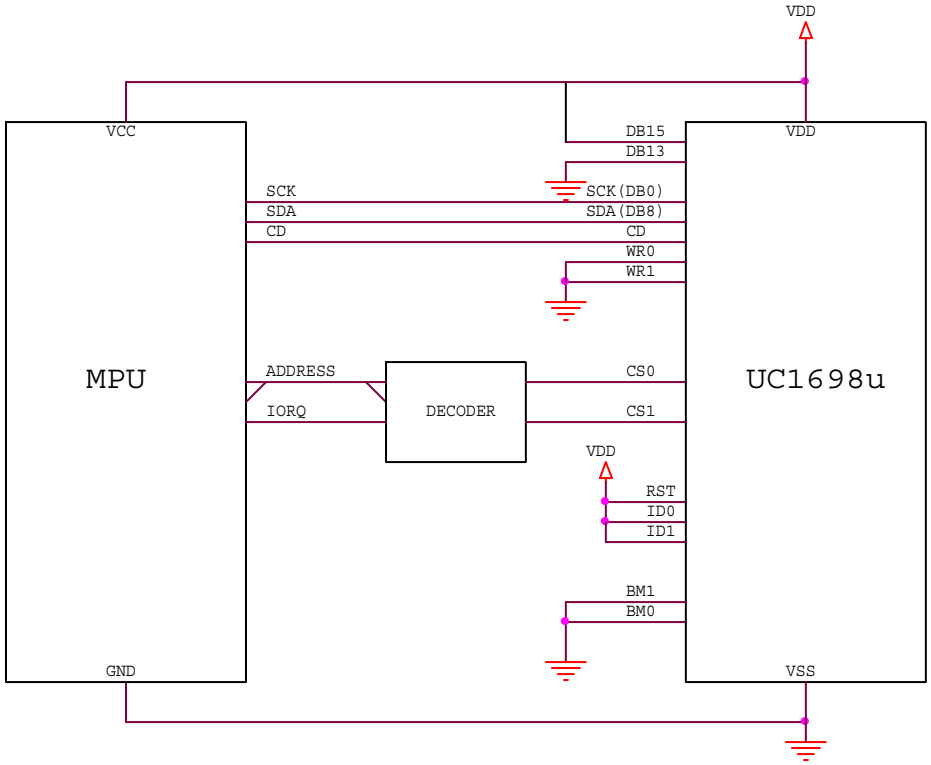


FIGURE 9: 4-Wires SPI (S8) serial mode example

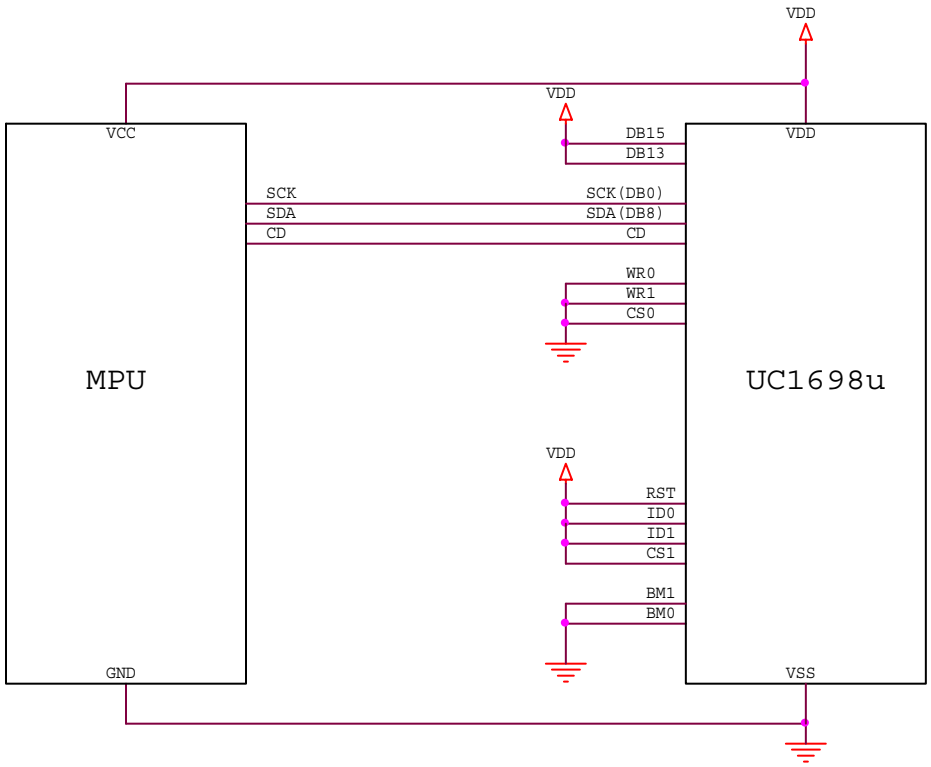


FIGURE 10: 3/4-Wires SPI (S8uc) serial mode example

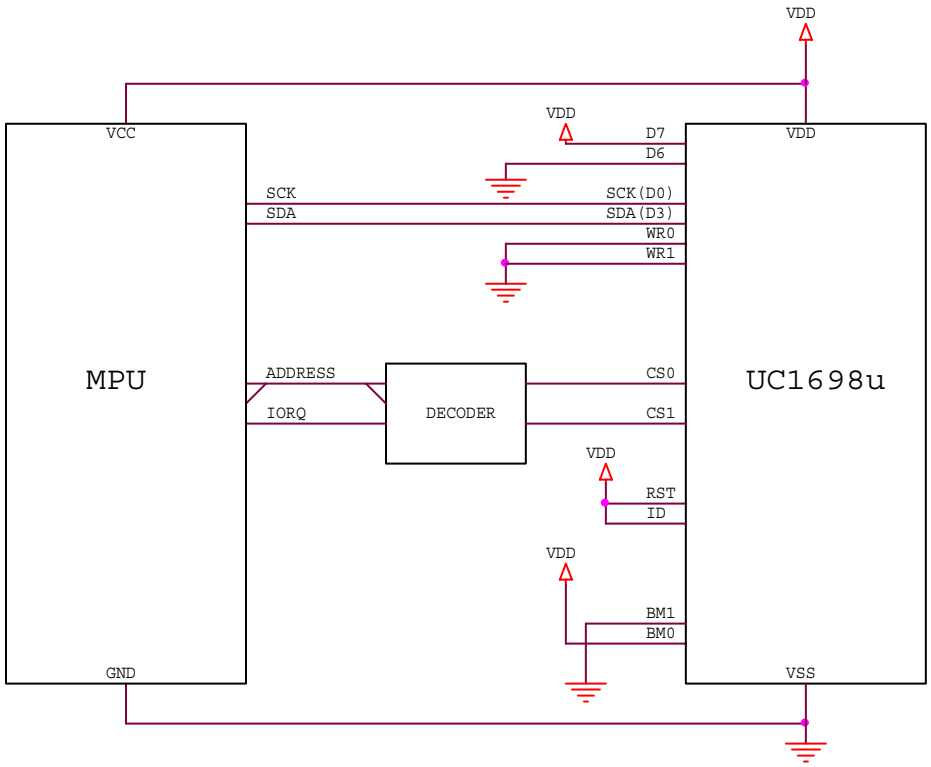


FIGURE 11: 3-Wire (S9) mode example

Note

- Pins ID0 and ID1 are for production control. Their connection will affect the content of D[3:2] of the third byte of the `Get Status` command. Connect to V_{DD} for “H” or V_{SS} for “L”.
- The RST pin is optional. Connect it to V_{DD} when not used.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 160x128X16.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *`Set Row Address`* and `Set Column Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (159), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 159), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (127–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FTB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 160)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches 160. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, 160)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1*, 160)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

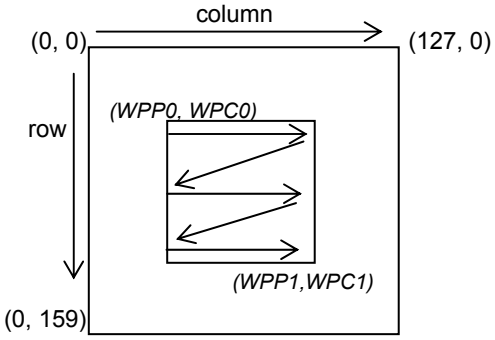
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and AC[3] setting for inside/outside window mode. When AC[3] is set to '0' (default value), data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). When AC[3] is set to '1', data will be written to whole SRAM excluding the specified window area.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

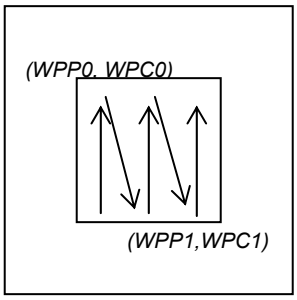
Example1 (AC[2:0] = 001) **:**

AC[3]=0 MX=0



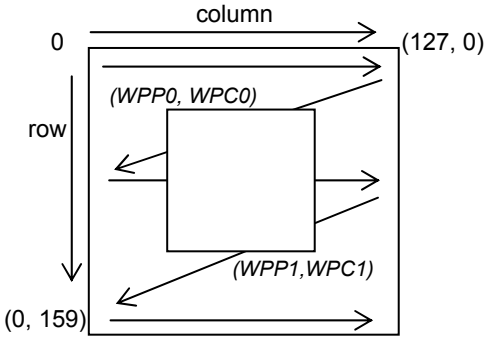
Example 2 (AC[2:0] = 111) **:**

AC[3] = 0 MX = 0



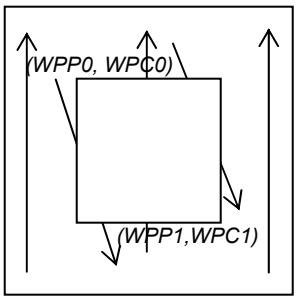
Example1-1 :

AC[3]=1 MX=0



Example 2-1 :

AC[3] = 1 MX = 0



Row Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H		COM1	COM17	COM160	COM16
01H		COM2	COM18	COM159	COM15
02H		COM3	COM19	COM158	COM14
03H		COM4	COM20	COM157	COM13
04H		COM5	COM21	COM156	COM12
05H		COM6	COM22	COM155	COM11
06H		COM7	COM23	COM154	COM10
07H		COM8	COM24	COM153	COM9
08H		COM9	COM25	COM152	COM8
09H		COM10	COM26	COM151	COM7
0AH		COM11	COM27	COM150	COM6
0BH		COM12	COM28	COM149	COM5
0CH		COM13	COM29	COM148	COM4
0DH		COM14	COM30	COM147	COM3
0EH		COM15	COM31	COM146	COM2
0FH		COM16	COM32	COM145	COM1
10H		COM17	COM33	COM144	COM160
11H		COM18	COM34	COM143	COM159
12H		COM19	COM35	COM142	COM158
13H		COM20	COM36	COM141	COM157
14H		COM21	COM37	COM140	COM156
15H		COM22	COM38	COM139	COM155
16H		COM23	COM39	COM138	COM154
17H		COM24	COM40	COM137	COM153
18H		COM25	COM41	COM136	COM152
19H		COM26	COM42	COM135	COM151
1AH		COM27	COM43	COM134	COM150
1BH		COM28	COM44	COM133	COM149
1CH		COM29	COM45	COM132	COM148
88H		COM137	COM153	COM24	COM40
89H		COM138	COM154	COM23	COM39
8AH		COM139	COM155	COM22	COM38
8BH		COM140	COM156	COM21	COM37
8CH		COM141	COM157	COM20	COM36
8DH		COM142	COM158	COM19	COM35
8EH		COM143	COM159	COM18	COM34
8FH		COM144	COM160	COM17	COM33
90H		COM145	COM1	COM16	COM32
91H		COM146	COM2	COM15	COM31
92H		COM147	COM3	COM14	COM30
93H		COM148	COM4	COM13	COM29
94H		COM149	COM5	COM12	COM28
95H		COM150	COM6	COM11	COM27
96H		COM151	COM7	COM10	COM26
97H		COM152	COM8	COM9	COM25
98H		COM153	COM9	COM8	COM24
99H		COM154	COM10	COM7	COM23
9AH		COM155	COM11	COM6	COM22
9BH		COM156	COM12	COM5	COM21
9CH		COM157	COM13	COM4	COM20
9DH		COM158	COM14	COM3	COM19
9EH		COM159	COM15	COM2	COM18
9FH		COM160	COM16	COM1	COM17

MX	SEG1	SEG2	SEG3	SEG4	SEG5			SEG380	SEG381	SEG382	SEG383	SEG384
0	SEG1	SEG2	SEG3	SEG4	SEG5			SEG380	SEG381	SEG382	SEG383	SEG384
1	SEG382	SEG383	SEG384	SEG379	SEG380			SEG5	SEG6	SEG1	SEG2	SEG3

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st Byte write data: 11111111b

⇒ 2nd Byte write data: 11111111b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1698u has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 150mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command (that's Software Reset) or by connecting RST pin to ground (that's Pin Reset).

In the following discussions, Reset means Software Reset.

RESET STATUS

When UC1698u enters RESET sequence:

- Operation mode will be "Reset".
- All control registers are reset to default values. Refer to section *Control Registers* for details of their default values.

OPERATION MODES

UC1698u has three operating modes (OM): Reset, Sleep, Normal.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by `Set Display Enable`, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1698u internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` or `System Reset` command.

Action	Mode	OM
Reset command Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

The difference between Software Reset and Pin Reset is that, Pin Reset does not drain the charge stored in the external capacitors C_{B0}, C_{B1} and C_L.

It is recommended to use Sleep Mode for Display OFF operations as UC1698u consumes very little energy in Sleep mode (typically under 2µA).

EXITING SLEEP MODE

UC1698u contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1698u internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1698u power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1698u. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD}, $V_{DD2/3}$ should be started not later than V_{DD}.

Delay allowance between V_{DD} and $V_{DD2/3}$ is illustrated as Figure 14.

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L from causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

When internal V_{LCD} is not used, UC1698u will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

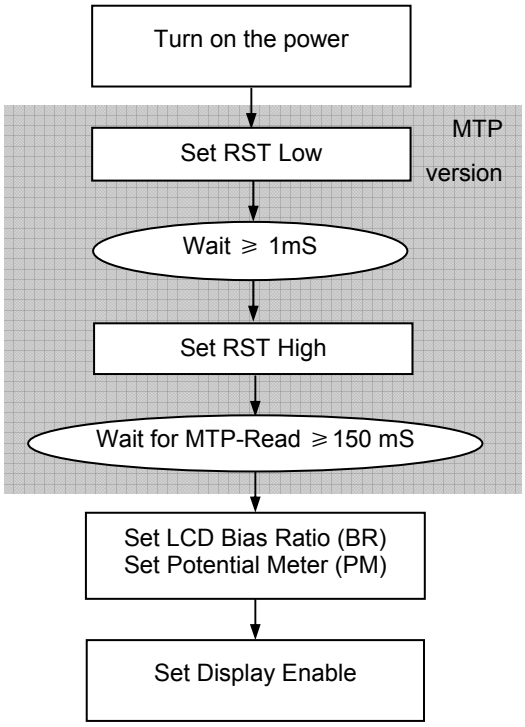


Figure 12: Reference Power-Up Sequence

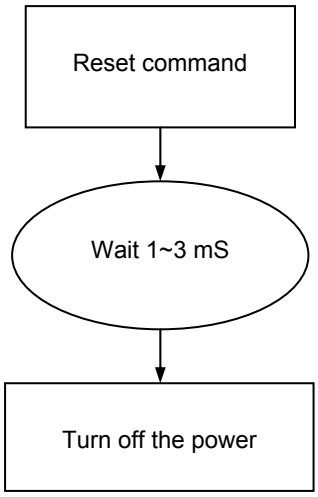


Figure 13: Reference Power-Down Sequence

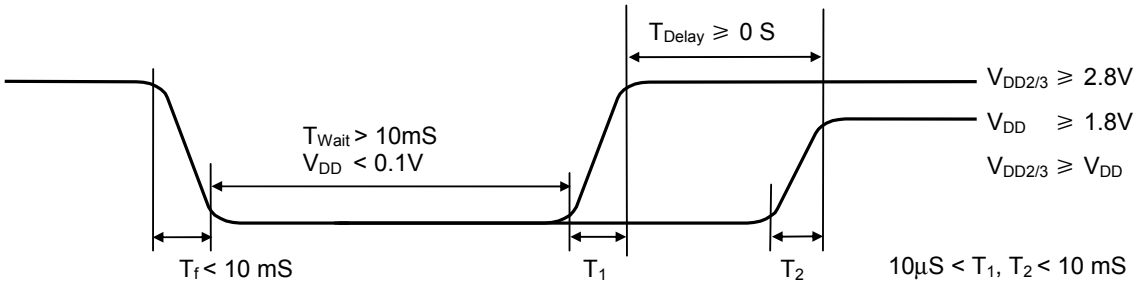


Figure 14: Delay allowance and Power Off-On Sequence

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1698u such that LCM makers can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1698u:

MTP-Erase, MTP-Program, MTP-Read.

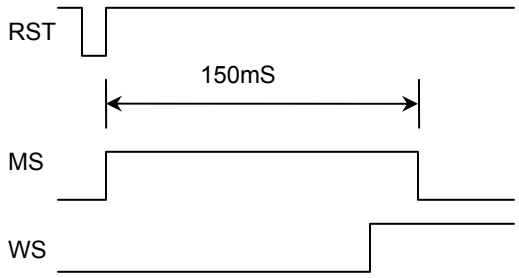
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1698u, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1698u, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use *Read Status* command in a polling loop to make sure {MS, WS}={0, 1} before proceeding with the normal operations, however, it may be simpler to just issue *Set Display Enable* command every 0.5~2 seconds, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above “Periodical re-initializing” approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose while use power down and hardware RESET only during the event of power up.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operations, TST4 should be open, or connected to V_{DD3}.

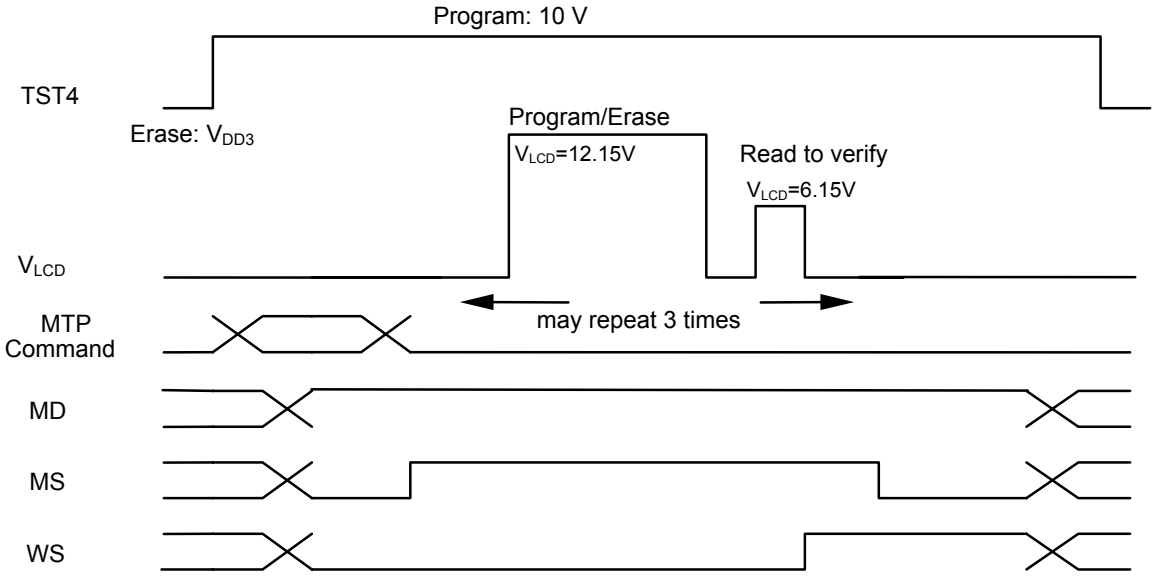
	V_{LCD}	**TST4 (external input)**
Program	MTP3 : 00h (12.15 V)	10V (1mA per bit)
Erase	MTP3 : 00h (12.15 V)	Floating or V_{DD3}
Read	MTP2 : 00h (6.15 V)	Floating or V_{DD3}

Note:

1. Do Erase before Program and program one bit at a time.
2. When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqq 3.0V$

2. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

MTP CELL VALUE USAGE

There are 9 MTP cell bits. They are divided into two groups for different purpose.

MTP[6:0] : V_{LCD} Trim
When PMO[6]=1: PM with trim = PM - PMO[5:0]
When PMO[6]=0: PM with trim = PM + PMO[5:0]

MTPID[1:0]: For LCM manufacturer's configuration.

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP1: 00h(6.15 V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(12.15 V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP3: 50h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP4: 08h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	1 0	MTPM MTPM1	Ex: To program MTPM[0] to be 1, set the value to 00000001b *
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 10 V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0 and WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP1: 00h(6.15V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h (12.15V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP3: 50h (100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP4: 08h (10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0 0	0 0	0 0	0 0	1 0	1 0	1 0	1 0	MTPM MTPM1	Ex: To erase MTPM[3:0], set the value to 00001111b
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R											V_{DD}=0V	Power OFF

Note: It is recommended that users clear all the bits to be programmed.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Color Mode	
C	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	LCD specific operating voltage setting
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

* For power saving mode, please refer to UltraChip document "03-OTS-003 Power Saving Mode Disable Application Note version A".

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1698u require special "ESD Sensitivity" consideration in particular:

		Test Mode			
		MM V_{DD}	MM V_{SS}	HBM V_{DD}	HBM V_{SS}
LCD Driver		200	200	2000	2000
LCM Interface		300	300	3000	3000
LCM HV pin/ Test pin	TST1/2/4	200	200	2000	2000
	C_B pins	200	200	2000	2000
	V_{LCDIN}	200	200	2000	2000
	V_{LCDOUT}	200	200	2000	2000
PWR / GND			300		3000

* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, Note 1 and 2

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Driving voltage (-25^{O}C ~ +75^{O}C)	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

NOTE:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.465	V
$V_{DD2/3}$	Supply for bias & pump		2.7		3.465	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ = 2.8V, 25^{O}C		15.2	18	V
V_D	LCD data voltage	$V_{DD2/3}$ = 2.8V, 25^{O}C	1.09		1.95	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	µA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85^{O}C			50	µA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 16.5V		850	1100	Ω
$R_{ON(COM)}$	COM output impedance	V_{LCD} = 16.5V		950	1100	Ω
f_{LINE}	Average line rate	LC[4:3] = 10b, 25^{O}C	-10%	37.0	+10%	Klps

POWER CONSUMPTION

V_{DD} = 2.7 V,
V_{LCD} = 16.5 V,
Mux Rate = 160,
C_B = 2.2 µF,
N-line inversion = 31 lines

Bias Ratio = 12,
Line Rate = 10b,
Bus mode = 6800,
Temperature = 25^{o}C,
Color Mode = 64K color mode,

PM = 64,
Panel Loading (PC[1:0]) = 0b,
C_L = 330 nF,
MTP=00 H,
All HV outputs are open circuit.

Display Pattern	Conditions	Typ. (µA)	Max. (µA)
All-Pixel-OFF	Bus = idle	1764	2470
2-pixel checker	Bus = idle	2468	3455
None	Reset (stand-by current)	<1	5

AC CHARACTERISTICS

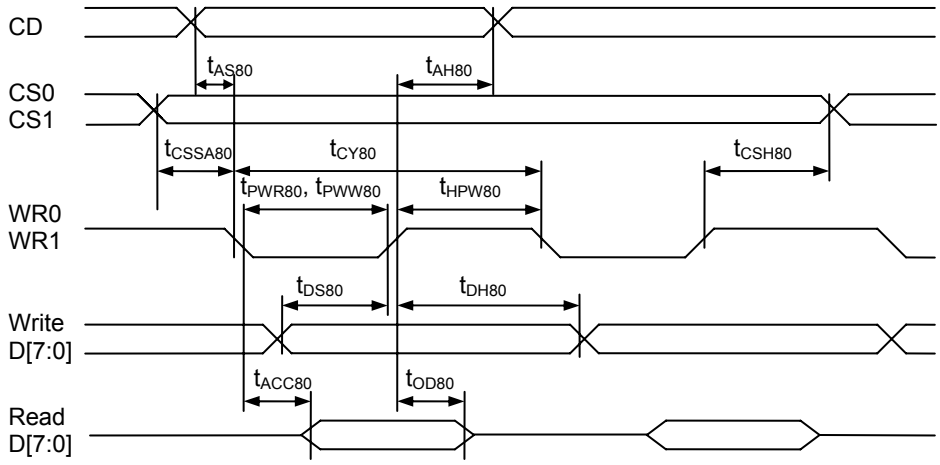


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 170 130 100 80 90	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit	 LC[7:6]=10b LC[7:6]=01b	65 40 45	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 85 65 50 40 45	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
T_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 5		nS

(1.65V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 320 270 180 145 220	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit		160 90	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit	 LC[7:6]=10b LC[7:6]=01b	135 73 110	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bits bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 160 135 90 72 110	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		60 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 30	120 60	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10		nS

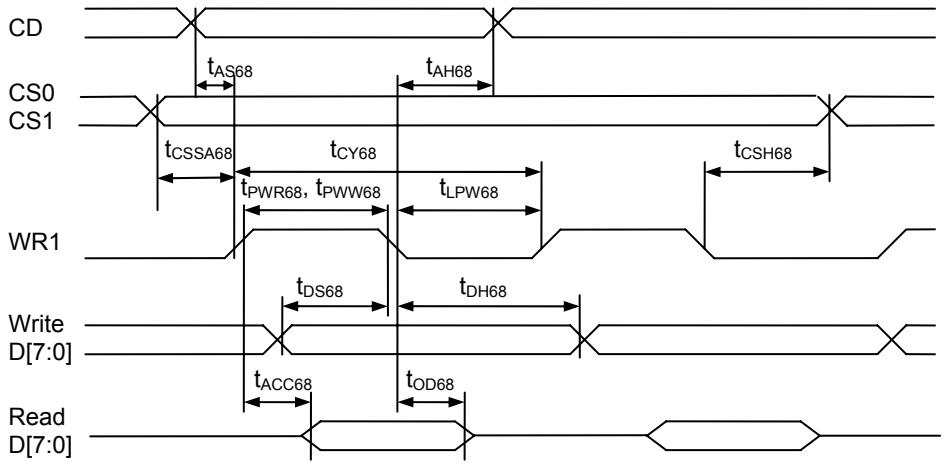


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 170 130 100 80 90	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit	 LC[7:6]=10b LC[7:6]=01b	65 40 45	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 85 65 50 40 45	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 5		nS

(1.65V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 320 270 180 145 220	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit		160 90	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit	 LC[7:6]=10b LC[7:6]=01b	135 73 110	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)	 LC[7:6]=10b LC[7:6]=01b	 160 135 90 72 110	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	- 30	120 60	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10		nS

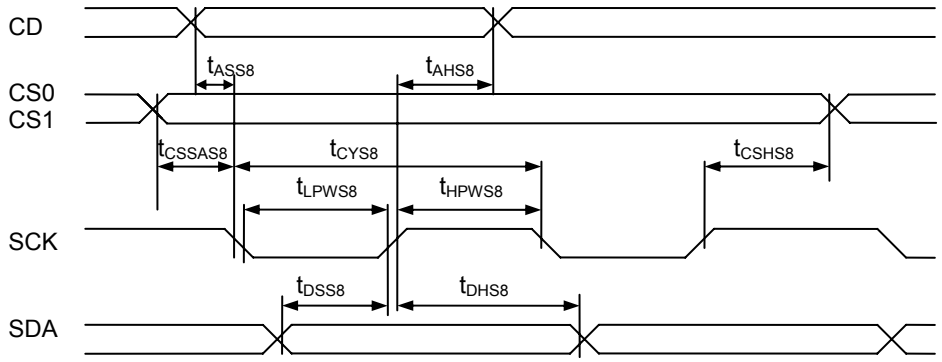


FIGURE 17: Serial Bus Timing Characteristics (for S8/S8uc)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		40	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		75	–	nS
t_{LPWS8}		Low pulse width		37	–	nS
t_{HPWS8}		High pulse width		38	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10		nS

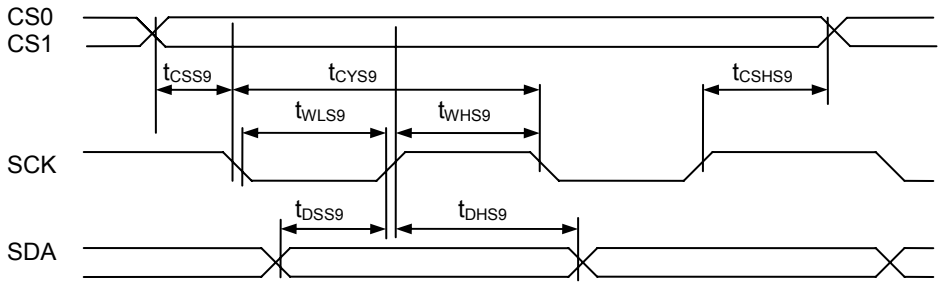


FIGURE 18: Serial Bus Timing Characteristics (for S9)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		40	–	nS
t_{LPWS9}		Low pulse width		20	–	nS
t_{HPWS9}		High pulse width		20	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		75	–	nS
t_{LPWS9}		Low pulse width		38	–	nS
t_{HPWS9}		High pulse width		38	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10		nS

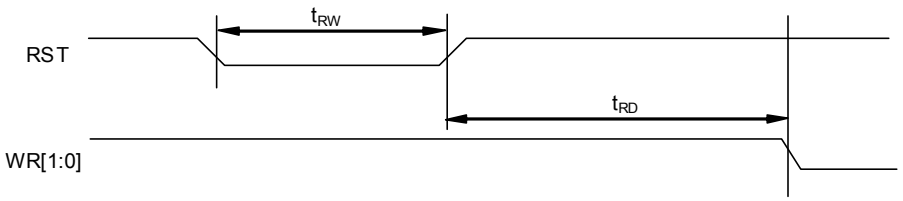


FIGURE 19: Reset Characteristics

(1.65V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
13380µM x 1712µM ± 50µM

DIE THICKNESS:
0.4mm ± 0.02mm

BUMP HEIGHT:
15 µM
(H_{MAX}-H_{MIN}) within die < 2µM

COM/SEG SIZE:
17.5 x 115 μM^2 (Typ.)

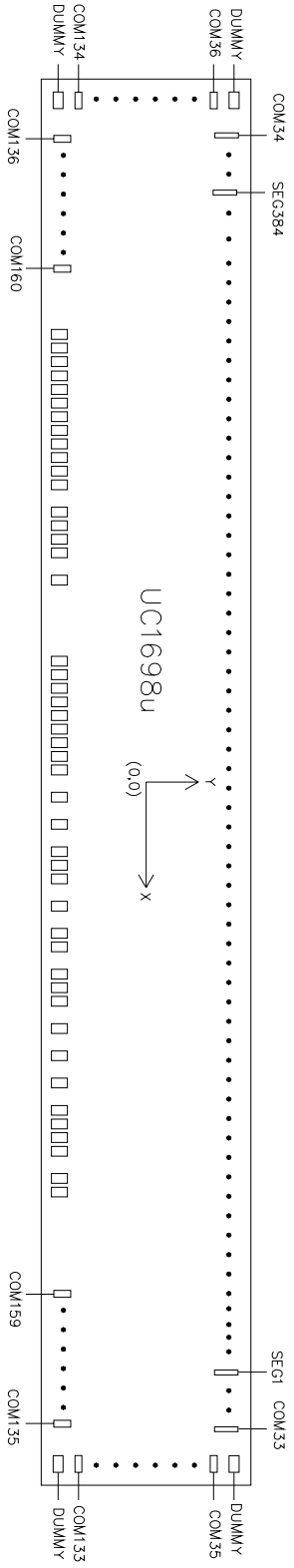
BUMP PITCH:
COM: 31 µM (Typ.)
SEG: 31 µM (Typ.)

BUMP GAP:
SEG/COM: 13.5µM (Typ.)
11.5µM (Min.)

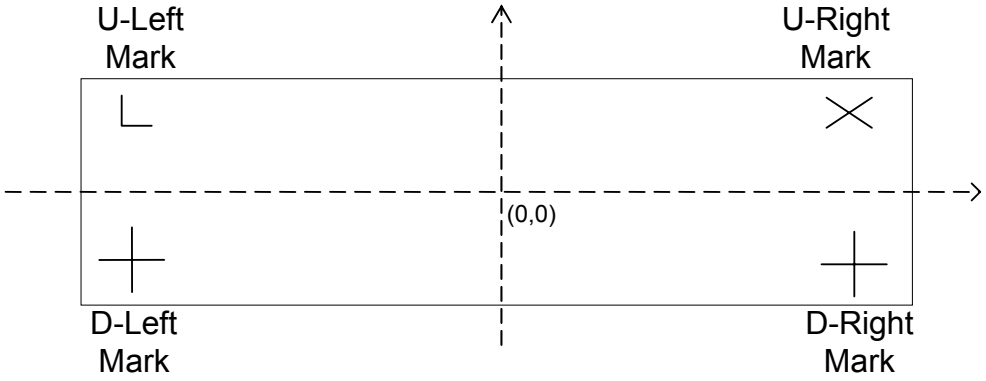
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

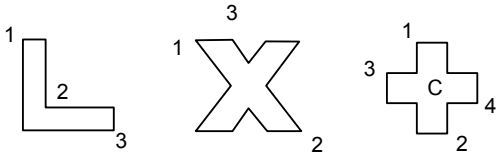
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

The “x” and “+” marks are symmetric both horizontally and vertically.

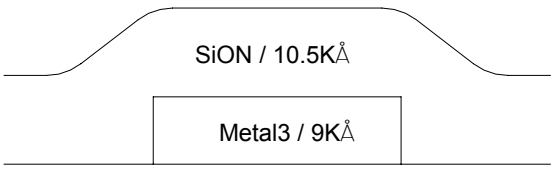
COORDINATES:

	U-Left Mark (L)		U-Right Mark (X)	
	X	Y	X	Y
1	-6479.3	593.2	6439.8	593.2
2	-6463.7	568.7	6479.8	553.2
3	-6439.4	553.2	6449.8	593.2

	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1	-6003.0	-711.6	5983.0	-711.6
2	-5983.0	-796.6	6003.0	-796.6
3	-6035.5	-744.1	5950.5	-744.1
4	-5950.5	-764.1	6035.5	-764.1
C	-5993.0	-754.1	5993.0	-754.1

Note: The values of x-coordinate and y-coordinate in the tables are after-rounded.

TOP METAL AND PASSIVATION:



FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-6579.8	792.5	115	21.5
2	COM36	-6579.8	759.5	115	17.5
3	COM38	-6579.8	728.5	115	17.5
4	COM40	-6579.8	697.5	115	17.5
5	COM42	-6579.8	666.5	115	17.5
6	COM44	-6579.8	635.5	115	17.5
7	COM46	-6579.8	604.5	115	17.5
8	COM48	-6579.8	573.5	115	17.5
9	COM50	-6579.8	542.5	115	17.5
10	COM52	-6579.8	511.5	115	17.5
11	COM54	-6579.8	480.5	115	17.5
12	COM56	-6579.8	449.5	115	17.5
13	COM58	-6579.8	418.5	115	17.5
14	COM60	-6579.8	387.5	115	17.5
15	COM62	-6579.8	356.5	115	17.5
16	COM64	-6579.8	325.5	115	17.5
17	COM66	-6579.8	294.5	115	17.5
18	COM68	-6579.8	263.5	115	17.5
19	COM70	-6579.8	232.5	115	17.5
20	COM72	-6579.8	201.5	115	17.5
21	COM74	-6579.8	170.5	115	17.5
22	COM76	-6579.8	139.5	115	17.5
23	COM78	-6579.8	108.5	115	17.5
24	COM80	-6579.8	77.5	115	17.5
25	COM82	-6579.8	46.5	115	17.5
26	COM84	-6579.8	15.5	115	17.5
27	COM86	-6579.8	-15.5	115	17.5
28	COM88	-6579.8	-46.5	115	17.5
29	COM90	-6579.8	-77.5	115	17.5
30	COM92	-6579.8	-108.5	115	17.5
31	COM94	-6579.8	-139.5	115	17.5
32	COM96	-6579.8	-170.5	115	17.5
33	COM98	-6579.8	-201.5	115	17.5
34	COM100	-6579.8	-232.5	115	17.5
35	COM102	-6579.8	-263.5	115	17.5
36	COM104	-6579.8	-294.5	115	17.5
37	COM106	-6579.8	-325.5	115	17.5
38	COM108	-6579.8	-356.5	115	17.5
39	COM110	-6579.8	-387.5	115	17.5
40	COM112	-6579.8	-418.5	115	17.5
41	COM114	-6579.8	-449.5	115	17.5
42	COM116	-6579.8	-480.5	115	17.5
43	COM118	-6579.8	-511.5	115	17.5
44	COM120	-6579.8	-542.5	115	17.5
45	COM122	-6579.8	-573.5	115	17.5
46	COM124	-6579.8	-604.5	115	17.5
47	COM126	-6579.8	-635.5	115	17.5
48	COM128	-6579.8	-666.5	115	17.5
49	COM130	-6579.8	-697.5	115	17.5
50	COM132	-6579.8	-728.5	115	17.5
51	COM134	-6579.8	-759.5	115	17.5
52	DUMMY	-6579.8	-792.5	115	21.5
53	COM136	-6463.5	-748.1	17.5	115
54	COM138	-6432.5	-748.1	17.5	115
55	COM140	-6401.5	-748.1	17.5	115

#	Pad	X	Y	W	H
56	COM142	-6370.5	-748.1	17.5	115
57	COM144	-6339.5	-748.1	17.5	115
58	COM146	-6308.5	-748.1	17.5	115
59	COM148	-6277.5	-748.1	17.5	115
60	COM150	-6246.5	-748.1	17.5	115
61	COM152	-6215.5	-748.1	17.5	115
62	COM154	-6184.5	-748.1	17.5	115
63	COM156	-6153.5	-748.1	17.5	115
64	COM158	-6122.5	-748.1	17.5	115
65	COM160	-6091.5	-748.1	17.5	115
66	D15	-5801.4	-762.6	45	84
67	VDDX	-5741.4	-762.6	45	84
68	D14	-5681.4	-762.6	45	84
69	D13	-5435.4	-762.6	45	84
70	D12	-5375.4	-762.6	45	84
71	D11	-5129.4	-762.6	45	84
72	D10	-5069.4	-762.6	45	84
73	D9	-4823.4	-762.6	45	84
74	D8	-4763.4	-762.6	45	84
75	D7	-4517.4	-762.6	45	84
76	D6	-4457.4	-762.6	45	84
77	D5	-4211.4	-762.6	45	84
78	D4	-4151.4	-762.6	45	84
79	D3	-3905.4	-762.6	45	84
80	D2	-3845.4	-762.6	45	84
81	D1	-3599.4	-762.6	45	84
82	D0	-3539.4	-762.6	45	84
83	RST	-3377.4	-762.6	45	84
84	WR0	-3131.4	-762.6	45	84
85	VDDX	-3071.4	-762.6	45	84
86	WR1	-3011.4	-762.6	45	84
87	CD	-2849.4	-762.6	45	84
88	CS0	-2603.4	-762.6	45	84
89	VDDX	-2543.4	-762.6	45	84
90	CS1	-2483.4	-762.6	45	84
91	BM0	-2237.4	-762.6	45	84
92	VDDX	-2177.4	-762.6	45	84
93	BM1	-2117.4	-762.6	45	84
94	TST4	-1955.4	-762.6	45	84
95	TST4	-1895.4	-762.6	45	84
96	TST1	-1484.5	-762.6	45	84
97	TST2	-1424.5	-762.6	45	84
98	ID0	-1167.9	-762.6	45	84
99	VDDX	-1107.9	-762.6	45	84
100	ID1	-1047.9	-762.6	45	84
101	VSS	-885.9	-762.6	45	84
102	VSS	-825.9	-762.6	45	84
103	VSS	-765.9	-762.6	45	84
104	VSS	-705.9	-762.6	45	84
105	VSS	-645.9	-762.6	45	84
106	VSS	-585.9	-762.6	45	84
107	VSS	-525.9	-762.6	45	84
108	VSS	-465.9	-762.6	45	84
109	VSS	-405.9	-762.6	45	84
110	VSS	-345.9	-762.6	45	84

#	Pad	X	Y	W	H
111	VSS	-285.9	-762.6	45	84
112	VSS	-225.9	-762.6	45	84
113	VSS2	-52.9	-762.6	45	84
114	VSS2	7.1	-762.6	45	84
115	VSS2	67.1	-762.6	45	84
116	VSS2	127.1	-762.6	45	84
117	VSS2	187.1	-762.6	45	84
118	VSS2	247.1	-762.6	45	84
119	VSS2	307.1	-762.6	45	84
120	VSS2	367.1	-762.6	45	84
121	VSS2	427.1	-762.6	45	84
122	VSS2	487.1	-762.6	45	84
123	VSS2	547.1	-762.6	45	84
124	VSS2	607.1	-762.6	45	84
125	VDD	667.1	-762.6	45	84
126	VDD	727.1	-762.6	45	84
127	VDD	787.1	-762.6	45	84
128	VDD	847.1	-762.6	45	84
129	VDD	907.1	-762.6	45	84
130	VDD	967.1	-762.6	45	84
131	VDD	1027.1	-762.6	45	84
132	VDD	1087.1	-762.6	45	84
133	VDD	1147.1	-762.6	45	84
134	VDD2	1697.4	-762.6	45	84
135	VDD2	1757.4	-762.6	45	84
136	VDD2	1817.4	-762.6	45	84
137	VDD2	1877.4	-762.6	45	84
138	VDD2	1937.4	-762.6	45	84
139	VDD2	1997.4	-762.6	45	84
140	VDD2	2057.4	-762.6	45	84
141	VDD2	2117.4	-762.6	45	84
142	VDD2	2177.4	-762.6	45	84
143	VDD3	2442.2	-762.6	45	84
144	VDD3	2502.2	-762.6	45	84
145	VB0+	2577.2	-762.6	45	84
146	VB0+	2637.2	-762.6	45	84
147	VB0+	2697.2	-762.6	45	84
148	VB0+	2757.2	-762.6	45	84
149	VB1+	2973.4	-762.6	45	84
150	VB1+	3033.4	-762.6	45	84
151	VB1+	3093.4	-762.6	45	84
152	VB1+	3153.4	-762.6	45	84
153	VB1-	3369.5	-762.6	45	84
154	VB1-	3429.5	-762.6	45	84
155	VB1-	3489.5	-762.6	45	84
156	VB1-	3549.5	-762.6	45	84
157	VB0-	3765.7	-762.6	45	84
158	VB0-	3825.7	-762.6	45	84
159	VB0-	3885.7	-762.6	45	84
160	VB0-	3945.7	-762.6	45	84
161	VS-	4162.2	-762.6	45	84
162	VS-	4502.2	-762.6	45	84
163	VS-	4562.2	-762.6	45	84
164	VS+	4902.2	-762.6	45	84
165	VS+	4962.2	-762.6	45	84
166	VS+	5302.2	-762.6	45	84
167	VLCDIN	5510.4	-762.6	45	84
168	VLCDIN	5570.4	-762.6	45	84
169	VLCDOUT	5630.4	-762.6	45	84
170	VLCDOUT	5690.4	-762.6	45	84
171	COM159	6091.5	-748.1	17.5	115
172	COM157	6122.5	-748.1	17.5	115
173	COM155	6153.5	-748.1	17.5	115
174	COM153	6184.5	-748.1	17.5	115
175	COM151	6215.5	-748.1	17.5	115
176	COM149	6246.5	-748.1	17.5	115
177	COM147	6277.5	-748.1	17.5	115
178	COM145	6308.5	-748.1	17.5	115
179	COM143	6339.5	-748.1	17.5	115
180	COM141	6370.5	-748.1	17.5	115
181	COM139	6401.5	-748.1	17.5	115
182	COM137	6432.5	-748.1	17.5	115
183	COM135	6463.5	-748.1	17.5	115
184	DUMMY	6579.8	-792.5	115	21.5
185	COM133	6579.8	-759.5	115	17.5
186	COM131	6579.8	-728.5	115	17.5
187	COM129	6579.8	-697.5	115	17.5
188	COM127	6579.8	-666.5	115	17.5
189	COM125	6579.8	-635.5	115	17.5
190	COM123	6579.8	-604.5	115	17.5
191	COM121	6579.8	-573.5	115	17.5
192	COM119	6579.8	-542.5	115	17.5
193	COM117	6579.8	-511.5	115	17.5
194	COM115	6579.8	-480.5	115	17.5
195	COM113	6579.8	-449.5	115	17.5
196	COM111	6579.8	-418.5	115	17.5
197	COM109	6579.8	-387.5	115	17.5
198	COM107	6579.8	-356.5	115	17.5
199	COM105	6579.8	-325.5	115	17.5
200	COM103	6579.8	-294.5	115	17.5
201	COM101	6579.8	-263.5	115	17.5
202	COM99	6579.8	-232.5	115	17.5
203	COM97	6579.8	-201.5	115	17.5
204	COM95	6579.8	-170.5	115	17.5
205	COM93	6579.8	-139.5	115	17.5
206	COM91	6579.8	-108.5	115	17.5
207	COM89	6579.8	-77.5	115	17.5
208	COM87	6579.8	-46.5	115	17.5
209	COM85	6579.8	-15.5	115	17.5
210	COM83	6579.8	15.5	115	17.5
211	COM81	6579.8	46.5	115	17.5
212	COM79	6579.8	77.5	115	17.5
213	COM77	6579.8	108.5	115	17.5
214	COM75	6579.8	139.5	115	17.5
215	COM73	6579.8	170.5	115	17.5
216	COM71	6579.8	201.5	115	17.5
217	COM69	6579.8	232.5	115	17.5
218	COM67	6579.8	263.5	115	17.5
219	COM65	6579.8	294.5	115	17.5
220	COM63	6579.8	325.5	115	17.5
221	COM61	6579.8	356.5	115	17.5
222	COM59	6579.8	387.5	115	17.5
223	COM57	6579.8	418.5	115	17.5
224	COM55	6579.8	449.5	115	17.5

#	Pad	X	Y	W	H
225	COM53	6579.8	480.5	115	17.5
226	COM51	6579.8	511.5	115	17.5
227	COM49	6579.8	542.5	115	17.5
228	COM47	6579.8	573.5	115	17.5
229	COM45	6579.8	604.5	115	17.5
230	COM43	6579.8	635.5	115	17.5
231	COM41	6579.8	666.5	115	17.5
232	COM39	6579.8	697.5	115	17.5
233	COM37	6579.8	728.5	115	17.5
234	COM35	6579.8	759.5	115	17.5
235	DUMMY	6579.8	792.5	115	21.5
236	COM33	6463.5	748.1	17.5	115
237	COM31	6432.5	748.1	17.5	115
238	COM29	6401.5	748.1	17.5	115
239	COM27	6370.5	748.1	17.5	115
240	COM25	6339.5	748.1	17.5	115
241	COM23	6308.5	748.1	17.5	115
242	COM21	6277.5	748.1	17.5	115
243	COM19	6246.5	748.1	17.5	115
244	COM17	6215.5	748.1	17.5	115
245	COM15	6184.5	748.1	17.5	115
246	COM13	6153.5	748.1	17.5	115
247	COM11	6122.5	748.1	17.5	115
248	COM9	6091.5	748.1	17.5	115
249	COM7	6060.5	748.1	17.5	115
250	COM5	6029.5	748.1	17.5	115
251	COM3	5998.5	748.1	17.5	115
252	COM1	5967.5	748.1	17.5	115
253	SEG1	5936.5	748.1	17.5	115
254	SEG2	5905.5	748.1	17.5	115
255	SEG3	5874.5	748.1	17.5	115
256	SEG4	5843.5	748.1	17.5	115
257	SEG5	5812.5	748.1	17.5	115
258	SEG6	5781.5	748.1	17.5	115
259	SEG7	5750.5	748.1	17.5	115
260	SEG8	5719.5	748.1	17.5	115
261	SEG9	5688.5	748.1	17.5	115
262	SEG10	5657.5	748.1	17.5	115
263	SEG11	5626.5	748.1	17.5	115
264	SEG12	5595.5	748.1	17.5	115
265	SEG13	5564.5	748.1	17.5	115
266	SEG14	5533.5	748.1	17.5	115
267	SEG15	5502.5	748.1	17.5	115
268	SEG16	5471.5	748.1	17.5	115
269	SEG17	5440.5	748.1	17.5	115
270	SEG18	5409.5	748.1	17.5	115
271	SEG19	5378.5	748.1	17.5	115
272	SEG20	5347.5	748.1	17.5	115
273	SEG21	5316.5	748.1	17.5	115
274	SEG22	5285.5	748.1	17.5	115
275	SEG23	5254.5	748.1	17.5	115
276	SEG24	5223.5	748.1	17.5	115
277	SEG25	5192.5	748.1	17.5	115
278	SEG26	5161.5	748.1	17.5	115
279	SEG27	5130.5	748.1	17.5	115
280	SEG28	5099.5	748.1	17.5	115
281	SEG29	5068.5	748.1	17.5	115

#	Pad	X	Y	W	H
282	SEG30	5037.5	748.1	17.5	115
283	SEG31	5006.5	748.1	17.5	115
284	SEG32	4975.5	748.1	17.5	115
285	SEG33	4944.5	748.1	17.5	115
286	SEG34	4913.5	748.1	17.5	115
287	SEG35	4882.5	748.1	17.5	115
288	SEG36	4851.5	748.1	17.5	115
289	SEG37	4820.5	748.1	17.5	115
290	SEG38	4789.5	748.1	17.5	115
291	SEG39	4758.5	748.1	17.5	115
292	SEG40	4727.5	748.1	17.5	115
293	SEG41	4696.5	748.1	17.5	115
294	SEG42	4665.5	748.1	17.5	115
295	SEG43	4634.5	748.1	17.5	115
296	SEG44	4603.5	748.1	17.5	115
297	SEG45	4572.5	748.1	17.5	115
298	SEG46	4541.5	748.1	17.5	115
299	SEG47	4510.5	748.1	17.5	115
300	SEG48	4479.5	748.1	17.5	115
301	SEG49	4448.5	748.1	17.5	115
302	SEG50	4417.5	748.1	17.5	115
303	SEG51	4386.5	748.1	17.5	115
304	SEG52	4355.5	748.1	17.5	115
305	SEG53	4324.5	748.1	17.5	115
306	SEG54	4293.5	748.1	17.5	115
307	SEG55	4262.5	748.1	17.5	115
308	SEG56	4231.5	748.1	17.5	115
309	SEG57	4200.5	748.1	17.5	115
310	SEG58	4169.5	748.1	17.5	115
311	SEG59	4138.5	748.1	17.5	115
312	SEG60	4107.5	748.1	17.5	115
313	SEG61	4076.5	748.1	17.5	115
314	SEG62	4045.5	748.1	17.5	115
315	SEG63	4014.5	748.1	17.5	115
316	SEG64	3983.5	748.1	17.5	115
317	SEG65	3952.5	748.1	17.5	115
318	SEG66	3921.5	748.1	17.5	115
319	SEG67	3890.5	748.1	17.5	115
320	SEG68	3859.5	748.1	17.5	115
321	SEG69	3828.5	748.1	17.5	115
322	SEG70	3797.5	748.1	17.5	115
323	SEG71	3766.5	748.1	17.5	115
324	SEG72	3735.5	748.1	17.5	115
325	SEG73	3704.5	748.1	17.5	115
326	SEG74	3673.5	748.1	17.5	115
327	SEG75	3642.5	748.1	17.5	115
328	SEG76	3611.5	748.1	17.5	115
329	SEG77	3580.5	748.1	17.5	115
330	SEG78	3549.5	748.1	17.5	115
331	SEG79	3518.5	748.1	17.5	115
332	SEG80	3487.5	748.1	17.5	115
333	SEG81	3456.5	748.1	17.5	115
334	SEG82	3425.5	748.1	17.5	115
335	SEG83	3394.5	748.1	17.5	115
336	SEG84	3363.5	748.1	17.5	115
337	SEG85	3332.5	748.1	17.5	115
338	SEG86	3301.5	748.1	17.5	115

#	Pad	X	Y	W	H
339	SEG87	3270.5	748.1	17.5	115
340	SEG88	3239.5	748.1	17.5	115
341	SEG89	3208.5	748.1	17.5	115
342	SEG90	3177.5	748.1	17.5	115
343	SEG91	3146.5	748.1	17.5	115
344	SEG92	3115.5	748.1	17.5	115
345	SEG93	3084.5	748.1	17.5	115
346	SEG94	3053.5	748.1	17.5	115
347	SEG95	3022.5	748.1	17.5	115
348	SEG96	2991.5	748.1	17.5	115
349	SEG97	2960.5	748.1	17.5	115
350	SEG98	2929.5	748.1	17.5	115
351	SEG99	2898.5	748.1	17.5	115
352	SEG100	2867.5	748.1	17.5	115
353	SEG101	2836.5	748.1	17.5	115
354	SEG102	2805.5	748.1	17.5	115
355	SEG103	2774.5	748.1	17.5	115
356	SEG104	2743.5	748.1	17.5	115
357	SEG105	2712.5	748.1	17.5	115
358	SEG106	2681.5	748.1	17.5	115
359	SEG107	2650.5	748.1	17.5	115
360	SEG108	2619.5	748.1	17.5	115
361	SEG109	2588.5	748.1	17.5	115
362	SEG110	2557.5	748.1	17.5	115
363	SEG111	2526.5	748.1	17.5	115
364	SEG112	2495.5	748.1	17.5	115
365	SEG113	2464.5	748.1	17.5	115
366	SEG114	2433.5	748.1	17.5	115
367	SEG115	2402.5	748.1	17.5	115
368	SEG116	2371.5	748.1	17.5	115
369	SEG117	2340.5	748.1	17.5	115
370	SEG118	2309.5	748.1	17.5	115
371	SEG119	2278.5	748.1	17.5	115
372	SEG120	2247.5	748.1	17.5	115
373	SEG121	2216.5	748.1	17.5	115
374	SEG122	2185.5	748.1	17.5	115
375	SEG123	2154.5	748.1	17.5	115
376	SEG124	2123.5	748.1	17.5	115
377	SEG125	2092.5	748.1	17.5	115
378	SEG126	2061.5	748.1	17.5	115
379	SEG127	2030.5	748.1	17.5	115
380	SEG128	1999.5	748.1	17.5	115
381	SEG129	1968.5	748.1	17.5	115
382	SEG130	1937.5	748.1	17.5	115
383	SEG131	1906.5	748.1	17.5	115
384	SEG132	1875.5	748.1	17.5	115
385	SEG133	1844.5	748.1	17.5	115
386	SEG134	1813.5	748.1	17.5	115
387	SEG135	1782.5	748.1	17.5	115
388	SEG136	1751.5	748.1	17.5	115
389	SEG137	1720.5	748.1	17.5	115
390	SEG138	1689.5	748.1	17.5	115
391	SEG139	1658.5	748.1	17.5	115
392	SEG140	1627.5	748.1	17.5	115
393	SEG141	1596.5	748.1	17.5	115
394	SEG142	1565.5	748.1	17.5	115
395	SEG143	1534.5	748.1	17.5	115

#	Pad	X	Y	W	H
396	SEG144	1503.5	748.1	17.5	115
397	SEG145	1472.5	748.1	17.5	115
398	SEG146	1441.5	748.1	17.5	115
399	SEG147	1410.5	748.1	17.5	115
400	SEG148	1379.5	748.1	17.5	115
401	SEG149	1348.5	748.1	17.5	115
402	SEG150	1317.5	748.1	17.5	115
403	SEG151	1286.5	748.1	17.5	115
404	SEG152	1255.5	748.1	17.5	115
405	SEG153	1224.5	748.1	17.5	115
406	SEG154	1193.5	748.1	17.5	115
407	SEG155	1162.5	748.1	17.5	115
408	SEG156	1131.5	748.1	17.5	115
409	SEG157	1100.5	748.1	17.5	115
410	SEG158	1069.5	748.1	17.5	115
411	SEG159	1038.5	748.1	17.5	115
412	SEG160	1007.5	748.1	17.5	115
413	SEG161	976.5	748.1	17.5	115
414	SEG162	945.5	748.1	17.5	115
415	SEG163	914.5	748.1	17.5	115
416	SEG164	883.5	748.1	17.5	115
417	SEG165	852.5	748.1	17.5	115
418	SEG166	821.5	748.1	17.5	115
419	SEG167	790.5	748.1	17.5	115
420	SEG168	759.5	748.1	17.5	115
421	SEG169	728.5	748.1	17.5	115
422	SEG170	697.5	748.1	17.5	115
423	SEG171	666.5	748.1	17.5	115
424	SEG172	635.5	748.1	17.5	115
425	SEG173	604.5	748.1	17.5	115
426	SEG174	573.5	748.1	17.5	115
427	SEG175	542.5	748.1	17.5	115
428	SEG176	511.5	748.1	17.5	115
429	SEG177	480.5	748.1	17.5	115
430	SEG178	449.5	748.1	17.5	115
431	SEG179	418.5	748.1	17.5	115
432	SEG180	387.5	748.1	17.5	115
433	SEG181	356.5	748.1	17.5	115
434	SEG182	325.5	748.1	17.5	115
435	SEG183	294.5	748.1	17.5	115
436	SEG184	263.5	748.1	17.5	115
437	SEG185	232.5	748.1	17.5	115
438	SEG186	201.5	748.1	17.5	115
439	SEG187	170.5	748.1	17.5	115
440	SEG188	139.5	748.1	17.5	115
441	SEG189	108.5	748.1	17.5	115
442	SEG190	77.5	748.1	17.5	115
443	SEG191	46.5	748.1	17.5	115
444	SEG192	15.5	748.1	17.5	115
445	SEG193	-15.5	748.1	17.5	115
446	SEG194	-46.5	748.1	17.5	115
447	SEG195	-77.5	748.1	17.5	115
448	SEG196	-108.5	748.1	17.5	115
449	SEG197	-139.5	748.1	17.5	115
450	SEG198	-170.5	748.1	17.5	115
451	SEG199	-201.5	748.1	17.5	115
452	SEG200	-232.5	748.1	17.5	115

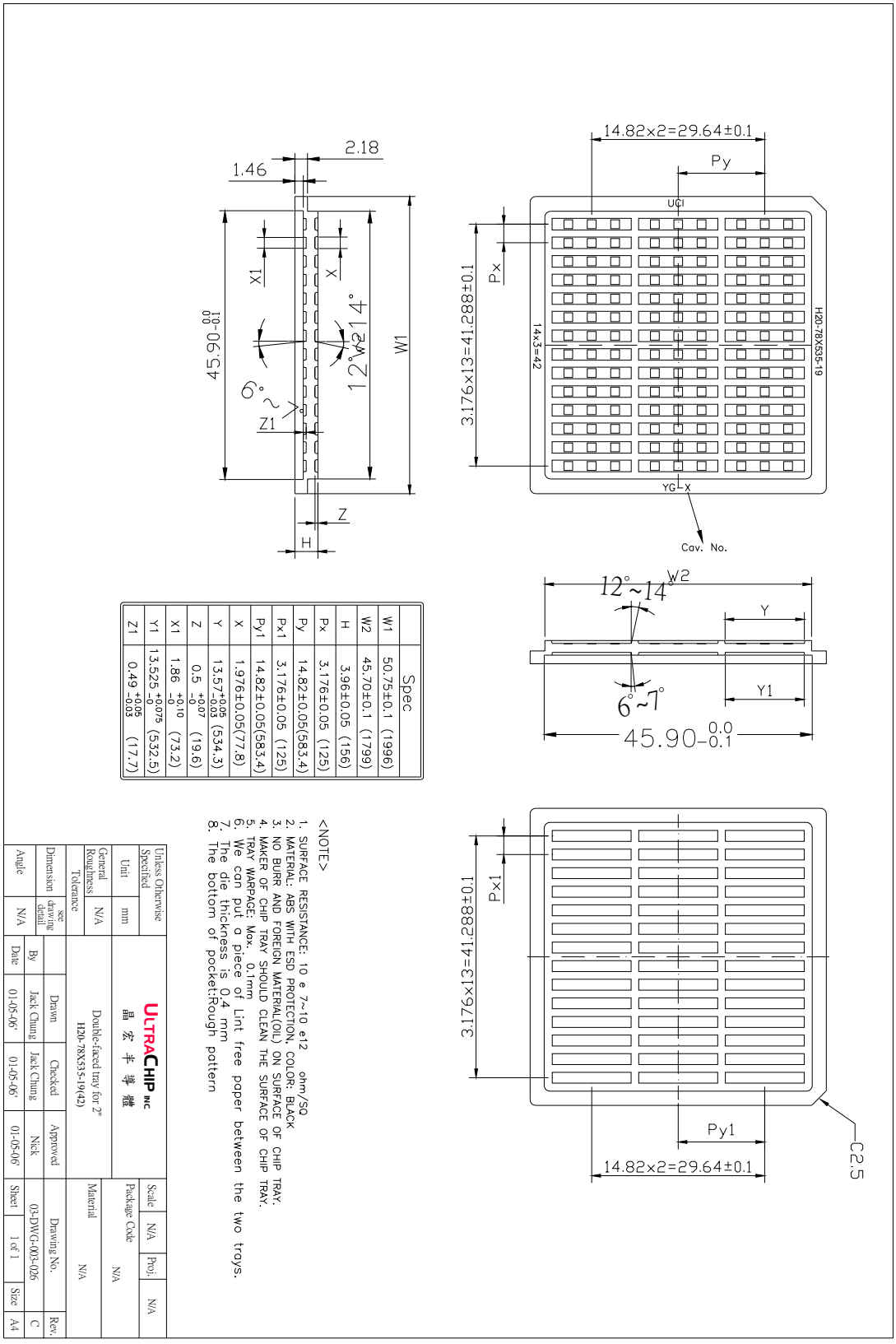
#	Pad	X	Y	W	H
453	SEG201	-263.5	748.1	17.5	115
454	SEG202	-294.5	748.1	17.5	115
455	SEG203	-325.5	748.1	17.5	115
456	SEG204	-356.5	748.1	17.5	115
457	SEG205	-387.5	748.1	17.5	115
458	SEG206	-418.5	748.1	17.5	115
459	SEG207	-449.5	748.1	17.5	115
460	SEG208	-480.5	748.1	17.5	115
461	SEG209	-511.5	748.1	17.5	115
462	SEG210	-542.5	748.1	17.5	115
463	SEG211	-573.5	748.1	17.5	115
464	SEG212	-604.5	748.1	17.5	115
465	SEG213	-635.5	748.1	17.5	115
466	SEG214	-666.5	748.1	17.5	115
467	SEG215	-697.5	748.1	17.5	115
468	SEG216	-728.5	748.1	17.5	115
469	SEG217	-759.5	748.1	17.5	115
470	SEG218	-790.5	748.1	17.5	115
471	SEG219	-821.5	748.1	17.5	115
472	SEG220	-852.5	748.1	17.5	115
473	SEG221	-883.5	748.1	17.5	115
474	SEG222	-914.5	748.1	17.5	115
475	SEG223	-945.5	748.1	17.5	115
476	SEG224	-976.5	748.1	17.5	115
477	SEG225	-1007.5	748.1	17.5	115
478	SEG226	-1038.5	748.1	17.5	115
479	SEG227	-1069.5	748.1	17.5	115
480	SEG228	-1100.5	748.1	17.5	115
481	SEG229	-1131.5	748.1	17.5	115
482	SEG230	-1162.5	748.1	17.5	115
483	SEG231	-1193.5	748.1	17.5	115
484	SEG232	-1224.5	748.1	17.5	115
485	SEG233	-1255.5	748.1	17.5	115
486	SEG234	-1286.5	748.1	17.5	115
487	SEG235	-1317.5	748.1	17.5	115
488	SEG236	-1348.5	748.1	17.5	115
489	SEG237	-1379.5	748.1	17.5	115
490	SEG238	-1410.5	748.1	17.5	115
491	SEG239	-1441.5	748.1	17.5	115
492	SEG240	-1472.5	748.1	17.5	115
493	SEG241	-1503.5	748.1	17.5	115
494	SEG242	-1534.5	748.1	17.5	115
495	SEG243	-1565.5	748.1	17.5	115
496	SEG244	-1596.5	748.1	17.5	115
497	SEG245	-1627.5	748.1	17.5	115
498	SEG246	-1658.5	748.1	17.5	115
499	SEG247	-1689.5	748.1	17.5	115
500	SEG248	-1720.5	748.1	17.5	115
501	SEG249	-1751.5	748.1	17.5	115
502	SEG250	-1782.5	748.1	17.5	115
503	SEG251	-1813.5	748.1	17.5	115
504	SEG252	-1844.5	748.1	17.5	115
505	SEG253	-1875.5	748.1	17.5	115
506	SEG254	-1906.5	748.1	17.5	115
507	SEG255	-1937.5	748.1	17.5	115
508	SEG256	-1968.5	748.1	17.5	115
509	SEG257	-1999.5	748.1	17.5	115

#	Pad	X	Y	W	H
510	SEG258	-2030.5	748.1	17.5	115
511	SEG259	-2061.5	748.1	17.5	115
512	SEG260	-2092.5	748.1	17.5	115
513	SEG261	-2123.5	748.1	17.5	115
514	SEG262	-2154.5	748.1	17.5	115
515	SEG263	-2185.5	748.1	17.5	115
516	SEG264	-2216.5	748.1	17.5	115
517	SEG265	-2247.5	748.1	17.5	115
518	SEG266	-2278.5	748.1	17.5	115
519	SEG267	-2309.5	748.1	17.5	115
520	SEG268	-2340.5	748.1	17.5	115
521	SEG269	-2371.5	748.1	17.5	115
522	SEG270	-2402.5	748.1	17.5	115
523	SEG271	-2433.5	748.1	17.5	115
524	SEG272	-2464.5	748.1	17.5	115
525	SEG273	-2495.5	748.1	17.5	115
526	SEG274	-2526.5	748.1	17.5	115
527	SEG275	-2557.5	748.1	17.5	115
528	SEG276	-2588.5	748.1	17.5	115
529	SEG277	-2619.5	748.1	17.5	115
530	SEG278	-2650.5	748.1	17.5	115
531	SEG279	-2681.5	748.1	17.5	115
532	SEG280	-2712.5	748.1	17.5	115
533	SEG281	-2743.5	748.1	17.5	115
534	SEG282	-2774.5	748.1	17.5	115
535	SEG283	-2805.5	748.1	17.5	115
536	SEG284	-2836.5	748.1	17.5	115
537	SEG285	-2867.5	748.1	17.5	115
538	SEG286	-2898.5	748.1	17.5	115
539	SEG287	-2929.5	748.1	17.5	115
540	SEG288	-2960.5	748.1	17.5	115
541	SEG289	-2991.5	748.1	17.5	115
542	SEG290	-3022.5	748.1	17.5	115
543	SEG291	-3053.5	748.1	17.5	115
544	SEG292	-3084.5	748.1	17.5	115
545	SEG293	-3115.5	748.1	17.5	115
546	SEG294	-3146.5	748.1	17.5	115
547	SEG295	-3177.5	748.1	17.5	115
548	SEG296	-3208.5	748.1	17.5	115
549	SEG297	-3239.5	748.1	17.5	115
550	SEG298	-3270.5	748.1	17.5	115
551	SEG299	-3301.5	748.1	17.5	115
552	SEG300	-3332.5	748.1	17.5	115
553	SEG301	-3363.5	748.1	17.5	115
554	SEG302	-3394.5	748.1	17.5	115
555	SEG303	-3425.5	748.1	17.5	115
556	SEG304	-3456.5	748.1	17.5	115
557	SEG305	-3487.5	748.1	17.5	115
558	SEG306	-3518.5	748.1	17.5	115
559	SEG307	-3549.5	748.1	17.5	115
560	SEG308	-3580.5	748.1	17.5	115
561	SEG309	-3611.5	748.1	17.5	115
562	SEG310	-3642.5	748.1	17.5	115
563	SEG311	-3673.5	748.1	17.5	115
564	SEG312	-3704.5	748.1	17.5	115
565	SEG313	-3735.5	748.1	17.5	115
566	SEG314	-3766.5	748.1	17.5	115

#	Pad	X	Y	W	H
567	SEG315	-3797.5	748.1	17.5	115
568	SEG316	-3828.5	748.1	17.5	115
569	SEG317	-3859.5	748.1	17.5	115
570	SEG318	-3890.5	748.1	17.5	115
571	SEG319	-3921.5	748.1	17.5	115
572	SEG320	-3952.5	748.1	17.5	115
573	SEG321	-3983.5	748.1	17.5	115
574	SEG322	-4014.5	748.1	17.5	115
575	SEG323	-4045.5	748.1	17.5	115
576	SEG324	-4076.5	748.1	17.5	115
577	SEG325	-4107.5	748.1	17.5	115
578	SEG326	-4138.5	748.1	17.5	115
579	SEG327	-4169.5	748.1	17.5	115
580	SEG328	-4200.5	748.1	17.5	115
581	SEG329	-4231.5	748.1	17.5	115
582	SEG330	-4262.5	748.1	17.5	115
583	SEG331	-4293.5	748.1	17.5	115
584	SEG332	-4324.5	748.1	17.5	115
585	SEG333	-4355.5	748.1	17.5	115
586	SEG334	-4386.5	748.1	17.5	115
587	SEG335	-4417.5	748.1	17.5	115
588	SEG336	-4448.5	748.1	17.5	115
589	SEG337	-4479.5	748.1	17.5	115
590	SEG338	-4510.5	748.1	17.5	115
591	SEG339	-4541.5	748.1	17.5	115
592	SEG340	-4572.5	748.1	17.5	115
593	SEG341	-4603.5	748.1	17.5	115
594	SEG342	-4634.5	748.1	17.5	115
595	SEG343	-4665.5	748.1	17.5	115
596	SEG344	-4696.5	748.1	17.5	115
597	SEG345	-4727.5	748.1	17.5	115
598	SEG346	-4758.5	748.1	17.5	115
599	SEG347	-4789.5	748.1	17.5	115
600	SEG348	-4820.5	748.1	17.5	115
601	SEG349	-4851.5	748.1	17.5	115
602	SEG350	-4882.5	748.1	17.5	115
603	SEG351	-4913.5	748.1	17.5	115
604	SEG352	-4944.5	748.1	17.5	115
605	SEG353	-4975.5	748.1	17.5	115
606	SEG354	-5006.5	748.1	17.5	115
607	SEG355	-5037.5	748.1	17.5	115
608	SEG356	-5068.5	748.1	17.5	115
609	SEG357	-5099.5	748.1	17.5	115
610	SEG358	-5130.5	748.1	17.5	115
611	SEG359	-5161.5	748.1	17.5	115
612	SEG360	-5192.5	748.1	17.5	115
613	SEG361	-5223.5	748.1	17.5	115
614	SEG362	-5254.5	748.1	17.5	115
615	SEG363	-5285.5	748.1	17.5	115
616	SEG364	-5316.5	748.1	17.5	115
617	SEG365	-5347.5	748.1	17.5	115
618	SEG366	-5378.5	748.1	17.5	115
619	SEG367	-5409.5	748.1	17.5	115
620	SEG368	-5440.5	748.1	17.5	115
621	SEG369	-5471.5	748.1	17.5	115
622	SEG370	-5502.5	748.1	17.5	115
623	SEG371	-5533.5	748.1	17.5	115
624	SEG372	-5564.5	748.1	17.5	115
625	SEG373	-5595.5	748.1	17.5	115
626	SEG374	-5626.5	748.1	17.5	115
627	SEG375	-5657.5	748.1	17.5	115
628	SEG376	-5688.5	748.1	17.5	115
629	SEG377	-5719.5	748.1	17.5	115
630	SEG378	-5750.5	748.1	17.5	115
631	SEG379	-5781.5	748.1	17.5	115
632	SEG380	-5812.5	748.1	17.5	115
633	SEG381	-5843.5	748.1	17.5	115
634	SEG382	-5874.5	748.1	17.5	115
635	SEG383	-5905.5	748.1	17.5	115
636	SEG384	-5936.5	748.1	17.5	115
637	COM2	-5967.5	748.1	17.5	115
638	COM4	-5998.5	748.1	17.5	115
639	COM6	-6029.5	748.1	17.5	115
640	COM8	-6060.5	748.1	17.5	115
641	COM10	-6091.5	748.1	17.5	115
642	COM12	-6122.5	748.1	17.5	115
643	COM14	-6153.5	748.1	17.5	115
644	COM16	-6184.5	748.1	17.5	115
645	COM18	-6215.5	748.1	17.5	115
646	COM20	-6246.5	748.1	17.5	115
647	COM22	-6277.5	748.1	17.5	115
648	COM24	-6308.5	748.1	17.5	115
649	COM26	-6339.5	748.1	17.5	115
650	COM28	-6370.5	748.1	17.5	115
651	COM30	-6401.5	748.1	17.5	115
652	COM32	-6432.5	748.1	17.5	115
653	COM34	-6463.5	748.1	17.5	115

(The values of the x-coordinate and the y-coordinate in the table are after rounded.)

TRAY INFORMATION



	Spec
W1	50.75±0.1 (1996)
W2	45.70±0.1 (1799)
H	3.96±0.05 (156)
Px	3.176±0.05 (125)
Py	14.82±0.05(583.4)
Px1	3.176±0.05 (125)
Py1	14.82±0.05(583.4)
X	1.976±0.05(77.8)
Y	13.57 +0.05 -0.03 (534.3)
Z	0.5 +0.07 -0 (19.6)
X1	1.86 +0.10 -0 (73.2)
Y1	13.525 +0.075 -0 (532.5)
Z1	0.49 +0.05 -0.03 (17.7)

<NOTE>
1. SURFACE RESISTANCE: 10 e 7~10 e12 ohm/SQ
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: BLACK
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: Max. 0.1mm
6. We can put a piece of Lint free paper between the two trays.
7. The die thickness is 0.4 mm
8. The bottom of pocket:Rough pattern

Unless Otherwise Specified		ULTRACHIP INC 晶宏半導體						Scale	N/A	Proj	N/A
Unit	mm							Package Code	N/A		
General Roughness	N/A	Double-faced tray for 2" H20-78X535-19(42)						Material	N/A		
Tolerance											
Dimension	see drawing detail		Drawn	Checked	Approved			Drawing No.			Rev.
Angle	N/A	By	Jack Chung	Jack Chung	Nick			03-DWG-003-026			C
		Date	01-05-06'	01-05-06'	01-05-06'			Sheet	1 of 1	Size	A4

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	First Release	Jun. 2, 2006
0.7	(1) Some ESD data are corrected. (Section "ESD Consideration", page 53)	Jun. 15, 2006
	(2) An I_{SB} entry is added for standby current. (Section "Specifications" – DC Characteristics, page 55)	
1.0	(1) LCD V_{OP} is adjusted: 6.4V~18V 6.15V~18V (Section "Feature Highlights", page 1)	Aug. 21, 2006
	(2) The recommended capacitor C_S is defined: 150~220nF / 25V. C_B is adjusted: 2.2μF/2V → 2.2μF/5V (Section "Pin Description", page 4: "Hi-V Generator Reference Circuit", page 31)	
	(3) "When Mux rate is under 33, …" → under 40 (Section "Command Description" – (29) Set Partial Display End, page 23)	
	(4) "… with $V_{DD2/3}$ ≥2.7V" → ≥2.8V (Section "LCD Voltage Setting" – Load Driving Strength for COG, page 29)	
	(5) V_{LCD} formula is updated. (Section "V_{LCD} Quick Reference", page 30)	
	(6) "Frame rate 231 Hz" → "Line rate 37.0 Klps" (Section "LCD Display Controls" – Clock & Timing Generator, page 32)	
	(7) The description of 64K color is updated. (Section "LCD Display Controls" – Input Color Formats, page 33)	
	(8) For S8uc interface, the description is updated. (Section "Host Interface" – Serial Interface, page 38)	
	(9) One paragraph on MTP-READ is removed. (Section "MTP NV Memory", page 47)	
	(10) V_{LCD} for Program / Erase / Read are adjusted: 12.3V / 12.3V / 6.4V → 12.15V / 12.15V / 6.15V (11) External input for Program, TST4, is adjusted : 8.5V → 10V (12) A note on $V_{DD2/3}$ is added. (Section "MTP Operation for LCM Makers", Pp 48~51)	
	(13) Some data are corrected. (Section "ESD Consideration", page 53)	
	(14) The typical value of COM output impedance, $R_{ON(COM)}$: 750 → 850 Ω The typical value of SEG output impedance, $R_{ON(SEG)}$: 750 → 950 Ω The condition for $R_{ON(COM)}$ & $R_{ON(SEG)}$: V_{LCD} = 15V → 16.5V (Section "Specifications" – DC Characteristics, page 55)	
	(15) The maximum power consumption present. (Section "Power Consumption", page 55)	
	(16) Some more AC timings are provided. (Section "AC Characteristics", Pp 56~60)	
1.1	(1) The S9 mode is added. (Overall, pages 1, 4, 5, 6, 36, 38, 42, 47, 62)	Oct. 2, 2006
1.2	(1) The V_{LCD} Generation sub-section is enriched by adding a diagram. (Section "V_{LCD} Voltage Setting", page 32)	Mar. 25, 2008
1.21	(1) The description of the Read Data command is enriched. (Section "Command Description" – (2) Read Data, page 9)	Aug. 7, 2008
	(2) The description on Reset is updated. (Section "Reset & Power Management", Pp 49~51)	

Revision	Contents	Date of Rev.
1.3	V_{DD}, $V_{DD2/3}$ (Max.) : 3.3V → 3.465V (Section "Specifications" – DC Characteristics, page 59)	Mar. 31, 2009