Sequential Circuit Analysis

Circuit Diagram to State Diagram State Diagram to Circuit Diagram Counters Application of Counters



What is sequential logic

- Sequential circuit has additional dimension which is time
- Combinational logic only depends on current input
- Sequential circuit output depends on previous input other than current input
- More powerful than combination logic
- Able to model condition which can't be modeled by combinational logic



Circuit Diagram to State Diagram

Example 1: Draw the state diagram for the given circuit

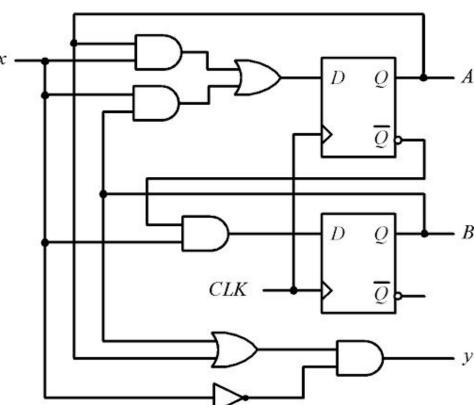
Sequential circuit using D flip flop

Present Next

States: States:

A and B A+ and B+ **Input**: **Output**:

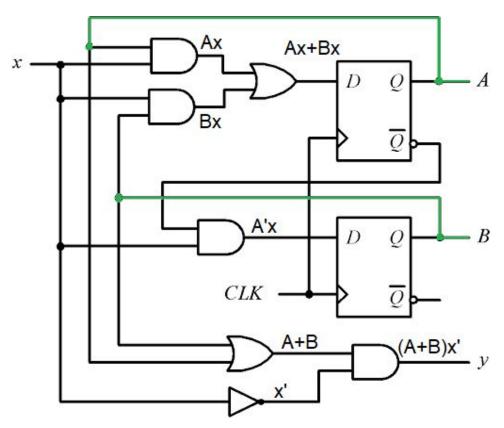
DA, DB, x





Example 1: Draw the state diagram for the given circuit

1. Find out the input equations of the flip flop and the output equation





Example 1: Draw the state diagram for the given circuit

2. Construct the state table according to the flip flop input and output equations

When A=0, B=0, x=0, When A=0, B=0, x=1, DA = 0.0 + 0.0 = 0DA = 0.1 + 0.1 = 0DB = 0'.0 = 0DB = 0'.1 = 1y = (0+0).0' = 0y = (0+0).1' = 0

Α	В	X	DA	DΒ	У
0	0	0	0	0	0
0	0_	_1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

 $D \Lambda$

DD



Example 1: Draw the state diagram for the given circuit

3. Find out the next states from the flip flop input values

D Flip-flop Truth table

D	Q
0	0
1	1



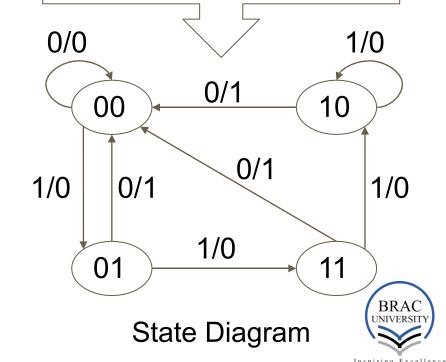
-	ı		Α	_	Α	+
•	•	L)	М	_	М	т

	Α	В	X	DA	DB	У	A+	B+
•	0	0	0	0	0	0	0	0
	0	0	1	0	1	0	0	1
	0	1	0	0	0	1	0	0
	0	1	1	1	1	0	1	1
	1	0	0	0	0	1	0	0
	1	0	1	1	0	0	1	0
	1	1	0	0	0	1	0	0
	1	1	1	1	0	0	1	0

Example 1: Draw the state diagram for the given circuit

Α	В	Х	Α+	B+	У
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

4. Draw the state diagram from the state table



Example 2: Draw the state diagram for the given circuit

Sequential circuit using JK flip flop

Sequential circuit using JK flip flop

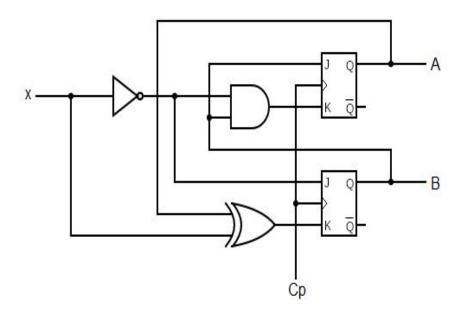
Present Next

States: States:

A and B A+ and B+

Input:

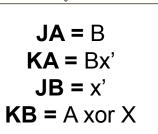
JA, KA, JB, KB, x

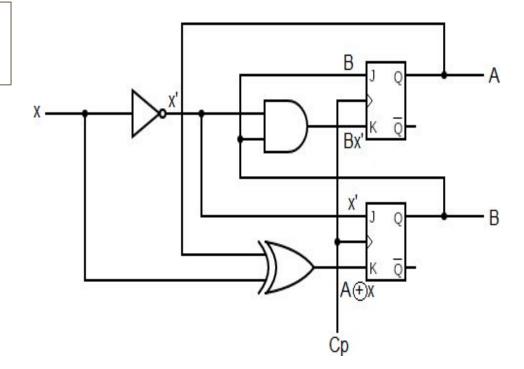




Example 2: Draw the state diagram for the given circuit

1. Find out the input equations of the flip flop and the output equation







Example 2: Draw the state diagram for the given circuit В KA JB

0

0

0

0

2. Construct the state table according to the flip flop input and output equations

When A=0, B=0, x=0,

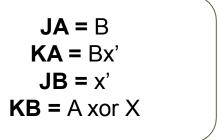
JA = 0

KA = 0.0' = 0

KB = 0 xor 0 = 0

JB = 0' = 1





KA = 0.1' = 0

KB = 0 xor 0 = 0

JB = 1' = 0

or X	
When A=0, B=0, x=1, JA = 0	
$V\Lambda = 0.4' = 0$	

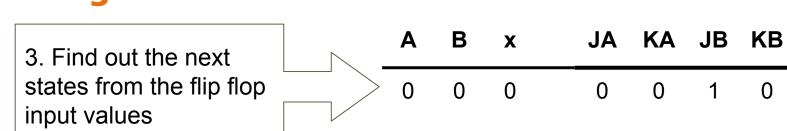
0

	1	1	U
1	0	0	1
0	0	1	1
0	0	0	0
1	1	1	1
1	0	0	0

KB



Example 2: Draw the state diagram for the given circuit



JK Flip-flop Truth table

J	K	Q
0	0	Memory/ No change
0	1	0
1	0	1
1	1	Toggle

0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
4	4	4	4	0	•	0	4	4

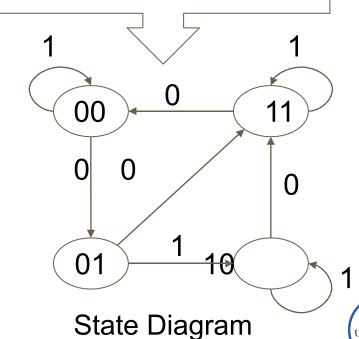
A+ B+

0

Example 2: Draw the state diagram for the given circuit

A	В	X	A	+ B+	
0	0	0	C) 1	
0	0	1	C	0	
0	1	0	1	1	
0	1	1	1	0	
1	0	0	1	1	
1	0	1	1	0	
1	1	0	C	0	
1	1	1	1	1	

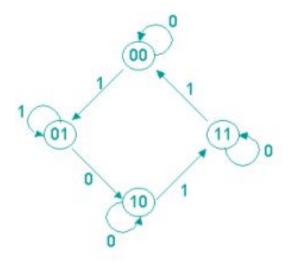
4. Draw the state diagram from the state table



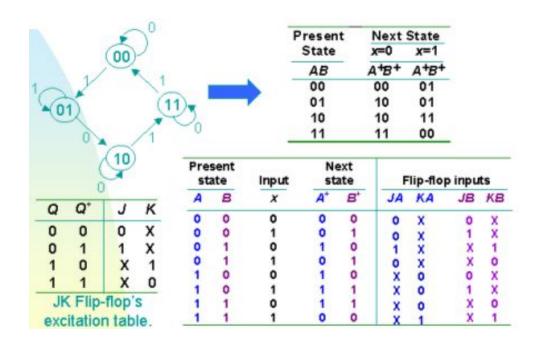
BRAC

State Diagram to Circuit Diagram

Given state diagram as follows, get the sequential circuit using JK flip-flop

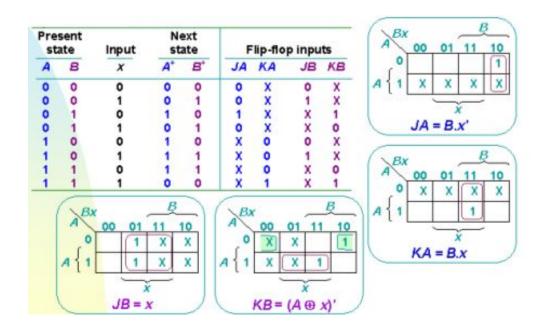


State/excitation table using JK flip-flop



Note: Step 1: Build state table Step 2: Find no. of Flip-Flop (i.e. 2^m states means m flip-flips) Step 3: Build Excitation table Step 4: Use K-map to find input functions Step 5: Design logic diagram

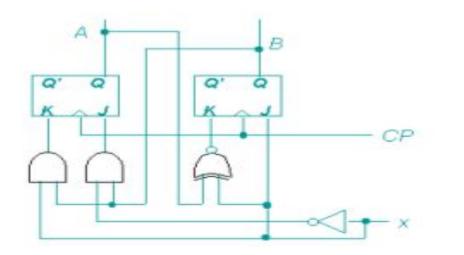
From state table, get input flip-flop function



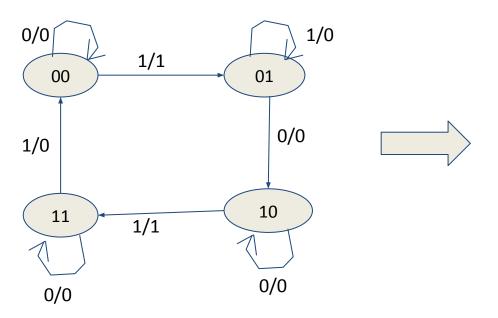
Input flip-flop function

$$JA = B.x'$$
 $JB = x$ $KB = (A \oplus x)'$

Logic Diagram



Design, using D flip-flop, circuit is based on state table below. (Exercise: How if using JK flip-flop)

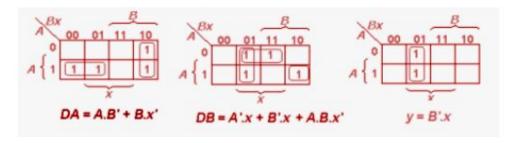


Present state		Input		ate	Output
A	В	X	A^{+}	B ⁺	У
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

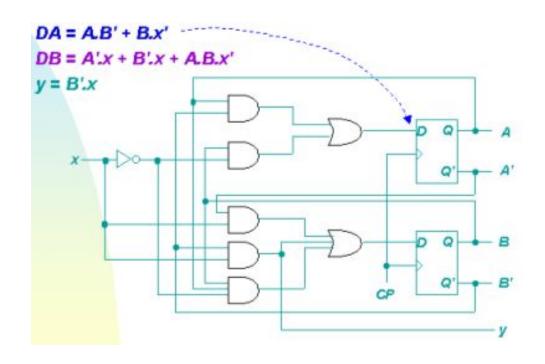
Determine input expression for flip-flop and y output

Α	В	x	A+	B+	у	DA	DB
0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1
0	1	0	1	0	0	1	0
0	1	1	0	1	0	0	1
1	0	0	1	0	0	1	0
1	0	1	1	1	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	0	0

0	0
-	U
1	1
0	0
1	1
	1 0 1 ip-flo



From expression built, draw logic diagram

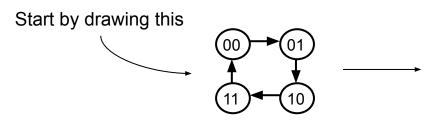


Introduction: Counters

- Counters are circuits that cycle through a specified number of states.
- Two types of counters:
 - synchronous (parallel) counters
 - asynchronous (ripple) counters
- Ripple counters allow some flip-flop outputs to be used as a source of clock for other flip-flops.
- Synchronous counters apply the same clock to all flip-flops.
- We will cover only synchronous this time

- Synchronous (parallel) counters: the flip-flops are clocked at the same time by a common clock pulse.
- We can design these counters using the sequential logic design process.
- Example: 2-bit synchronous binary counter (using T flip-flops, or JK flip-flops with identical J,K inputs).

Question: Design a 2-bit synchronous binary counter (using T flip-flops).



	sent ate		ext ate	-	-flop uts
A ₁	A_0	A_1^{\dagger}	A_0^{\dagger}	<i>TA</i> ₁	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Q _n	Q _{n+1}	Т
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of Tflip flop

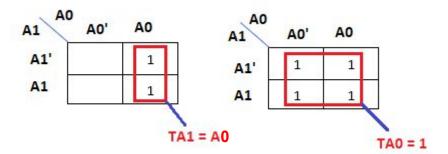
	sent ate	N st	Flip-flop inputs		
A ₁	A_0	A_1^{\dagger}	$A_1^+ A_0^+$		TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Next, find out the equations for the flip-flop inputs.

$$TA_1 = A_1'A_0 + A_1A_0 = A_0(A_1'+A_1) = A_0$$

 $TA_0 = 1$

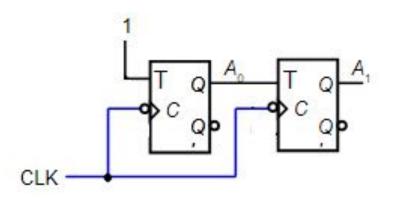
FYI, these can also be calculated using K-Maps



$$TA_1 = A_1'A_0 + A_1A_0 = A_0(A_1'+A_1) = A_0$$

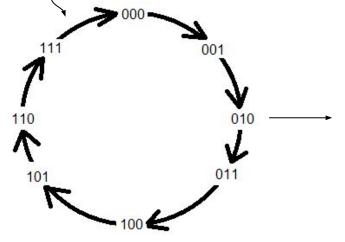
 $TA_0 = 1$

Finally draw the circuit diagram



Start by drawing this

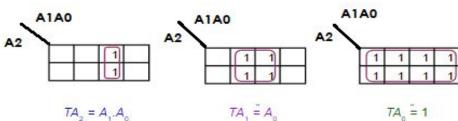
Question: Design a 3-bit synchronous binary counter (using T).



	rese state			Next state			Flip-flop inputs			
A ₂	A_1	A_0	A_2^+	A_1^{\dagger}	A_0^{\dagger}	TA ₂	TA_1	TA_0		
0	0	0	0	0	1	0	0	1		
0	0	1	0	1	0	0	1	1		
0	1	0	0	1	1	0	0	1		
0	1	1	1	0	0	1	1	1		
1	0	0	1	0	1	0	0	1		
1	0	1	1	1	0	0	1	1		
1	1	0	1	1	1	0	0	1		
1	1	1	0	0	0	1	1	1		

Q _n	Q _{n+1}	Т
0	0	0
0	1	1
1	0	1
1	1	0

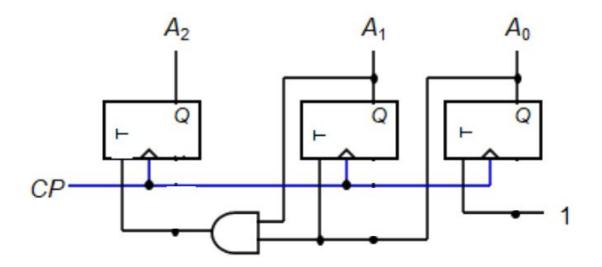
Excitation table of Tflip flop



FYI, these can also be calculated using Boolean simplifications

Draw the circuit diagram

$$TA_2 = A_1.A_0$$
 $TA_1 = A_0$ $TA_0 = 1$



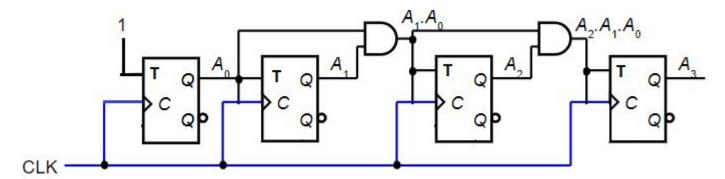
Self-Study

4 bit synchronous up counter

Equations and diagram will look like the following:

$$TA_3 = A_2 \cdot A_1 \cdot A_0$$

 $TA_2 = A_1 \cdot A_0$
 $TA_1 = A_0$
 $TA_0 = 1$

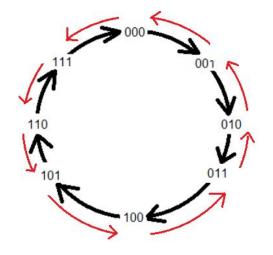


Up/Down Synchronous Counters

- Up/down synchronous counter: a bidirectional counter that is capable of counting either up or down.
- An input (control) line *Up/Down* (or simply *Up*) specifies the direction of counting.
 - ❖ $Up/Down = 0 \rightarrow Count upward$
 - ❖ $Up/Down = 1 \rightarrow Count downward$

U/D	Pres	Present states			xt Sta	tes	Flipt	flop in	puts
М	Q ₂	Q ₁	Q ₀	Q ₂ +	Q ₁ +	Q ₀ +	TQ ₂	TQ ₁	TQ
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

3 bit Synchronous Up/Down Counter

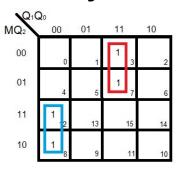


Q _n	Q _{n+1}	Т
0	0	0
0	1	1
1	0	1
1	1	0

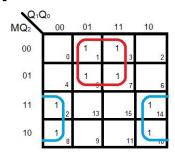
Excitation table of Tflip flop

U/D	Pres	Present states			xt Sta	tes	Flip	flop in	puts
M	Q ₂	Q ₁	Q ₀	Q ₂ +	Q ₁ +	Q ₀ +	TQ ₂	TQ ₁	TQ ₀
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

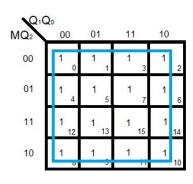
3 bit Synchronous Up/Down Counter



$$\mathsf{TQ}_2 = \mathsf{M'Q}_1 \mathsf{Q}_0 + \mathsf{MQ}_1' \mathsf{Q}_0'$$



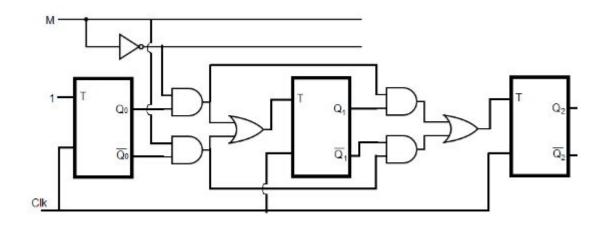
$$TQ_1 = M'Q_0 + MQ_0'$$



$$TQ_0 = 1$$

3 bit Up/Down Synchronous Counter

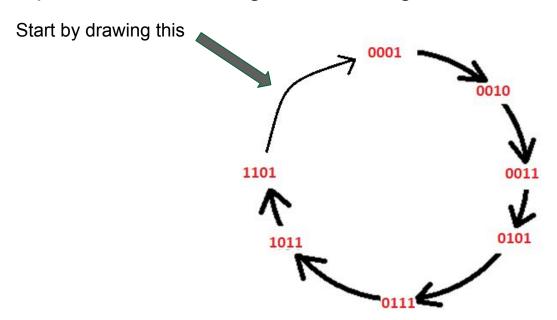
Draw the circuit diagram (The number of present state will be equal to the number of flip-flops in the circuit)



Practice Problem using Counters

PRACTICE PROBLEM - 1

Implement the following counter using T FF: 1->2->3->5->7->11->13->1



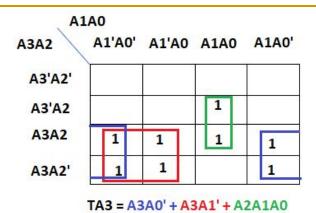
Р	resen	t state	es		Next	States	8	F	Flip-flop inputs			
A ₃	A ₂	A ₁	A ₀	A3+	A ₂ +	A ₁ +	A ₀ +	TA ₃	TA ₂	TA ₁	TA	
0	0	0	0	0	0	0	1	0	0	0	1	
0	0	0	1	0	0	1	0	0	0	1	1	
0	0	1	0	0	0	1	1	0	0	0	1	
0	0	1	1	0	1	0	1	0	1	1	0	
0	1	0	0	0	0	0	1	0	1	0	1	
0	1	0	1	0	1	1	1	0	0	1	0	
0	1	1	0	0	0	0	1	0	1	1	1	
0	1	1	1	1	0	1	1	1	1	0	0	
1	0	0	0	0	0	0	1	1	0	0	1	
1	0	0	1	0	0	0	1	1	0	0	0	
1	0	1	0	0	0	0	1	1	0	1	1	
1	0	1	1	1	1	0	1	0	1	1	0	
1	1	0	0	0	0	0	1	1	1	0	1	
1	1	0	1	0	0	0	1	1	1	0	0	
1	1	1	0	0	0	0	1	1	1	1	1	
1	1	1	1	0	0	0	1	1	1	1	0	

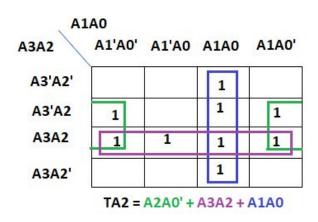
Q _n	Q _{n+1}	Т
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of Tflip flop

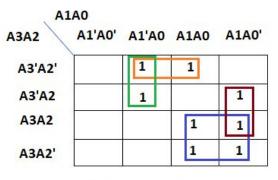
For present states not mentioned in the question, next state will be the INITIAL STATE [0001 in this question]. It's important to show the states that are not mentioned in the question. Otherwise, the circuit will stop working if any of those states show up.

Present states				Next States			Flip-flop inputs				
A ₃	A ₂	A ₁	A ₀	A3+	A ₂ +	A ₁ +	A ₀ +	TA ₃	TA ₂	TA ₁	TA
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	1	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	1	1	1	0	0	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	0	1	1	1	1	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	0	0	0	1	1	0	0	0
1	0	1	0	0	0	0	1	1	0	1	1
1	0	1	1	1	1	0	1	0	1	1	0
1	1	0	0	0	0	0	1	1	1	0	1
1	1	0	1	0	0	0	1	1	1	0	0
1	1	1	0	0	0	0	1	1	1	1	1
1	1	1	1	0	0	0	1	1	1	1	0

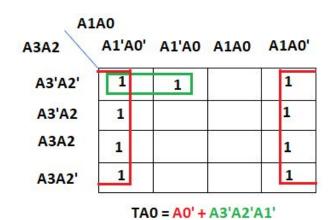




Present states				Next States			Flip-flop inputs				
A ₃	A ₂	A ₁	A ₀	A ₃ +	A ₂ +	A ₁ +	A ₀ +	TA ₃	TA ₂	TA ₁	TA
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	1	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	1	1	1	0	0	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	0	1	1	1	1	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	0	0	0	1	1	0	0	0
1	0	1	0	0	0	0	1	1	0	1	1
1	0	1	1	1	1	0	1	0	1	1	0
1	1	0	0	0	0	0	1	1	1	0	1
1	1	0	1	0	0	0	1	1	1	0	0
1	1	1	0	0	0	0	1	1	1	1	1
1	1	1	1	0	0	0	1	1	1	1	0



TA1 = A3'A1'A0 + A3'A2'A0 + A2A1A0' + A3A1

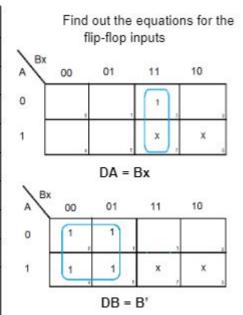


Draw the circuit yourself

PRACTICE PROBLEM - 2

Implement the following counter using D FF: Green->Yellow->Red->Yellow->Green Let's assume: Green = 00, Yellow = 01, Red = 10

Pre	sent s	tates	Next 5	States	Flip-flop inputs		
Α	В	х	Α+	B+	DA	DB	
0	0	0	0	1	0	1	
0	0	1	0	1	0	1	
0	1	0	0	0	0	0	
0	1	1	1	0	1	0	
1	0	0	0	1	0	1	
1	0	1	0	1	0	1	
1	1	0	х	x	х	х	
1	1	1	х	х	х	х	



Q _n	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table of D flip flop

Special Note: You may need to use more than 1 external input depending upon the question.

Draw the circuit diagram (The number of present state will be equal to the number of flip-flops in the circuit)

