BRAC UNIVERSITY
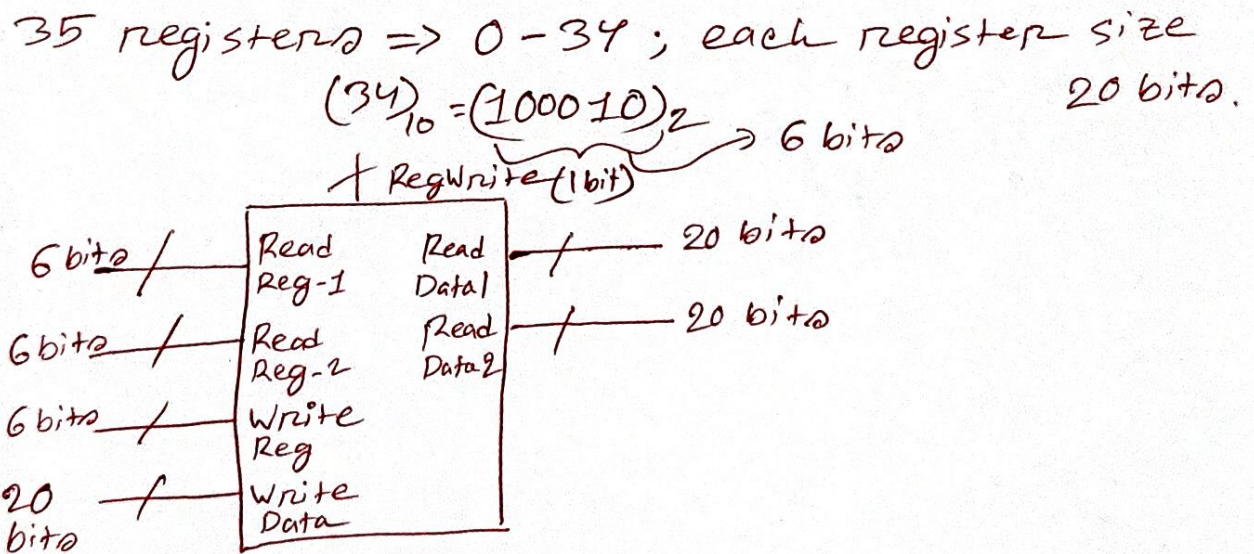## Department of Computer Science and Engineering

Examination: Surprise Test - 4
Duration: 10 minutes

Semester: Fall 2024
Full Marks: 05

CSE 340: Computer Architecture

| Name: *Solution* | ID: | Section: 06 |

1. In a special version of RISC-V there are 35 registers and each register can store 20 bits of data. Draw the block diagram of the register file mentioning all the input and output pins and their sizes. [2]

35 registers => 0 - 34 ; each register size 20 bits.

$(34)_{10} = (100010)_2$ → 6 bits

+ RegWrite (1bit)

- 6 bits → Read Reg-1
- 6 bits → Read Reg-2
- 6 bits → Write Reg
- 20 bits → Write Data
- Read Data1 → 20 bits
- Read Data2 → 20 bits

2. **Identify** the necessary resources or components from the list provided to construct the datapath for each of the following instructions. Just put a tick(✓) sign in the respective cells to show your selection.[3]

		PC	Instruction Memory	Data Memory	Register File	ALU	Immediate Generation Unit	Control Unit	ALU Control
i	ADD X21, X22, X23	✓	✓		✓	✓		✓	✓
ii	Slli X21, X22, 23	✓	✓		✓	✓	✓	✓	✓
iii	SB X21, 10(X22)	✓	✓	✓	✓	✓	✓	✓	✓