BRAC UNIVERSITY Department of Computer Science and Engineering

Examination: Quiz - 2 Duration: 25 minutes Semester: Fall 2024 Full Marks: 15

CSE 340: Computer Architecture

Name: Solution ID: Section:

 Write RISC-V assembly code that checks if the number stored in register X25 is divisible by 2 or not. If divisible then store 1 in register X26 otherwise store 0. [4]

2. In the RISC-V architecture, each instruction is encoded as a 32-bit binary sequence. In this standard format, the rs (source register) and rd (destination register) fields are typically 5 bits in size.

Suppose we are working with a prototype version of RISC-V that includes 56 registers. For this prototype version, what would be the required size of the rs or rd field? [3]

nswer: 56 registers = 0-55 =) 55 = 110111
6 bits
required size = 6 bits

3. Find the RISC-V code of the following machine Codes.

i. 0x00AA9B93

Answer: 0000 0000 1010 1010 1001 1011 1001 0011

Fo | Fall F3 | F2d | Opende > I type

S111 X23, X21, 10

ii. 0x08C2BAB3

Answer: 0000 1000 1100 0010 1011 1010 1011 0011

fumet 7 1202 1201 f3 12d opeode > Ptype

OR X21, X5, X12

4. What is the significance of the funct3 field in terms of LD instruction? [2]

Answer:

Machine unederstands the size of data transfer and the signedness of the transfer through funets field.

Format	Inst	Instruction		Opcode		Funct3		Funct7/Funct6	
	1	ADD		0110011		001		0000000	
\$ A		SUB		0110011		110		0000001	
R		AND	0110011		010		0000001		
		OR	011001		011		0000100		
		SLL	10	0110011 101		0000100			
		LD	0000011 000		N/A				
		LW	0000011			010		N/A	
	-	LH		0000011		011 N		N/A	
	1	LB		0000011		001		N/A	
I		ADDI		0010011		000		N/A	
		SLLI		0010011		001		000000	
		SRLI		0010011		1 010		000000	
		ORI		001001	1	011		N/A	
		SD		01000	11	000		N/A	
		SW	SW		11	001		N/A	
	S	SH	SH		11	11 010		N/A	
		SB		01000)11	011		N/A	