

BRAC UNIVERSITY
Department of Computer Science and Engineering

Examination: Quiz - 2
 Duration: 25 minutes

Semester: Fall 2024
 Full Marks: 15

CSE 340: Computer Architecture

Name: <u>Solution</u>	ID:	Section:
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1. Write RISC-V assembly code that checks if the number stored in register X25 is divisible by 2 or not. If divisible then store 1 in register X26 otherwise store 0. [4]

Answer:

```

ADDI X21, X0, 1
AND  X26, X25, X21
BEQ  X26, X0, If
ADDI X26, X0, 0
BEQ  X0, X0, Exit
    
```

```

If:
ADDI X26, X0, 1
Exit:
    
```

2. In the RISC-V architecture, each instruction is encoded as a 32-bit binary sequence. In this standard format, the rs (source register) and rd (destination register) fields are typically 5 bits in size.

Suppose we are working with a prototype version of RISC-V that includes 60 registers. For this prototype version, what would be the required size of the rs or rd field? [3]

Answer:

60 registers = 0-61 $\Rightarrow 61 = 111101$
 6 bits
 Required size = 6 bits

3. Find the RISC-V code of the following machine Codes.

i. 0x00AA9B93

[3]

Answer:

0000 0000 1010 1010 1001 1011 1001 0011
 imm rs1 f3 rd opcode \rightarrow I type

Sllr X23, X21, 10

to find the instruction

ii. 0x08C2BAB3

[3]

Answer:

0000 1000 1100 0010 1011 1010 1011 0011
 funct3 rs2 rs1 f3 rd opcode \rightarrow R type

OR X21, X5, X12




combination of

funct3 + funct2 to find the instruction

4. Although SLLI is an I-type instruction, the immediate field is restricted to 6 bits. Explain the reason for this constraint? [2]

Answer: Register size = 64 bits. If we left/right shift a number by 64 bits, the value becomes 0. So, at max we can shift 63 times. [Valid shifting]


 6 digits. | Hence, imm. field size is restricted to 6 bits.

Format	Instruction	Opcode	Funct3	Funct7/Funct6
✓ R	ADD	0110011	001	0000000
	SUB	0110011	110	0000001
	AND	0110011	010	0000001
	OR	0110011	011 ✓	0000100 ✓
	SLL	0110011	101	0000100 ✓
✓ I	LD	0000011	000	N/A
	LW	0000011	010	N/A
	LH	0000011	011	N/A
	LB	0000011	001	N/A
	ADDI	0010011	000	N/A
	SLLI	0010011	001 ✓	000000
	SRLI	0010011	010	000000
	ORI	0010011	011	N/A
S	SD	0100011	000	N/A
	SW	0100011	001	N/A
	SH	0100011	010	N/A
	SB	0100011	011	N/A