

Chapter 4 (The Processor)

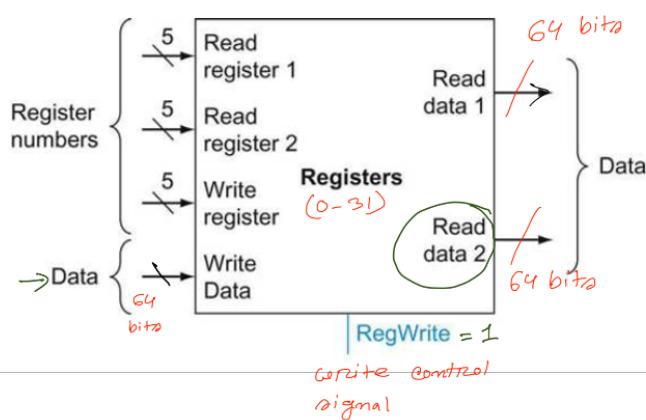
Question - 1:

Draw a diagram of the register file, clearly indicating all input and output pins.

a. Provide a detailed explanation of how the register file performs both read and write operations.

b. Explain why the size of the read/write register pin is 5 bits.

Register File



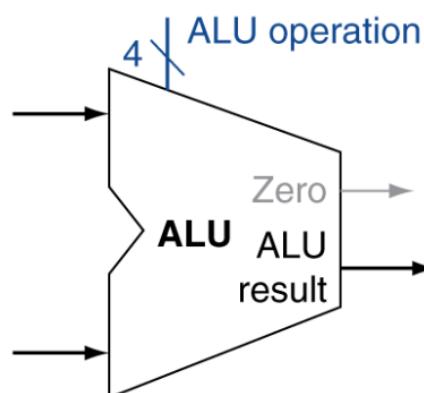
Hint: How many registers are there in Risc-V?

Question - 2:

Draw a diagram of the ALU, clearly indicating all input and output pins.

a. Explain the significance of the Zero pin in the ALU.

b. Describe how the ALU determines which operation to perform on the given inputs.



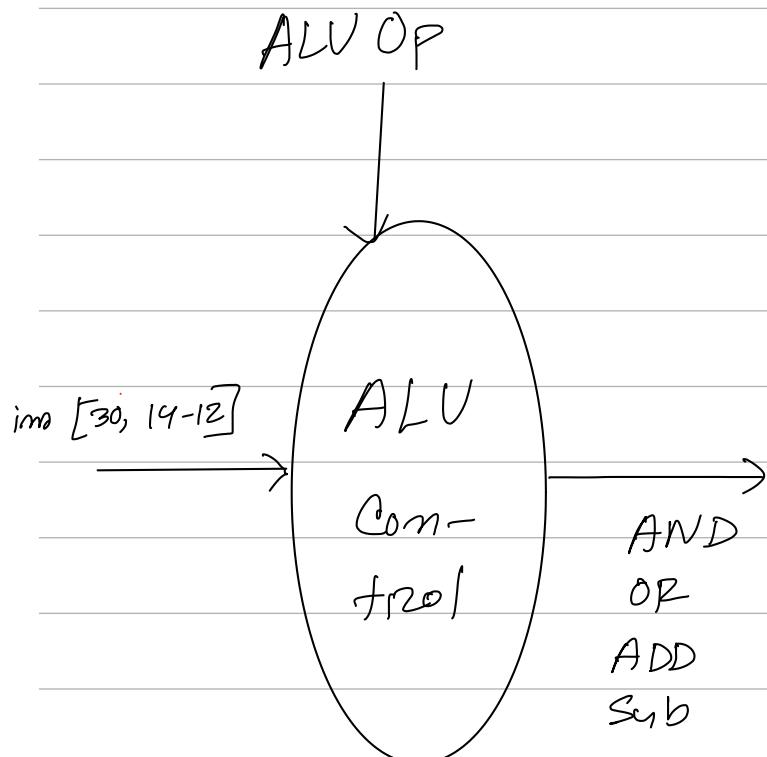
a) Hint: Branch instructions

b) Hint: Explore control & ALU Control units.

Question - 3:

Draw a diagram of the ALU Control, clearly indicating all input and output pins.

- Does the ALU control utilize Instruction bits 30 and 14-12 to generate the output for the LD instruction? Provide a justification for your answer.
- Identify the specific cases in which the ALU control utilizes Instruction bits 30 and 14-12 to generate the output. Additionally, explain why only these four bits (Instruction bits 30 and 14-12) are used in such cases.



a) No.

Hint for justification:

What does ALU do internally
of Load, Store and Addi instructions.

b) R-type.

Hint: Can you identify
which operation ALU should
by looking only looking at
the opcode?

If not, which other
fields are responsible?

Question - 4:

Identify the necessary resources or components from the list provided to construct the datapath for each of the following instructions.

PC	Instruction Memory	Data Memory	Register File	A L U	Immediate Generation Unit	Control Unit	ALU Control
1	2	3	4	5	6	7	8

i.	ADD X ₂₁ , X ₂₂ , X ₂₃
ii.	AND X ₂₁ , X ₂₂ , X ₂₃
iii.	OR X ₂₁ , X ₂₂ , X ₂₃
iv	ADDi X ₂₁ , X ₂₂ , X ₂₃
v.	LD X ₂₁ , 22(X ₂₁)
vi.	SD X ₂₁ , 22(X ₂₁)
vii	BEQ X ₂₁ , X ₂₂ , End

1, 2, 4, 5, 7, 8

} try yourself.

1, 2, 4, 5, 6, 7, 8

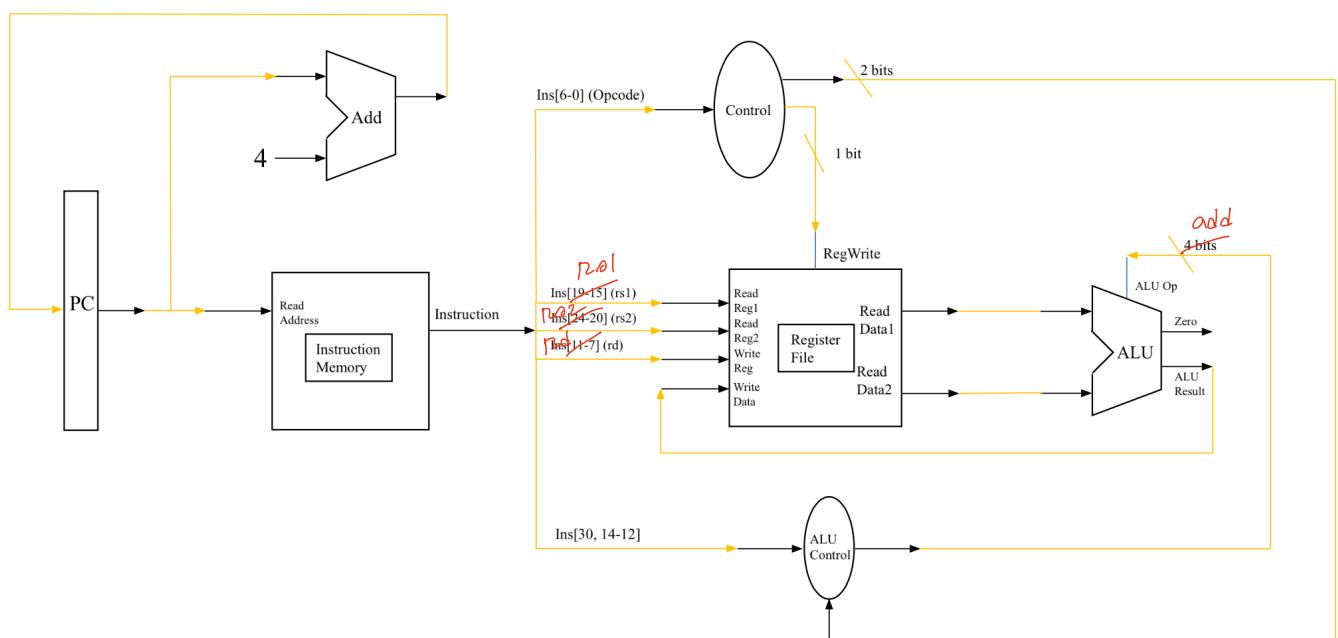
1, 2, 3, 4, 5, 6, 7, 8

} try yourself.

Question - 5:

Draw a simplified datapath with control unit that can process ADD X21, X22, X23

rd rd1 rd2



Question - 6:

Draw a simplified datapath with control unit that can process ADD X21, X22, X23

try
yourself

Question - 7:

Draw a simplified datapath with control unit that can process LD X21, 14(X22)

Question - 8:

Draw a simplified datapath with control unit that can process only the following codes:
Mention the control signals also for each instructions

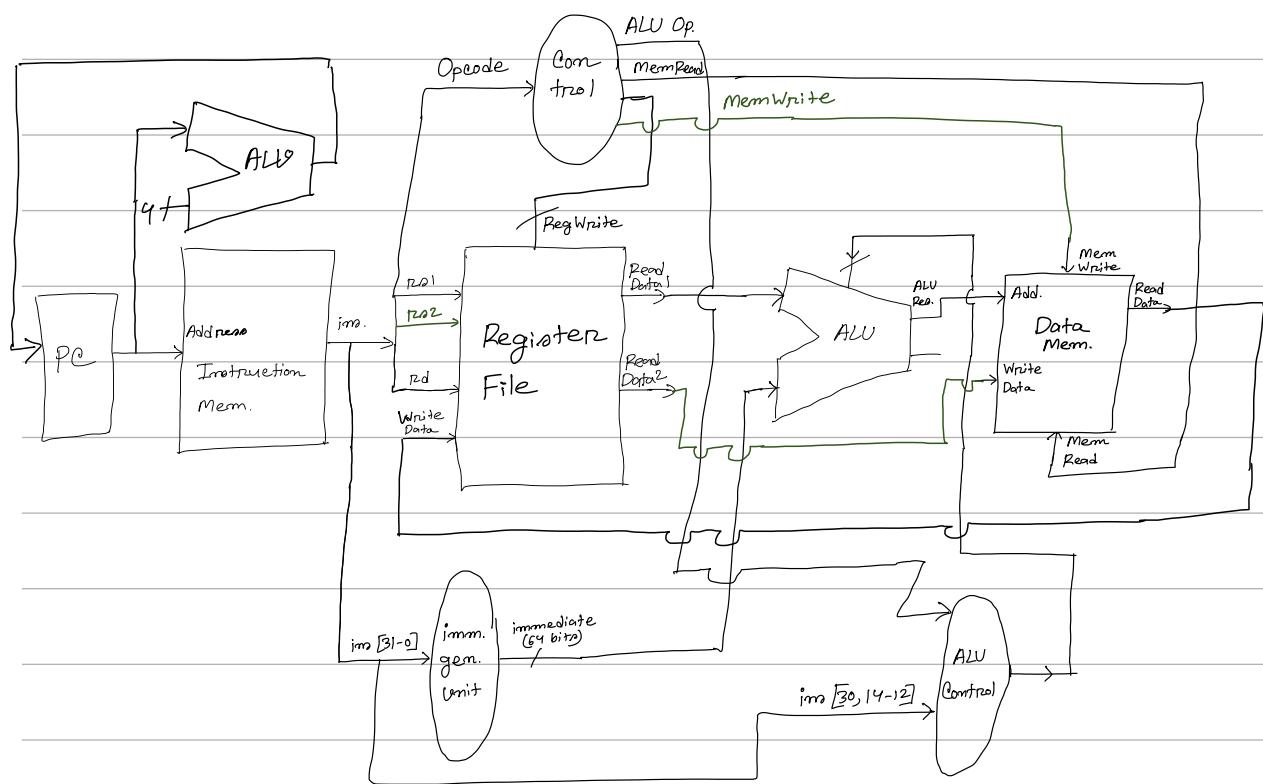
LD X21, 14(X22)

SD X22, 16(X21)

Control \Rightarrow ALU Op \rightarrow Add
 (Load) MemRead \rightarrow 1
 MemWrite \rightarrow 0
 Reg Write \rightarrow 1

Control \Rightarrow ALU Op \rightarrow Add
 (Store) MemRead \rightarrow 0
 MemWrite \rightarrow 1
 RegWrite \rightarrow 0

As the code for add is not mentioned.



Question - 9:

Draw a simplified datapath with control unit that can process only the following codes:

ADDI X21, X22, 5

LD X21, 14(X22)

Mention the control signals also for each instructions.

try
yourself.

Question - 10:

Draw a simplified datapath with control unit that can process the following codes:

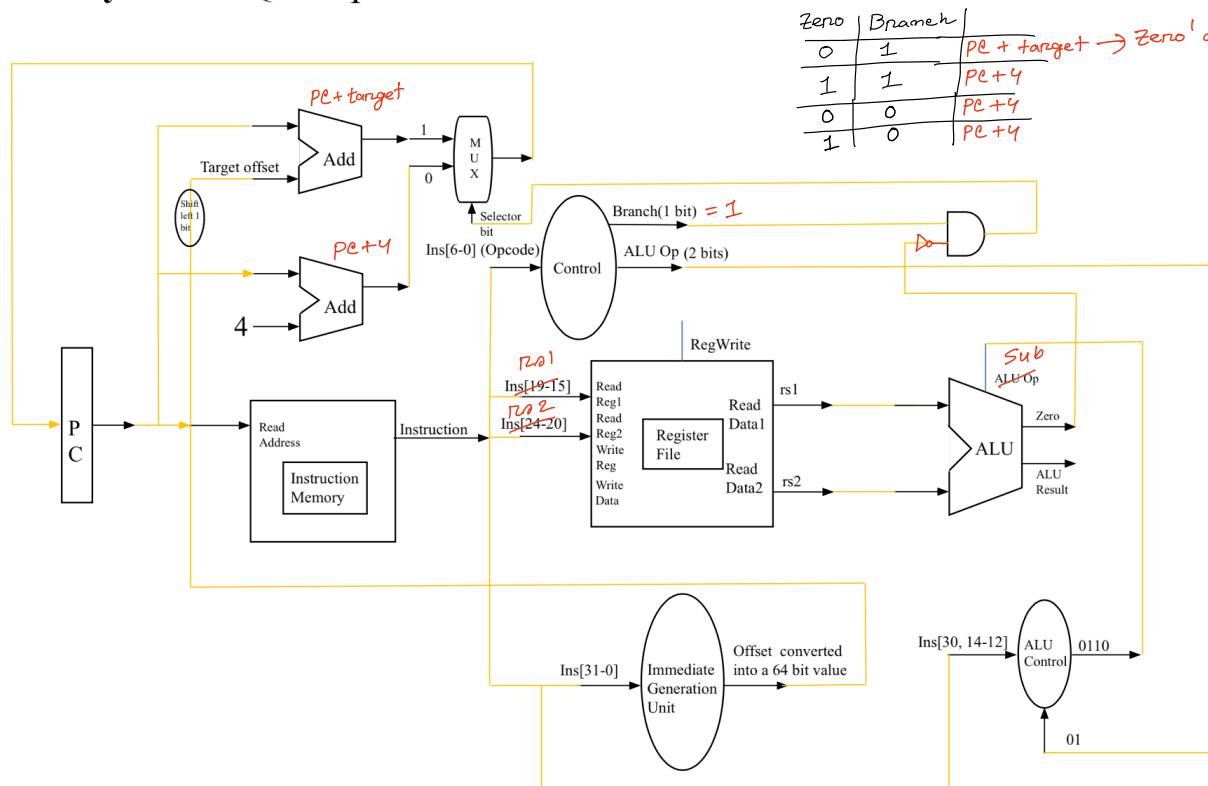
ADDI X21, X22, 5

LD X21, 14(X22)

Mention the control signals also for each instructions.

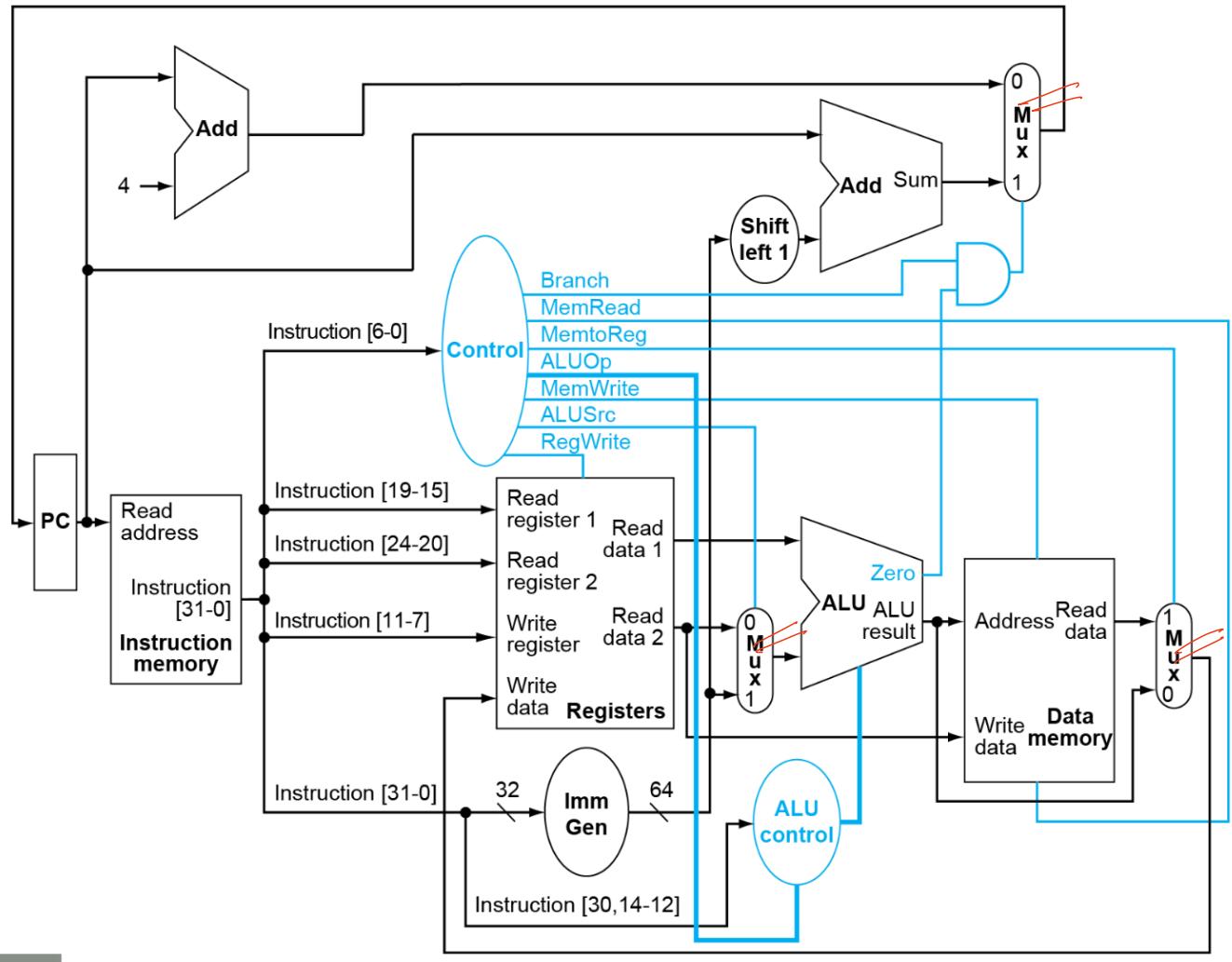
Question - 11:

Modify the BEQ datapath so that it works for BNE.

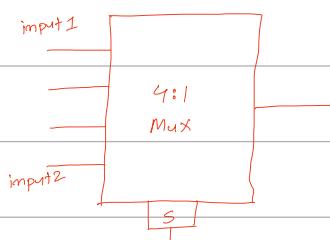


Question - 12:

Construct a single-cycle full-datapath, ensuring that you use only 4:1 multiplexer(s) wherever multiplexer(s) are required.



Just replace the 2:1 Mux(s) with the below

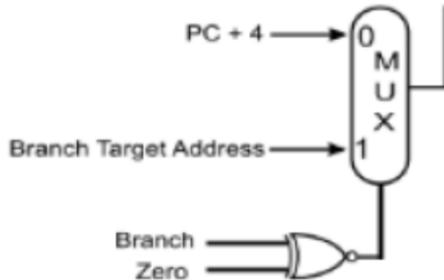


4:1 Mux that will
act as 2:1 Mux

Question - 13:

Suppose that in a buggy implementation of the RISC V datapath, the AND gate for the branching decision was replaced with an **XNOR** gate. Describe how this error would affect the execution of the following instruction.

- SUB** x1, x2, x3 [3 points]
- BEQ** x1, x2, target [3 points]



Branch = 0 ; Zero = 0 \Rightarrow Mux selects Data1 for output. Which causes error.

Branch = 0 ; Zero = 1 \Rightarrow Mux selects Data0 for output. u u no error.

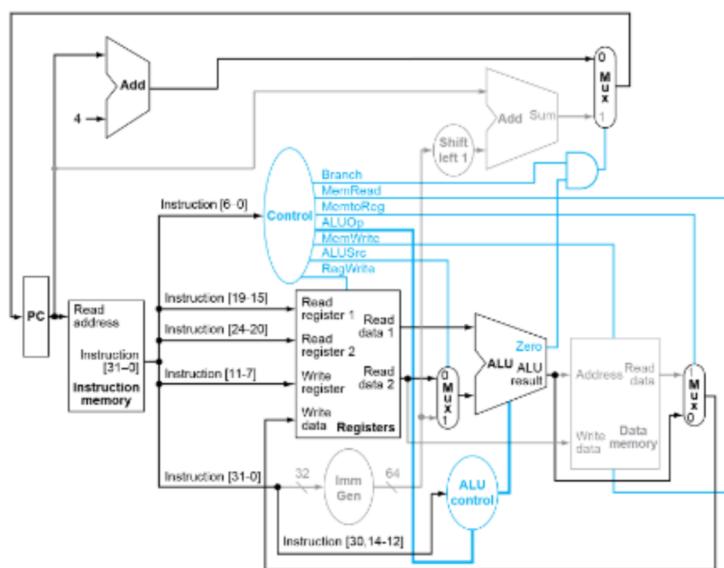
Branch = 1 ; Zero = 0 \Rightarrow Mux selects Data0 for output. Which causes no error.

Branch = 1 ; Zero = 1 \Rightarrow Mux selects Data1 for output. u u no error.

\rightarrow XNOR gate acting like and gate

for these two combo.

Question - 14:



Determine the values of the following control bits when executing the instruction "Add X21, X22, X23" in the provided single-cycle datapath.

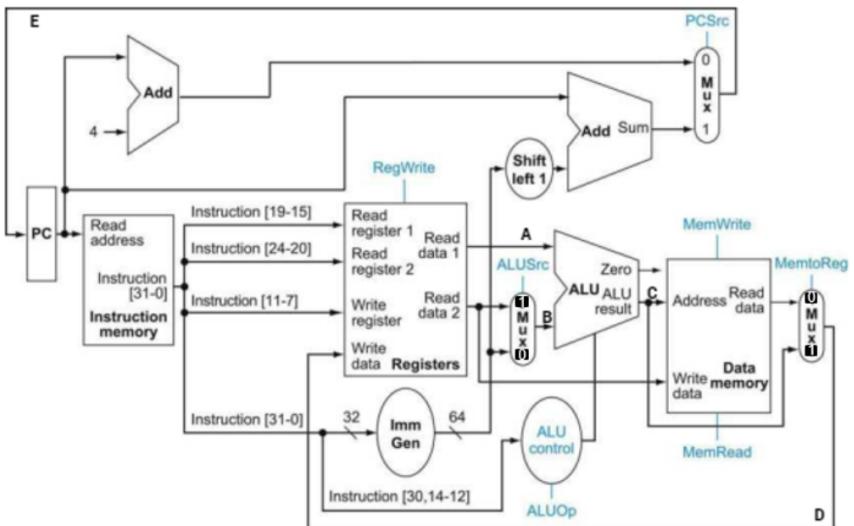
Branch	MemWrite	RegWrite	ALUSrc
0	0	1	0

Question - 15

Determine the values of the following control bits when executing the instruction "Addi X21, X22, X23" in provided single-cycle datapath for Q-13

Branch	MemWrite	RegWrite	ALUSrc
○	○	1	1

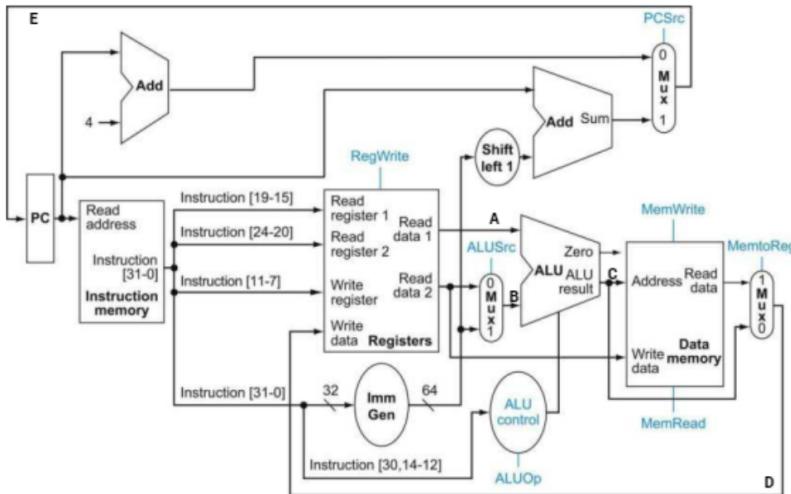
Question - 16:



Determine the values of the following control bits when executing the instruction "Add X21, X22, X23" in the provided single-cycle datapath.

Branch	ALUSrc	RegWrite	MemToReg
○	1	1	1

Question - 17:



Study the above RISC-V Datapath thoroughly. Assume that initially $PC=600_h$, $x_1 = 222_h$, $x_2 = 444_h$, $x_3 = 666_h$, $x_4 = 999_h$.

Determine the values of A, B, C, D, E in hex for the instructions executed in following order. If the value does not matter, write it as X (don't care)

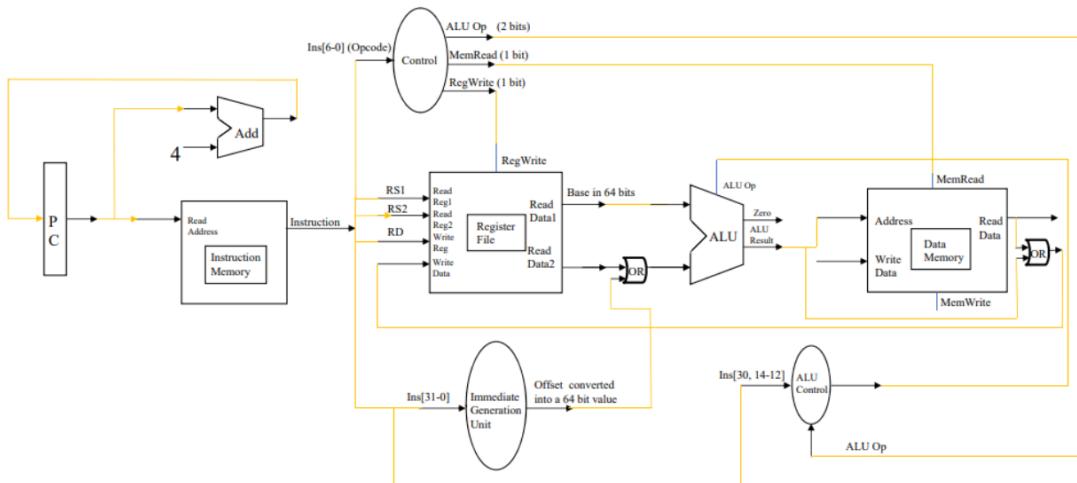
		A	B	C	D	E
i.	sub x_1, x_2, x_1	$444h$	$222h$	$222h$	$222h$	$604h$
ii.	sd $x_4, 12(x_2)$	$444h$	ch	$450h$	X	$608h$

Question - 18:

Carefully examine the RISC-V datapath provided in Q-17. Assume the initial values are: $PC = 600h$, $x_1 = 222h$, $x_2 = 444h$, $x_3 = 666h$, and $x_4 = 999h$. For the following instructions executed sequentially, determine the hexadecimal values of A, B, C, D, and E. If the value is irrelevant, indicate it as X (don't care).

i.	sub x_1, x_2, x_1	<i>try yourself!</i>				
ii.	sd $x_4, 12(x_2)$	<i>try yourself!</i>				
		PC	A	B	C	D
iii.	Addi $x_1, x_1, 12$				X	

Question - 19:



Given the following code sequence:

1. ADD X1, X2, X3
2. LD X5, 10(X4)
3. OR X2, X3, X23

Is it possible to execute this code sequence using the provided datapath?
If not, correct the datapath.

No, trace it to find the result.

Hint : Use mux.

Question - 20:

PC = 0x0040ABCD123045B1

Instruction Memory:

Address	Content
0x40ABCD123045AD	0111 0101
..... AE	1011 1110
..... AF	1001 0001
..... BO	1100 0000
..... BI	0000 0001
..... B2	1001 0101
..... B3	0000 0101
..... BY	0011 0011

Data Memory:

Address	Content
0x40ABCD123045AD	0111 0101
.....	0111 0100
.....	1000 0000
.....	1000 0001
.....	0000 0000
.....	0001 0111
.....	1000 0101
.....	1111 0011

* instructions are stored in instruction memory sequentially.

* instruction size = 32 bits

0000 0001 1001 0101

0000 0101 0011 0011

$\Rightarrow (01950533)_h$

Fetch the instruction from memory. Convert your answer in Hex.

Question - 21:

The following table shows the different stages involved in executing instructions and the corresponding durations for each stage:

stages	Instruction Fetch	Register Read	ALU Op	Memory Access	Register Write
Duration	50ps	10ps	30ps	20ps	10ps

Given the above durations, determine the total time required to complete each of the following instructions:

	Instructions	Time to complete each instructions
i.	ADD X ₂₁ , X ₂₂ , X ₂₃	50 + 10 + 30 + 10 = 100 ps
ii.	AND X ₂₁ , X ₂₂ , X ₂₃	
iii.	OR X ₂₁ , X ₂₂ , X ₂₃	
iv	ADDi X ₂₁ , X ₂₂ , X ₂₃	
v.	LD X ₂₁ , 22(X ₂₁)	
vi.	SD X ₂₁ , 22(X ₂₁)	
vii	BEQ X ₂₁ , X ₂₂ , End	

Question - 22:

Instruction	Time (PS)
Add X ₂₁ , X ₂₂ , X ₂₃	10
Sub X ₂₁ , X ₂₃ , X ₂₄	20
Mul X ₂₂ , X ₂₃ , X ₂₆	15
LD X ₂₂ , 0(X ₂₁)	25 ✓

The above instructions are being run in a **single cycle datapath**.

- a. Now determine what is the clock period of this system? — longest delay determines
- b. What would be the total time to run this instruction sequence? the clock period.

$$\begin{aligned} \hookrightarrow 1 \text{ ins.} &= 25 \text{ ps} \\ \therefore 4 \text{ ins.} &= (25 \times 4) = 100 \text{ ps} \end{aligned}$$

So, 25 ps.

Question - 23 :

What do you understand by the term "single-cycle" in the context of a single-cycle datapath?

→ Hint: 1 instruction per clock cycle.

Question - 24 :

Stage	IF	ID	EX	MEM	WB
Time (PS)	10	20	20	20	10

The below instructions are being run in a pipelined datapath. Calculate the time required to execute each instruction.

Instruction	Time (PS)
Add X21, X22, X23	
Sub X21, X23, X24	
Mul X22, X23, X26	
LD X22, 0(X21)	

{ try yourself.

Determine what is the clock period of this system? 20 ps

Question - 25 :

Write a comparison between the single cycle datapath and a pipelined datapath. Mention why pipelined datapath is implemented in real life.

Question - 26 :

In the RISC-V pipelined datapath we have 5 stages. Can we divide these 5 stages into more stages to make the datapath more efficient?

→ Open ended question. Do a bit research.