CSE341 Theory Assignment 04

Total Marks - 15

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1. IR2 and IR4 are masked. At t = 0, an interrupt request occurs in the IR6 that needs 45ns to be served. At t = 25ns, three interrupts occur at the same time namely: IR2, IR5 and IR7 each requires 30 ns to be served. At time t = 65, two interrupts occur simultaneously namely: IR0 and IR4 where both require a time of 20ns. Assume STI is set for the scenario.

Draw the IRR and ISR showing the simulation of how the values change in those resistors.
When will IR7 be fully serviced?

2. A) Calculate the minimum number of PICs (Master and Slaves) if the total number of interrupt requests is 59 at a time.

B) Calculate the minimum number of PICs (Master and Slaves) if the total number of interrupt requests is 32 at a time

C) Suppose there is a faulty 8259A where CAS2 is 0 signal. Now how many slave PIC can be added here. How many total interrupt requests can be used in cascaded mode.

D) Suppose there is a faulty 8259A where CAS0 is 0 signal. And IR0 and IR4 do not work. How many total interrupt requests can be used in cascaded mode.

E) Suppose there is a faulty 8259A where CAS0 is 0 signal. And IR1 and IR4 do not work. How many total interrupt requests can be used in cascaded mode.

3.

Intel. decided to create a new version of the 8237A DMA controller called “DMA 6” which supports 6 channels instead of the traditional 4 channels and has 20 address pins. Additionally, the size of the port addresses are now changed to 20 bits. A special register in 8086 named “QX” keeps the value of the 20 bits port address when using Variable Addressing. But for fixed addressing assume the size of the P8 byte remains the same.
A. Deduce the maximum number of I/O devices the DMA 6 can handle. [1]
B. Calculate the total size of the memory that the DMA 6 is capable of addressing [1]

C. Deduce the new range of addressing space for fixed addressing and variable addressing if Isolated I/O is used for I/O address mapping [1]
D. Assume DMA 6 is in cascading mode. Illustrate using a diagram how 2 secondary DMA 6's can be connected with one primary DMA 6 showing necessary pins for cascading mode. Also, explain the total process of how data transfer takes place between an Intel 8086 and the cascaded DMA 6's. [3]

4. "MOV AX, [1578h] can not be used in Isolated I/O meanwhile it can be used in memory mapped I/O for I/O addressing". Explain the statement.

5. Repeat question 1. With STI not set [this is if a higher priority interrupt arrives, it will not pause a lower priority interrupt].