Lecture 1

1. For each of the following devices, would you use a microcontroller or a microprocessor?
   i) Washing Machine
   ii) Android Phones
   iii) Remote controller
   iv) Microwave Oven

2. Your friend claims that an 8-bit microprocessor is always faster than a 4-bit microprocessor. How would you explain the factors that influence processor performance?

Lecture 2 **[MUST]**

1. Why is the address bus unidirectional while the data bus is bidirectional?
2. If a computer system needs to store startup instructions permanently, should it use RAM or ROM? Explain.
3. What is the role of the program counter in instruction fetching?
4. Differentiate between the Memory Address Register (MAR) and the Memory Data Register (MDR).
5. Suppose a microprocessor has a 16-bit address bus. How many memory locations can it address?
6. A CPU is executing a program, but you notice that some instructions take longer to execute than others. Which part of the fetch-decode-execute cycle could be causing this delay?
7. Imagine a data-intensive application that frequently transfers large amounts of data. Would increasing the size of the data bus improve performance? Why or why not?
8. If a microprocessor system frequently communicates with external hardware devices, what role does the control bus play in ensuring smooth operation?

Lecture 3

1. Find the values of the status flag registers for each set of instructions. **Explain** the values:
   i)
   ```
   MOV AX, 7E40h
   MOV BX, 3BC0h
   ADD AX, BX
   ```

ii)

```
MOV AX, 4B35h
MOV CX, CC74h
ADD AX, CX
```

iii)

```
MOV AX, FFh
MOV BX, 01h
ADD AX, BX
```

2. Suppose two hexadecimal numbers (i) FFCDh and (ii) FFYXh are to be added by an Intel 8086 microprocessor. Find

   i)

   Given PF = 0 & AF = 1 , Maximum value for XY

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ii) Find the minimum value for XY for same values of PF and AF given in i) **[MUST]**

[MUST] iii) Find the **minimum** value for X and **maximum** value for Y for the given PF and AF in i)

[MUST] iv) Find the **maximum** value for X and **minimum** value for Y for the given PF and AF in i)

v) Find the **maximum** value for X and **minimum** value for Y for PF = 1 **[MUST]**

v) Find the **maximum** value for X and **minimum** value for Y for PF = 0 **[MUST]**

3. **[MUST]** Suppose we have i) AB67h and ii) CD12h are to be added by intel 8086 microprocessor. Find:

   i) Given OF=1 CF=1 SF=0 ZF=0 , minimum AB & CD

   ii) Given OF=0 CF =1 SF=1 ZF=0 , minimum AB & CD

   iii) Given OF=0 CF =0 SF=0 ZF=0 , minimum AB & CD

4. **[MUST]** Suppose we have i) ABFFh and ii) CD52h are to be added by intel 8086 microprocessor. Find:

   i) Given OF=1 CF=1 SF=0 ZF=0 , maximum AB & CD

   ii) Given OF=0 CF =1 SF=1 ZF=0 , maximum AB & CD

   iii) Given OF=0 CF =0 SF=0 ZF=0 , maximum AB & CD

5. Find the logical addresses with the largest and smallest possible segment address for each of the following physical addresses. Also, mention the logical addresses for each case. (Maximum segment size can be 64KBytes)

i) 54213h
ii) 12h given here
ii) 1234Bh

6. **[MUST]** Find the 2nd, 3rd and 9th lowest logical address from the following physical address:
   a) 41216h given here
   b) 8124Ah
   c) 12450h
7. **[MUST]** Find the 4th, 7th and 12th largest logical address from the following physical address.
   a) 5131Fh
   b) A1240h
   c) 96823h given here

8. Instead of 64KB, assume the size of each segment for an 8086 is 4KB. In that case, deduce the 2nd last address of a segment whose starting address is 10000h.
→ 4KB means we are working with a data bus of size 12 bit. Hence 3 hex digits. So max value of offset FFFh. 2nd last address of a segment = 10000h + FFFh - 1 = 10FFEh

9. Find at least three logical addresses for each of the following physical addresses. If three logical addresses are not possible, state the reason:
   i) 15132h YT video Link
   ii) 16h
   iii) 6213Bh

1. **Given DS = 1000h, CS = 3000h, SS = 2000h, SI = 1005h, IP = 1234h, SP = 2342h.**

Address	Data
22345	12h
22344	23h
22343	34h
22342	45h
22341	56h

A. **Deduce** the instruction that loads data from the top of the stack into the AX register. [1 mark]

B. From the given table of the stack section **determine** what data will be stored in the AX register. [NB: For every byte of data loaded from the stack top, the value of SP increases by 1]. [2 marks]

C. If one further data load is done, what will be the value of SP.

D. Now we want to push data from the AX register to the stack, write the instruction for it.

E. Now what is the value of SP.

Ans: A) POP AX or MOV AX, [SS + SP]

B) Location the top of the stack points to→ (SSx10) + SP

= 20000 + 2342

= 22342h

Data in AX = 3445h

C) After the original pop, value of SP is 2342 + 2 = 2344h

After another pop, value of SP is 2344 + 2 = 2346h

D) PUSH AX or MOV [SS+SP], AX

E) After this PUSH, value of SP will be = 2346h - 2 = 2344h

Theoritical Question Section, **[MUST]**

1. Explain the difference between status flags and control flags in the flag register.
2. What does the Zero Flag (ZF) indicate, and how is it useful in programming?
3. What is the function of the Direction Flag (DF) in string operations?
4. What is the Trap Flag (TF) used for in debugging?

5. A program needs to process a string of characters from the end to the beginning. How should the Direction Flag (DF) be set?
6. If an external hardware device sends an interrupt signal to the CPU, but the Interrupt Enable Flag (IF) is cleared (0), will the CPU respond to the interrupt? Explain why.
7. When adding two 8-bit numbers, the sum causes a carry from the lower nibble to the upper nibble but not from the most significant bit. Which flag(s) will be set?
8. A programmer enables single-step debugging on the 8086. Which flag is responsible for this, and how does it function?
   → Trap Flag. If TF = 1, then we execute the program in a single step manner.
9. If a segment starts at address 20000H and another starts at 20100H, are they overlapping? Justify your answer.
10. If a segment has a starting address 31240H, what should be the next starting address of the segment provided we are working with non overlapping segmentation.
    → 31240h + FFFFh + 1 =
11. Provided we are working with non overlapping segmentation, what is the last address of a segment 5234.
    → 52340h + FFFFh =

Lecture 4

1. Write the equivalent instruction for the following machine code.
   i) 891Ah
   ii) 88CFh
   iii) 8B5654h
   iv) 890E1256h
   v) 8AA93762h
   vi) 8B5475h **[MUST]**
   vii) 88160080h
   viii) 8BD0 **[MUST]**
   ix) 8BDA **[MUST]**
   x) 8816FF96h **[MUST]**

2. Write the equivalent machine code for the following instruction.
   i) MOV AH, BL
   ii) MOV [5134h], DX
   iii) MOV AX, 1234h[BP+SI]
   iv) MOV [6341h], [6123h] →Invalid. Two memory locations can not be there.
   v) MOV CL, [SI]87h
   vi) MOV AX, [DS + BP + 1000h] →Invalid. As BP can not be the register of DS

vii) MOV BL, [1234h]

ix) MOV AX, [1234H]

a. MOV 5678H[DI], CL
b. MOV [BX + SI + 5312h], AX.
c. MOV BX, [BP + SI+23FFh]
d. MOV [BX], [BP + SI+23FFh]
e. MOV AX, [BX]
f. MOV 1234h[SI], AX
g. MOV DI, [BP+42h]
h. MOV C5A4h, CX
i. MOV [BX + SI +56H], [1234H]

3. State the addressing mode for the following instructions. Explain: **[MUST]**

i) MOV [BX+SI+10], AX → Base relative plus index

ii) MOV AX, BX → Register direct.

iii) MOV 1234h, CX →Invalid. As immediate value is in the destination

iv) MOV [1454h], BX → Direct Addressing

v) MOV [1246h],[2423h]

vi) MOV CL, [AX]

vii) MOV AL, BX → Invalid. As we can not transfer data between register of varying length

viii) MOV AX, [SS + SI + 1000h] → invalid. As SI is not the offset of SS

ix)

a. MOV [BX], CL → register indirect
b. MOV CL, [BX+SI] → Base plus index
c. RET [1234h]
d. MOV AX, [BP] → register indirect
e. IN 05h, DX → invalid. Here DX is correct. But the dest has to be a register.
f. OUT DX → invalid. Only one operand.
g. MOV CL, [BX+SI+4592H] → Base relative plus index
h. MOV BL, [2000H] → direct addressing
i. MOV 34H, CL → invalid. Immediate value/data not as destination.
j. MOV AH, [BP] → register indirect
k. HLT AX → invalid. Can not have any operand. One operand here.
l. MOV [BX], [BP + SI+23FFh] → invalid. Two memory locations can not be there.

4. **[MUST]**

Address	30300h	30301h	30700h	30701h	40700h	40701h	52700h	52701h
Data	23h	12h	51h	76h	11h	32h	91h	47h

Given DS = 3000h, SS = 5000h, ES = 4000h, CS = 1000h, BP = 0500h, SI = 0200h , DI = 0300h

Find the value stored in the register:

i) MOV AX,[SI+ BP]→(DS x 10) + 0200 + 0500 = 30000 + 0200 + 0500 = 30700h. AX stores 7651h

ii) MOV BL, [BP+SI+2000h]

iii) MOV DH, [DI]

iv) MOV CX, [0700h] → (DSx10) + 0700h = 30000 + 0700 = 30700h. CX stores 7651h

v) MOV DL, [ES + SI + BP] → (ESx10) + SI + BP = 40000 + 0200 + 0500 = 40700h . DL stores 11h

vi) MOV DH, [ES + BP + SI] → Invalid. ES can not have BP as an offset register.

5.

Address	07000h	07001h	27000h	27001h	37000h	37001h
Data	12h	34h	56h	78h	10h	20h

a. Assume for an Intel 8086, CS = 2000h, DS = 3000h, SS = 2000h, BX = 1000h, BP = 2000h, IP = 3456h, and SI = 3000h. Now if MOV DX, [BP + SI + 2000h] is the next instruction that is to be fetched, then deduce from which memory location will the 8086 start fetching the above-given instruction.

b. Deduce using mathematical calculations, what data will be stored in DX after the execution of the above given instruction.

6. **[MUST]**

Address	10600h	10601h	20600h	20601h	30600h	30601h
Data	12h	34h	56h	78h	10h	20h

Given DS = 1000h, SS = 2000h, CS = 3000h, BP = 0500h, SI = 0100h. Deduce what data will be stored in BX if the instruction MOV BX, [BP + SI] is executed.

7. **[MUST]**

Address	33413h	33412h	14001h	14000h	8D401h	8D400h	03000h
Data	67	45	78h	56h	34h	12h	ABh

Given DS = 1000h, CS = 3000h, SS = 8A40h, BP = 2000h, CX = 43AEh, DI = 030Fh. We execute the JMP [BP + 1000h] instruction. Deduce the physical address of the instruction that 8086 will jump to. Finally, find the value stored (16 bit) in the location

Location of IP = (SSx10) + 2000 + 1000h = 8A400 + 2000 + 1000 = 8D400h
Value of IP = 3412h
Physical location 8086 jumps to = (CSx10) + IP = 30000 + 3412 = 33412h

Value stored = 6745h

8.

Address	31234h	31235h	12000h	12001h	30600h	30601h
Data	12h	34h	10h	20h	11h	21h

Assume for an 8086, DS = 1000h, CS = 3000h, SS = 8A40h, BX = 2000h, BP = 1234h, SI = 0020h, DI = 030Fh. We execute the JMP [BX] instruction. Deduce the physical address of the memory location 8086 will jump to.

Lecture 5

1. Assume a scenario where another device is requesting control over the system bus of 8086. 8086 has rejected that request. Also, the 8086 is currently working in minimum mode.

Deduce the values of the concerned pins. Give reasons behind your answer.

Ans: HOLD = 1, it signifies another device is requesting access to the system bus. HLDA= 0 , it shows the hold request is denied. S6= 0 which shows the bus is in control of an 8086 microprocessor.

2. Based on the scenario, write what is happening based on RD' and WR' pins values.

RD' =1 and WR'= 1⟶ Neither read nor write

RD' = 0 and WR' = 1 ⟶ Read operation

RD' = 1 and WR' = 0 ⟶ Write operation

RD' = 0 and WR'= 0 ⟶ Invalid (can NOT read and write at the same time.)