Timing Diagrams:

[Must] 1. Suppose you have an Intel 8086 which is operating at a Duty Cycle of 60% and for each clock pulse assume T_{off} = 40ns. The 8086 is now going to execute the instruction MOV [1235h], AX. Based on this, answer the following questions:

a. Estimate the frequency at which the 8086 is operating.
b. Calculate the total time for one Instruction Cycle of the given instruction.
c. Calculate the values of the A_0 and BHE' pins during the execution of the given instruction.

2. Suppose an 8086 is operating in a way such that T_{ON} is 1/4th of the total time required for one clock pulse. Consider T_{ON} is 30ns. Now the 8086 is going to execute the instruction MOV AX, [2315h] i.e. 16 bits of data will be read from memory.

a. Calculate the frequency in MHz at which the 8086 is operating.
b. Calculate the time required for 1 Machine / Bus Cycle.
c. Deduce the total time required to execute the given instruction MOV AX, [2315h].
d. Explain with proper reasoning the values of pins A_0 and BHE' during the execution of the given instruction MOV AX, [2315h].

[Must] 3. For the following instructions, mention the states of $\overline{RD}$, $\overline{WR}$, $M/\overline{IO}$, $\overline{BHE}$ pins during the T2 cycle.

a. MOV AL, [34h]
b. MOV [33h], BL
c. OUT 82h, AL
d. IN AL, 82h

4. 8086 executes MOV AX, [1233H] on a system clocked at **20MHz** with **a 50% duty cycle**.

(a) Draw the **timing diagram** for both bus cycles showing A0–A19, D0–D15, ALE, RD, DEN', DT/R', and BHE'.

(b) Label the states (T1–T4) and indicate where the address and data appear.

(c) Highlight where a **wait state** would be inserted if memory response was delayed by 1 cycle during the first byte transfer.

Memory Banks:

1.

Suppose you have an Intel 8086 working at a frequency of 40MHz. Then, it comes across a memory-read instruction from an odd addressed location whose **Instruction cycle** would be 200ns.

a. Based on the given scenario, **deduce** the possible values of the A_0 and BHE' pins for the above given instruction. Please show the necessary calculations that support your conclusion. **[3]**
b. **Draw** the timing diagram for the given instruction. You must showcase the values of the A_0 - A_{19}, D_0 - D_{15}, ALE, M/IO, DT/R', and DEN' pins. **[4]**

2. A 64-bit processor is attempting to read a 64-bit (8-byte) word from memory, where each memory bank is 8 bits wide and memory banking is used to improve performance. The read begins at byte address 03H.

Determine whether this address is aligned or unaligned. Then, calculate how many memory cycles are required to complete the full 8-byte read operation from this unaligned address. Justify your answer based on how data is distributed across the memory banks.

3. An 8086 cpu has a RAM of 1MB split into two equal memory banks. The A_0 and BHE' pins of the cpu are used to access the two memory banks. For each of the given instructions in QS 4 (below), determine the following information:

(i) Size of the data being transferred (byte/word)
(ii) Which portion of the data bus was used to transfer the data from source location to destination register
(iii) Value of A_0 and BHE' required to make the transfer

(iv) Memory bank from which the data is fetched
(v) Total number of data cycles used to move data

[Must]-- [Solve in Review Class 2] 4. Assuming DS=1523h, consider the following instructions-

a. MOV AH, [8085h]
b. MOV AL, [8085h]
c. MOV BH, [8085h]
d. MOV BL, [8085h]

Do the values of A0 and BHE' values change for the above instructions?

5. [Solve in Review Class 2] Complete the following table:

Instruction	Size	Address	A_0	BHE'	Memory Bank(s) Used	Bus Cycles
MOV AX, [1001H]	Word	Odd	?	?	?	?
MOV AH, [1002H]	Byte	Even	?	?	?	?
MOV BX, [1000H]	Word	Even	?	?	?	?
MOV DL, [1003H]	Byte	Odd	?	?	?	?

[Must]-- [Solve in Review Class 2] 6. Suppose a faulty compiler always places 16-bit variables at **odd addresses**.

(a) What performance penalty would this impose on the 8086?
(b) How would this affect the values of A_0 and BHE'?
(c) If a memory system adds a 1-cycle delay for switching banks, estimate the impact of misalignment across 1000 instructions.

[Must] 7. Imagine Intel redesigned the 8086 to support 4 memory banks, each 4 bits wide.

(a) How would this change the A_0/BHE' decoding logic?
(b) How many control lines would be needed to select among 4 banks?

(c) Propose a new pin scheme (similar to A_0 and BHE' in 8086) to select among these 4 banks.
(d) For word access from an unaligned address, how many banks and cycles are now involved?
Ans:
a) need to check additional address bits ie A1 and an additional BHE like pin. if 00 at the last bits of address it will chose the first bank, 01 -> second, 10 -> third, 11 -> fourth
b) 4 in total
c) A1A0, BHE1, BHE0 with diagrams
d) At most 2 cycles will be required in the worst case. Not more than that. 4 banks are involved.

[Must]-- [Solve in Review Class 2] 8. 8086 microprocessor working with the frequency of 40 MHz. Then it comes across a memory read operation whose instruction cycle would be 100 ns. Bus cycle = 100ns. 1 instruction has 1 bus cycle.

a) Explain the possible options here referencing to size of register and even/odd address . 8 bit from even, odd address. 16 bit from even address
b) Suppose the instruction fetches from the odd location, find the A0 and BHE' . Size of register. Suggest an instruction.
Ans: 8 bits from an odd location. A0 = 1 BHE' = 0. MOV AL, [1235h]
c) Suppose the instruction is fetched from an even location. Explain why it is not possible to find the values of A0 and BHE'.
Ans: two options: 8 bit from even location or 16 bit from even location. Different combination of A0 and BHE'
d) Now, let's say we now know the size of the register is 8 bits. Find the A0 and BHE' . Suggest an instruction. A0 = 0 and BHE' = 1.
e) Now, the T_{off} is three times compared to T_{on}. Find the Duty Cycle.

[Must]-- [Solve in Review Class 2] 9. Suppose an 8086 is operating in a way such that T_{OFF} is 1/5th of the total time required for one clock pulse. Consider T_{ON} is 30ns. Now the 8086 is going to execute the instruction MOV AX, [2315h] i.e. 16 bits of data will be read from memory.
A. Calculate the frequency in MHz at which the 8086 is operating. [1]
B. Calculate the time required for 1 Machine / Bus Cycle. [1]

C. Deduce the total time required to execute the given instruction MOV AX, [2315h]. [1]
D. Explain with proper reasoning the values of pins A0 and BHE' during the execution of the given instruction MOV AX, [2315h]. [2]
E. Suppose from the start of the T3 clock pulse, the memory took 240 ns to finalize uploading data on the data bus. Explain with reason whether the processor will exert a Wait State or not.

Interrupts:

1.

Assume the table below represents a portion of the 8086 memory address space. At the time of execution, the microprocessor has the following register values:

SS = 1F00h, SP = 10FAh
CS = 2A00h, IP = 1230h

Suddenly, a signal arrives at the INTR pin.

Address	00A08h	00A09h	00A0Ah	00A0Bh	00100h	00101h	00102h	00103h
Data	34h	12h	78h	56h	78h	56h	34h	12h

a) Which bits of the FLAGS register will change when the interrupt is accepted? Explain briefly.
b) If the signal corresponds to interrupt type 40h, determine the new values of IP and CS as the 8086.
c) Show how the stack changes after the interrupt is acknowledged (show what values are pushed and where, in terms of addresses)

2.

a. **Assume a hypothetical scenario** where **CS** and **IP** values for the starting address of an **Interrupt Service Routine (ISR)** are **1230h** and **2000h**, respectively. Here each memory location can store a maximum of 1 byte data. Now the ISR consists of **14 lines** of code and **assume 5 bits** are required to store each line of code. Now, **deduce** mathematically the **address** where the **IRET** instruction will be found. **[2]**

3. **[Solve in Review Class 1]**

Addr.	D4h	D5h	D6h	D7h	751ECh	751EDh	221h	222h	223h	224h
Data	9Ch	A0h	15h	6Bh	89h	5Bh	12h	34h	11h	ABh

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A. **Deduce** the size of the **Interrupt Vector Table** (IVT) of the Intel 8086. [1]

B. **Calculate** the **interrupt vector** of the **ISR** corresponding to the interrupt caused by **INT 53**. Also, deduce the first **2-byte** hex instruction that will be fetched to the instruction queue from the ISR. [3+1 = 4]

C. **Explain** in detail the **actions** taken by **8086** when responding to an **interrupt** request in the **INTR** pin. [3]

3. **[MUST]- [Solve in Review Class 2]** Suppose the CS value needed to reach a particular Interrupt Service Routine (ISR) is A12Bh, and it is stored at memory locations 000B2h (low byte) and 000B3h (high byte). Additionally, suppose the physical address of the ISR is A45D4h.

a. Determine the Interrupt Type that triggered this ISR.
b. Calculate the value that will be stored at memory location 000B1h.

4. **[Solve in Review Class 2]**

Suppose while the current instruction is executing, an NMI occurs. The NMI will be serviced before the next instruction begins executing. Find out the physical address of the NMI interrupt service routine. [2]

Interrupt Vector Table(in hex): BB 08 0B 02 65 04 70 00 16 05 DA 09 65 04 70 00

Qs5. [Solve in Review Class 2]

An 8086 µp has some segments which have the following segment addresses respectively: DS = 2000h, CS =3000h, SS = 4000h. In this 8086 µp, a program X was running but suddenly an interrupt N occurred. To service this interrupt N, we need to go to ISR which is at 386A9h and it is located in the same code segment of the µp. Additionally, before fetching the ISR, the offset of the stack top became 3509h. Some parts of the memory is also given below:

Address	Data
43510h	57h
43509h	76h
43508h	32h
43507h	13h

Address	Data
43506h	93h
43505h	38h
43504h	56h
03AFh	30h

Address	Data
03AEh	00h
03ADh	86h
03ACh	A9h
03ABh	98h

a) **What** is a non-maskable interrupt? Provide an example. [1]
b) **State** the difference between **Type-1** and **Type-3** interrupt, **if any**. [2]
c) **Deduce** the value of **CS** and **IP** of program X. You must show the calculation. [3]
d) **Deduce** the memory addresses or locations of the IVT table where the **CS** and **IP** of Interrupt N is situated. You must show the calculation. [2]
e) **Deduce** the Interrupt **Type N**. You must show the Calculation. [2]

PIC (part of interrupt)

1. A student developed a custom interrupt controller named "PIC-X", which can handle 16 interrupt requests via pins IR0 – IR15. It has three 16-bit registers: Interrupt Request Register (IRR),Interrupt Mask Register (IMR), In-Service Register (ISR)

Each bit corresponds to one interrupt line, where bit 0 represents IR0 (highest priority) and bit 15 represents IR15 (lowest priority).

Assume the following partial values for bits 0–5 of these registers:

ISR[0–5] = 001000

IMR[0–5] = 010101

IRR[0–5] = 111001

a. Identify which interrupt(s) are currently being serviced.
b. Identify which interrupt(s) are currently masked and hence cannot be serviced.
c. Determine the order in which the pending interrupts from IRR will be serviced, if any.

[Assume IR0 has the highest priority, and only one interrupt can be serviced at a time.]

4

5. A new PIC “Z” handles 16 interrupt request lines and mimics the 8259A architecture. Number of interrupt types is 280.

a. What is the size of the Interrupt Request Register (IRR), Interrupt Service Register (ISR), and Interrupt Mask Register (IMR)?
b. Justify if 8 data bus lines would be sufficient to communicate with an 8086 processor. Ans - Not valid. As 2^8 = 256. So there are 256 types of interrupts that can be handled. Hence we can NOT handle 280 types of interrupts.

[Must] 6. Design a scenario where the PIC "X" is in cascading mode with 1 master and multiple slave PICs.

a. If PIC "X" can support 10 IR lines per controller, how many PICs are required to support 100 I/O devices?
b. How many cascade lines must be implemented?.

[Must] 7. A new PIC handles 16,384 interrupts.
a. Calculate the number of bits needed to uniquely identify each interrupt type.
b. What implication does this have on the internal architecture of the PIC?

[Must] 8. You are designing a PIC named "X" with 12 interrupt request lines (IR0–IR11). At some point during operation, the following register states are observed:

IRR = 000001000000

ISR = 000000010000

IMR = 000000100100
An interrupt request is now received on **IR5**.

a. Will the PIC generate a new interrupt signal to the CPU?
b. Will the currently executing ISR (IR4) be stopped? Justify your answers.

[Must] 9. PIC "X" is designed to support **4096 types of interrupts**. It communicates interrupt type information to the 8086 via the data bus.

a. How many bits are required to encode 4096 types of interrupts.
b. Based on this, how many **data bus lines** should be connected between PIC "X" and the 8086 processor?

[Must] 10. PIC "X" is connected to the 8086 and designed to support **4096 different interrupt types**. If each interrupt type takes 4 bytes in the interrupt vector table, how much memory is required for the complete table?

Addr	B3h	B4h	B5h	B6h	B7h h	0471 1h	2544 dh	2544 Eh	192h	193h
Data	7Ah	1Dh	2Bh	9Eh	22h	44h	5Ch	6Fh	88h	1Ah

a. Deduce the size of the Interrupt Vector Table (IVT) of the Intel 8086.
b. Calculate the interrupt vector of the ISR corresponding to the interrupt caused by INT 45. Also, deduce the first 2-byte hex instruction that will be fetched to the instruction queue from the ISR.
c. Explain in detail the actions taken by 8086 when responding to an interrupt request in the INTR pin.

[Must] — 11. [Solve in Review Class 1]

a. **Assume a hypothetical scenario** where **CS** and **IP** values for the starting address of an **Interrupt Service Routine (ISR)** are **1230h** and **2000h**, respectively. Here each memory location can store a maximum of 1 byte data. Now the ISR consists of **14 lines** of code and **assume 5 bits** are required to store each line of code. Now, **deduce** mathematically the **address** where the **IRET** instruction will be found. **[2]** [(
b. Assume the **CS** value required to locate an **ISR** is **CBDCh** and is stored at memory locations **000AAh** and **000ABh** respectively. Additionally assume the **Interrupt vector (IV)** of that ISR is **CCFF2h**. Hence, **deduce** the **Interrupt Type** that caused the aforementioned ISR and the **value** that will be stored at **000A9h**. **[2+2]**

11. When servicing an interrupt explain why does the 8086 clear IF and TF?

[Must] 12. [Solve in Review Class 1]

a) Suppose we have a PIC Z with 20 IR pins instead of 8. It is cascaded with the same PIC Z as slave PICs. How many CAS pins are required. Ans - 5
b) Now PIC Z is the master and normal 8259A PICs are slaves. How many CAS pins are required. Ans - 5
c) For 8259 PIC, Suppose CAS2 is faulty (always 0). Find the max number of slave PICs that can be added. Maximum number of I/O devices. Ans - 4 slaves, 36 I/O device

d) For 8259 PIC, Suppose CAS2 is faulty (always 0) and IR3 and IR5 is not working . Find the max number of slave PICs that can be added. Maximum number of I/O devices. Ans: 2 slave pics. 27 I/O
e) For 8259 PIC, Suppose setup is like qs ©, how many min slave pics are required for I/O numbers - Ans: i) 33 ii) 22.
f) For 8259 PIC, Suppose setup is like qs (d), how many min slave pics are required for I/O numbers - i) 15 Ans - 2 ii) 27 Ans- 3 iii) 34 Ans-Invalid

Basic I/O System, DMA and DMAC:

1. Explain what is variable addressing? Which register is used for variable addressing?

2.

A. The utility of 15 channels, estimate the minimum number of secondary 8237 DMA controllers needed.
B. Construct the DMA cascading diagram based on your answer in (A). Your diagram should show how the secondary controllers are connected with the primary controller using the appropriate pins.

3. Describe the values of the given pins of an 8237 DMA Controller during a DMA write cycle: i. $\overline{IOR}$ ii. $\overline{IOW}$ iii. $\overline{MEMW}$ iv. $\overline{MEMR}$

[Must] 4. Describe the values of the given pins of an 8237 DMA Controller during a DMA read cycle: i. $\overline{IOR}$ ii. $\overline{IOW}$ iii. $\overline{MEMW}$ iv. $\overline{MEMR}$

[Must] – 5. For data transfer the following scenarios, among programmed I/O, Interrupt based I/O and DMA based I/O, which one would you prefer and why?

a. Matrix keypad connected to a door locking mechanism - Programmed I/O
b. Power outage detection in computers – Interrupt I/O
c. Transferring data from Hard disk to RAM. – DMA

6. How many I/O ports does the 8086 processor support in the isolated I/O method? Why?

[Must] 7. A particular I/O device utilizes the MOV operation to take input from a temperature sensor. Is the device memory-mapped or isolated?

[Must] 8. i. IN AX, DX where DX = 1234h ii. MOV AX, [1234h] Explain in detail how the I/O addressing technique in i. and ii. is different from each other.

9. Suppose a developed data acquisition system which is using an Intel 8086 microprocessor interfaced with an 8237 DMA controller. Where a high-speed memory-mapped sensor periodically sends large blocks of data that need to be stored directly into memory without involving the CPU.

During one such transfer, the sensor sends a signal to the DMA controller indicating that data is ready to be moved. The DMA controller initiates a DMA operation to transfer the data from the sensor to system memory.

Explain the sequence of operations that takes place between the DMA controller, the 8086 CPU, memory, and the sensor during the mentioned DMA process. Also, describe the expected states of the following control signals at each stage: HRQ, HLDA, DREQ, DACK, IOR', IOW', READY, MEMR', and MEMW'.