CSE341 Quiz 03

ID: **Total Marks: 15**

Duration: 25 mins

Name: **Sec:**

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1. Suppose there is an instruction MOV X, [412Yh]. The values of pins are as follows A_0 = 1 and BHE' = 0. **State** the values of X(any valid register) and Y(single digit) with proper explanation relating to the memory banks. **[1+1 = 2]**

Ans: A0 = 1 means the address is odd. And BHE' = 0, means the odd bank is used. Hence it means we are getting 8 bits of data from odd address. So ,

Valid values of X is any 8 bit register for eg. AL, AH, BL, CH , etc
Valid values of Y is any odd values for eg. 1,3,5,7,9, B, D

2. Suppose you have an 8086 microprocessor that takes 80ns for one clock cycle that asks to take in 16 bits of data from an unaligned word and
store it inside the AX register. Now deduce the following based on the given information (show all necessary calculations): **[Total - 5]**
i. Length of 1 instruction cycle for the aforementioned instruction. **[1]**
ii. Time for 1 Bus cycle for the 8086. **[1]**
iii. Time for T_{ON} and T_{OFF} for one bus cycle. (duty cycle = 60%). **[2]**
iv. Frequency at which the 8086 operates. **[1]**

3. The instruction cycle length is 400 ns for an aligned word. The T_{off} = 10 ns for a clock cycle. **Calculate** the duty cycle. **Calculate** the T_{off} time for a bus cycle here. **[1+1 = 2]**

Time for the bus cycle = 400 ns.
Toff for one bus cycle (4 clock cycles in a bus cycle) = 10 * 4 = 40 ns
Ton for one bus cycle = 400 - 40 = 360 ns.

Duty Cycle = 360 / 400 = 0.9 = 90%

Toff for one bus cycle = 40 ns.

4. “In the READ timing diagram, the Ready pin can be 1 in the 2nd clock cycle. This will result in the bus cycle being only 3 clock cycles long”. Is the statement correct, **explain** briefly with reasons. **[1+1 =2]**

No it is not possible. Bus cycle can NOT be less than 4 clock cycles. Furthermore, the ready pin is only high in the very end of 2nd clock cycle or just before the beginning of the third clock cycle.

5. “All software interrupts are non - maskable”.Is the statement correct, **explain** briefly with reasons Give at least 2 examples of software interrupts **[1+1 =2]**

Yes, correct. Software interrupts have to be serviced when it is encountered in the code.
Examples - Divide error, NMI

6.**[Total - 2]**

Address	00117h	00116h	00115h	00114h	00276h	00277h	00248h	00279h
Data	45h	86h	22h	14h	12h	34h	56h	78h

If the signal is of Interrupt type 69, then
Calculate the location where CS and IP are located in this table. **[1]**
Deduce the values of CS and IP as the 8086 starts the service routine. **[1]**

Ip is located in - 00114h and 00115h
CS is located in - 00116h and 00117h.

Value of IP = 2214h **Value of CS = 4286h.**

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1. Suppose there is an instruction MOV X, [412Yh]. The values of pins are as follows A_0 = 0 and BHE' = 1 **State** the values of X(any valid register) and Y(single digit) with proper explanation relating to the memory banks. **[1+1 = 2]**

Ans: A0 = 0 means the address is even. And BHE' = 1, means the odd bank is NOT used. Hence it means we are getting 8 bits of data from even address. So ,

Valid values of X is any 8 bit register for eg. AL, AH, BL, CH , etc
Valid values of Y is any even values for eg 0,2,4,6,8,A, C, etc

2. Suppose you have an 8086 microprocessor that takes 160 ns for one clock cycle that asks to take in 16 bits of data from an unaligned word and
store it inside the AX register. Now deduce the following based on the given information (show all necessary calculations): **[Total - 5]**
i. Length of 1 instruction cycle for the aforementioned instruction. **[1]**
ii. Time for 1 Bus cycle for the 8086. **[1]**
iii. Time for T_{ON} and T_{OFF} for one bus cycle. (duty cycle = 60%). **[2]**
iv. Frequency at which the 8086 operates. **[1]**

3. The instruction cycle length is 800 ns for an aligned word. The T_{off} = 10 ns for a clock cycle. **Calculate** the duty cycle. **Calculate** the T_{off} time for a bus cycle here. **[1+1 = 2]**

Time for the bus cycle = 800 ns.
Toff for one bus cycle (4 clock cycles in a bus cycle) = 10 * 4 = 40 ns
Ton for one bus cycle = 800 - 40 = 760 ns.

Duty Cycle = 760 / 800 = 0.95 = 95%

Toff for one bus cycle = 40 ns.

4. “In the READ timing diagram, the AD0 - AD15 pins are in floating state when no data or address is being transferred”. Is the statement correct, **explain** briefly with reasons. **[1+1 =2]**

Yes this state is true. When no data or address is being transferred, the pins will no be 1 or 0, otherwise a value will be registered. And since we are not transferring any data , so we do not want any value to be register

5. “All hardware interrupts are maskable”.Is the statement correct, **explain** briefly with reasons Give at least 2 examples of hardware interrupts **[1+1 =2]**

That is not true. Non Maskable hardware interrupts will occur when interrupts occur in NMI pins.

Hardware interrupt example - Interrupt from I/O , Power supply offline, Disk error.

6.**[Total - 2]**

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Valid values of X is any 8 bit register for eg. AL, AH, BL, CH , etc
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2. Suppose you have an 8086 microprocessor that takes 80ns for one bus cycle an instruction that asks to take in 16 bits of data from an unaligned word and store it inside the AX register. Now deduce the following based on the given information (show all necessary calculations): **[Total - 5]**
   i. Length of 1 instruction cycle for the aforementioned instruction. **[1]**
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   iv. Frequency at which the 8086 operates. **[1]**

3. The instruction cycle length is 400 ns for an aligned word. The T_{off} = 10 ns for a clock cycle. Calculate the duty cycle. Calculate the T_{off} time for a bus cycle here. **[1+1 = 2]**

Time for the bus cycle = 800 ns.
Toff for one bus cycle (4 clock cycles in a bus cycle) = 10 * 4 = 40 ns
Ton for one bus cycle = 800 - 40 = 760 ns.

Duty Cycle = 760 / 800 = 0.95 = 95%

Toff for one bus cycle = 40 ns.

4. “In the READ timing diagram, the DT/R’ pin can become 1 in the 3rd bus cycle and read operation happens as it should”. Is the statement correct, **explain** briefly with reasons. **[1+1 =2]**

No it is wrong. If DR/R’ pin becomes 1, then the transceiver is told / instructed to transmit data which would not allow the read operation to work properly.

5. “All software interrupts are non - maskable”.Is the statement correct, **explain** briefly with reasons Give at least 2 examples of software interrupts **[1+1 =2]**

Yes, correct. Software interrupts have to be serviced when it is encountered in the code.
Examples - Divide error, NMI

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[Total - 2]
If the signal is of Interrupt type 69, then
Calculate the location where CS and IP are located in this table. **[1]**
Deduce the values of CS and IP as the 8086 starts the service routine. **[1]**

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Value of IP = 2214h **Value of CS = 4286h**

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Ans: A0 = 0 means the address is even. And BHE' = 1, means the odd bank is NOT used. Hence it means we are getting 8 bits of data from even address. So ,

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3. The instruction cycle length is 800 ns for an unaligned word. The T_{off} = 10 ns for a clock cycle. Calculate the duty cycle. Calculate the T_{off} time for a bus cycle here. **[1+1 = 2]**

Time for the bus cycle = 800 ns.
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Duty Cycle = 760 / 800 = 0.95 = 95%

Toff for one bus cycle = 40 ns.

4. “In the READ timing diagram, the ALE pin is 1(high) in the 1st bus cycle only”. Is the statement correct, **explain** briefly with reasons. **[1+1 =2]**

Wrong. ALE pin only in the 1st cycle only. The address is transferred in the first clock cycle. Not the entire bus cycle.

5. “Hardware interrupts will always use the INTR pin”.Is the statement correct, **explain** briefly with reasons **. Show with calculation if there is a divide error for DIV BL, where AX is FFFFh and BL is F3h [1+1 =2]**

No it is not valid. Hardware interrupts can also go to NMI pins (if it is not maskable). Quotient = 10Dh. AL register stores the quotient. It can not be more than 8 bit hence div error is called.

6.

Address	00117h	00116h	00115h	00114h	00276h	00277h	00248h	00279h
Data	45h	86h	22h	14h	12h	34h	56h	78h

[Total - 2]
If the signal is of Interrupt type x, then the low byte of CS is 86h,
Calculate the location where CS and IP. And Find the value of x **[0.5 +1 = 1.5]**

Using values of CS and IP, find the location where the ISR is located. **[0.5]**

Ip is located in - 00114h and 00115h
CS is located in - 00116h and 00117h.

Value of IP = 2214h **Value of CS = 4286h**