CSE341 Quiz 04

ID: **Total Marks: 15**

Duration: 20 mins

Name: **Sec:**

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1. Describe the Interrupt Request Register (IRR). **[2]**

A 8 bit register to keep track of the interrupt that has arrived.
IRR0 has a higher priority compared to IRR7. If two interrupts arrive at the same time, then the higher priority will be serviced.

2. There is no interrupt that is being serviced. Suppose IR2 = 1, IR3 = 1 and IR7 = 1 at the same (interrupt arrives at the same time) and then there are no other interrupts. The IMR2 = 1. Now **explain** logically which interrupt is serviced first ? Assume we are in fixed priority mode. **[2]**

IR3 is serviced first. As it the unmasked and highest possible priority.
Here IR2 is not serviced even though it has a higher priority because it is masked.

3. There is a PIC Z where there are 20 IR pins instead of 8 pins. Based on this answer the following question: **[1 x 3 = 3]**
a) The PIC Z is in cascading mode where PIC Z are connected as slave PIC. Show with calculation how many total I/O devices can be attached in this scenario.
b) State the minimum number of CAS (Cascading) pins required for question (a).
c) Now 3 IR pins are faulty in the master PIC Z only, the slave PIC Z are fully functional. Now with proper calculation, find the total number of I/O devices that can be attached here.

a) Total I/O devices that can be added is = 20 x 20
b) Ceiling of [Log_2 (20)] = 5
c) 17 x 20

4. Write a short note on “Interrupt Driven I/O”. Is it faster than Programmed I/O? **[2+1 = 3]**

See slide .
Interrupt driven is more efficient and faster than programmed I/O

5. For the following, explain with logical reasoning whether each falls into variable I/O addressing, fixed I/O addressing or invalid. **[1x3 = 3]**

a) OUT DX , FFh
b) IN AX, 246
c) IN AX, CX where CX is 246

a) Not valid. As we can only have a register in the source (AL or AX)
b) Valid . Fixed addressing
c) Not valid. As register has to be DX.

6. What is the DMA read cycle? Calculate the maximum number of peripherals in the second level cascading scheme where DREQ3 and DACK1 pins are faulty in the master DMA controller only. **[1 + 1 = 2]**

DMA read - read from memory and write to I/O

2 channel functional in the primary DMA. Hence 2 * 4 = 8 . Total 8 peripherals can be added.

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1. Describe the In-Service Reg (ISR). **[2]**

8 bit register which keeps tracks of the interrupts in service.

2. There is no interrupt that is being serviced. Suppose IR5 = 1, IR3 = 1 and IR7 = 1 at the same (interrupt arrives at the same time) and then there are no other interrupts. The IMR3 = 1. Now **explain** logically which interrupt is serviced first ? Assume we are in fixed priority mode. **[2]**

IR5 is serviced first. As it the unmasked and highest possible priority.
Here IR3 is not serviced even though it has a higher priority because it is masked.

3. There is a PIC Z where there are 34 IR pins instead of 8 pins. Based on this answer the following question: **[1 x 3 = 3]**
a) The PIC Z is in cascading mode where PIC Z are connected as slave PIC. Show with calculation how many total I/O devices can be attached in this scenario.
b) State the minimum number of CAS (Cascading) pins required for question (a).
c) Now 4 IR pins are faulty in the master PIC Z only, the slave PIC Z are fully functional. Now with proper calculation, find the total number of I/O devices that can be attached here.

a) 34 * 34 = 1156
b) ceiling of $[\log_2(34)]$ = 6
c) 30 * 34 = 1020

4. Write a short note on “Programmed I/O”. Is it faster than Interrupt driven I/O? **[2+1 = 3]**

See slide
No. Interrupt driven I/O is faster.

5. For the following, explain with logical reasoning whether each falls into variable I/O addressing, fixed I/O addressing or invalid. **[1x3 = 3]**

a) OUT DX , CL
b) OUT BX, AX
c) IN AX, CX where CX is 12354h

a) Invalid. Only AL or AX can be used here as register. Allow valid.
b) Invallid. As the destination register can not be anything other than DX
c) Invalid. As CX can only hold 4 hex digits (2 bytes) of data.

6. What is the DMA write cycle? Calculate the maximum number of peripherals in the second level cascading scheme where DREQ3 and DACK3 pins are faulty in the master DMA controller only. **[1 + 1 = 2]**

DMA write - write to memory and read from the I/O

3 channel functional in the primary DMA. Hence 3 * 4 = 12 . Total 12 peripherals can be added.

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a) The PIC Z (master) is in cascading mode where PIC Z are connected as slave PIC. Show with calculation how many total I/O devices can be attached in this scenario.
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a) Total I/O devices that can be added is = 20 x 20
b) Ceiling of [Log_2 (20)] = 5
c) 17 x 20

4. MOV operation can be used to access I/O addresses. Is it memory mapped I/O or Isolated I/O. Answer with proper reasoning. **[2]**

Memory based I/O. Since in memory based I/O, the I/O mapping is done in memory hence using MOV operation we can access the section of memory which is dedicated for I/O mapping.

5. For the following, explain with logical reasoning whether each falls into variable I/O addressing, fixed I/O addressing or invalid. **[1x3 = 3]**

a) OUT DX , FFh
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c) IN AX, CX where CX is 246

a) Not valid. As we can only have a register in the source (AL or AX)
b) Valid . Fixed addressing
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6. What is the DMA read cycle? Values of IOR' , IOW' , MEMW', MEMR' in a DMA read cycle. Calculate the maximum number of peripherals in the second level cascading scheme where DREQ3 and DACK1 pins are faulty in the primary DMA controller **only. [1 +1+ 1 = 2]**

DMA read - read from memory and write to I/O
IOR' = 1 , IOW' = 0, MEMW' = 1 , MEMR' = 0
2 channel functional in the primary DMA. Hence 2 * 4 = 8 . Total 8 peripherals can be added.

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b) OUT BX, AX
c) IN AX, CX where CX is 1234h

a) Valid. Variable addressing
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6. What is the DMA write cycle? Values of IOR' , IOW' , MEMW', MEMR' in a DMA write cycle. Calculate the maximum number of peripherals in the second level cascading scheme where DREQ3 and DACK3 pins are faulty in the primary DMA controller **only. [1 + 1 +1 = 3]**

DMA write - write to memory and read from the I/O
IOR' = 0 , IOW' = 1, MEMW' = 0 , MEMR' = 1
3 channel functional in the primary DMA. Hence 3 * 4 = 12 . Total 12 peripherals can be added.