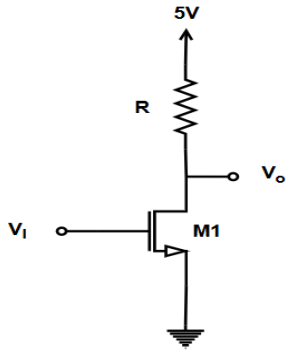
Question 01.

Following is the circuit of a N-MOS NOT gate. Given $V_{TN} = 0.5\ V,\ R = 20\ k\Omega$

$V_{DD} = 5V,\ K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 0.3\ mA/V^2$

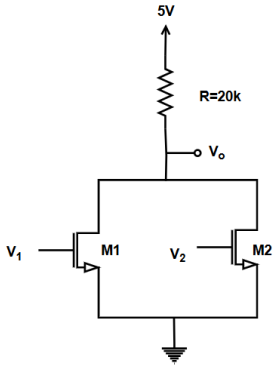


(a)	Find the output voltage of the inverter for the input voltage 5 V and 1.5 V.
(b)	Find the transition voltage (Saturation to triode) of the inverter.
(c)	Suppose, the input logic high and input logic low values of the NOT gate are 5V and 0V. Find the average power of the NOT gate.

Question 02.

Here, $V_{TN} = 0.8\ V\ and\ K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 0.1\ mA/V^2$

Value of the logic high is 5 V and logic low is 0V.



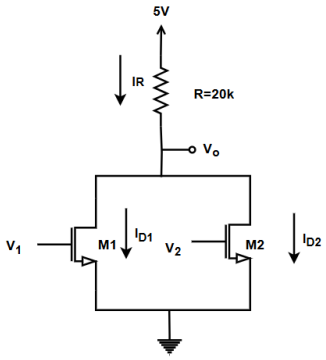
(a)	Identify the logic gate and make a truth table of the logic gate.
(b)	Find the output voltage of the logic gate for all possible case.
(c)	What will be the maximum and minimum power of the logic gate.

Question 03

Here, $V_{TN1} = 0.8\ V, V_{TN2} = 0.7\ V\ and\ K_{n1} = 0.1\ \ mA/V^2\ , K_{n2} = 0.2\ mA/V^2$

$Here, K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$

Value of the logic high is 5 V and logic low is 0V.

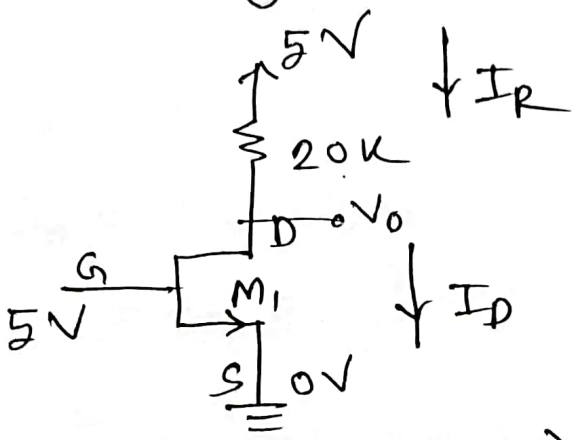


(a)	What will be the value of V_o and I_R of the circuit if both inputs are high.
(b)	Find the output of the NOR gate for the case $V_1 = 5\ V, V_2 = 0\ V$ and $V_1 = 0\ V, V_2 = 5\ V$. Why the values of the output voltage are different for the above two cases?

MOS

Q1. a) If, $V_I = 5V$, $V_{GS} > V_{TN}$, $M \rightarrow ON$

Assuming Triode Mode



Here, $V_{GS} = 5V$, $V_{DS} = V_0$

$$\frac{5 - V_0}{20} = 0.2\left[2(5-0.5)V_0 - V_0^2\right]$$

$\Rightarrow V_0 = 0.091V$ or $9.074V$

$V_0 = 0.091V$, $V_0 \neq 9.074V$

Verification: $V_{DS} = 0.091V$,

$V_{GS} - V_{TN} = 5 - 0.5 = 4.5V$

$\therefore V_{DS} < V_{GS} - V_{TN}$

M_1 will be in triode mode.

$\therefore V_0 = 0.091V$,

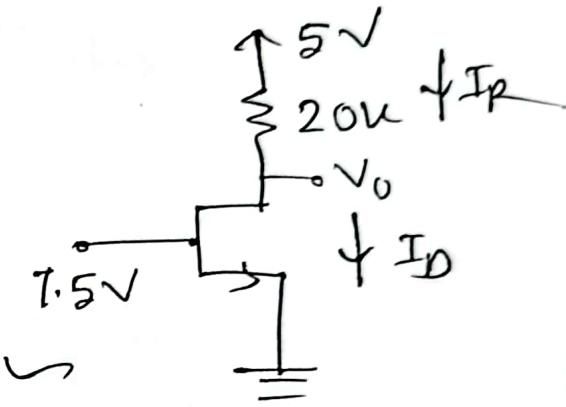
Q4)

For $V_I = 1.5V$,

$V_{GS} = 1.5V$, $V_{TN} = 0.5V$

$\therefore V_{GS} > V_{TN}$, $\longrightarrow$ M1 $\longrightarrow$ ON

Assuming M1 on saturation [V_I is low]



$$I_R = \frac{5 - V_o}{20}$$

$$I_D = k_n (V_{GS} - V_{TN})$$

$$= 0.3 \times (1.5 - 0.5)$$

$$\frac{5 - V_o}{20} = 0.3 (1.5 - 0.5)$$

$\Rightarrow V_o = -1V$,

Verification: $V_{DS} = V_o = -1V$,

$V_{GS} - V_T = 1.5 - 0.5 = 1V$

So, $V_{DS} \not> V_{GS} - V_{TN}$

Incorrect Assumption

Again, Assuming Triode,

$$\frac{5 - V_o}{20} = 0.3 \left[2 (1.5 - 0.5) V_o - V_o^2\right]$$

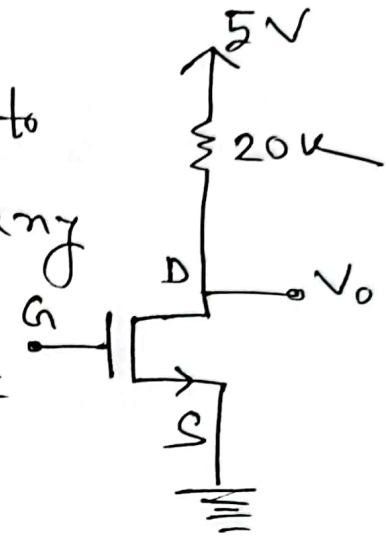
$V_o = \cancel{2.29}$ 0.5V, $V_o \neq$ other values 1.67V

$V_o = \cancel{2.29}$ 0.5V

Verification: $V_{DS} = \cancel{2.29}$ 0.5V, $V_{GS} - V_{TN} = 1V$

$V_o = 0.5V \therefore V_{DS} < V_{GS} - V_{TN}$ Assumption correct

Q1. b) $V_{TN} = 0.5V$, $K_n = 0.3 mA/V^2$



For transition of saturation to triode, we can apply any of the formula, Triode/Saturation.

However,

$$V_{DS} = V_{GS} - V_{TN}$$

$$\Rightarrow V_o = V_I - 0.5 \longrightarrow (1) \quad [V_{DS} = V_o \text{ and } V_{GS} = V_I]$$

We need to find the input voltage, V_I

$$\frac{5 - V_o}{20} = 0.3 (V_{GS} - V_{TN})^2$$

$$\Rightarrow \frac{5 - V_o}{20} = 0.3 \times (V_I - 0.5)^2$$

$$\Rightarrow \frac{5 - V_o}{20} = 0.3 \times V_o^2$$

$$\Rightarrow 6V_o^2 + V_o - 5 = 0$$

$$V_o = 0.833V \text{ and, } V_o \neq -1V$$

$$V_o = V_I - 0.5$$

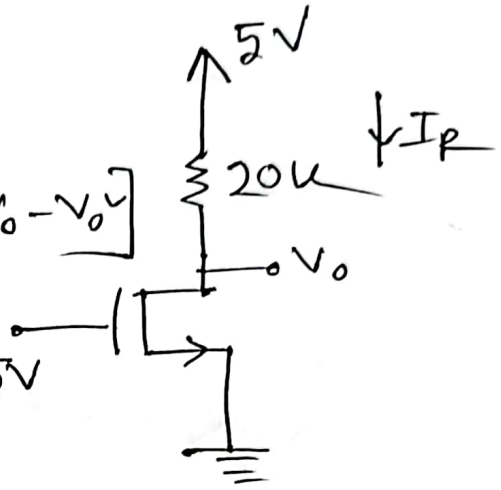
$$\therefore V_I = V_o + 0.5 = 0.833 + 0.5$$

$$= 1.33V$$

So transition voltage is 1.33V. Below 1.33V, MOS will be in saturation and above 1.33V, it will be in triode.

Q1.c)

Case 01: $V_I = 5\,V$



Assuming Triode,

$$\frac{5 - V_o}{20} = 0.3\left[2(5-0.5)V_o - V_o^2\right]$$

$$\Rightarrow 5 - V_o = 6\left[9V_o - V_o^2\right]$$

$$\Rightarrow 5 - V_o = 54V_o - 6V_o^2$$

$$\Rightarrow 6V_o^2 - 55V_o + 5 = 0$$

$$\Rightarrow V_o = 0.0918\,V, \quad V_o \neq 9.07\,V$$

$$I_R = 0.3\left[2\times(5-0.5)\times 0.0918 - 0.0918^2\right]$$

$$= 0.2453\,mA$$

$$P_1 = (5-0)\times 0.2453\,mW$$

$$= 1.227\,mW$$

Case-02: $V_I = 0$,

$V_{GS} < V_{TN}$, Cutoff Region,

$$I_D = 0 = I_R$$

$$\therefore V_o = 5\,V,$$

$$P_2 = (5-0)\times 0 = 0\,mW$$

$$P_{av} = \frac{P_1 + P_2}{2} = \frac{1.227 + 0}{2} = 0.6133\,mW$$

Q2.a) This is a NOR gate.

Truth Table

V_1(A)	V_2(B)	V_o(Y)
0	0	1
0	1	0
1	0	0
1	1	0

Q2.b) For, Case: $V_1 = 0V$, $V_2 = 0V$,

$V_{GS1} < V_{TN}$ and $V_{GS2} < V_{TN}$

Both are in cutoff,

$I_{D1} = I_{D2} = 0$,

$I_R = 0$

$\therefore V_o = 5V$

For, Case: $V_1 = 0V$, $V_2 = 5V$,

$V_{GS1} < V_{TN}$ and $V_{GS2} > V_{TN}$

$M_1 \rightarrow$ Cutoff, $I_{D1} = 0$

$M_2 \rightarrow$ Triode, $I_{D2} = 0.3\left[2(5-0.8)V_o - V_o^2\right]$

$$\frac{5 - V_o}{20} = 0 + 0.3\left[8.4V_o - V_o^2\right]$$

$$\Rightarrow 5 - V_o = 6\left[8.4V_o - V_o^2\right]$$

$$V_o = 0.0984V,$$

For, Case: $V_1 = 5V$, $V_2 = 0V$,

Similar to previous case,

$$V_o = 0.0984V$$

For Case,: $V_1 = 5V$, $V_2 = 5V$

$V_{GS1} > 0.8V$, $\longrightarrow M_1$ Triode

$V_{GS2} > 0.8V$, $\longrightarrow M_2$, Triode

$$I_{D1} = I_{D2} = 0.3\left[2(5-0.8)V_o - V_o^2\right]$$

$$\frac{5-V_o}{20} = 2\times 0.3\left[2(5-0.8)V_o - V_o^2\right]$$

$$V_o = 0.049406V$$

(2.c) Maximum power:

$V_1 = 5V$, $V_2 = 5V$,

From (b)

$V_o = 0.0494V$

$$I_R = \frac{5-0.0494}{20k} = 0.24753mA$$

$$P_{max} = (5-0)\times 0.24753mW$$

$$= 1.23765mW$$

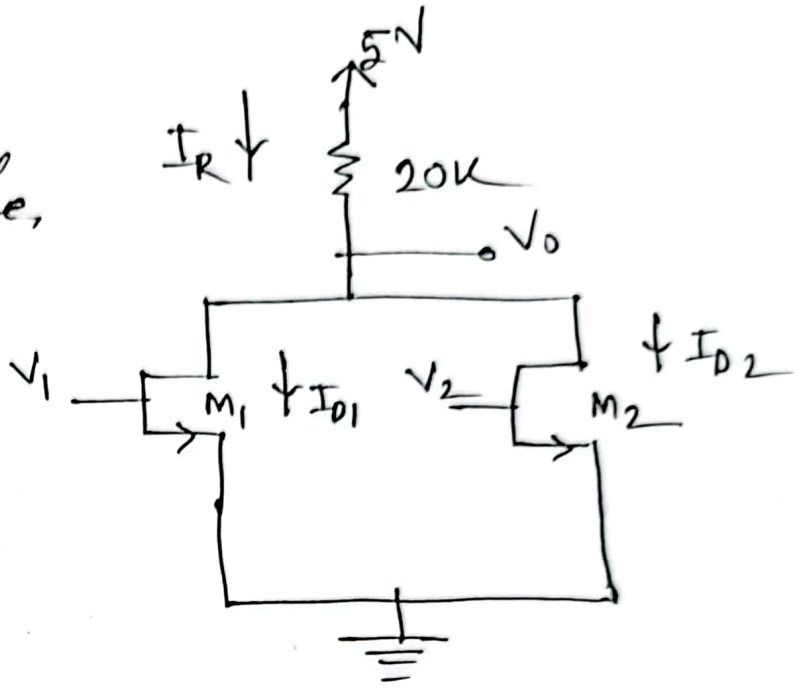
Minimum power:

$V_1 = 0V$, $V_2 = 0V$

From (b), $V_o = 5V$, $I_R = 0$

$P_{min} = (5-0)\times 0 = 0mW$

Q3. a) $V_1 = V_2 = 5\,V$



M_1 and M_2 are in Triode,

$$I_R = I_{D1} + I_{D2}$$

$$\Rightarrow \frac{5 - V_0}{20K} = 0.1 \times \left[2(5 - 0.8)V_0 - V_0^2\right] + 0.2\left[2 \times (5 - 0.7)V_0 - V_0^2\right]$$

$$\Rightarrow V_0 = 0.0986\,V$$

Q3. b) For, $V_1 = 5\,V$, $V_2 = 0\,V$,

$M_1 \rightarrow$ Triode, $M_2 \rightarrow$ Cutoff

$$\frac{5 - V_0}{20} = 0.1 \times \left[2(5 - 0.8)V_0 - V_0^2\right] + 0$$

$$V_0 = 0.290\,V$$

For, $V_1 = 0\,V$, $V_2 = 5\,V$,

$M_1 \rightarrow$ Cutoff, $M_2 \rightarrow$ Triode

$$\frac{5 - V_0}{20} = 0 + 0.2\left[2 \times (5 - 0.7)V_0 - V_0^2\right]$$

$$V_0 = 0.1435\,V$$

As the MOS given in NOR gate have not the same parameter, 01 and 10 cases are not same.