CSE 350
Digital Electronics and Pulse Techniques

Analog to Digital Converter (ADC)

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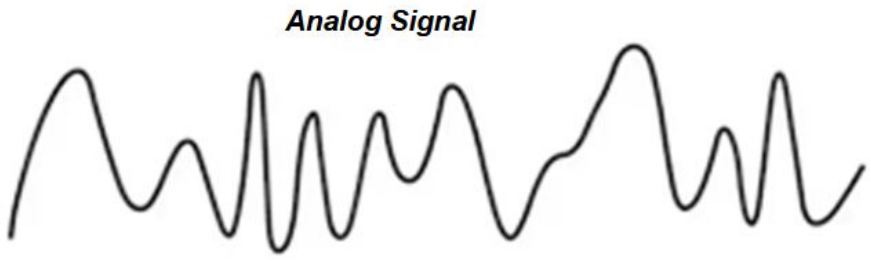
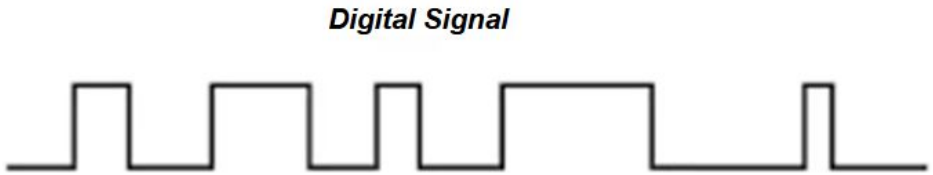
Analog to Digital Converter (ADC)

Signal can be classified into two broad categories.

i. Analog Signal ii. Digital Signal





Analog to Digital Converter (ADC)

Physical world's information are mostly analog. Analog means data could take any real value at each instant of time.

In order to store/process we use digital data in our computers and microprocessor

Digital data means binary bit of strings.

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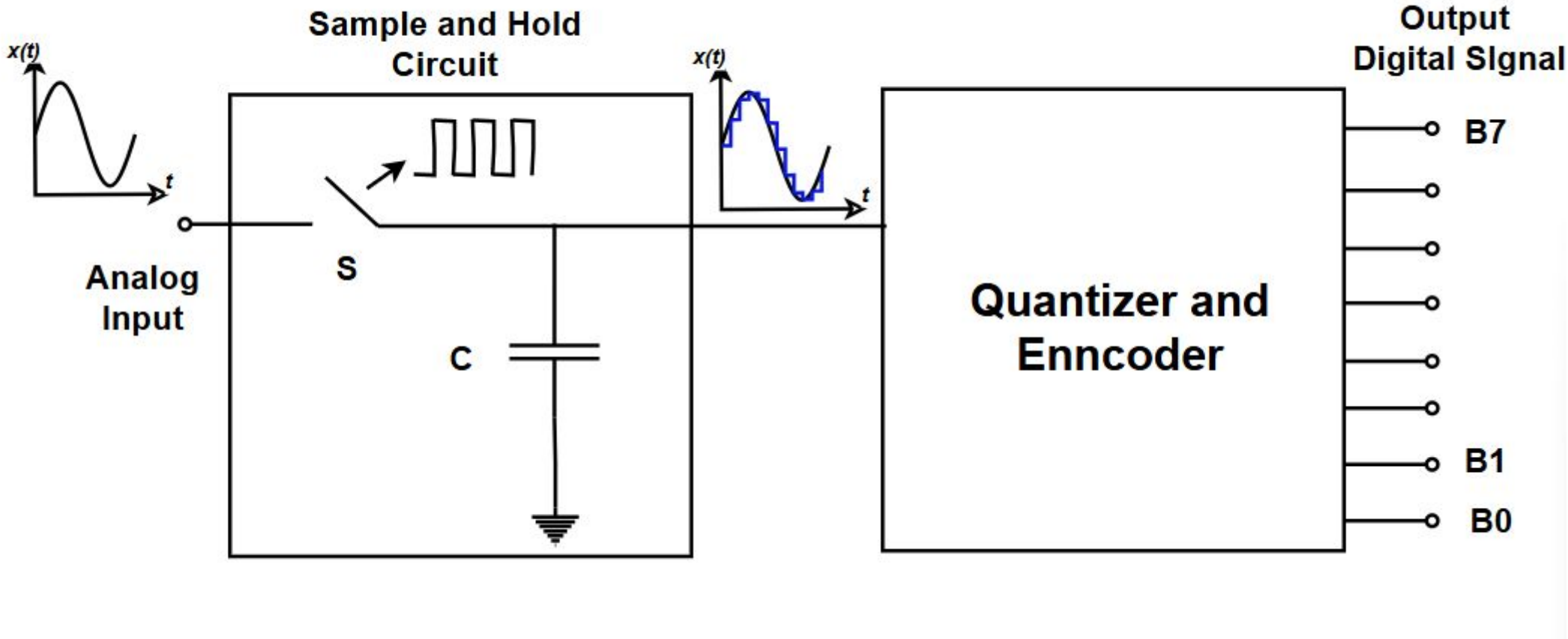
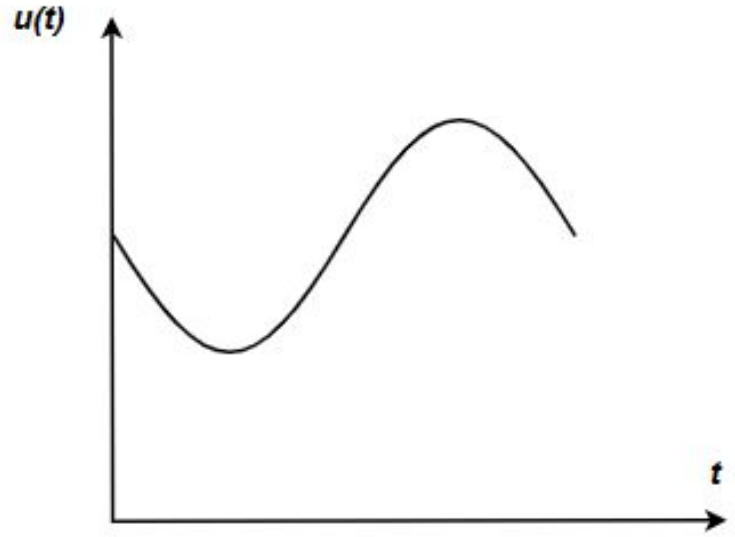
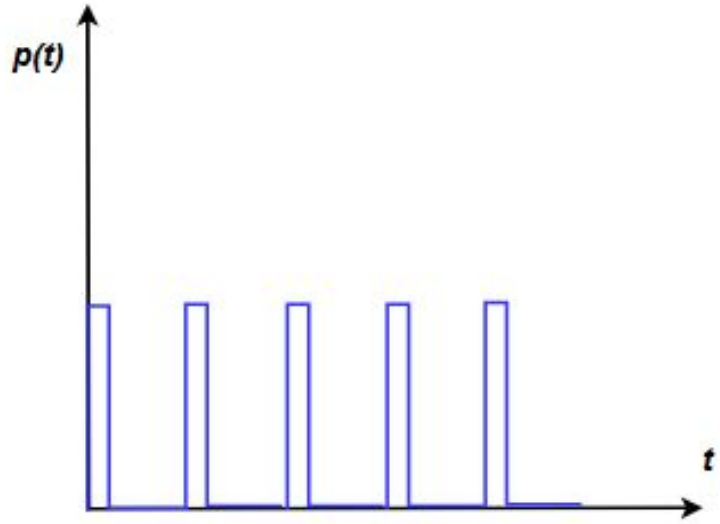
A/D conversion process



Sample and Hold Circuit





Quantization:

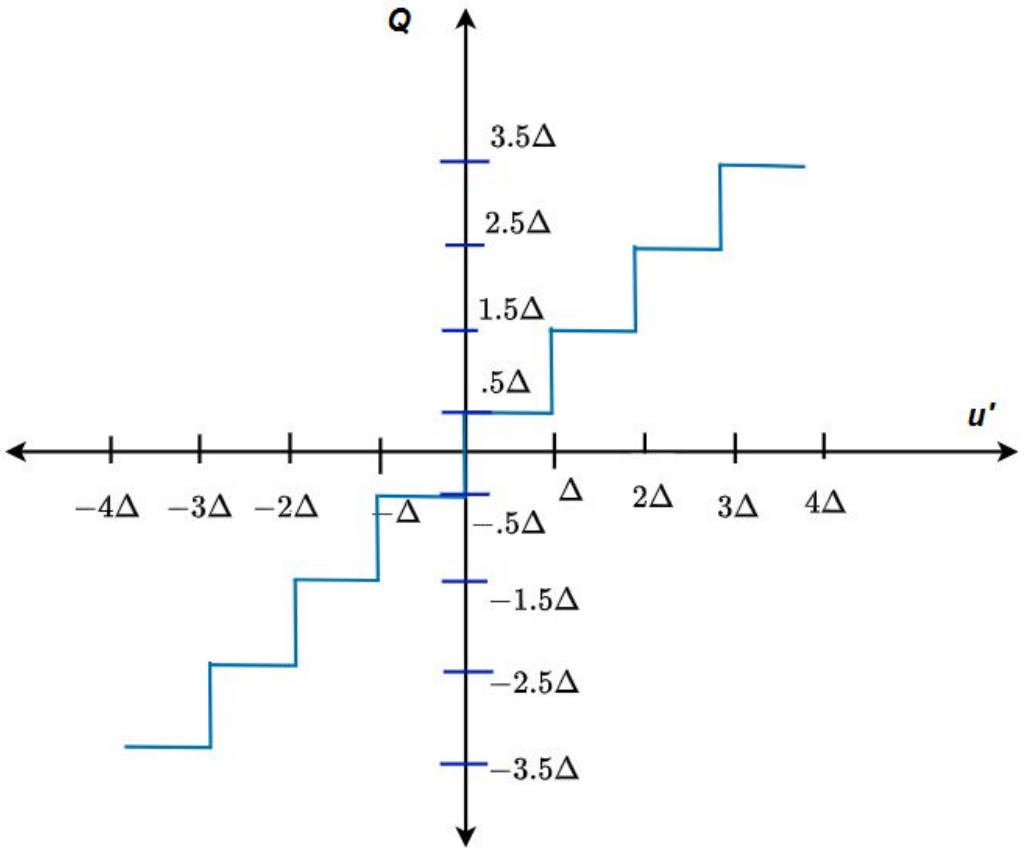
Quantization is a process by which we assign sampled and hold signal sata to some fixed preassigned values.

i. Midrise Quantization

ii. Midtread Quantization

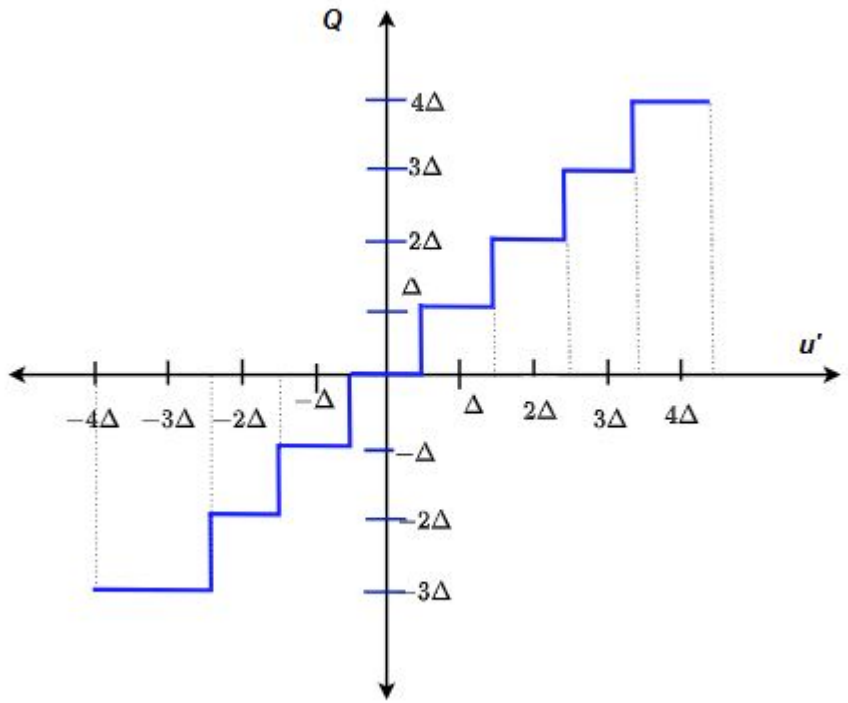
$$N = Number\ \ of\ bits$$
$$2^N = Number\ of\ levels$$
$$\Delta = \text{resolution} = \frac{\mathrm{V_{max}} - Vmin}{2^N}$$

Midrise Quantization:



Quantization Range	Quantization Level

Mid tread Quantization
(Not symmetrical and Equally Spaced)



Quantization Range	Quantization Level

Encoding

- We can choose binary values for each of the level.

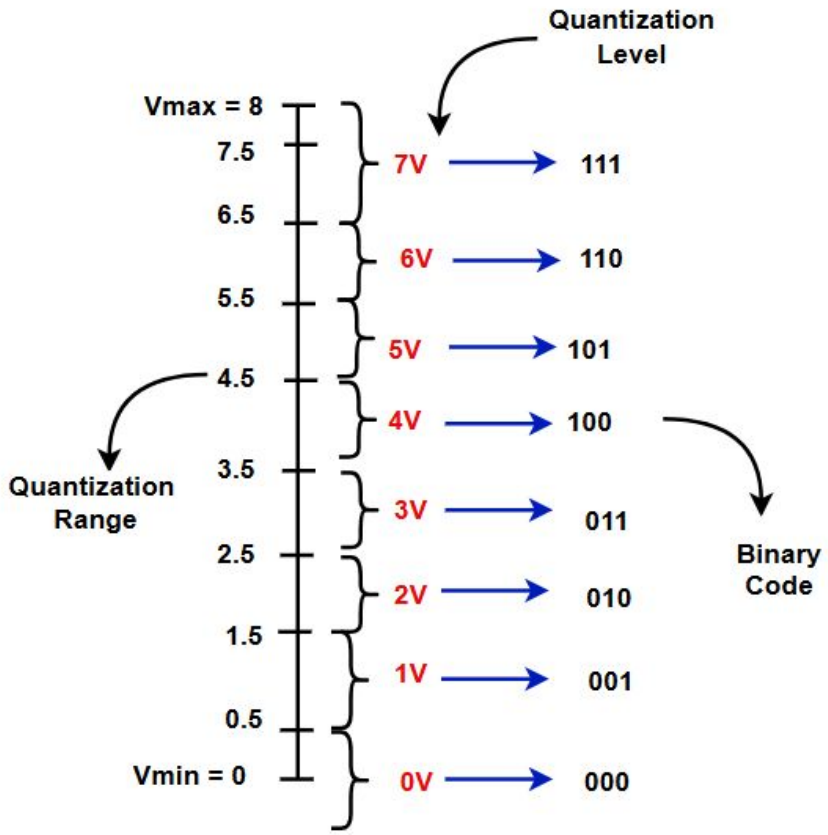
$$Number\ of\ bits = Ceil\ (log2(\ Number\ of\ levels\ ))$$

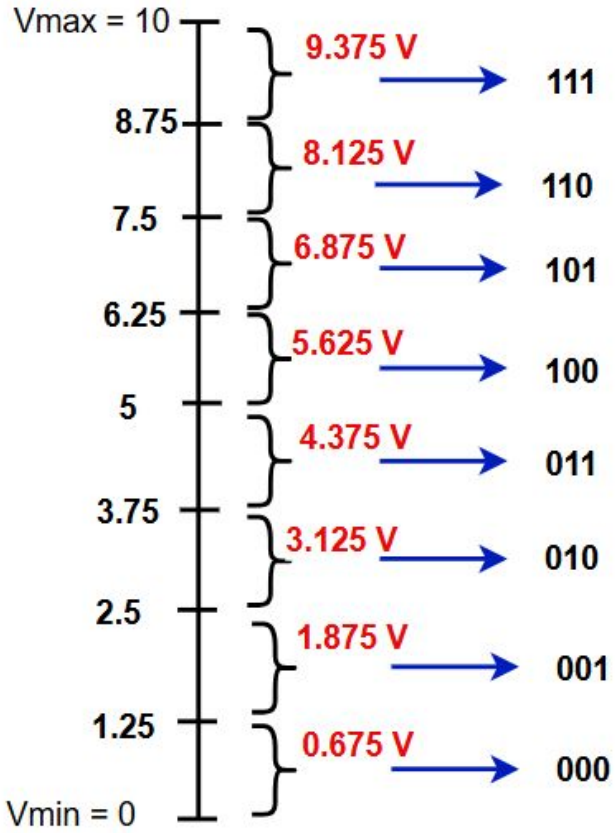
Assign lower Q level to 0

Then increase one for each next level

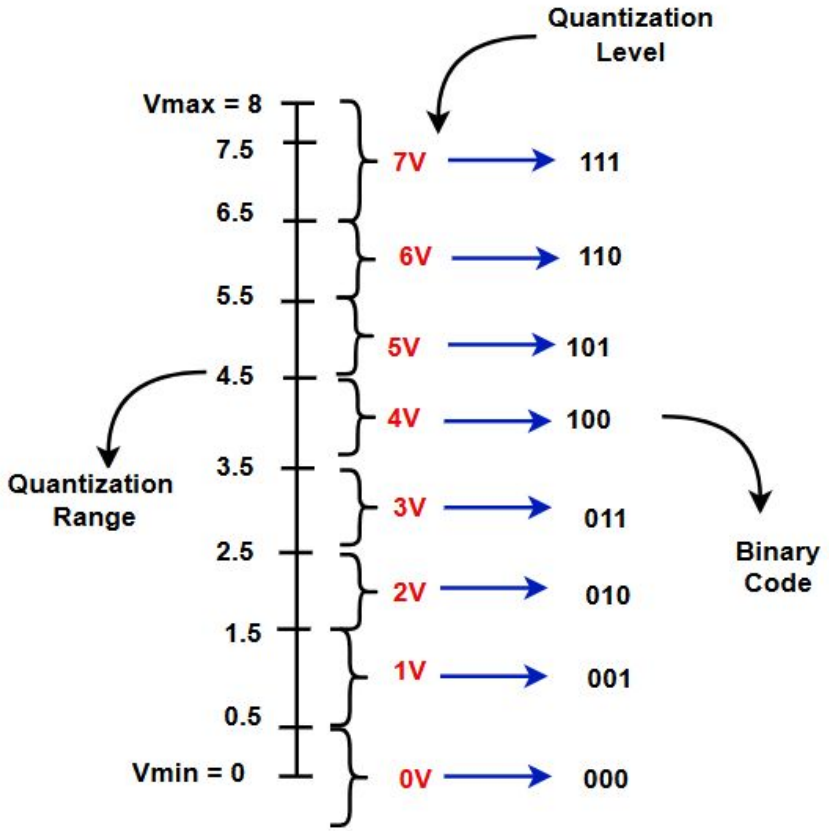
Quantization Range, Level, code

Ex: Identify which one is Mid rise and Mid tread.





Quantization Range, Level, code



Here,

$$\frac{Vmax + Vmin}{2} = \frac{8 + 0}{2} = 4\ V$$

As 4 V is a Quantization level. So, it is a mid tread quantization

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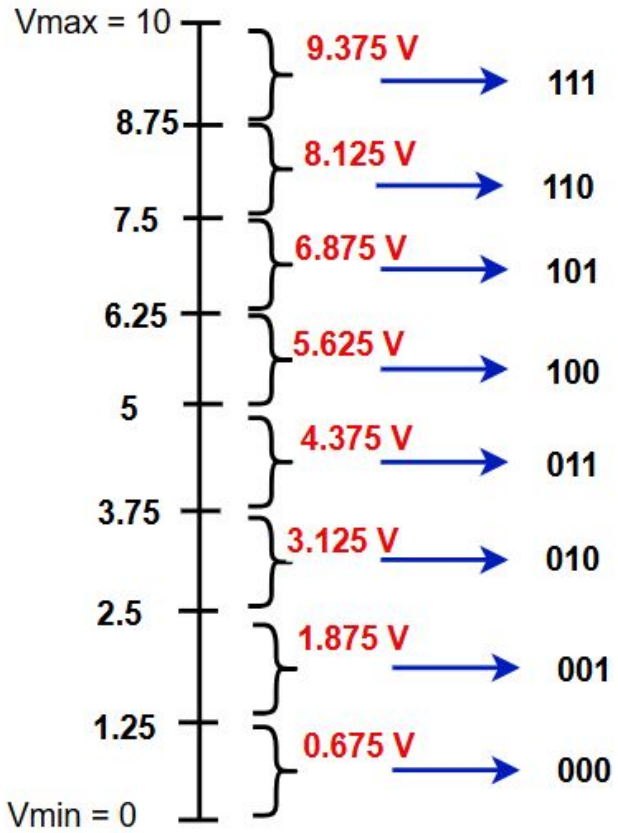
Quantization Range, Level, code

Ex: Identify which one is Mid rise and Mid tread.



Here,

$$\frac{Vmax + Vmin}{2} = \frac{10 + 0}{2} = 5\ V$$

As 5 V is not a Quantization level. So, it is a mid rise quantization

Flash A/D converter

Features of the Flash A/D converter

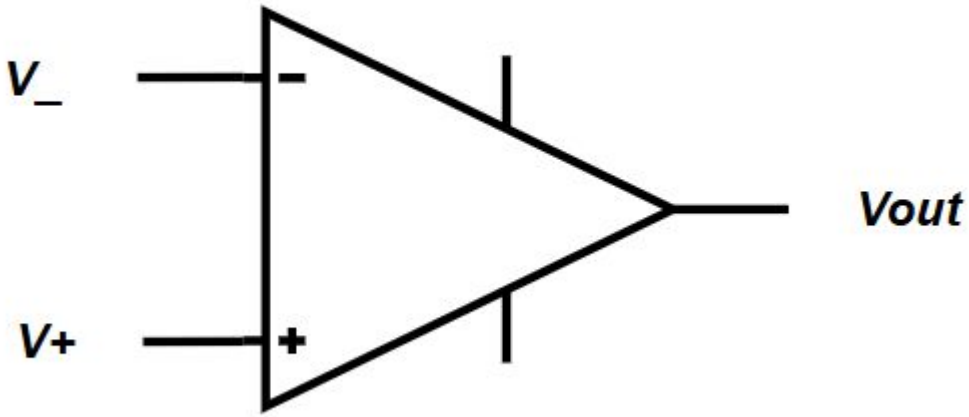
- ✔ This converter is very fast.
- ✔ It requires one clock cycle to convert the analog to digital data.
- ✔ It requires a lot components.

Op-Amp

For open loop configuration

$If\ V_+ > V\_\ , V_{out} = High\ (logic\ 1\ )$

$If\ V_+ < V\_\ , V_{out} = Low\ (logic\ 0\ )$



Flash ADC design

Suppose you have a signal with Vmax = 10 V and Vmin = 0V. Design a simple flash ADC converter. Use 3 bits for designing.

Flash ADC design

Suppose you have a signal with Vmax = 10 V and Vmin = 0V. Design a simple flash ADC converter. Use 3 bits for designing. Provide your encoder truth table.

Design:

Here,

$N = 3$

$\#Number\ of\ registor = 2^3 = 8$

$\#Number\ of\ comparator = 2^3 - 1 = 7$

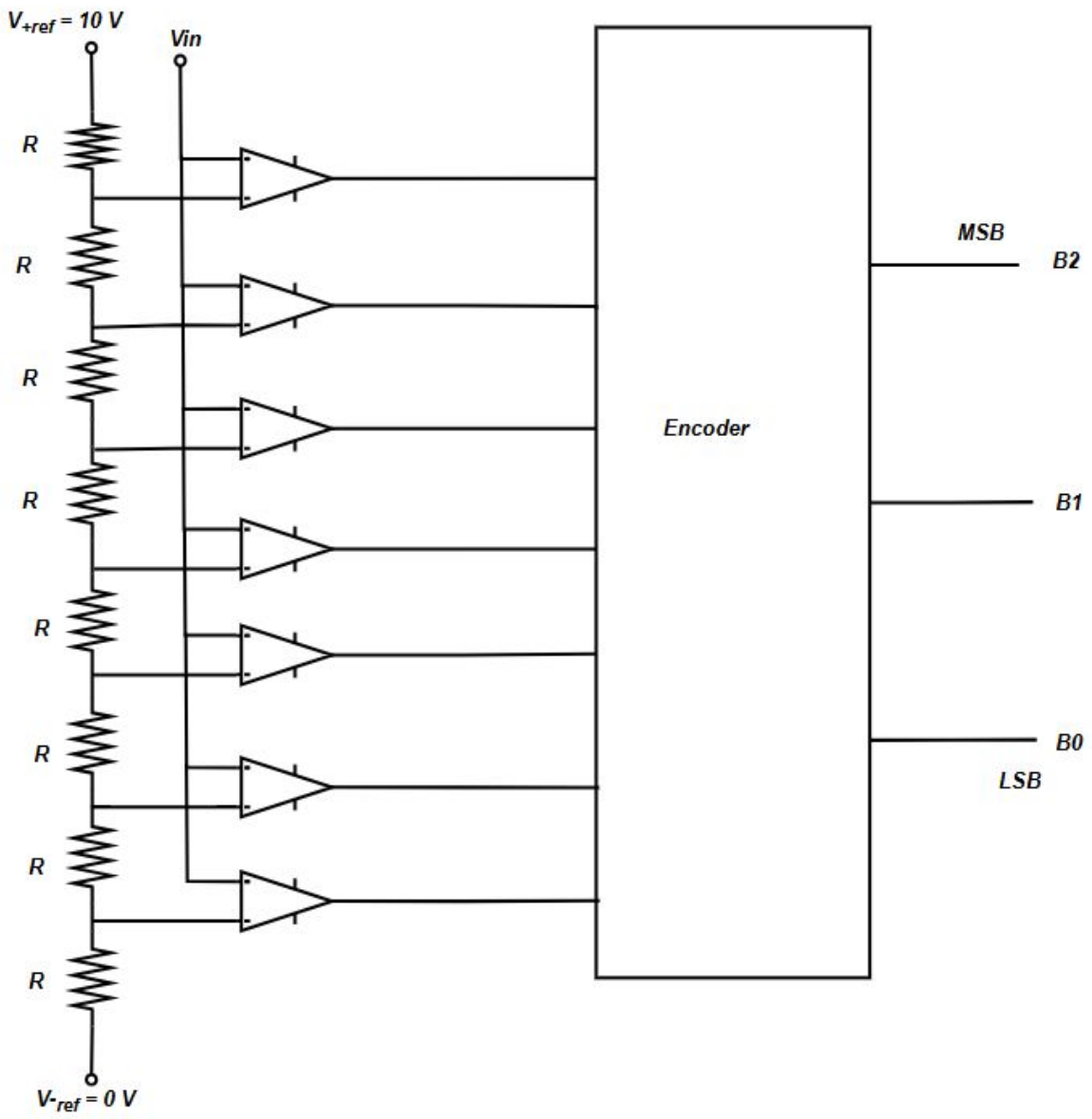
$V_{+ref} = Vmax = 10\ V$

$V_{-ref} = Vmin = 0\ V$

Circuit

The following is the Circuit of a 3 bits Flash ADC,

V+ of the comparator is connected to the input.



Circuit Analysis

The following is the Circuit of a 3 bits Flash ADC,

$$I = \frac{10 - 0}{8R} = \frac{10}{8R}$$

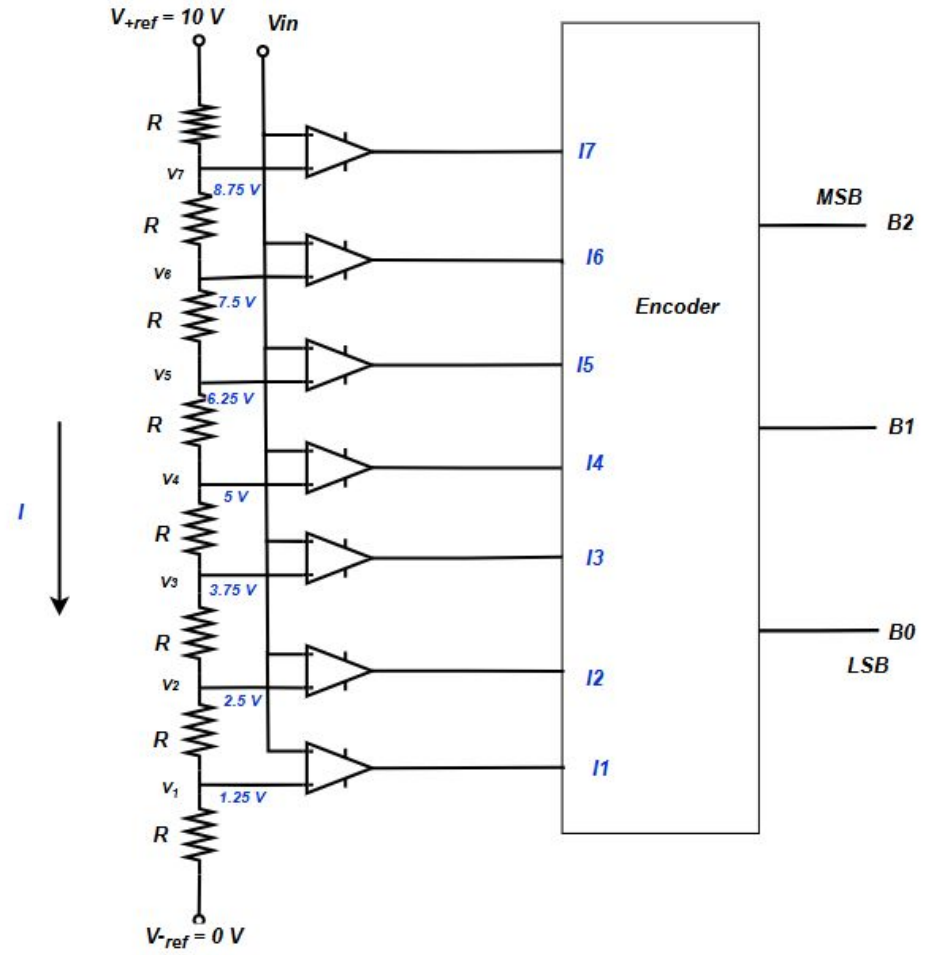
$$I = \frac{V1 - V_{-ref}}{R}$$

$$V1 = V_{-ref} + IR = 0 + \frac{10}{8R} * R = 1.25\,V$$

Similarly, $I = \frac{V2 - V1}{R} \Rightarrow V2 = V1 + IR$

$$\Rightarrow \quad V2 = 1.25 + \frac{10}{8R} * R = 2.5\,V$$

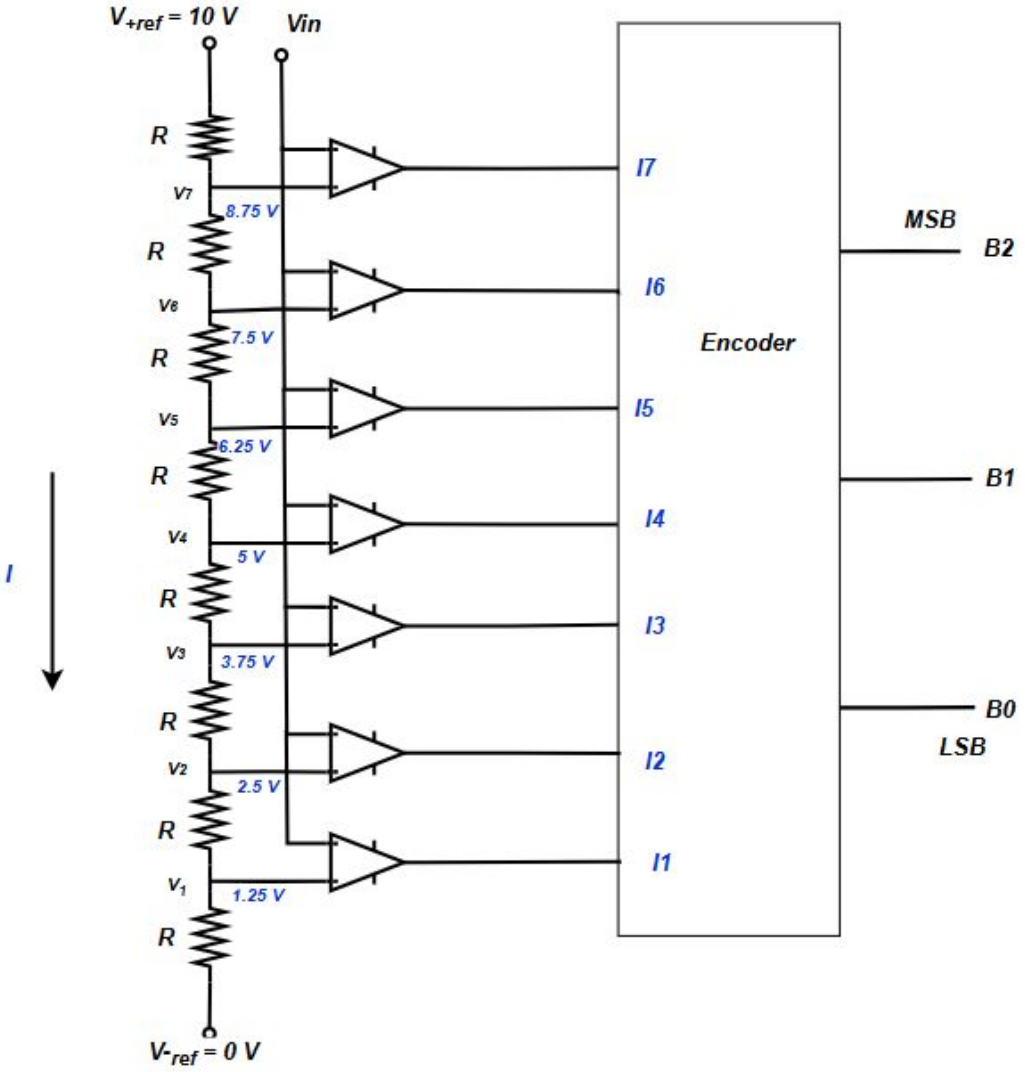
You can find other voltage in this way.



Circuit Analysis

Summary table:

Q Range	Q level	I7I6I5I4I3I2I1	Binary (B2B1B0)
0 - 1.25	0.675	000 000 0	
1.25 - 2.5	1.875	000 000 1	
2.5 - 3.75	3.125	000 001 1	
3.75 – 5	4.375	000 011 1	
5 – 6.25	5.625	000 111 1	
6.25 – 7.5	6.875	001 111 1	
7.5 – 8.75	8.125	011 111 1	
8.75 - 10	9.375	111 111 1	



Circuit Analysis

Encoder Truth Table:

(V+ of the comparator is connected to the Input)

Encoder can be implemented using the combinational network.

I7I6I5I4I3I2I1	Binary (B2B1B0)
000 000 0	000
000 000 1	001
000 001 1	010
000 011 1	011
000 111 1	100
001 111 1	101
011 111 1	110
111 111 1	111

Circuit Analysis

Encoder Truth Table:

(V- of the comparator is connected to the Input)

Encoder can be implemented using the combinational network.

I7I6I5I4I3I2I1	Binary (B2B1B0)
111 111 1	000
111 111 0	001
111 110 0	010
111 100 0	011
111 000 0	100
110 000 0	101
1 000 000	110
000 000 0	111

Problem:

Make a table with Quantization Range, Quantization Level and Binary values for the given ADC circuit.

What will be the final output if the input voltage $V_A = 2.125\ V$.

[VREF = 12 V]