CSE 350
Digital Electronics and Pulse Techniques

Transistor-Transistor Logic

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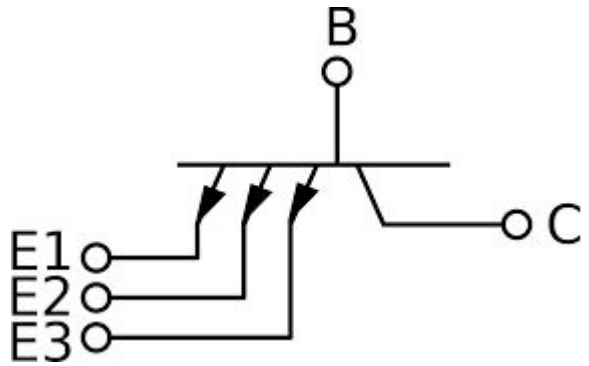
Transistor-Transistor Logic (TTL)

Transistor-Transistor Logic (TTL): TTL is a digital logic family that uses bipolar junction transistors (BJTs) for logic operations.

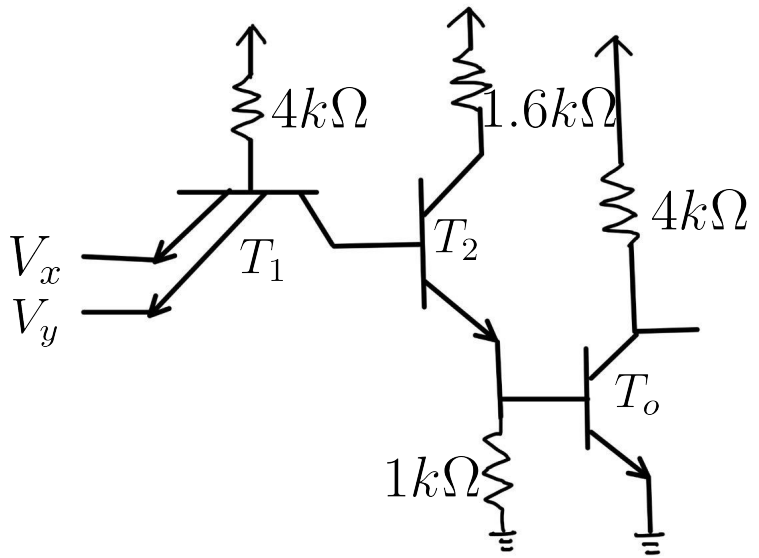
Multi-Emitter Transistors: A BJT with multiple emitters is shown here.

The operating mode of the BJT depends on the emitter voltages.



Transistor-Transistor Logic (TTL)

Operation of a TTL Circuit: Find the current and voltages involved in the following TTL circuit. Verify that it works like a NAND gate.



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TTL NAND Gate:

Logic Low: 0.1 V

Logic High : 5 V

We need to analyze the TTL NAND gate circuit for four different cases.

Transistor-Transistor Logic (TTL)

Case 01: $(\mathbf{0}, \mathbf{0}) \boldsymbol{V_x = 0.1\ V\ and\ V_Y = 0.1\ V}$

Transistors T_2 and T_0 will be in cutoff, just like $D_3\ and\ D_4$ in DTL circuit. However, to understand what will be the state of , we need to analyze a bit differently, since it's not a regular BJT. The two emitter BJT can be visualized as follows:

Thus, there are **two base-emitter junctions**. The voltage states in the four terminals are as shown in the figure. Thus, all the three junctions are forward biased.

Thus, we can assume that the transistor is operating in **saturation** mode.

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Now, $I_{C1} = -I_{B2} = 0, \quad I_{C2} = 0 = I_{E2} = I_{Co} = I_{Eo}$

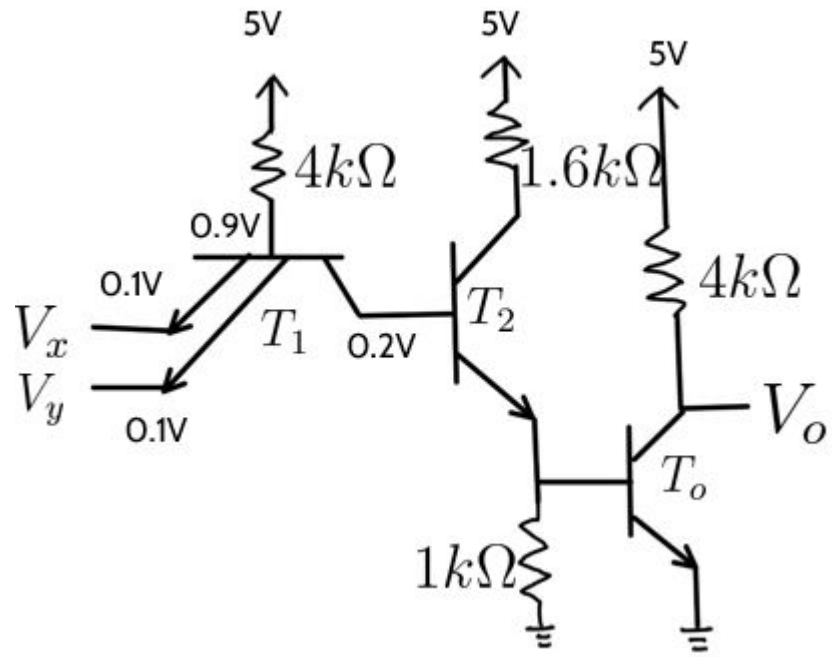
$V_o = 5\ V$

$$I_{B1} = \frac{5 - 0.9}{4k} = 1.025\ mA,$$

$$I_{E1x} = I_{E1y} = \frac{I_{B1}}{2} = 0.5125\ mA$$

We find, $\beta_{forced} = \frac{I_{C1}}{I_{B1}} = \frac{0}{1} = 0 < \beta_F$

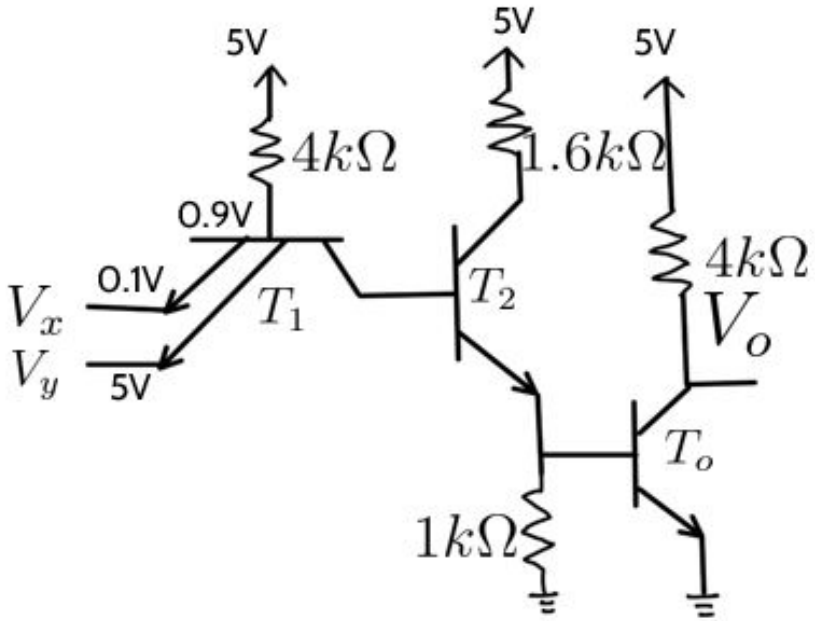
Thus, our assumption is valid.



Transistor-Transistor Logic (TTL)

Case 02: (01) $\boldsymbol{V_x = 0.1\ V\ and\ V_Y = 5\ V}$

This time, one of the emitter terminals of the multi-emitter transistor will have high voltage, and thus that B-E junction will be reverse biased, and off. Thus, current from base will only flow through the low input emitter. However, since there is still one B-E junction left in forward bias, we can assume here too that the transistor is in saturation. The analyses are quite similar except for the emitter currents of the input transistor.

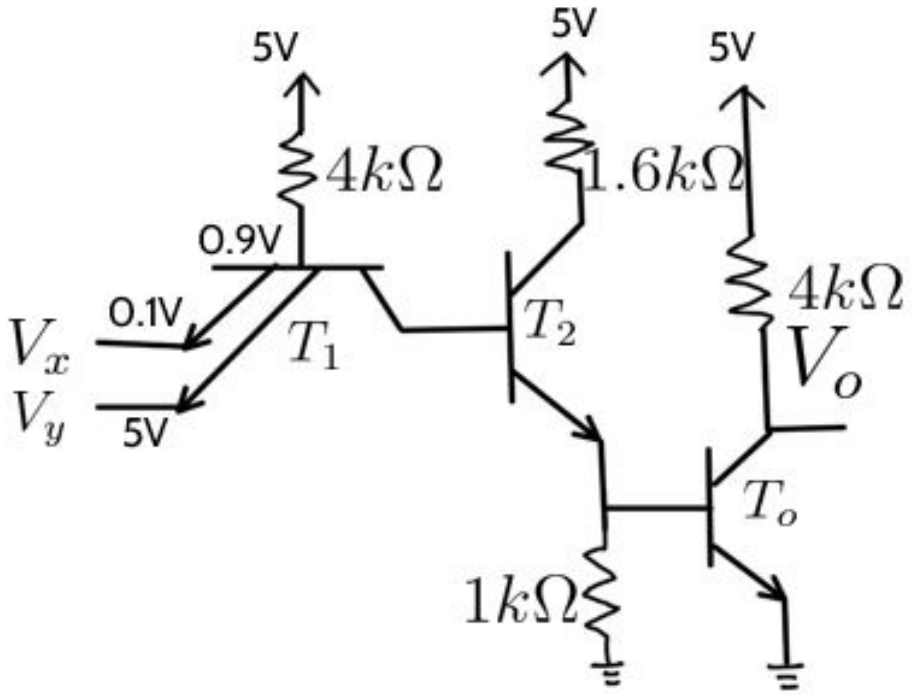


Transistor-Transistor Logic (TTL)

$$I_{B1}^{\cdot} = \frac{5 - 0.9}{4k} = 1.025\ mA$$

$$I_{E1x} = I_{B1} = 1.025\ mA$$

$$I_{E1y} = 0, V_o = 5\ V$$



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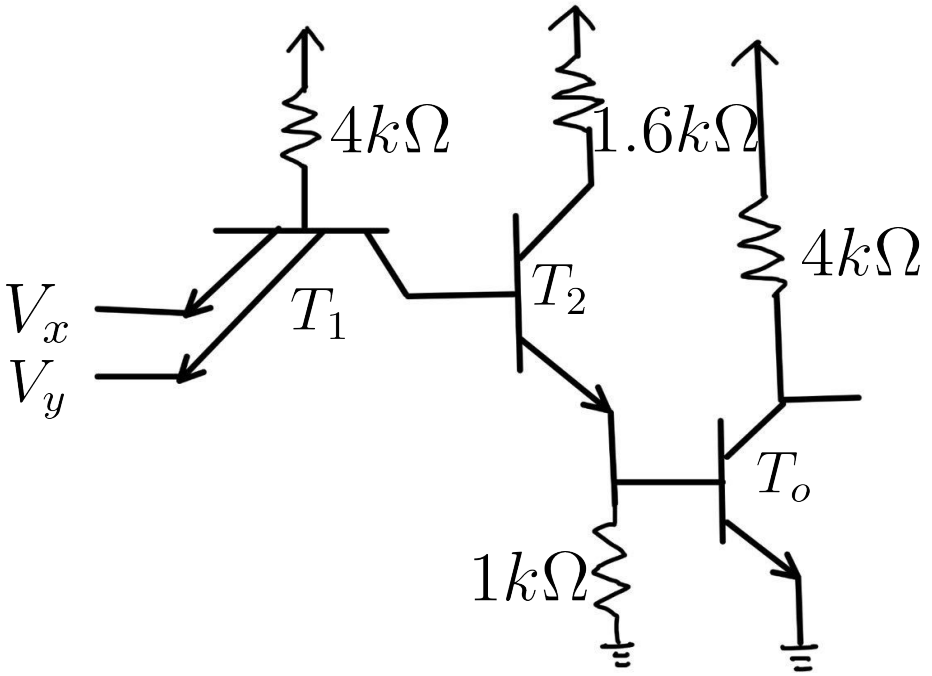
Case 03: (10) $\boldsymbol{V_x = 5\ V\ and\ V_Y = 0.1\ V}$

This is similar to the case 02.

$$I_{B1} = \frac{5 - 0.9}{4k} = 1.025\ mA$$

$$I_{E1y} = I_{B1} = 1.025\ mA$$

$$I_{E1x} = 0, V_o = 5\ V$$



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Case 04: (11) $\boldsymbol{V_x = 5\ V\ and\ V_Y = 5\ V}$

When both inputs are high, both the B-E junctions will be reverse biased, while the B-C junction will be forward biased. This corresponds to Reverse Active mode. The emitters & the collector of input transistor will switch their roles.

The other two transistors can be assumed to be in saturation

(since output logic will be 0), and it can be proved.

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In $R.A.$, we know that:

$$V_{BC_1} = 0.7\,\text{V}$$

Thus,

$$V_{B_1} = 2.3\,\text{V}$$

$$I_{B_1} = \frac{5-2.3}{4k} = 0.675\,\text{mA}$$

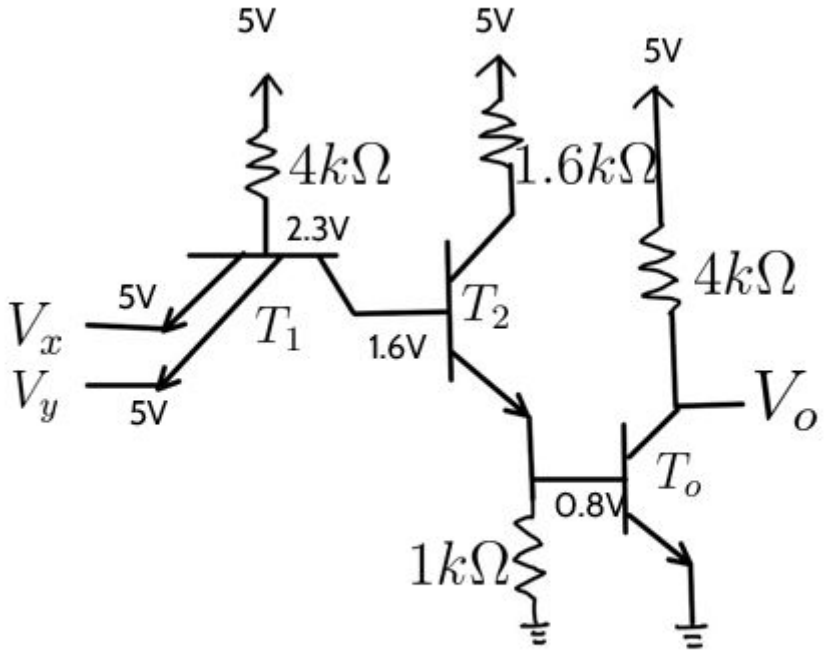
$$V_{CE_0} = 0.1\,\text{V} = V_O$$

$$V_{CE_2} = 0.1\,\text{V}$$

$$I_C = \frac{5-0.1}{4k} = 1.225\,\text{mA}$$

$$V_{C_2} = 0.8 + 0.1 = 0.9\,\text{V}$$

$$I_{C_2} = \frac{5-0.9}{1.6k} = 2.5625\,\text{mA}$$



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Say it is given, $\beta_R = 0.1$

$\beta_F = 25$

Then, $I_{B_o} = I_{E_2} - \frac{0.8}{1k} = 2.5725mA$

$I_{E_{1x}} = I_{E_{1y}} = I_{B_1} * \beta_R = 0.0675mA$

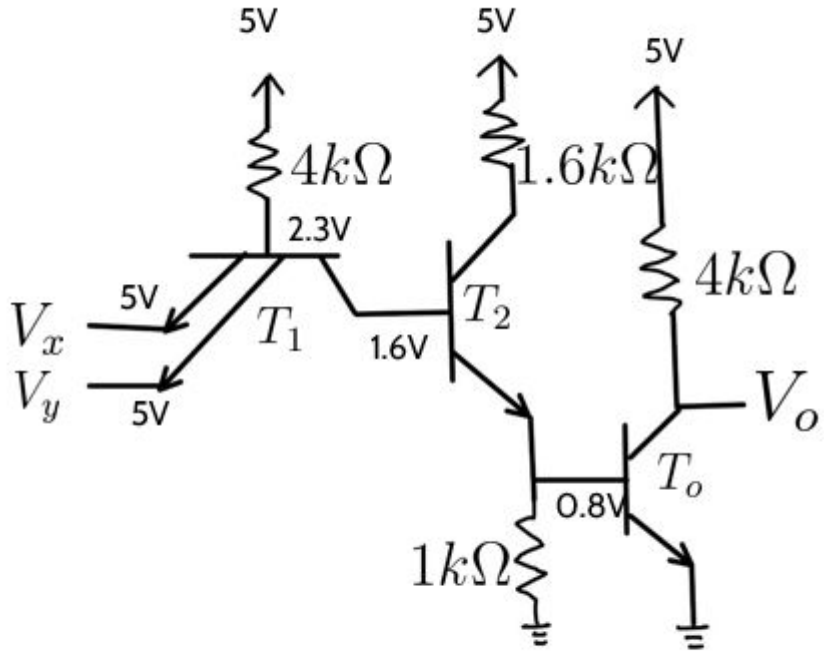
$I_{C_1} = I_{B_1} + I_{E_{1x}} + I_{E_{1y}} = 0.675 + 2 * 0.0675 = 0.81mA = I_{B_2}$

$I_{E_2} = I_{B_2} + I_{C_2} = 3.3725mA$

$I_{E_o} = I_{B_o} + I_{C_o} = 3.7975mA$

$\beta_{forced_{T_o}} = \frac{I_{C_o}}{I_{B_o}} = 0.36 < 25$

$\beta_{froced_{T_2}} = \frac{I_{C_2}}{I_{C_2}} = 3.16 < 25$



Thus our assumptions were valid.