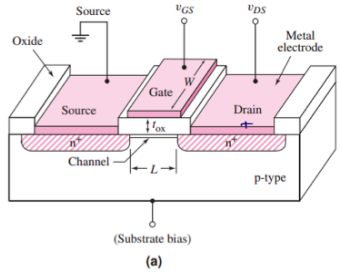
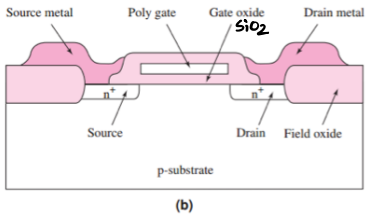
Lecture 15 : MOS Logic Families 1

MOSFET: Metal oxide semiconductor field effect Transistor.

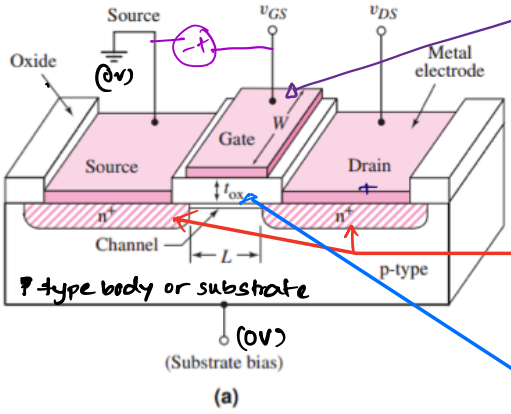
- gate (input terminal)
- SiO_2 (Silicon di-oxide)
- body and source/drain
- Electric field causes current flow



MOSFET	BJT
Drain	Collector
Gate (input)	Base (input)
Source	Emitter
N-type MOSFET	NPN-type BJT



Enhancement type MOSFET (NMOS):

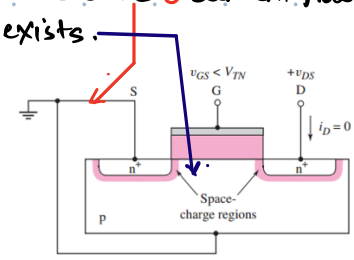


③ A polysilicon gate was constructed on top of SiO_2 to ensure no current flow between gate and body

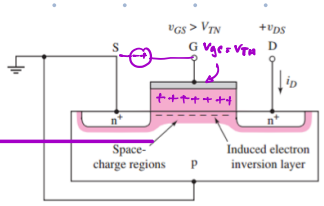
① • In a P-type body, two n^+ diffusion (n-type) are constructed.
Hence 2 P–n junctions get created
• These n^+ diffusions are called source and Drain terminal. Since MOSFET is symmetrical, these two terminals can be interchanged.

② Over the n^+ diffusion, there was a thin layer of di-electric or insulator (SiO_2). with thickness t_{ox}.

4. Body and Source is connected to the same Potential to ensure 0 current flow.
5. In an enhancement type MOSFET, initially no channel exists.
6. Need to create a channel to ensure current flow or conduction, an external electric field / voltage is applied between gate and Source, Vgs.



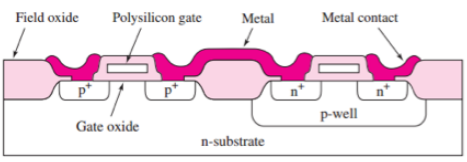
7. This Vgs is quite weak to attract the minority career or e^- in a p-type body. When $V_{gs} = V_{th}$, (here, V_{th} or V_{thn} (threshold voltage) is actually the applied V_{gs}) the applied voltage is strong enough to attract e^- towards gate. Due to SiO_2, these free e^- cannot recombine with +ve charge in gate and stored underneath the SiO_2. The stored e^- creates a bridge between both n^+ diffusion (source & Drain) and equal to the gate (+ve) charge. So, at $v_{gs} = V_{th}$ mosfet turns ON.

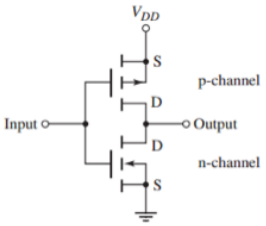


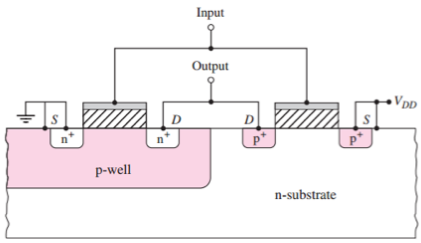
8. To create current flow between Drain & source, another electric field / voltage is applied between Drain and source. Vds.

Lecture 18 : CMOS Logic Families 2

CMOS Structure

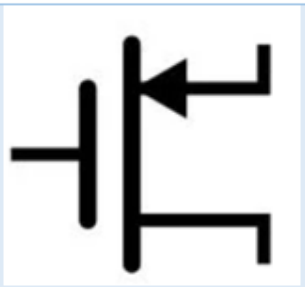






CMOS Transfer Characteristics

Summary:

	NMOS	PMOS
High Voltage at Gate	ON	OFF
Low Voltage at Gate	OFF	ON
Symbol	 Outward arrow	 Inward arrow

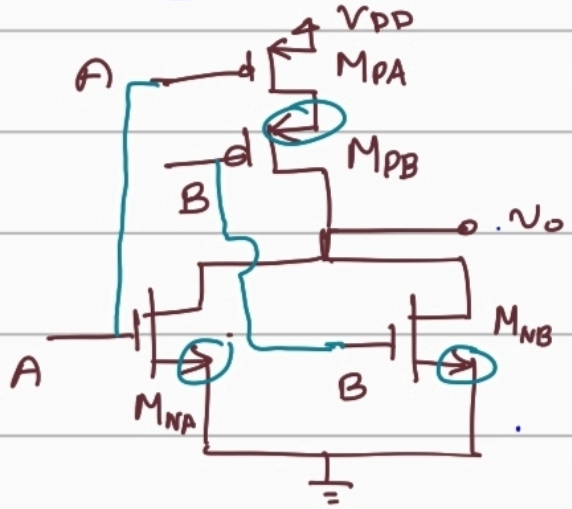
Logic circuits using CMOS

Rule 1: If the gate voltage is high/low then NMOS will turn ON/OFF and PMOS will turn OFF/ON. If any MOSFET turns on then drain and source terminal would be short circuited.

Rule 2: Conduction complement: We will design "pull-up network" using PMOS as the conduction complement of "pull-down network" using CMOS.

- Conduction complement means if NMOS are in series/parallel connection then PMOS are going be in parallel/series.
- Pull-up network rises the output level to the logical high voltage.
- Pull down networks declines the output level to the logical low voltage.

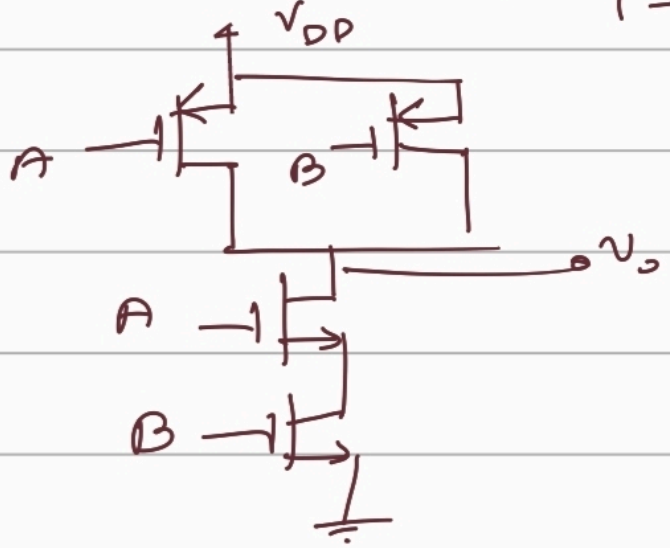
Example: CMOS NOR GATE: $Y = \overline{A+B}$



A	B	M_{PA}	M_{PB}	M_{NA}	M_{NB}	V_o
0	0	ON	ON	OFF	OFF	V_{DD}
0	V_{DD}	ON	OFF	OFF	ON	0
V_{DD}	0	OFF	ON	OFF	ON	0
V_{DD}	V_{DD}	OFF	OFF	ON	ON	0

CMOS NAND GATE

$Y = \overline{AB}$

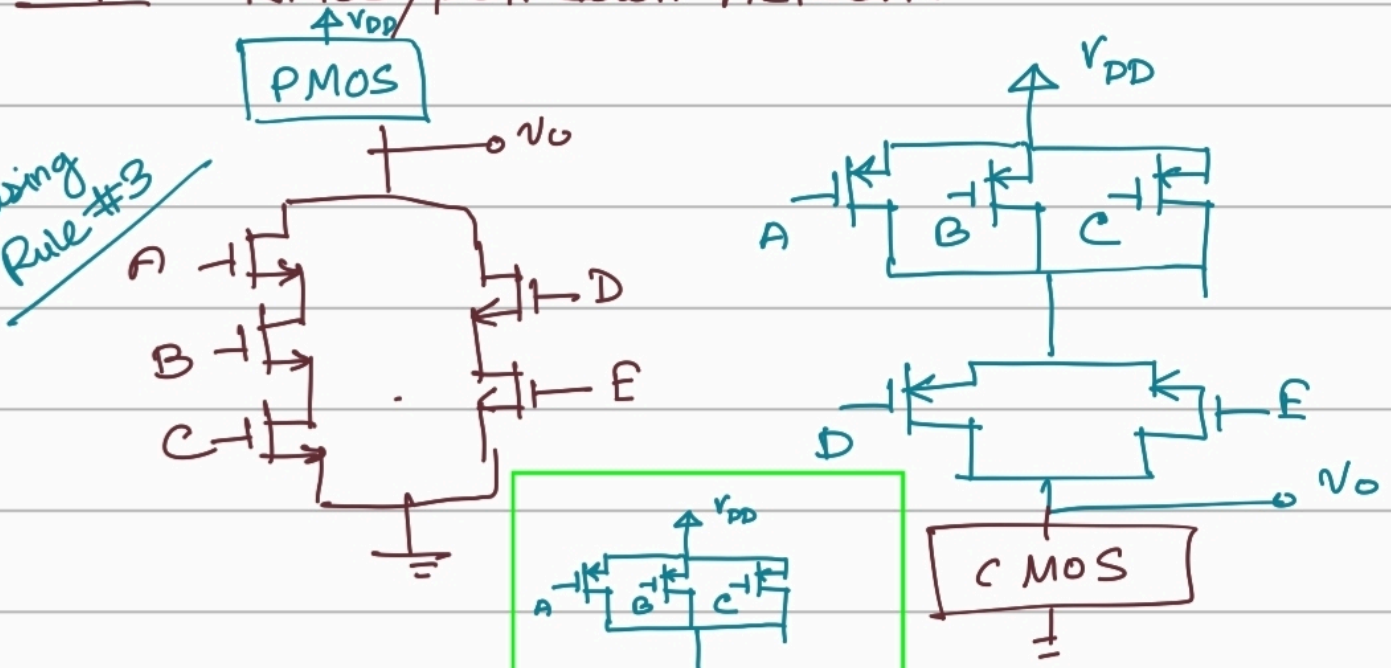


You can easily verify this works like a NAND gate.

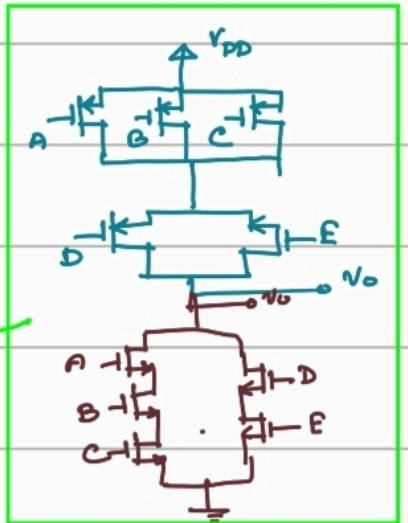
#Rule 3: In order to design pull-down network we must use series NMOS connection for AND logic and parallel NMOS connection for OR logic under the whole inverse sign.

Example: $Y = \overline{ABC + DE}$

Soln: NMOS/pull down network:



Total circuit.

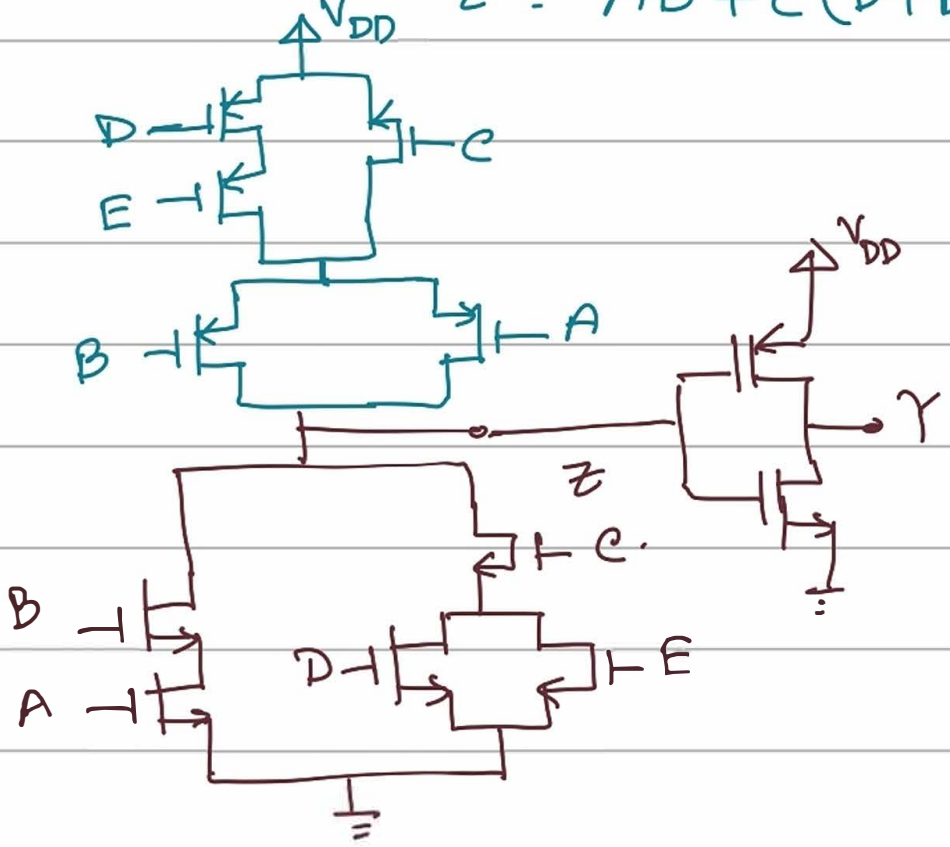


Example: 16.11

$$Y = AB + C(D+E)$$

$$Y = \overline{Z}$$

$$Z = \overline{AB + C(D+E)}$$



Switching up series connections doesn't change output.