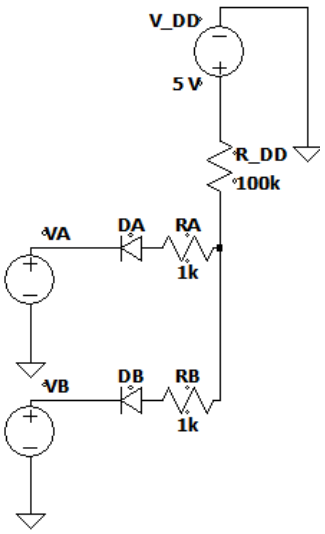
Basic Operation

Exercise 1



For the AND gate-

a) For logic case (1,0), find the output voltage & verify your assumption of the diode model used.
b) Find the current through R_{DD} for logic case (0,1).
c) If R_B is doubled, find the currents through the diodes for logic case (0,0).
d) Find the voltage of the node between D_B & R_B for the case in (c)

$Ans: a)\ 0.743\ V$

$b)\ 0.043\ mA$

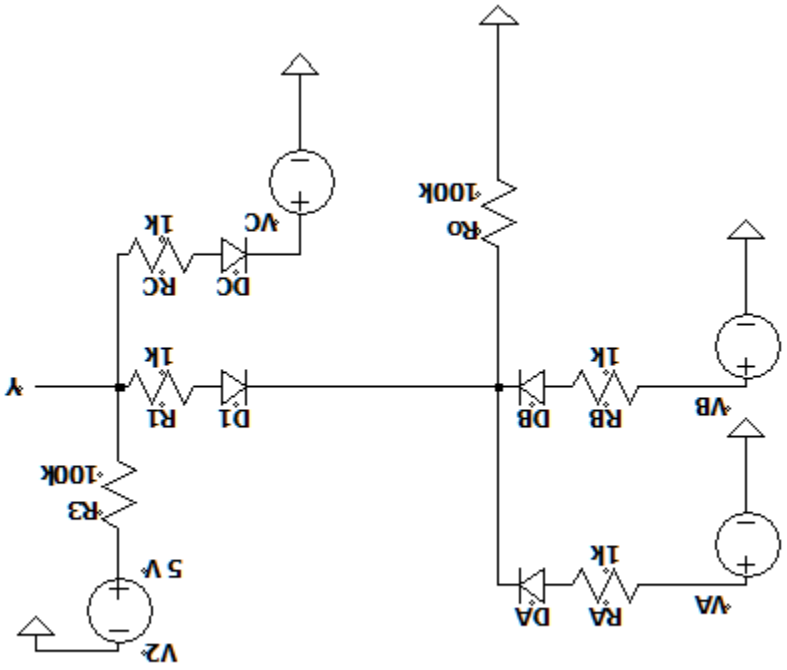
$c)\ 0.028\ mA, 0.014\ mA$

$d)\ 0.7\ V$

Practice Problem 1:

Implement the Boolean function, Y = (A+B)C using diode logic.

$Ans:$



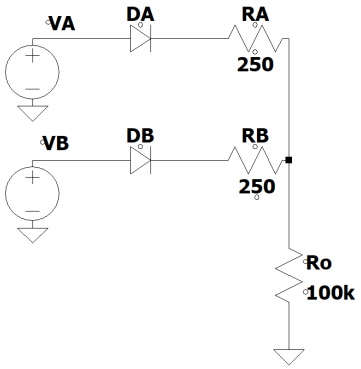
Exercise 2

Find the lower threshold voltage for the AND gate in **Exercise 1**, so that the output logic state can be determined correctly.

$Ans: 0.743\ V$

Power Dissipation

Exercise 3



Find the power dissipation for all input logic cases.

[High input = 5 V, Low input = 0.2 V]

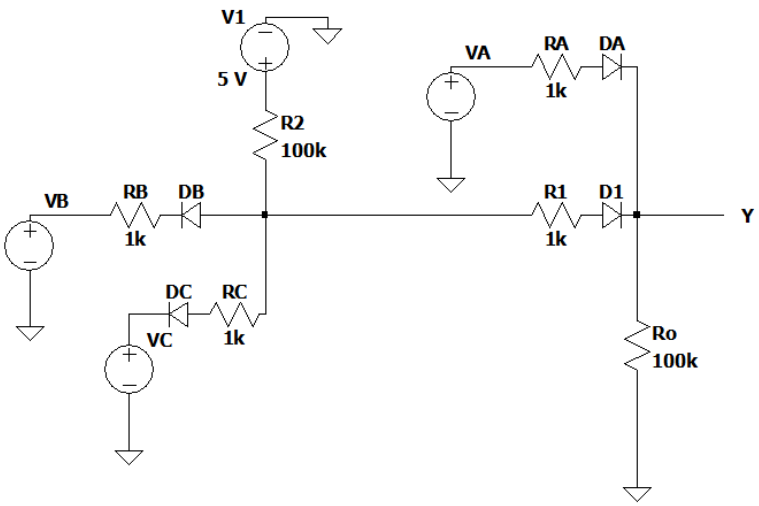
$Ans: 0\ mW, 2.145\ \mu W, 214.5\ \mu W, 214.5\ \mu W$

Practice Problem 2:

Find the maximum & average power dissipation for the OR gate in **Exercise 3**.

$Ans: 21.45\ \mu W, 16.0875\ \mu W$

Exercise 4



For the diode logic circuit given-

a) Find the Boolean expression of Y.
b) Determine the higher & lower threshold of output voltage.
c) Find the maximum & average power dissipation of the full circuit.

Ans:

$a)\ Y = A + BC$

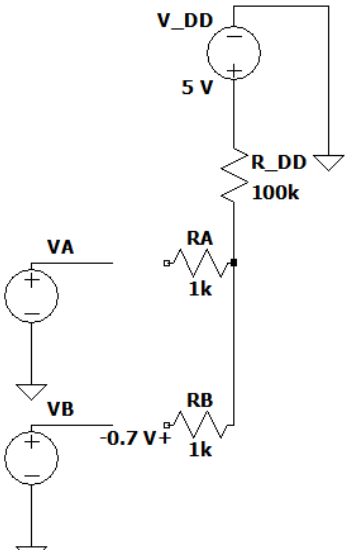
$b)\ 2.14\ V, 0\ V$

$c)\ 3.8\ mW, 0.742\ mW$

Exercise 1

Solution:

a) Assuming High input = $V_{DD} = 5\ V$ & Low input = $0\ V$, we assume, D_A will be off & D_B will be on for (1,0).



KCL gives, $I_{DD} = I_{DA} + I_{DB}$

$\rightarrow \frac{5-V_o}{R_{DD}} = 0 + \frac{V_o-(V_B+0.7)}{R_B}$

$\rightarrow \frac{5-V_o}{100} = \frac{V_o-0-0.7}{1} \rightarrow V_o = 0.743\ V$

Verification: Voltage across D_A, $V_{D_A} = (V_o - I_A \times R_A - V_A)$

$= (0.743 - 0 - 5) = -4.267 < 0.6\ V$

Voltage across D_B, $V_{D_B} = 0.7$

Also, the output voltage is lower than that of the high input.

b) For (0,1), D_A will be on & D_B will be off. However, since R_A & R_B are same, V_o will be the same. Now,

$I_{DD} = I_{DA} + I_{DB} = \frac{V_o-V_A-0.7}{R_A} + 0 = \frac{0.743-0-0.7}{1} = 0.043\ mA$

Note: This is also the current that is flowing through R_A.

c) Both diodes will be on in this case.

So, $I_{DD} = I_{DA} + I_{DB} = \frac{V_o-V_A-0.7}{R_A} + \frac{V_o-V_B-0.7}{R_B}$

$\rightarrow \frac{V_{DD}-V_o}{R_{DD}} = \frac{V_o-0-0.7}{1} + \frac{V_o-0-0.7}{2} \rightarrow \frac{5-V_o}{100} = \frac{3(V_o-0.7)}{2} \rightarrow V_o = 0.728\ V$

$$\therefore I_{DA} = \frac{V_o - 0.7}{R_A} = \frac{0.728 - 0.7}{1} = 0.028\, mA$$
$$\therefore I_{DB} = \frac{V_o - 0.7}{R_B} = \frac{0.7228 - 0.7}{2} = 0.014\, mA$$

d) Voltage of the node between $D_B \& R_B = V_B + 0.7 = 0 + 0.7 = 0.7\, V$

Exercise 2

Solution:

From **Exercise 1**, we found that the output voltage for (1,0) & (0,1) is 0.743V. The other case when the output voltage will be low is (0,0). For this, KCL gives,

$$I_{DD} = I_{DA} + I_{DB} \rightarrow \frac{V_{DD} - V_o}{R_{DD}} = \frac{V_o - V_A - 0.7}{R_A} + \frac{V_o - V_B - 0.7}{R_B}$$
$$\rightarrow \frac{5 - V_o}{100} = \frac{V_o - 0.7}{1} + \frac{V_o - 0.7}{1} \rightarrow V_o = 0.721\, V$$

Thus the lower threshold voltage of output for the AND gate $=$
$\max\left(V_{o_{0,0}}, V_{o_{0,1}}, V_{o_{1,0}}\right)$
$= \max(0.721, 0.743, 0.743) = 0.743\, V$

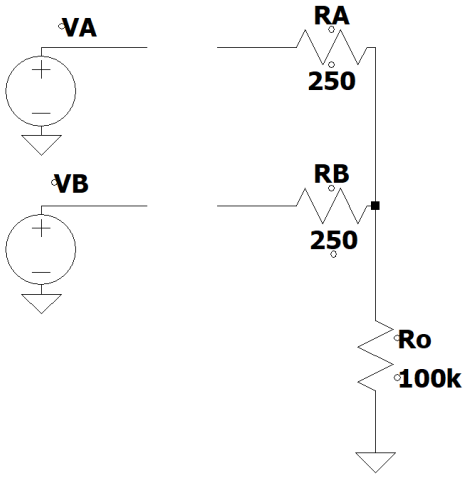
Exercise 3

Solution:

Step 1:

Case	DA	DB
0,0	Off	Off
0,1	Off	On
1,0	On	Off
1,1	On	On

(0,0):



Step 2:

$I_{DA} = I_{DB} = 0$

$\therefore I_o = I_{DA} + I_{DB} = 0$

$V_A = V_B = 0.2\ V$

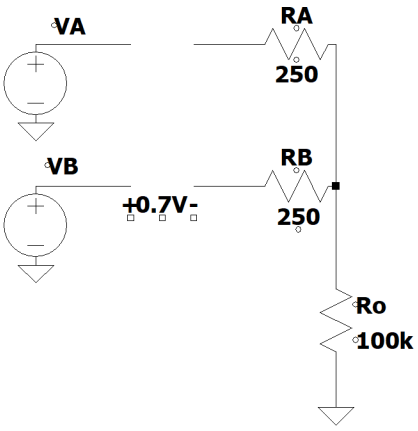
Both I_{DA}& I_{DB}flows from their respective sources to the ground.

Step 3:

$P = (V_A - 0) \times I_{DA} + (V_B - 0) \times I_{DB}$

$\therefore P_{0,0} = (0.2 - 0) \times 0 + (0.2 - 0) \times 0 = 0\ W$

(0,1):



Step 2:

$I_{DA} = 0\ , I_{DB} = \frac{V_B - 0.7}{250 + 100 \times 10^3} = \frac{5 - 0.7}{100250} = 42.9\ \mu A$

$V_A = 0.2\ V, V_B = 5\ V$

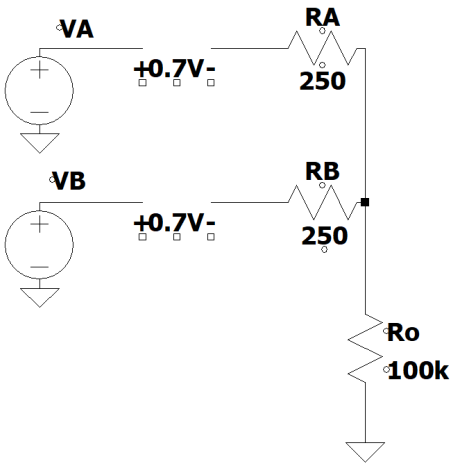
Step 3:

$P = (V_A - 0) \times I_{DA} + (V_B - 0) \times I_{DB}$

$\therefore P_{0,1} = (0.2 - 0) \times 0 + (5 - 0) \times 42.9 = 214.5\ \mu W$

(1,0) can be found similarly. Note that both the diode branches have the same resistances & input voltages. Hence, the result for (1,0) will be the same as (0,1). If those were not the same, the results would differ.

(1,1):



Step 2:

$I_{DA} = I_{DB} = \frac{V_A - 0.7 - V_o}{250}$, $I_o = I_{DA} + I_{DB} = \frac{V_o - 0}{100 \times 10^3}$

$\rightarrow 2 \times \frac{V_A - 0.7 - V_o}{250} = \frac{V_o - 0}{100 \times 10^3} \rightarrow V_o = 4.29\ V$

$\therefore I_{DA} = I_{DB} = \frac{V_o}{100 \times 2} = 21.45\ \mu A$

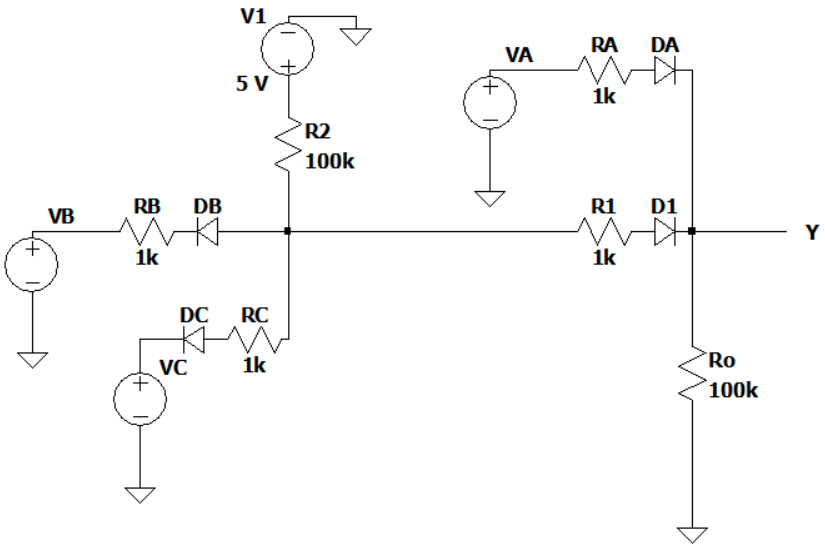
$V_A = V_B = 5\ V$

Step 3:

$P_{1,1} = (5 - 0) \times 21.45 + (5 - 0) \times 21.45$
$= 214.5\ \mu W$

Exercise 4

Solution:



a) Y = A + BC

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

b) Output voltage is high for the last 5 rows of input in the truth table.

Case (0,1,1):

$D_A, D_B \ \& \ D_C \ all \ are \ off, D_1 \ on$

Hence, KCL at the output voltage node of the AND gate, $V_{o(and)}$ gives,

$$I_{R2} = I_{DB} + I_{DC} + I_{R1} \rightarrow \frac{5 - V_{o(and)}}{100} = 0 + 0 + \frac{V_{o(and)} - V_Y - 0.7}{1}$$

$$\rightarrow 101\, V_{o(and)} - 100 V_Y = 75$$

KCL at Y gives,

$$I_{R1} + I_A = I_{R_o} \rightarrow \frac{V_{o(and)} - V_Y - 0.7}{1} = \frac{V_Y - 0}{100} \rightarrow 100 V_{o(and)} - 101 V_Y = 70$$

Solving the two equations, $V_{o(and)} = 2.86\, V, V_Y = 2.14\, V$

Case (1,0,0):

$D_A, D_B \& D_C \ all \ are \ on, D_1 \ can \ be \ assumed \ off \ (since \ output \ of \ AND \ gate \ is \ low)$

KCL at AND gate output node,

$$I_{R2} = I_{DB} + I_{DC} \rightarrow \frac{5 - V_{o(and)}}{100} = \frac{V_{o(and)} - 0 - 0.7}{1} \times 2 \rightarrow V_{o(and)} = 0.721\, V$$

KCL at Y,

$$I_{RA} = I_{R_o} \rightarrow \frac{5 - V_Y}{1} = \frac{V_Y - 0}{100} \rightarrow V_Y = 4.95\, V$$

Case (1,0,1):

$D_A, D_B \ on, D_C \ off, D_1 \ can \ be \ assumed \ off \ (since \ output \ of \ AND \ gate \ is \ low)$

KCL at AND gate output node,

$$I_{R2} = I_{DB} + I_{DC} \rightarrow \frac{5 - V_{o(and)}}{100} = \frac{V_{o(and)} - 0 - 0.7}{1} \rightarrow V_{o(and)} = 0.742\, V$$

KCL at Y,

$$I_{RA} = I_{R_o} \rightarrow \frac{5 - V_Y}{1} = \frac{V_Y - 0}{100} \rightarrow V_Y = 4.95\, V$$

Case (1,1,0): Same as Case (1,0,1)

Case (1,1,1):

$D_A, D_1\ on, all\ other\ diodes\ are\ off$

KCL at Y,

$I_{RA} + I_{R1} = I_{R_o} \rightarrow \frac{5-V_Y-0.7}{1} + \frac{5-V_Y-0.7}{101} = \frac{V_Y-0}{100} \rightarrow V_Y = 4.25\ V$

$\therefore V_{o(and)} = 5 - I_{R1} \times 100 = 5 - \frac{5-4.94-0.7}{101} \times 100 = 4.96\ V$

Thus, the higher threshold of output voltage =
$\min(V_Y\ of\ all\ high\ output\ cases) = 2.14\ V$

Output voltage is low for the first 3 rows of input in the truth table.

Case (0,0,0):

$D_A\ off, D_B \& D_C\ on, D_1 can\ be\ assumed\ off$

$(since\ the\ output\ of\ thte\ AND\ gate\ is\ low)$

KCL at AND gate output node,

$I_{R2} = I_{DB} + I_{DC} \rightarrow \frac{5-V_{o(and)}}{100} = \frac{V_{o(and)}-0-0.7}{1} \times 2 \rightarrow V_{o(and)} = 0.721\ V$

$V_Y = 0\ (since\ all\ diode\ branches\ connected\ to\ Y\ are\ open)$

Case (0,0,1):

$D_A\ off, D_B\ on, D_C\ off, D_1\ can\ be\ assumed\ off$

KCL at AND gate output node,

$I_{R2} = I_{DB} + I_{DC} \rightarrow \frac{5-V_{o(and)}}{100} = \frac{V_{o(and)}-0-0.7}{1} \rightarrow V_{o(and)} = 0.742\ V$

$V_Y = 0\ (for\ the\ same\ reason\ as\ previous\ case)$

Case (0,1,0): Same as Case (0,0,1)

Thus, lower threshold of output voltage $= \max(V_Y\ of\ all\ low\ output\ cases)$
$= 0\ V$

c) Power dissipation of all cases:

Case (0,0,0):

$P_{0,0,0} = (5-0) \times I_{R2} = 5 \times \frac{5-0.721}{100} = 0.214\ mW$

Case (0,0,1):

$P_{0,0,1} = (5-0) \times I_{R2} = 5 \times \frac{5-0.742}{100} = 0.213\ mW$

Case (0,1,0): Same as Case (0,0,1).

Case (0,1,1):

$P_{0,1,1} = (5-0) \times I_{R2} = 5 \times \frac{5-2.86}{100} = 0.107\ mW$

Case (1,0,0):

$P_{1,0,0} = (5-0) \times I_{R2} + (5-0) \times I_{RA} = 5 \times \left(\frac{5-0.721}{100} + \frac{5-4.95}{1}\right) = 0.464\ mW$

Case (1,0,1):

$P_{1,0,1} = (5-0) \times I_{R2} + (5-0) \times I_{RA} = 5 \times \left(\frac{5-0.742}{100} + \frac{5-4.95}{1}\right) = 0.463\ mW$

Case (1,1,0): Same as Case (1,1,0).

Case (1,1,1):

$P_{1,1,1} = (5-0) \times I_{R1} + (5-0) \times I_{RA} = 5 \times \left(\frac{4.96-4.25-0.7}{1} + \frac{5-4.25}{1}\right) = 3.8\ mW$

$\therefore Maximum\ Power\ Dissipation, P_{max} = 3.8\ mW$

$$\therefore Average\ Power\ Dissipation, P_{avg} = \frac{0.214+0.213\times2+0.107+0.464+0.463\times2+3.8}{8}$$

$$= 0.742\ mW$$