CSE 350
Digital Electronics and Pulse Techniques

RTL circuits

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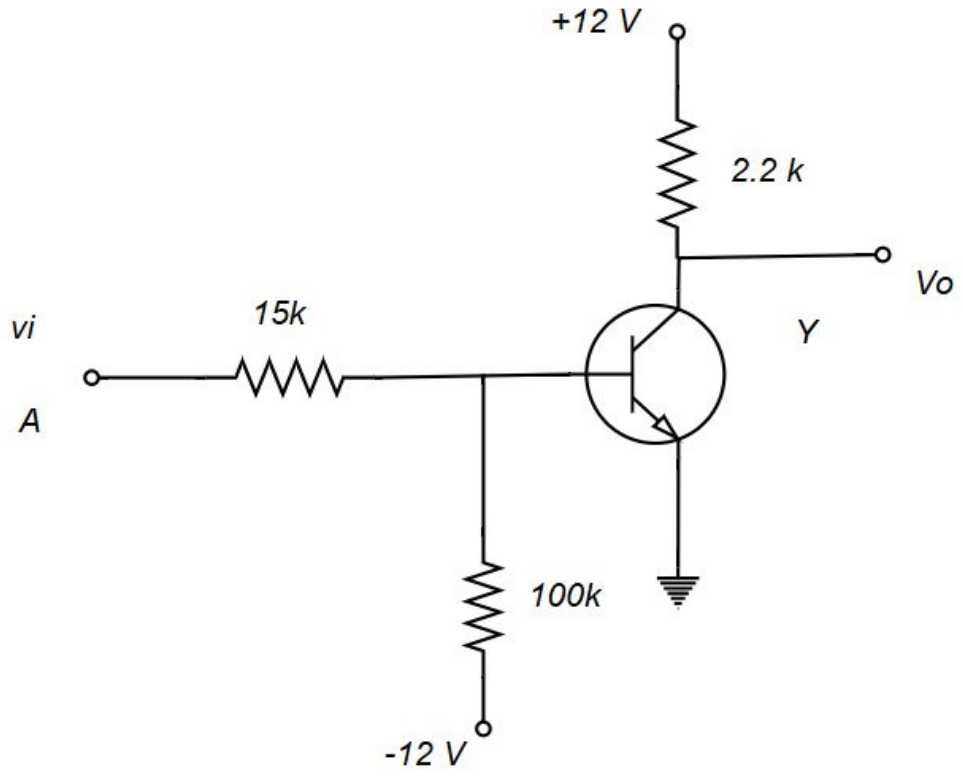
Resistor Transistor Logic (RTL)

Not gate



Resistor Transistor Logic (RTL)

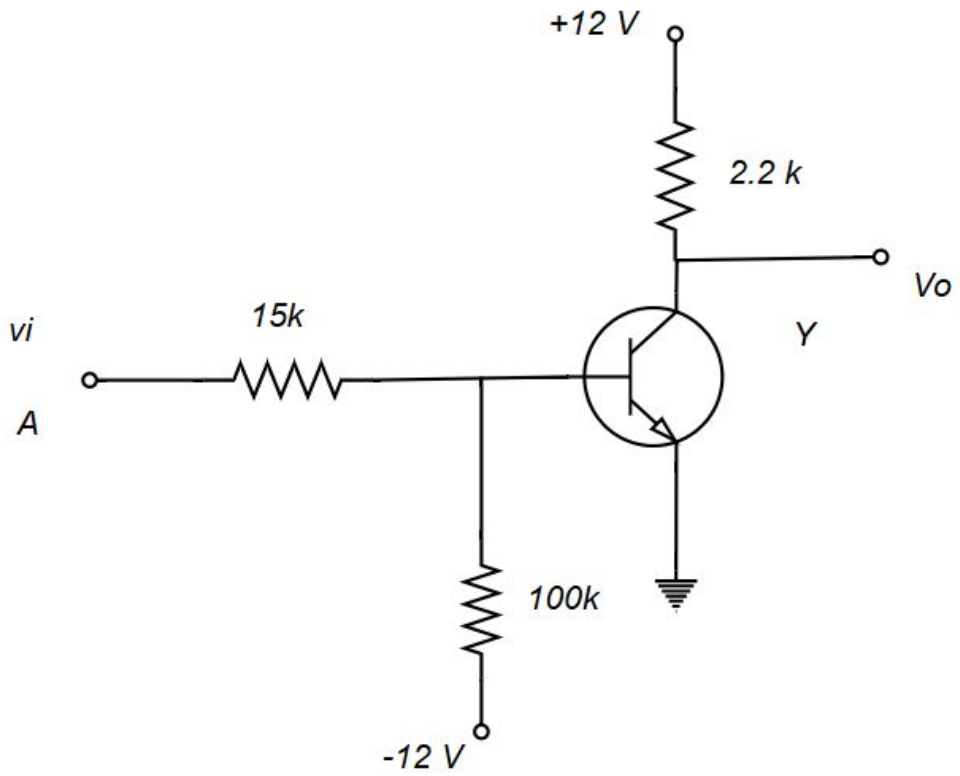
Case 1: A = 0 , vi = 0 V

input low, output

expected to be high.

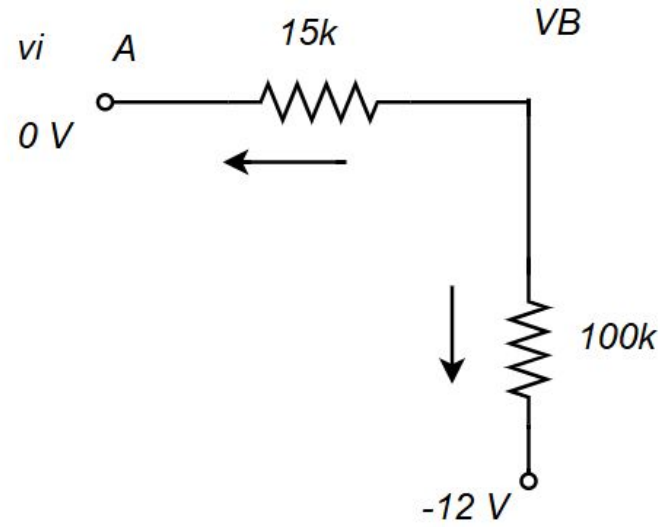
We need to prove it.

Assumption: Cutoff mode



Resistor Transistor Logic (RTL)

Verification



$$\frac{Vb-0}{15\ k}+\frac{Vb-(-12)}{100k}=0 => V_B=-1.565\ V\ ,$$

$$Here, V_E = 0$$

As V_{BE} = -1.565 V<0.7 V , | Assumption is correct

For cutoff mode: $I_B = I_C = I_E = 0$

$$Ic = 0 = \frac{12-Vc}{2.2\ k}\ , \qquad Vc = 12\ V$$

Resistor Transistor Logic (RTL)

Case 2: $A = 1, V_i = 12\ V$

input high, output

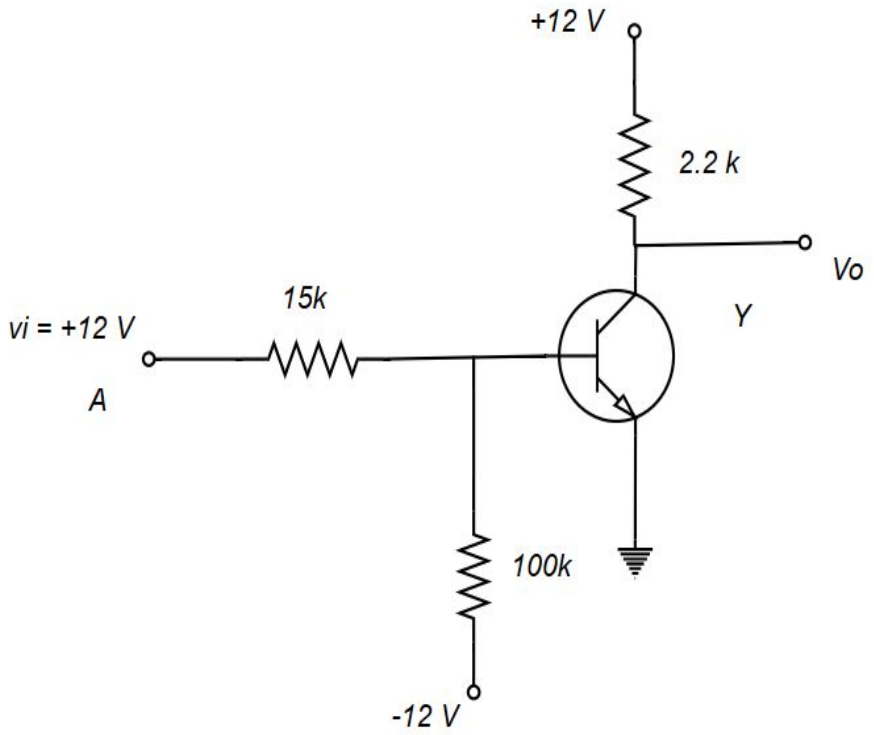
expected to be low.

$V_{CE} = 0.2\ V$

We can expect this BJT

to be operating in saturation mode.

Assumption: Saturation mode



Resistor Transistor Logic (RTL)

$$I_C = \frac{12 - 0.2}{2.2\ k} = 5.36\ mA$$

$$\boldsymbol{T \rightarrow Saturation}, V_{BE} = 0.8\ V\ and\ V_{CE} = 0.2\ V$$

$$I_1 = \frac{12 - 0.8}{15\ k} = 0.746\ mA$$

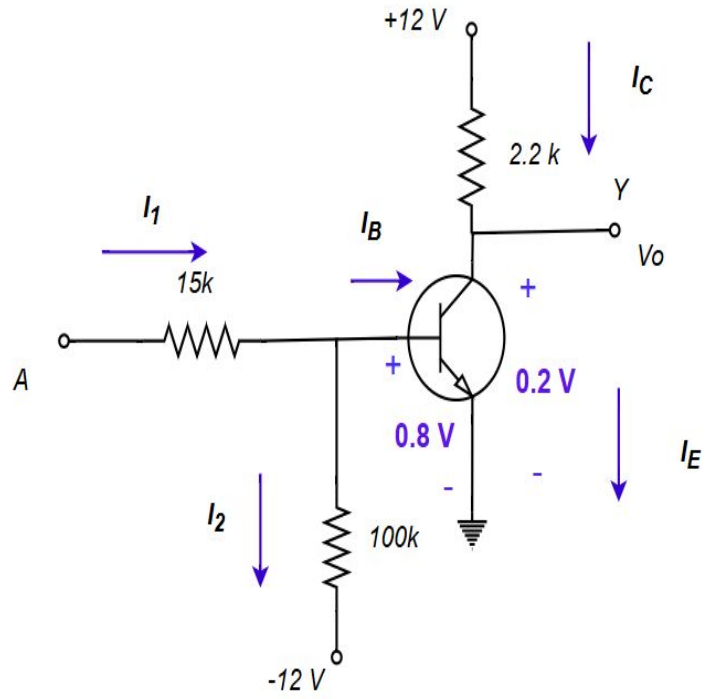
$$I_2 = \frac{0.8 - (-12)}{100\ k} = 0.128\ mA$$

$$I_B + I_2 - I_1 = 0$$

$$I_B = I_1 - I_2 = 0.619\ mA$$

$$Here, \beta_{forced} = \frac{I_C}{I_B} = 8.659 < \beta_F$$

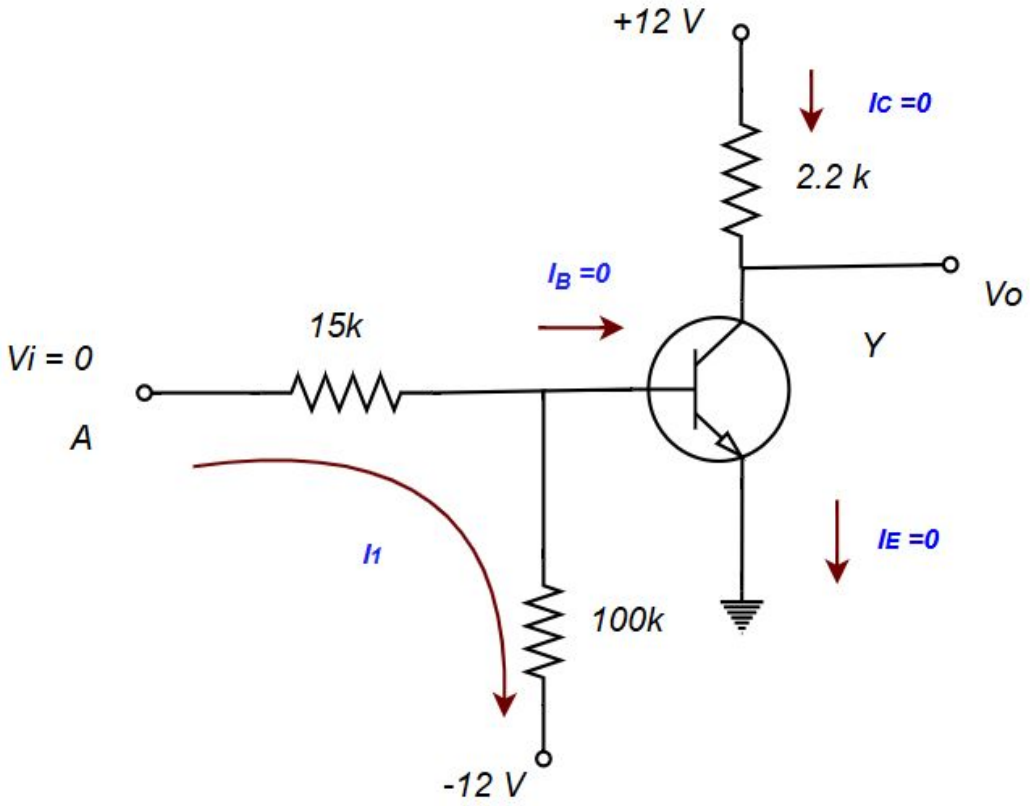
(Saturation assumption is correct)



Power dissipation for RTL inverters:

Case 01: T --> Cutoff mode

$$I_B = I_C = I_E = 0$$

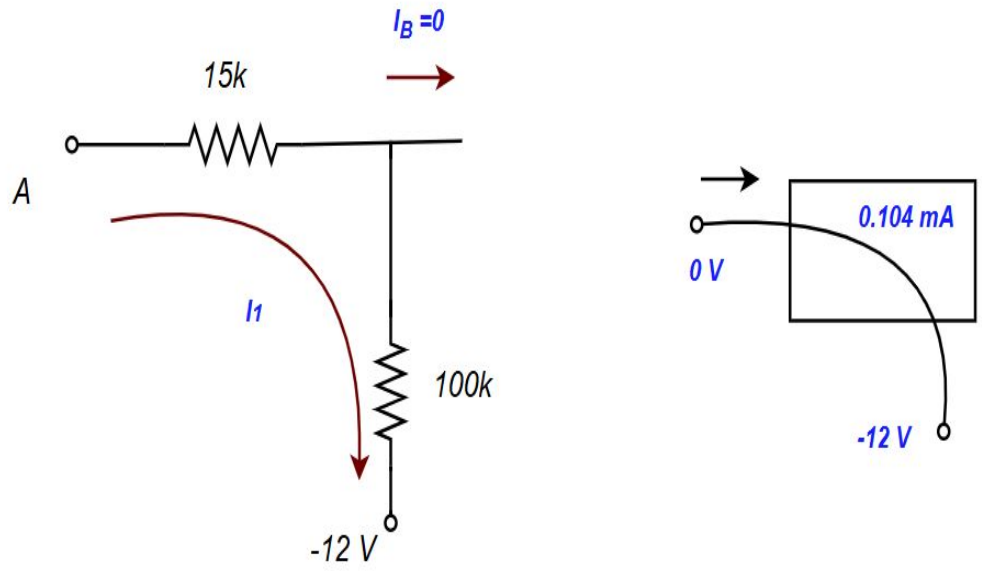


Power dissipation for RTL inverter

$$I_1 = \frac{0 - (-12)}{(100 + 15)\ k} = 0.104\ mA$$

Power dissipation,

$$P = (0 - (-12)) * 0.104 = 1.2521\ mW$$



Power dissipation for RTL inverter

Case 2: $A = 1, V_i = 12\ V$

input high, output

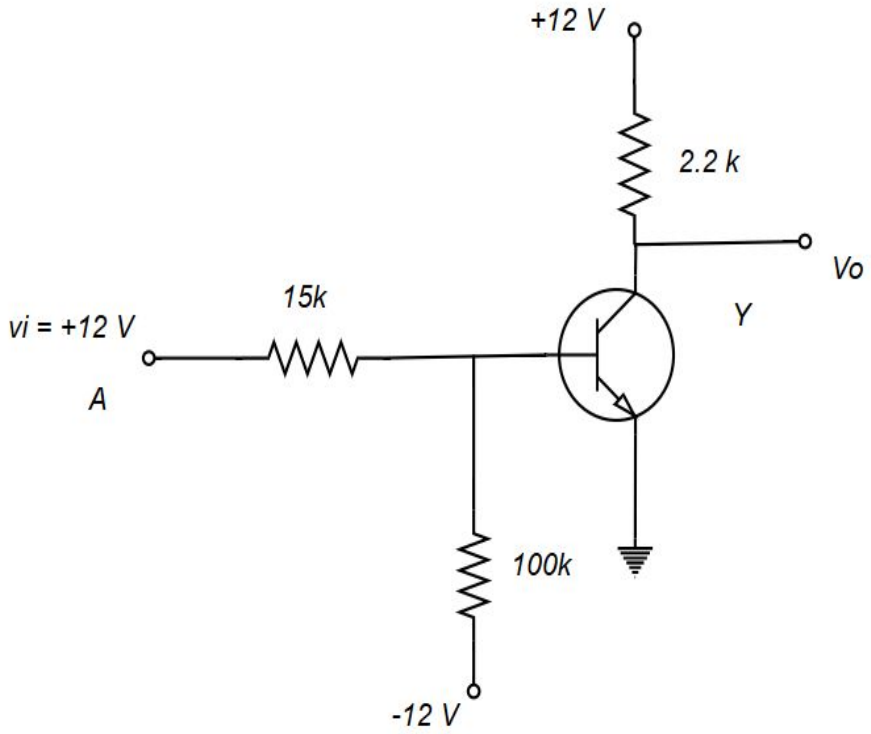
expected to be low.

$V_{CE} = 0.2\ V, V_{BE} = 0.8\ V$

We can expect this BJT

to be operating in saturation mode.

Assumption: Saturation mode



Power dissipation for RTL inverter

$$I_C = \frac{12 - 0.2}{2.2\ k} = 5.36\ mA$$

$\boldsymbol{T \rightarrow Saturation,}$

$V_{BE} = 0.8\ V\ and\ V_{CE} = 0.2\ V$

$$I_1 = \frac{12 - 0.8}{15\ k} = 0.746\ mA$$

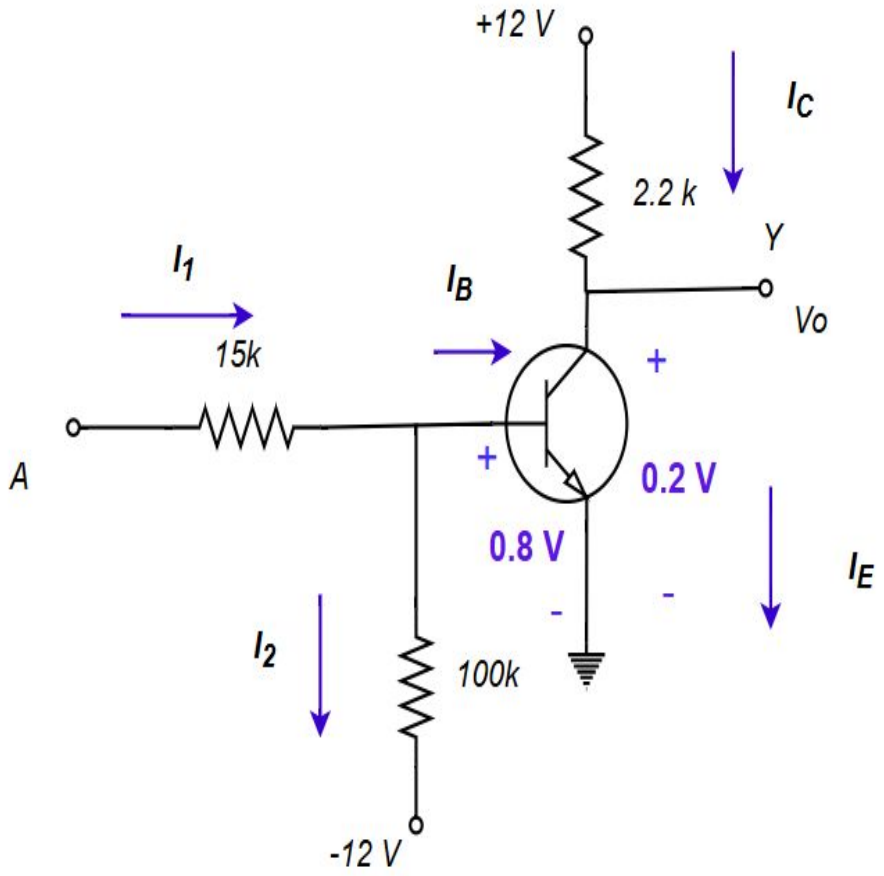
$$I_2 = \frac{0.8 - (-12)}{100\ k} = 0.128\ mA$$

$$I_B + I_2 - I_1 = 0$$

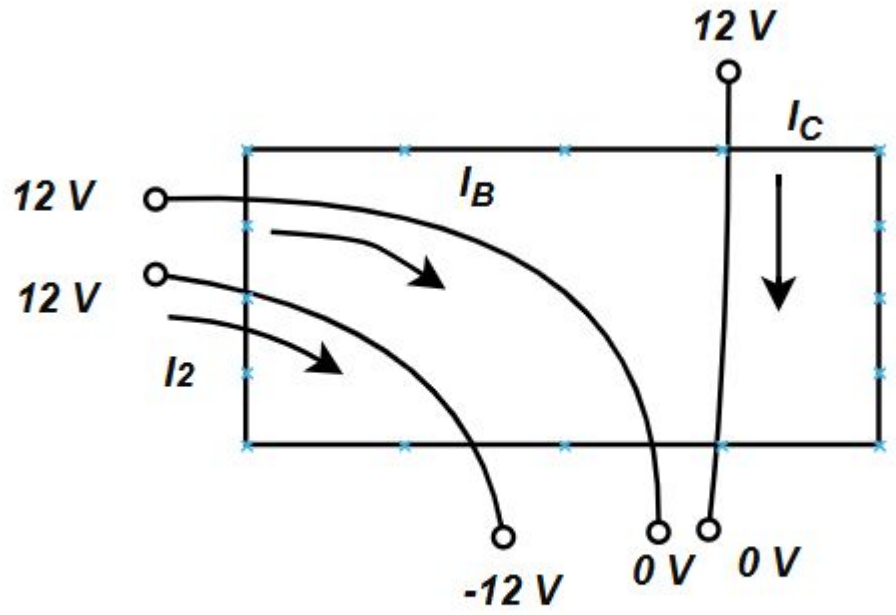
$$I_B = I_1 - I_2 = 0.619\ mA$$

$$\beta_{forced} = \frac{I_C}{I_B} = 8.659 < \beta_F$$

$\boldsymbol{(Saturation\ assumption\ is\ correct)}$



Power dissipation for RTL inverter



Power dissipation for RTL inverter

$$P1 = \big(12 - (-12)\big)V * 0.128\,mA = 3.072\,mW$$

$$P2 = (12 - 0)V * 0.6186\,mA = \ 7.4323\,mW$$

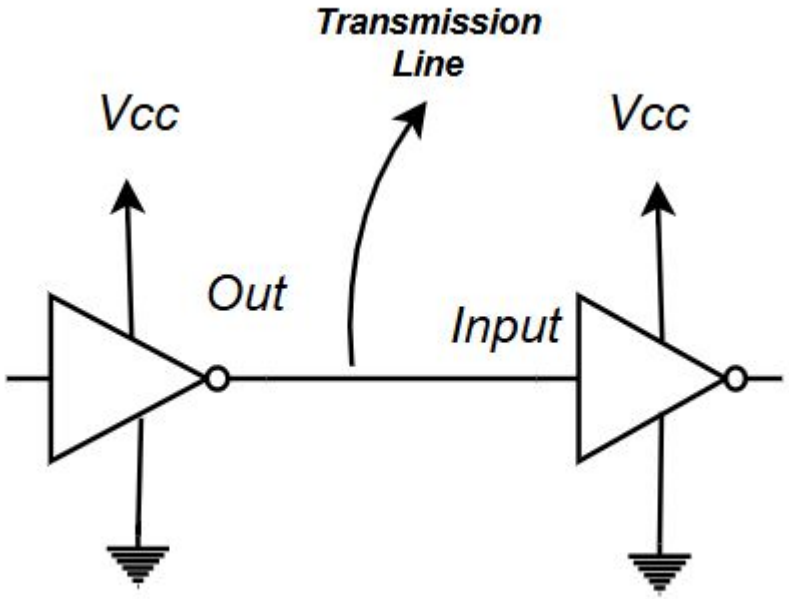
$$P3 = (12 - 0)\,V * 5.3632\,mW = 64.3632\,mW$$

Total Power, $P = P1 + P2 + P3 = 74.8584mW$

Noise Margin

Output from one inverter is received as input to the next inverter.

External interference, noise can hamper the signal transmission



Noise Margin

Noise Margin: The maximum amount of noise voltage can be tolerated by a circuit while completing a successful transmission from output to input.

High state noise margin:

$$V_{NH} = V_{OH} - V_{IH}$$

Low state noise margin:

$$V_{NL} = V_{IL} - V_{OL}$$

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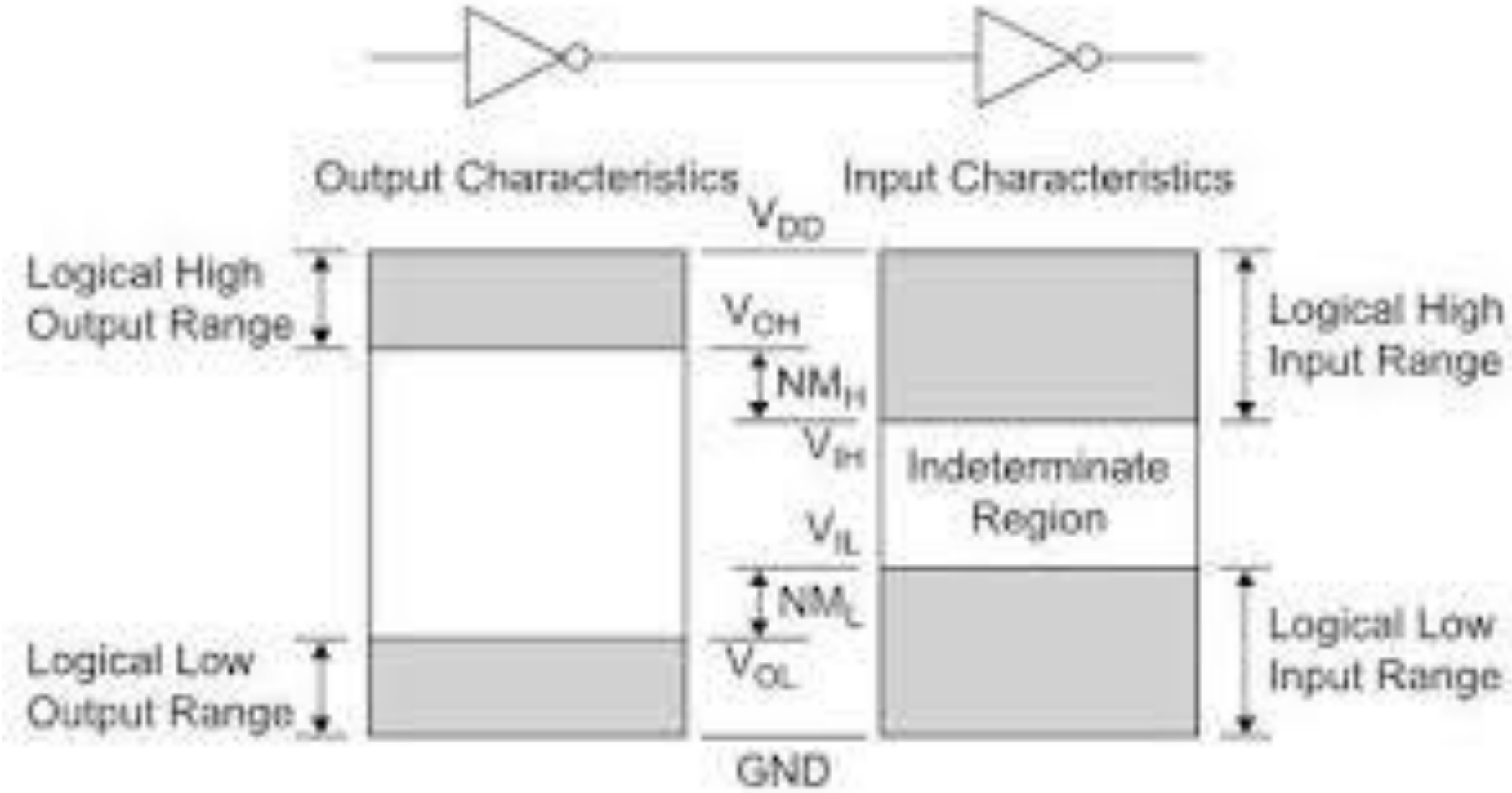
Noise Margin



Noise Margin

V_{OH} □ The minimum voltage level at an output in logical ‘1’ state under defined load condition

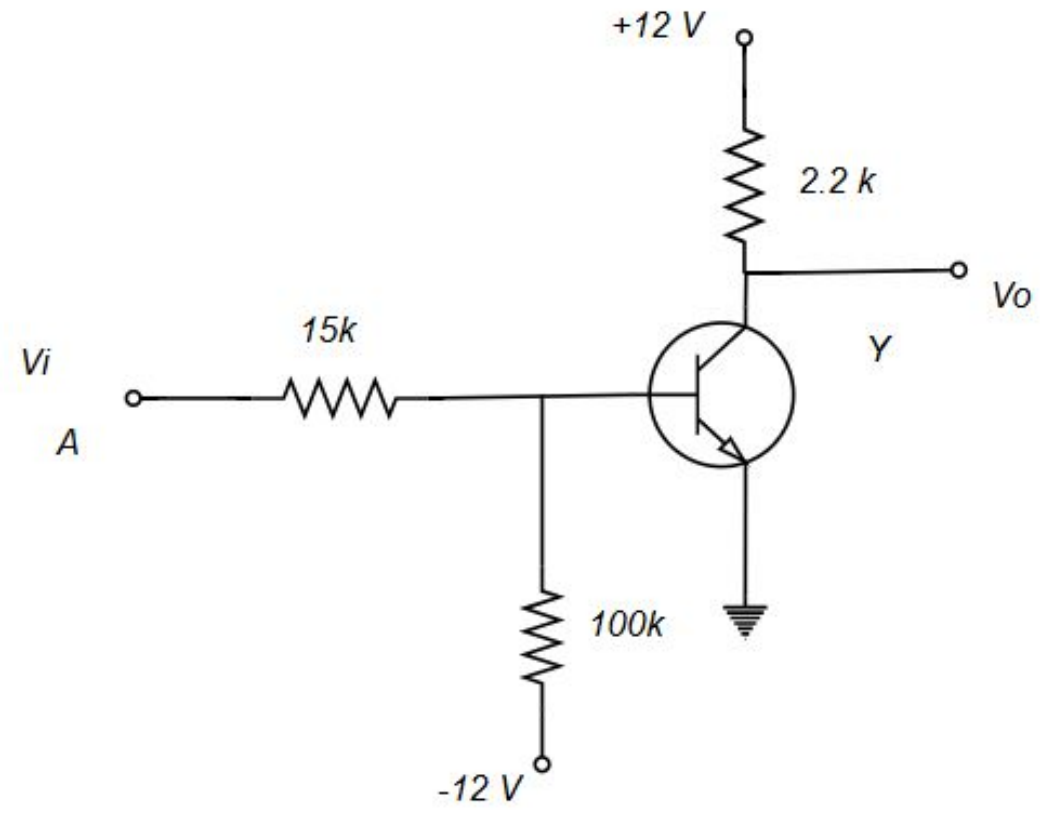
V_{IH} □ The minimum voltage level at an input in logical ‘1’ state under defined load condition

V_{OL} □ The maximum voltage level at an output in the logical ‘0’ state under defined load condition.

V_{IL} □ The maximum voltage level at an input in the logical ‘0’ state under defined load condition.

Example:

The output voltage might drop 0.5V from the maximum voltage. Find out the Noise Margin of the circuit. Given $\beta_F = 30$.



V_{OL} Calculation:

When input is high output should be low and BJT will remain at the saturation mode.

Max Vo for saturation mode will be 0.2 V

V_{OL} = 0.2 V (saturated)

V_{OH} Calculation:

Maximum output voltage = 12V ,

V_{OH} = 12 -0.5 =11.5 V

Noise Margin

V_{IL} calculation :

The maximum voltage we might apply so that the transistor is still turn off.

VBE = 0.5 V, we are on the verge of turning on the transistor T.

→ T : cutoff , $I_B = 0$, $I_1 = I_2$

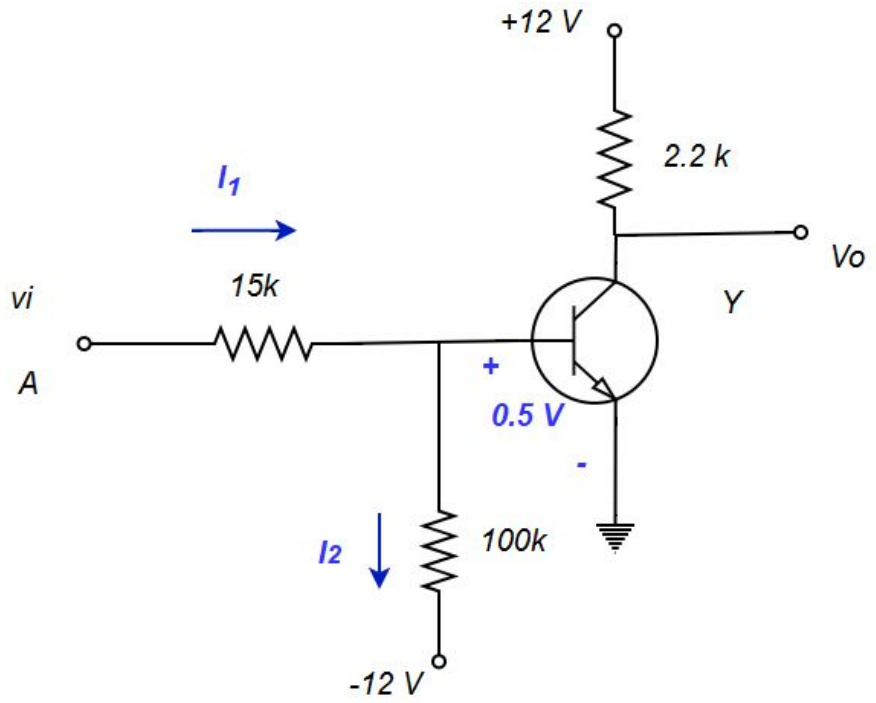
We need to find out for $V_{BE} = 0.5\ V$, what should be the input voltage.

$$I_2 = \frac{0.5 - (-12)}{100k} = 0.125\ mA$$

$$=> V_i = 0.5 + 15 * 0.125 = 2.375\ V$$

This voltage is maximum that we can apply to the inverter without turning on the transistor.

$$V_{IL} = 2.375\ V$$



Noise Margin

V_{IH} calculation :

T → Saturation

The minimum high voltage that we can apply to the input so that the transistor is still operating in saturation mode. β_F = 30

We need to apply such input voltage that transistor T is operating on the verge of going to saturation from forward active mode.

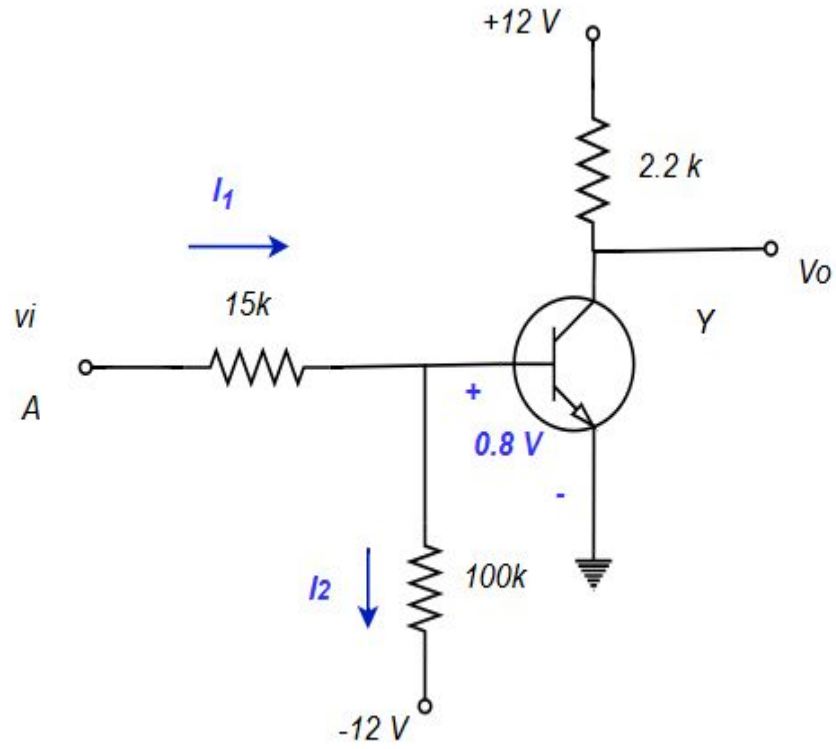
on , $V_{BE} = 0.8\,V, V_{CE} = 0.2\,V$

$$I_C = \frac{12 - 0.2}{2.2k} = 5.3636\,mA$$

$$\beta_{forced} = \frac{I_C}{I_B} \approx \beta_F$$

(This will occur on the average of going from

sat. to forward active mode)



Noise Margin

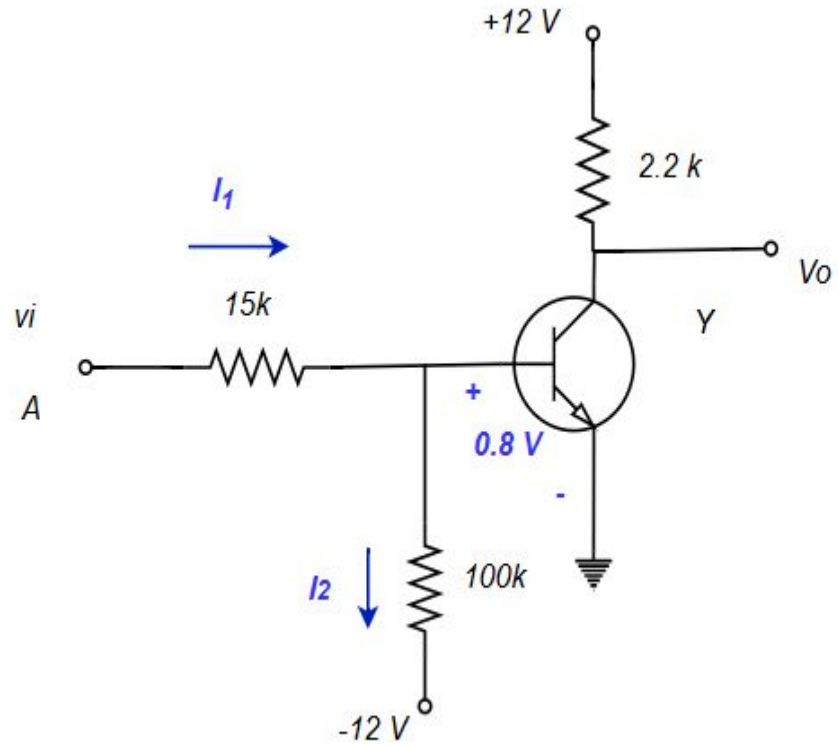
$$I_B^{\bullet} = \frac{I_C}{\beta_F} = 0.1788 \text{ mA},$$

$$I_2 = \frac{0.8 - (-12)}{100k} = 0.128\, mA$$

$$I_1 = I_2 + I_B = 0.3068\, mA$$

$$\frac{V_i - 0.8}{15k} = I_1 = 0.3068$$

$$V_i = 0.8 + 0.3068 * 15 = 5.4018\, V$$



Noise Margin

$$V_{NH} = 11.5 - 5.4018 = 6.0982\,V < -High\ noise\ margin$$

$$V_{NL} = 2.375 - 0.2 = 2.175\,V < -Low\ noise\ margin$$

$$\boldsymbol{Noise\ Margin = \min(V_{NH}, V_{NH}) = 2.175\,V}$$

This noise voltage can be tolerated for both input and output voltages.

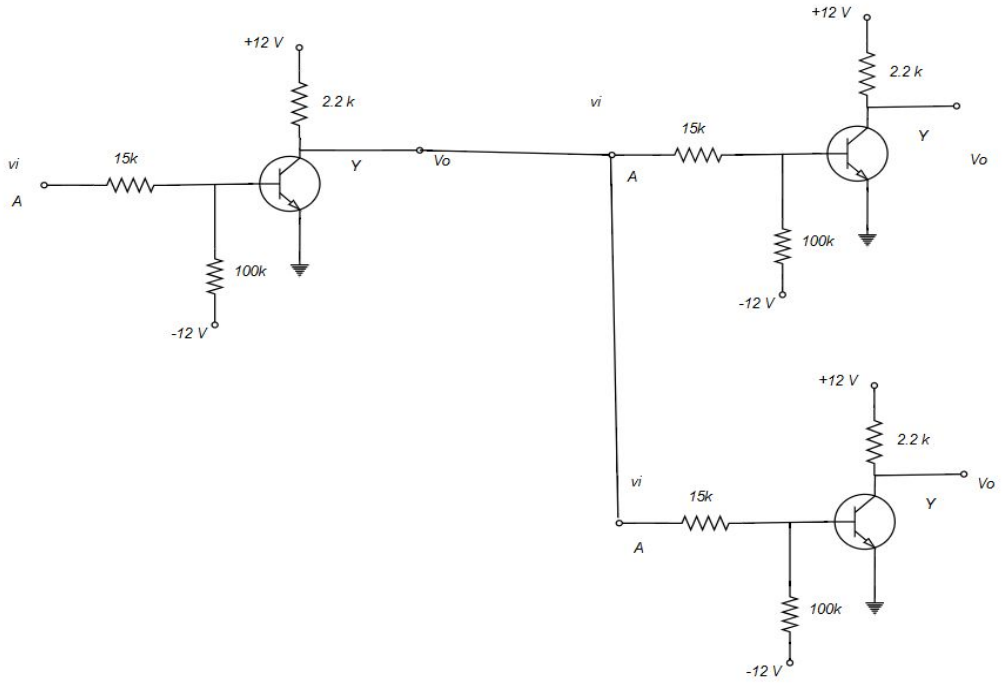
Fanout

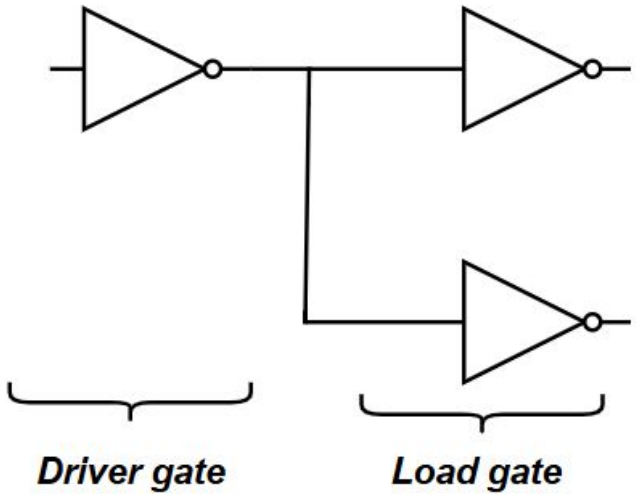
Fanout:

The maximum number of logic inputs (of the same logic family) that an output can drive reliably is called maximum fanout.

- ✔ **calculate fanout □ maximum fanout**
- ✔ **fanout given in question may not be maximum**

Fanout

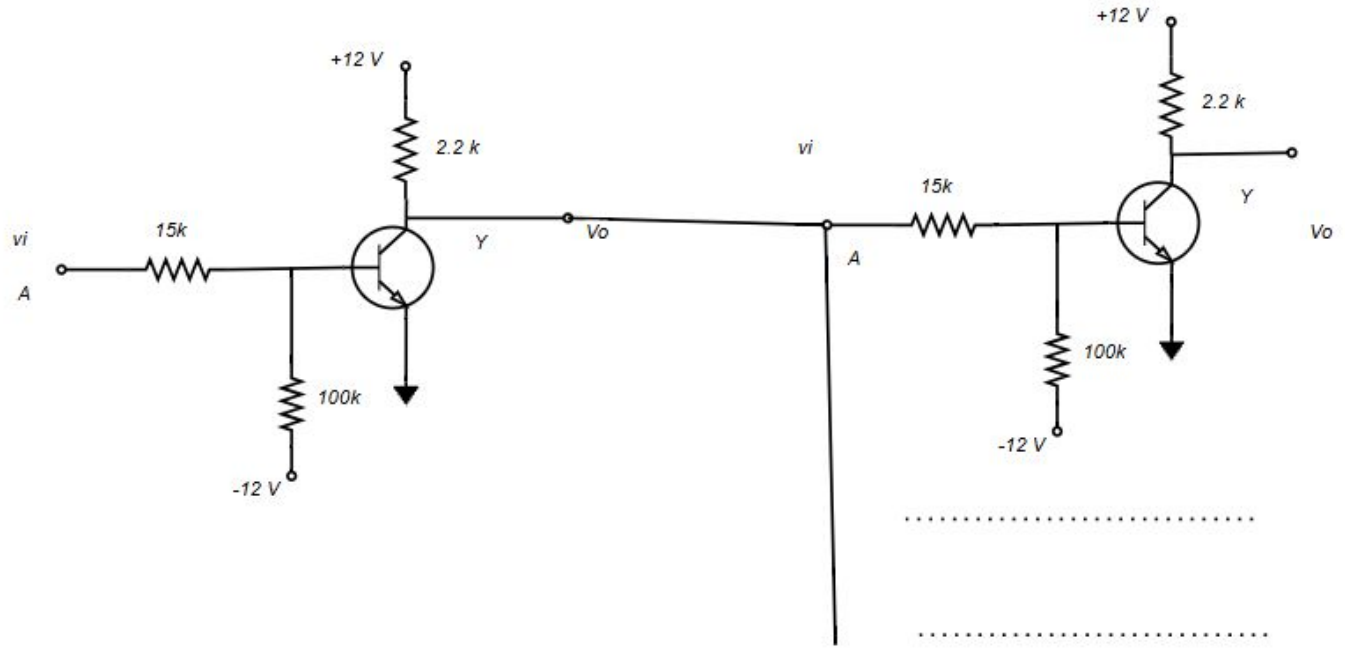




Here output is connected with two other gate input. Fanout = 2

Fanout

Example: Calculate the fanout of the RTL circuit. Assume V_{OH} = 10V.



Fanout

Driver gate □ Supply current

Load gate □ Consume current

Two case:

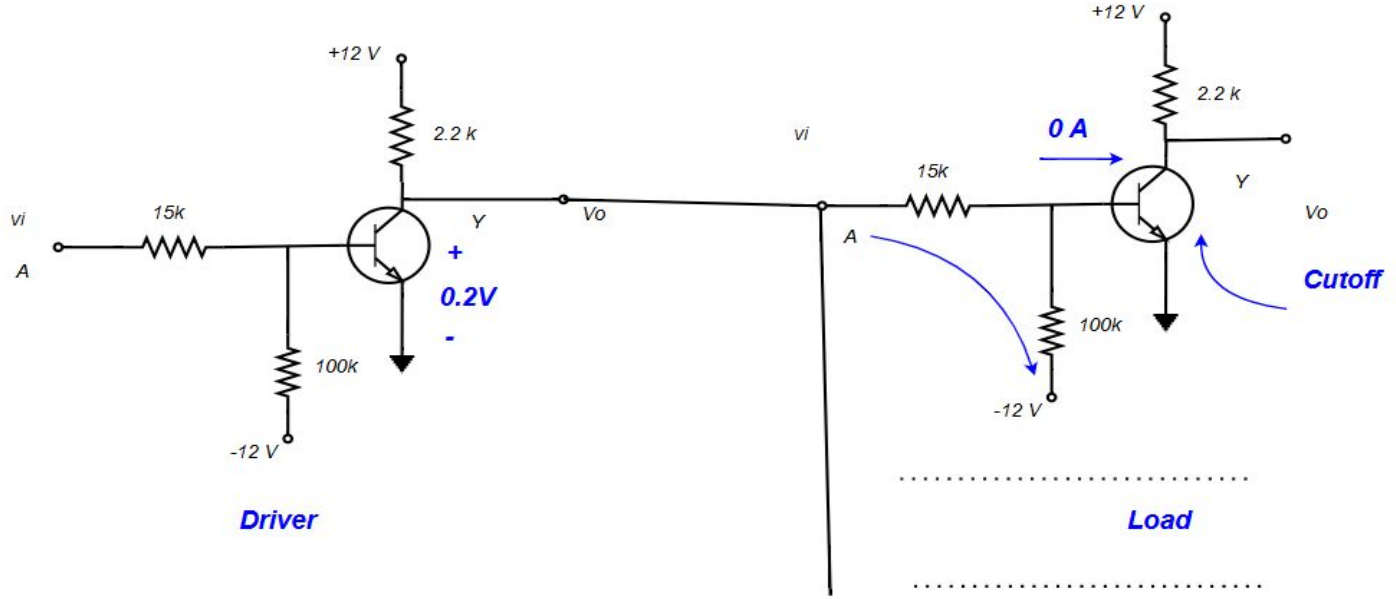
Case 1: Driver output Low,

Case 2: Driver output high

Calculate:

1. Individual demand current for each load circuit/ gate
2. The maximum current that can be supplied from driver circuit

Fanout



Case 1. When output voltage at the driver is low.

$V_{OL} = 0.2$ V

Maximum total supply = $\frac{12-0.2}{2.2k} = 5.3636\ mA$

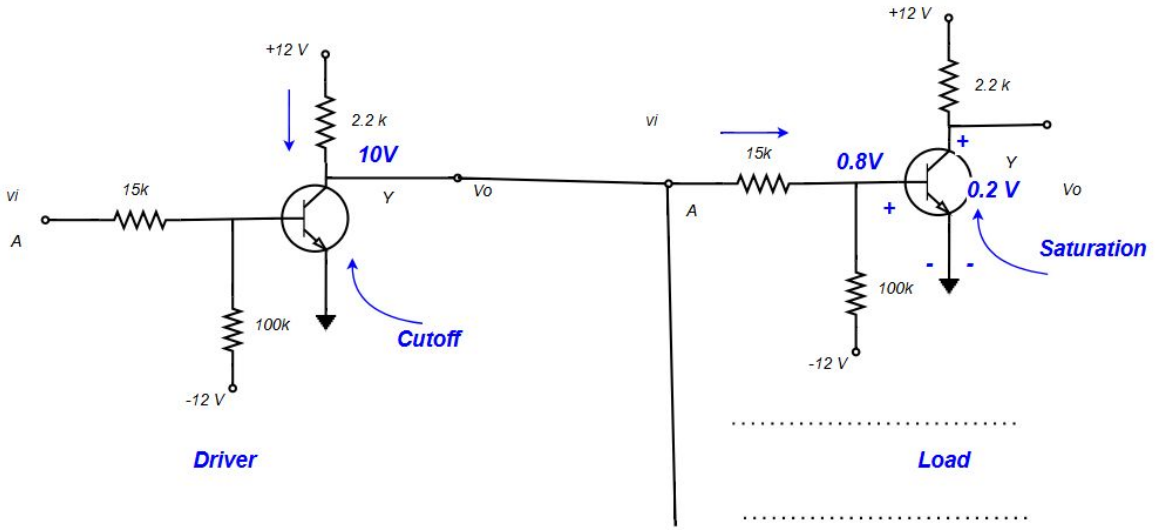
Individual load current demand = $\frac{0.2\ -(-12)}{115\ k} = 0.106\ mA$

(in this case load circuits transistors are in cutoff mode)

Maximum number of load circuits that we can afford ,

$Fanout = \frac{5.3636\ mA}{0.106\ mA} = |\_50.6\_| = 50$ (Floor)

Fanout



Case 2: When output voltage driver circuit is high. V_{OH}.

Driver transistor is in cutoff and load transistor is in saturation

Maximum supply current $= \frac{12-10}{2.2\ k} = 0.909\ mA$

Individual load current = $I_L = \frac{10-0.8}{15k} = 0.6133\ mA$

Maximum fanout for this = $\left|\frac{0.909}{-0.6133}\right| = 1$

Fanout

Overall maximum fanout must be calculated by considering worst case scenario.

To prevent malfunction of driver circuit , we need to take the minimum of the two cases.

Max Fanout = Min (50,1) = 1