CSE 350
Digital Electronics and Pulse Techniques

DTL-Noise Margin, Fanout, Power Dissipation

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DTL

$\boldsymbol{\beta_{min} = the\ minimum\ value\ of \beta_F\ of\ the\ switching\ transistor\ T,}$

That will keep the circuit operation error free.

case(1) , (2) and (3) will not help us to determine the β_{min} because in these case the transistor is turn off.

However for case (4) transistor is on and operates in saturation mode, Therefore, to maintain correct operating we must choose a value of

$$\beta_{min} = \frac{I_C}{I_B} = \frac{2.182}{0.4} = 5.46$$

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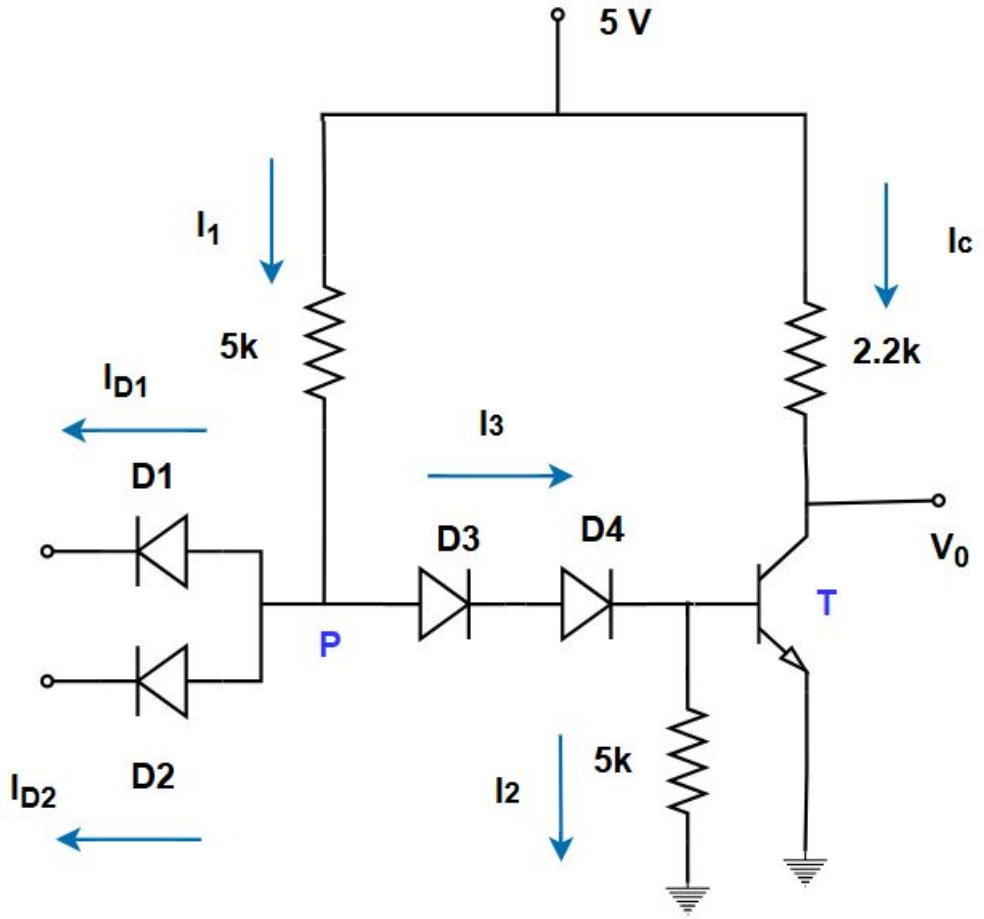
Noise Margin of DTL

NM calculation of DTL is not similar to the RTL circuit.



Noise Margin of DTL

Example: IF all the inputs are high, what is the magnitude of noise voltage which will cause the gate to malfunction ?

correct operating condition when all inputs are high.

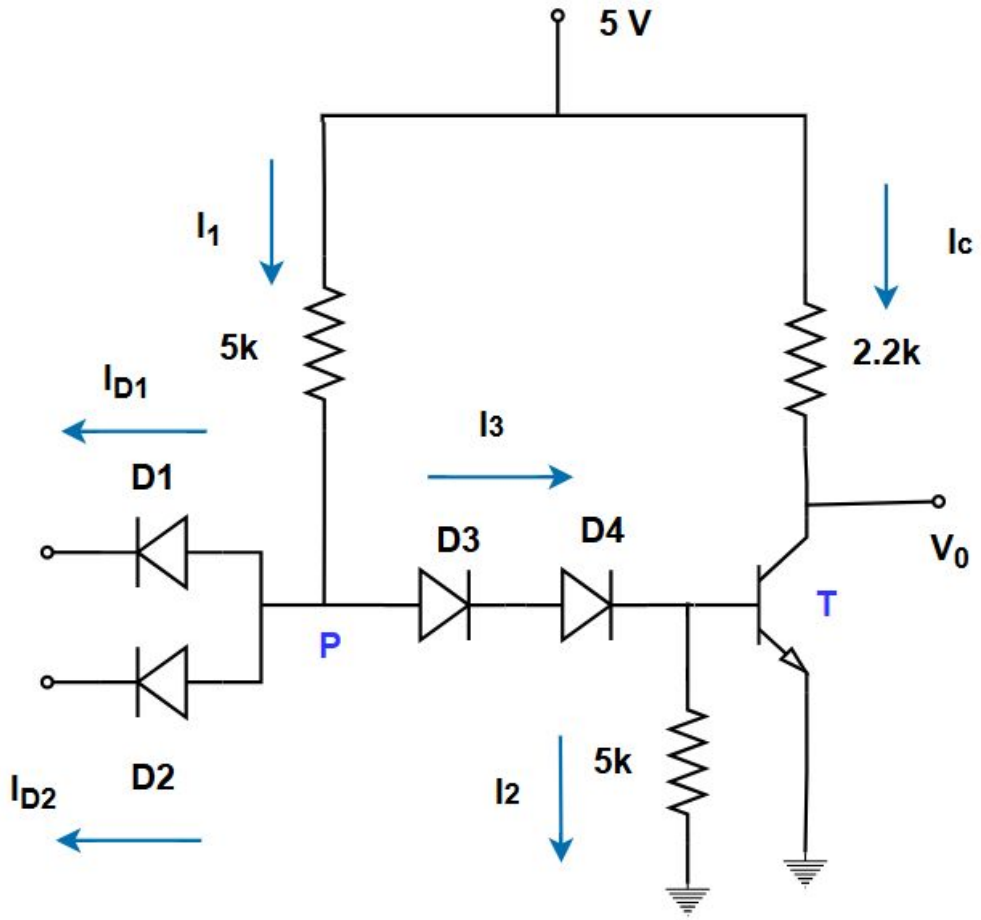
Case (4). D1 , D2 off.

D3 and D4 ON Sat

The circuit will malfunction if it starts operating in case (1) conditions.

D1, D2 on, D3 , D4, T off.

If D1 and D2 starts conducting, they will have precedence over D3, D4 and T because of lower resistance at that direction.



Noise Margin of DTL

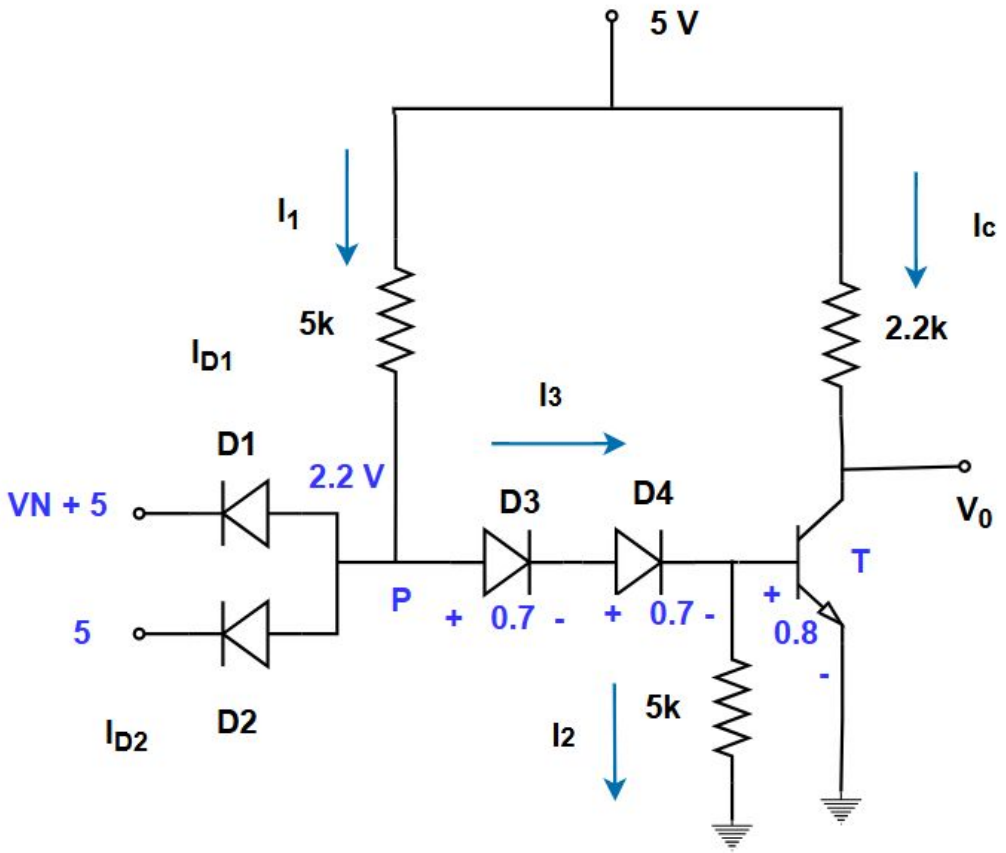
So the circuit will malfunction when the voltage difference VA and VP is equal to cut in voltage of diode.

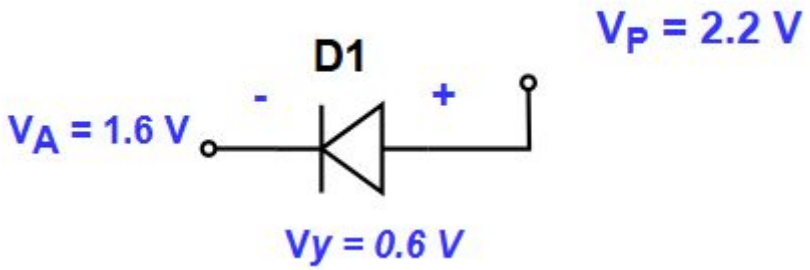
If VA = 1.6V, then anode voltage of D1 will have enough voltage to start conducting. Hence circuit will malfunction.

$$V_N + 5 = 1.6 \Rightarrow V_N = -3.4\ V$$

$$V_N = 3.4\ (\ taking\ magnitude\ )$$

$$V_{NM} = 3.4\ V$$





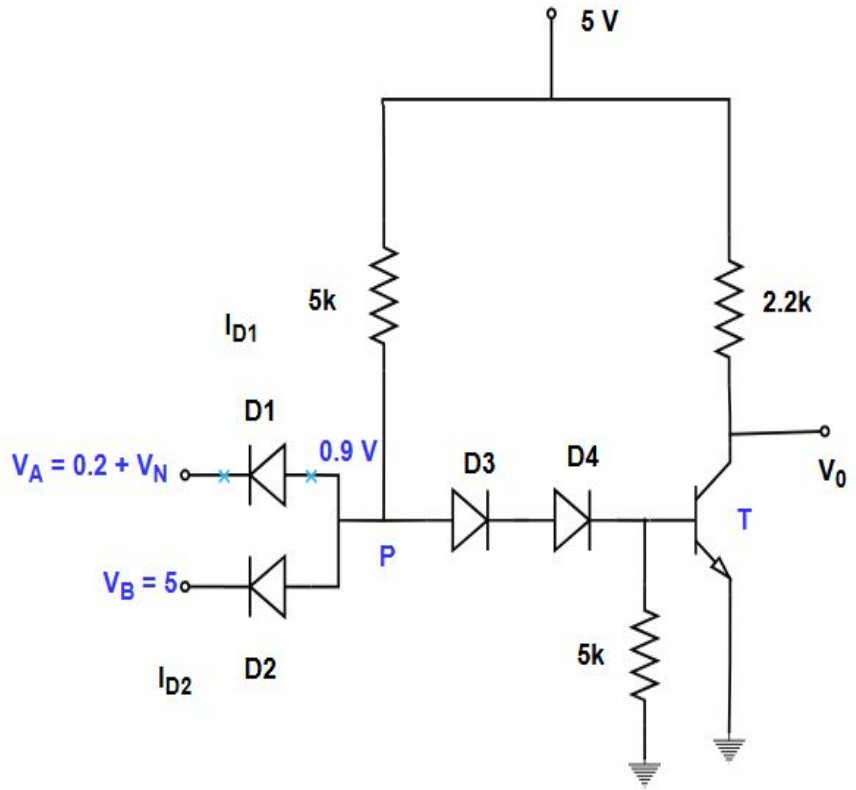
Noise Margin of DTL

Q. If one of the inputs is low and others are high, then what magnitude of noise voltage at low input terminal will cause the transistor to malfunction ?

valid operation: case (2) D1 on, D2, D3, D4 , T off.

The circuit will malfunction if D3, D4 and T start conducting or turned on.

As long as D1 is on any increment in noise voltage at node A will also increase the voltage at Vp. Because, the difference between anode and cathode terminal should be 0.7 V for conducting diode D1.



DTL NAND Gate

If we increase Vp upto 1.7 V for conducting , then D3, D4 and T will turn on.

$$V_P + V_N = 1.7$$

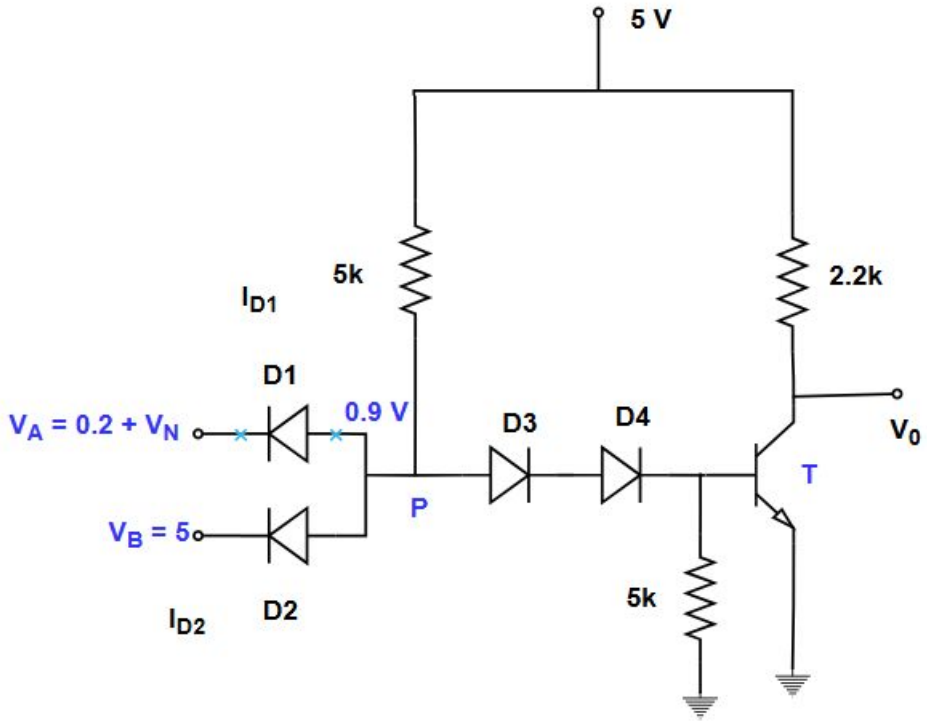
$$\Rightarrow V_N = 1.7 - 0.9 = 0.8\,V$$

Low noise margin = 0.8 V

Finally, total noise margin, NM

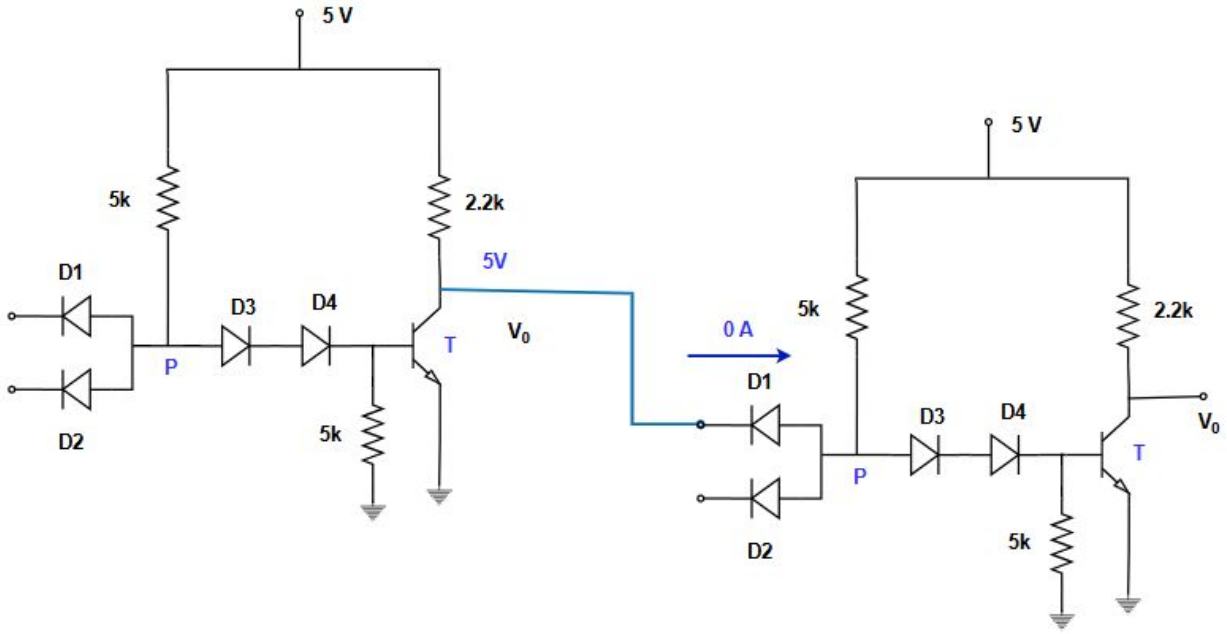
= min (NML, NMH)

= (0.8, 3.4) = 0.8 V



Fanout Calculation

Different from RTL



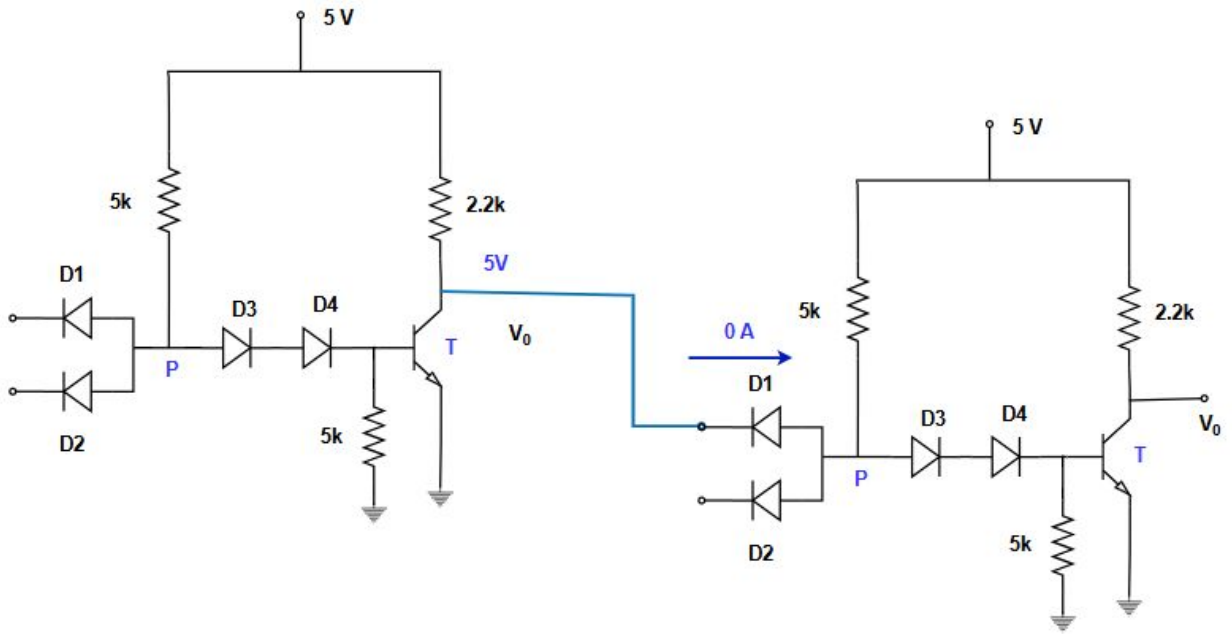
Fanout Calculation

Case 1: Output voltage of driver is high (5V).

If $V_o = 5\ V$, then the demand current of the load circuit is zero.

Therefore, we can connect as many load circuit as we wish for this case.

Max Fanout = ∝



Fanout Calculation

Case 2: Output voltage of driver is low.(0.2 V)

Individual load circuit delivers IL current

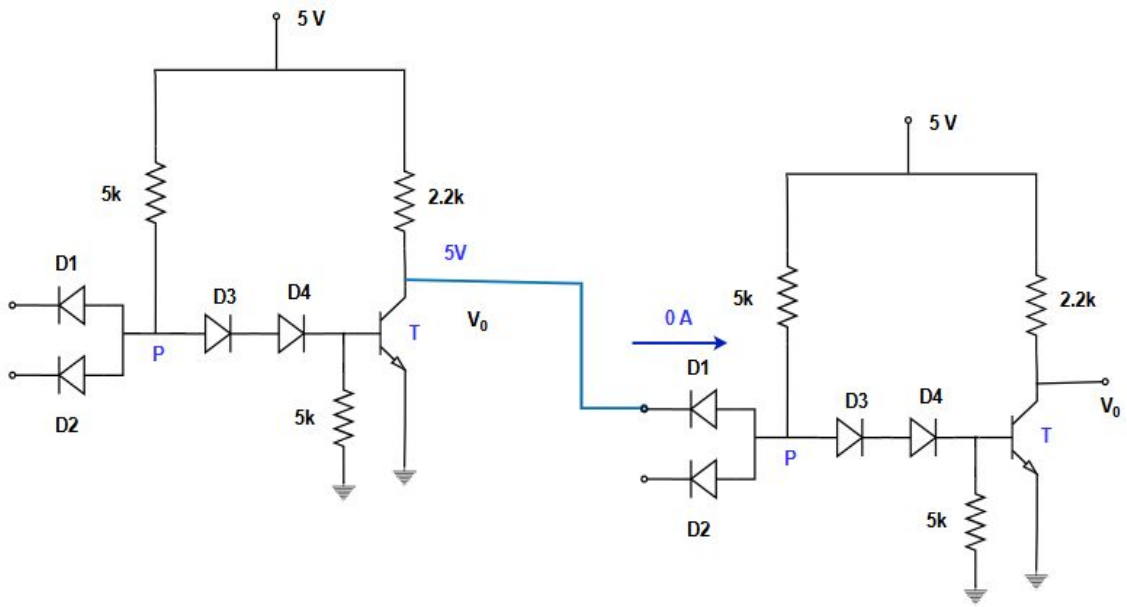
IL = standard load

$$I'_C = No\ load\ collector\ current$$

$$I_C = Total\ collector\ current$$

If the number of fanout = N,

Total collector current, $I_C = I'_C + N * I_L$



Fanout Calculation

Constraint: Since the transistor T in driver circuit in saturation mode, the collector current cannot cross a certain value. That will push the transistor T from saturation to forward active mode.

$$\beta_{forced} > \beta_F (\, Not\ in\ saturation)$$

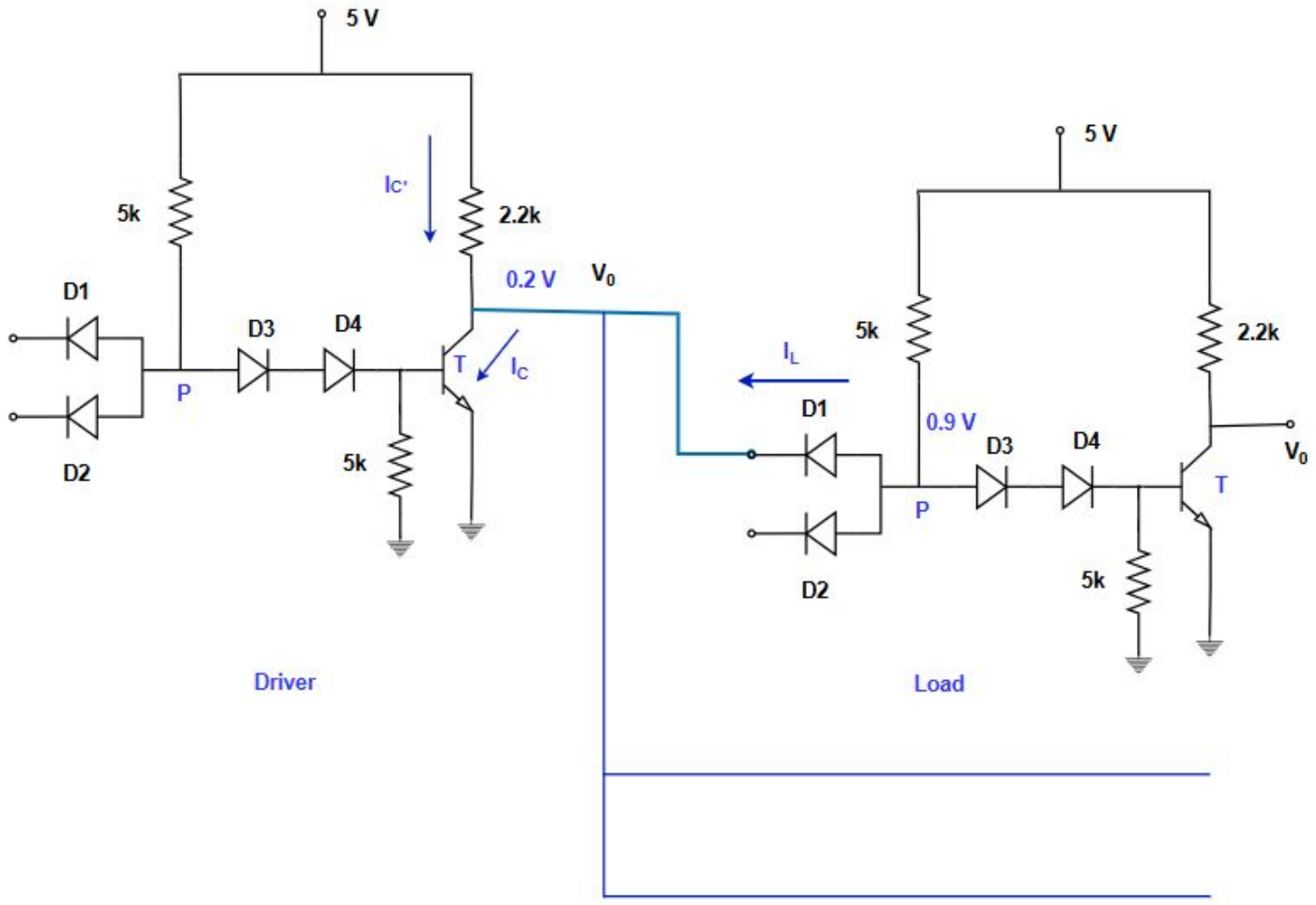
$$\beta_{forced} \approx \beta_F \,(\, Edge\ of\ sat. and\ F > A]$$

$$I_{Cmax}, = \beta_F * I_B$$

= 30 * 0.4

= 12 mA

Fanout Calculation



Fanout Calculation

- $$I_{Cmax} = I'_C + N * I_L \, , Floor(N)$$
$$will\ be\ the \max fanout$$

Standard load , $I_L = \frac{5-0.9}{5k} = 0.82\ mA$

No load collector current ,

$$I'_C = \frac{5\ -0.2}{2.2k} = 2.182\ mA$$

Fanout Calculation

Now, $12 = 2.182 + N * 0.82$

$$\Rightarrow N = 11.97 \approx 11\ (\ Floor\ )$$

We cannot choose 12, because in that case collector current will overflow and make transistor T to operate in Forward Active.

Fanout $= Min\ (\ \infty\ , 11\ ) = 11$

DTL Power Dissipation

Power dissipation for DTL circuit.

Case 1: $V_o = 0.2\ V$

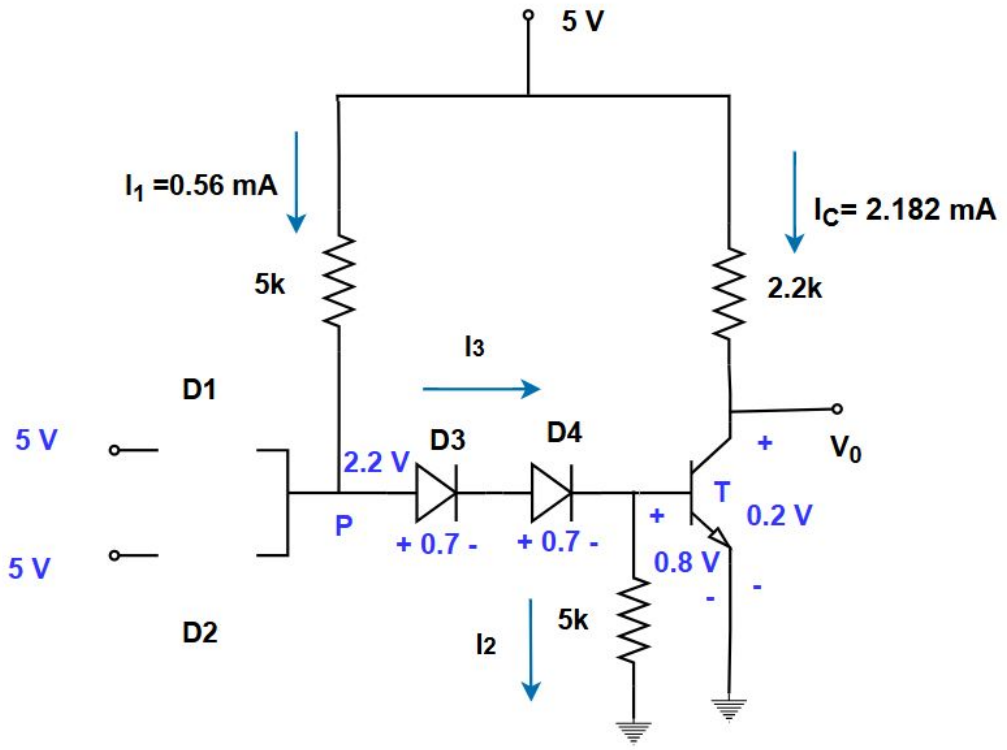
$V_1 = V_2 = 5\ V$

$D_1, D_2, \rightarrow OFF$

$D_3\ , D_4, T\ \rightarrow ON$

$$I_1 = \frac{5 - 2.2}{5k} = 0.56\ mA$$

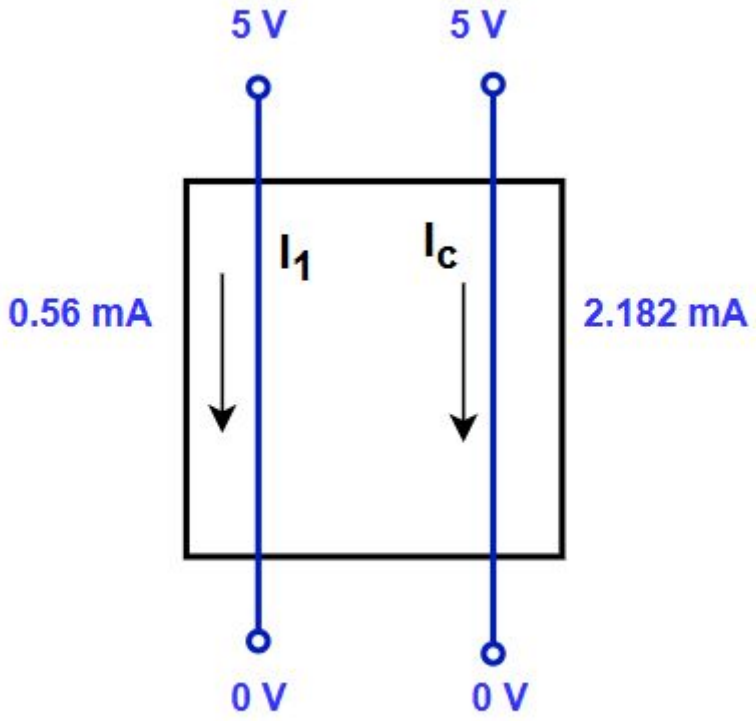
$$I_c = \frac{5 - 0.2}{2.2k} = 2.182\ mA$$



DTL Power Dissipation

Power

$$P_1 = (5 - 0) * 0.56\,mA = 2.8\,mW$$
$$P_2 = (5 - 0) * 2.182\,mA = 10.91\,mW$$
$$P = P_1 + P_2 = 13.71\,mW$$



DTL Power Dissipation

Power dissipation for DTL circuit.

Case 2: $V_o = 5\ V$

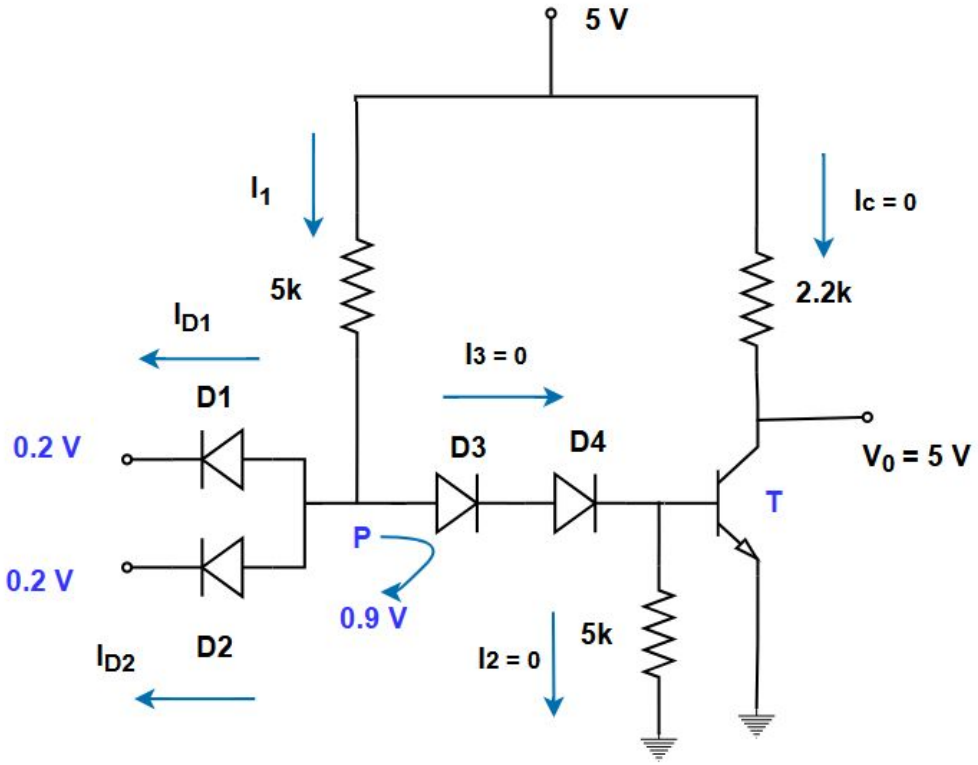
$V_1 = V_2 = 0.2\ V$

$D_1, D_2, \rightarrow ON$

$D_3\ , D_4, T\ \rightarrow OFF$

$$I_1 = \frac{5 - 0.9}{5k} = 0.82\ mA$$

$$I_{D1} = I_{D2} = \frac{I_1}{2} = 0.41\ mA$$

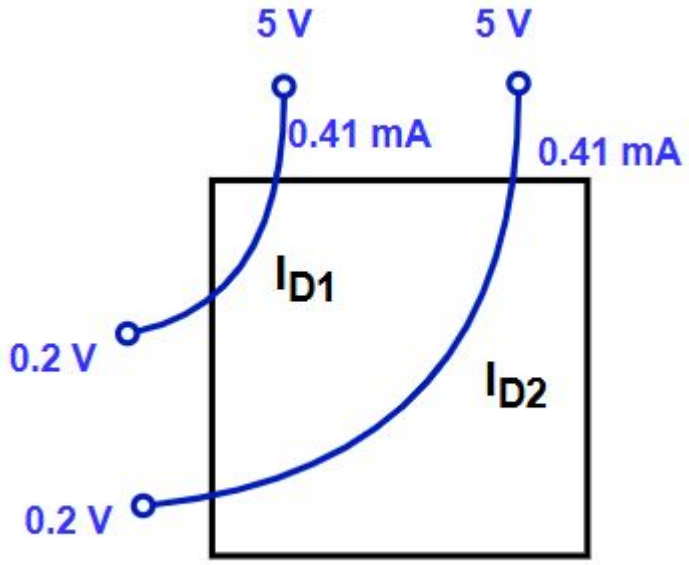


DTL Power Dissipation

Power dissipation for DTL circuit.

$$P1 = (5 - 0.2) * 0.41\,mA = 1.968\,mW$$
$$P2 = (5 - 0.2) * 0.41\,mA = 1.968\,mW$$

P = P1 + P2 = 3.936 m W



DTL Power Dissipation

Case 3: $V_o = 5\ V$
$V_1 = 0.2\ V, V_2 = 5\ V$

Case 4: $V_o = 5\ V$
$V_1 = 5V, V_2 = 0.2\ V$

Try yourself. Both will give the same result as the case 2.