CSE 350 : Digital Electronics and Pulse Techniques

Prerequisite : CSE 251, CSE 260

Course Instructor : Shahnewaz Ahmed (SHA)

Theory : Saturday - Thursday (3:30-5:00 pm)

Marks Distribution :

<zoom>	Attendance	: 7%	<Bonus>
<no pdf>	Homework (bux)	: 8%	<best 6 out of 8>
<combined>	Quiz (Proctored)	: 15%	(best 3 out of 4)
Sat-Thur / after 5 pm	Midterm (1 hr)	: 15%	(offline)
	Lab (———)	: 20%	
(13th May 2-5 pm)	Final (2.5 hr)	: 35%	(offline)
		100%	

Course Content :-

70% 1. Digital Electronics { Digital Logic families + DC analysis

30% 2. Pulse Techniques { Signal generators, A/D . D/A converters

Lecture content : Review of CSE 250

Charge, Voltage, Current, Ohm's law,

Node, KVL, KCL, Nodal Analysis

Charge: Fundamental property of elementary particles.

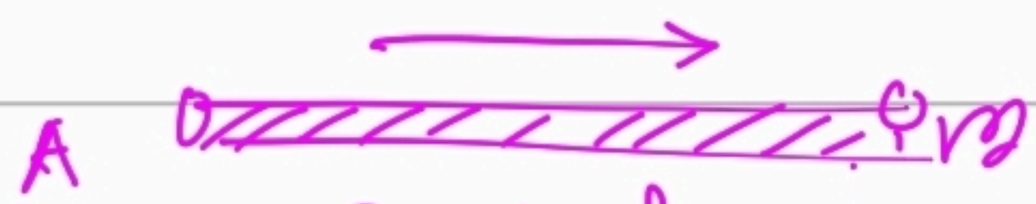
Atom ← {electron (−e), proton (+e), neutron (0)}

Coloumb's law is used to calculate the force between charged particle.

Voltage: The amount of work (1J) needed to displace a (1C) unit charge from one point to another is called voltage. (1V)

$$V_B - V_A = \frac{W}{q}$$

Current: The rate of flow of charge within a conductor is called current.

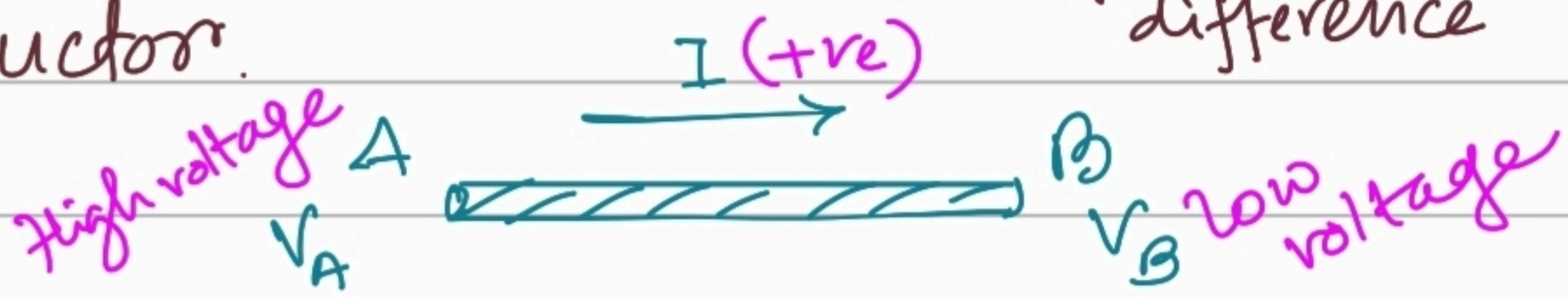


Conductor

$$\boxed{\frac{dq}{dt} = i}$$

SI unit of current is ampere.

Ohm's law: For a certain temperature the amount of current flows through a conductor is proportional to the voltage difference across the conductor.



$I \propto (V_B - V_A) \Rightarrow I = G(V_B - V_A)$

$G \rightarrow$ conductance

$R \rightarrow$ resistance

$\underbrace{(V_B - V_A)}_{V_{BA} = RI} = RI = \frac{1}{G} I$

Electrical Components :-

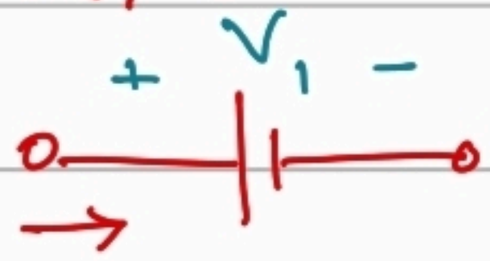
① Resistor :

$R \neq 0$

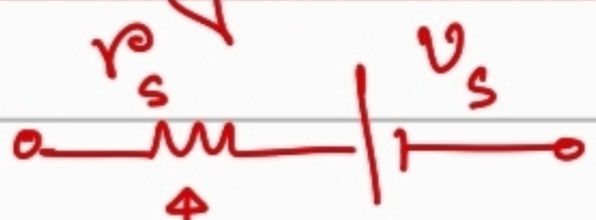
Perfect conductor

$R = 0$

② Voltage source :



V_1 doesn't depend on current.

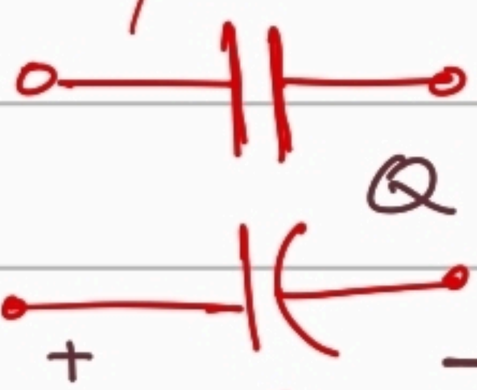


internal resistance

Practical case

source resistance

③ Capacitor :

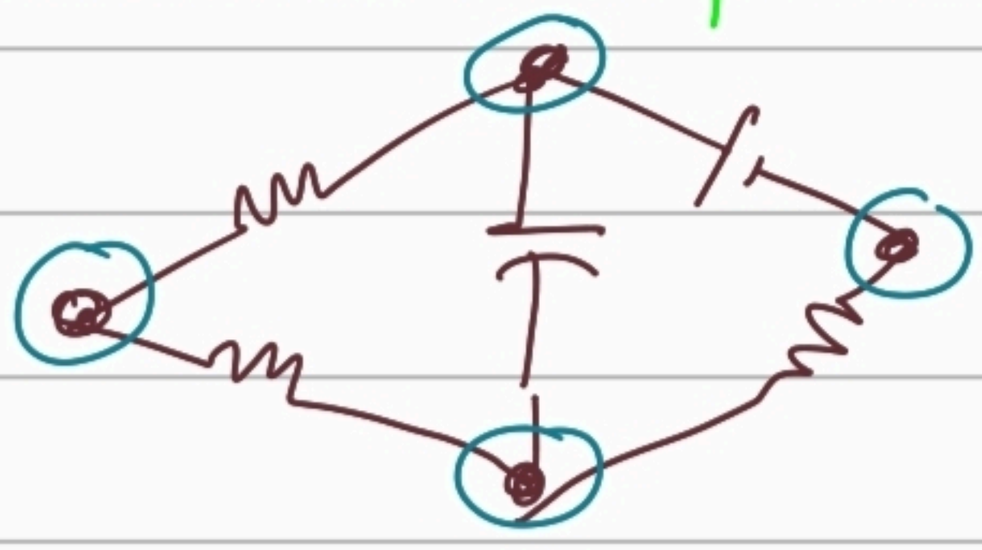


parallel plate capacitor

The amount of charge stored in a capacitor is proportional to the voltage difference across the capacitor.

$Q \propto V \Rightarrow Q = CV$ | $C \rightarrow$ capacitance

Node : The interconnection point between more than electrical component is called a node.



4 nodes

KCL : Kirchoff's Current Law

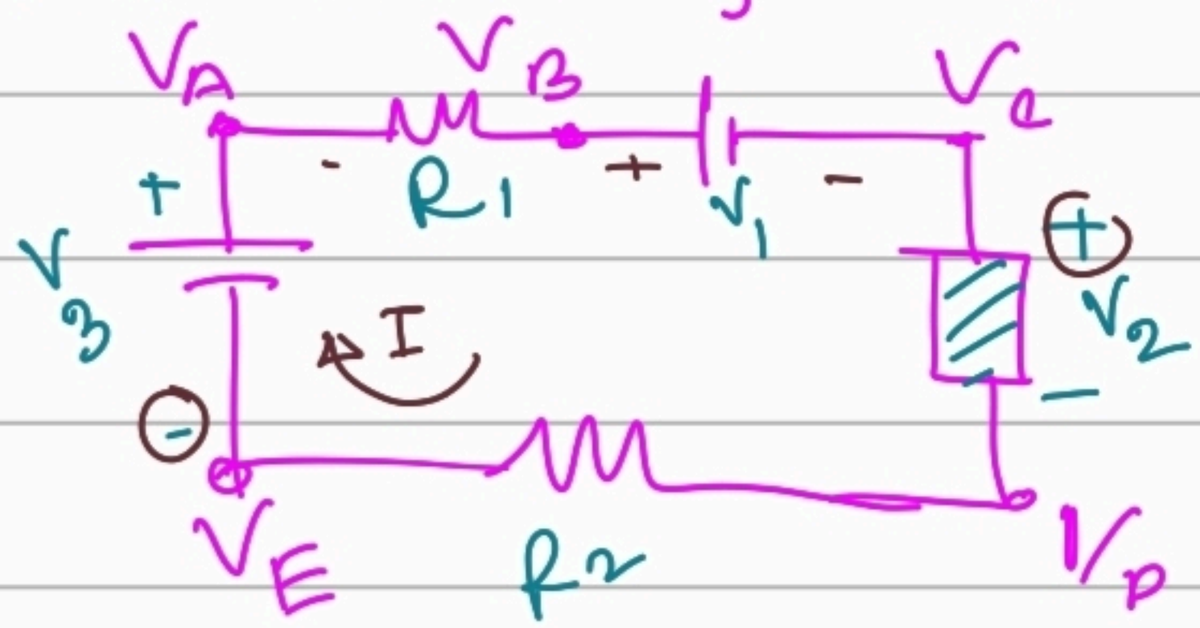
The algebraic sum of currents on a node is zero.

$$-i_1 + i_2 + i_3 - i_4 + i_5 = 0$$

- current entering a node would be negativ current

- current exiting a node would be positive current.

KVL : The voltage drop across a loop inside a electric circuit is zero.



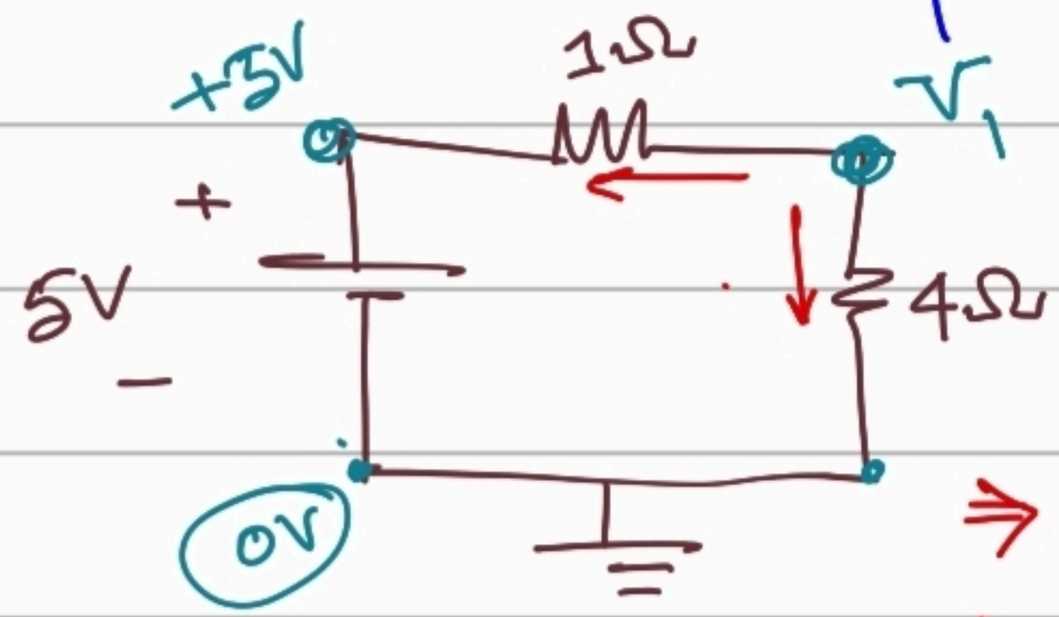
$$V_{AB} + V_{BC} + V_{CD} + V_{DE} + V_{EA} = 0$$

$$IR_1 + V_1 + V_2 + IR_2 - V_3 = 0$$

NODE ANALYSIS :

1. Identify a reference node (ground)
2. Identify all the unknown node
3. Write the nodal equation
4. Solve the nodal equations together.

Example 1:



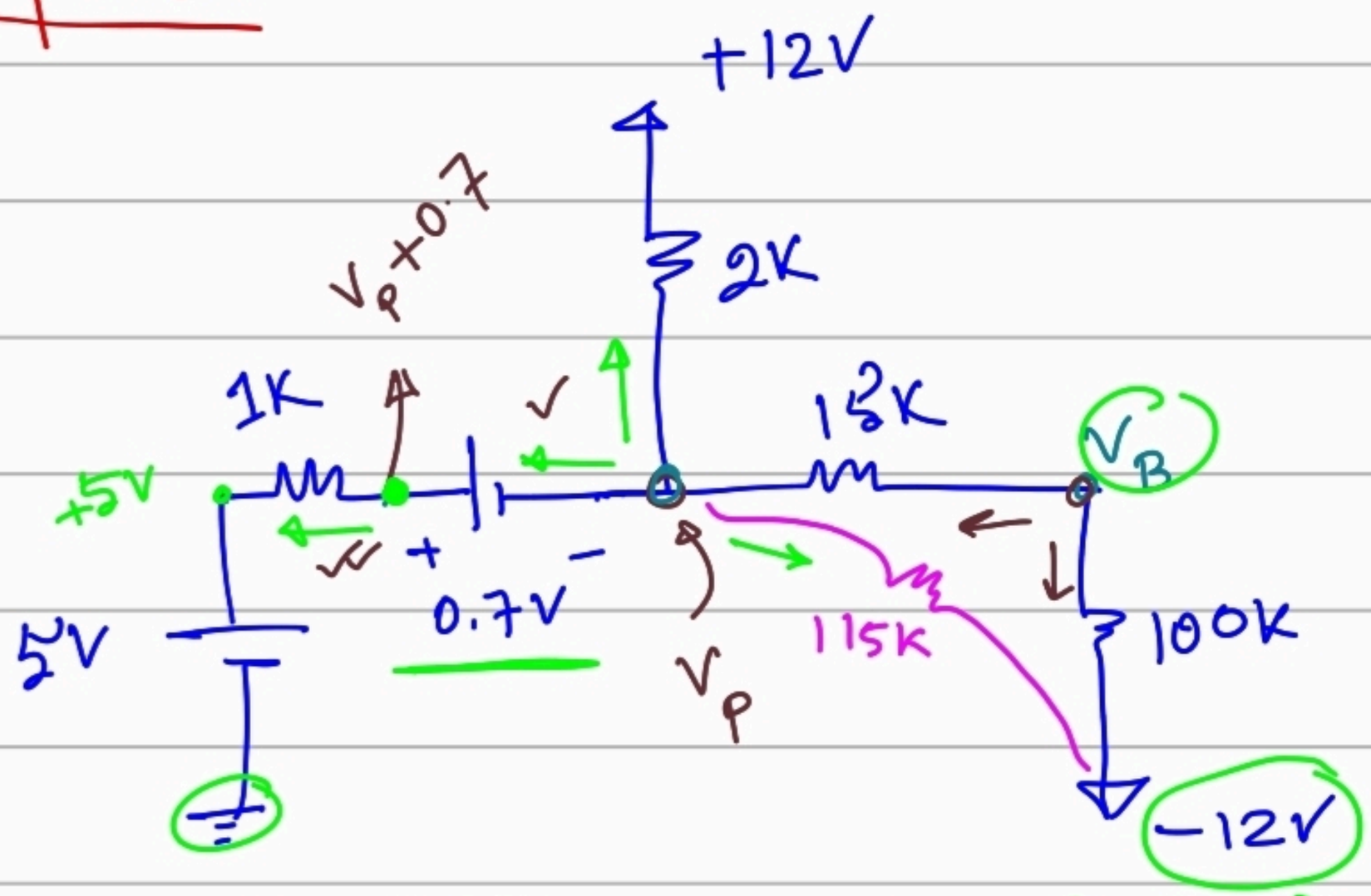
V1:

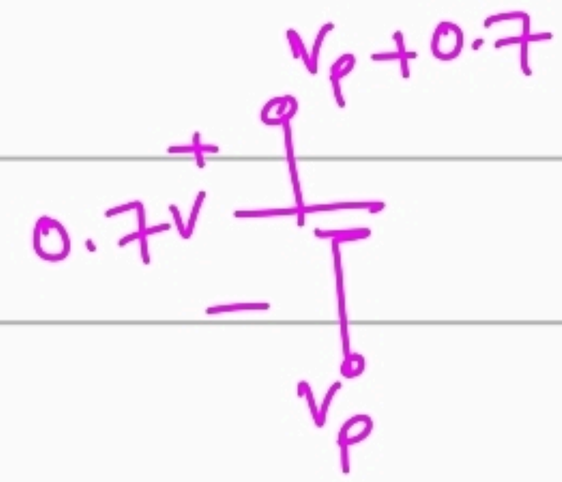
$$\frac{V_1 - 0}{4} + \frac{V_1 - 5}{1} = 0$$

$$\Rightarrow V_1\left(\frac{1}{4} + 1\right) = 5$$

$$\Rightarrow V_1 \, 5/4 = 5 \Rightarrow V_1 = 4V$$

Example : 2





~~Online Calculator~~

KCL

$$\frac{V_p-(-12)}{115}+\frac{V_p-12}{2}+\frac{(V_p+0.7)-5}{1}=0$$

$$V_p:\quad \frac{V_p-V_B}{15K}+\frac{(V_p-12)}{2}+\frac{(V_p+0.7)-5}{1}=0$$

$$V_B:\quad \frac{V_B-(-12)}{100}+\frac{(V_B-V_p)}{15}=0$$

Lecture 2: CSE 251 Review

Electronic Circuits and Devices.

Electronic : The method or process by which we can control the flow of electron using external forces / voltage.

Spintronics, Photonics, Twistronics, Valleytronics
[opto electronics]

Materials can be classified roughly into three categories based on their conductivity.

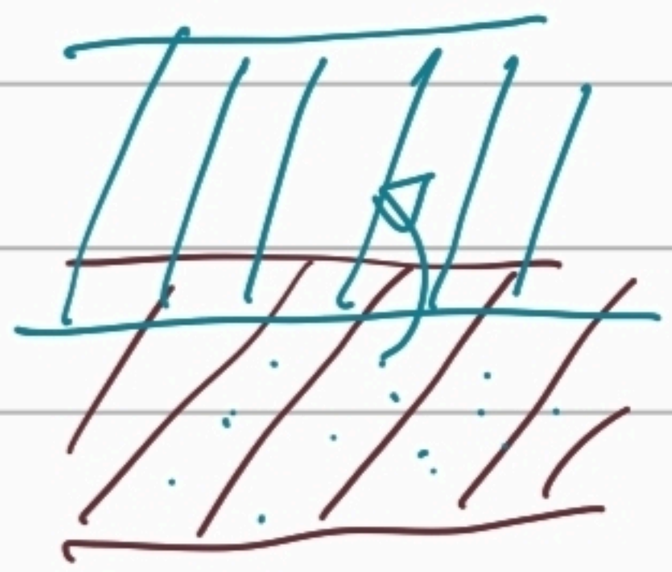
1. Metal (Good conductor)

2. Semiconductor

3. Insulator (Bad conductor)

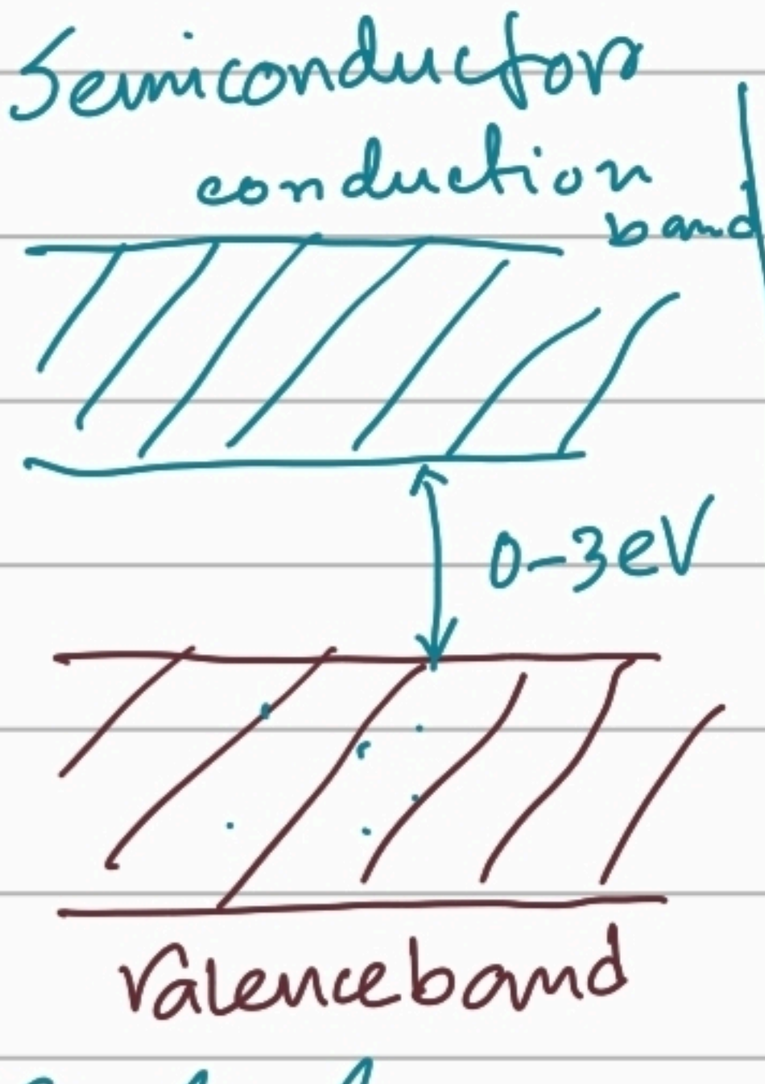
Electron's energy levels form energy bands within a solid. (Quantum Mechanics)

Metal



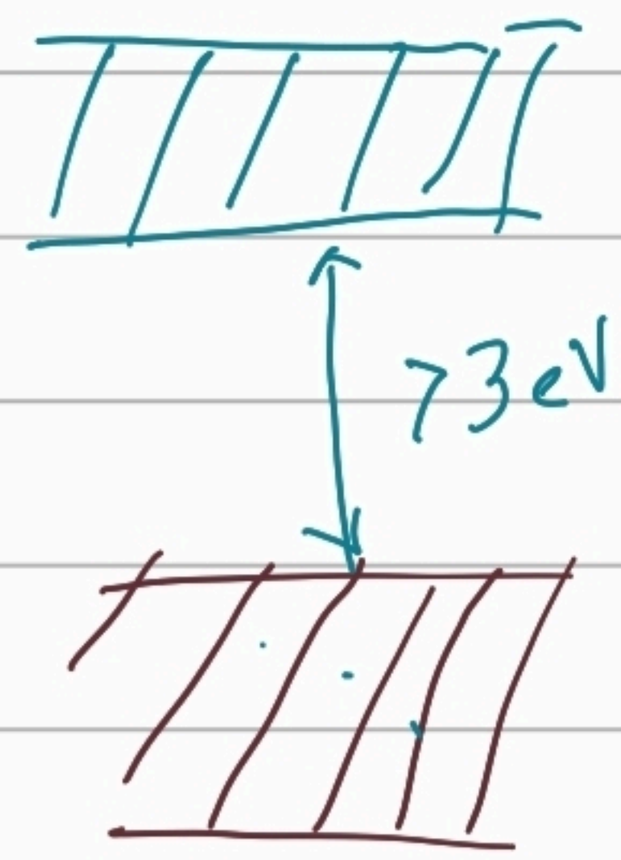
Ex: Ag, Au, Al, Na, Mg, K

Semiconductor



Ex: Si, Ge, GaAs, GaN, InSb,

Insulator

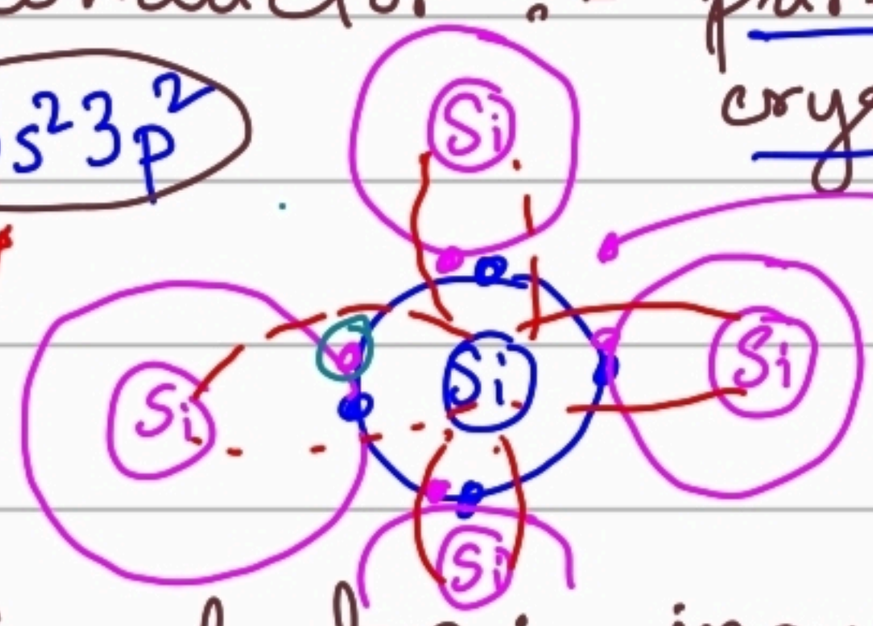


Ex. SiO_2, SiN, Al_2O_3

Intrinsic Semiconductor :- pure semiconductor crystal. (Si)

Si : $1s^2\ 2s^2 2p^6\ 3s^2 3p^2$

Valence electrons



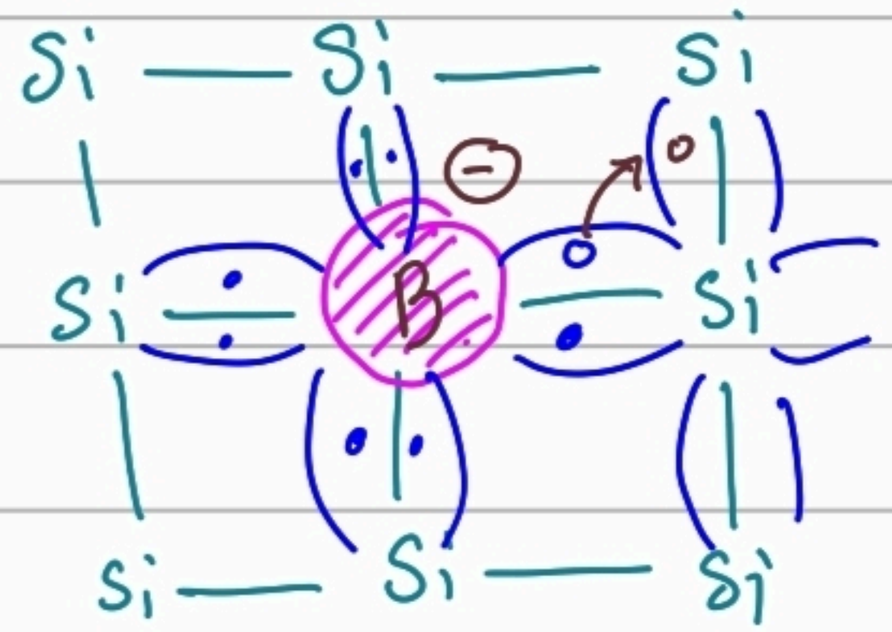
covalent bond

Extrinsic Semiconductor :- impurities are introduced artificially.

① P-type semiconductor: Doping → introduction of different atom in pure crystal.

Dopant atom : Group III A , Group 13 (B, Al)

ns^2np^1 $n = 2, 3, 4 \ldots$

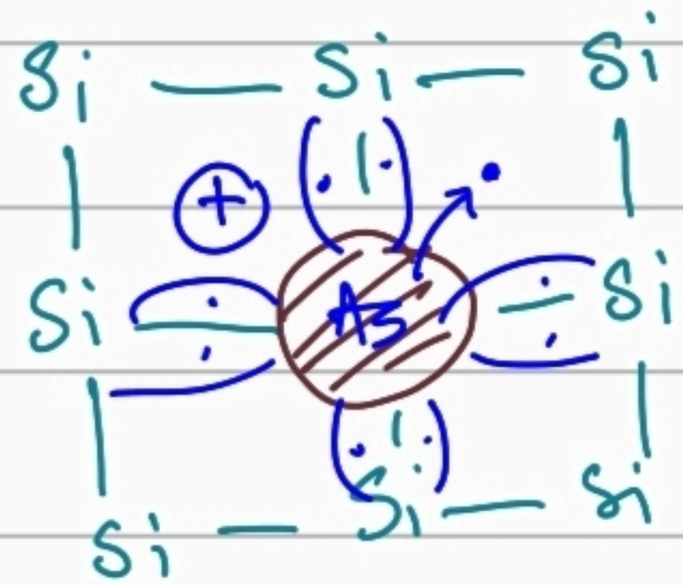


majority charge carrier is called hole. (h^+)

bound charge (-ve)

N-type Semiconductor :- Dopant atom : Group V. G-15

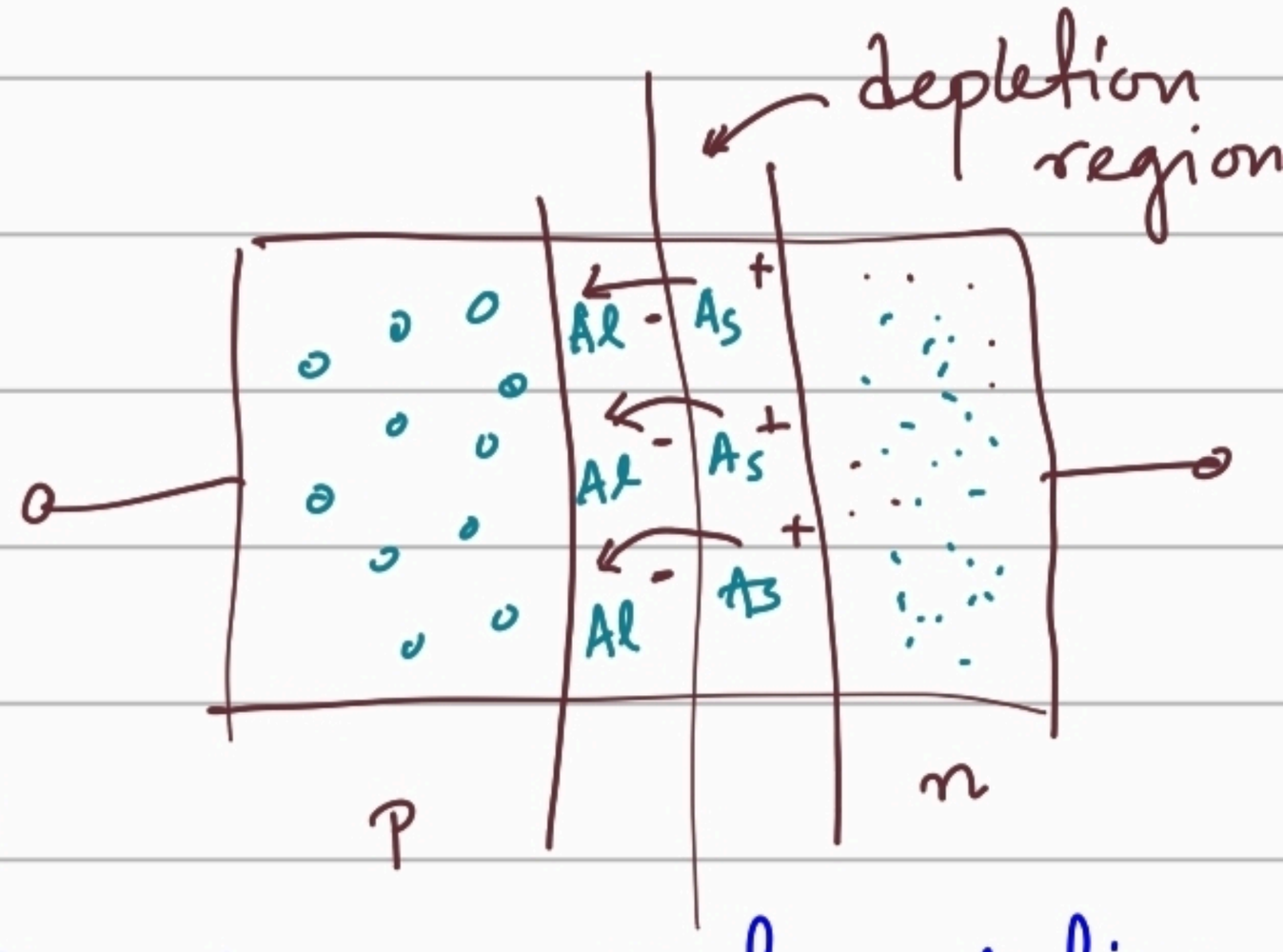
(As, P, Sb) ns^2np^3



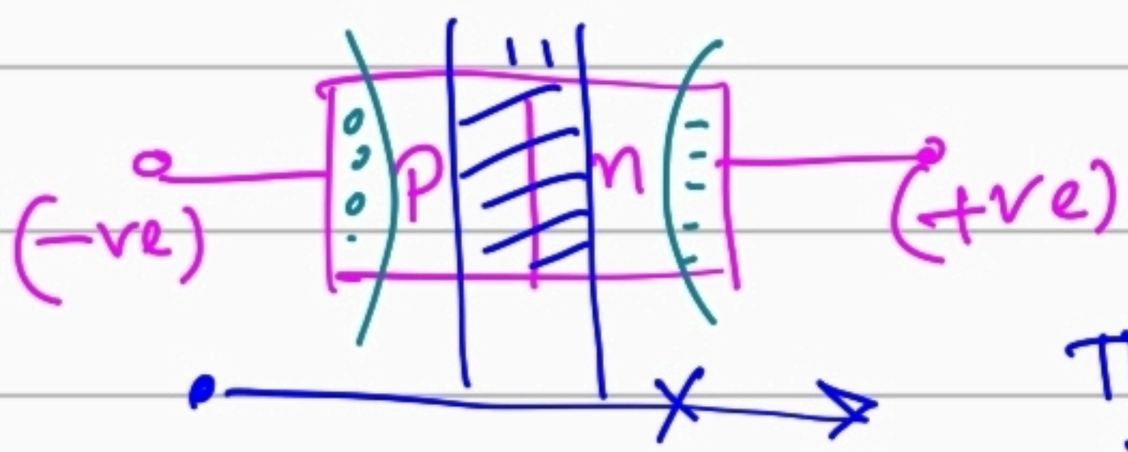
majority carrier → electron

bound charge is (+ve)

P-n junction diode :-



① Reverse Bias :-



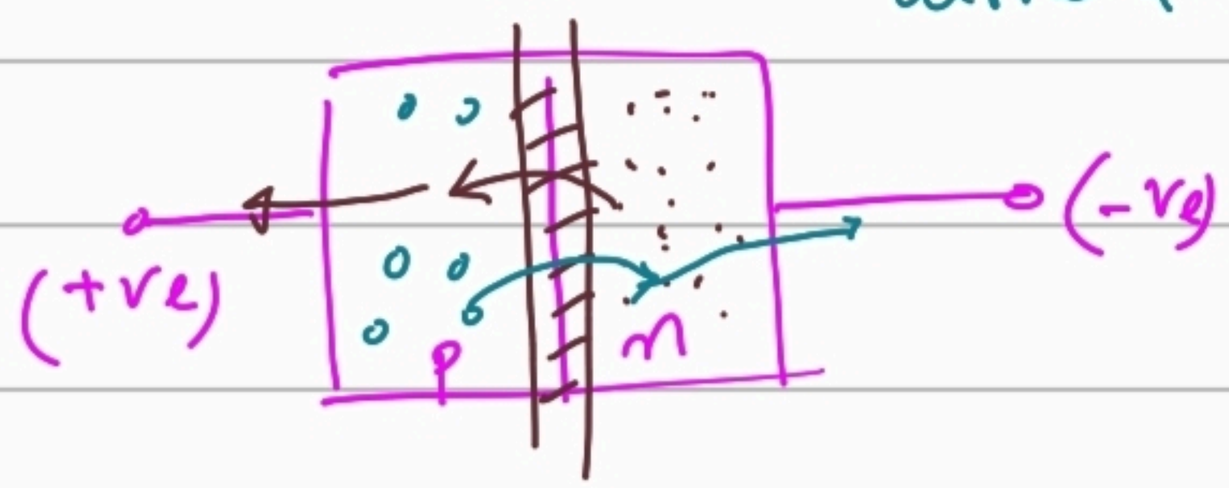
There is no current conduction in case of reverse bias.

Forward bias :-

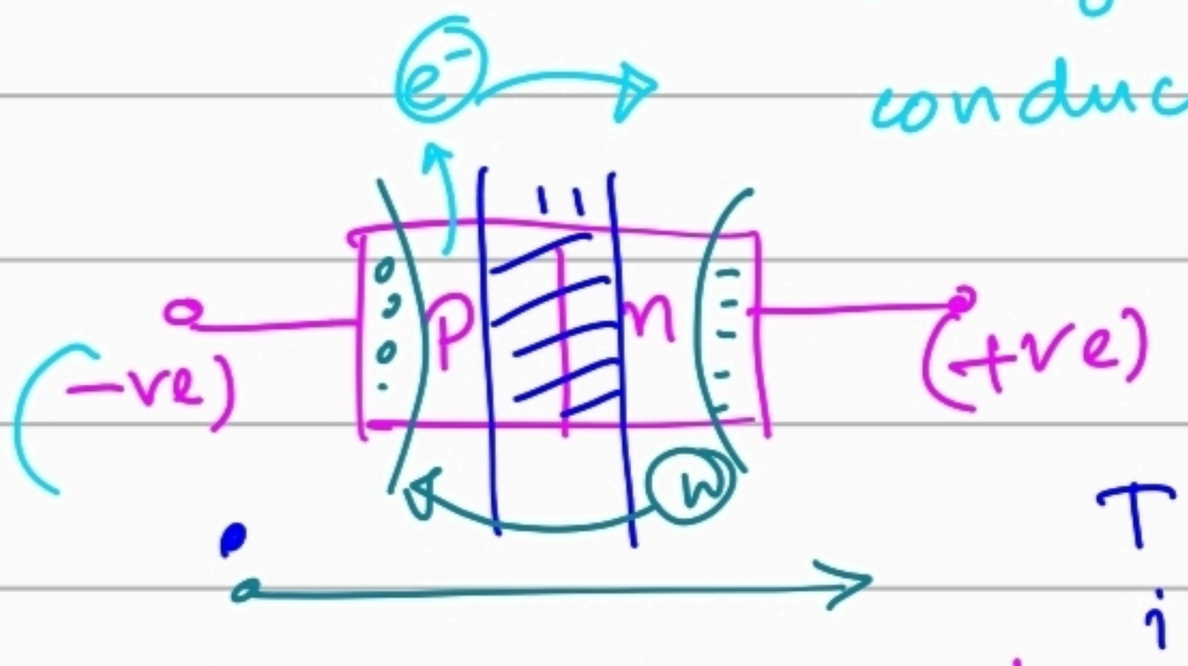
Si, $V_D > 0.6 \sim 0.7V$

Ge V_D $0.2 \sim 0.3V$

current flow



Breakdown :- If the applied reverse bias voltage is high then diode might start conduction.



typical Si diode 25 V

Zener diode ~ 5V, 10V

Diode → constant voltage drop model

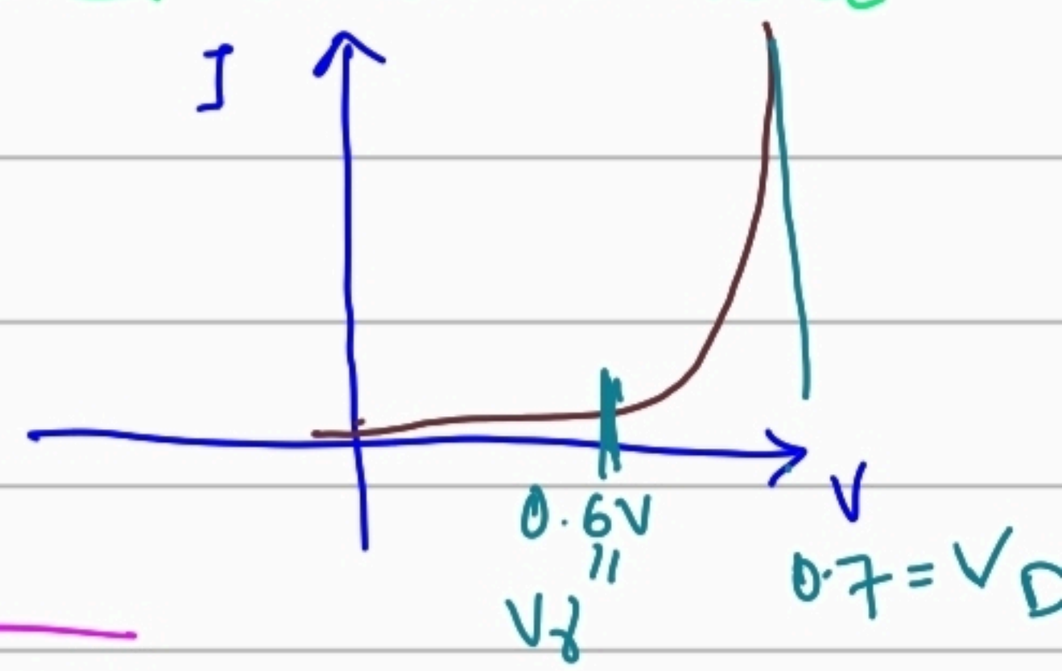
①

Diode conduction voltage, $V_D = 0.7V$

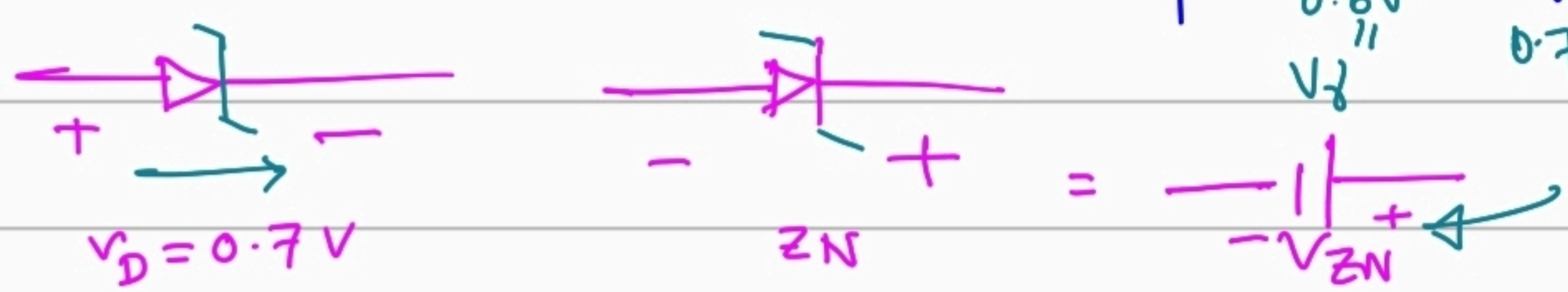
②

③ Activation / Threshold / Turn on voltage:

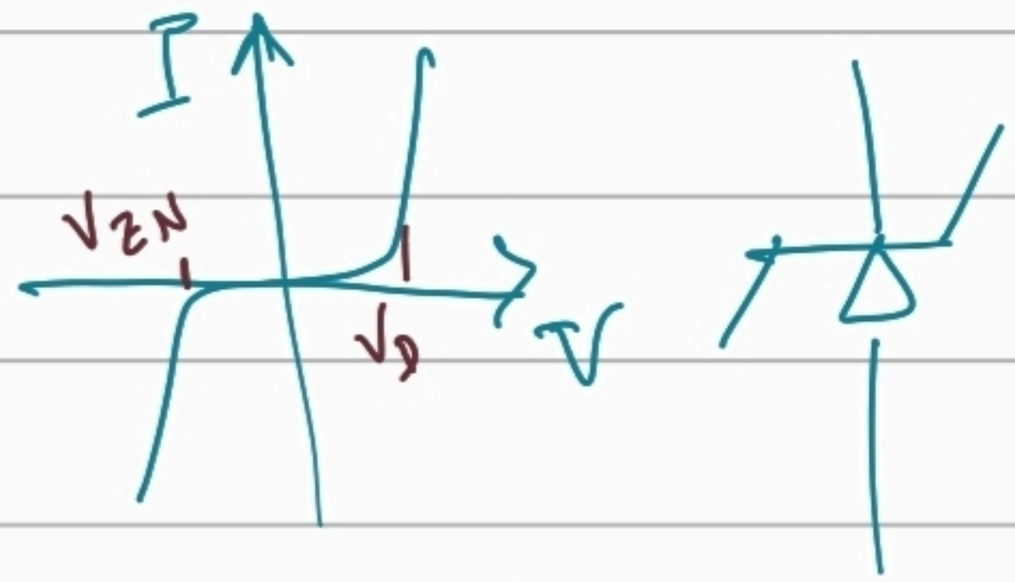
The minimum voltage required to turn on a diode. V_γ (diode) = 0.6 V



④ Zener Diode:



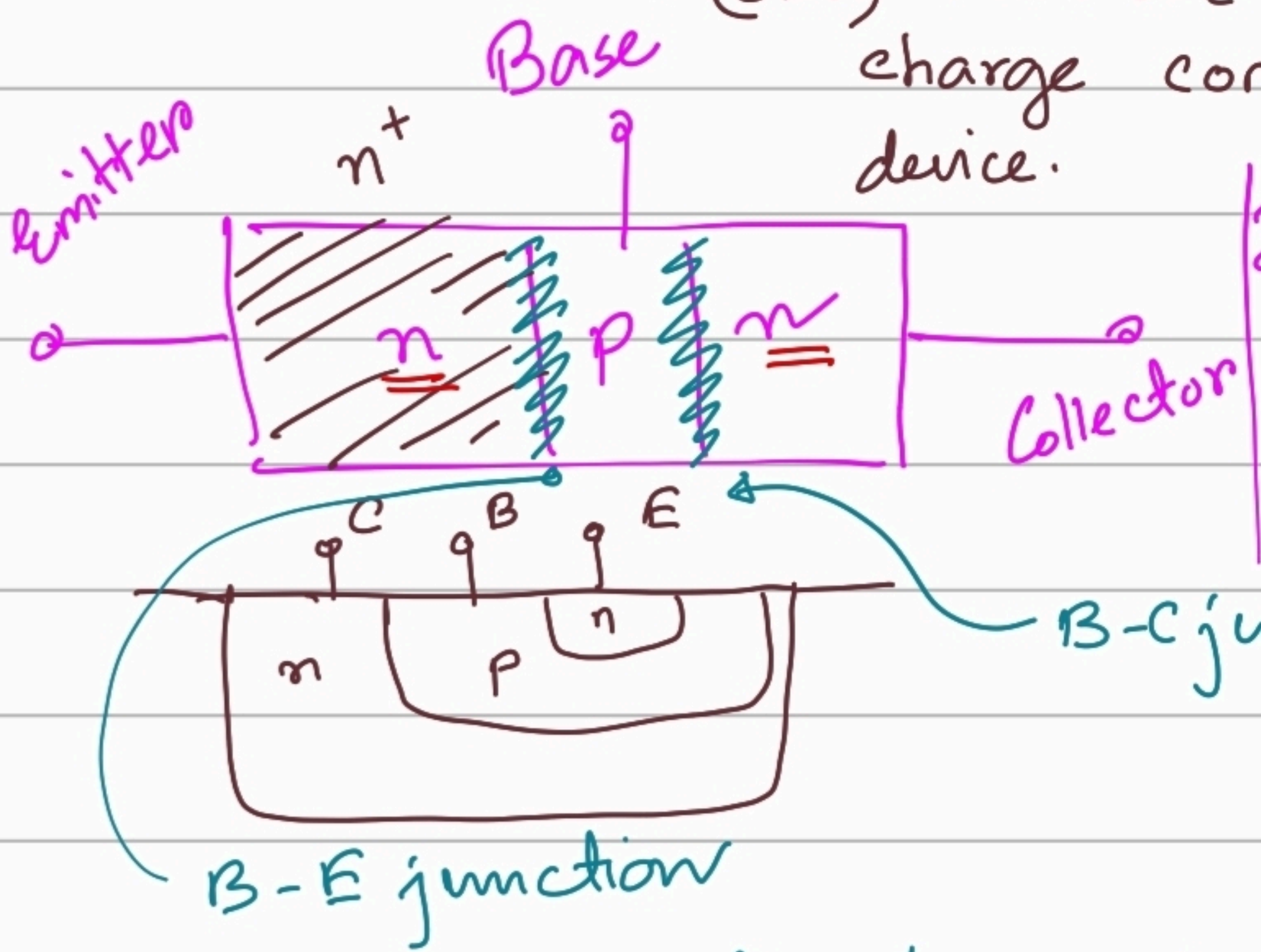
If the applied reverse bias voltage is higher than V_{ZN}, Zener diode starts conducting.



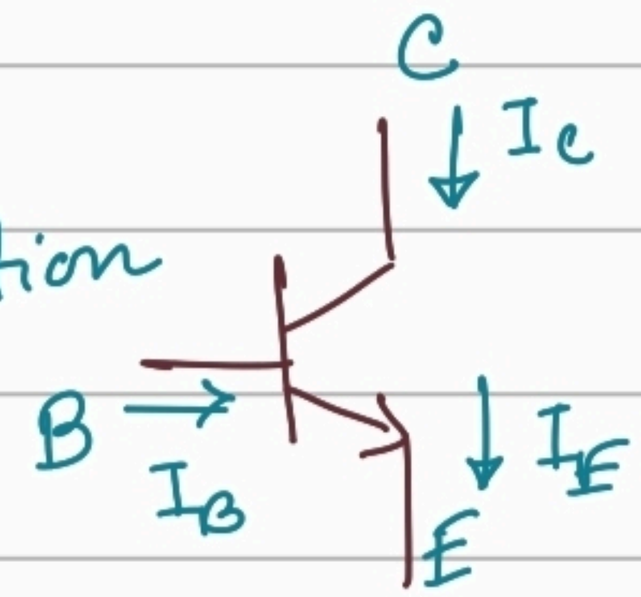
Transistor: Switching Device (~~Amplification~~)

n-p-n | Bipolar Junction Transistor (BJT)

(e-h) both are responsible for charge conduction in this device.



3 terminal devices



Depending junctions' operating mode BJT's operating mode can be classified into four different categories.

B-C junction	B-E junction	mode
Reverse	Forward	Forward Active (FA)
Forward	Forward	Saturation (S)
Reverse	Reverse	Cutoff (C)
Forward	Reverse	Reverse Active (RA)

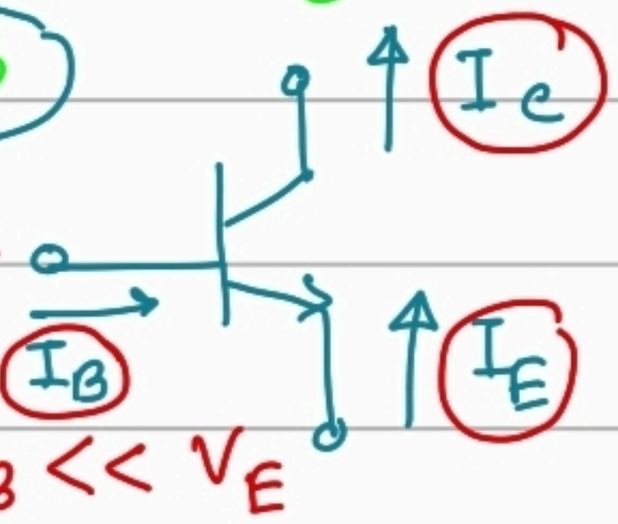
Reverse Active:

Emitter and Collector switche their roles.

$V_{BC} = 0.7V$, $\frac{I_E}{I_B} = \beta_R$

reverse β

$\beta_R \sim 0.1, 0.2, 0.3$



$V_C < V_B << V_E$

Cutoff: ($V_{BE} < 0$, $V_{BC} < 0$)

$V_{BE} < V_\gamma$ (transistor) = cutin voltage / turn on voltage $= 0.5V$

$$\boxed{I_C = I_B = I_E = 0}$$

0.5

Saturation

$V_{BE} > 0$, $V_{BC} > 0$

$\boxed{V_{BE} = 0.8V}$, $\boxed{V_{CE} = 0.2V / 0.1V}$

$V_{BC} = V_{BE} - V_{CE} = 0.6/0.7V$

Checking condition:

$I_C / I_B = \beta_{forced} < \beta_F$ (Forward)

Forward Active

$V_{BE} > 0$, $V_{BC} < 0$

$\boxed{V_{BE} = 0.7}$, $\boxed{\frac{I_C}{I_B} = \beta_F}$ 30, 50, 100

Forward β, common emitter current gain

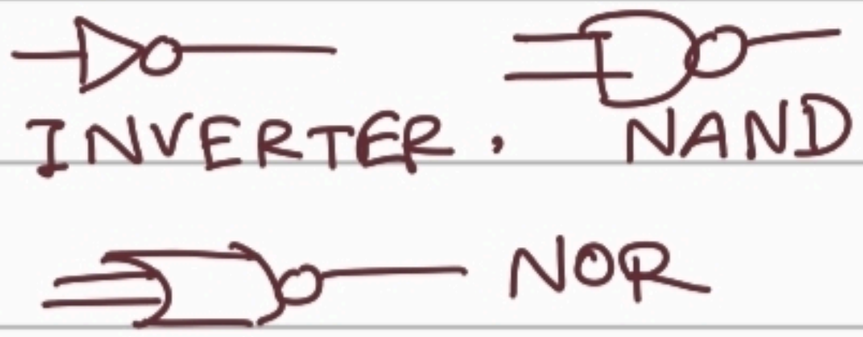
Checking condition:-

$V_{CE} > 0.2V$

$I_C + I_B = I_E$

Lecture 3: Introduction to Digital Logic Families

Digital logic design → { INVERTER, NAND, NOR }



Digital logic family are different groups of electronic circuits that can be used to construct digital logic gates.

Digital Logic family

Bipolar logic family
(electron and hole both contribute in current conduction)

B.J.T.

Saturated Logic family
(main transistors will operate in saturation and cutoff)

(a) Resistor Transistor Logic (RTL) ✓

(b) Diode Transistor Logic (DTL) ✓

(c) Direct Coupled Transistor Logic (DCTL)

(d) Integrated Injection Logic (IIL)

(e) High Threshold Logic (HTL) ✓

(f) Transistor transistor Logic (TTL) ✓

Unsaturated Logic family
(main transistors will operate in forward active and cutoff)

(a) Schottky TTL

(b) Emitter Coupled Logic (ECL) ✓

Unipolar logic family
(only single type of carrier contributes in current conduction) electron or hole.

JFET, MOSFET etc.

✓ (i) PMOS logic family

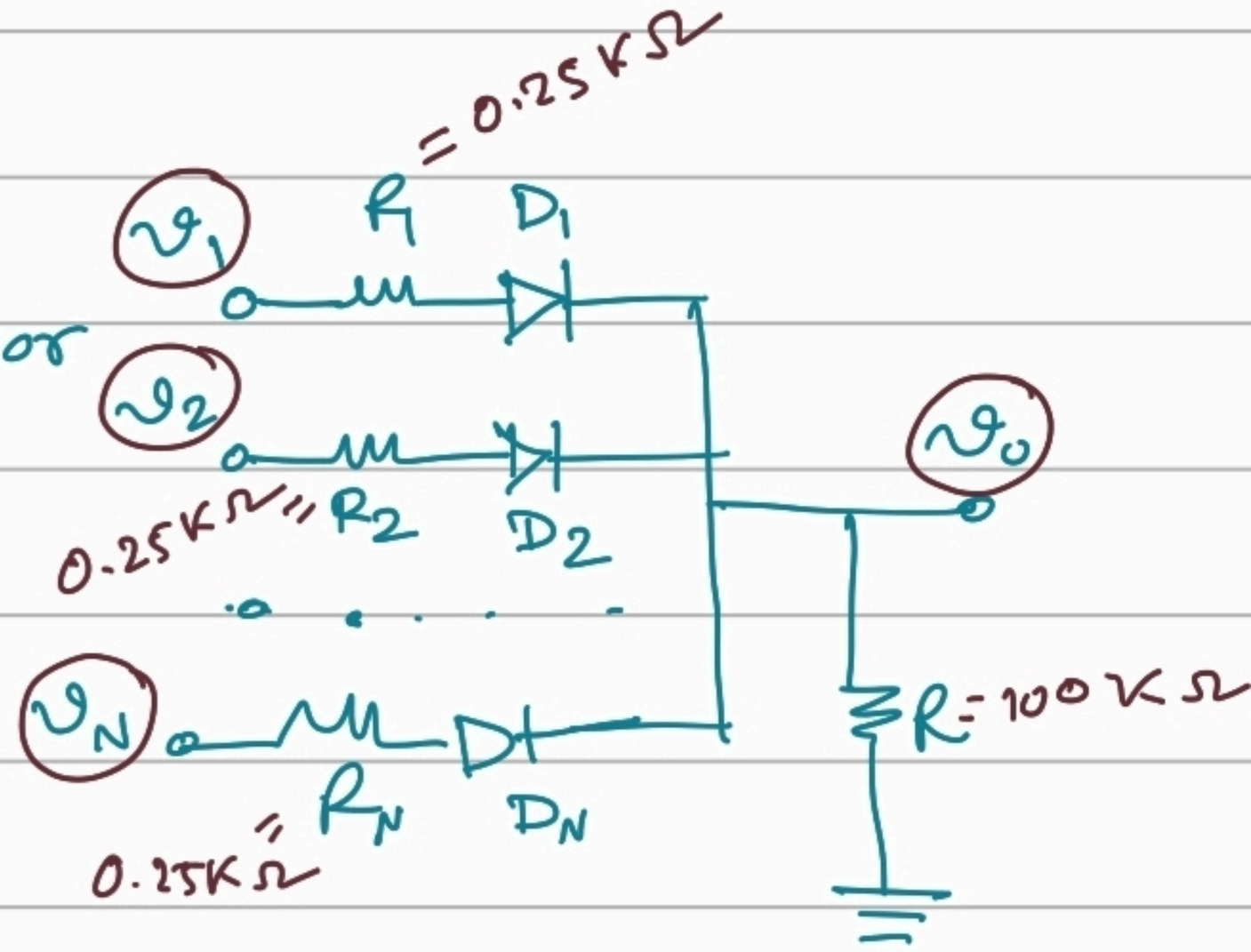
✓ (ii) NMOS " "

✓ (iii) CMOS " "

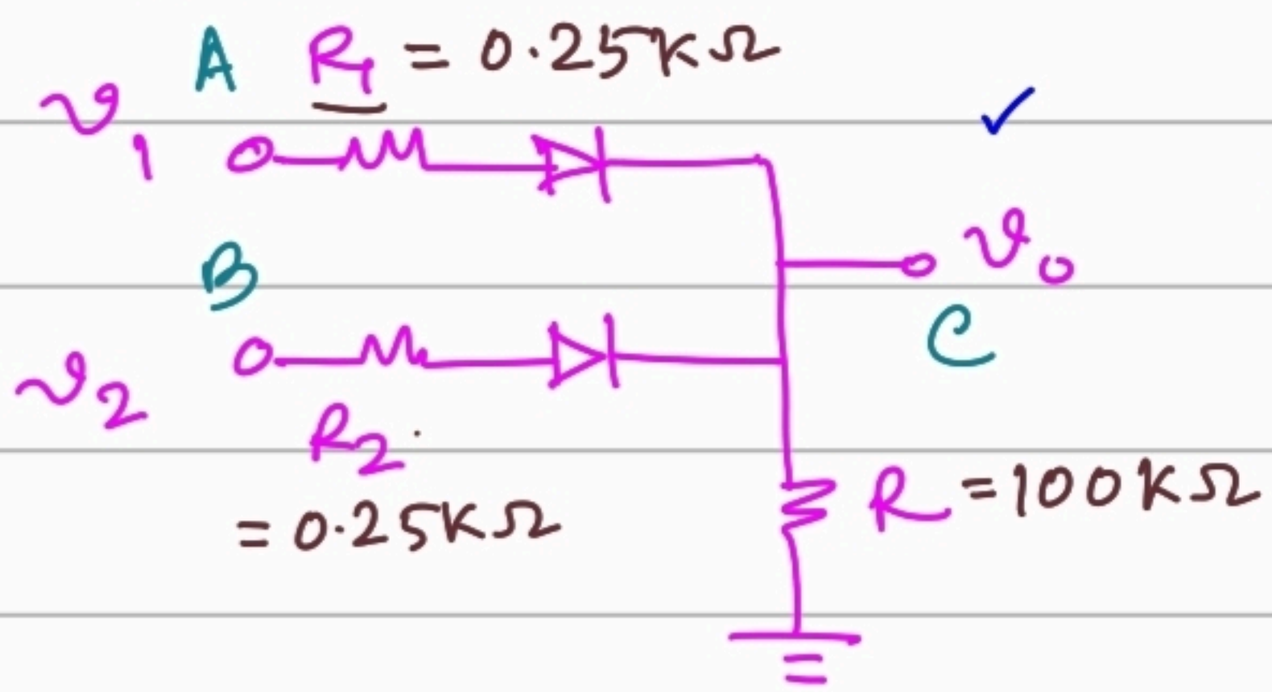
Diode Logic :-

OR GATE :-

N number of inputs for OR gate



Operation : 2-OR GATE

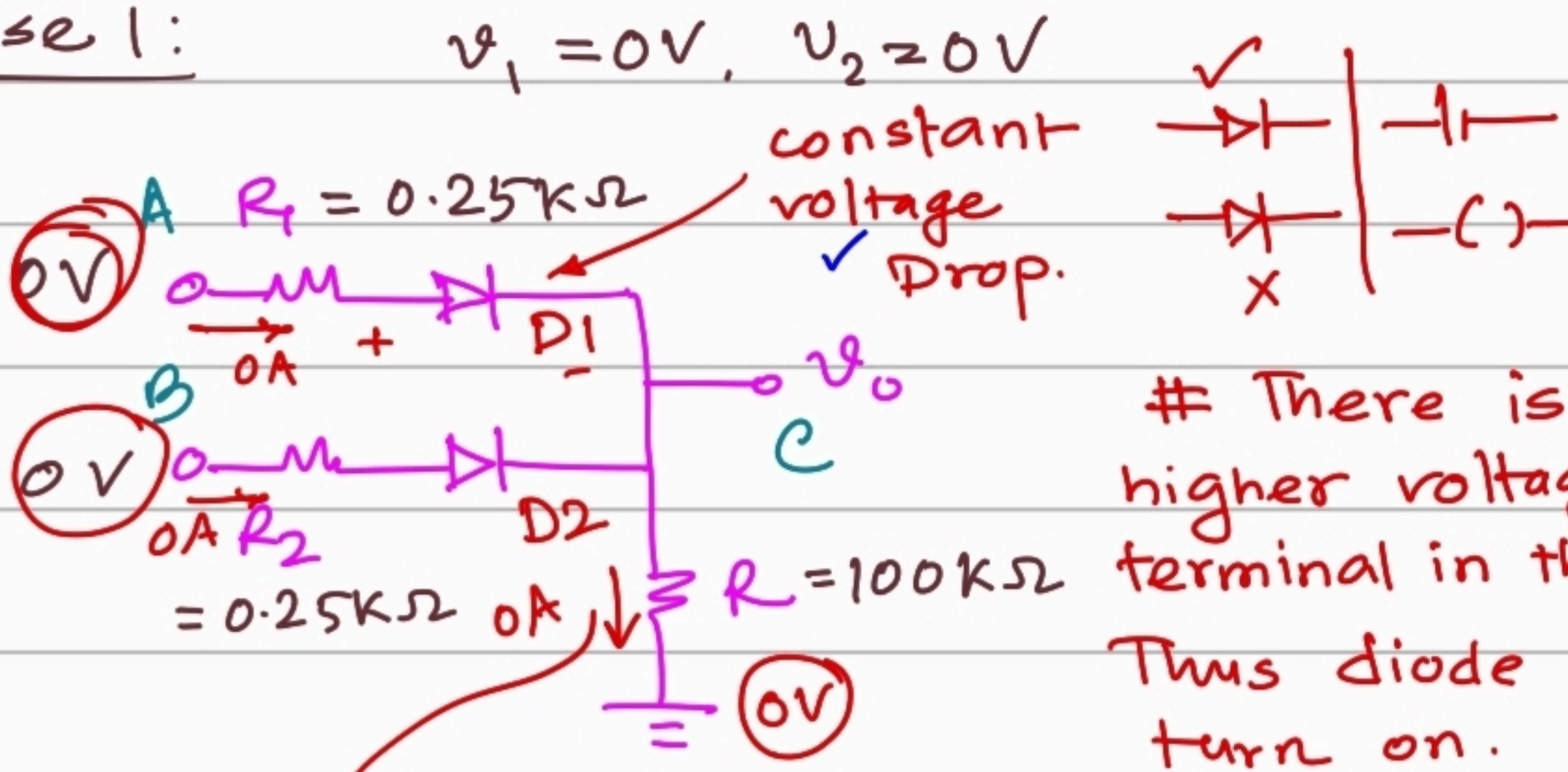


	A	B	v_1	v_2	v_o	C
1	0	0	0V	0V	0V	0
2	0	1	0V	5V	4.289	1
3	1	0	5V	0V	4.289	1
4	1	1	5V	5V	4.294	1

We will assume logic 1 for input part is 5V. and logic 0 for input part is 0V.

Case 1:

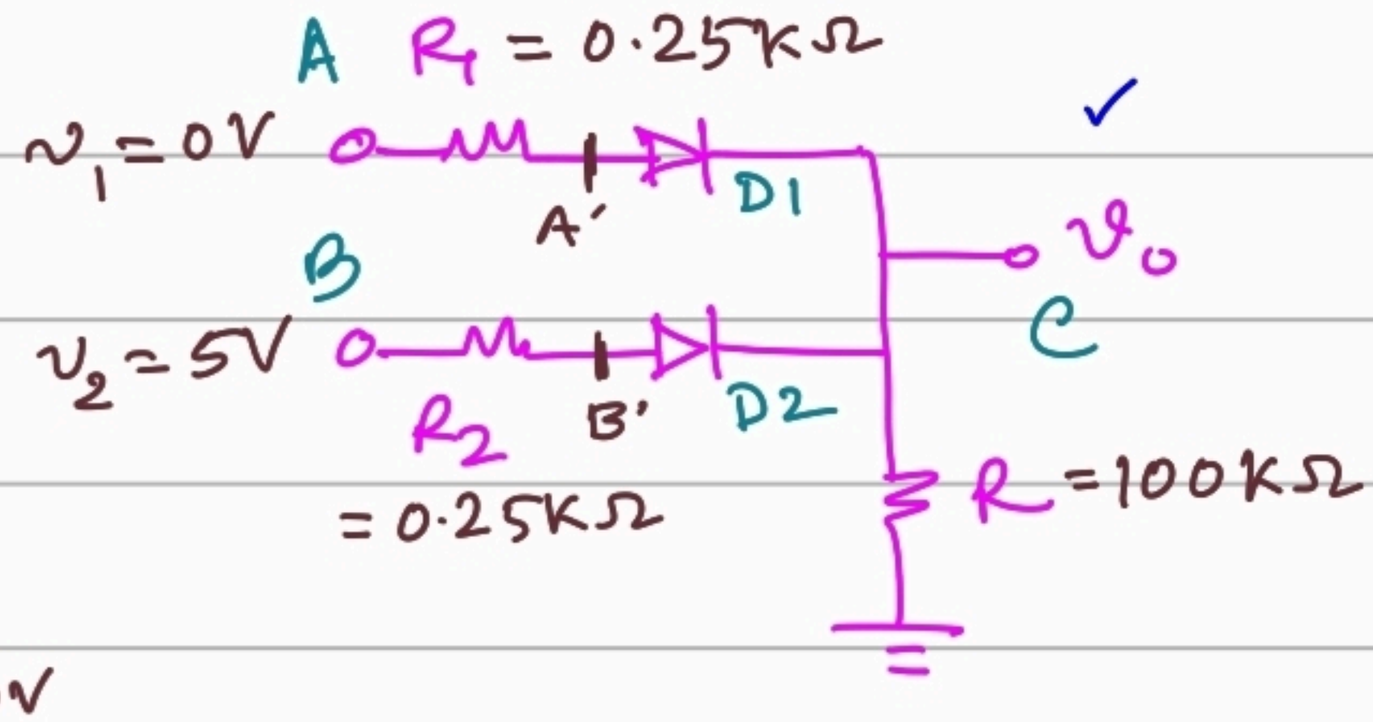
$v_1 = 0V$, $v_2 = 0V$



There is no higher voltage input terminal in this circuit. Thus diode will never turn on.

$$i = \frac{v_o - 0}{R} \Rightarrow 0 = \frac{v_o}{R} \therefore \boxed{v_o = 0V}$$

Case ②&③



Case ⓐ

* D1, OFF, D2, OFF

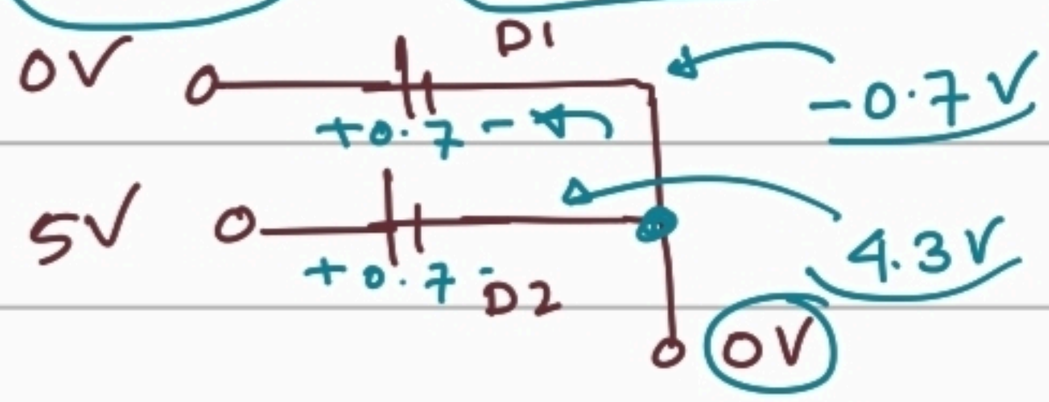
$v_{A'} = 0V, \; v_{B'} = 5V$

$v_o = 0V$.

Contradiction.

* D1 ON, D2 OFF. # Contradiction.

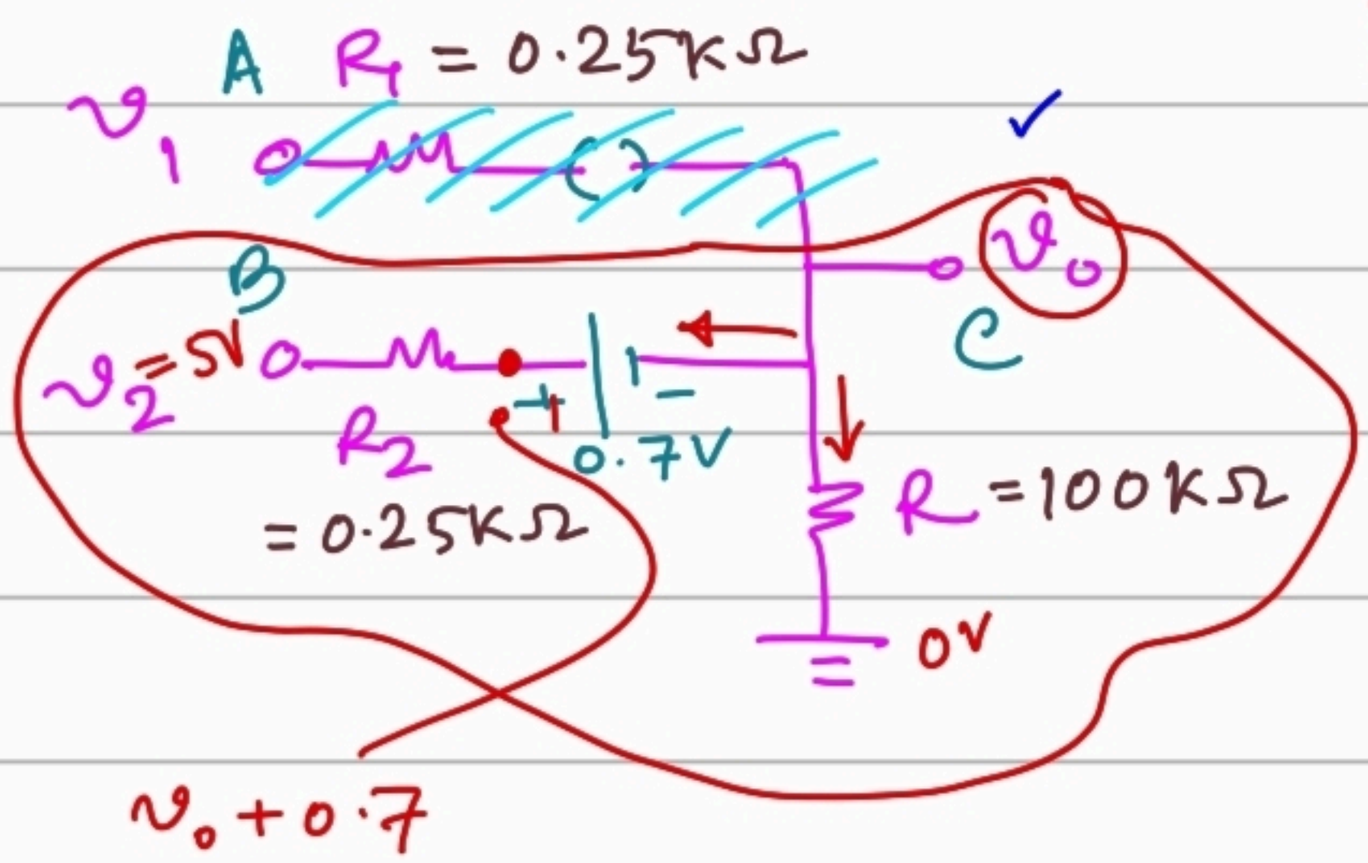
* D1 ON, D2, ON → Simplification



One node always has a single voltage.

If we do thorough analysis, we would find a contradictory result that current would flow in opposite direction through D1 diode.

* D1 OFF, D2 ON

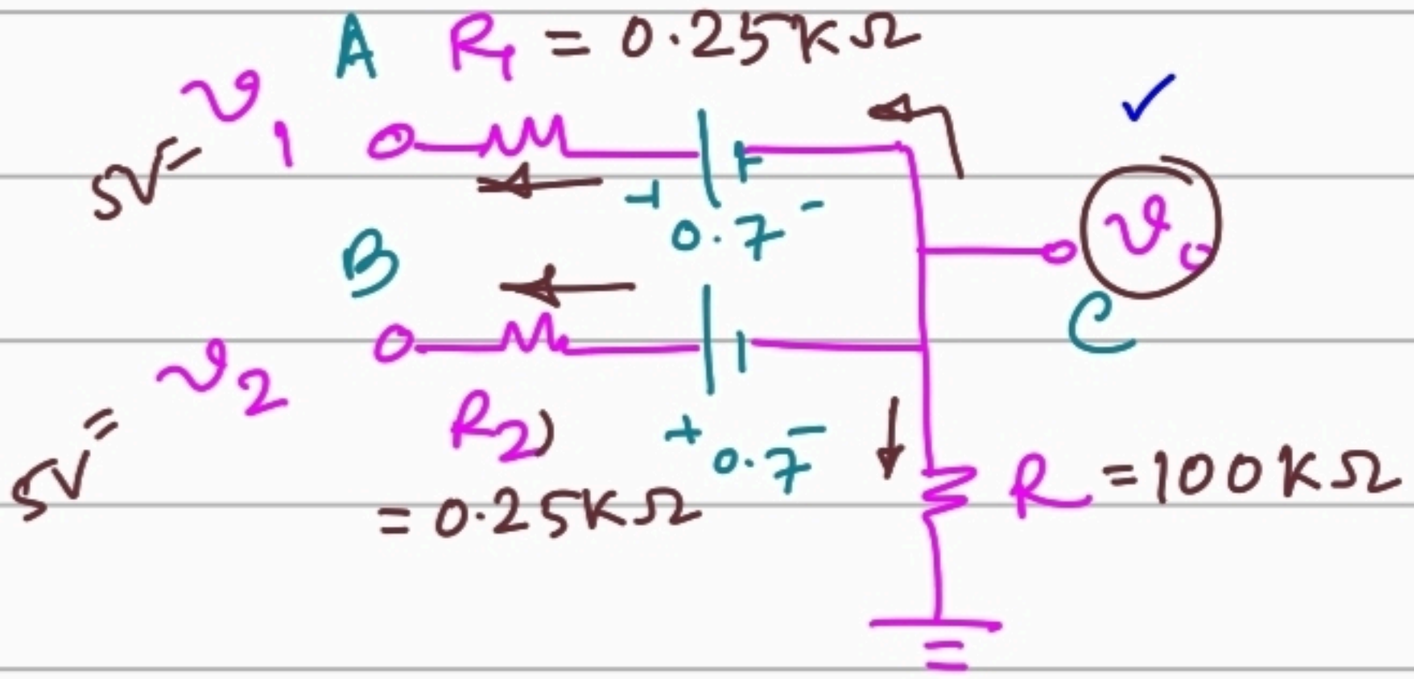


$$\frac{v_o - 0}{100K} + \frac{(v_o + 0.7) - 5V}{0.25K} = 0$$

$$\Rightarrow \boxed{v_o = 4.2893\ V}$$

Case 4: $v_1 = 5V, \; v_2 = 5V$

* D_1 ON, D_2 ON.



$$\frac{v_o - 0}{100K} + \frac{(v_o + 0.7) - 5V}{0.25K} \times 2 = 0$$

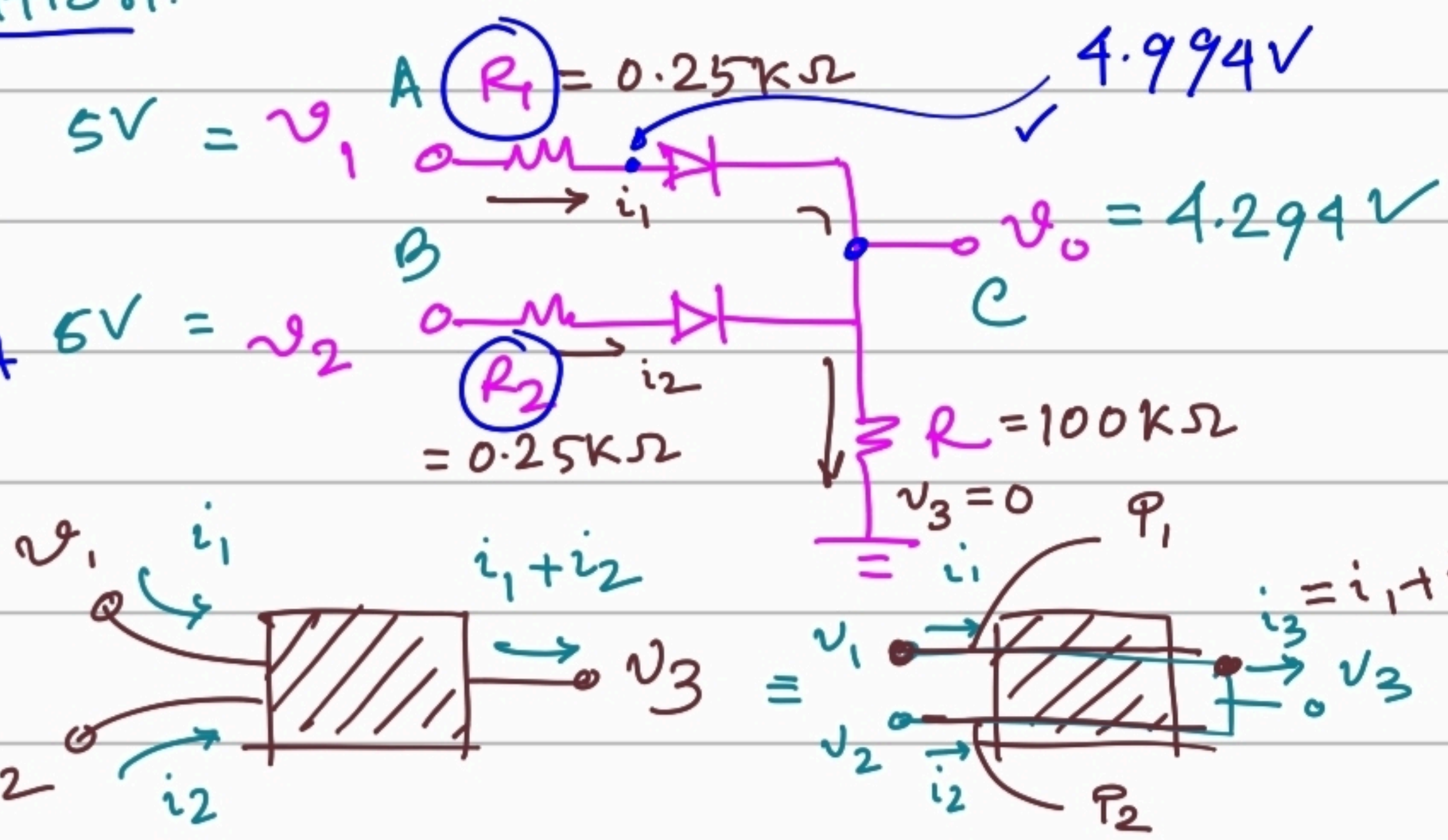
$$v_o = 4.2946V$$

$\boxed{4.289 \,,\; 4.294}$ We will choose the smallest of the high voltage as output voltage high.

$$v_{OH} = 4.289\,V$$

Power Dissipation :- Maximum dissipation of power among four cases.

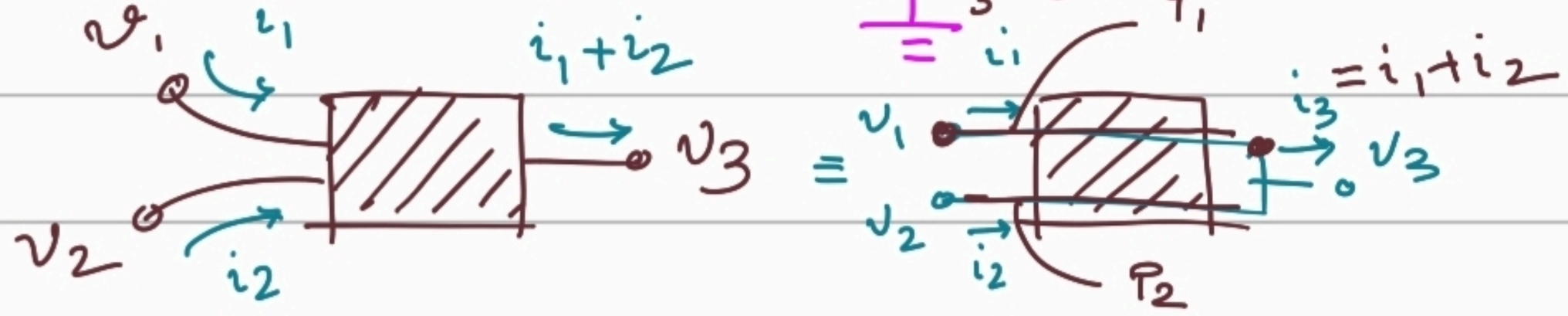
Case 4 : Each individual branch is conducting current, Thus it has maximum power dissipation.



$$i_1 = \frac{5 - 4.994}{0.25K} = 0.0215\,mA$$

$$i_1 = i_2$$

Theory:



$$P_1 = (v_1 - v_3)\, i_1 \,, \quad P_2 = (v_2 - v_3)\, i_2$$

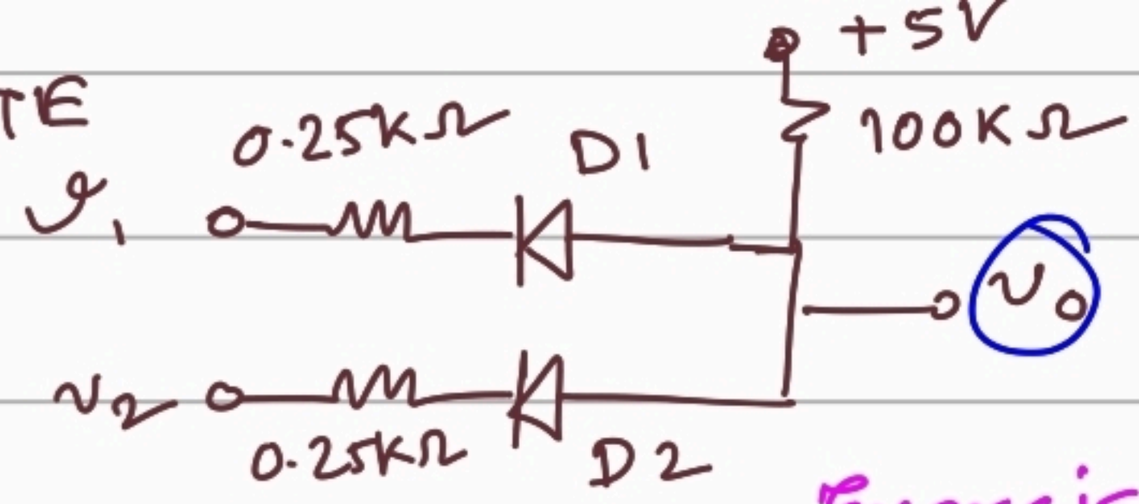
Total power, $P = P_1 + P_2$

$$P_2 = P_1 = (5 - 0)V(0.0215\,mA) \Rightarrow P = 0.215\,mW$$

$$V \cdot \mu A = \mu W$$

AND GATE: 2-AND GATE

v_1	v_2	v_o	D1	D2
5V	5V	5V	OFF	OFF
5V	0V	x	OFF	ON
0V	5V	x	ON	OFF
0V	0V	x	ON	ON



Exercise

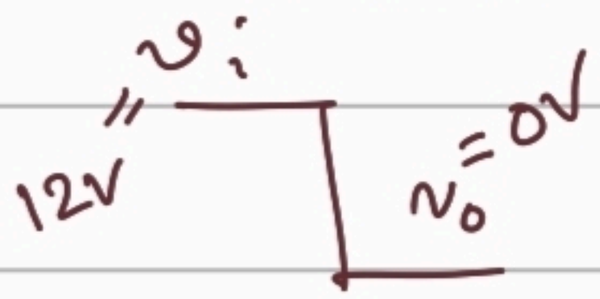
0.68 – 0.7 V

For choosing output logical low, we will take max of the logical output low.

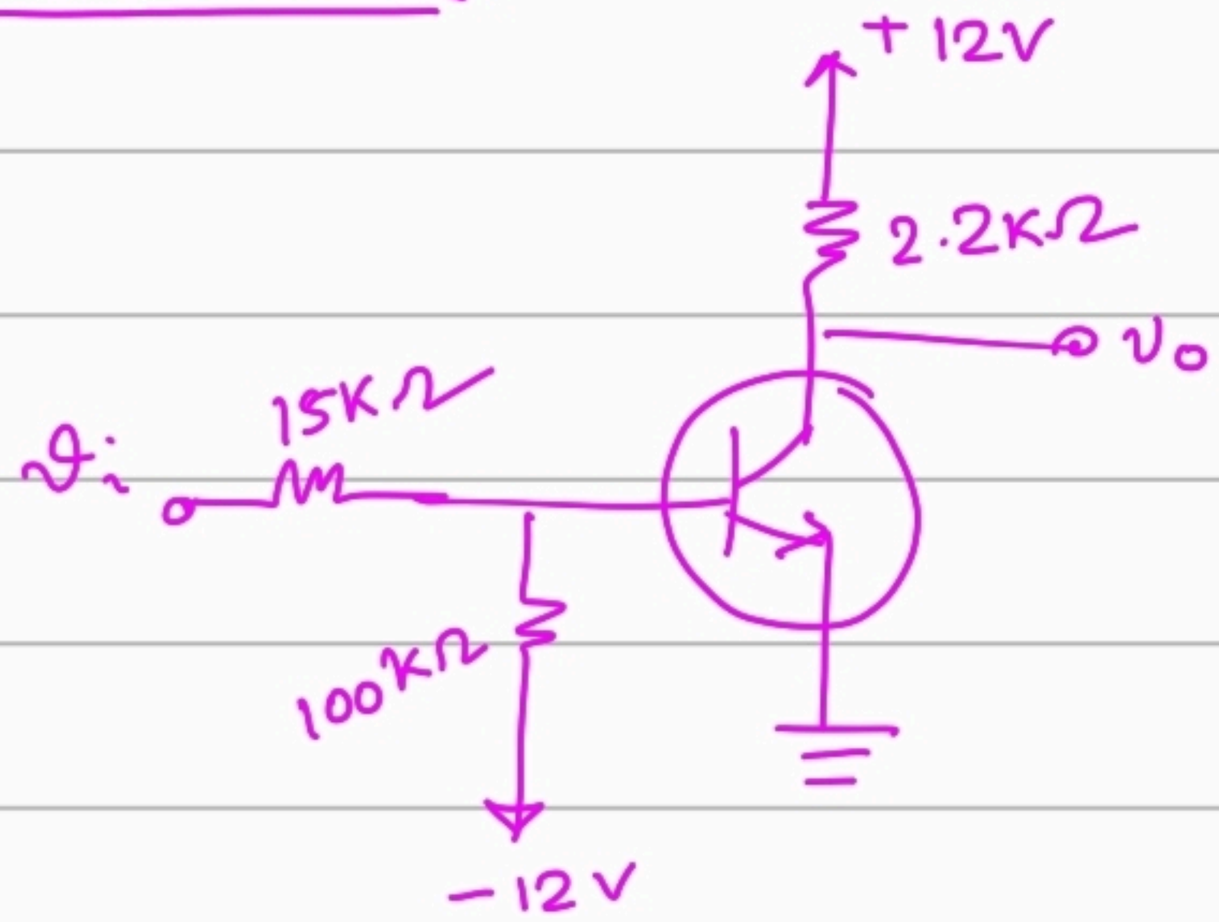
$V_{OL} = 0.7V$] all voltages below this voltage would be considered logical low.

Registor Transistor Logic (RTL)

RTL INVERTER:-



v_i	v_o
1	0
0	1



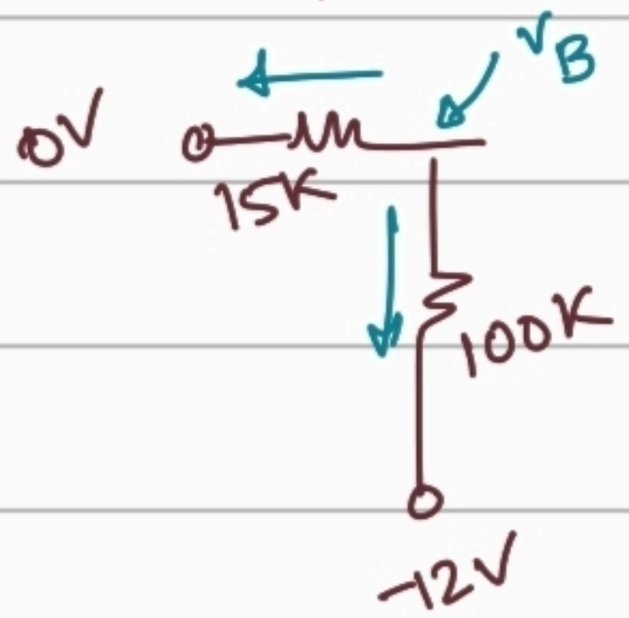
input logical

hi = +12V

low = 0V

Case 1 : $v_i = 0V$

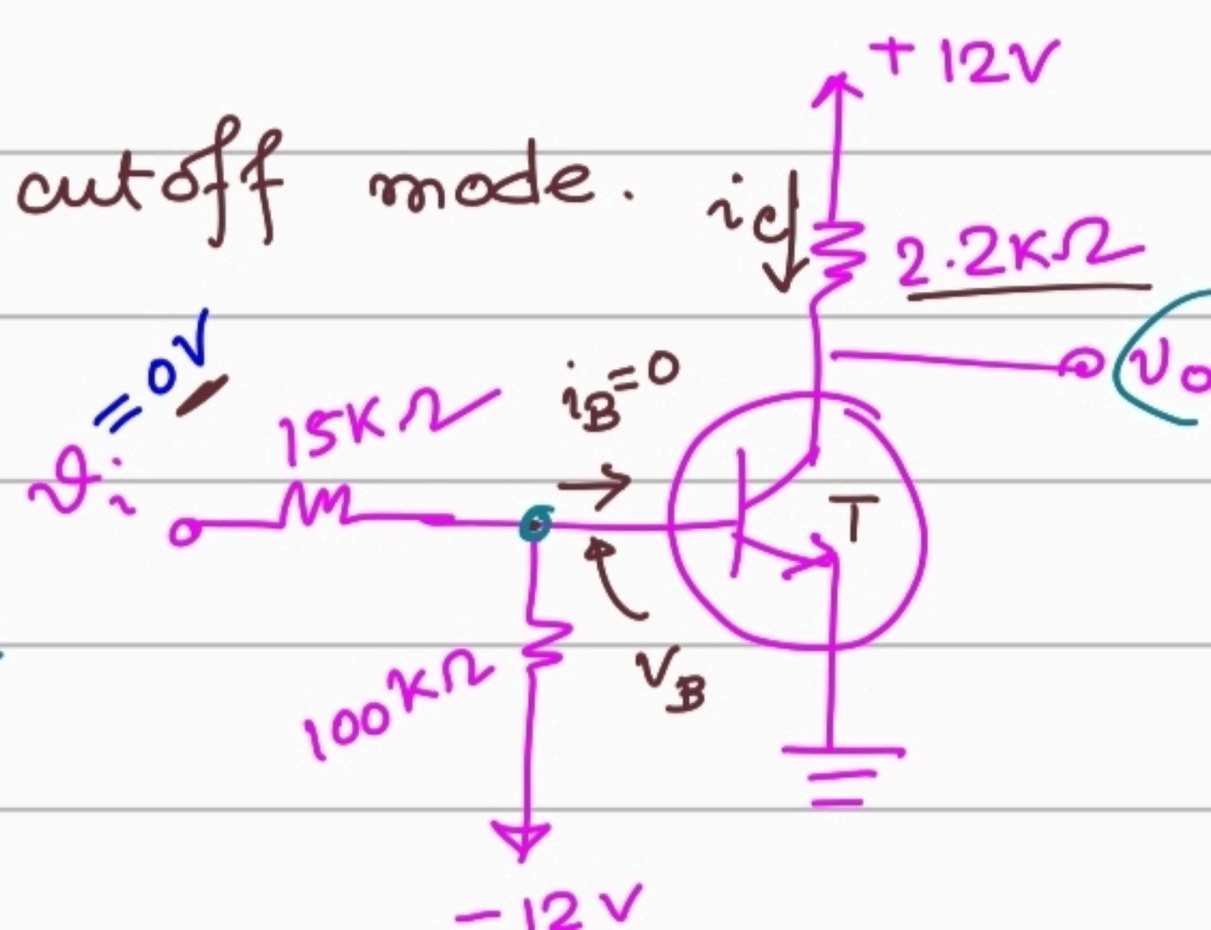
Guess/Assumption: T is in cutoff mode.



$$\frac{V_B-(-12)}{100K} + \frac{V_B-0}{15K} = 0$$

$\Rightarrow V_B = -1.565V$

$V_E = 0V$



Verification: $V_\gamma = V_{BE}$ (cutin voltage) $\leq 0.5V$

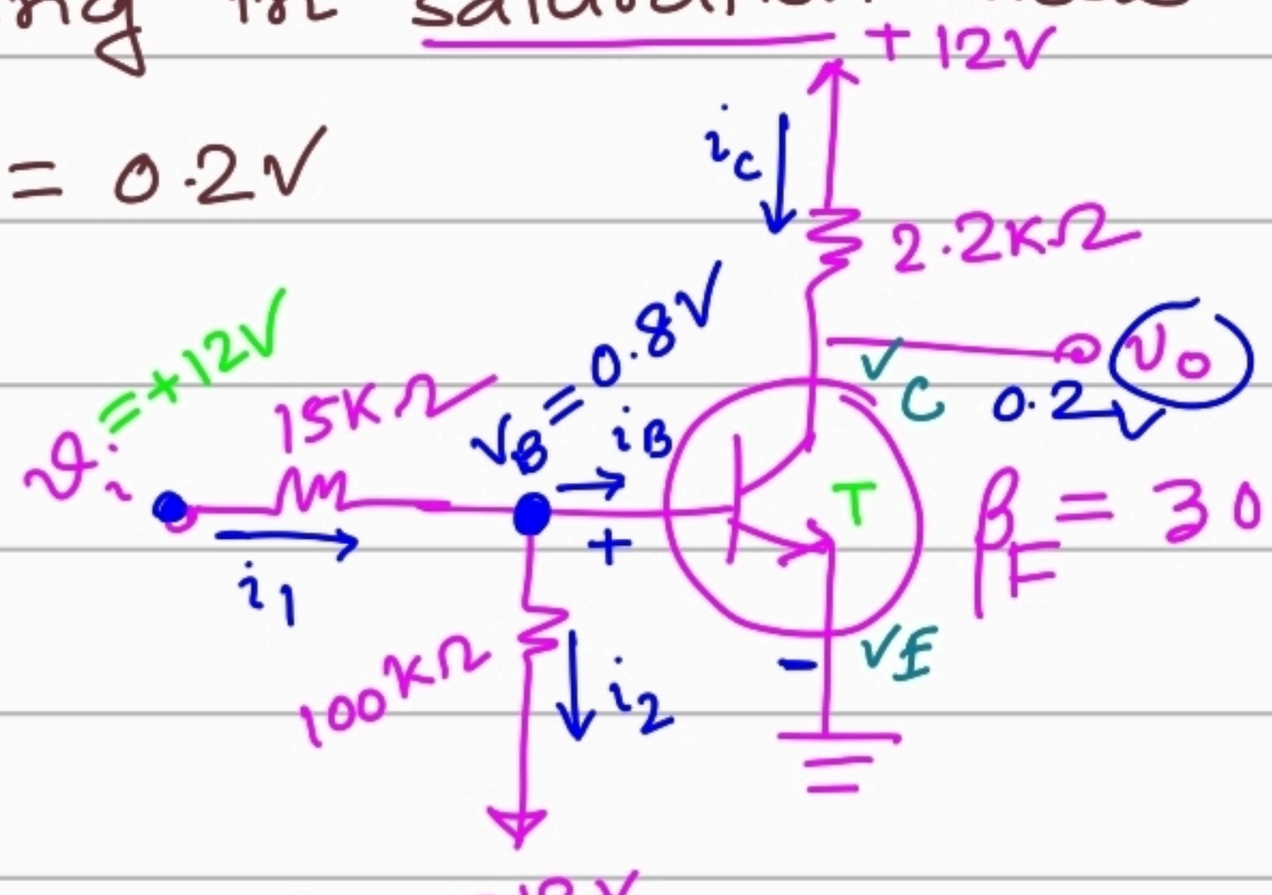
$V_{BE} = -1.565V < 0.5V$ (Our assumption is valid)

For cutoff mode. $i_C = i_B = i_E = 0\,mA$

$$i_C = \frac{12 - v_o}{2.2K} = 0 \Rightarrow \boxed{v_o = 12V}$$ logical high Output voltage.

Case ②: $v_i = +12V$

Assumption: T is operating in saturation mode.



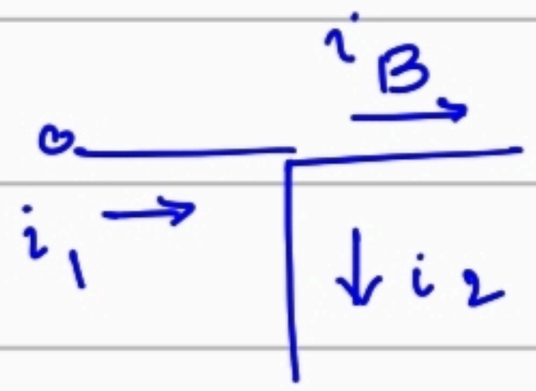
★ $v_o = V_C = V_C - V_E = V_{CE} = 0.2V$

★ $i_C = \frac{12 - 0.2}{2.2K} = 5.36\,mA$

★ $i_1 = \frac{12 - 0.8}{15K} = 0.746\,mA$

★ $i_2 = \frac{0.8 - (-12)}{100K} = 0.128\,mA$

When transistor is operating in saturation mode $V_{BE} = 0.8V$, $V_{CE} = 0.2V/0.1V$



$i_B = i_1 - i_2 = 0.619\,mA$

Verification: $\beta_{forced} = \frac{i_C}{i_B} = 8.659 < 30 = \beta_F$

Our assumption is valid.

Thus our analysis shows output voltage is now 0.2V. = logical low voltage at the output terminal.

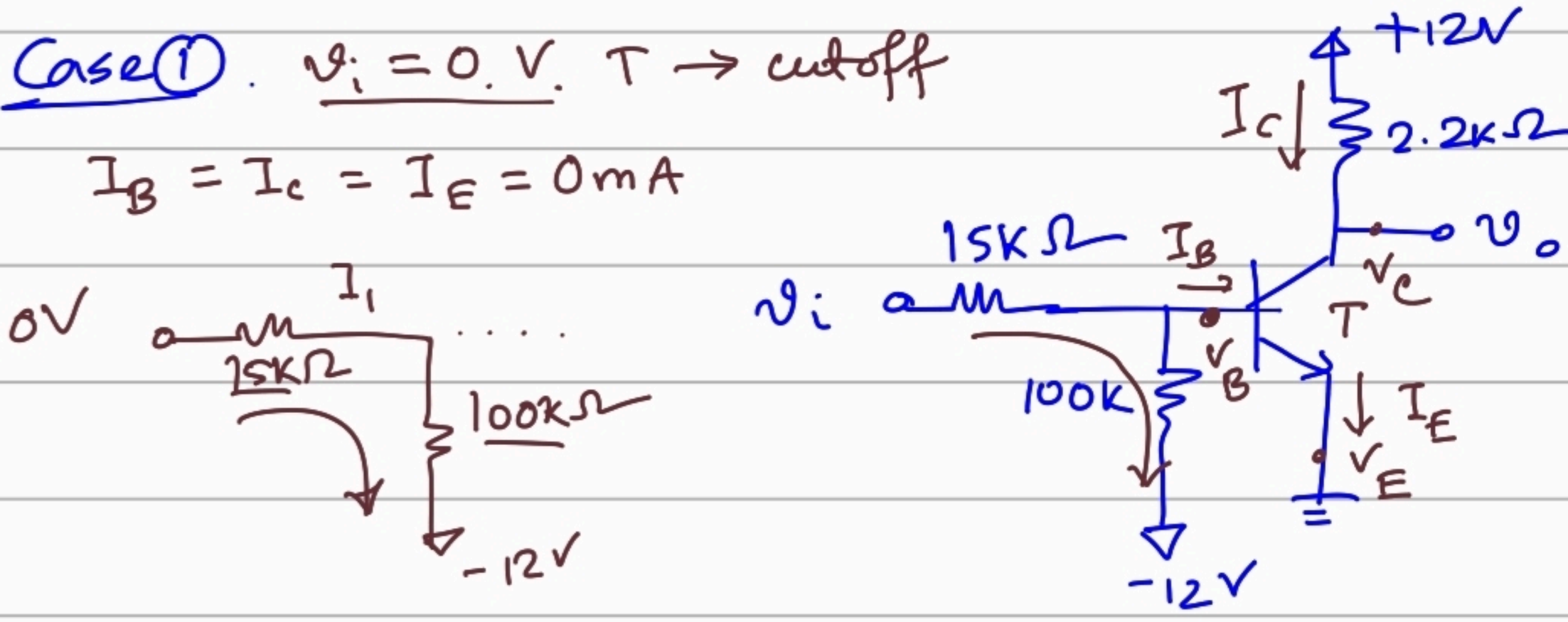
$V_{OL} = 0.2V$

Lecture 4: RTL circuits : Power dissipation, Noise Margin and Fanout Calculation.

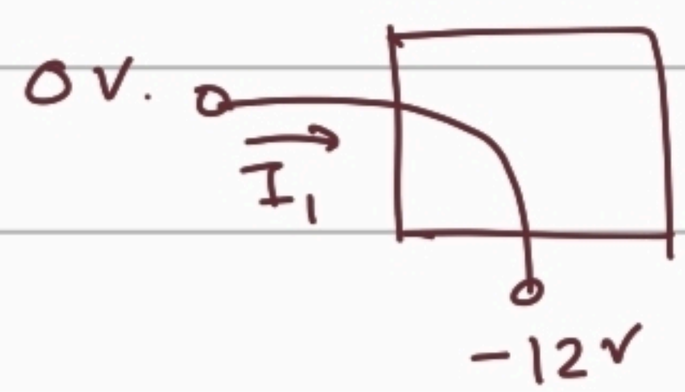
Power dissipation in RTL inverter :-

Case ① $v_i = 0\,V$. $T \rightarrow$ cutoff

$I_B = I_C = I_E = 0\,mA$



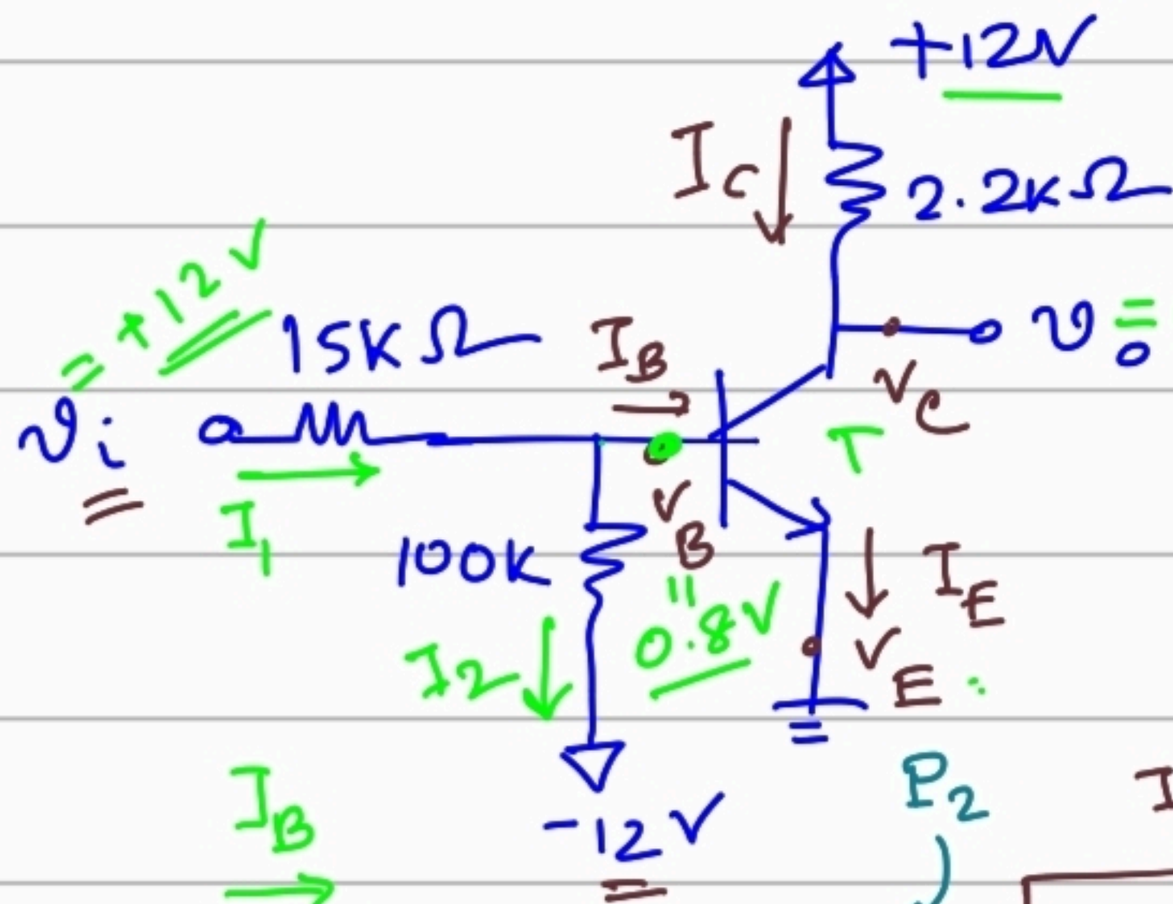
$$I_1 = \frac{0-(-12)}{115k\Omega} = 0.104\,mA$$



$$P = (0-(-12)) \times 0.104$$
$$= \boxed{1.2521\,mW}$$

Case ② $v_i = +12V$. $T \rightarrow$ saturation (RTL)

$V_{BE} = 0.8V$, $V_{CE} = 0.2V$ (0.1V)

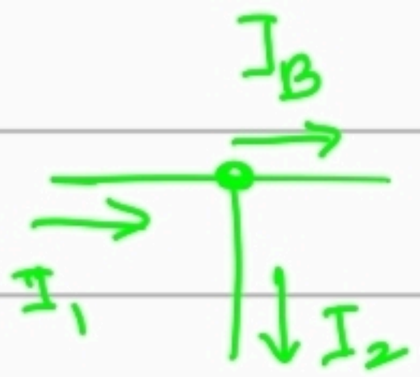


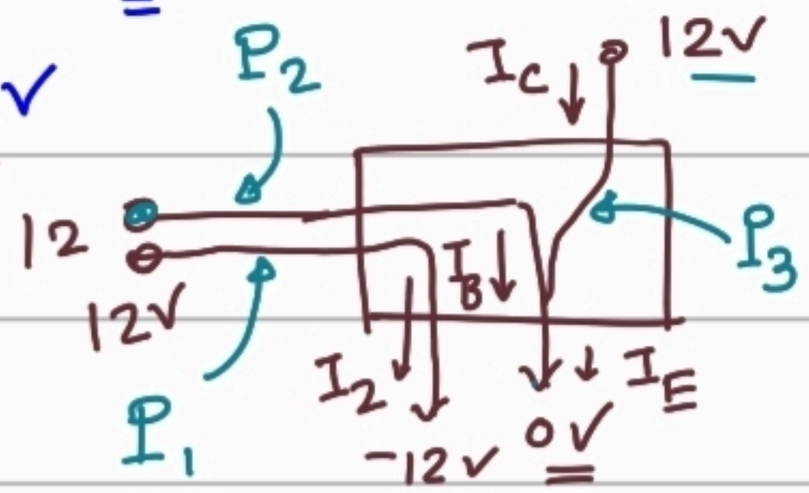
$$I_C = \frac{12-0.2}{2.2K} = 5.3636\,mA$$

$$I_1 = \frac{12-0.8}{15K} = 0.7466\,mA$$

$$I_2 = \frac{0.8-(-12)}{100K} = 0.128\,mA$$

$$I_B = I_1 - I_2 = 0.6186\,mA$$





$$P_1 = (12-(-12)) \times 0.128$$
$$= 3.072\,mW$$

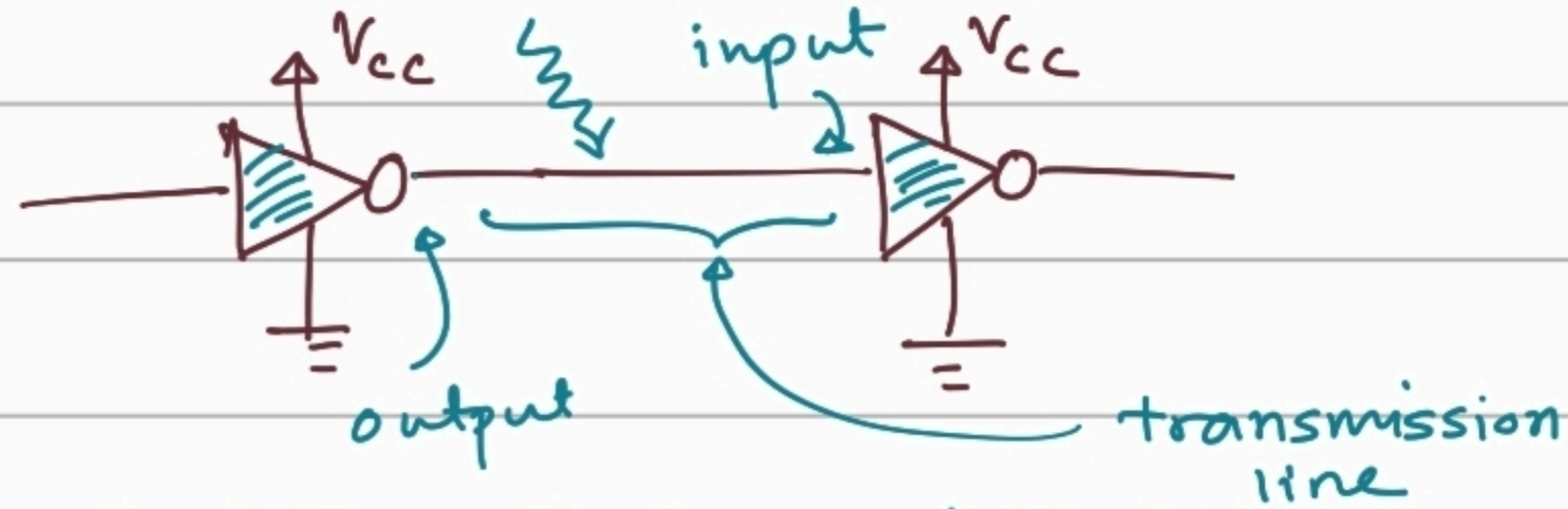
$$P_2 = (12-0) \times 0.6186$$
$$= 7.4323\,mW$$

$P_3 = (12-0) \times 5.3636 = 64.3632\,mW$

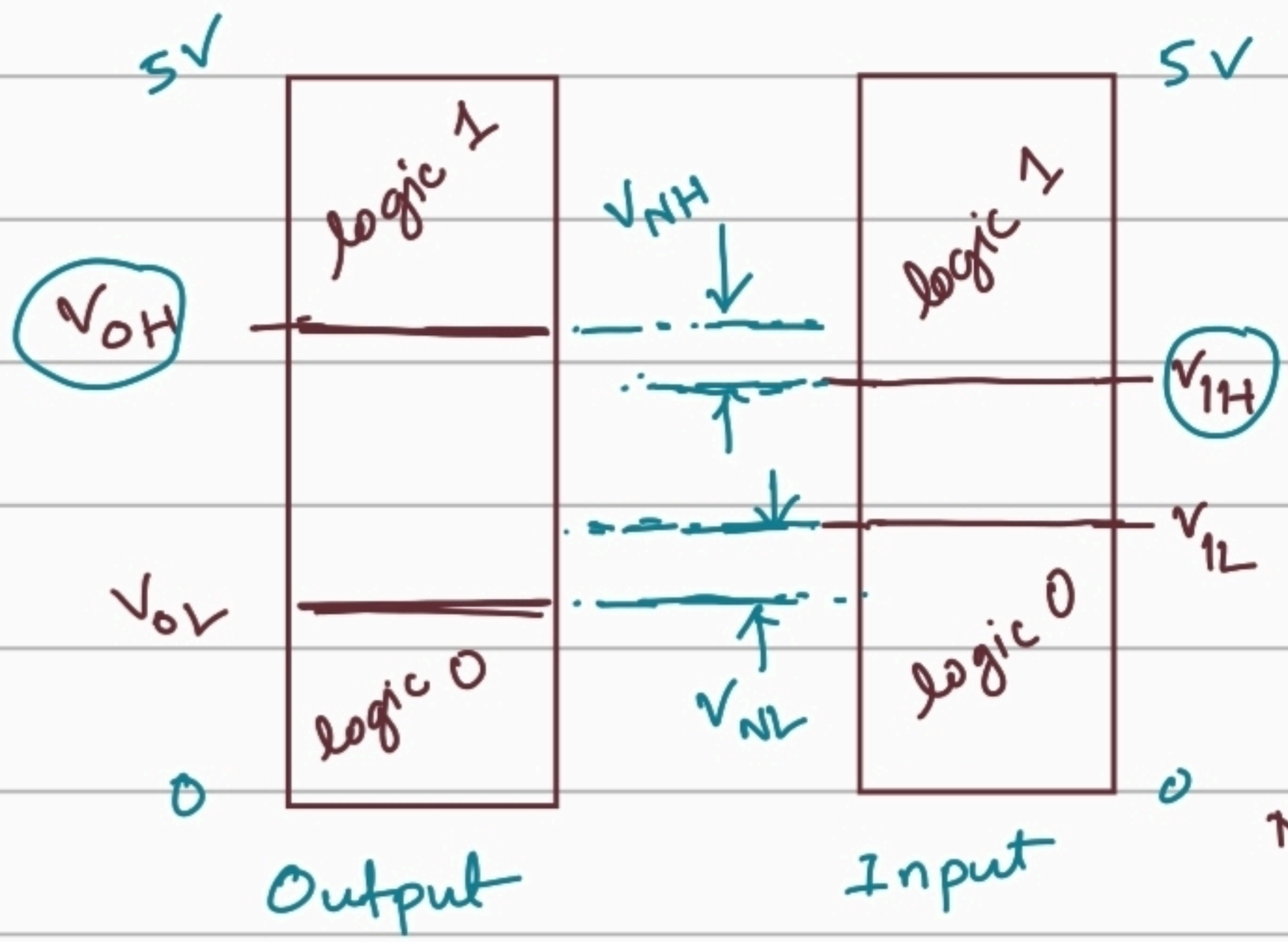
Total power dissipation, $P = P_1 + P_2 + P_3 = \boxed{74.8534\,mW}$

NOISE MARGIN:-

The amount of noise voltage a digital logic circuit can tolerate while successful transmission.



We model different types interference or noises using "noise voltage."



HIGH state noise margin:

$V_{NH} = V_{OH} - V_{IH}$

LOW state noise margin

$V_{NL} = V_{IH} - V_{OH}$

Noise margin.

$V_N = \min(V_{NH}, V_{NL})$

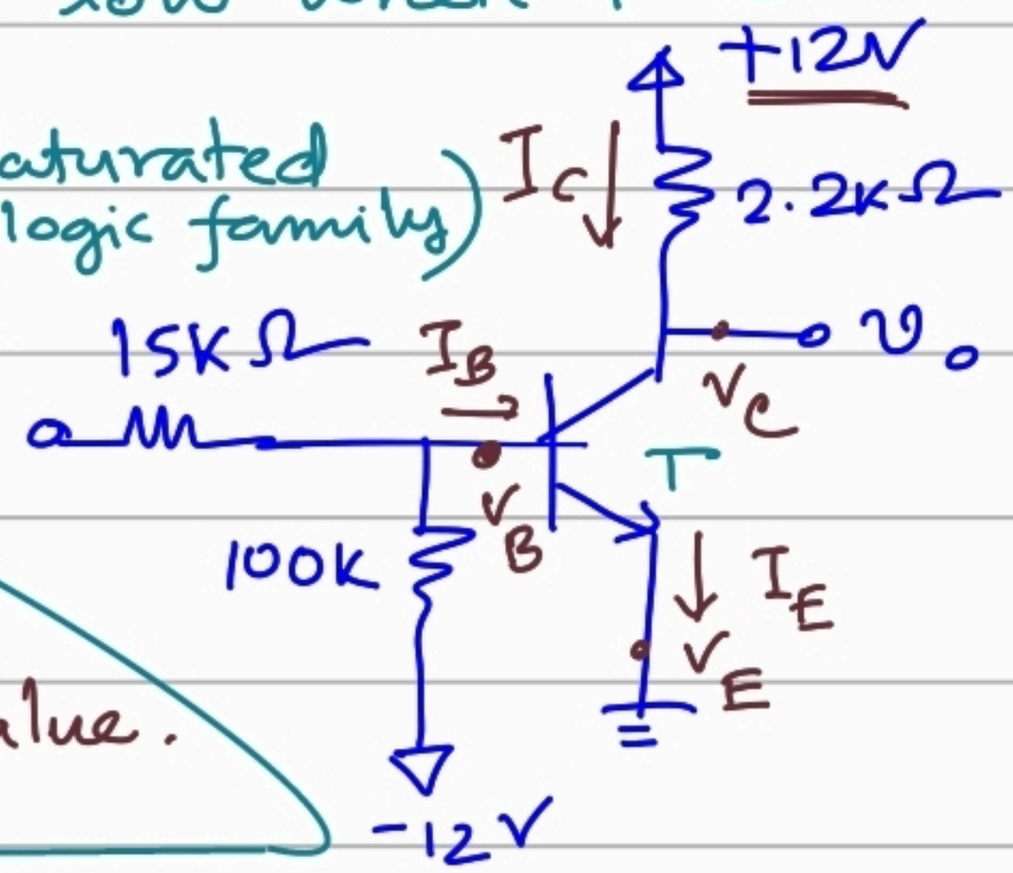
Why do we use minimum?

→ To ensure safety margins for both high and low voltages.

V_{OH} / V_{IH} → minimum voltage level at an output / input in the logical "1" state under defined load condition.

V_{OL} → maximum " " at an ~~output~~ input in the logical "0" state under defined load condition.
V_{IL}

Example: Output voltage is low when T is in saturation. $V_{OL} = 0.2V$ (Saturated logic family)

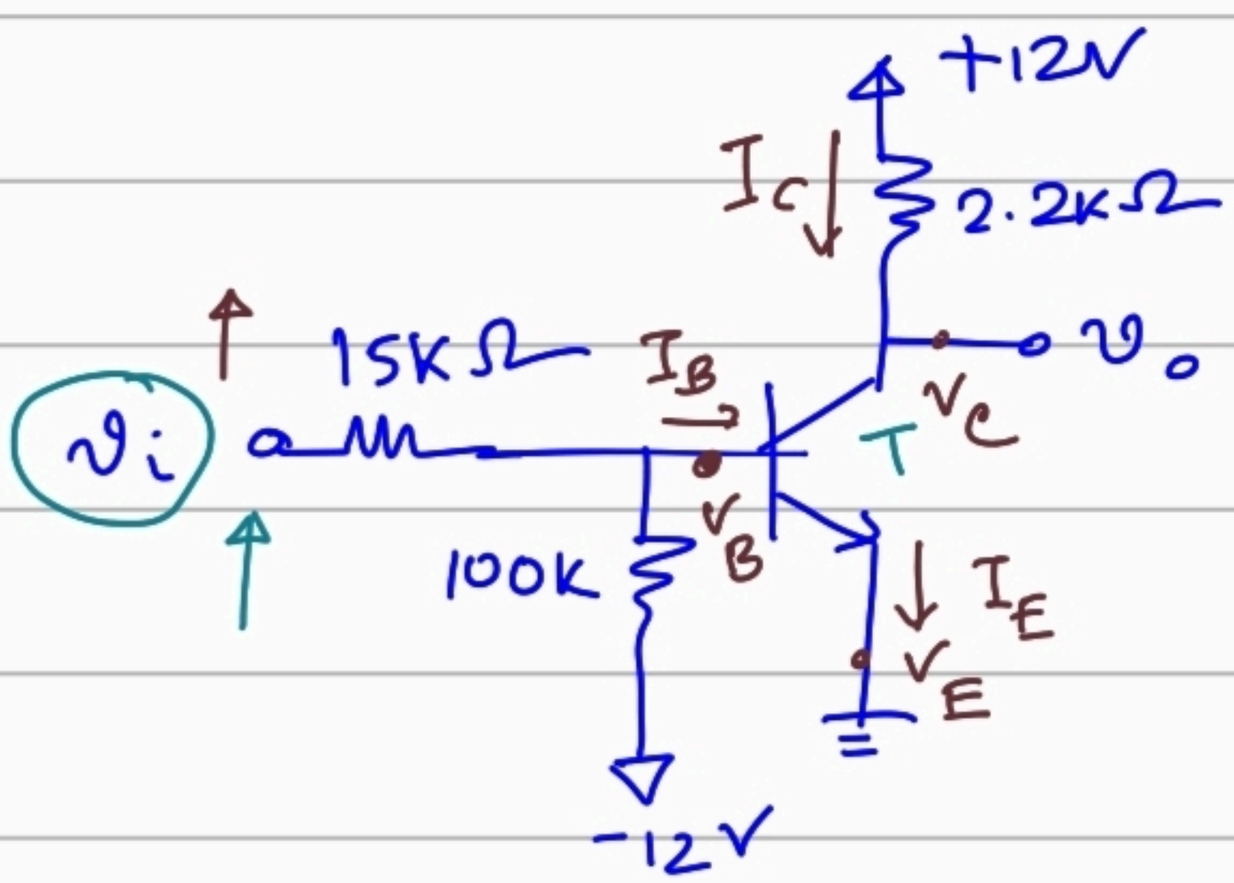


* V_{OH} = ? (This will be given)

The output high voltage can be allowed to decrease 0.5V from its maximum value.

* $V_{OH} = +12 - 0.5V = 11.5V$

* V_{IL} calculation:

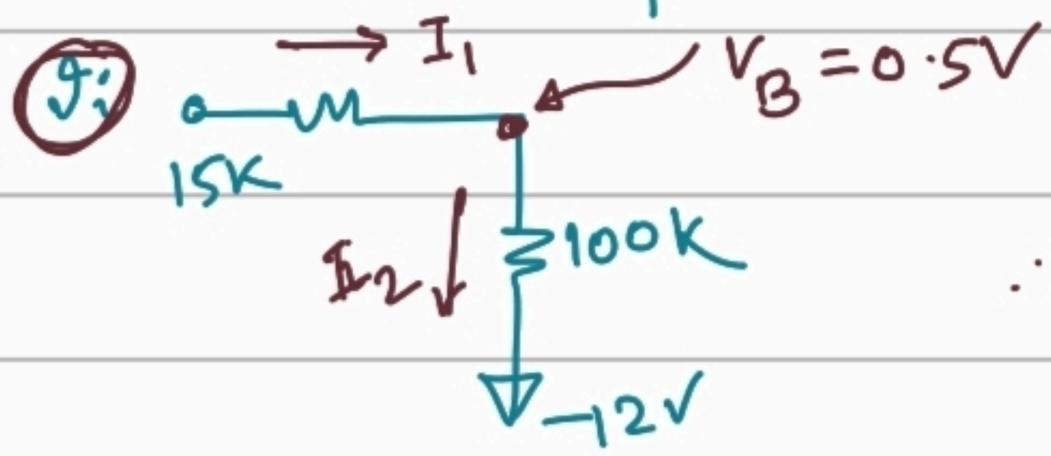


* When input voltage is low, transistor operates in cutoff mode.
* For RTL circuit, V_{IL} should be equal to the maximum voltage that takes the transistor on the verge of turn off to turn on condition.

* The transistor will turn on if $V_{BE} \geq 0.5V$.
* We need find the input voltage so that $V_{BE} = 0.5V$ but we assume transistor is in cutoff.

* T → cutoff, $I_B = 0$ mA

$$I_2 = \frac{0.5-(-12)}{100k} = 0.125\,mA$$



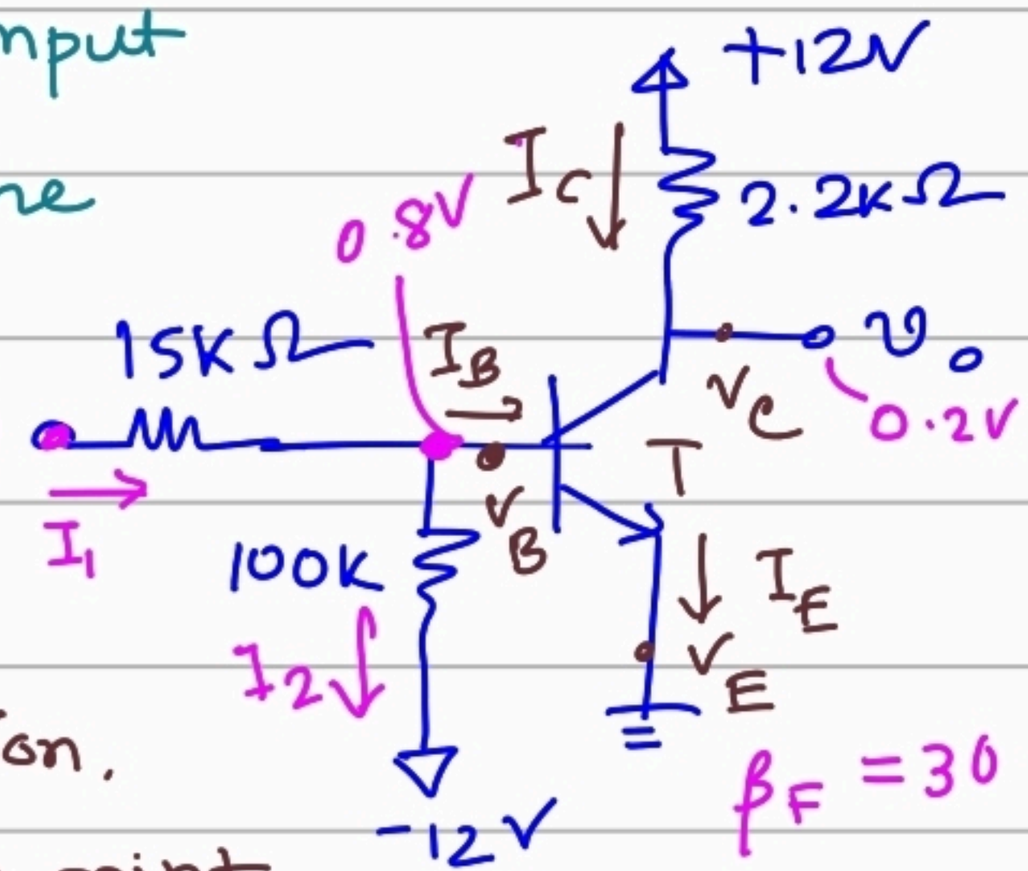
$I_1 = I_2$, $I_1 = \frac{v_i - 0.5}{15K} = 0.125\,mA$

$\therefore v_i = 0.5 + 15 \times 0.125 = 2.375\,V$

$$\boxed{V_{IL} = 2.375\,V}$$

V_{IH} calculation: When input voltage is high, transistor T operates in saturation mode. $v_{CE} = 0.2V = v_o$.

* The minimum voltage at the input terminal which will change the operating mode of transistor T to saturation to forward active mode should be V_{IH}.



* We will assume T is saturation, but $\beta_{forced} \approx \beta_F$. [Transition point between sat. and F.A.]

* T → saturation. $I_C = \frac{12-0.2}{2.2K} = 5.3636\,mA$

$\beta_{forced} = \frac{I_C}{I_B} = 30 \Rightarrow I_B = \frac{I_C}{\beta} = 0.1788\,mA$.

$I_2 = \frac{0.8-(-12)}{100K} = 0.128\,mA$. $I_1 = I_2 + I_B = 0.3068\,mA$

$\frac{v_i - 0.8}{15K} = 0.3068\,mA \Rightarrow v_i = 0.8 + 15 \times 0.3068$
$= 5.4018V$

$$\boxed{V_{IH} = 5.4018V}$$

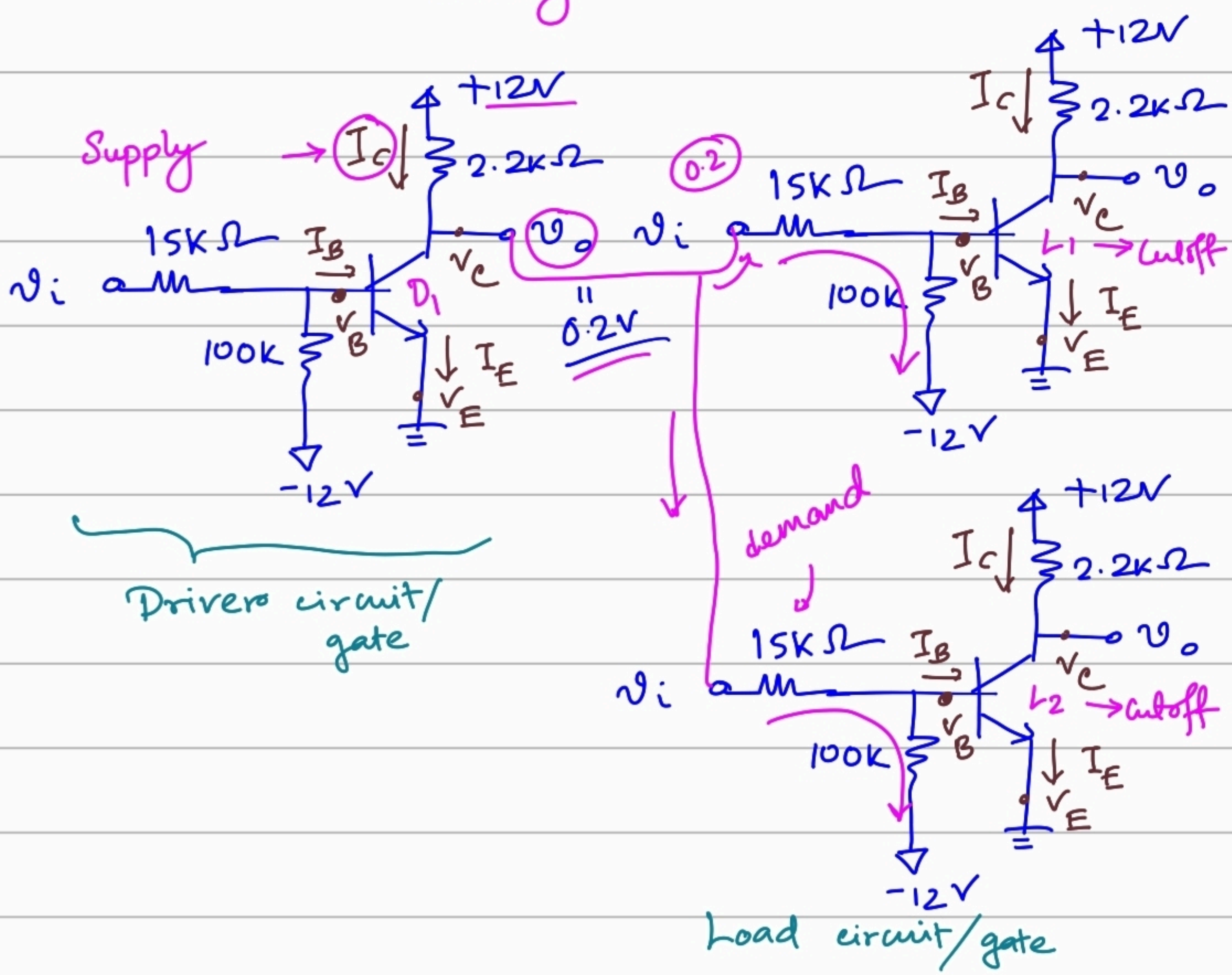
High state noise margin: $V_{NH} = V_{OH} - V_{IH}$
$= 6.0982V$

Low state noise margin: $V_{NL} = V_{IL} - V_{OL}$
$= 2.175V$

Noise margin $= \min(6.0982, 2.175)$
$= \boxed{2.175V}$

Fanout: The number of input terminals are connected to a output terminal.

Maximum fanout (fanout): The maximum number of logic inputs of the logic family that an output terminal can drive reliably is called maximum fanout.

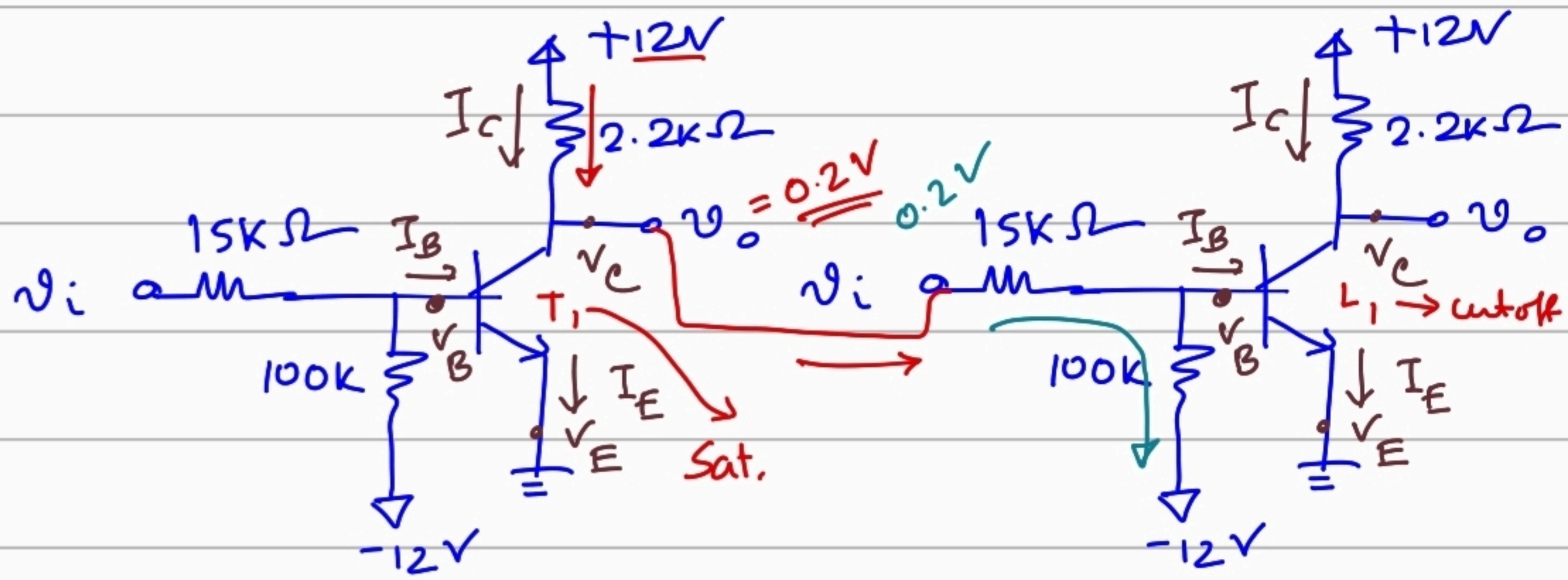


Question: Calculate the maximum fanout of the above RTL circuit. Assume $V_{OH} = 10V$.

Case ①: The output of the driver circuit is low.

* Maximum supply current :- The maximum of current can be delivered by the driver circuit without changing its operating mode.

* Individual demand load current :- The maximum amount of current needed by each individual load while driven by driver circuit.



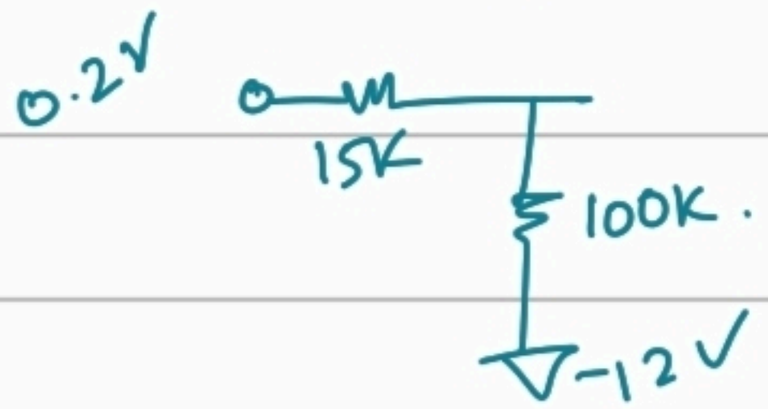
Driver circuit $T_1 \rightarrow$ Saturation. $V_o = 0.2V$

Load circuits $L_1, L_2 \rightarrow$ cutoff. $I_B = 0$.

* Maximum supply current. $\frac{12-0.2}{2.2K} = 5.3636\ mA$

* Individual demand load current, $\frac{0.2-(-12)}{(15+100)K}$

$= 0.106\ mA$



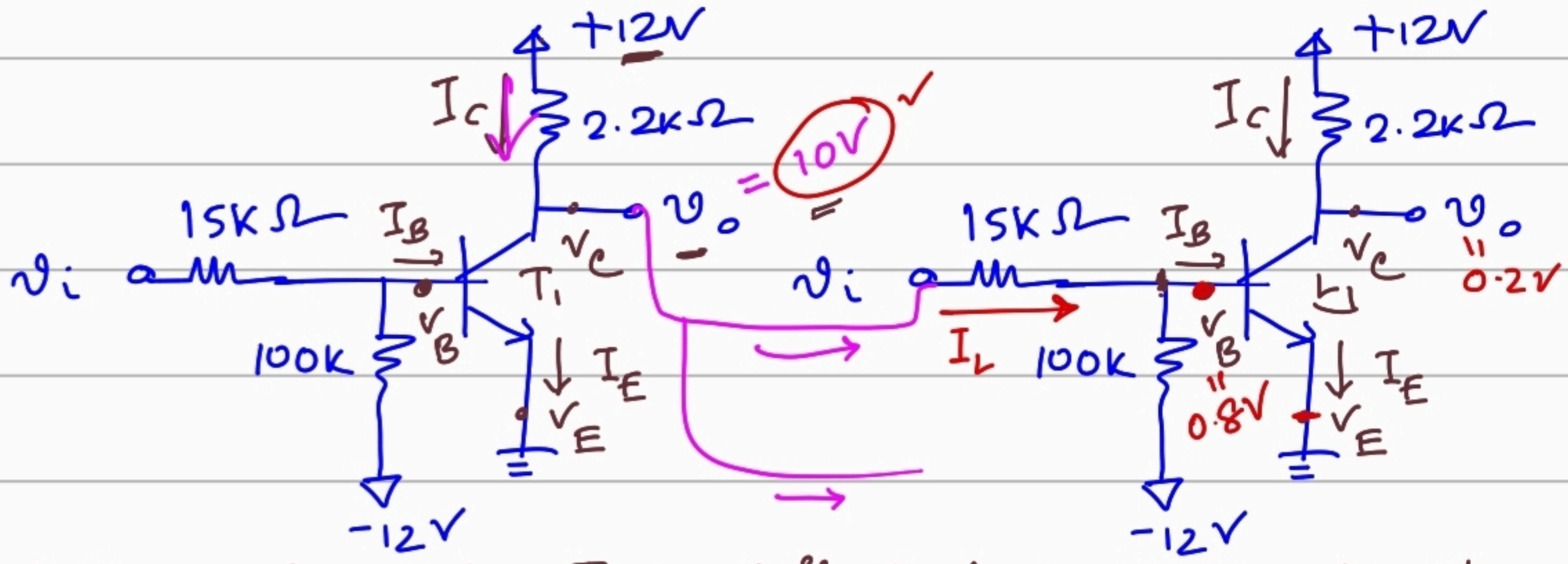
maximum fanout for this case.

$$= \left\lfloor \frac{5.3636}{0.106} \right\rfloor = \lfloor 50.6 \rfloor = 50$$

* If we connect 51 load circuits, then demand exceeds supply. Thus driver circuit will malfunction.

Case ② : The output voltage of the driver circuit is High.

* If we connect load circuits when output of driver is high, the output voltage of driver starts to drop. $\boxed{V_{OH} = 10V}$



* Driver transistor, $T_1 \rightarrow$ cutoff, load circuit's transistors L_1, L_2 Sat.
* Maximum supply current $= \frac{12-10}{2.2K\Omega} = 0.909mA$

* Individual load current, $I_L = \frac{10-0.8}{15K} = 0.6133\ mA$

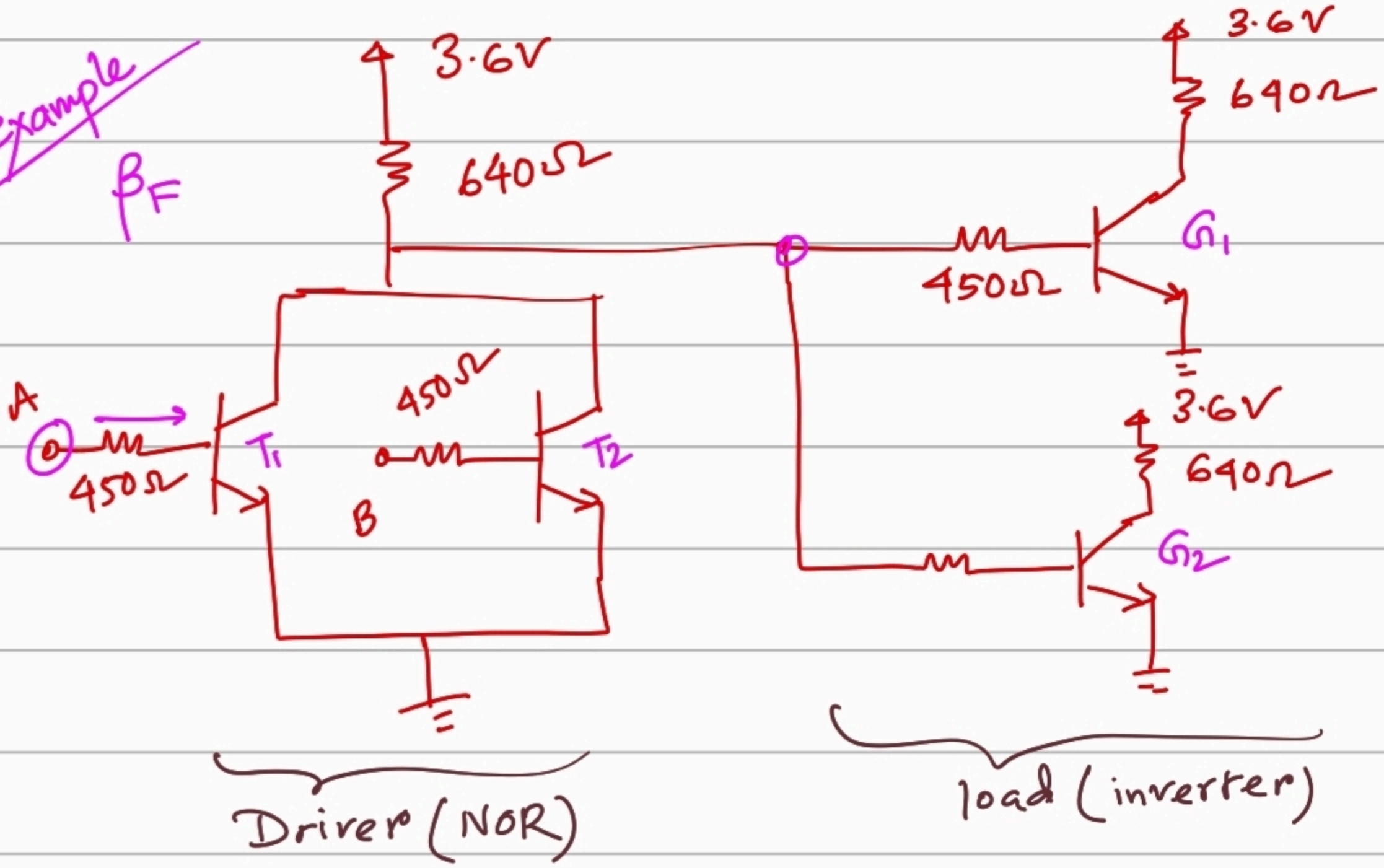
* Maximum fanout for this case. $= \left\lfloor \frac{0.909}{0.6133} \right\rfloor = \lfloor 1.48 \rfloor = 1$

⊞ Overall maximum fanout must be calculated by considering worst case scenario. To prevent malfunction of driver circuit, we need to take the minimum of the two cases.

⊞ Maximum fanout, $= \min(50, 1) = 1$

Example

β_F



* There would be resistor connected to input terminal and the resistor is connected to the transistor. (RTL circuit)

* If the input high voltage (RTL), you can assume switching transistor is operating in saturation, or if the input voltage is low, transistor is operating in cutoff mode.

* Question: If the number of fanout is 5. Find the minimum value of β_F, so that these circuits operate as NOR gate. Assume all transistors have same value of β.

Lecture 5: Introduction to DTL.

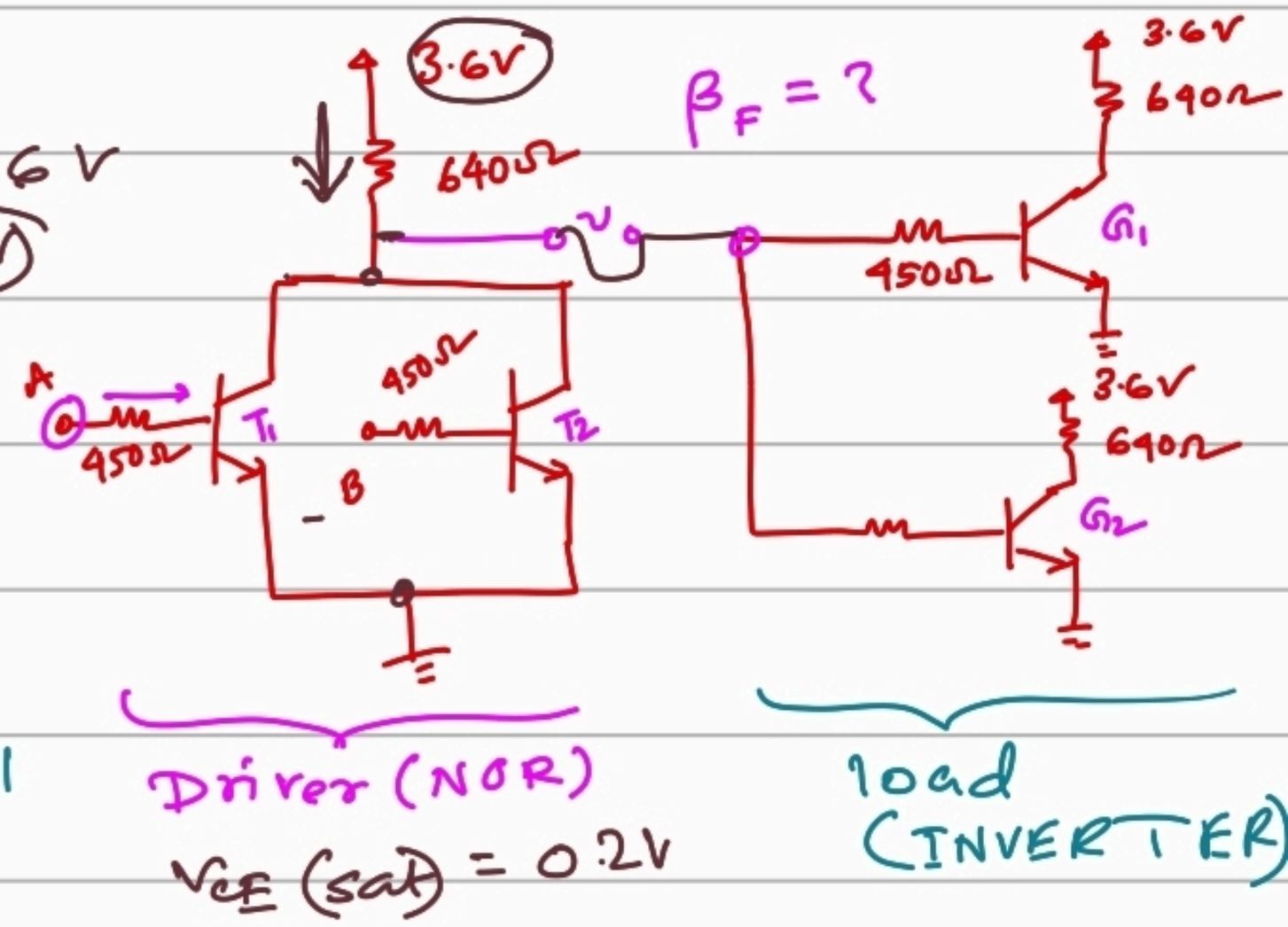
Example RTL:

Voltage logic High = 3.6 V
Low = 0V

A	B	T_1	T_2	v_o
3.6	3.6	S	S	0.2
3.6	0	S	C	0.2
0	3.6	C	S	0.2
0	0	C	C	3.6

→ LOW

→ HIGH

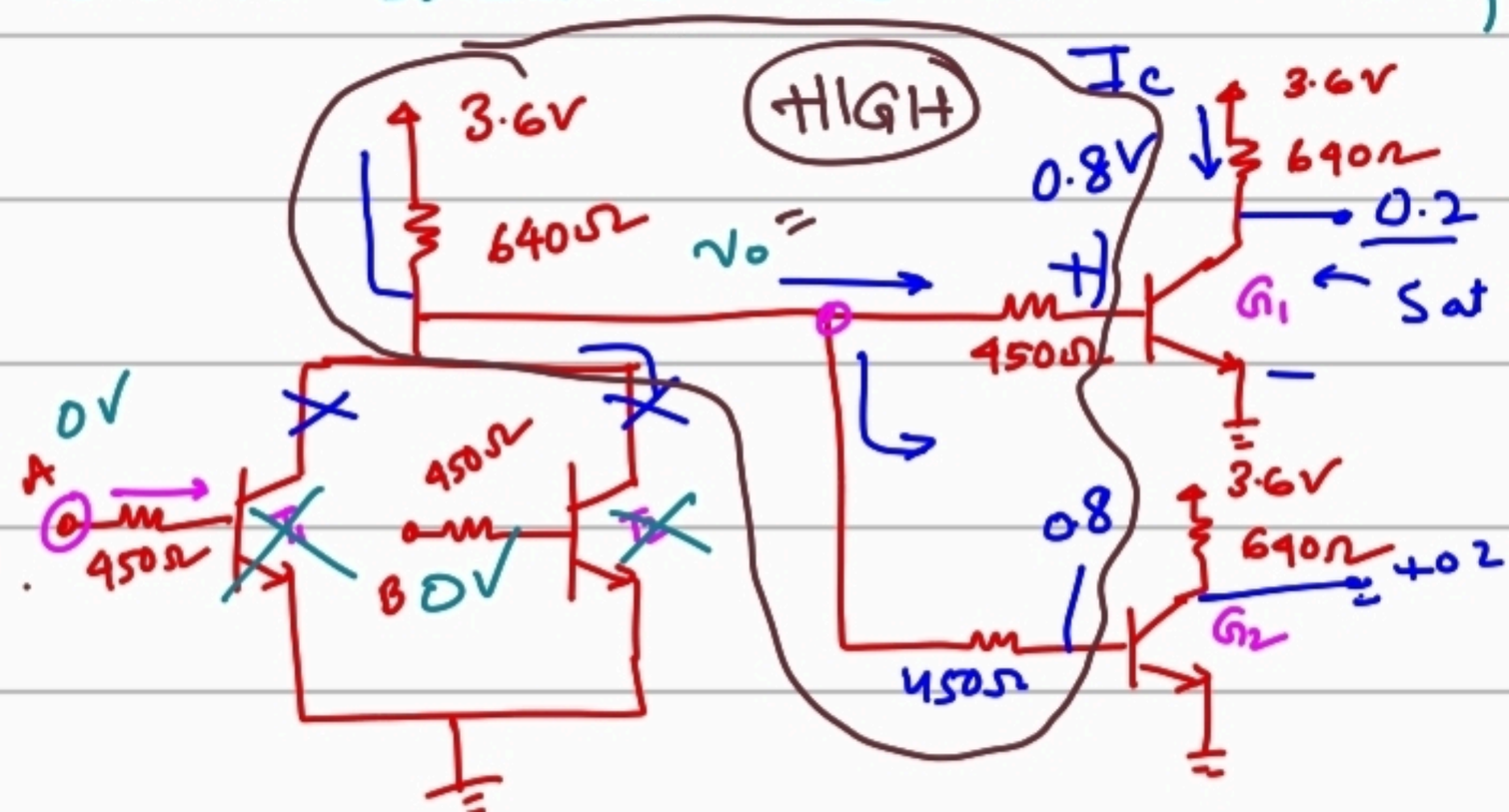


NOR → DRIVER circuit without any load connected to it.

* If we add load circuits, when driver output voltage low then it will not change because it is determined by $v_{CE}(sat) = 0.2$ V.

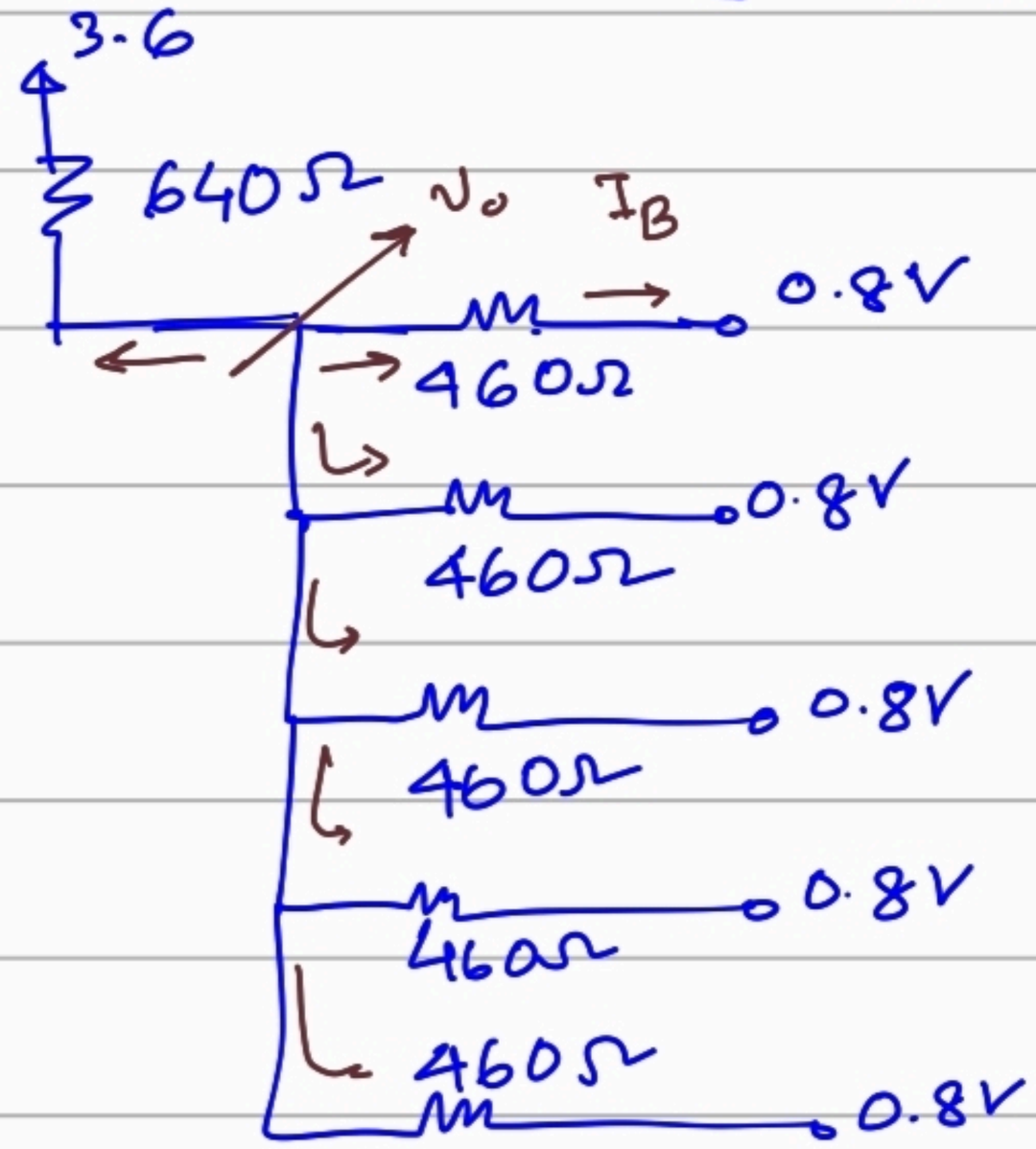
* On the other hand, if the output voltage of driver were high, the load circuits will draw current from the driver circuit, that will reduce the voltage.

- FANOUT = 5, in order to maintain proper circuit operation what should be the value of β_F?
- $T_1, T_2 \rightarrow$ cutoff
- $G_1, G_2, \ldots, G_5$ will operate in saturation.
- β_{forced} (load) = ?



Collector current in load circuit, $= \frac{3.6-0.2}{0.64K}$

$I_c = 5.3125\,mA$



$$\frac{v_o-3.6}{0.640K} + 5 \times \frac{v_o-0.8}{0.460K} = 0$$

$$\Rightarrow \boxed{v_o = 1.1452V}$$

base current for individual load

$$I_B = \frac{1.1452-0.8}{0.460K}$$

$$\boxed{I_B = 0.767\,mA}$$

$$\beta_{forced} = \frac{I_c}{I_B}\,(\text{load})$$

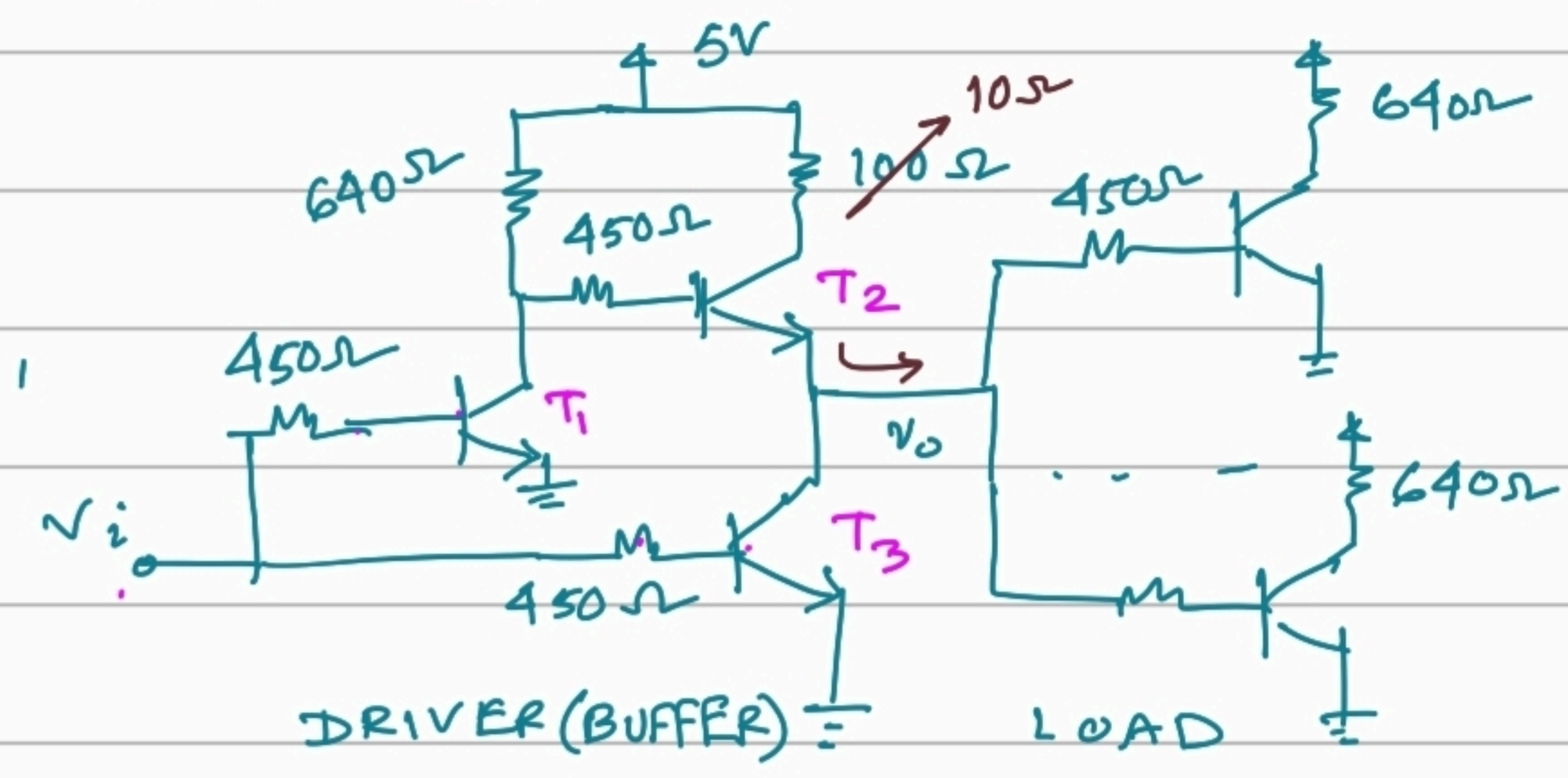
$$= \frac{5.3125}{0.767} = 6.9263$$

* Load circuits will remain in saturation if their $\beta_F \geq \beta_{forced}$. Load circuits must have β_F at least equal or greater that 6.9263 to maintain accurate operation.

$$\boxed{\beta_{min} = \beta_{forced} = 6.9263}$$

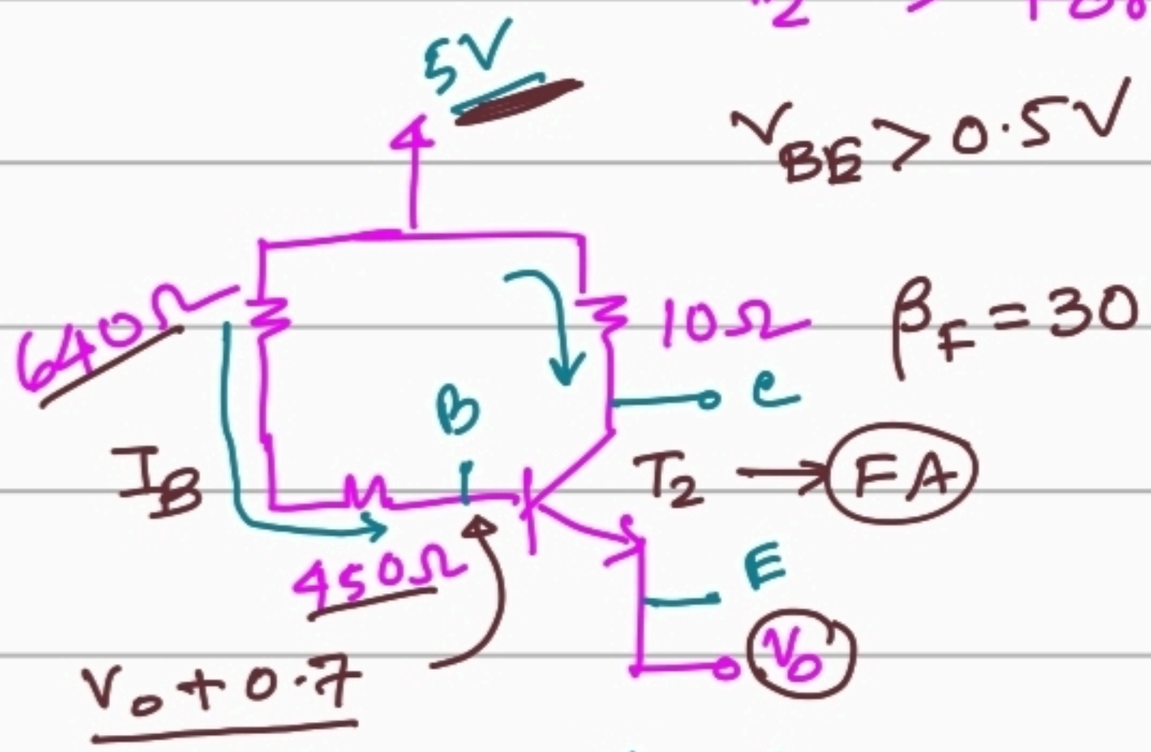
<u>Homework 2.5</u> (Quiz/Mid)

Remark: Buffer circuit → FANOUT for RTL increases



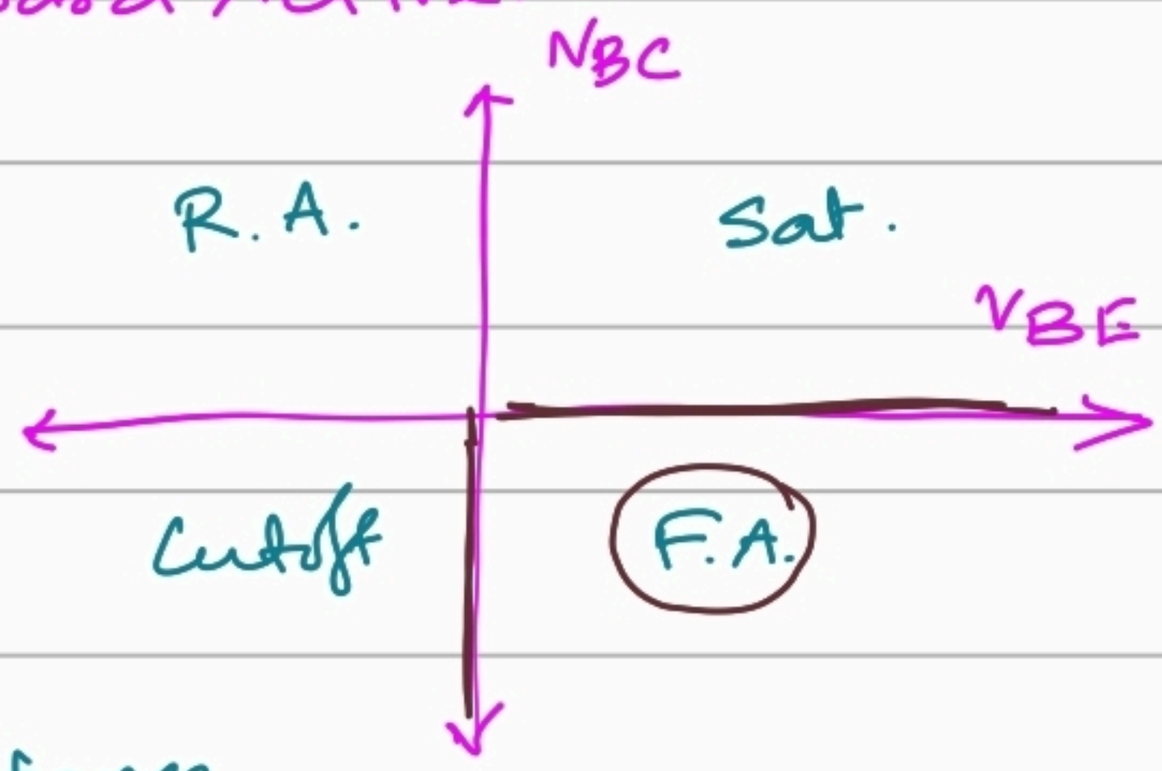
Hints : Case ①. $V_i = 0V$. $T_1, T_3 \rightarrow$ cutoff

$T_2 \rightarrow$ Forward Active.



$V_{BE} > 0.5V$

$\beta_F = 30$



As the collector resistance is very small then the collector voltage will be very close to 5V.

However, the base voltage will be significantly lower because of higher resistances.

$$V_C > V_B \Rightarrow V_B - V_C < 0 \Rightarrow V_{BC} < 0$$

$V_{BE} = 0.7V$

T_2 might be in forward active.

$I_B = \beta_F I_C$, $I_E = I_B + I_C = (\beta + 1) I_B$

$$I_B = \frac{5 - (V_o + 0.7)}{(0.64 + 0.45)k}$$, for this case I_E is the supply current.

Do it yourself.

Case ② $\boxed{V_i = 5V}$

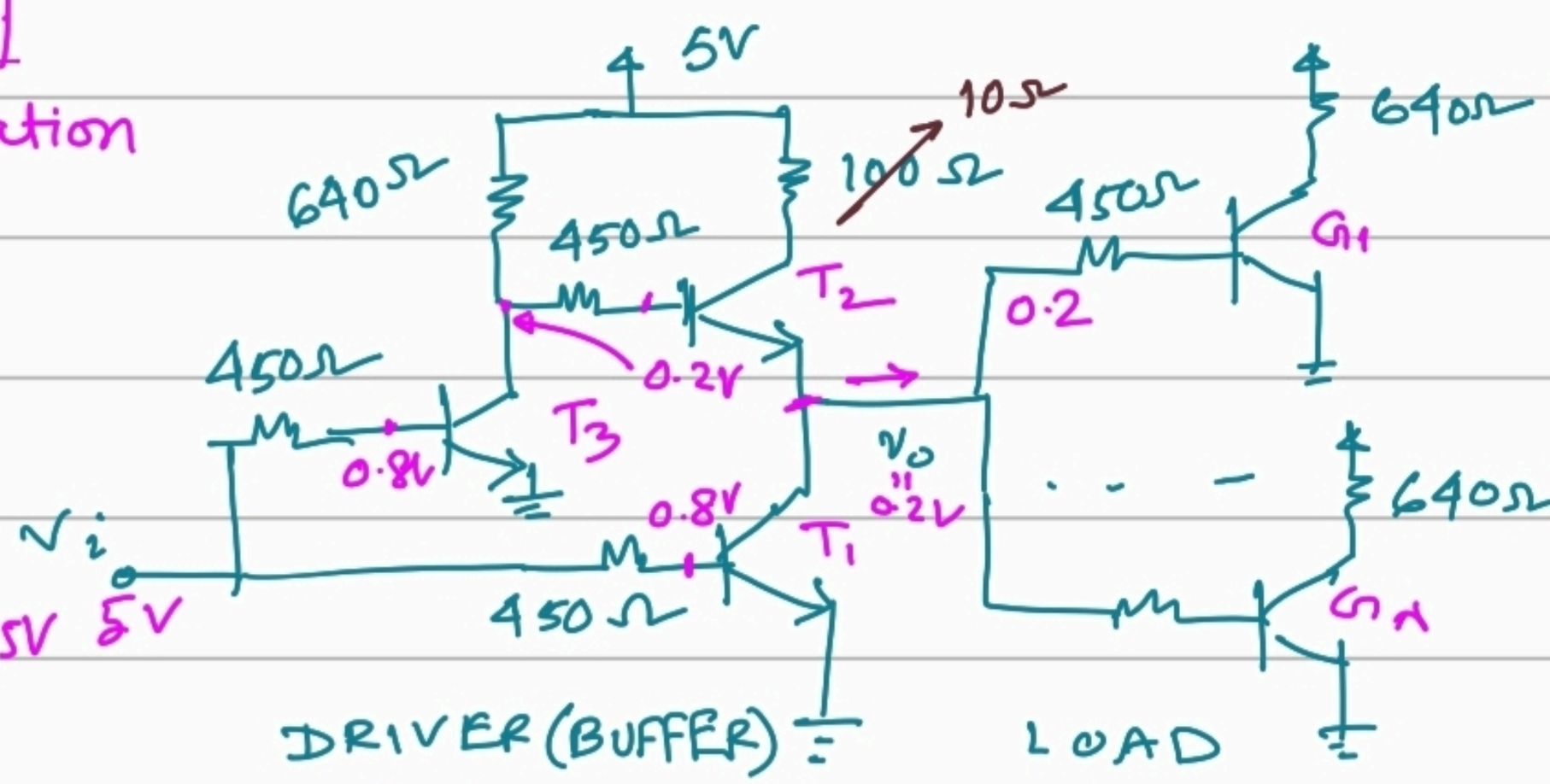
$T_1, T_3 \rightarrow$ saturation

$V_o = 0.2V$

$V_B(T_2) \approx 0.2V$

$V_E(T_2) \approx 0.2V$

$V_{BE}(T_2) = 0V < 0.5V$



$\Rightarrow T_2 \rightarrow$ cutoff

supply current = 0, | $G_1, G_2 \ldots G_N$ cutoff | demand current = 0

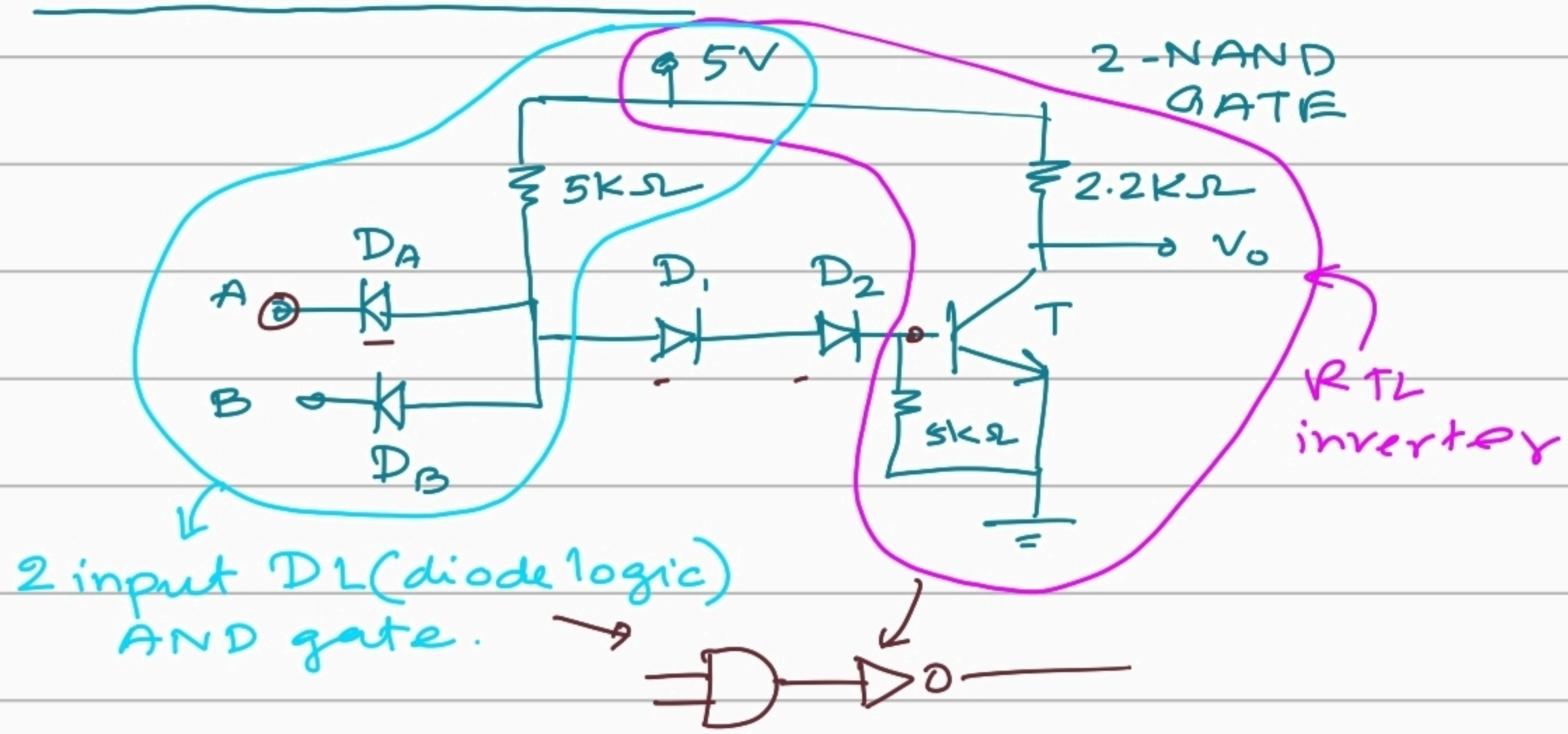
maximum fanout $= \frac{0}{0}$ = any answer is valid.

DTL (Diode Transistor Logic)

* Bipolar → Saturated
(Switching transistor will operate in saturation and cutoff mode).

* Input terminals connects through diodes to the switching transistor's base terminal.

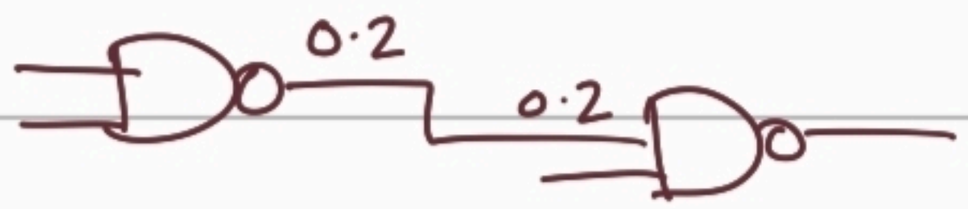
DTL NAND GATE:



Basic operation:

Calculate the currents and voltages of the following DTL gate and verify that it works like a NAND gate. Assume that input stages might be connected to the output stage of other DTL NAND gate.

$V_{BE}(sat) = 0.8V$, $V_{CE}(sat) = 0.2V$. $\beta_F = 30$.

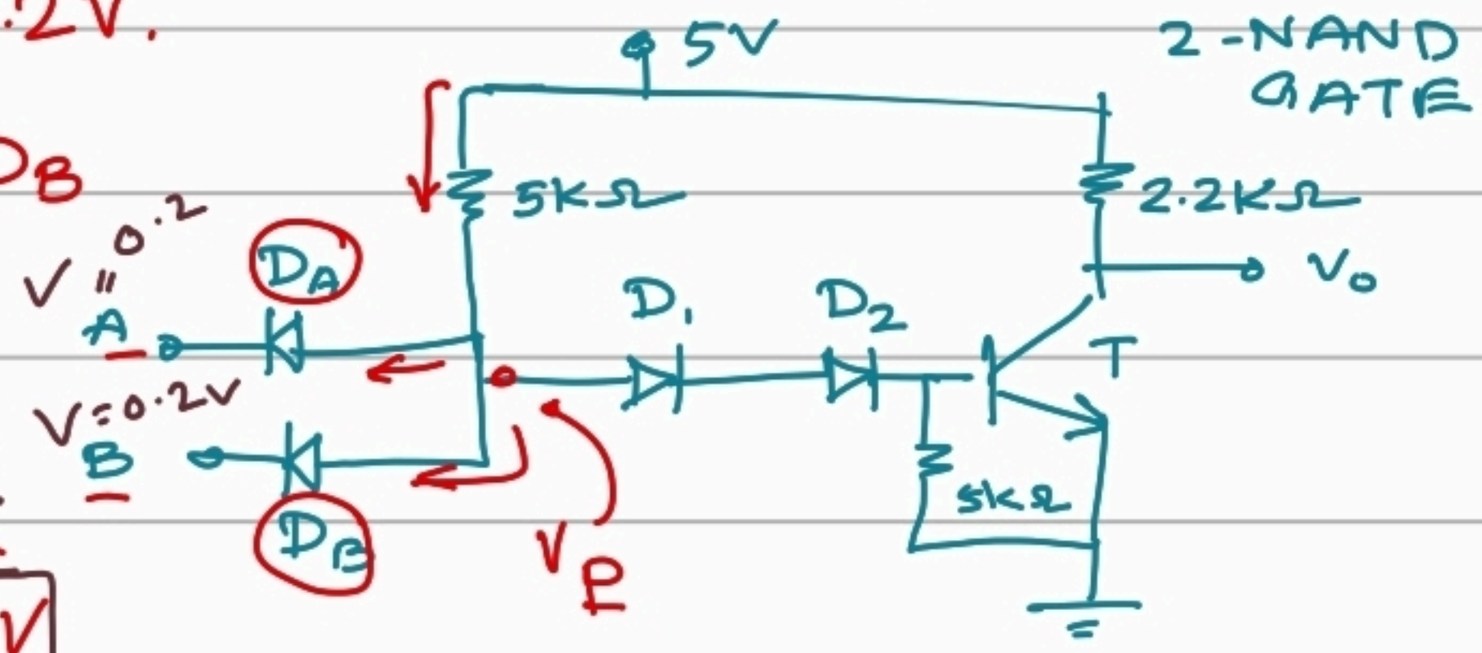


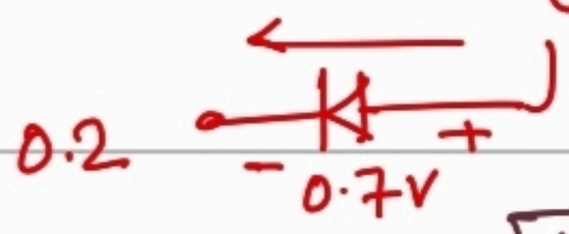
Ans:

Case ① Both inputs are low.

Because inputs are connected to some other output stage, the output voltage = input voltage = 0.2V. $V_A = V_B = 0.2V$.

Assume, D_A and D_B are conducting.



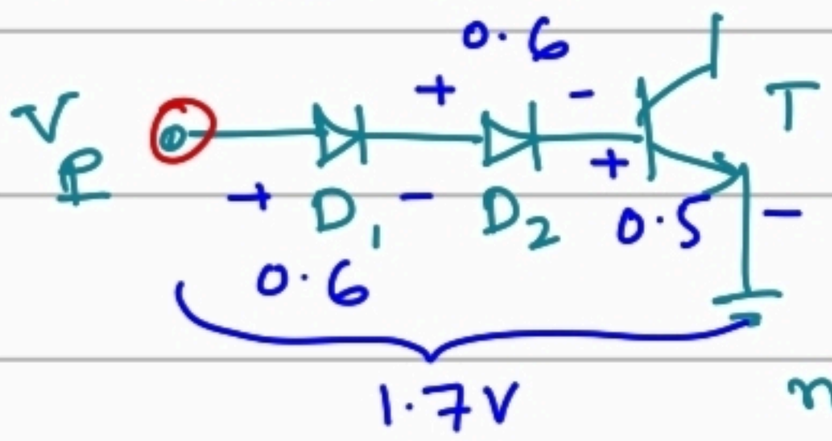


$V_p = \frac{0.7}{+0.2}$

$\boxed{V_p = 0.9V}$

Since we are assuming diodes are conducting the anode voltage V_p of D_A and D_B must be 0.7V higher than the cathode voltage. Thus $V_p = 0.9V$.

Necessary condition for transistor T to turn on:



V_{BE} (cut in voltage) = 0.5V

V_γ (cut in voltage of diode) = 0.6 V

In order for T to turn on we need to have $V_p \geq 1.7V$.

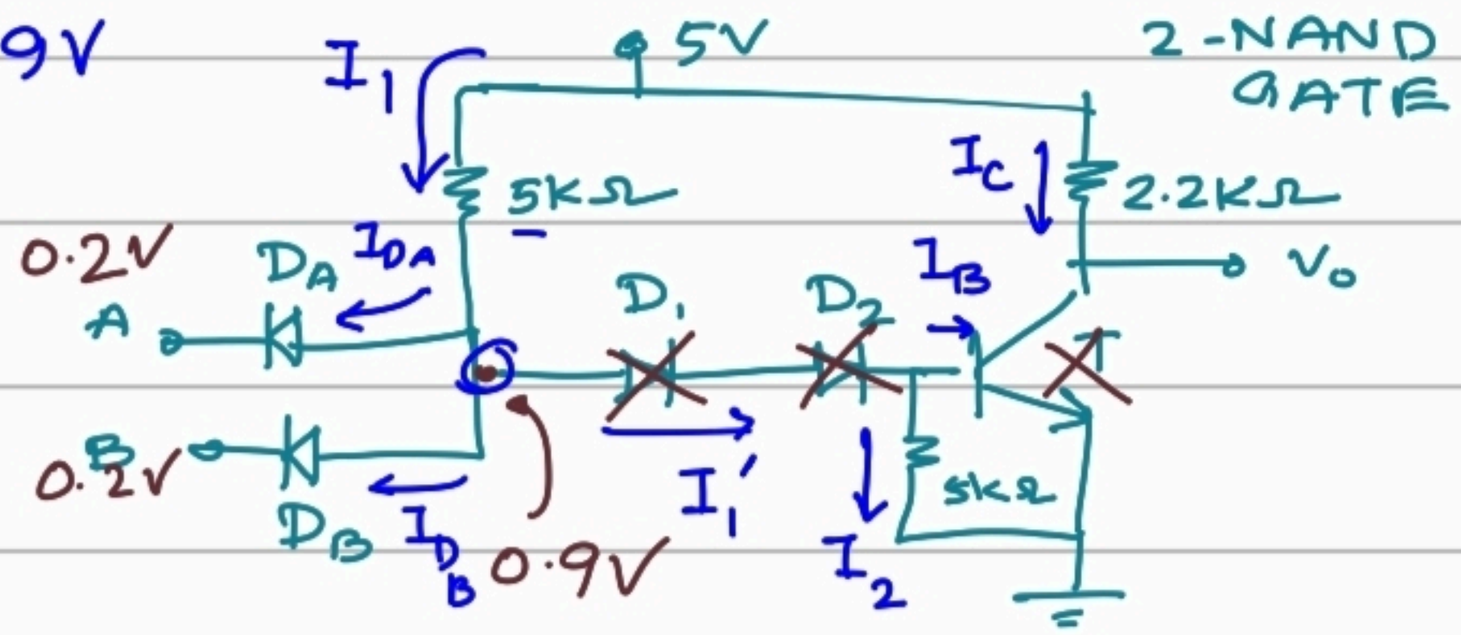
According to our assumption, V_p will not turn on D_1, D_2 and T and current will flow as we expected.

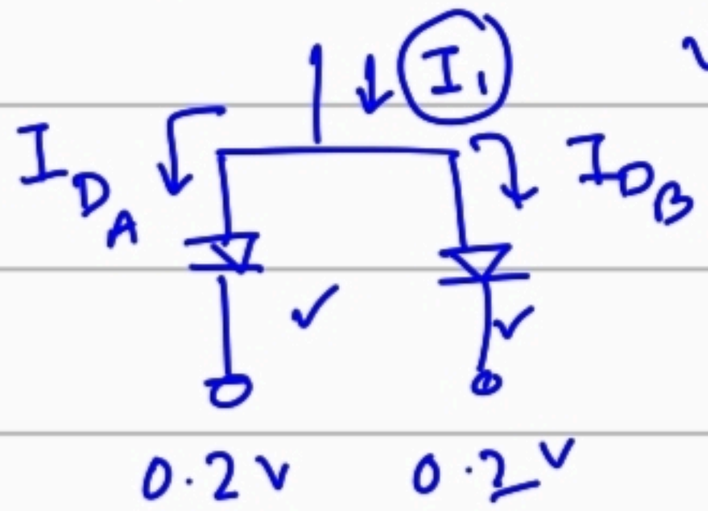
$V_A = V_B = 0.2V$, $V_p = 0.9V$

$I_1 = \frac{(5 - 0.9)}{5k} = 0.82mA$

$I_c = I_B = I_2 = I_1' = 0$

$V_o = 5V$





$I_{DA} = I_{DB}$ because both braches are identical.

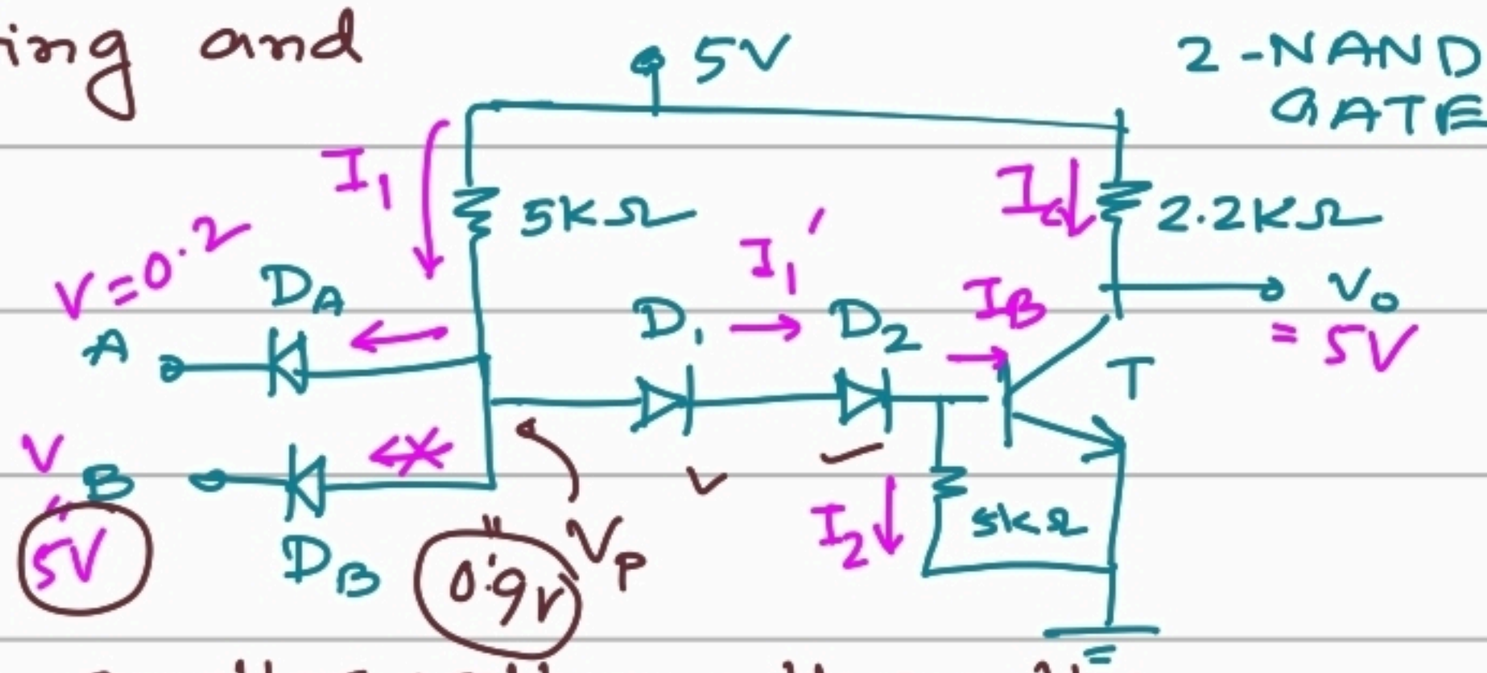
$I_{DA} = I_1/2 = 0.41$ mA.

Case ② $V_A = 0.2V$, $V_B = 5V$ | ($V_A = 5V$, $V_B = 0.2V$) Similar

Assume. D_A is conducting and D_B is off.

Therefore, $V_p = 0.9V$.

So D_1, D_2, T must be turned off.



The anode of D_B has smaller voltage than the cathode. So our assumption is right.

$I_C = I_B = I_1' = I_2 = 0$, $V_o = 5V$. $I_1 = \frac{5-0.9}{5K\Omega} = 0.82$ mA

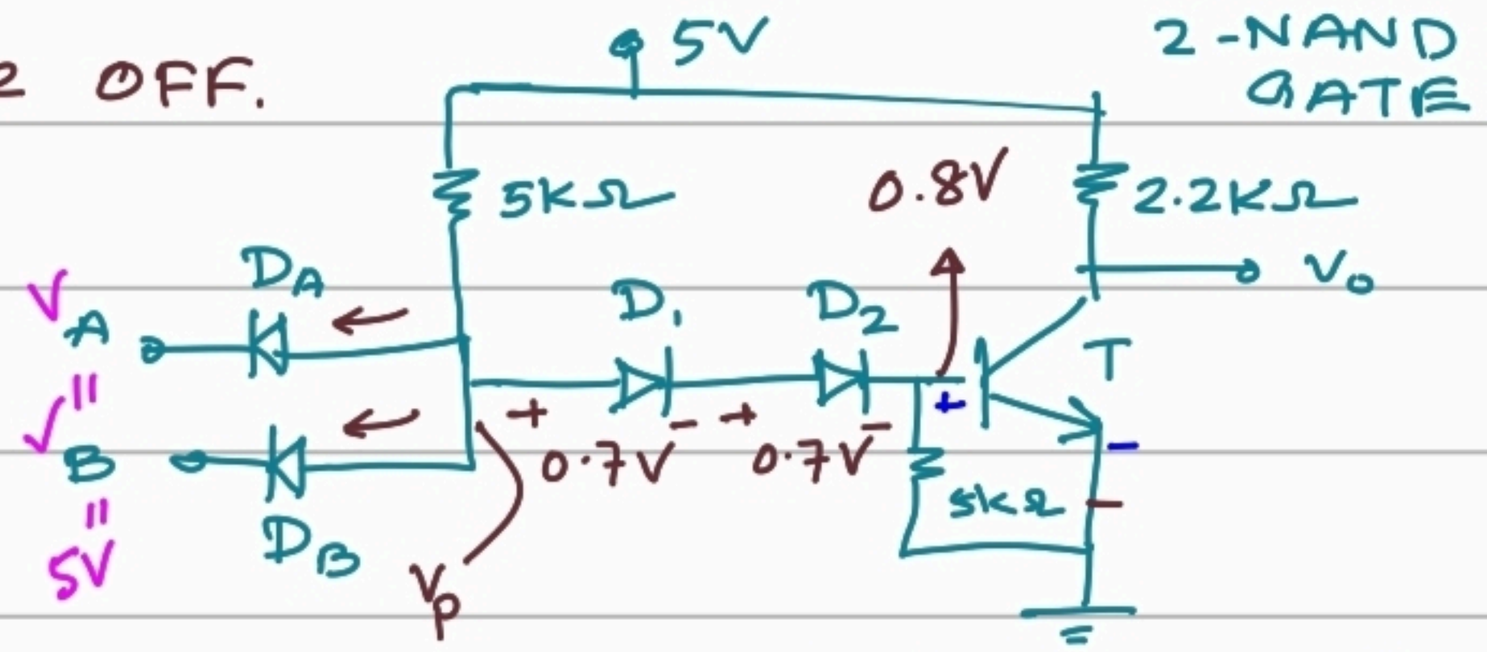
$$\boxed{I_{D_A} = I_1 = 0.82mA, \quad I_{D_B} = 0\,mA.}$$

Case ③ $V_A = V_B = 5V$.

Assume, D_A and D_B are OFF.

$I_{D_A} = I_{D_B} = 0$ mA.

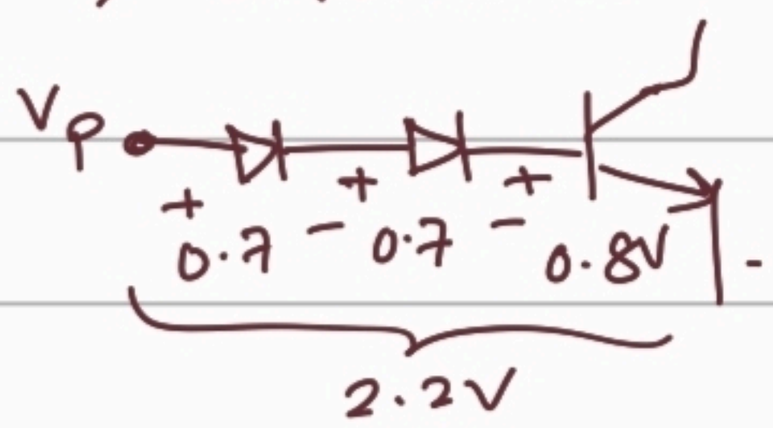
Therefore current must flow through D_1, D_2 and T.



Because it is a DTL circuit, the switching transistor must operate in saturation when it is turned on.

$V_{BE}(sat) = 0.8V$, $V_{CE}(sat) = 0.2V$

⇒ Conduction voltage of D_1 and D_2 diodes are 0.7V.



According to our assumption V_p must be 2.2V.

The cathode voltages of D_A and D_B is higher than the anode voltage $V_p = 2.2V$

This justifies our assumption.

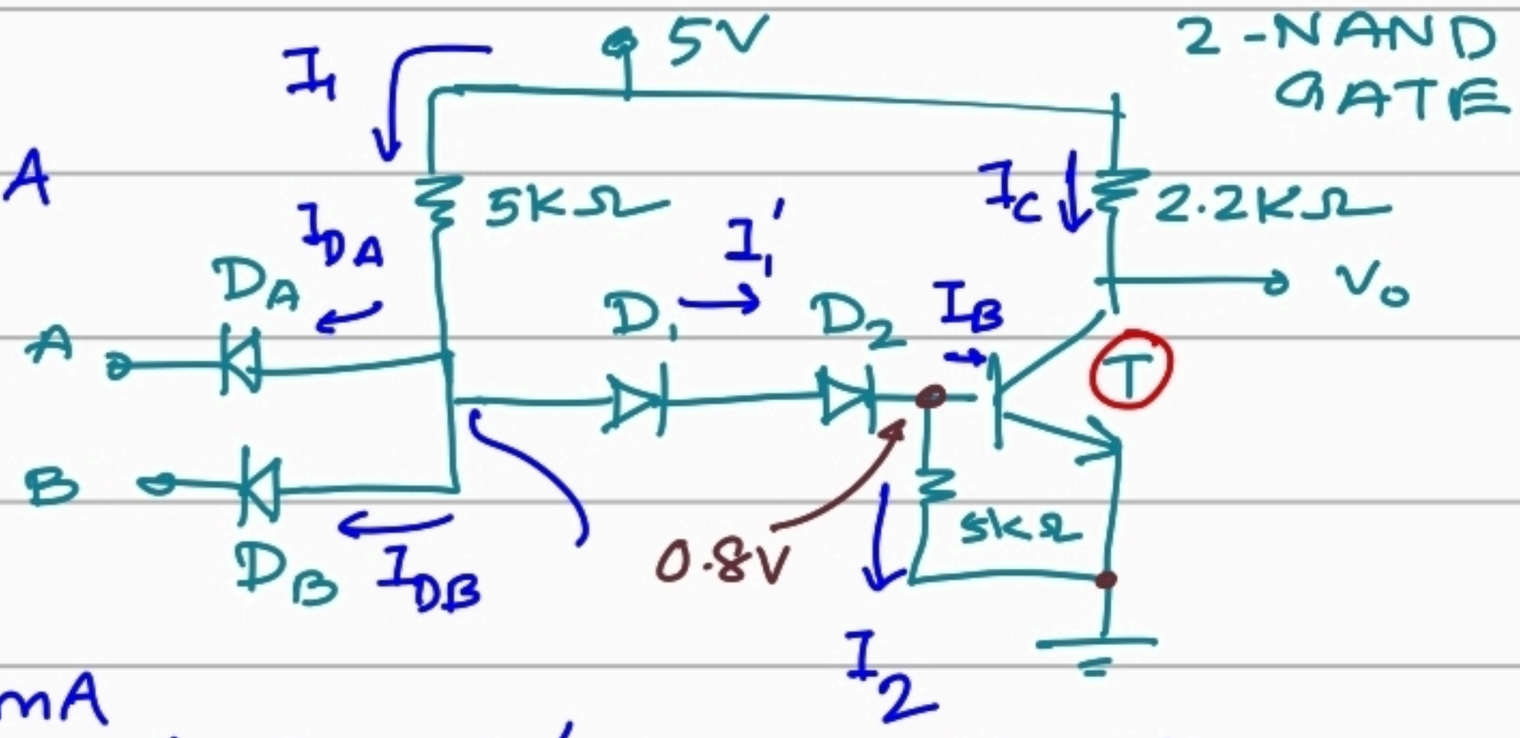
Current-voltage Calculation:

$V_P = 2.2V$

$I_1 = \left(\frac{5-2.2}{5k}\right) = 0.56mA$

$I_{D_A} = I_{D_B} = 0\ mA$

$I_1' = I_1 = 0.56\ mA$



$I_2 = \frac{0.8-0}{5K} = 0.16mA$, $I_B = I_1' - I_2 = 0.56 - 0.16$
$= 0.4\ mA$

$I_c = \frac{5-0.2}{2.2K} = 2.182\ mA$

Chart:

V_A	V_B	V_o
0.2	0.2	5V
0.2	5V	5V
5V	0.2	5V
5	5	0.2

From analyzing the cases we can clearly conclude that this circuit is a NAND gate.

β_{min} for this circuit:

$$\beta_{forced} = \frac{I_c}{I_B} = \frac{2.182}{0.4} = 5.45$$

We need to choose $\beta_F \geq 5.45$ for transistor T in order to prevent it from malfunctioning.

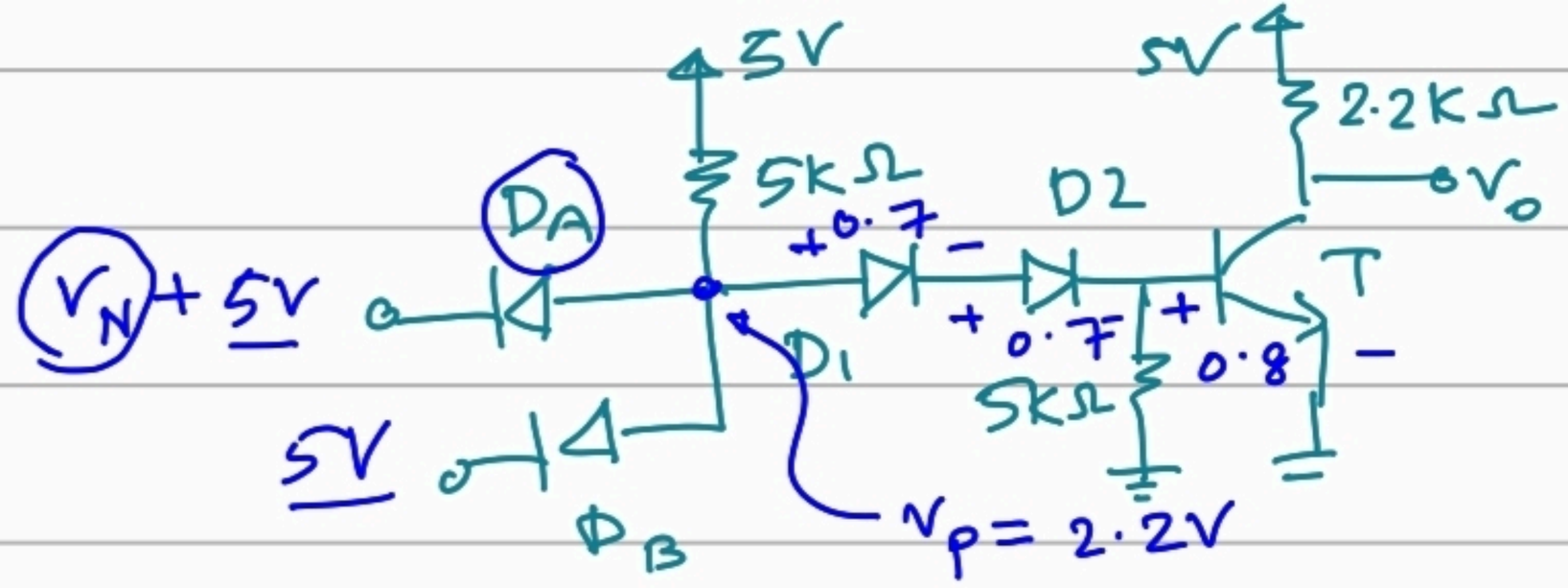
$$\boxed{\beta_{min} = 5.45}$$

Lecture 6: DTL NOISE MARGIN, FANOUT, Modified DTL, HTL

Noise Margin: Different calculation from RTL circuit.

V_{NH} (high noise margin):

Q: If all inputs are high, then what is the magnitude of noise voltage which will cause the gate to malfunction?



Case ③

T → sat

D_1, D_2 → ON

Correct operating condition: Case ③. D_A, D_B off, D_1, D_2, T will be on.

malfunction will happen if D_A turns on because of noise, thus drains all currents from otherside due to small resistance.

In order for D_A diode to turn on anode terminal voltage V_P must be 0.6/0.5V = V_γ (diode) higher than the cathode voltage V_A.

$$V_P - V_A = 0.6V \Rightarrow V_A = 2.2 - 0.6 = 1.6V$$

$$\Rightarrow 5 + V_N = 1.6 \Rightarrow V_N = 1.6 - 5 = -3.4V$$

Noise voltage can be positive or negative.

Ans: high threshold noise margin

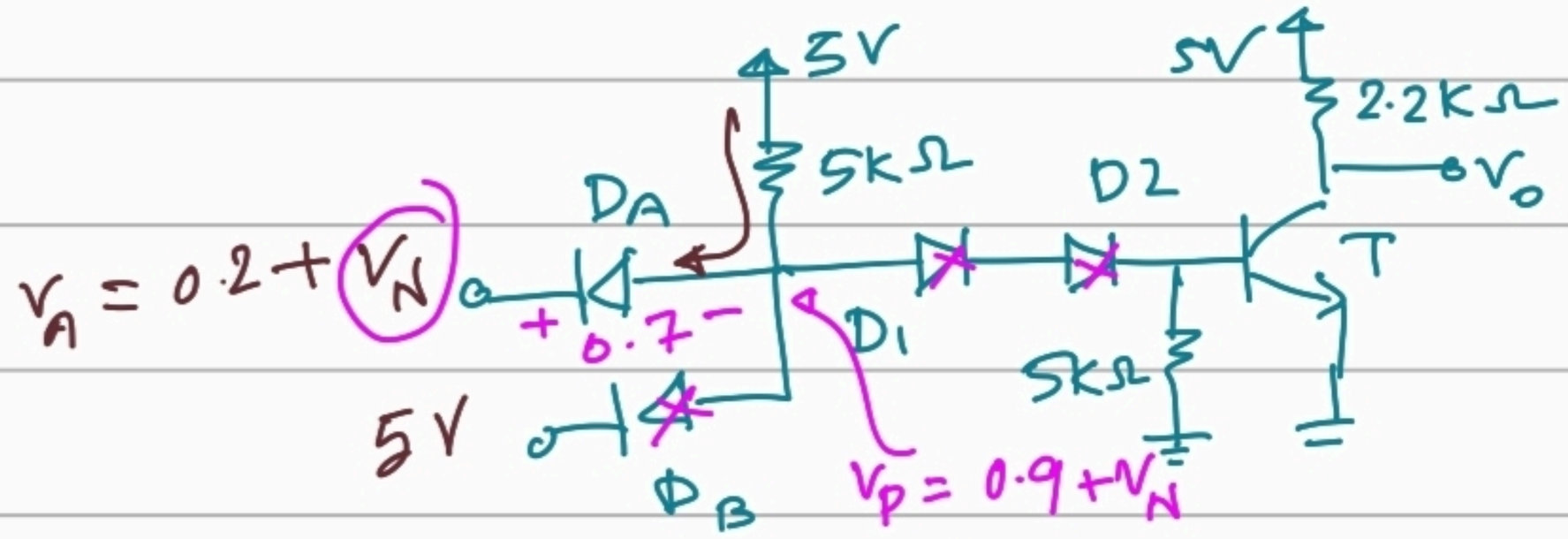
$NM_H = |V_N|$

$\boxed{NM_H = 3.4V}$

Q: If one input voltage is low and other inputs are high, then what magnitude of noise voltage at low voltage terminal will cause the gate to malfunction?

Ans: Correct operating condition: Case ② D_A on, D_B,

D_1, D_2, T → off.



Case ②
T → cutoff.
D_A → ON.

Malfunction occurs when D1, D2, T are turned on.

Since D_A diode is conducting, the voltage difference between "anode V_P" and "cathode V_A" must be 0.7V. $V_P - V_A = 0.7$

$$V_P = V_A + 0.7 = 0.9 + V_N$$

Whenever. $V_P \approx 1.7V$, D_1, D_2 and T will turn on.

This implies that, $V_P \approx 1.7 \approx 0.9 + V_N$, $\boxed{V_N = 0.8V}$

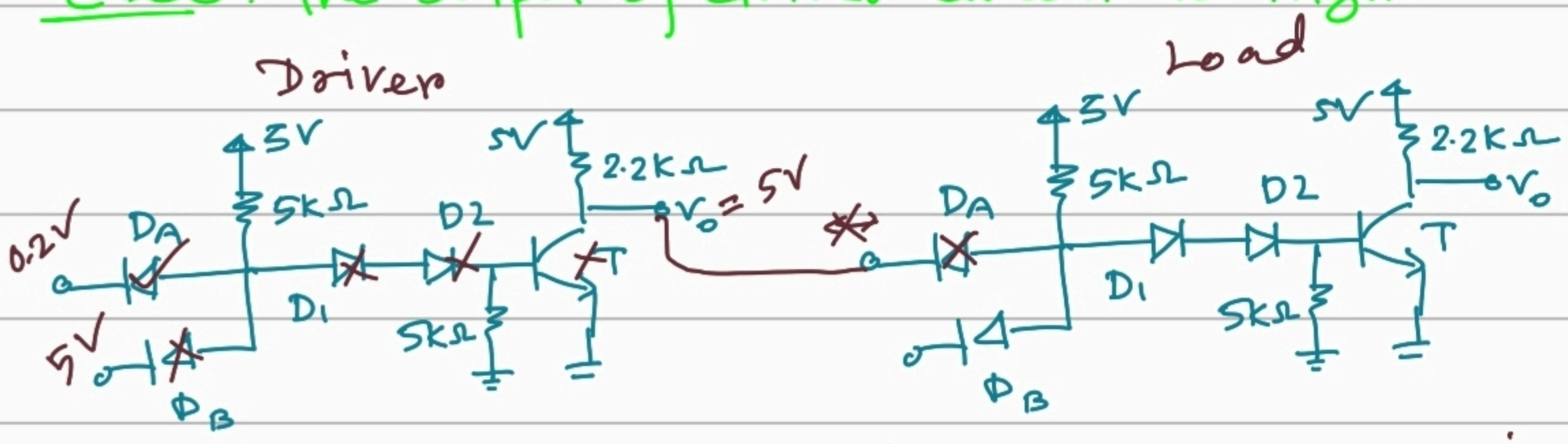
- Low threshold noise margin. $NM_L = 0.8V$.

Finally noise margin, $NM = \min(NM_H, NM_L)$
$= \min(0.8, 3.4)$

$$\boxed{NM = 0.8V}$$

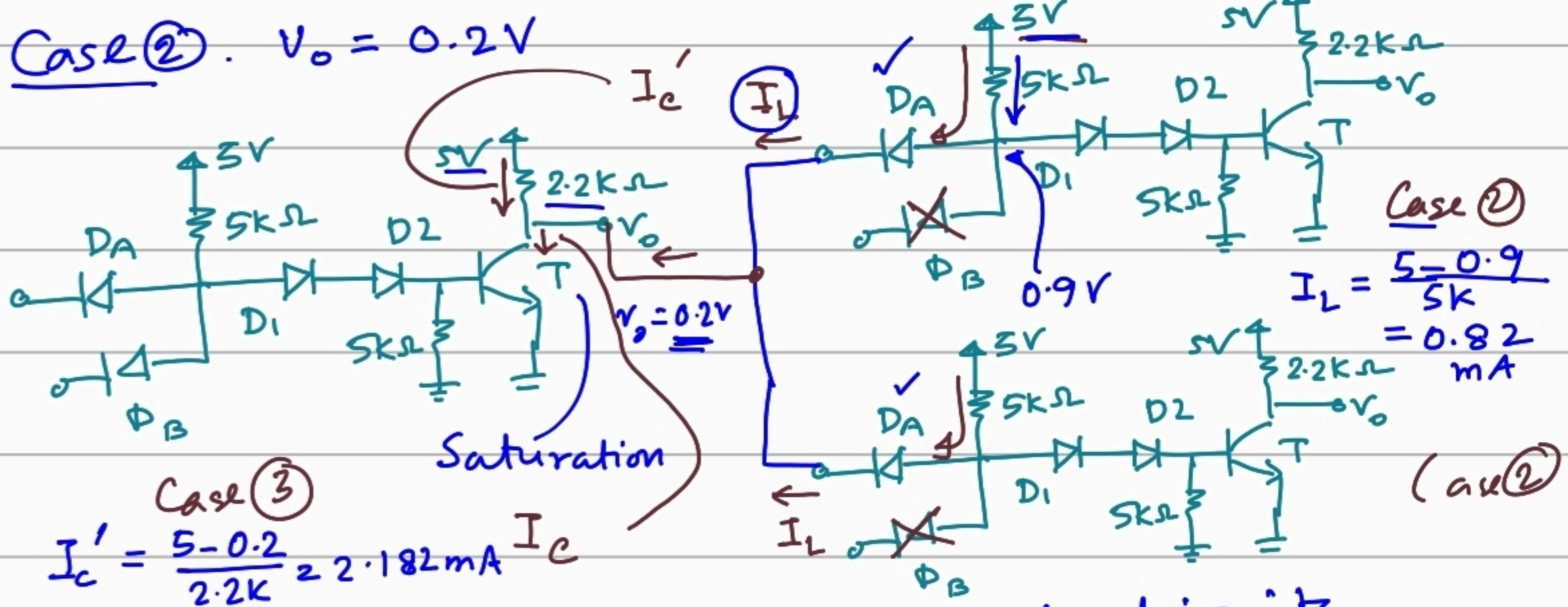
Maximum fanout Calculation :-

Case①. The output of driver circuit is high.



The demand current is zero. and supply is zero. also. Thus we can connect as much as load circuits we want. max Fanout = ∞.

Case ②. $V_o = 0.2V$



We want to consider worst case scenario, thus we will consider D_B of load circuits are off.

I_c = total collector current, I_c' = no. load collector current.

I_L = standard load (current), N = fanout

$$\boxed{I_c = I_c' + N I_L} = 2.182 + N \times 0.82$$

Constraint: When driver circuit's transistor is operating in saturation mode, the collector current can not exceed a certain value. Otherwise, the driver transistor T will change its operating mode saturation to forward active.

Marginal situation will be achieved if $\beta_{forced} \approx \beta_F$ for driver transistor T.

$$\beta_{forced} \approx \frac{I_c}{I_B} \Rightarrow I_{c,max} = \beta_F \times I_B$$ ← case ③

$$= 30 \times 0.4 = 1.2mA$$

Maximum fanout is N'. then the main equation becomes, $I_{c,max} = I_c' + N' I_L$

$$1.2 = 2.182 + N' \times 0.82$$

$$\Rightarrow N' = 11.96$$

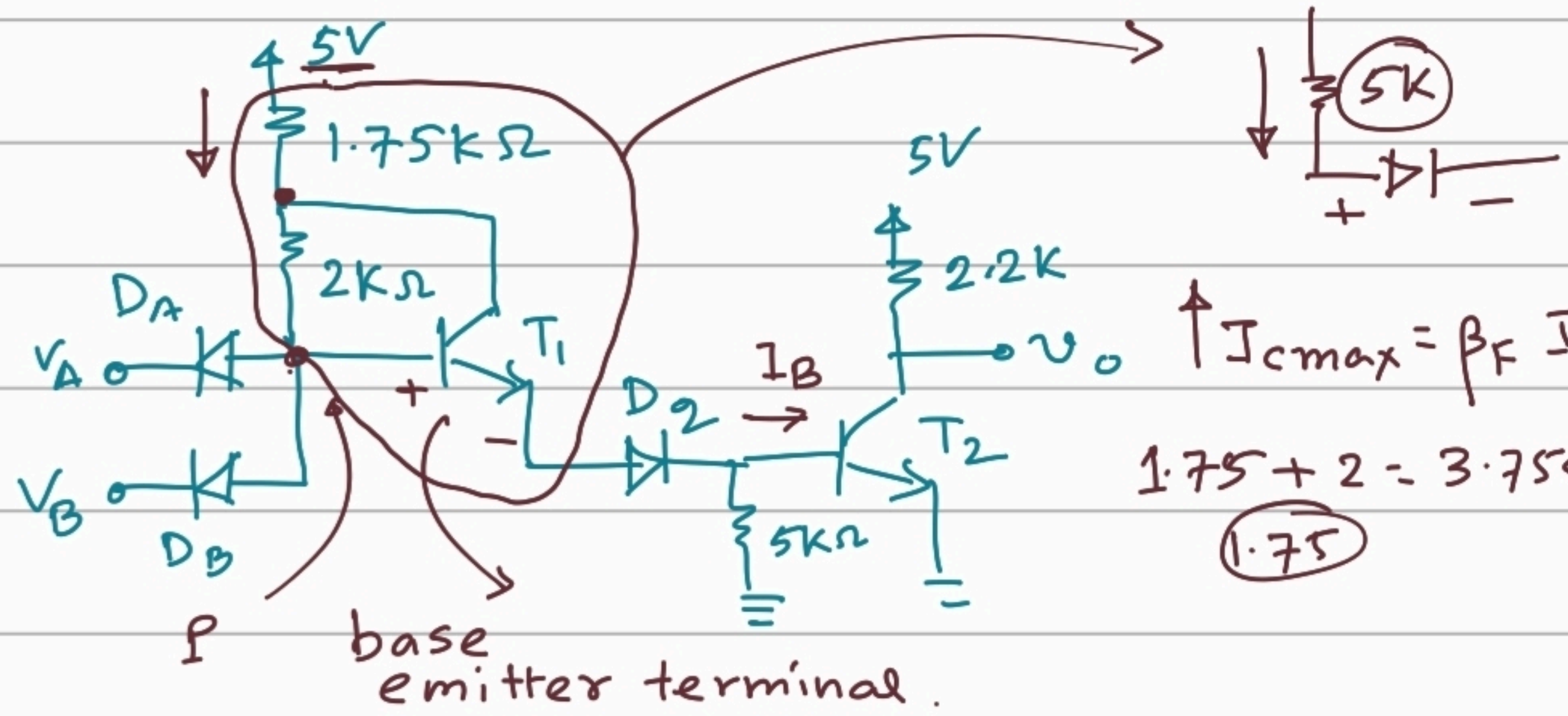
we can not choose maximum fanout $N' = 12$

because that will exceed the value of permitted collector current.

Therefore, maximum fanout for this case $[N'] = 11$

Finally maximum fanout $= \min(11, \infty)$
$= \boxed{11}$

Modified DTL circuit: To increase the number of fanout.



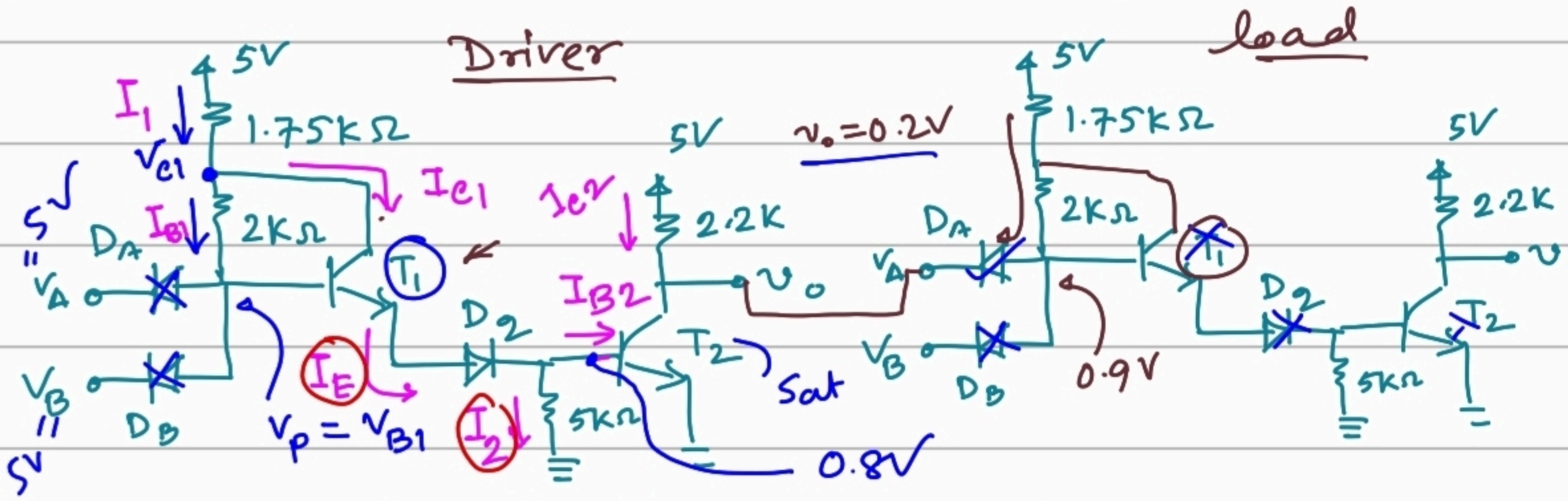
$\uparrow I_{cmax} = \beta_F I_B \uparrow$

$1.75 + 2 = 3.75 < 5$

1.75

Fanout Calculation: Case ① $v_o = 5V$. Similar to regular DTL. Thus fanout $= \infty$.

Case ②: $v_o = 0.2V$ (driver circuit)



$T_2 \rightarrow$ saturation (DTL, saturated), $D_2 \rightarrow$ ON.

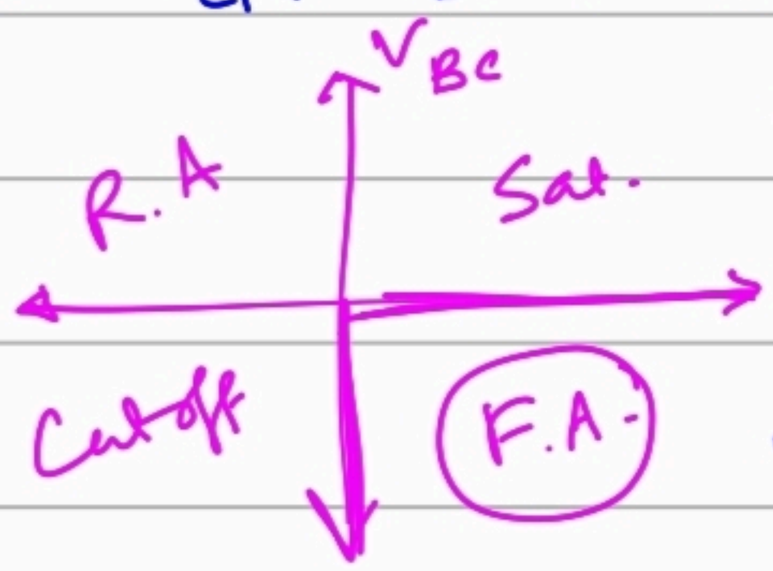
$T_1 \rightarrow$ Forward Active (V)

$T_1 \rightarrow$ ON $\Rightarrow V_{BE} \geq 0.5V$

$I_L = \frac{5 - 0.9}{3.75} = 1.092$ mA

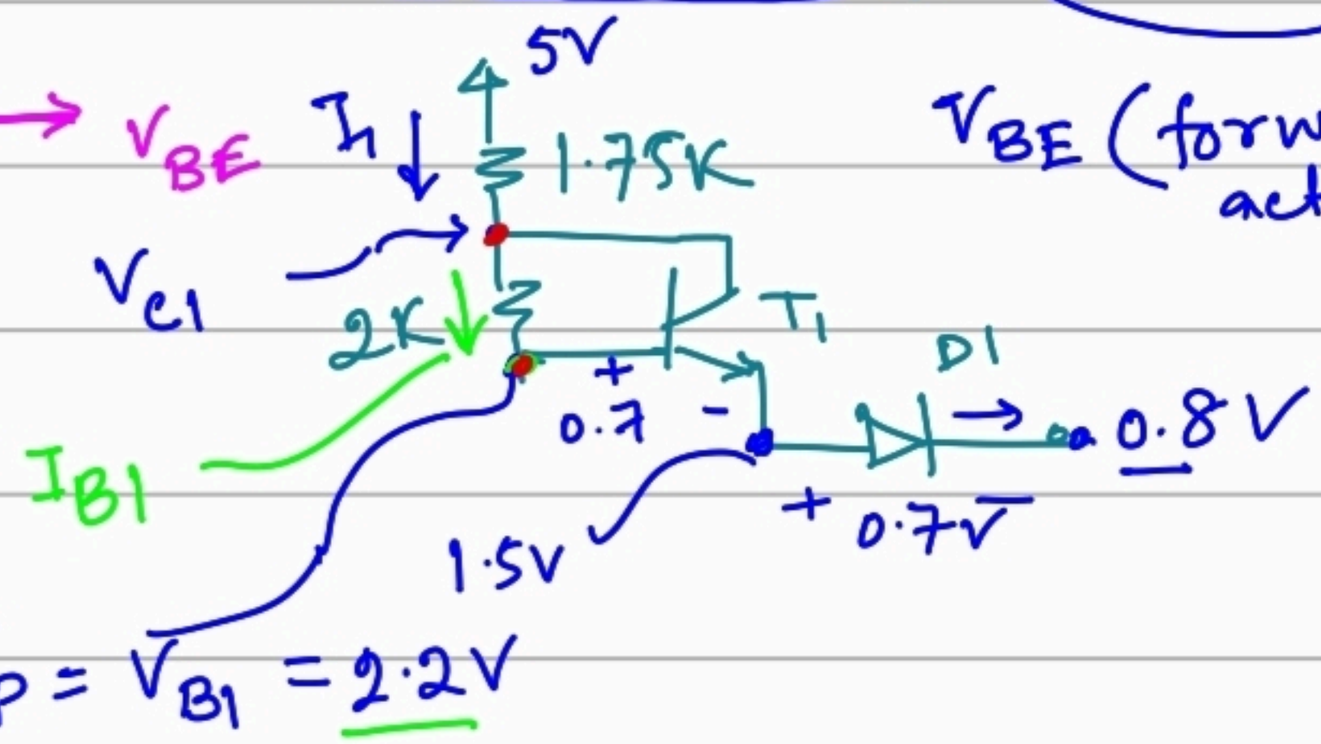
If current will flow from high voltage to low.

So $V_{C1} > V_{B1} \Rightarrow V_{B1} - V_{C1} < 0 \Rightarrow V_{BC1} < 0$.



So. $I_{C1} = \beta_F I_{B1}$, $I_1 = I_{E1}$

V_{BE} (forward active) $= 0.7\,V$



$I_1 = \dfrac{5 - V_{C1}}{1.75K}$, $I_{B1} = \dfrac{V_{C1} - 2.2}{2K}$. $I_1 = I_{E1}$

$I_1 = (\beta + 1) I_{B1}$

$\Rightarrow \dfrac{5 - V_{C1}}{1.75K} = (30+1) \times \left(\dfrac{V_{C1} - 2.2}{2K}\right) \Rightarrow V_{C1} = 2.3V$

$I_E = \dfrac{5 - 2.3}{1.75K} = 1.5432\,mA$, $I_2 = \dfrac{0.8}{5} = 0.16\,kΩ$

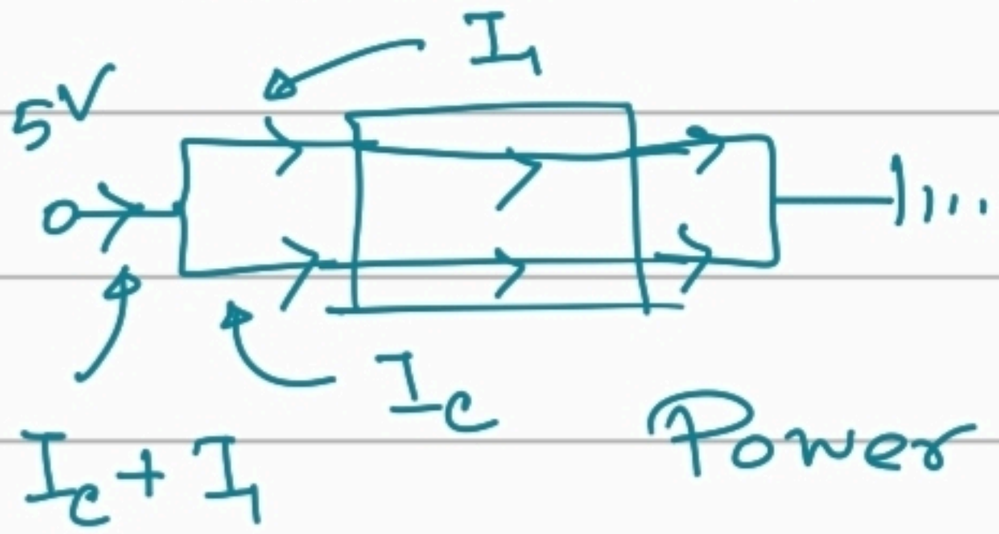
$I_{B2} = 1.383\,mA$, $I_{C,max} = 30 \times 1.383$

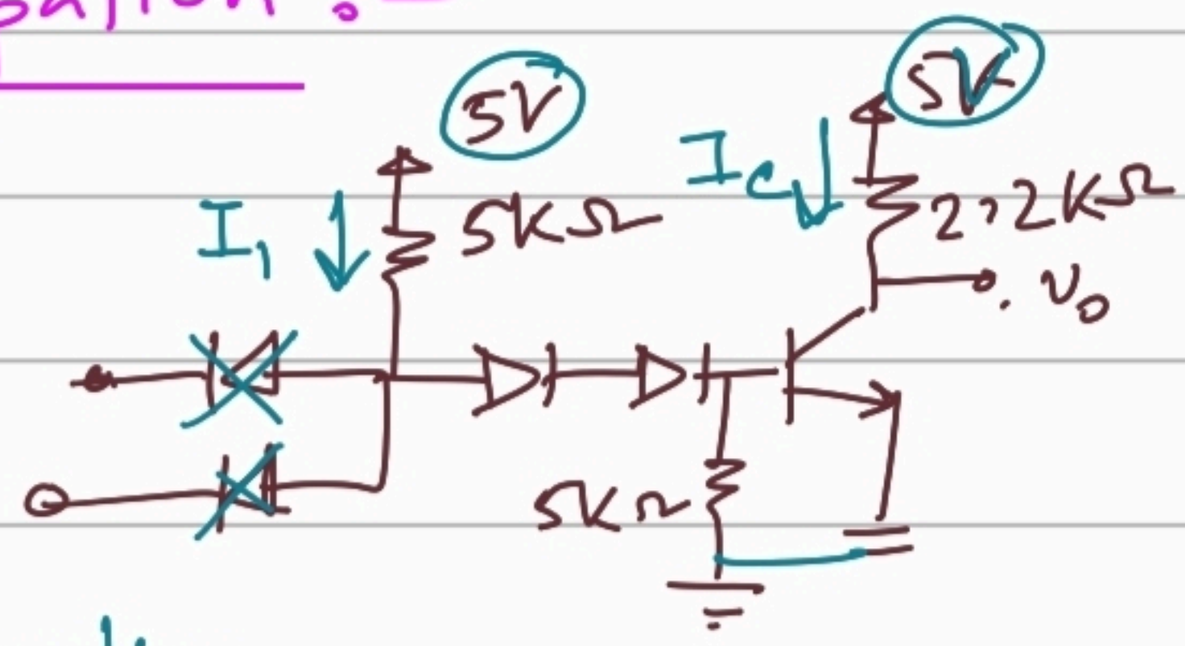
$$\Rightarrow \boxed{\begin{array}{l} 30 \times 1.383 = \underbrace{2.182}_{I_C'} + N' \times \underbrace{1.092}_{I_L'} \\ I_{C,max} = I_C' \end{array}}$$

$\Rightarrow \lfloor N' \rfloor = 35$ = maximum fanout

Maximum Power Dissipation :-

* Case (3) $V_A = V_B = 5V$



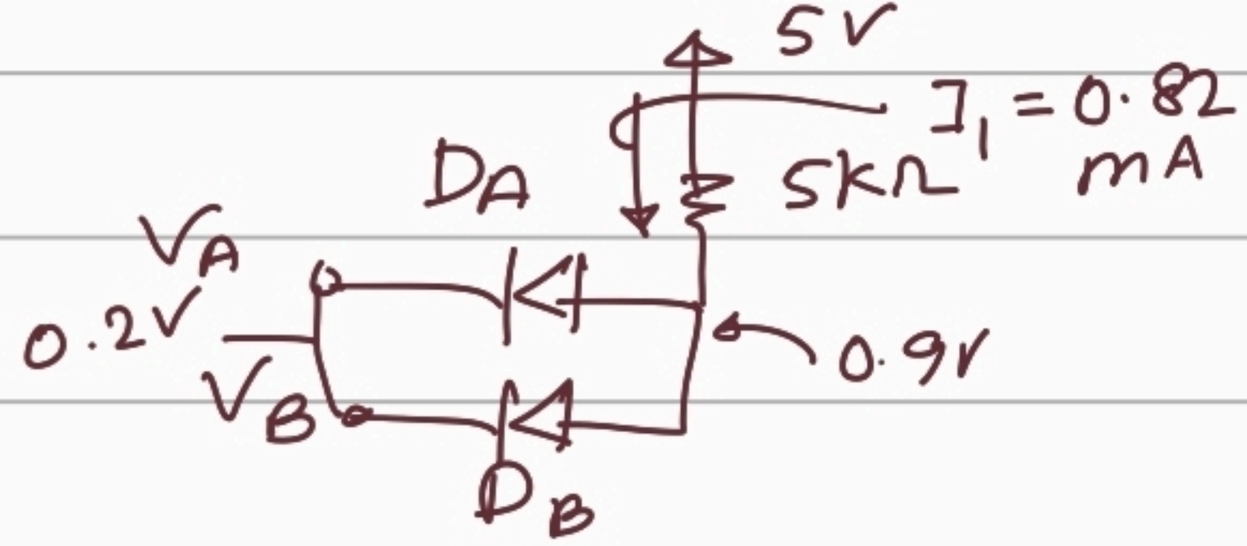


Power dissipation

$= (5 - 0) \times (2.182 + 0.56)$

$= \boxed{13.71\,mW}$

Case ① $V_A = V_B = 0.2$



Power dissipation, $(5-0.2) \times 0.82$

$= \boxed{3.936\ mW}$

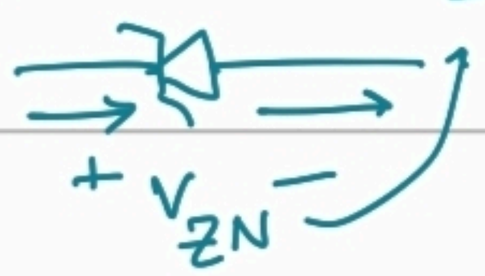
High Threshold Logic: D2 diode ⟷ Zener diode

This will improve the noise margin.

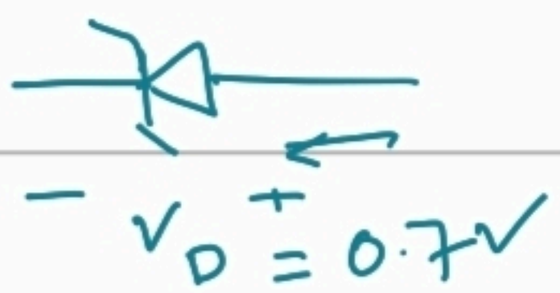
Lecture 7: HTL circuit and introduction to TTL circuit.

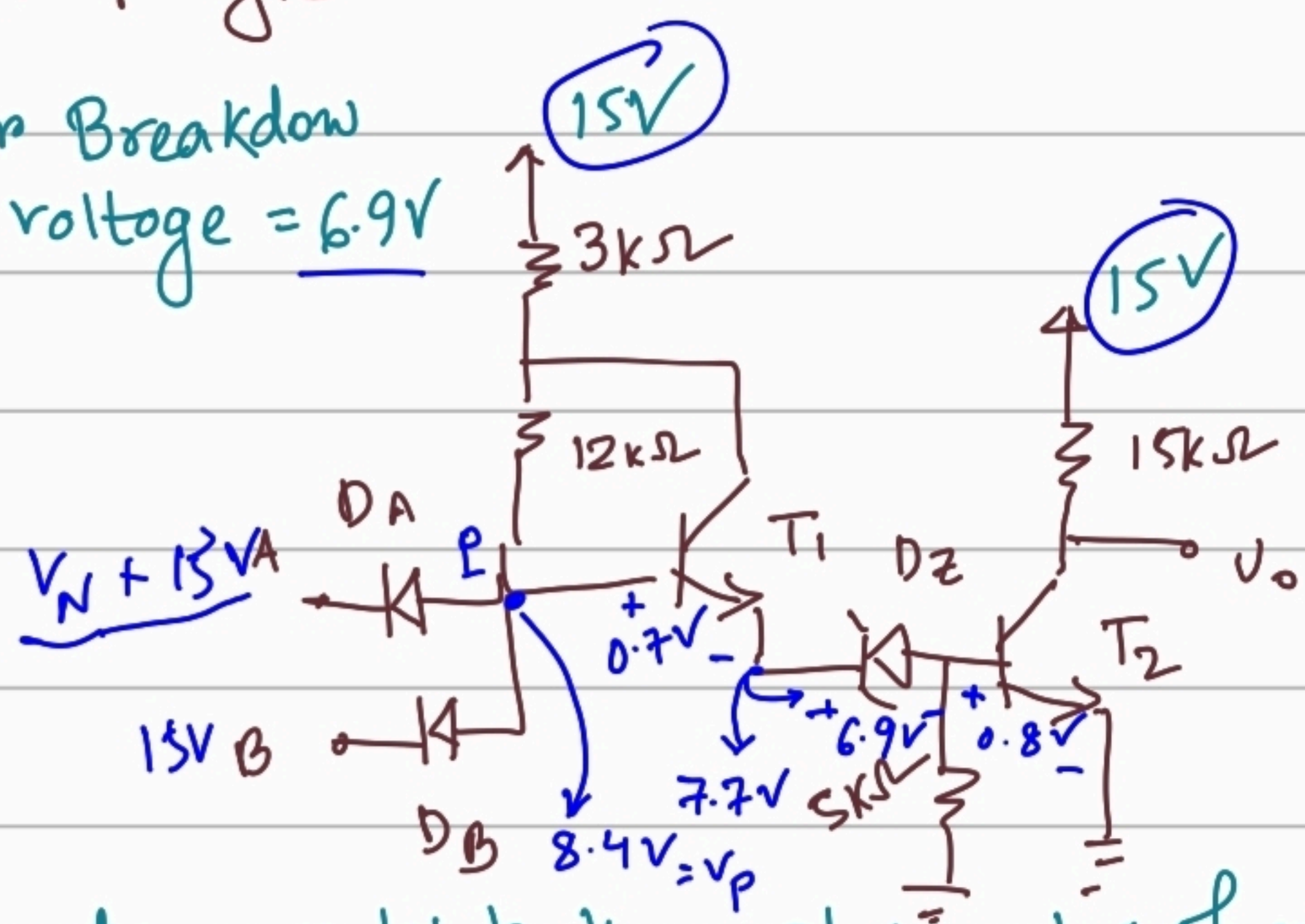
High Threshold Logic:

Q:



Zener Breakdow voltoge = 6.9V



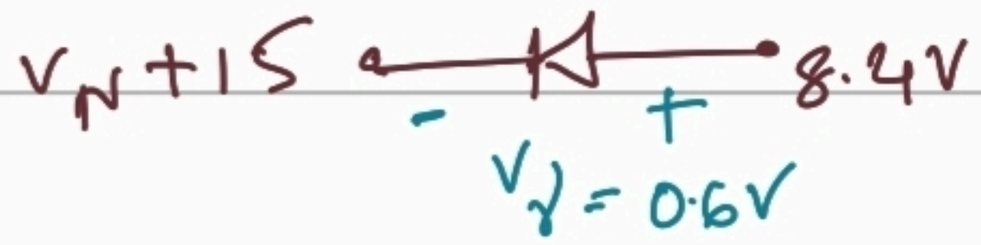


Q: If all the inputs are high, then what value of noise voltage will cause the gate to malfunction?

Ans: Original mode: $D_A, D_B \rightarrow$ OFF, $T_1 \rightarrow$ F.A., $D_Z \rightarrow$ ON, $T_2 \rightarrow$ saturation mode.

The gate will malfunction if noise voltage reduces the V_A to a voltage that allows D_A to turn

on. Because through D_A diode all the currents will drain from the other side.



$8.4 - 0.6 = V_N + 15$

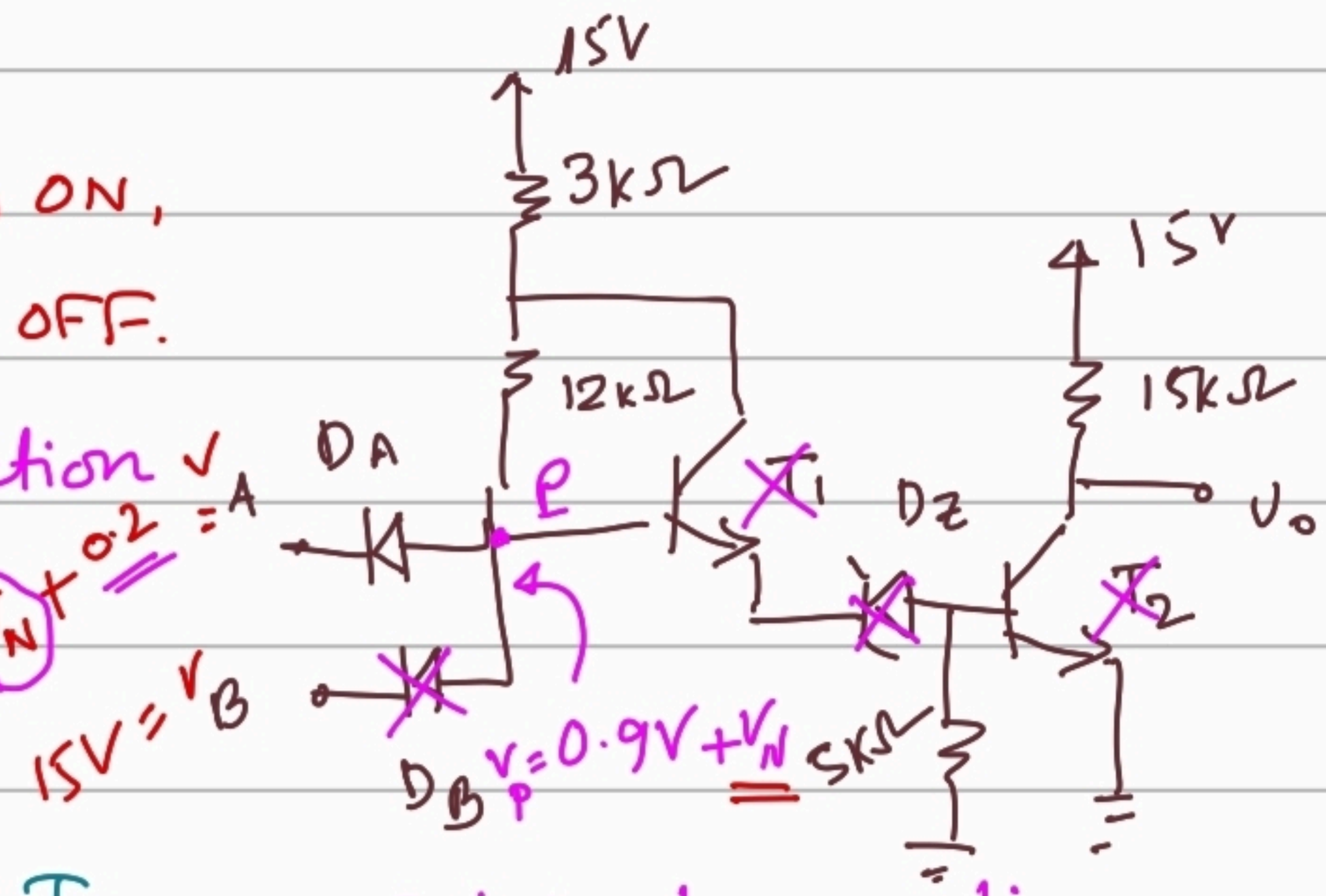
$\Rightarrow V_N = 7.8 - 15 = -7.2V$

High Noise Margin. $\boxed{V_{NH} = 7.2V}$

Q: ② If all the inputs are high except one, then what is the magnitude of noise voltage at that low voltage terminal so that gate will mal-function?

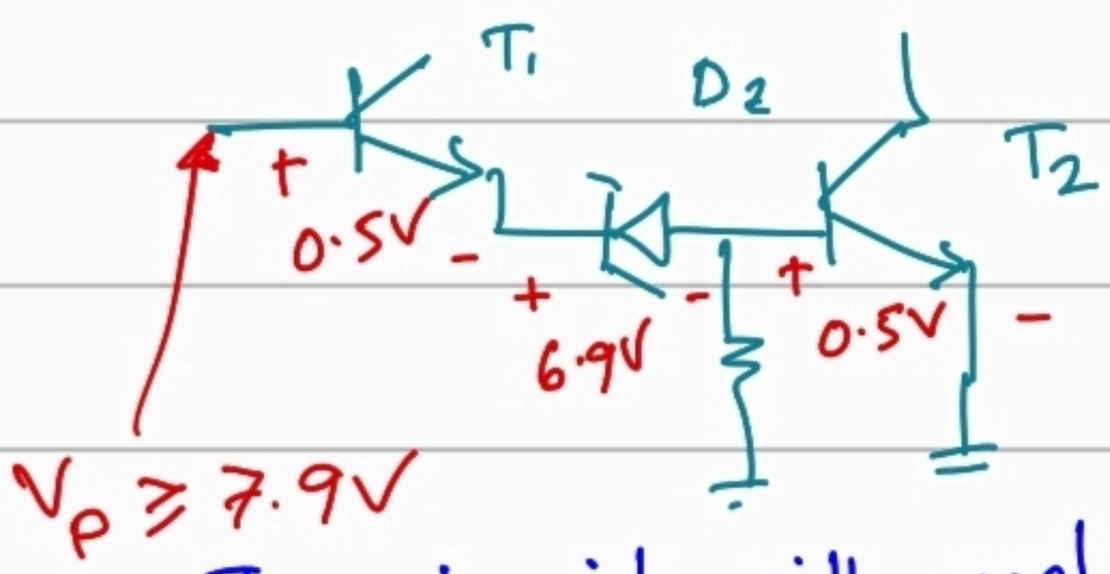
Ans: When $V_N = 0V$. D_A ON, D_B off. $T_1, D_Z, T_2 \rightarrow$ OFF.

If the gate malfunction then T_1, D_Z and T_2 migh turn on.



Original operation

Condition for T_1, D_Z, T_2 to turn on:



V_γ(transistor) $= 0.5V$

V_{ZN} (ON) $= 6.9V$

(cutin voltage = conduction voltage)

The circuit will malfunction if $V_P = 7.9V = V_N + 0.9$

Low Noise Margin. $V_{NL} = 7.9 - 0.9 = 7V$

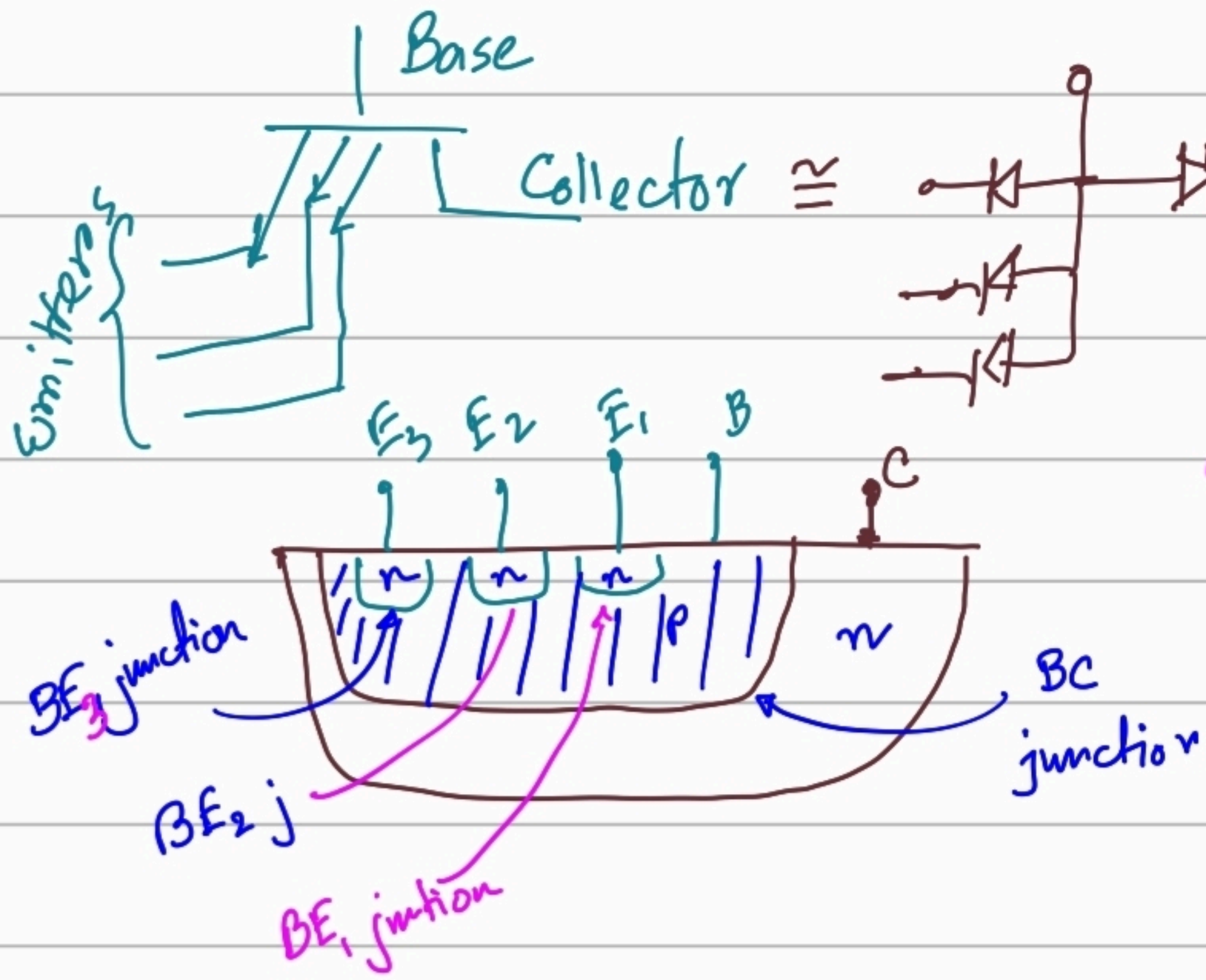
Noise margin. $NM = \min(V_{NL}, V_{NH}) = \boxed{7V}$

"Transistor-Transistor Logic"

Bipolar, → Saturated → TTL
BJT Switching time is faster than DTL.

The input terminals are connected to the emitter terminal of a transistor and the output terminal is connected to a switching transistor.

input terminals will be connected to multi-emitter transistor.



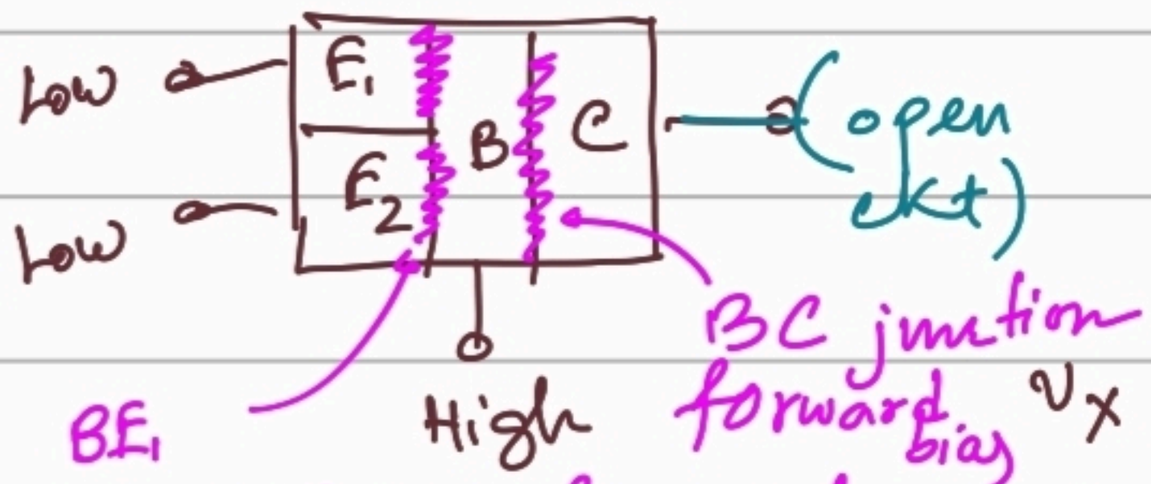
Transistor's operating mode will be determined from three emitter inputs altogether.

Basic Operation:

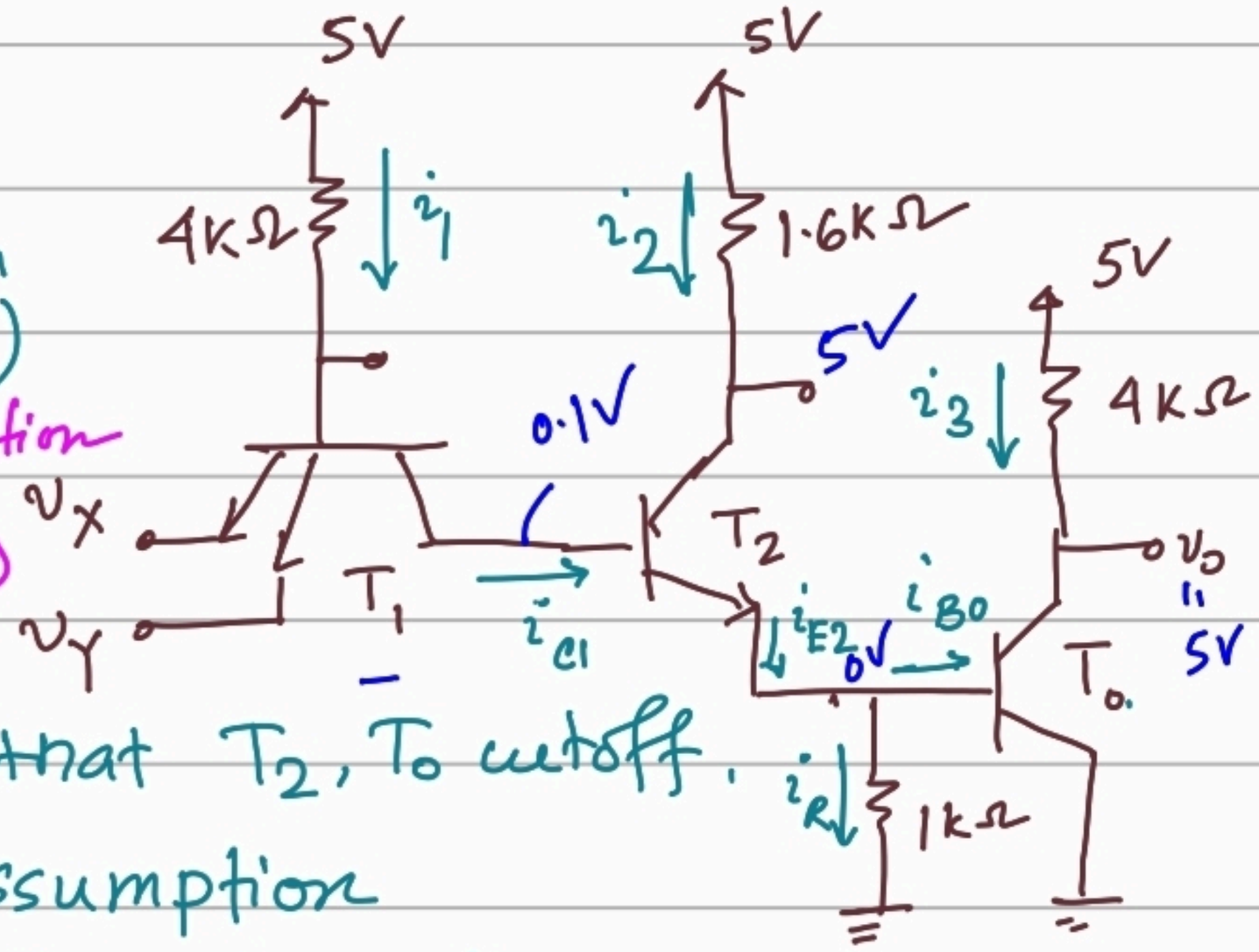
find out the current and voltage of the following gate. Verify that it works like a NAND gate.

Case ①. $v_X = v_Y = 0.1V$ [Neaman] $v_{CE}(sat) = 0.1V$
$v_{BE}(sat) = 0.8V$

For T_1 transistor



BE_2 will be in forward bias.



Our assumption is that T_2, T_0 cutoff.

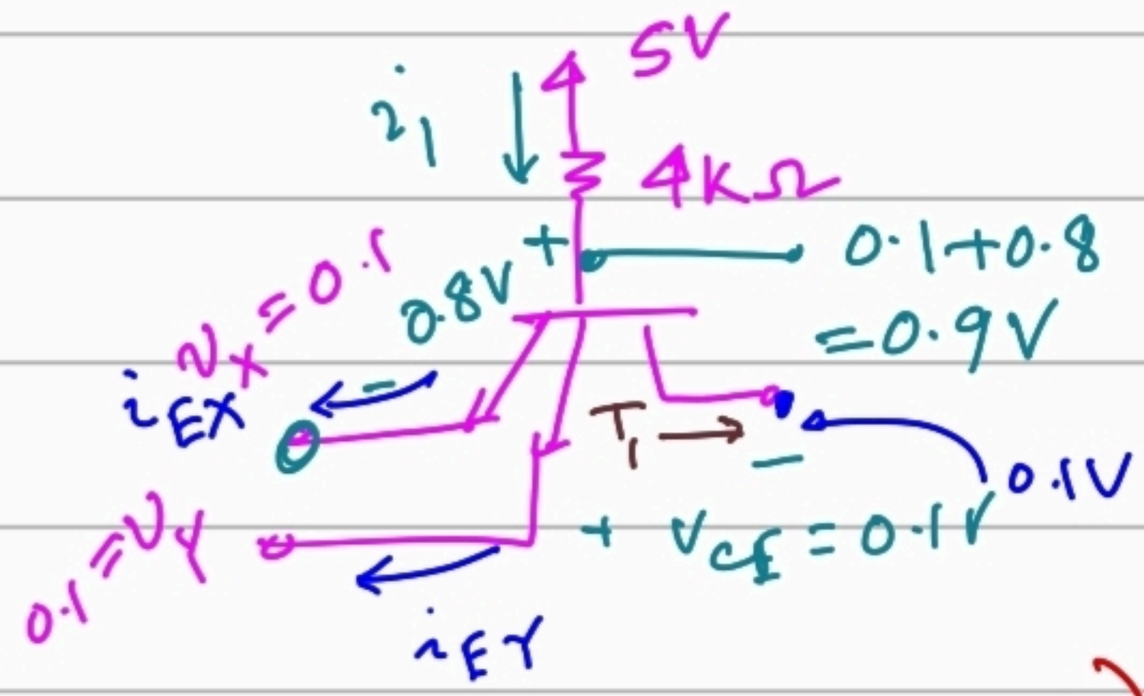
According to our assumption

$$i_2 = i_3 = i_R = i_{B0} = i_{E2} = i_{C1} = 0\ mA$$

Bonus Question: B-C terminal's bias ?

Ans: If B-C reverse bias, T_1 will be in forward active but for forward active we need. $i_C = \beta i_B$. But $i_C = 0$. Therefore not possible.

Hence T_1 must be in saturation mode. $\Rightarrow$ BC-junction is in forward bias

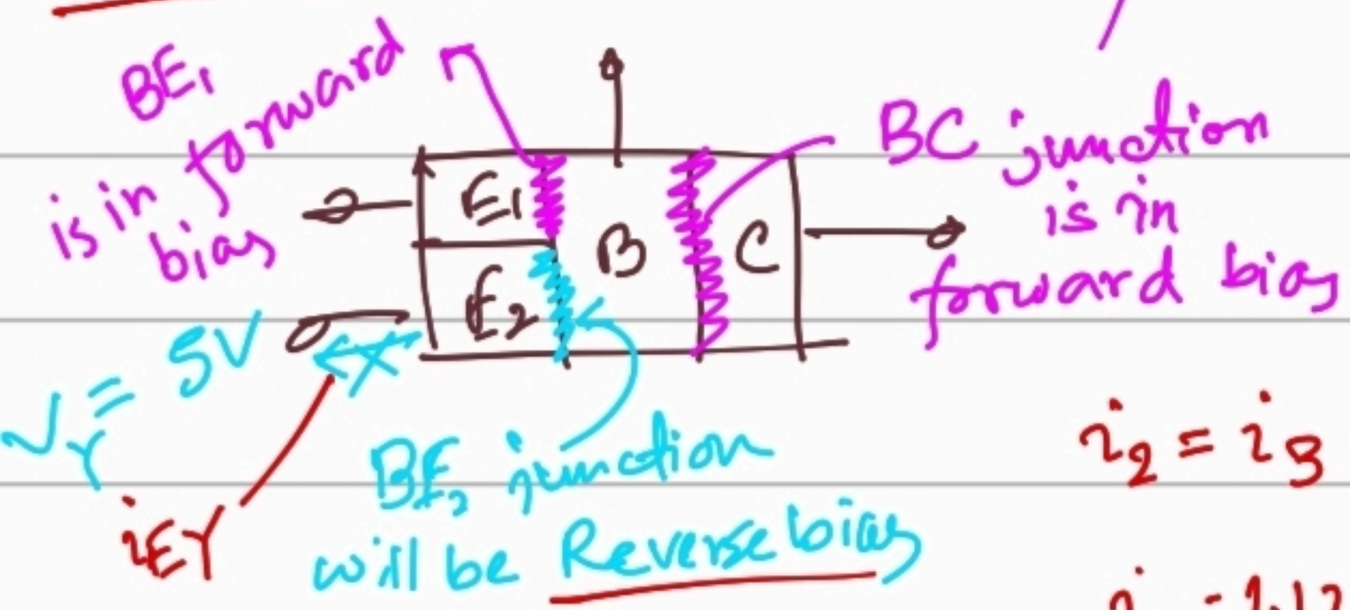


$$i_1 = \frac{5 - 0.9}{4K\Omega} = 1.125\ mA$$

$$i_{EX} = i_{EY} = \frac{i_1}{2} = 0.5675\ mA$$

$$\beta_{forced} = \frac{i_C}{i_B} = 0 < \beta_F$$. Our assumption is valid.

Case ② ($v_X = 0.2V$, $v_Y = 5V$) / $v_Y = 0.2V$, $v_X = 5V$



$T_1 \rightarrow$ saturation.

$T_0, T_2 \rightarrow$ cutoff.

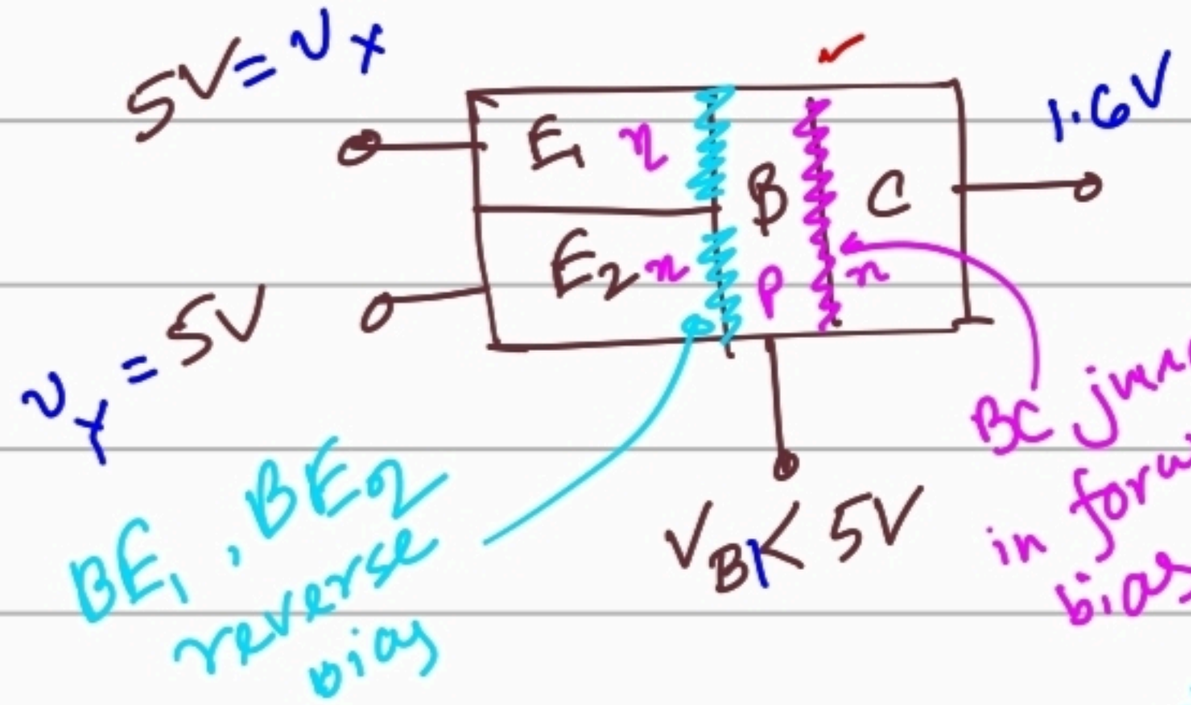
$$i_2 = i_3 = i_{B0} = i_{E2} = i_{C1} = i_R = 0$$

$i_1 = 1.125\ mA$. $\boxed{i_{EX} = i_1,\ i_{EY} = 0}$

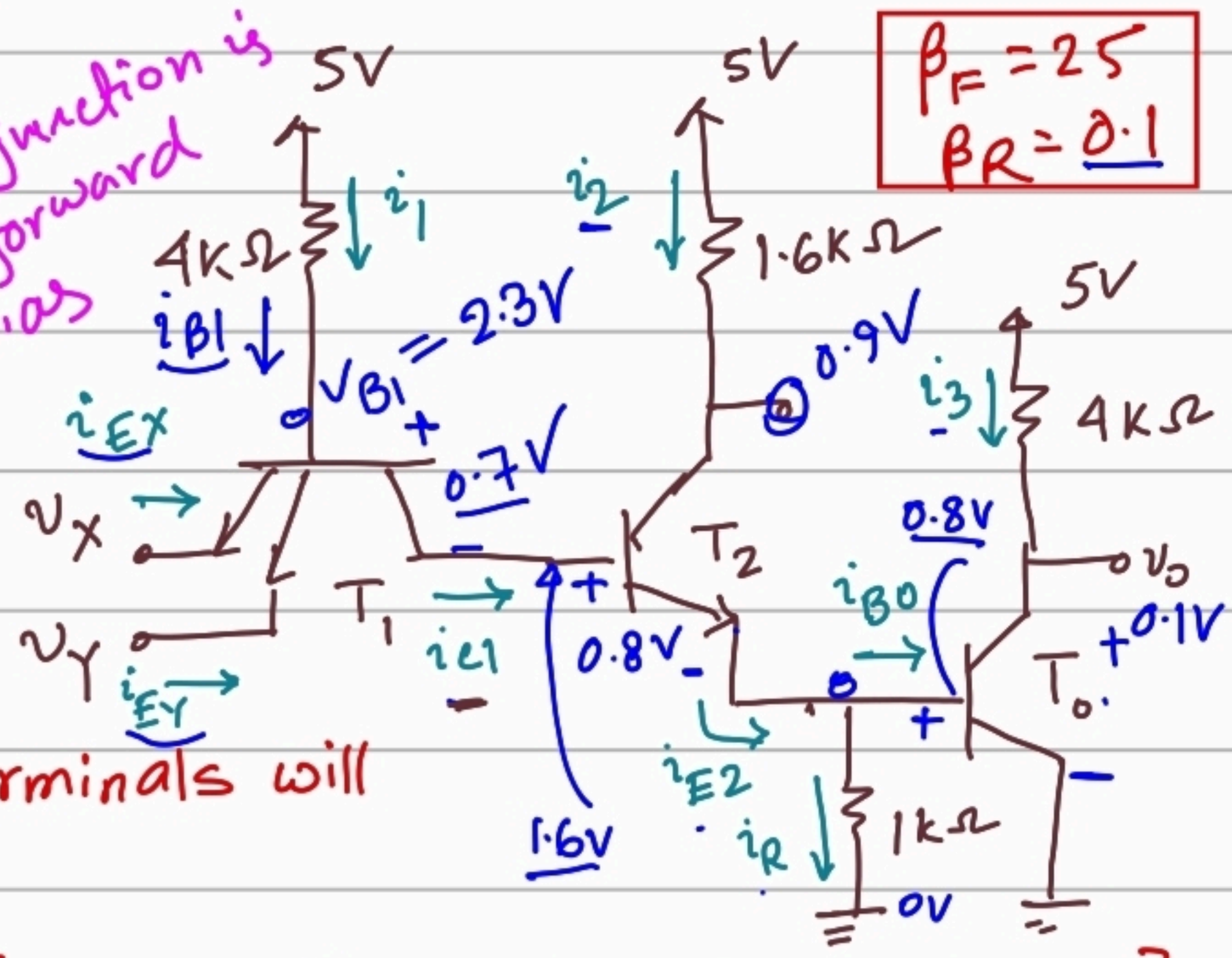
Case 3: $v_X = v_Y = 5V$ | Assumption:

$T_0, T_2 \rightarrow$ saturation

$v_{CE}(sat) = 0.1\,V$, $v_{BE}(sat) = 0.8V$



$\beta_F = 25$
$\beta_R = 0.1$



T_1 transistor must be in reverse active mode.

Collector and Emitter terminals will switch their roles.

V_{BC} (reverse active) = 0.7V. [because BC junction is in forward bias]

($i_{EX} = \beta_R i_B = i_{EY}$) β_R = reverse active current gain.

$i_{B1} = i_1 = \frac{5-2.3}{4k} = 0.675mA$, $i_2 = \frac{5-0.9}{1.6k} = 2.5625mA$.

$i_3 = \frac{5-0.1}{4k} = 1.225mA$, $i_{EX} = i_{EY} = \beta_R i_{B1} = 0.0675mA$

$i_{C1} = i_{EX} + i_{EY} + i_{B1} = 0.81mA$, $i_{E2} = i_2 + i_{C1} = 3.3725\,mA$,

$i_R = \frac{0.8-0}{1k} = 0.8mA$, $i_{B0} = i_{E2} - i_R = 2.5725mA$

$\beta_{forced}(T_2) = \frac{i_2}{i_{C1}} = \frac{2.5625}{0.81} = 3.16 < \beta_F = 25$

$\beta_{forced}(T_0) = \frac{i_3}{i_{B0}} = \frac{1.225}{2.5725} \approx 0.47 < \beta_F = 25$

Our assumptions are valid.

v_X	v_Y	v_0
0.1	0.1	5
0.1	5	5
5	0.1	5
5	5	0.1

This circuit works like a NAND gate.

Lecture 8: TTL circuit (continued)

Find the maximum fanout for the following circuit.

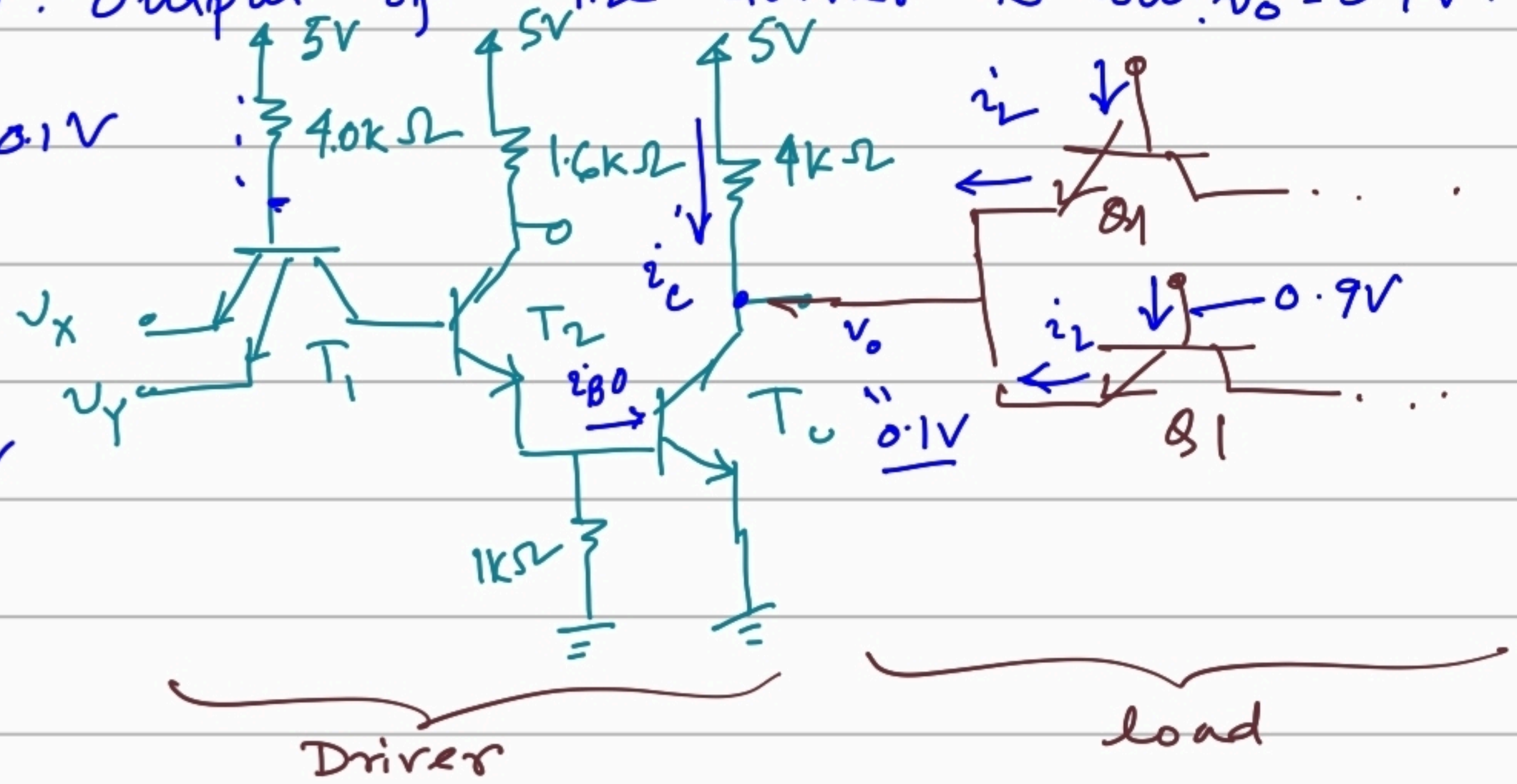
Case ①: Output of the driver is low. $v_o = 0.1\,V$.

$v_{c}(sat) = 0.1\,V$

$\beta_F = 25$

$\beta_R = 0.1$

$v_{OH} = 3.4\,V$



$T_0 \rightarrow$ sat, $T_2 \rightarrow$ sat.. $T_1 \rightarrow$ F.A (driver circuits).

$Q_1 \rightarrow$ sat. (load circuit).

i_c' = no load collector current $= \frac{5-0.1}{4k} = 1.225\,mA$

i_L = individual load current $= \frac{5-0.9}{4} = 1.025\,mA$

i_{B0} = base current of T_0 = 2.5725 mA.

$$i_{c,max} = \beta_F\, i_{B0} = 25 \times 2.5725$$

$$= i_L \times N + i_c' \quad (N \rightarrow \text{number of fanout})$$

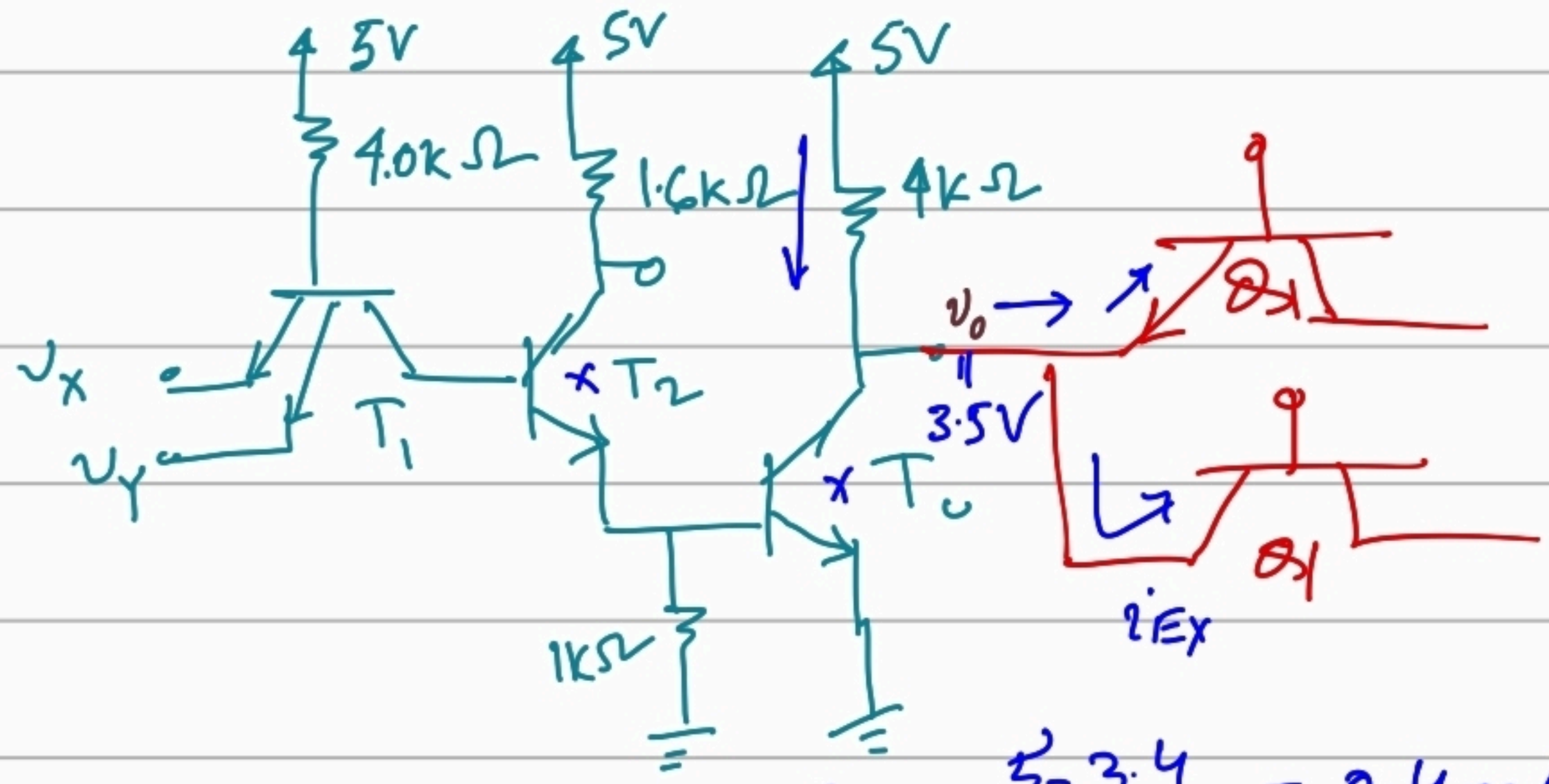
$$= 1.025 \times N + 1.225$$

By solving for N we get. $N = \lfloor 61.35 \rfloor = 61$.

Case: 02. The output of the driver circuit is high.

output voltage, $v_o = 3.4\,V$. (High voltage)

$T_0, T_2 \rightarrow$ cutoff, $T_1 \rightarrow$ sat. $Q_1 \rightarrow$ Reverse active.



maximum supply current, $= \frac{5-3.4}{4} = 0.4\,mA$

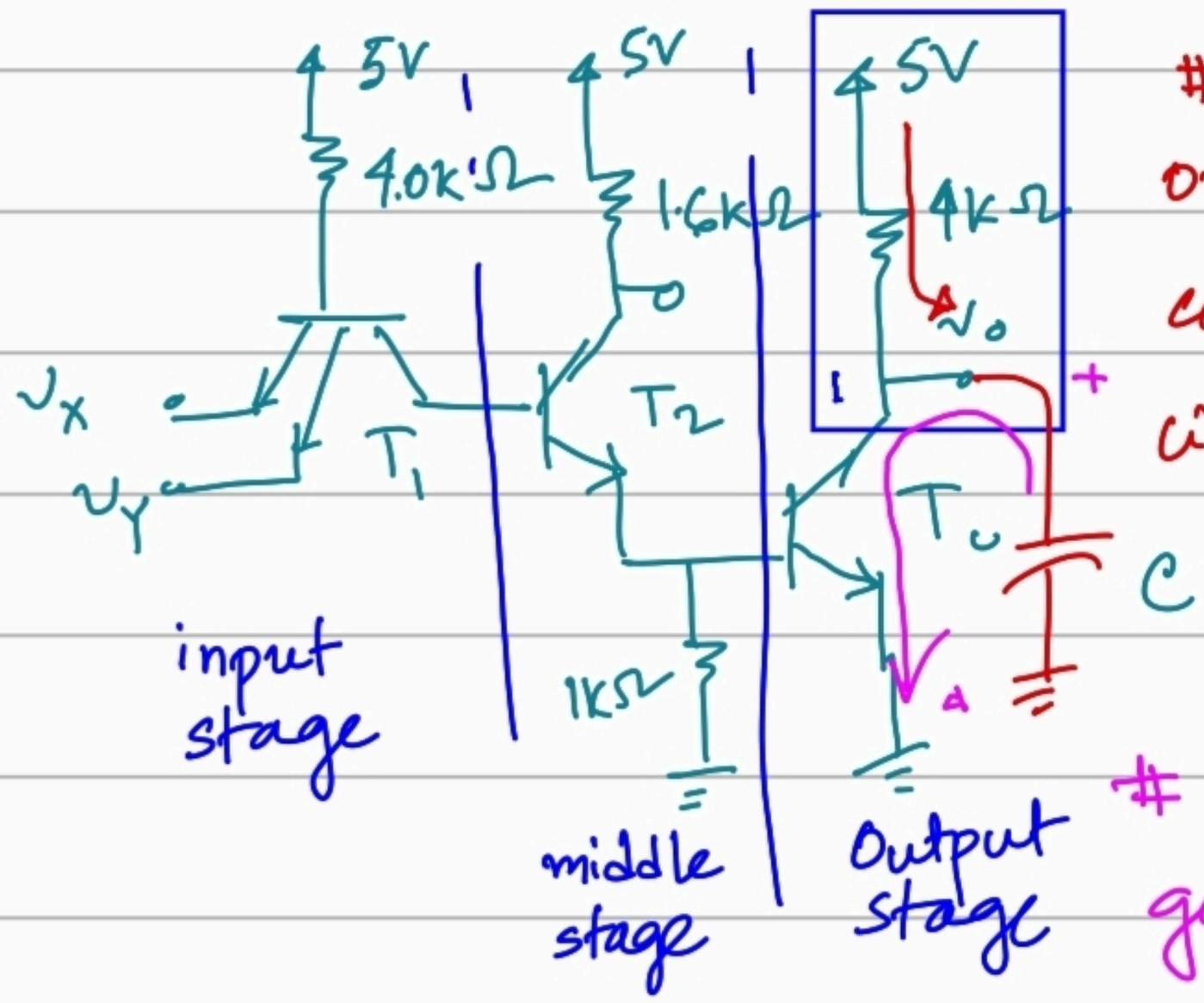
individual demand current, $i_{EX} = 0.0675\,mA$.

$\therefore$ max. Fanout $= \left\lfloor \frac{\text{supply}}{\text{demand}} \right\rfloor = \left\lfloor \frac{0.4}{0.0675} \right\rfloor = \lfloor 5.92 \rfloor = 5$

Finally the maximum fanout $= \min(5, 61)$

$= \boxed{5}$

TTL output stage classification :-



Because the output of any circuit is connected to many other circuits. we can lump their effect into a fictitous capacitor.

when output is going from high to low, we need to discharge the capacitor. In this

case To transistor is needed to be saturation mode.

When output goes from low to high, the capacitor gets charge from 5V, through the 4kΩ.

The switching speed (transition from low-high or high to low) totally depends on the resistances and the capacitor value.

The section of the circuit responsible for charging the capacitor and pull up the voltage of the output from low to high is called pull-up network.

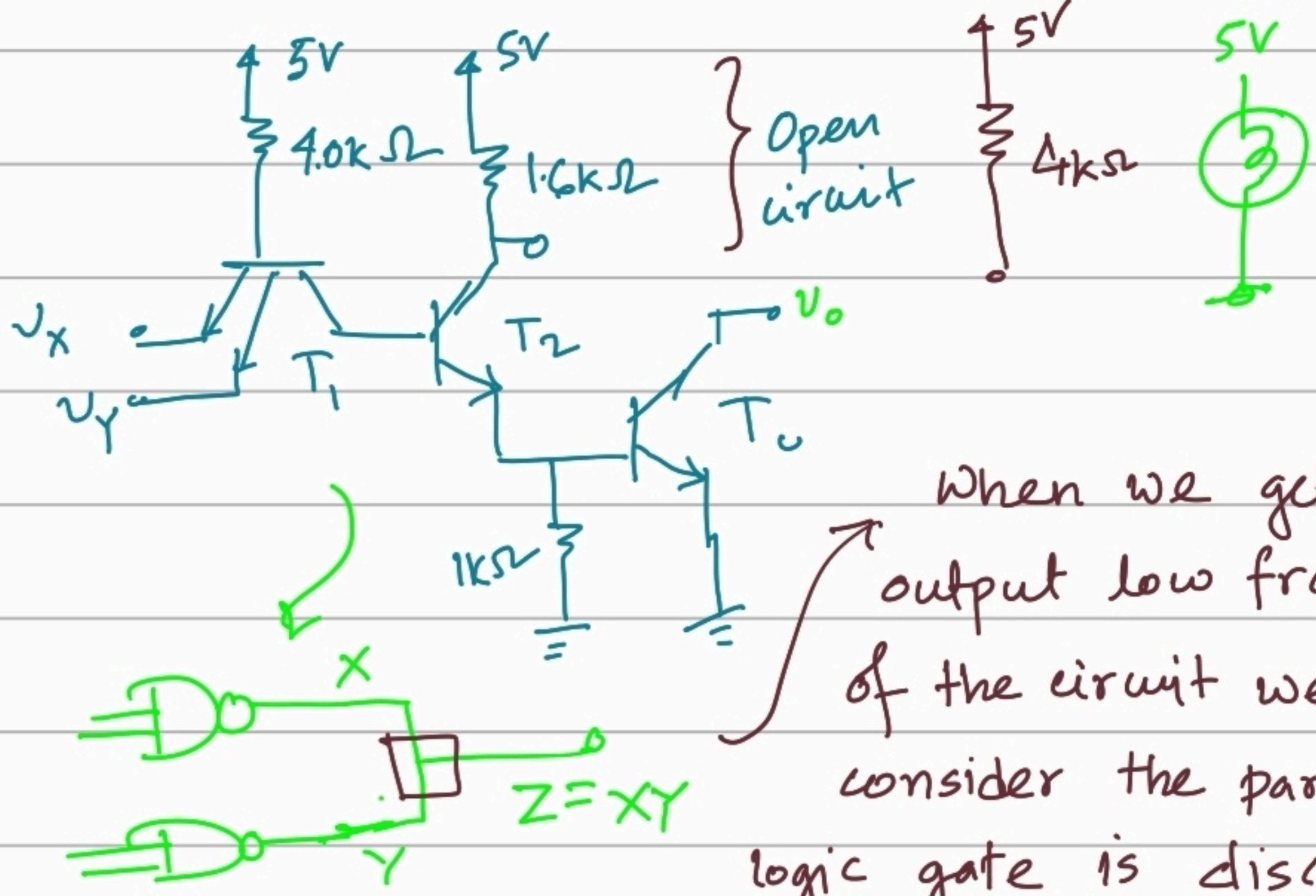
Similarly, there is a part of circuit is called pull-down network.

TTL circuits are classified into three categories depending on the output stage structure.

* Open collector output stage ✓
* Totem-pole output stage.
* Tristate output stage.

ⓐ Open collector output stage:

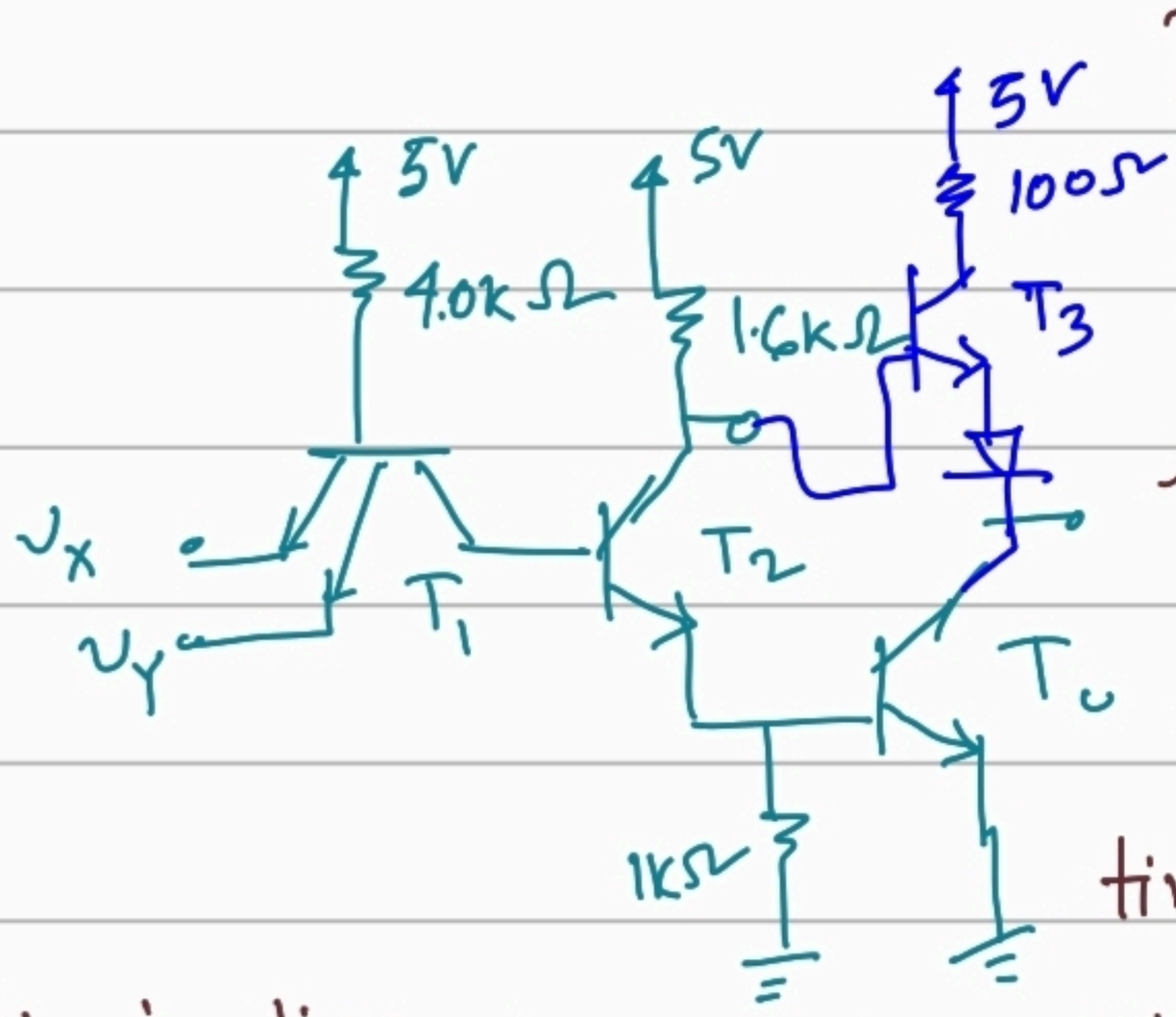
The collector terminal of the output stage is an opencircuit. Usage: open port, Wired AND gate.



When we get output low from any of the circuit we can consider the part of that logic gate is disconnected.

Wired-AND

b) Totem-pole Output stage:



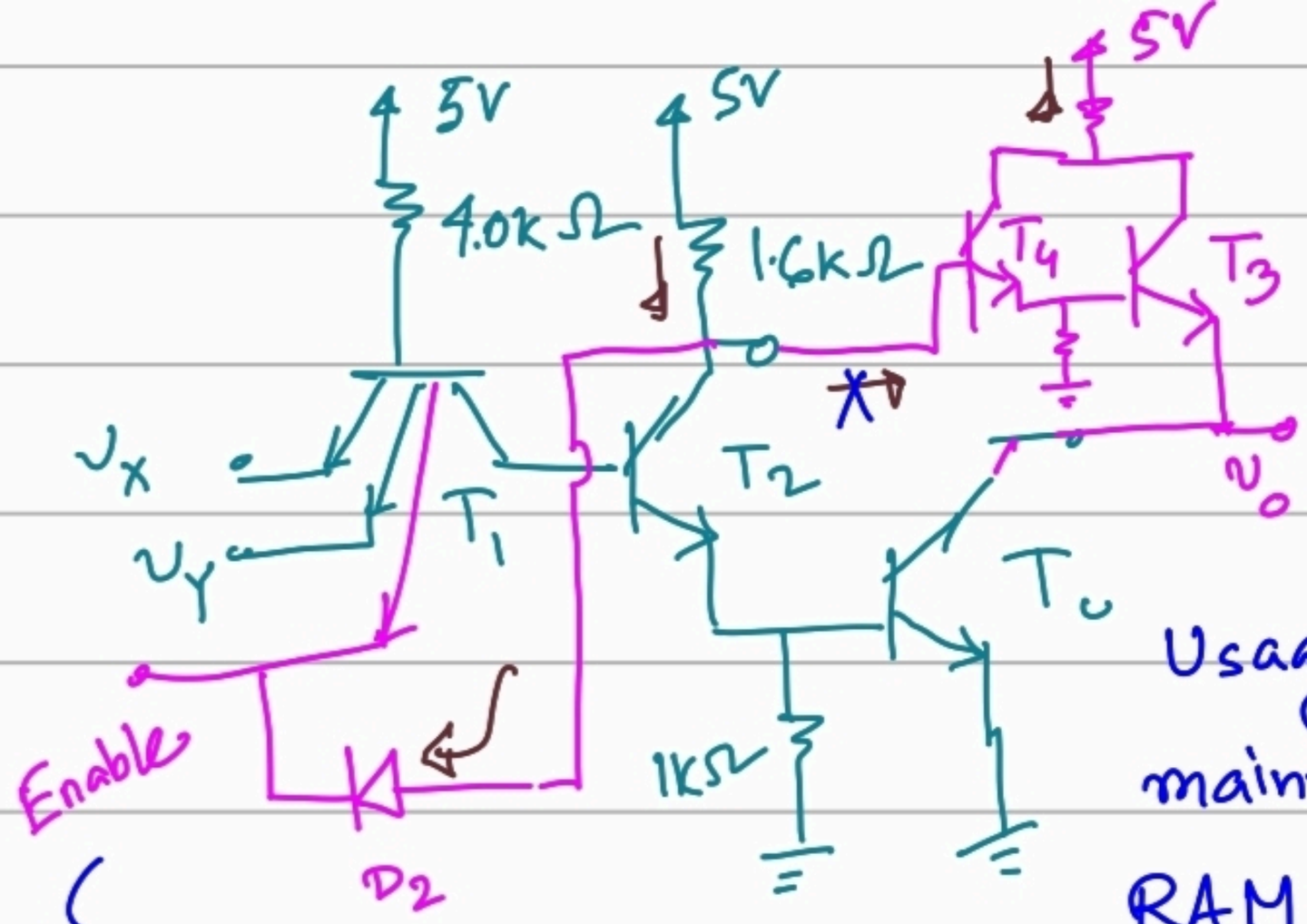
This new part can charge the capacitor faster. because it is made out of active circuit component like BJT.

Thus low to high transition time decreases while power dissipation is not increasing that much.

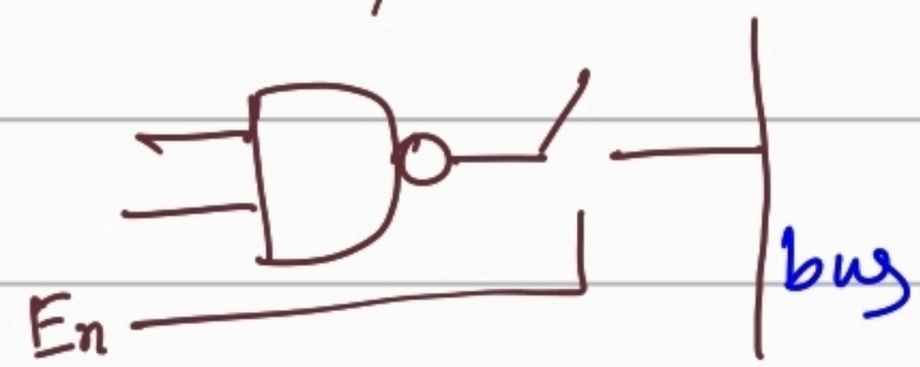
$$\boxed{\text{Switching speed increases due to active pull-up network.}}$$

c) Tristate output stage:

Output could be three types.
1. logic high
2. logic low



③ high impedance state / open circuit.



Usage: It is used to maintain connection between RAM output to data bus inside microprocessors.

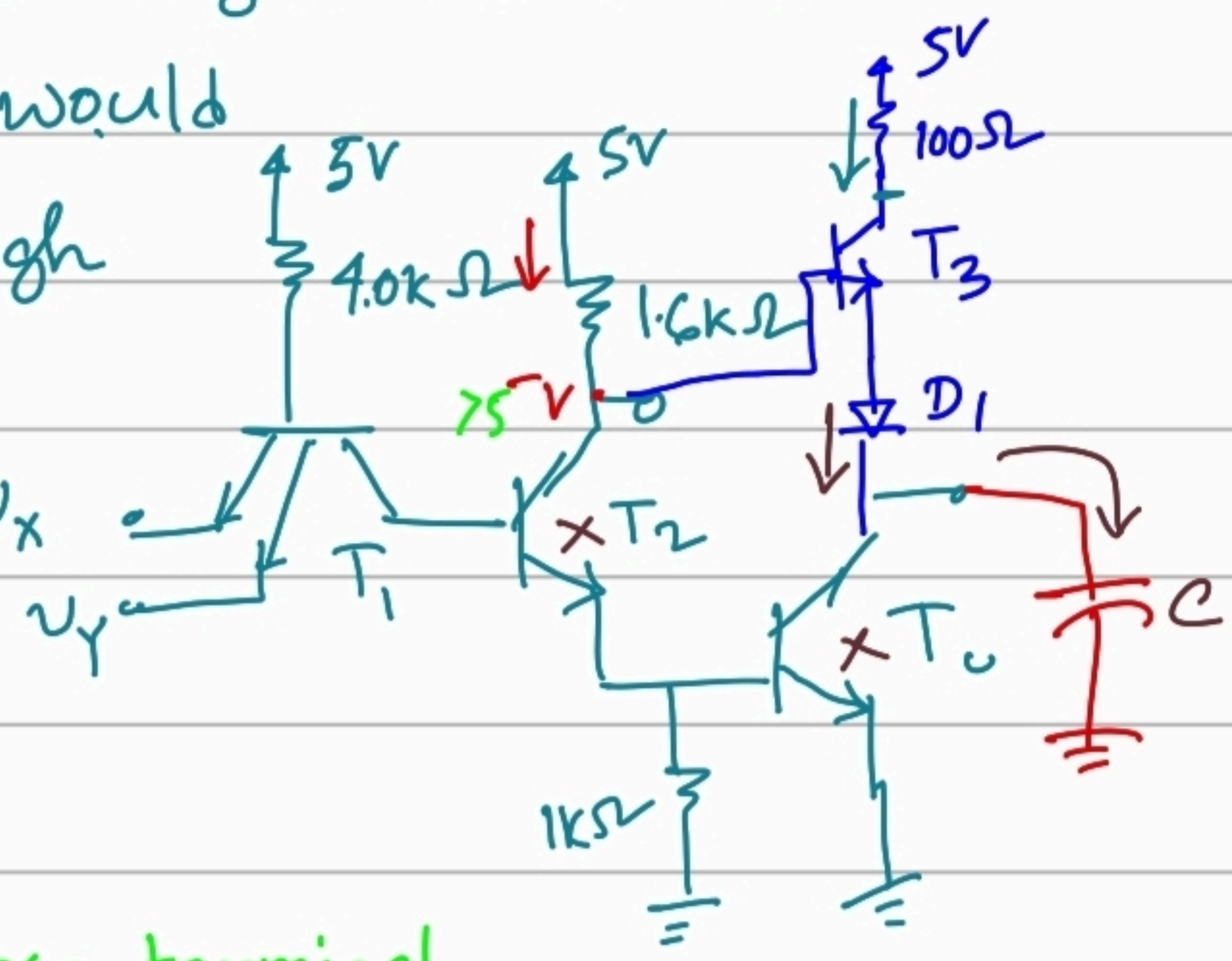
if enable pin is low. $T_1 \rightarrow$ sat, $T_2 \rightarrow$ cutoff, $T_0 \rightarrow$ cutoff. T_4, $T_5 \rightarrow$ cutoff. Thus output is disconnected from the rest of the circuit.

Basic operation of Totem-pole NAND gate:

Case ①: At least one input is at low voltage.

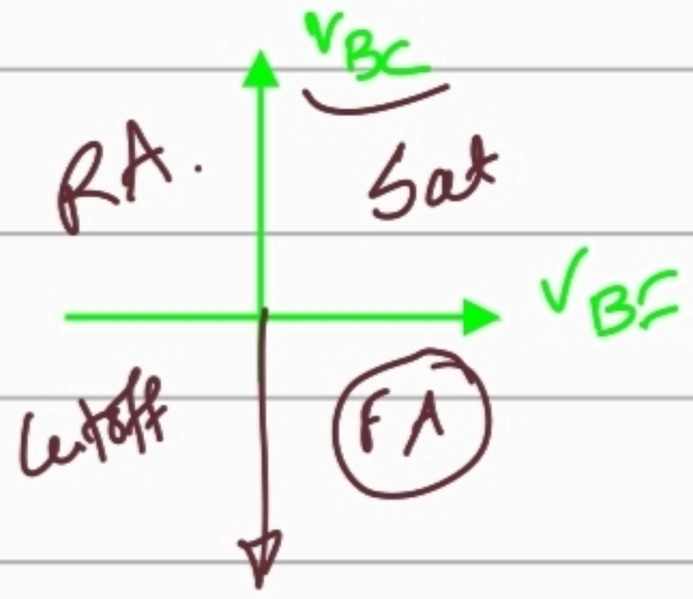
$T_1 \rightarrow$ Sat. T_2. $T_0 \rightarrow$ cutoff.

So base voltage of T_3 is high. So, we assume T_3 is ON. Then there would be some current through 100Ω resistance and collector terminal might have voltage less than 5V.



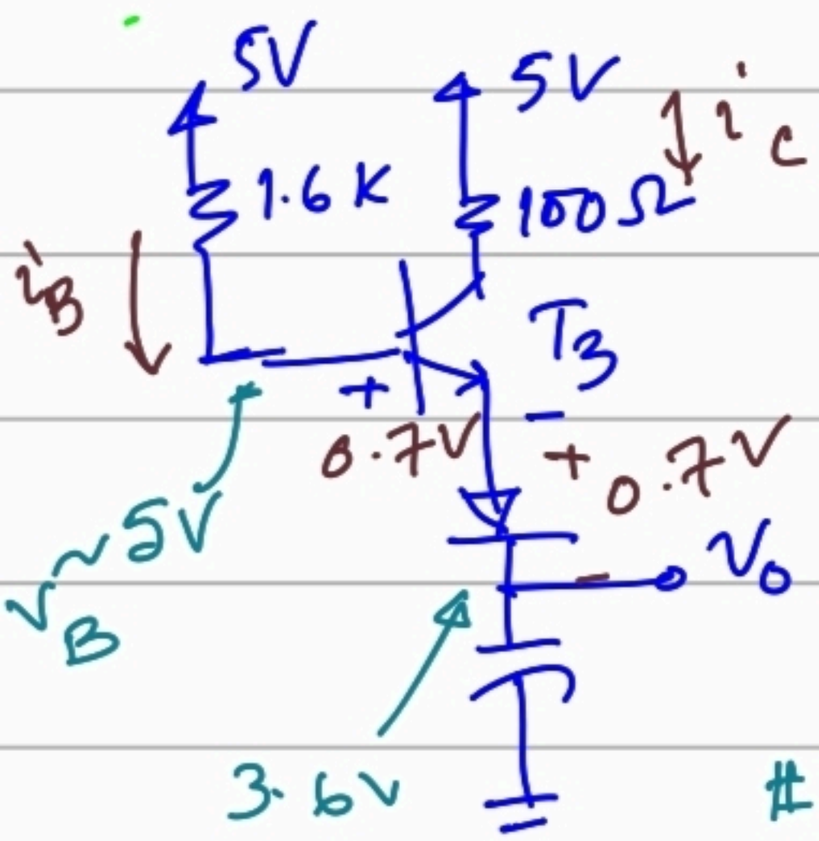
$V_B < 5V$, $V_C < 5V$. Now base terminal

has higher resistance. Therefore, $V_B < V_C \Rightarrow V_{BC} < 0$.



T_3 transistor might operate in forward active mode.

When we arrive near the "steady" state situation, the capacitor is almost done charging. and $i_B \approx 0$ and $i_C \approx 0$.



This will cause the base voltage of T_3 to be almost equal to 5V.

Finall $0.7 + 0.7 = 1.4$ V drop will make output voltage to $\boxed{3.6V}$.

We should take output/input logic high as $\boxed{3.6V}$ for totem pole circuit.

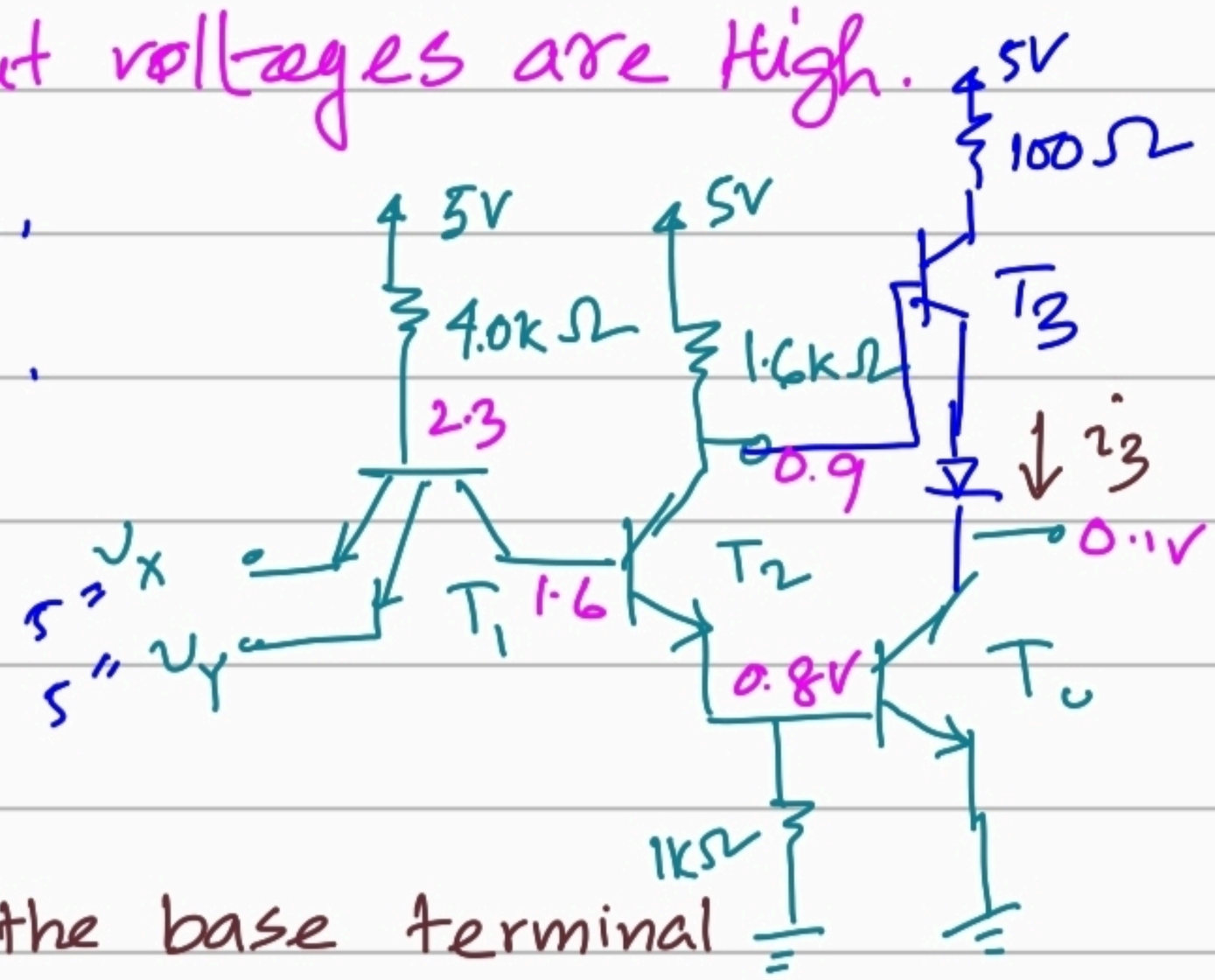
Other values would have been similar to open collector output stage circuit.

Case ②. All the input voltages are High.

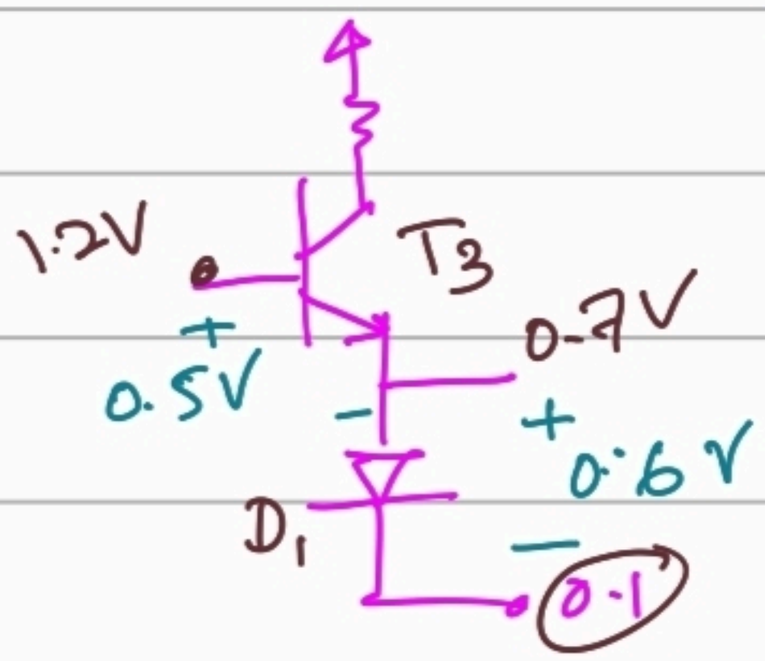
T_1, → Reverse active.

T_2, T_o → Saturation.

If we examine the output stage seperately we get,



we need 1.2V at the base terminal



of T_3 transistor.

But we have 0.9V there. So T_3 and D_1 diode can not turn on in this case.

Other than $i_3 = 0$, rest of the analysis is same as open collector output stage.

Fanout of Totem-pole Nand Gate:

Neamann's book. Exercise (17.6)

Transistor parameters. $\beta_F = 20$, $\beta_R = 0.1$

(a) Calculate the maximum fanout for $v_X = v_Y = 5V$.

(b) Calculate the maximum fanout $v_X = v_Y = 0.1V$ (Assume that v_o is allowed to decrease by 0.1V from the no load condition).

Lecture 9: Introduction to ECL.

Calculation of maximum fanout:

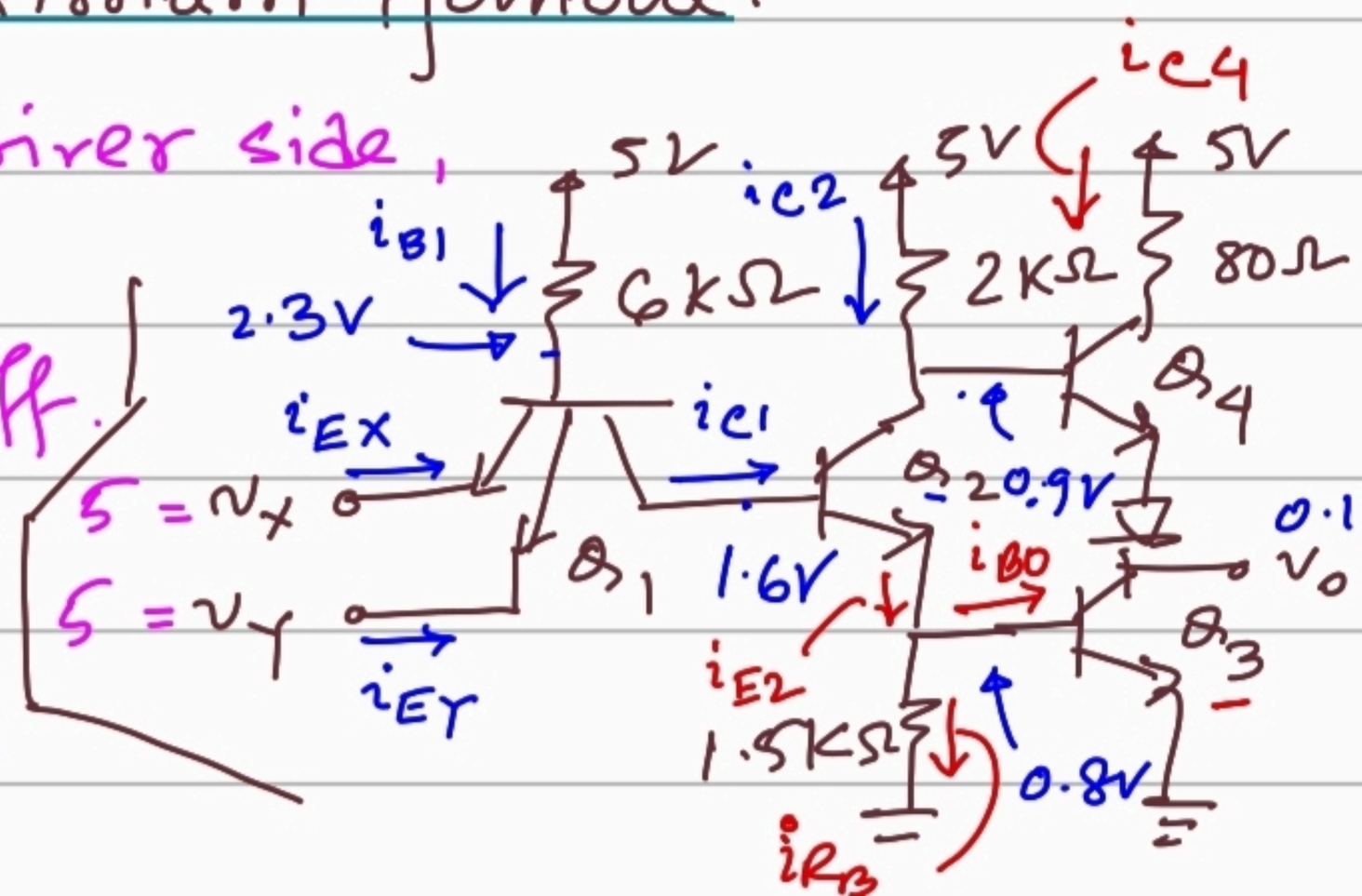
(a) $v_X = v_Y = 5V$. In driver side,

$Q_1 \rightarrow$ Reverse active

$Q_2, Q_3 \rightarrow$ sat, $Q_4 \rightarrow$ cutoff.

$$i_{B_1} = \frac{5 - 2.3}{6K} = 0.45mA$$

$$i_{EX} = i_{EY} = \beta_R i_B = 0.045mA$$



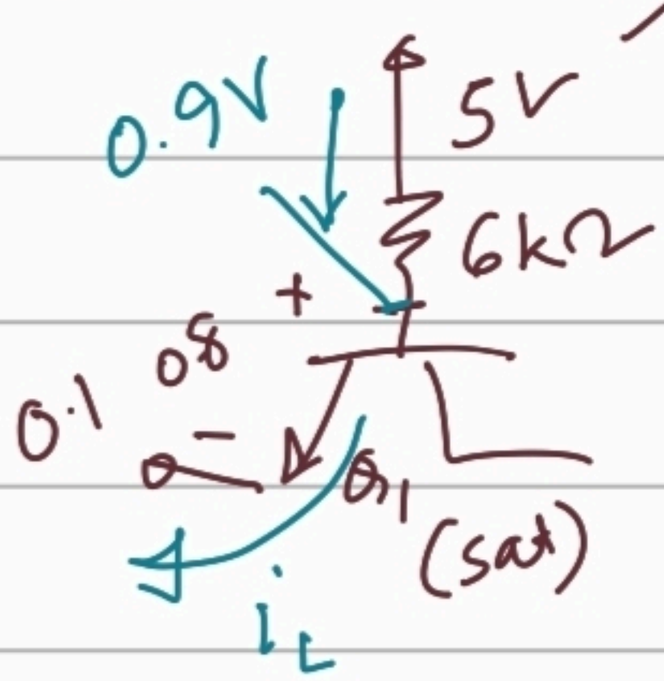
$i_{C1} = i_{B1} + i_{EX} + i_{EY} = 0.54\,mA = i_{B2}$

$i_{C2} = \frac{5-0.9}{2K} = 2.05\,mA$, $i_{E2} = i_{B2} + i_{E2} = 2.59\,mA$

$i_{R_B} = \frac{0.8-0}{1.5K} = 0.53\,mA$, $i_{B3} = i_{E2} - i_{RB} = 2.06\,mA$

$i_{C4} = i_{B4} = i_{E4} = i_{C3,noload} = 0$ [because Q_4 is off]

Now in load side Q_1 should be in saturation and the maximum load current is,



standard load, $i_L = \frac{5-0.9}{6k}$

$= 0.68\,mA$

Key equation:

$i_{c,max} = \beta_F i_{B3} = i_{c,noload} + N \times i_L$

$\Rightarrow 20 \times 2.06 = 0 + N \times 0.68$

$\boxed{N = 60}$

(b) If the inputs are 0.1 V. $v_{OH} = (3.6 - 0.1)$

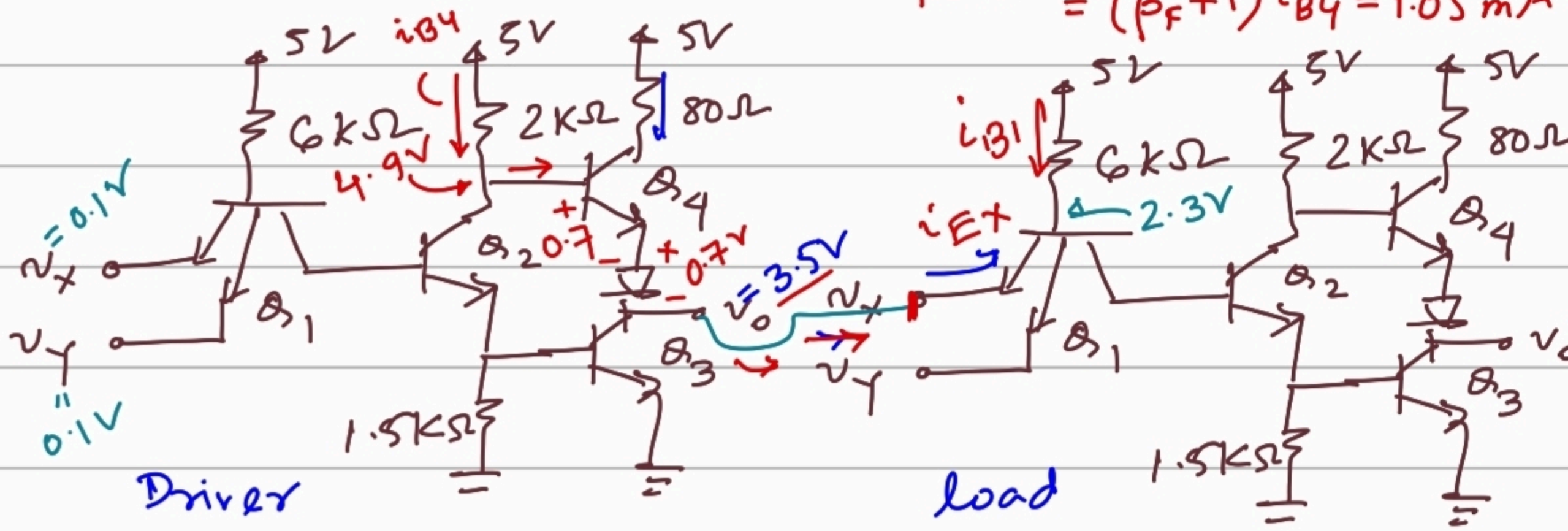
$= 3.5\,V$

Driver side: $Q_1 \to$ sat, $Q_2, Q_3 \to$ cutoff, Q_4 - F.A.

Load side: $Q_1 \to$ Reverse active, $Q_2, Q_3 \to$ sat. $Q_4 \to$ cutoff

$i_{B4} = \frac{5-4.9}{2K} = 0.05\,mA$, supply current $= i_{E4}$

$= (\beta_F + 1) i_{B4} = 1.05\,mA$



individual demand current $= i_{EX} = \beta_R \times i_{B1}$

$= 0.1 \times \frac{(5-2.3)}{6}$

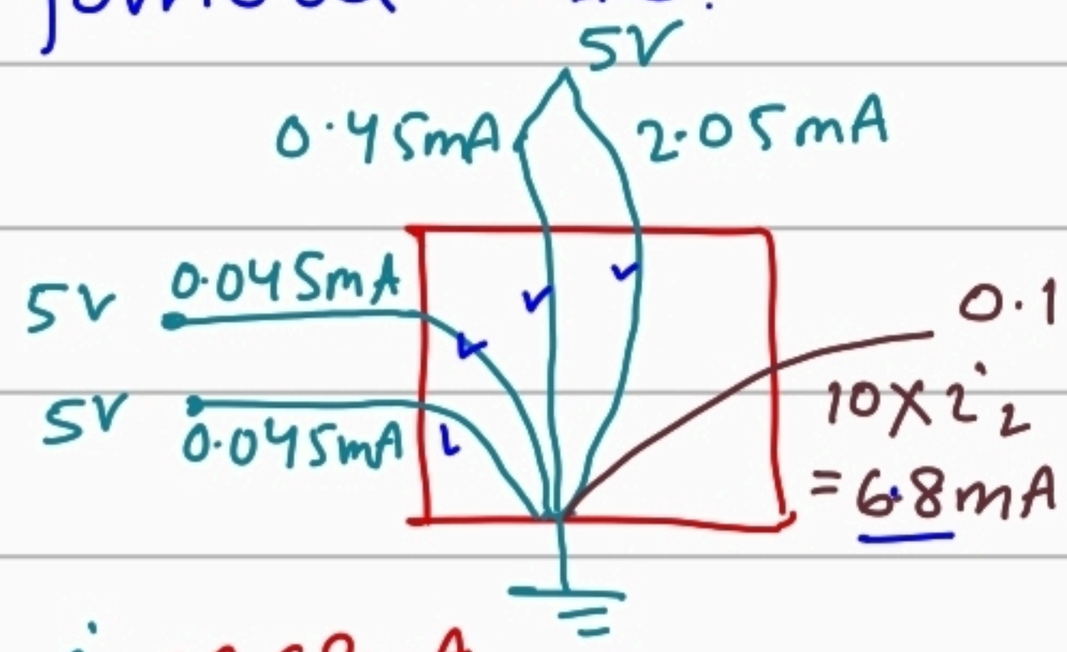
$= 0.045\ mA$

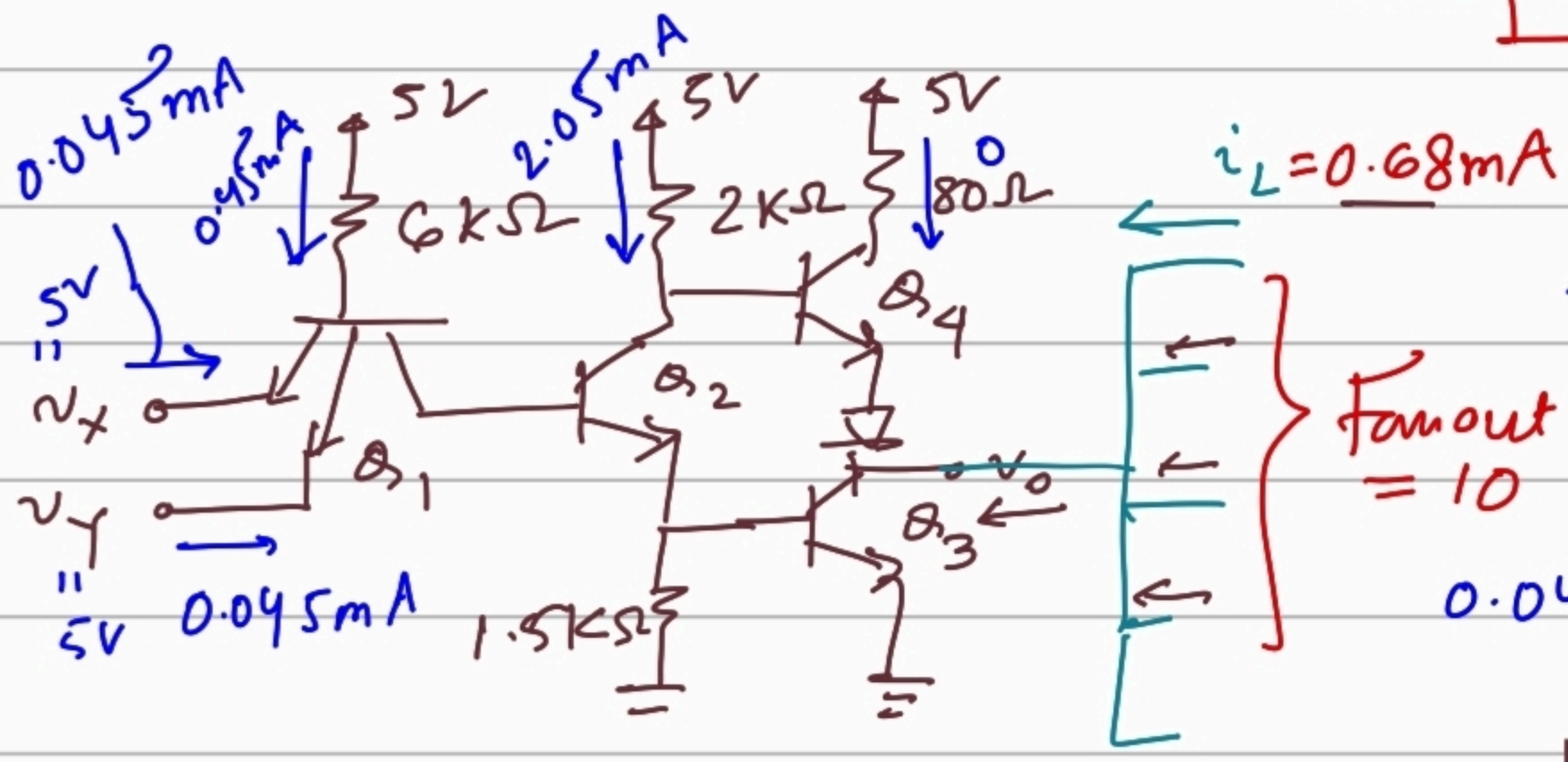
maximum fanout for this case $= \left\lfloor \frac{1.05}{0.045} \right\rfloor = \boxed{23}$

Total max fanout $= \min(23, 60) = 23.$

Power dissipation in driver circuit given the number of fanout = 10.

@ Case ① : $v_X = v_Y = 5V$

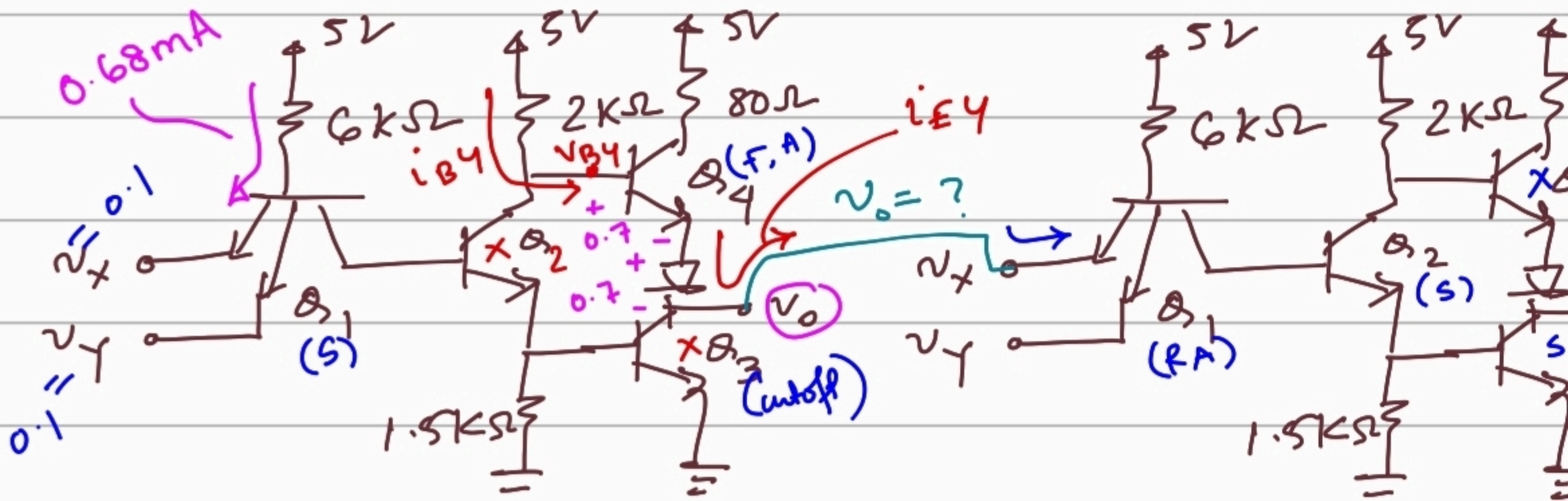




$P_{tot} = (5-0) \times (0.45 + 2.05 + 0.045 \times 2) + (0.1 - 0) \times 6.8$

$= \boxed{13.63\ mW}$

Case ② $v_X = v_Y = 0.1V$



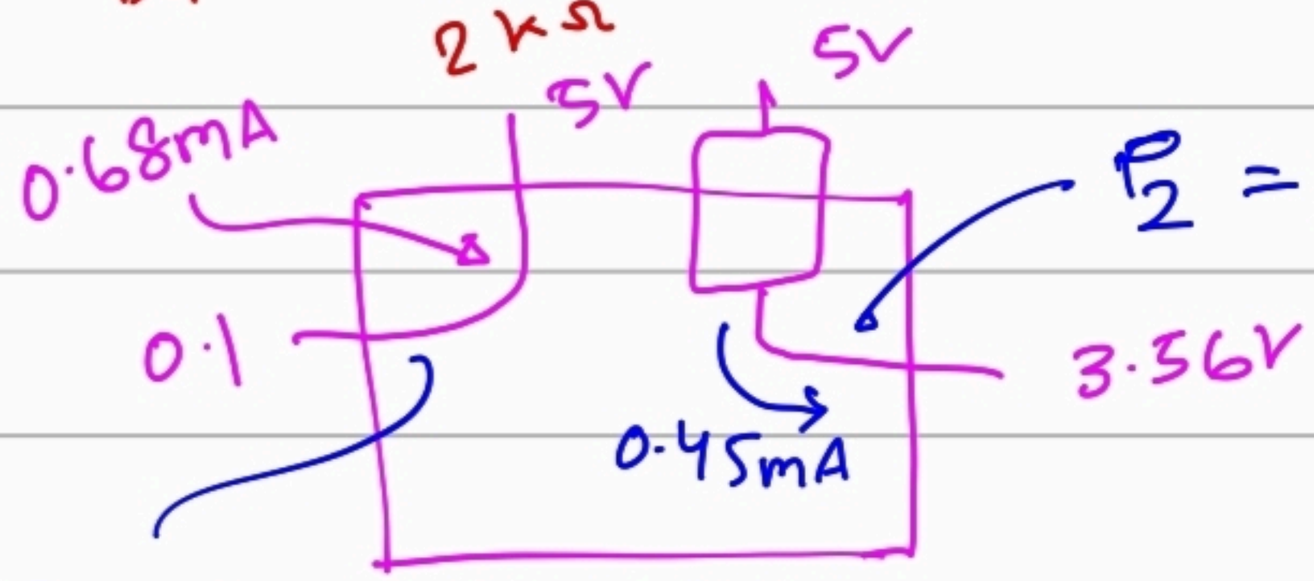
i_{EX} = individual demand = 0.045 mA

total demand = 10 × 0.045 = 0.45 mA = i_{E4}

$i_{B4} = i_{E4}/(\beta_F+1) = \frac{0.45}{21} = 0.02$ mA

$i_{B4} = \frac{5 - V_{B4}}{2\,k\Omega} \Rightarrow V_{B4} = 4.96$ V. $v_o = (4.96 - 1.4)$

$= 3.56$ V.



$P_2 = (5 - 3.56) \times 0.45$

$P_{tot} = P_1 + P_2$

$= \boxed{3.94 \text{ mW}}$

$P_1 = (5 - 0.1) \times 0.68$

Homework. 4.3 Modified Totem Pole (Bonus)

BUX video

Recommended problem (Mid syllabus ends here)

Neaman's book: Chapter 17. (DTL, TTL)

17.20, 17.21, 17.23, 17.25, 17.28, 17.32

(Mid/Final)

Emitter Coupled Logic
ECL logic family

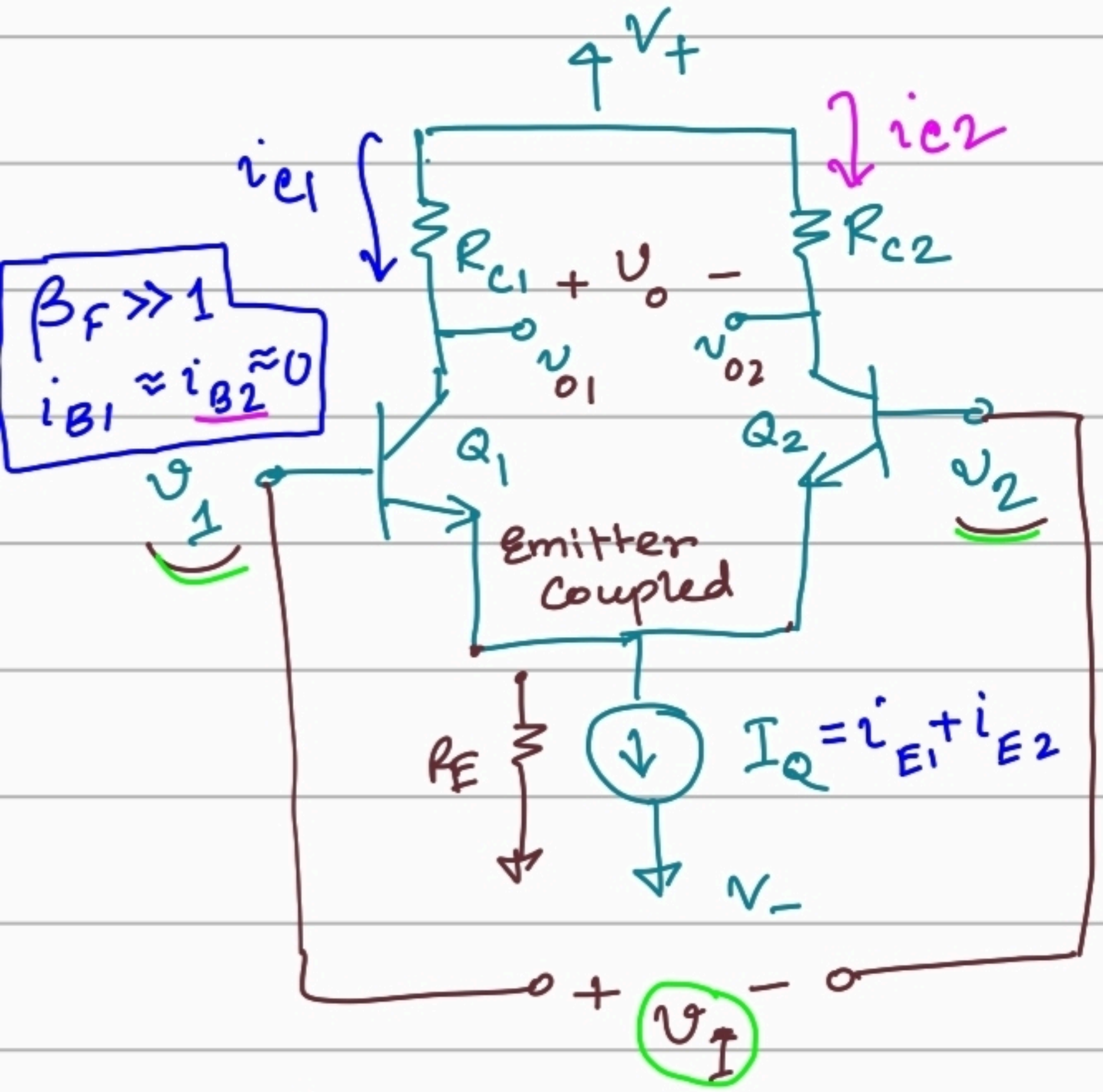
→ Bipolar → Unsaturated logic family

The logic transistors would operate in forward active or cutoff mode.

The transistors will not saturate. Hence, the storage time would be lower and switching time would be

faster.

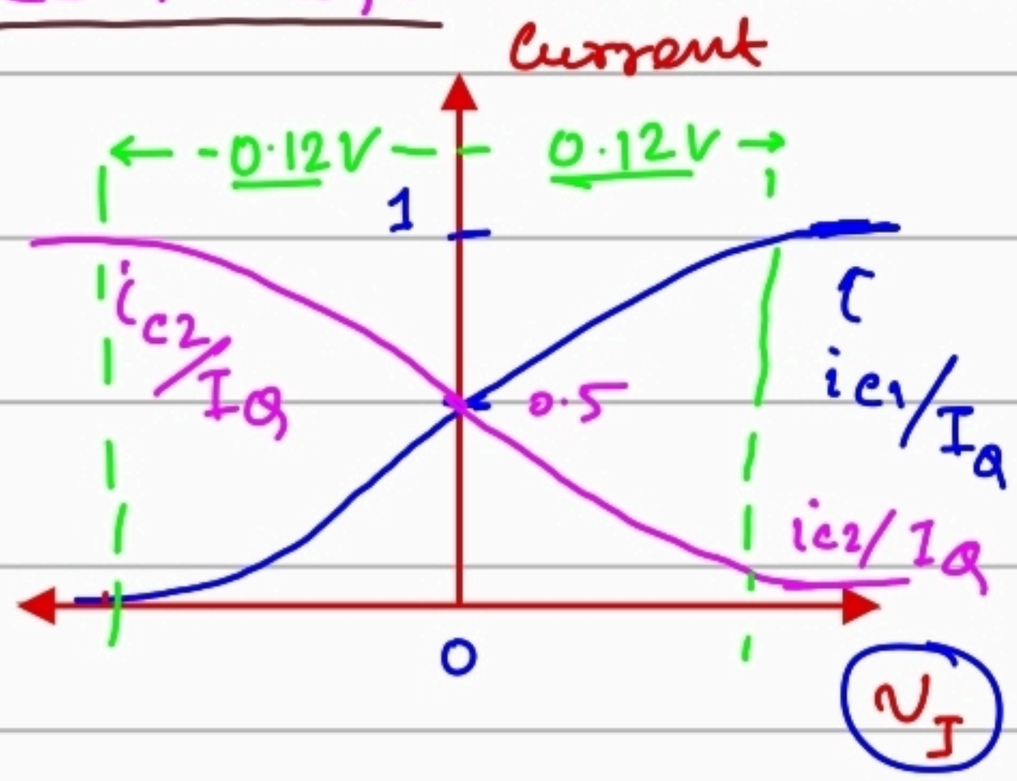
Basic Differential Amplifier:



$v_I = v_1 - v_2$

$v_o = v_{o1} - v_{o2}$

Qualitative description of dc transfer characteristic



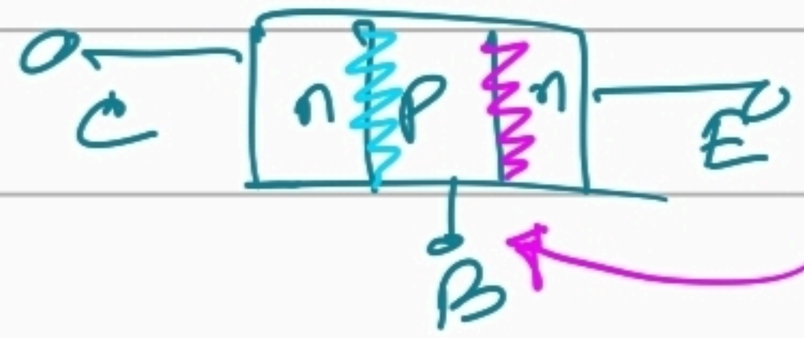
* $\begin{pmatrix} v_1 \gg v_2 \\ v_I \gg 1 \end{pmatrix}$. $Q_1 \to$ ON (F.A.). $Q_2 \to$ OFF. $i_{C1} \approx i_{E1} \approx I_Q$

  $i_{C2} \approx i_{E2}$, $i_{C1} + i_{C2} = I_Q \Rightarrow i_{C2} \approx 0$

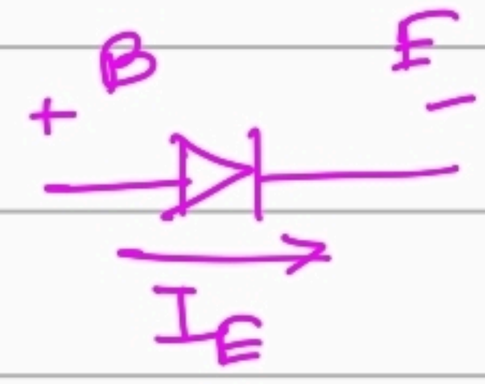
* $(v_1 \ll v_2)$ $Q_1 \to$ OFF, $Q_2 \to$ ON (F.A). $i_{C2} \approx i_{E2} \approx I_Q$

  $i_{C1} \approx i_{E1} \approx 0$ $[\because i_{C1} + i_{C2} = I_Q]$

Remarks: The coupled emitter causes the total emitter current $i_{E1} + i_{E2}$ to be constant. Also the high value of β_F is responsible for negligible amount of base current. So for ECL circuits we are going to ignore base currents and would take collector currents equal to emitter current if nothing mentioned in question.



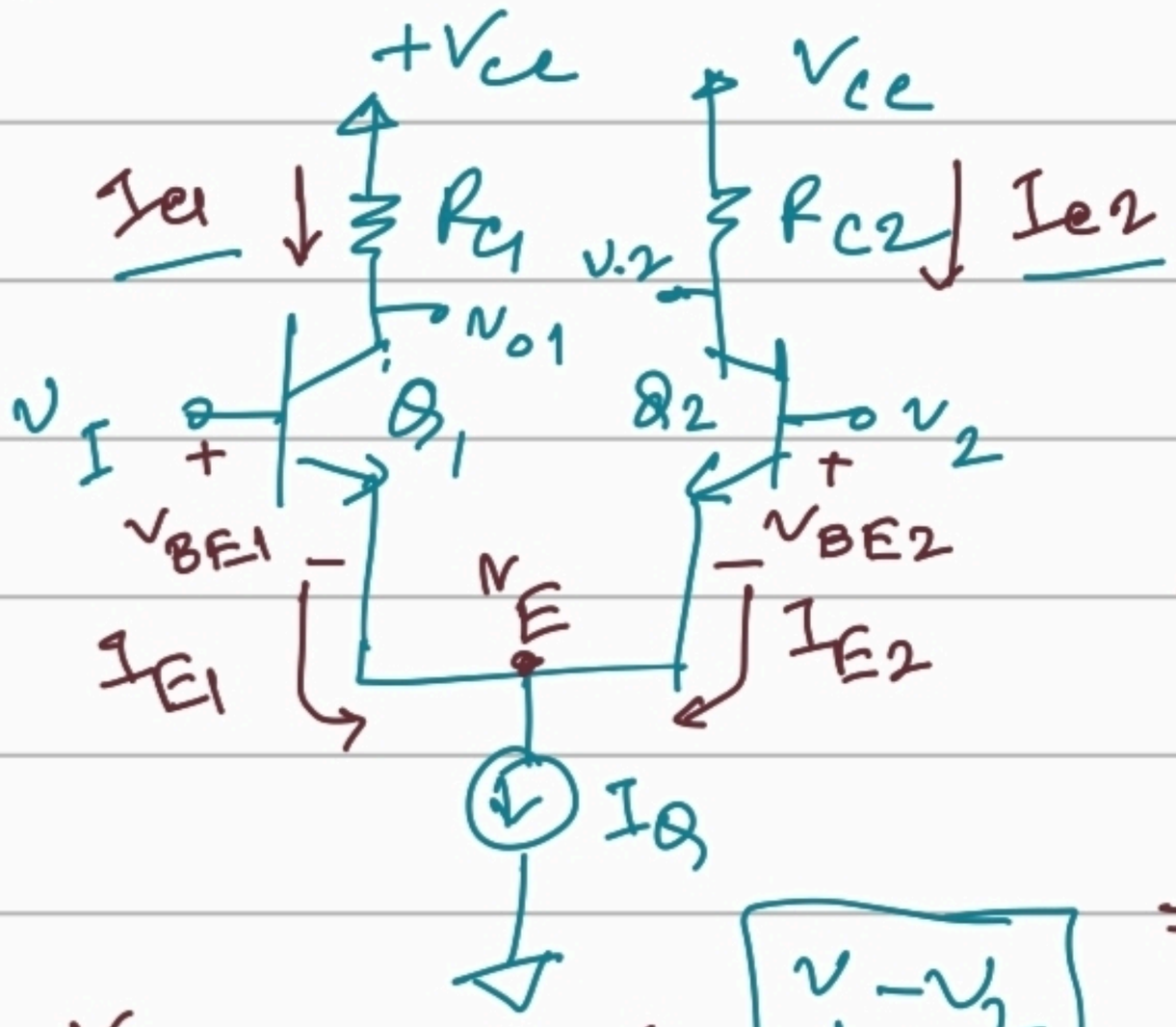
base emitter junction is at forward bias in forward active mode.



$$I_E = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

I_S = reverse saturation current $\sim 10^{-9}/10^{-10}$ A

$\boxed{V_T = \text{thermal voltage} = 0.0259\,V}$ [T = 300K]



$$\frac{I_{E1}}{I_{E2}} = \frac{I_S \exp\left(\frac{V_{BE1}}{V_T}\right)}{I_S \exp\left(\frac{V_{BE2}}{V_T}\right)}$$

$$\Rightarrow \frac{I_{E1}}{I_{E2}} = \exp\left(\frac{V_{BE1} - V_{BE2}}{V_T}\right)$$

$$V_{BE1} = v_1 - V_E$$
$$V_{BE2} = v_2 - V_E$$

$$\boxed{v_1 - v_2 = v_I}$$

$$\Rightarrow \frac{I_{E1}}{I_{E2}} = \exp\left(\frac{v_1 - v_2}{V_T}\right)$$

$$\Rightarrow \frac{I_{C1}}{I_{C2}} = \exp\left(\frac{v_I}{V_T}\right) \quad [I_B \approx 0$$

∴ Suppose, $I_{C1} \approx 100\, I_{C2}$, then

$$100 \approx \exp\left(\frac{V_I}{0.0259}\right) \Rightarrow V_I = 0.12\,V$$

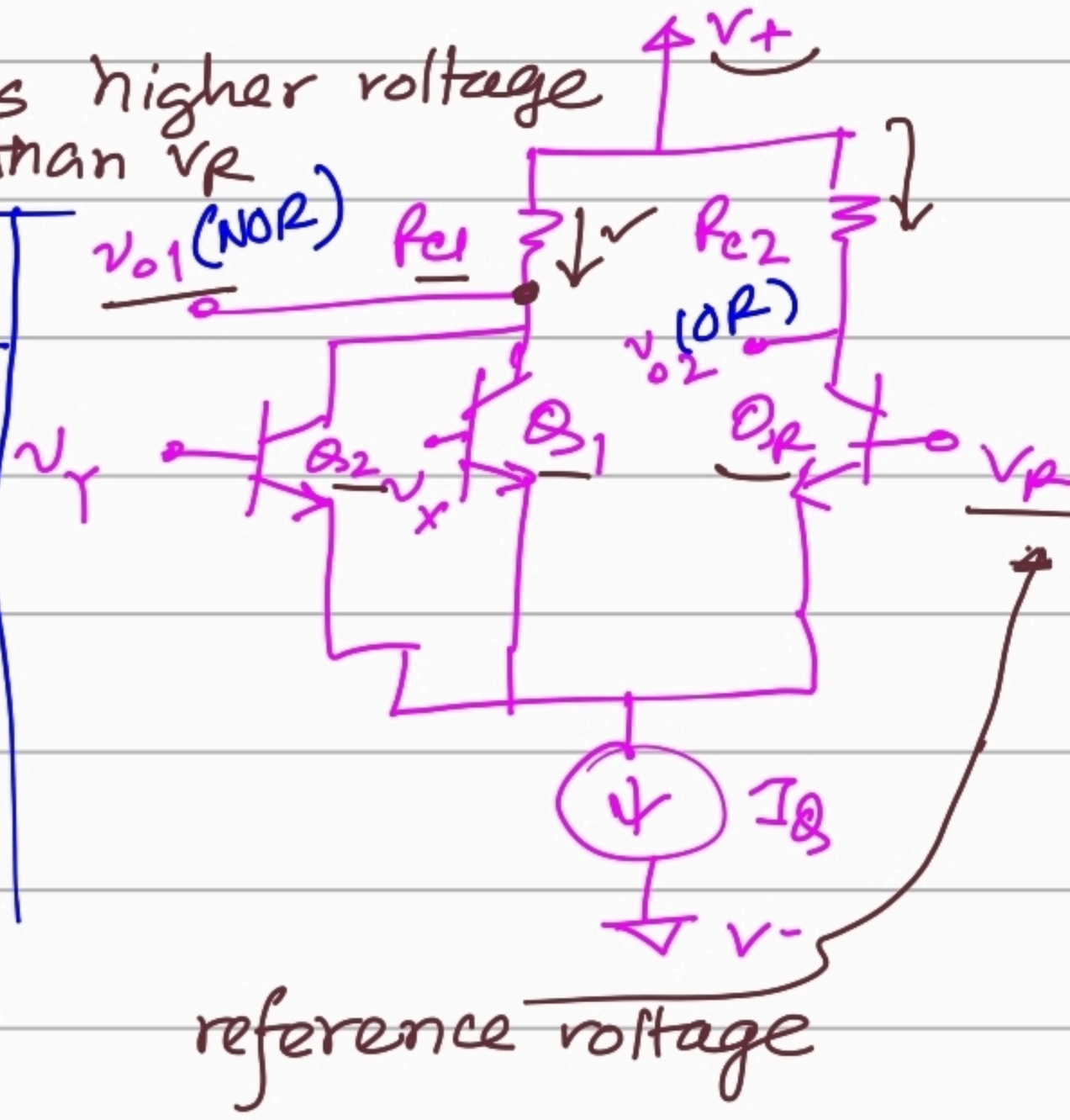
Because, $I_{E1} + I_{E2} = I_{C1} + I_{C2} = I_Q$, we can tell if $v_I > 0.12V$ we have $I_{C1} \approx I_Q$ and $I_{C2} \approx 0$.

Basic NOR gate operation:

logical high voltage means higher voltage than V_R

v_X	v_Y	Q_1	Q_2	Q_R	v_{o1}	v_{o2}
L	L	C	C	FA	H	L
L	H	C	FA	C	L	H
H	L	FA	C	C	L	H
H	H	FA	FA	C	L	H

V_x V_y NOR OR

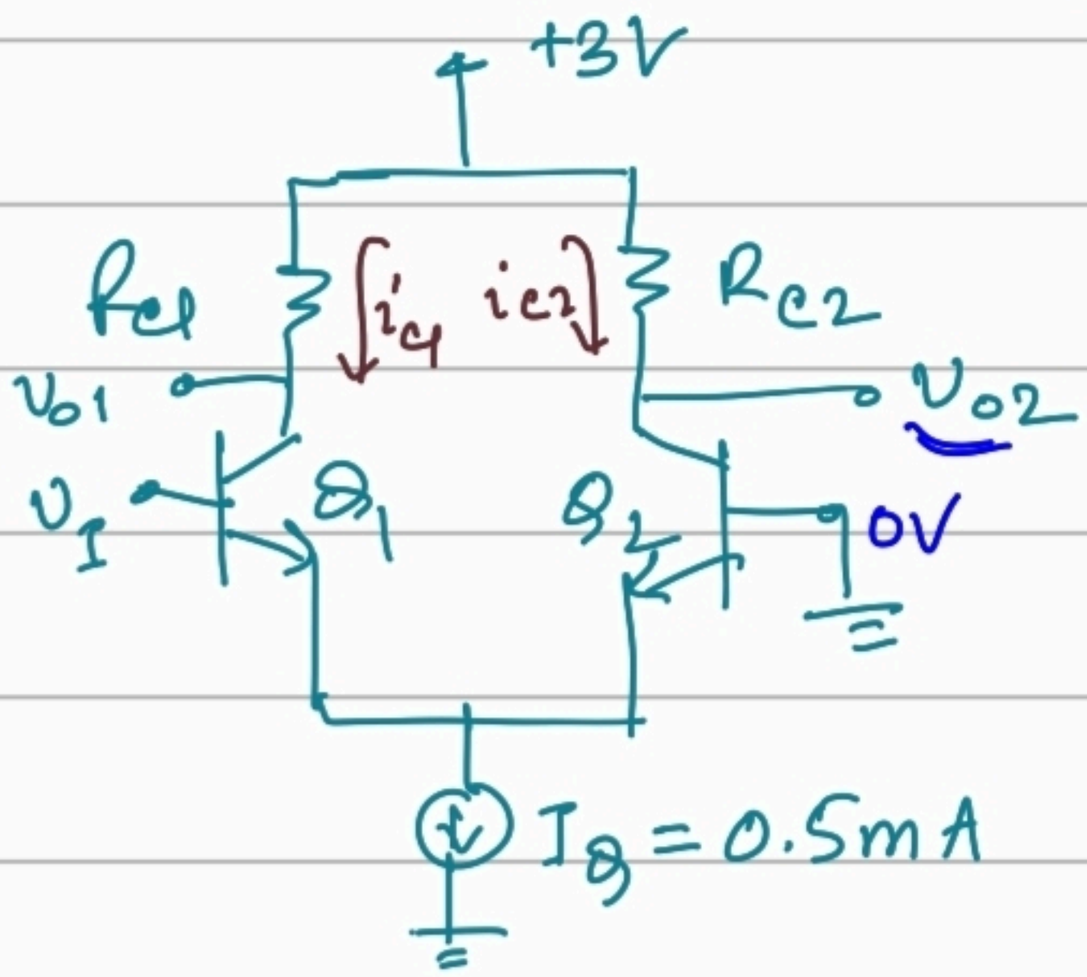


Neamen's 17.31 Neglect the base current for the following circuit.

(a) Determine the value of R_{c2} such that the minimum value of $v_{o2} = 0$.

(b) Determine the value of R_{c1} such that $v_{o1} = 1V$ and $v_I = 1V$.

(c) Determine the value of v_I so $i_{c1} = 0.40mA$ and $i_{c2} = 0.1mA$.



(a) we can achieve minimum voltage v_{o2} if current flows through R_{c2} resistor and voltage drops from 3V to given minimum value 0V.

maximum value of $i_{c2} = I_Q$

$$i_{c2} = \frac{3-0}{R_{c2}} \Rightarrow \boxed{R_{c2} = 3/0.5 = 6k\Omega}$$

We have to turn on Q_2 to make this happen.

(b) When $v_I = 1V > 0V$. $Q_1 \rightarrow$ F.A and $Q_2 \rightarrow$ cutoff. $i_{c2} \approx 0mA$ and $i_{c1} \approx 0.5mA$.

Therefore, $i_{c1} = 0.5mA = \frac{(3 - v_{o1})}{R_{c1}} = \frac{3-1}{R_{c1}}$

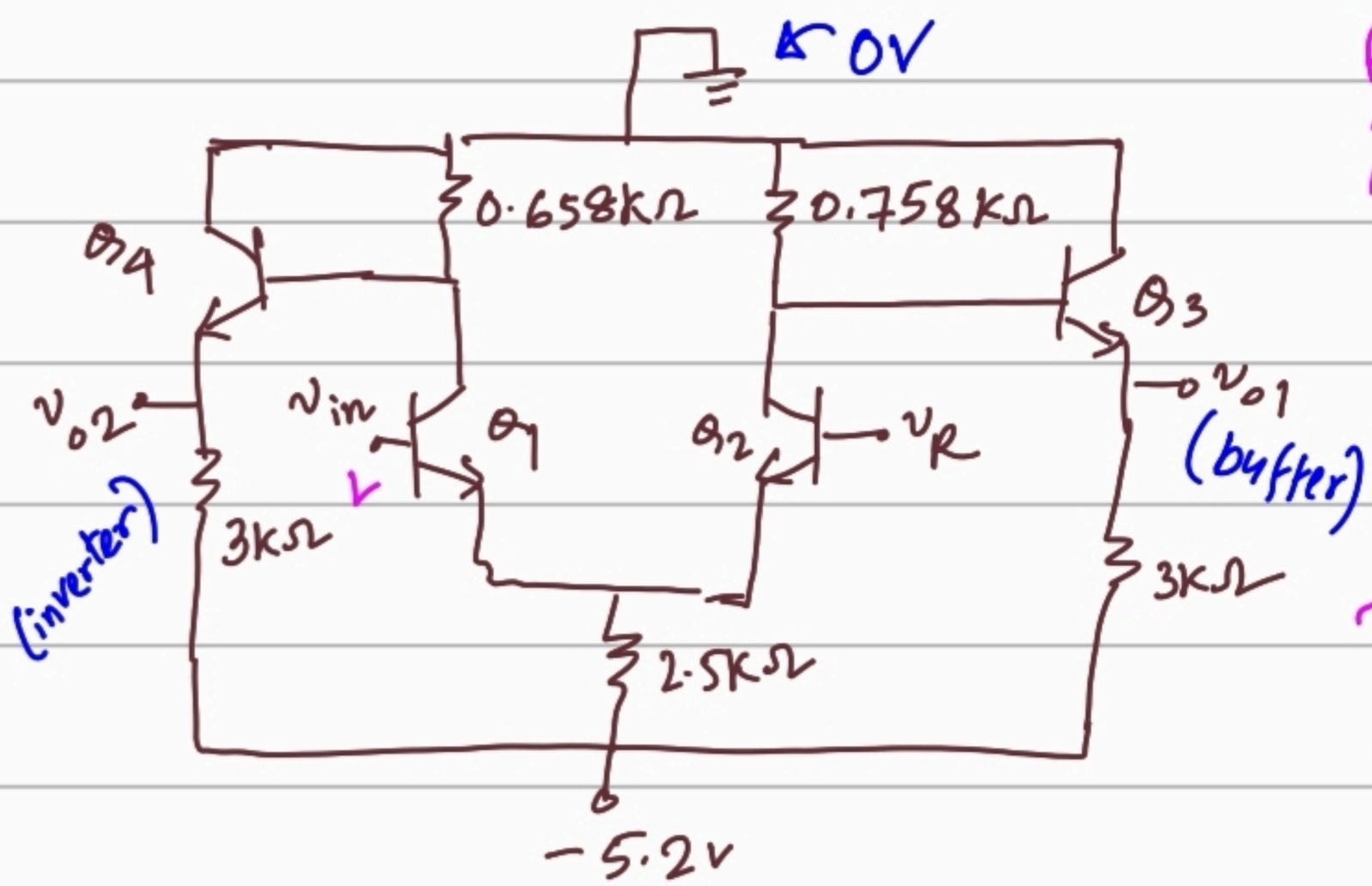
$\therefore \boxed{R_{c1} = 4k\Omega}$

(c) $\frac{i_{c1}}{i_{c2}} = \frac{0.1}{0.4} = \exp\left(\frac{V_{BE1} - V_{BE2}}{V_T}\right) = \exp\left(\frac{V_I - 0}{V_T}\right)$

$\Rightarrow V_I = V_T \ln\left(\frac{0.1}{0.4}\right) = 0.0259 \ln(1/4)$

$\boxed{V_I = -0.0359V}$

Q:# Find the logical low voltage and logical high voltage for the following ECL inverter.



Rule of thumb:
For ECL circuits logical output high/low voltages can be taken as logical input high/low.

	v_{in}	v_R	Q_1	Q_2	v_{o1}	v_{o2}
→	Low -1.7V	-1.35	Cutoff	F.A.	Low -1.7V	High -0.7
→	High -0.7	-1.35	F.A.	Cutoff	High -0.7	Low. -1.7V

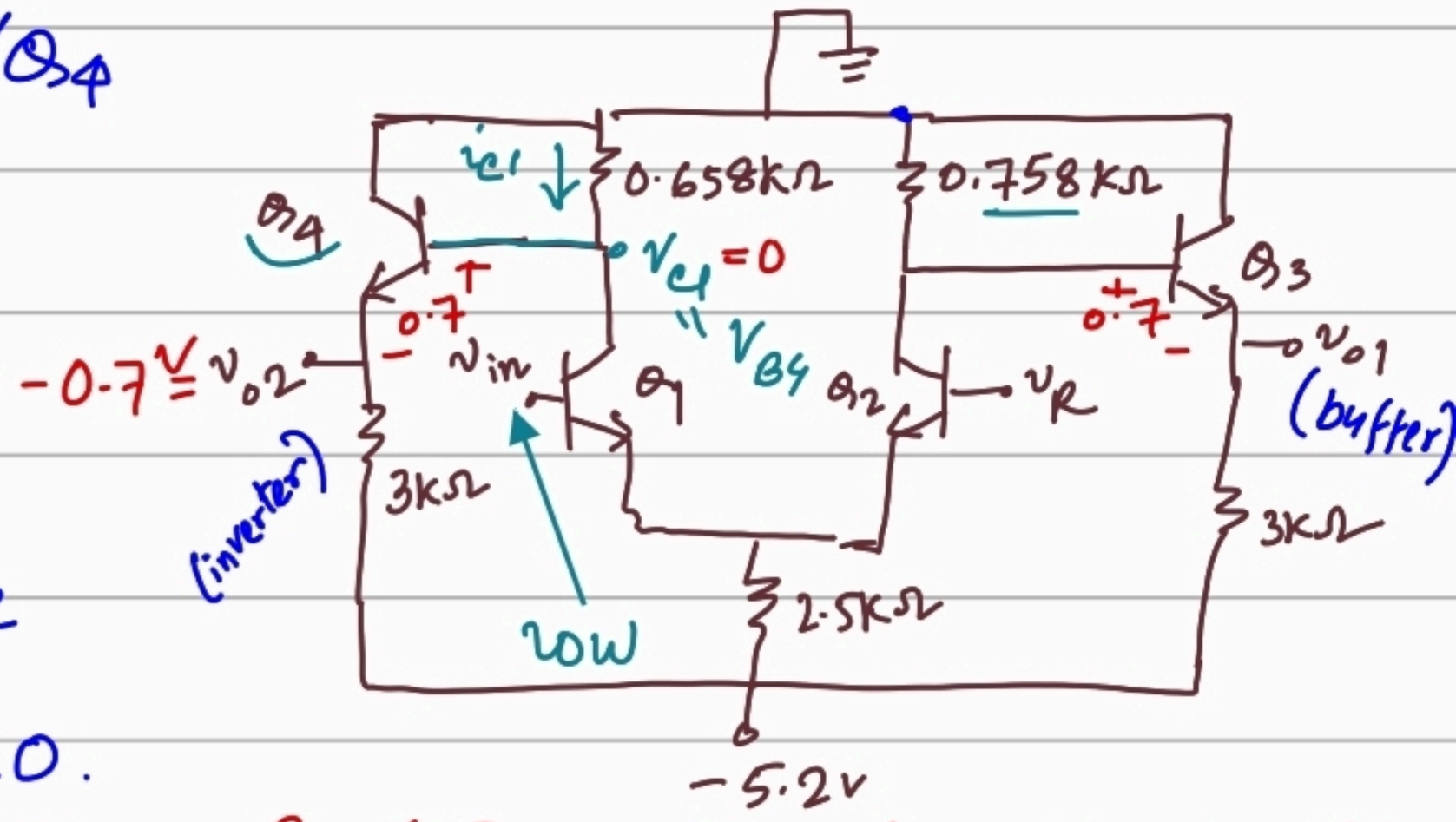
logical low voltage must be lower than v_R.

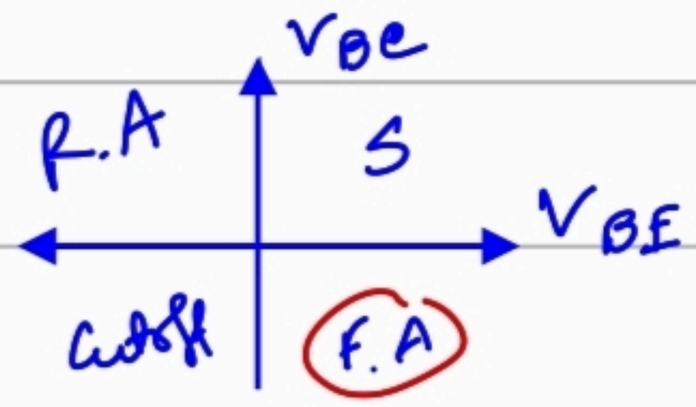
(a) If v_{in} is low voltage. $Q_1 \rightarrow$ cutoff, $Q_2 \rightarrow$ F.A.

$i_{c1} = 0\,mA$. $V_{c1} = 0V$.

<u>Observation</u>: Q_3/Q_4 transistors have higher value of collector voltage than base voltage

$V_B < V_C \Rightarrow V_{BC} < 0$.





Thus Q_3/Q_4 will always operate in forward active mode regardless of input voltage.

Because of this we get $V_{BE4} = 0.7V$.

$\underline{V_{B4}} - V_{E4} = 0.7V \Rightarrow V_{E4} = V_{o2} = -0.7V$

(0V)

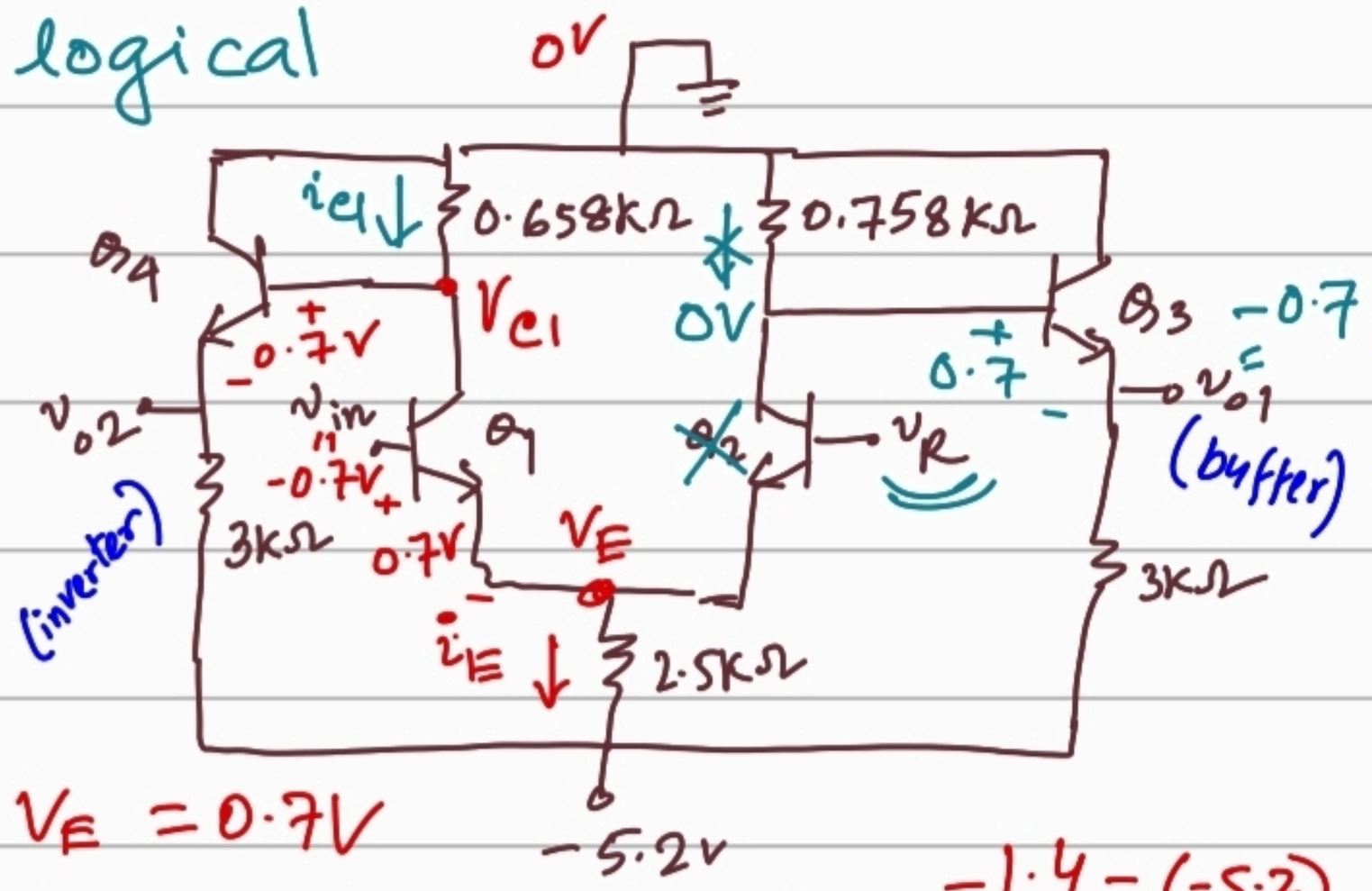
This implies logical high output/input voltage is $\boxed{-0.7V.}$

(b) If $v_{in} = -0.7V$ or logical high voltage. then

Q_1 Forward active,

Q_2 is in cutoff.

$v_{o2} \rightarrow$ <u>logical low</u>.



$V_{BE1} = 0.7V \Rightarrow v_{in} - V_E = 0.7V$

$\Rightarrow -0.7 - V_E = 0.7V \Rightarrow V_E = -1.4V$. $\therefore i_E = \dfrac{-1.4-(-5.2)}{2.5K}$

$i_E = 1.52\,mA$

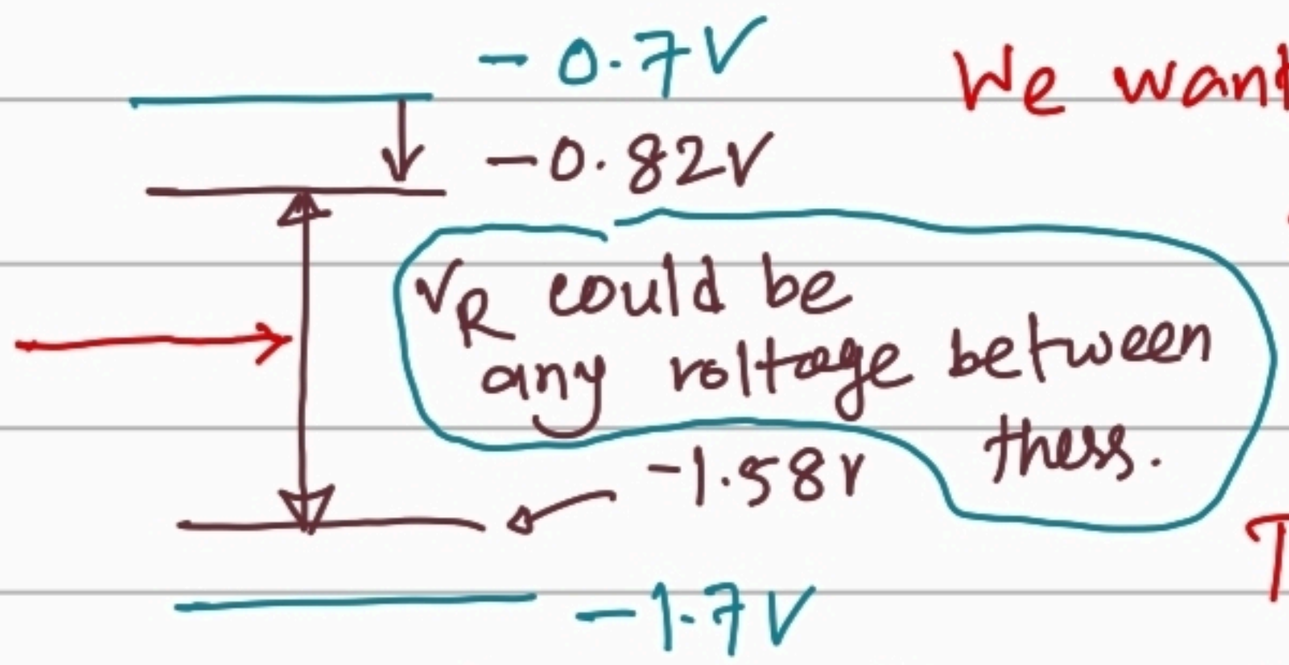
$i_{C1} = i_E \Rightarrow \frac{0 - V_{C1}}{0.658k} = 1.52m \Rightarrow V_{C1} = -1V.$

Again Q_4 is in forward active mode.

$V_{BE4} = 0.7V \Rightarrow V_{o2} = -1 - 0.7V = -1.7V$

Finally, we get logical low voltage is $-1.7V$.

(c) V_R should in between $-0.7V$ and $-1.7V$



We want to allow the symmetric variation between logical high and low voltage.

Thus, we choose reference voltage, $V_R = \frac{\text{logical high} + \text{logical low}}{2}$

$= \frac{-0.7 - 1.7}{2} = -1.35V$

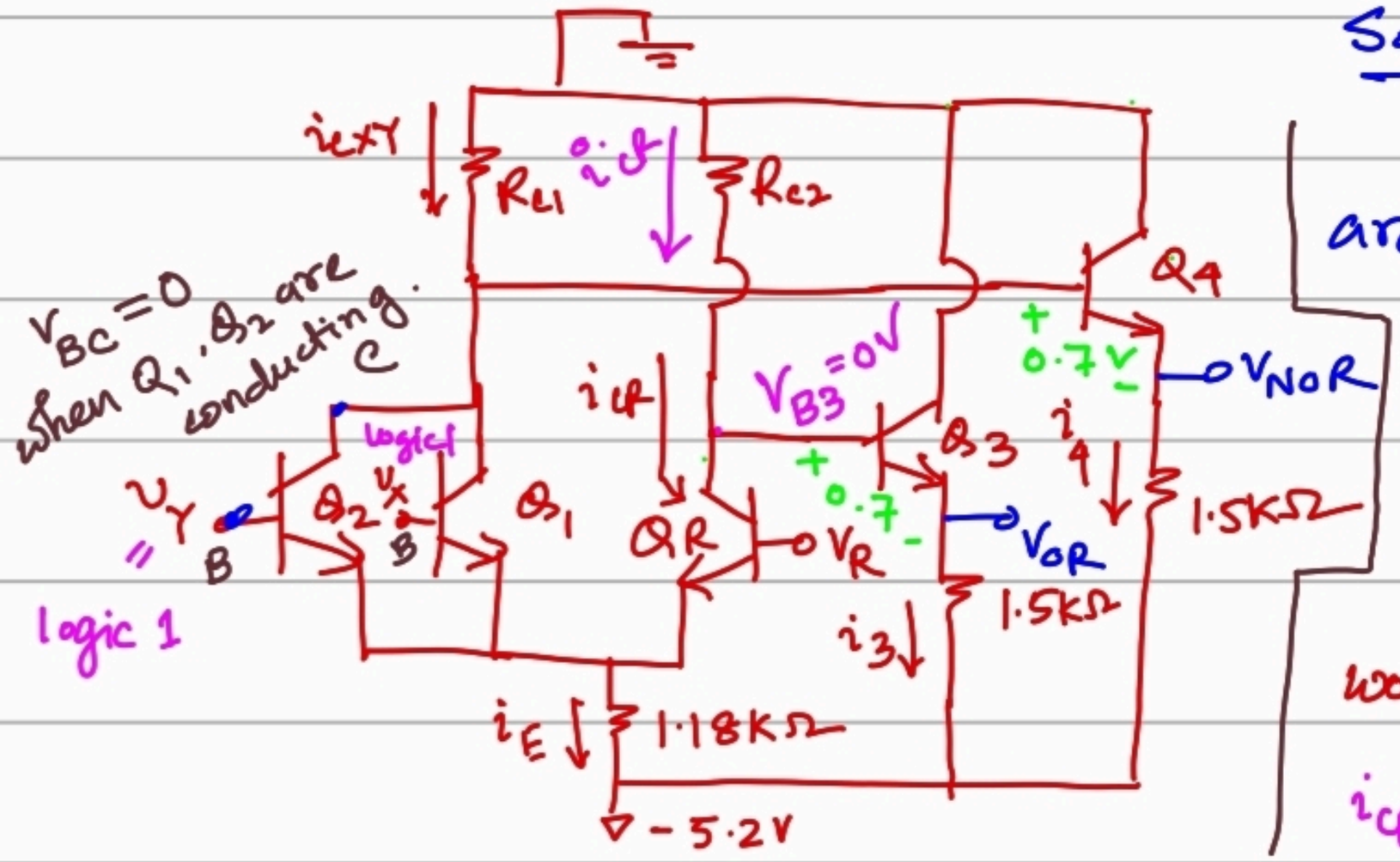
$$\boxed{V_R = -1.35V}$$

Lecture 11: ECL circuit reference circuit design, Power dissipation, fanout calculation.

Example: 17.2

Calculate current, resistor and logic 0 values in the basic ECL circuit.

Determine R_{C1} and R_{C2} such that when Q_1 and Q_2 are conducting, the B-C voltages are zero.



Solution:

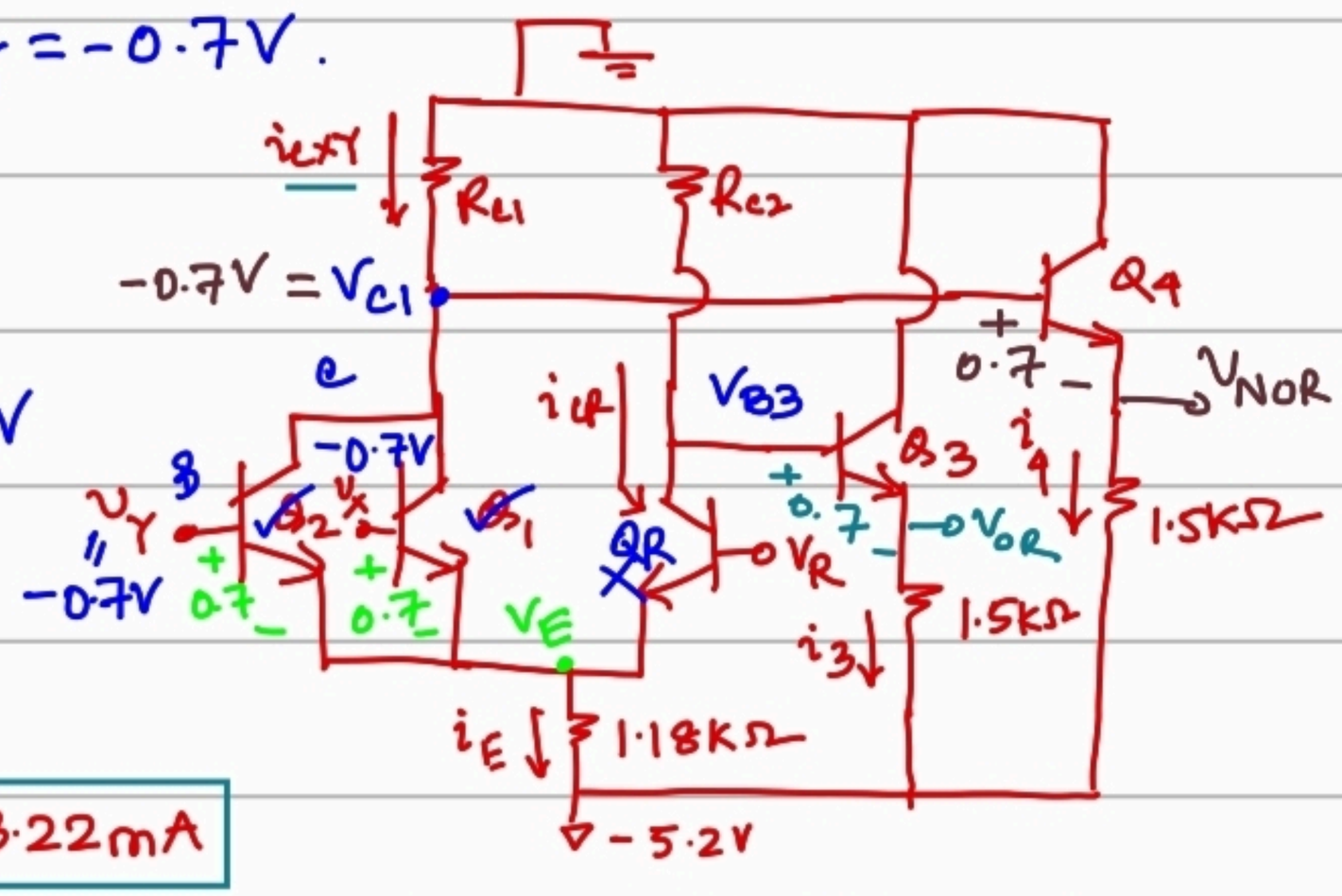
Suppose v_X and v_Y are logical high, then Q_1, Q_2 would turn on. Therefore, $V_{BC} = 0V$.

Now Q_R transistor would be in cutoff and $i_{CR} = 0\,mA$. So $V_{B3} = 0V$.

Remark: Q_3 and Q_4 will always operate in forward active mode because collector voltage is higher than base voltage.

Now $V_{OR} = V_{E3} = V_{B3} - V_{BE3} = -0.7V$ = logical high voltage

So we can write $v_X = v_Y = -0.7V$.



By imposing the condition $V_{BC} = 0V$, we can find $V_{C1} = V_X = V_{B1} = -0.7V$

Because Q_1, Q_2 are in F.A.

$v_E = -0.7 - 0.7 = -1.4V$

Thus, $\boxed{i_E} = \dfrac{-1.4-(-5.2)}{1.18K} = \boxed{3.22mA}$

So because Q_1 and Q_2 are ON, all current through v_E node would go through R_{C1} resistor. $\boxed{i_{CXY} = i_E = 3.22mA}$

Thus, $R_{C1} = \dfrac{0-(-0.7)}{3.22m} = 0.217\,K\Omega$

Since, $v_X = v_Y$ = logical high $= -0.7$, we get, v_{NOR} = logical low $= -1.4V$

$\boxed{\text{Logical 0 value} = -1.4V}$

$\boxed{i_4} = \dfrac{-1.4-(-5.2)}{1.5k} = \boxed{2.53\,mA}$, $\boxed{i_3} = \dfrac{-0.7-(-5.2)}{1.5K} = \boxed{3mA}$

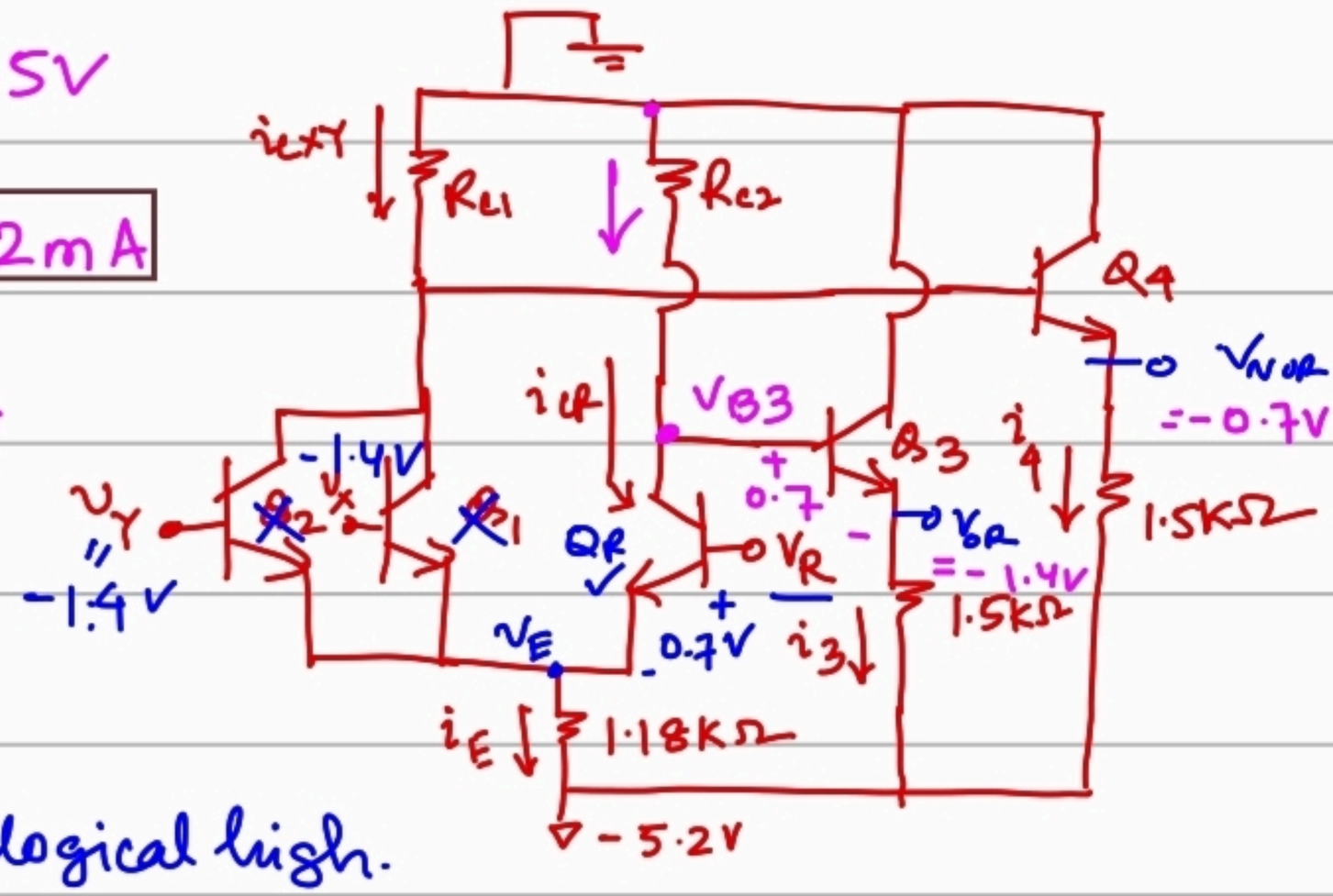
In order to calculate R_{C2}, we need to turn ON Q_R

transistor. Hence we need to put logical 0 to both v_X and v_Y. $v_R = \frac{\text{logical high} + \text{logical low}}{2} = -1.05\,V$.

Now Q_1 and Q_2 are in cutoff but Q_R is in forward active.

So $v_E = -1.05 - 0.7 = -1.75V$

$i_E = \frac{-1.75-(-5.2)}{1.18k\Omega} = \boxed{2.92mA}$



Because, Q_R is ON. $i_{cR} = i_E$

$\boxed{i_{cR} = 2.92mA}$, $\boxed{i_{cXY} = 0mA}$

As. $v_X = v_Y =$ logical low,

$v_{OR} =$ logical low and $v_{NOR} =$ logical high.

$\therefore v_{OR} = -1.4V$ and $v_{B3} = -1.4-(-0.7) = -0.7V$ [$Q_3 \rightarrow$ F.A]

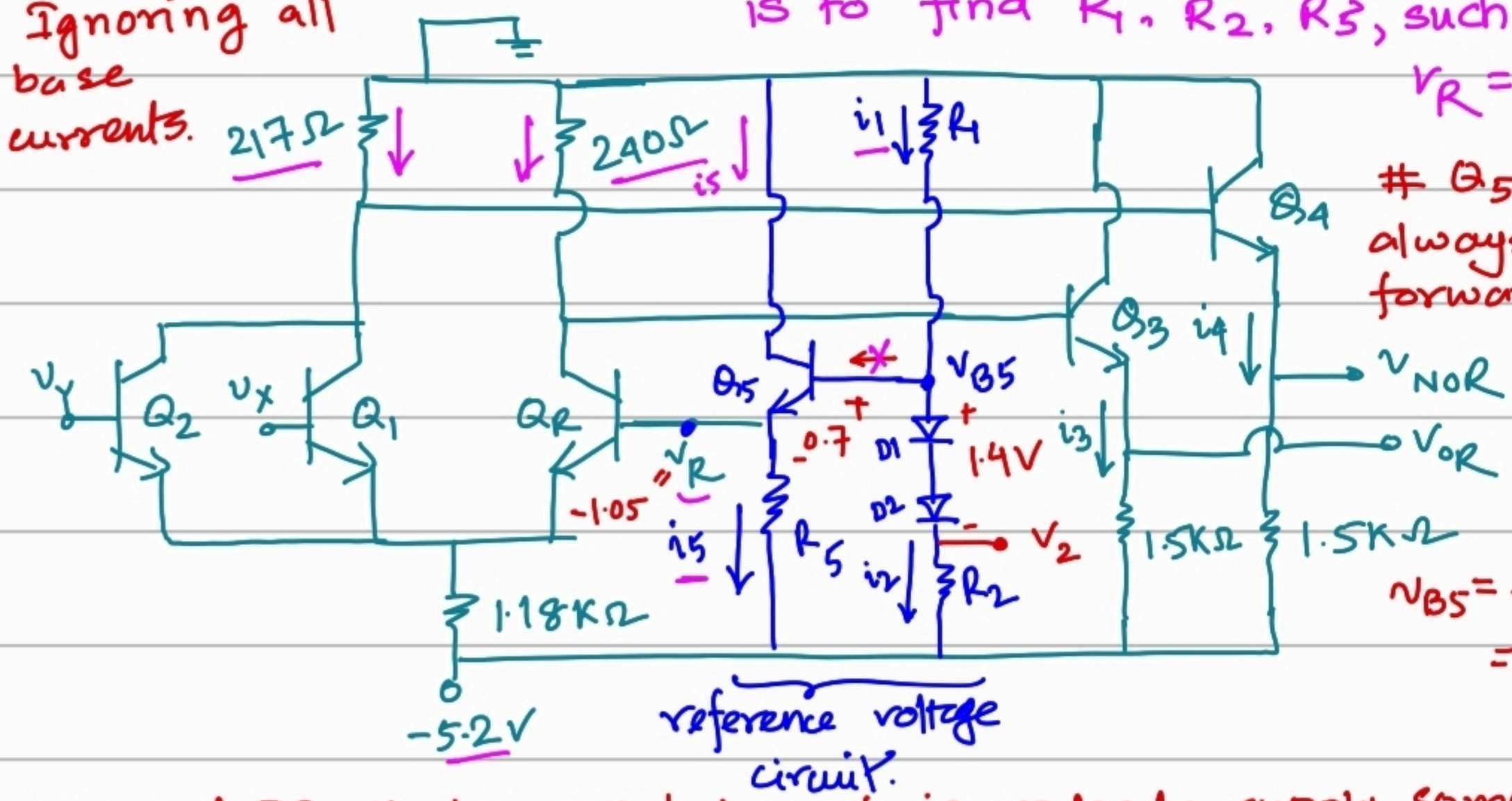
Finally. $R_{C2} = \frac{0-(-0.7)}{2.92m} = \boxed{0.24k\Omega}$. $\boxed{i_4 = 3mA,\ i_3 = 2.53mA}$

Reference voltage generation circuit design

Design the reference portion of the ECL circuit. $V_R = -1.05V$.

In this design problem our goal is to find R_1, R_2, R_3, such that $V_R = -1.05V$.

Ignoring all base currents.



Q_5 will always be in forward active mode.

$v_{B5} = -1.05 + 0.7 = -0.35V$

D1 and D2 diodes must be ON. in order to supply some base current in Q_5. So $V_2 = -0.35 - 1.4V = -1.75V$

Suppose, we choose $\boxed{R_1 = 250\Omega}$. $i_1 = \frac{0-(-0.35)}{.25K\Omega} = \boxed{1.4mA}$

$i_1 \approx i_2 = 1.4mA$. Thus, $R_2 = \frac{-1.75-(-5.2)}{1.4m} = \boxed{2.46K\Omega}$

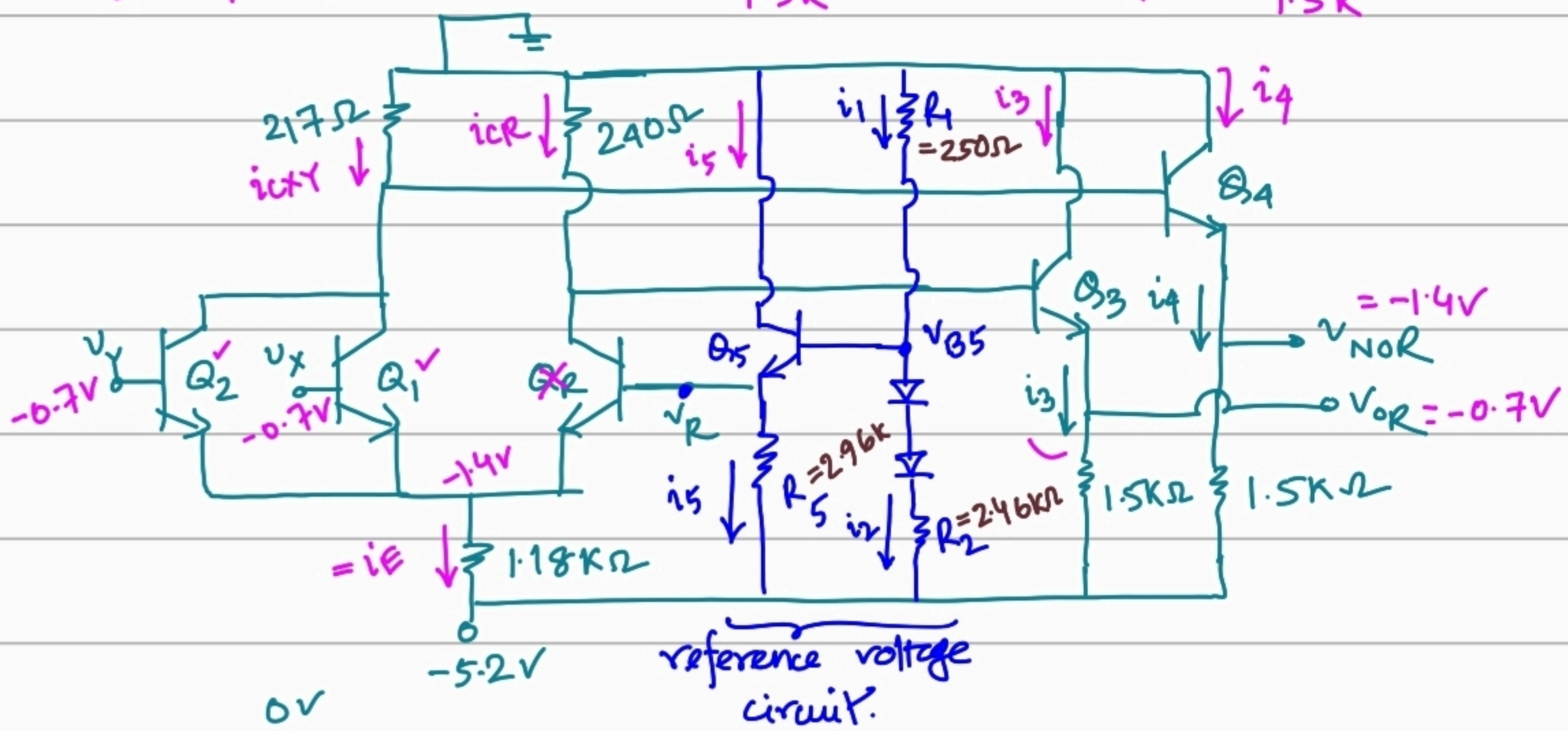
Next we choose, $\boxed{i_5 = i_1 = 1.4mA}$. $R_5 = \frac{-1.05-(-5.2)}{1.4m} = \boxed{2.96K}$

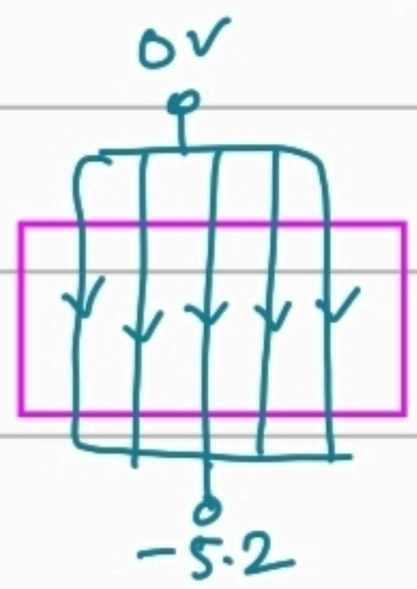
Power Dissipation Calculation:

Calculate the power dissipation when $v_X = v_Y = \text{logic } 1 = -0.7V$

$i_E = \frac{-1.4-(-5.2)}{1.18K} = 3.22mA = i_{CXY}$, $i_{CR} = 0mA$

$i_5 = i_1 = 1.4mA$, $i_3 = \frac{-0.7-(-5.2)}{1.5K} = 3mA$, $i_4 = \frac{-1.4-(-5.2)}{1.5K} = 2.53mA$





Finally total power dissipation is

$$P = (0-(-5.2))(i_{CXY} + i_{CR} + i_1 + i_5 + i_3 + i_4)$$

$$\boxed{P = 60.06\,mW}$$

Calculation of maximum fanout:

Example 17.5

Calculate the maximum fanout of an ECL logic gate, based on DC loading effect. ($\beta = 50$)

When output voltage reduces because of connecting new load circuit, we call it loading effect.

Assume, the logic 1 level at the OR output is allowed to decrease by 50 mV at most from −0.7V to −0.75V.

Sol^n: So we want to find maximum current that can be supplied to the load circuit. $v_{OR} = -0.75$ V. Now $Q_3 \rightarrow$ F.A.

So $v_{B3} = -0.05$V and $i_{B3} = \frac{0-(-0.05)}{0.24K} = 0.2083$ mA

$i_{E3} = (\beta+1)\, i_{B3}$

$= 10.625$ mA

$i_3 = \frac{-0.75-(-5.2)}{1.5K}$

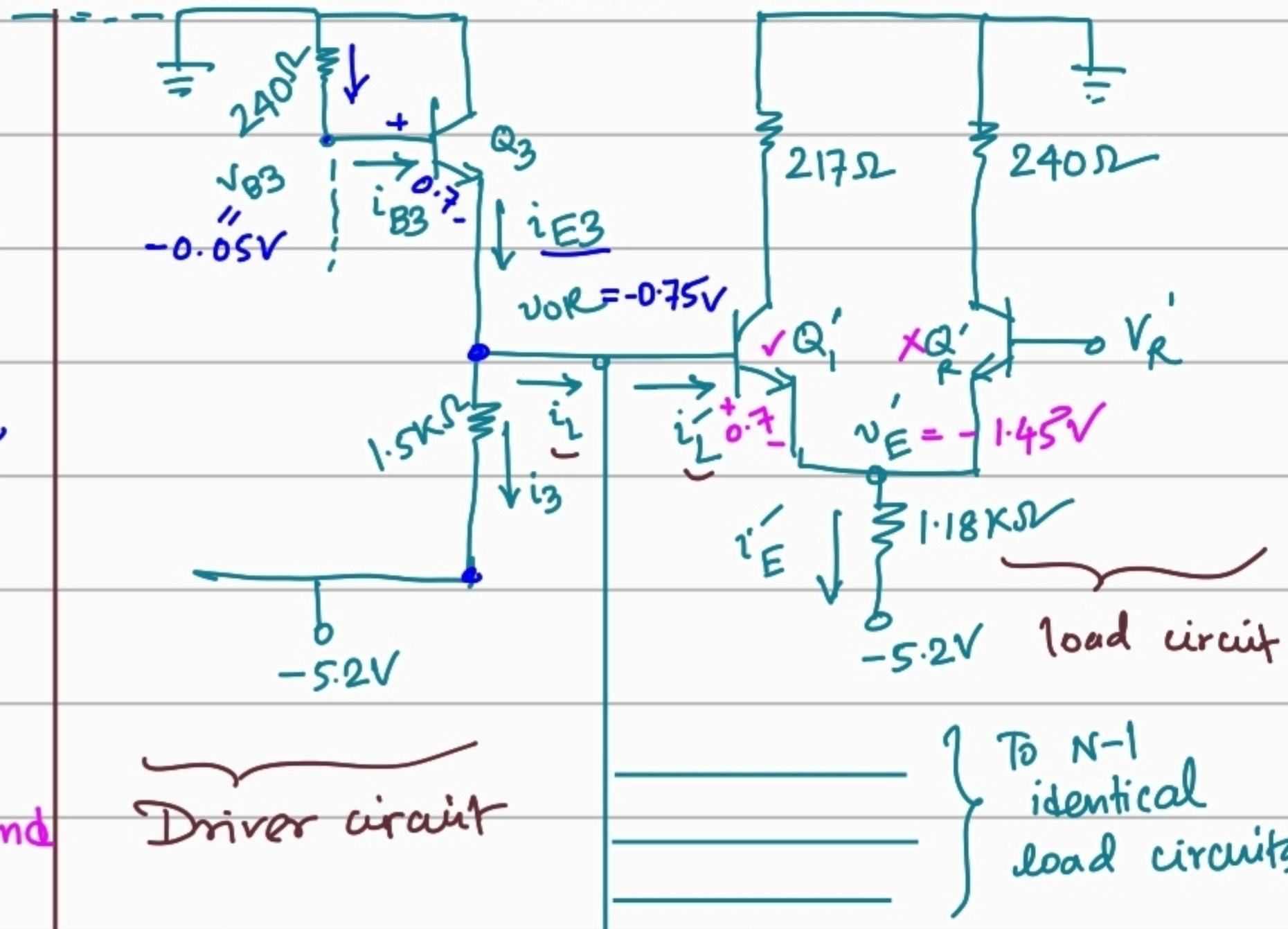
$= 2.967$ mA

i_L = supply current

$= i_{E3} - i_3$

$= 7.658$ mA

Now return to individual demand current.



$Q_1' \rightarrow$ F.A. so $v_E' = -1.45$ V. $i_E' = \frac{-1.45-(-5.2)}{1.18\,K\Omega} = 3.118$ mA

i_L' = base current of $Q_1' = \frac{i_E'}{(\beta+1)} = 0.06235$ mA

individual demand current = 0.06235 mA.

Finally, maximum fanout $= \frac{\text{supply current}}{\text{demand current}} = \left\lfloor \frac{7.658}{0.06235} \right\rfloor$

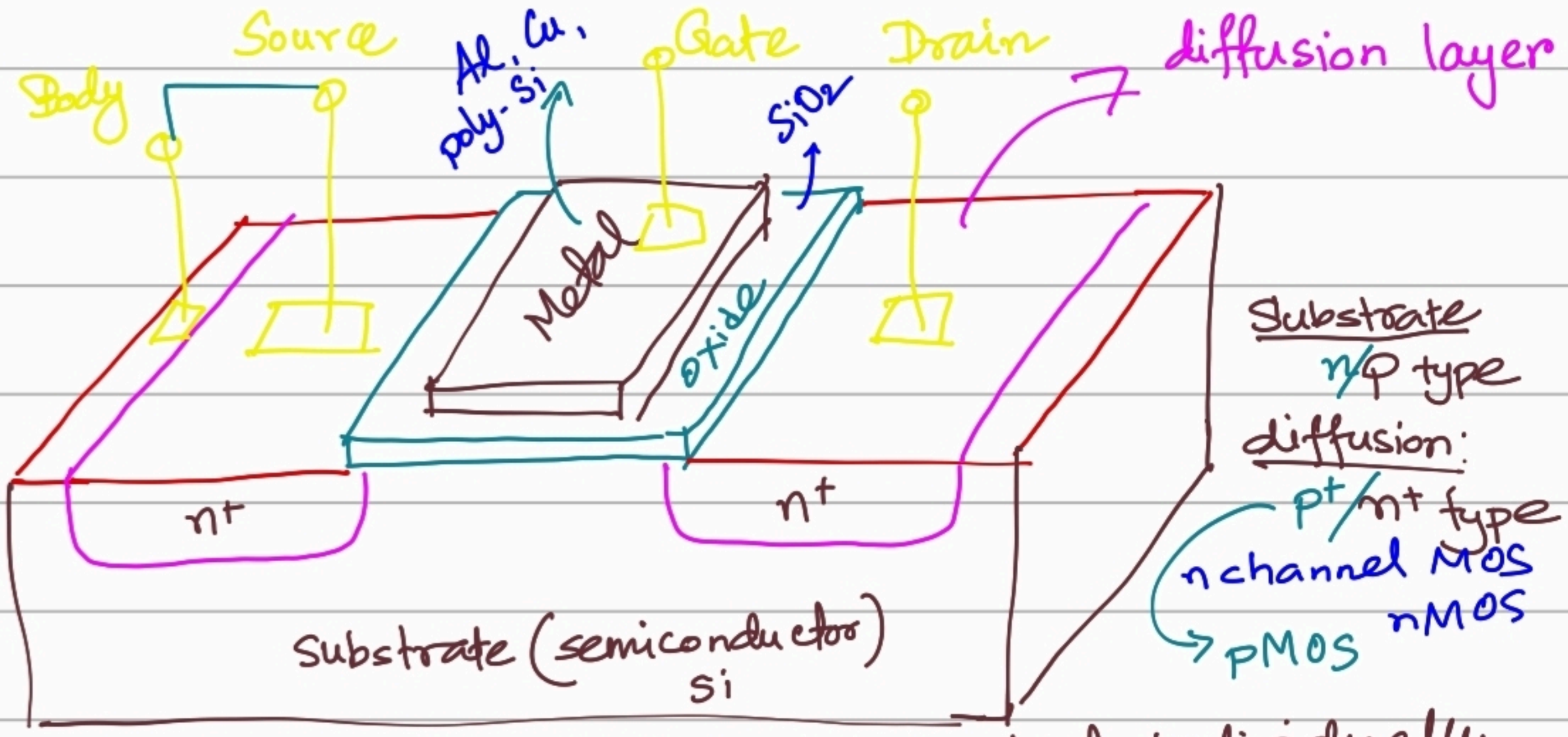
$= \boxed{122}$

Lecture 12: MOS Logic family

Unipolar logic family: Current conduction is done by one type of charge carriers.

e.g. electron or hole.

Basic Internal Structure:

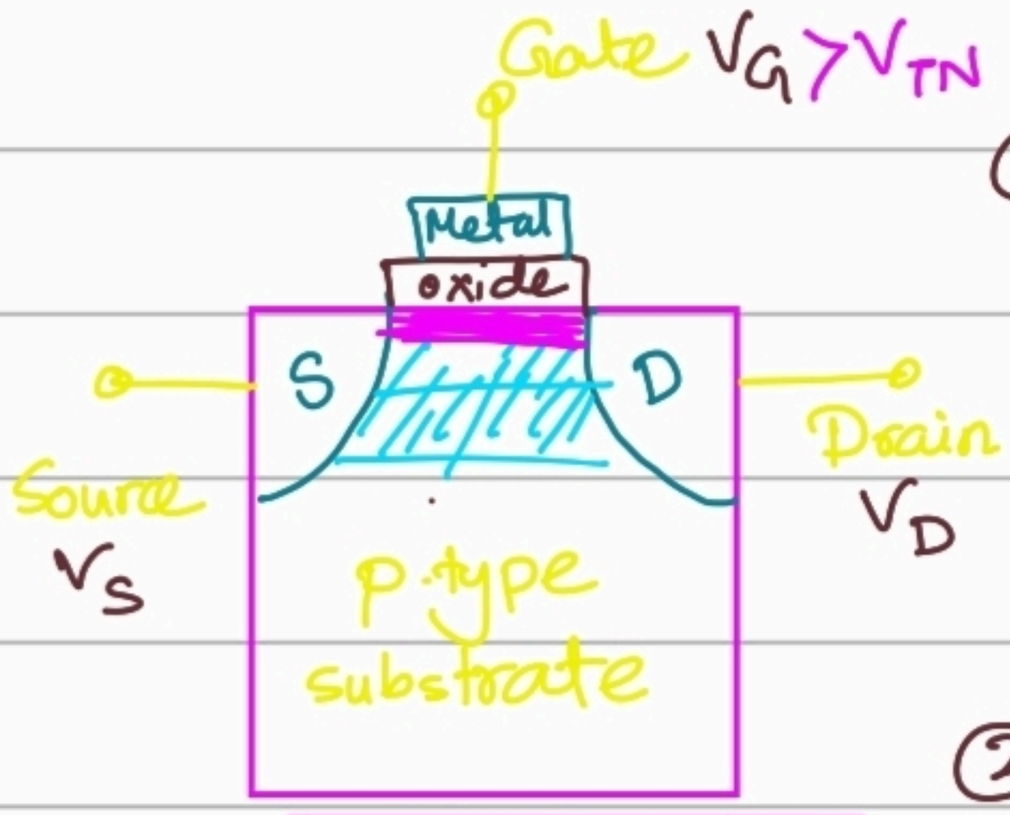


If some MOSFET is fabricated individually then source and body might be shorted.

In VLSI design we connect min/max for voltage is connected to body terminal, p-type/ntype substrate.

Basic Operations

If we apply voltage to the gate terminal.



① If V_G is less than zero, holes inside p-type semi-conductor might accumulate underneath the oxide layer.

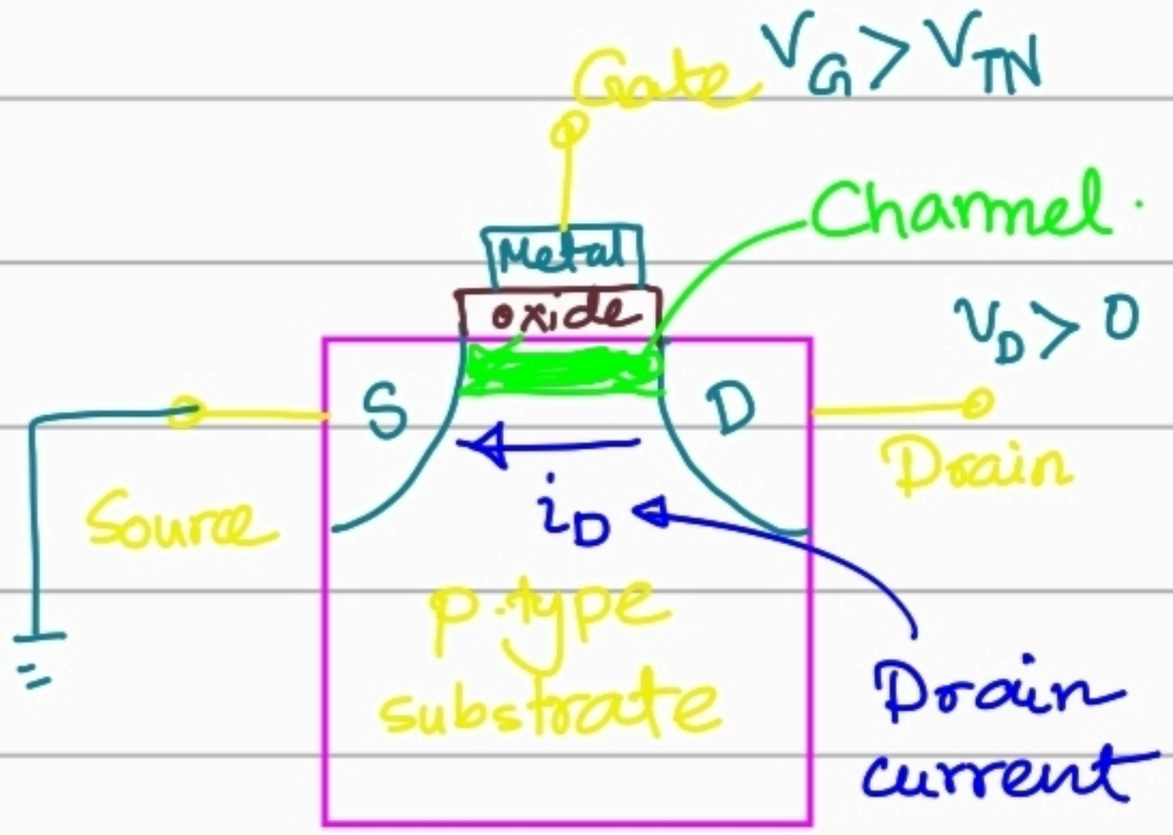
→ accumulation

② If $0 < V_G < V_{TN}$, then depletion layer forms beneath the oxide layer. → depletion

③ If $V_G > V_{TN}$, then an inversion layer would emerge under the oxide layer. → Inversion

Now if we apply positive voltage to drain terminal when $V_G > V_{TN}$

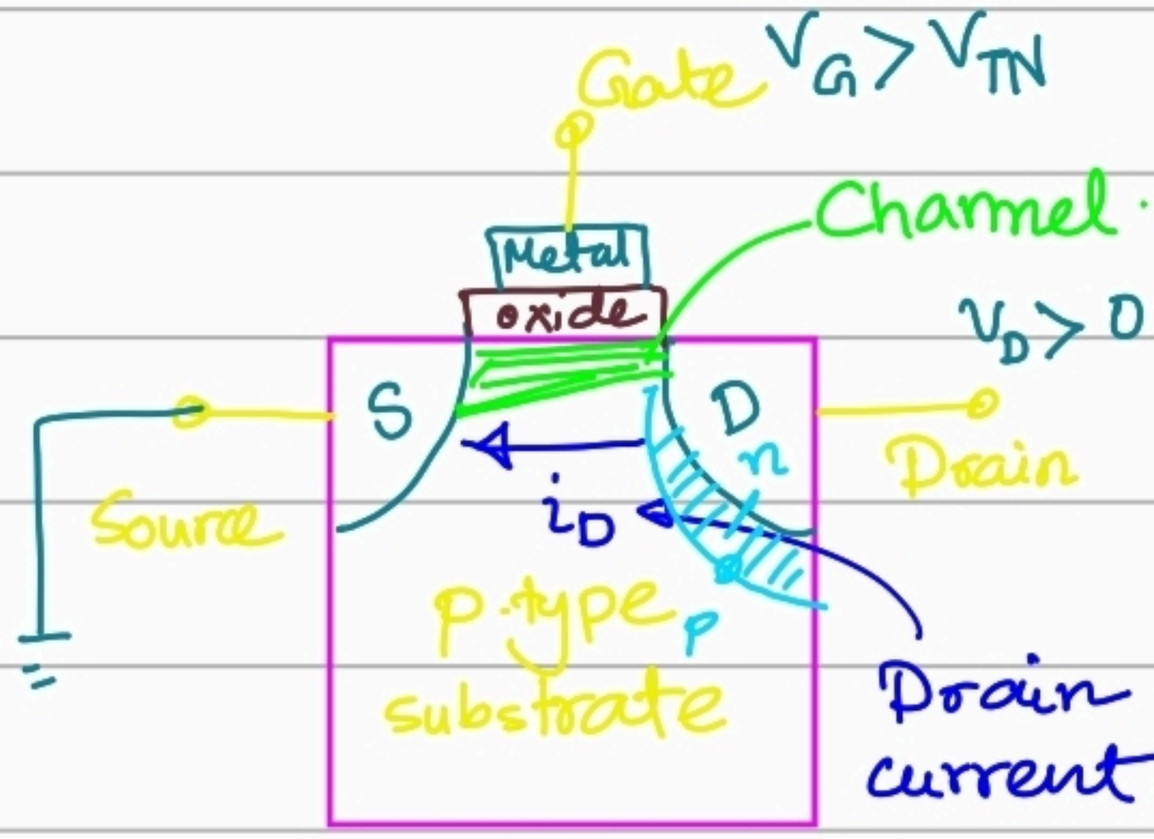
① When drain voltage is very small positive voltage.



- n MOS device.

It behaves like a resistor.

② When drain voltage is not very small.

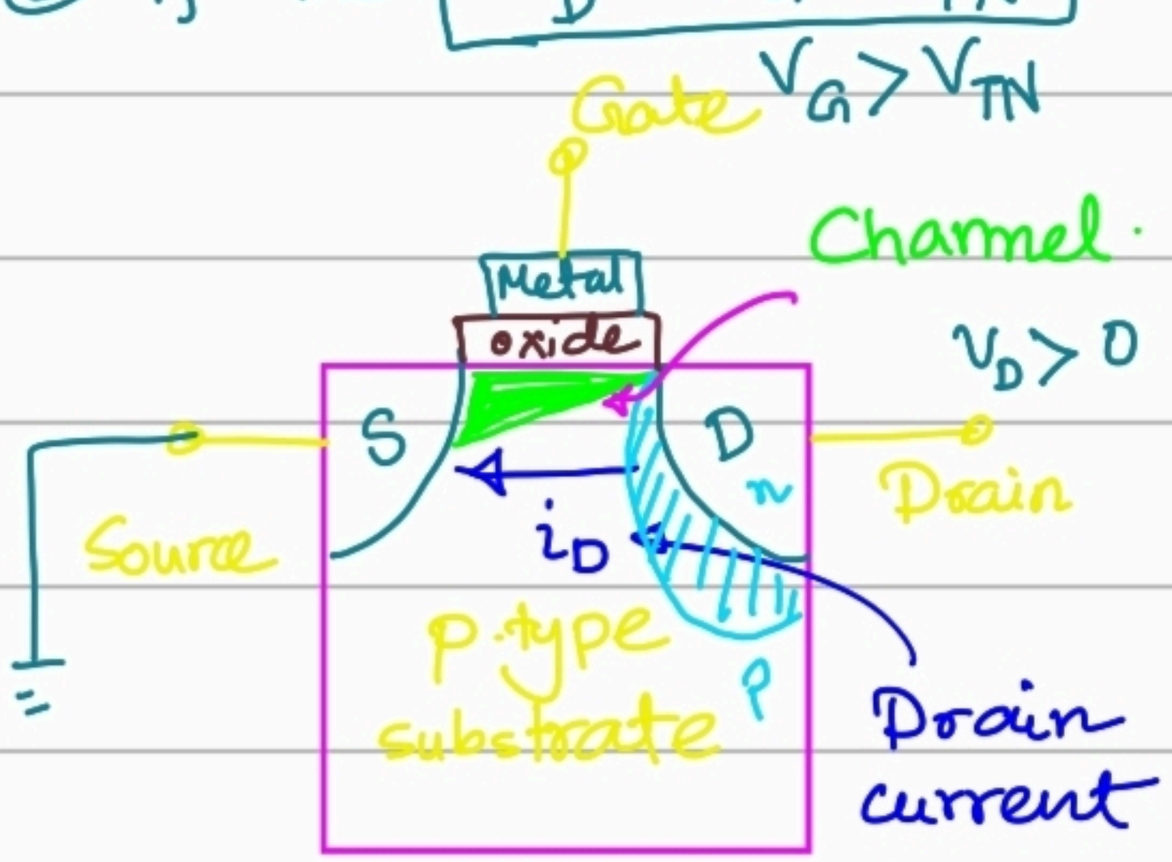


- n MOS device.

Drain-body p-n junction is in reverse bias

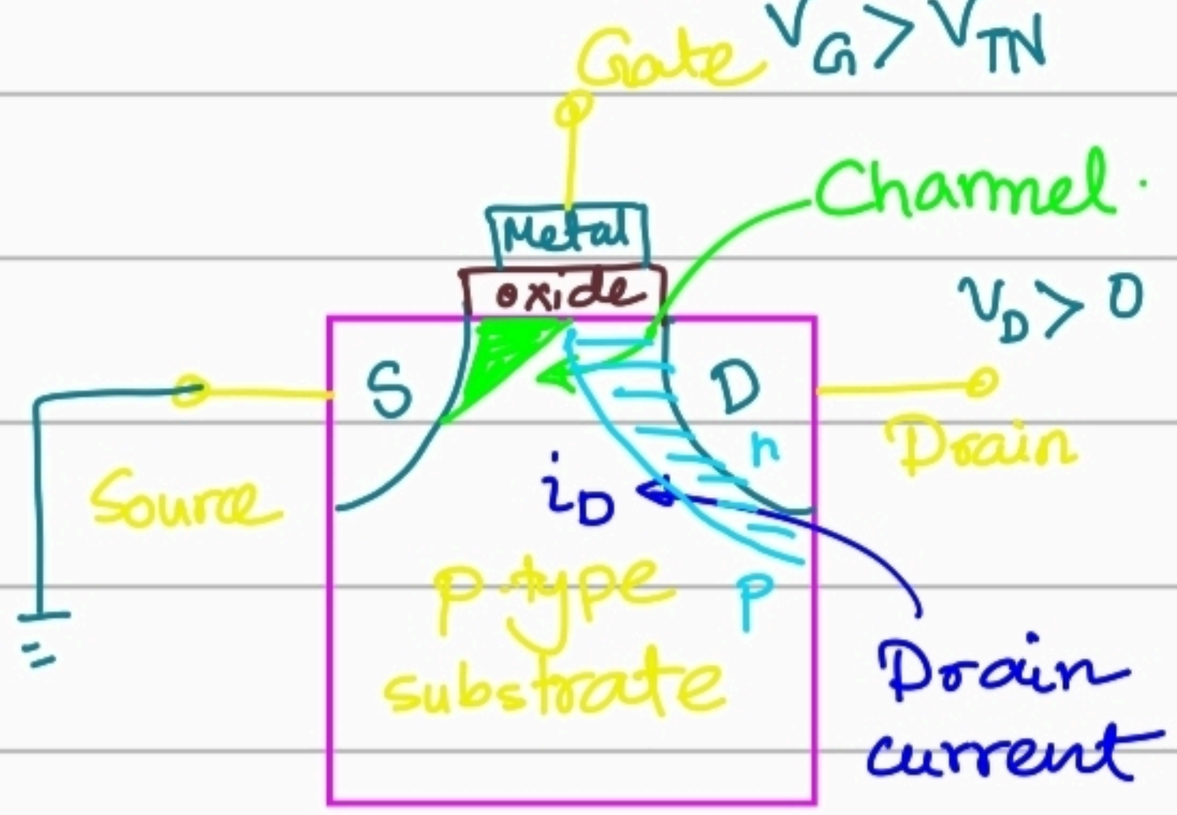
Channel is now shrinking near drain region

③ If the $\boxed{v_D = V_G - V_{TN}}$



- n MOS device.

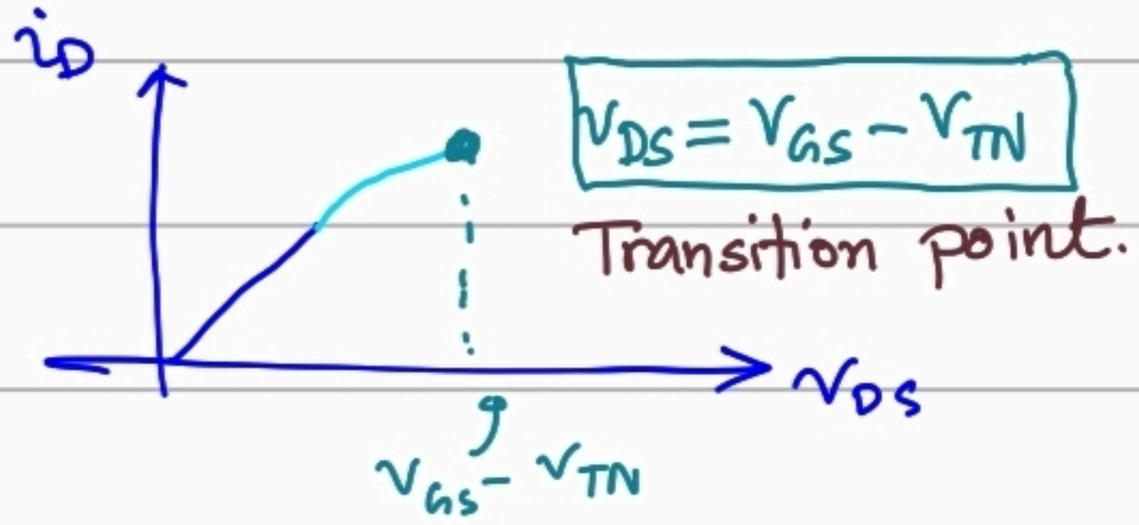
④ $V_D \geq V_G - V_{TN}$

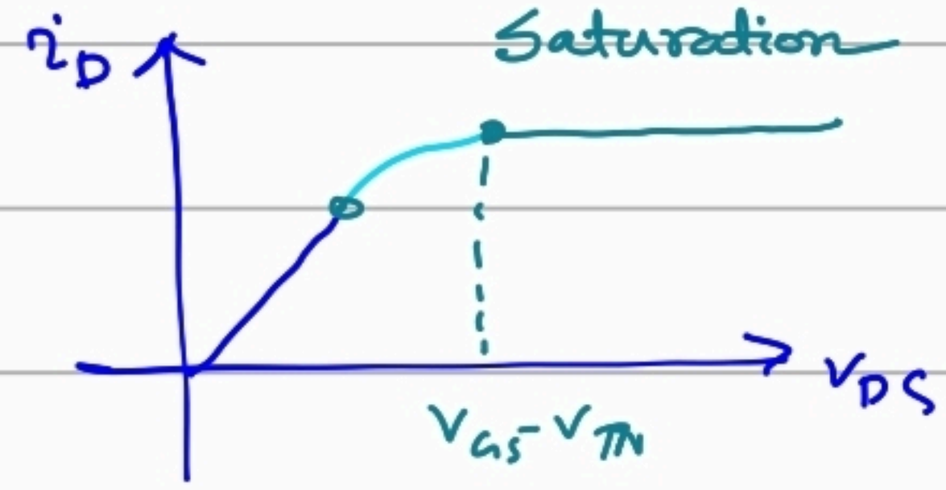


- n MOS device.

Channel region is now pinched off. Thus current can not increase if we apply more voltage.

i_D





Operating modes of MOS-FET

metal-oxide-semiconductor field-effect transistor

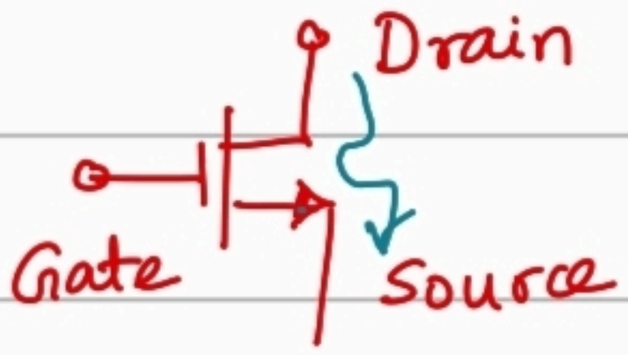
We apply electric field to perform switching operation inside the transistor.

1. Cutoff
2. Linear/Triode
3. Saturation

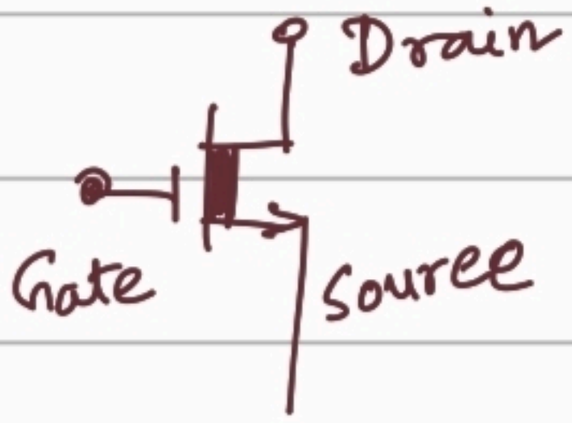
MOSFET types:

MOSFET type	Specially	Cutoff	Triode	Saturation
n-channel enhancement	p-type sub. $V_{TN} > 0$	$v_{GS} < V_{TN}$	$v_{GS} > V_{TN}$ $v_{DS} \leq V_{GS} - V_{TN}$	$v_{GS} > V_{TN}$ $v_{DS} \geq V_{GS} - V_{TN}$
n-channel depletion	p-type sub. $V_{TN} < 0$	$v_{GS} < V_{TN}$	$v_{GS} > V_{TN}$ $v_{DS} \leq V_{GS} - V_{TN}$	$v_{GS} > V_{TN}$ $v_{DS} \geq V_{GS} - V_{TN}$
p-channel enhancement	n-type sub $V_{TP} < 0$	$v_{SG} < \lvert V_{TP} \rvert$	$v_{SG} > \lvert V_{TP} \rvert$ $v_{SD} \leq v_{SG} + V_{TP}$	$v_{SG} > \lvert V_{TP} \rvert$ $v_{SD} \geq v_{SG} + V_{TP}$
p-channel depletion	n-type sub. $V_{TP} > 0$	$v_{SG} < \lvert V_{TP} \rvert$	$v_{SG} > \lvert V_{TP} \rvert$ $v_{SD} \leq v_{SG} + V_{TP}$	$v_{SG} > \lvert V_{TP} \rvert$ $v_{SD} \geq v_{SG} + V_{TP}$

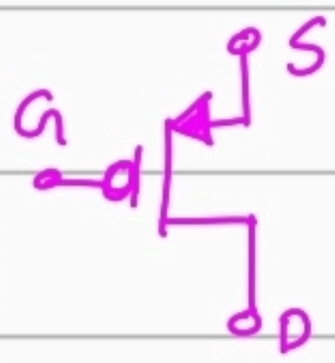
n channel enhancement MOSFET



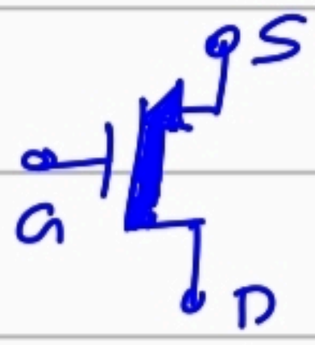
n channel depletion MOSFET



p-channel enhancement MOSFET



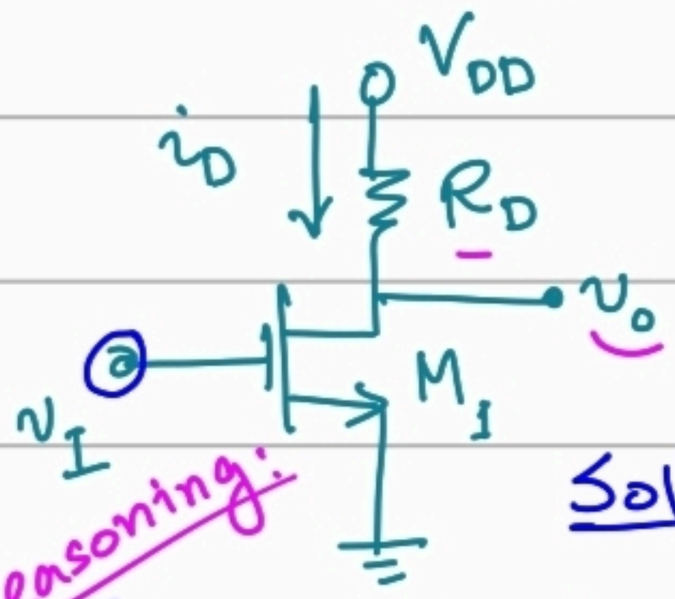
p-channel depletion MOSFET



Current-Voltage Relationships:

NMOS	PMOS
① Cutoff mode: $i_D = 0$	① Cutoff mode: $i_D = 0$
② Triode mode: $i_D = K_n\left(2(V_{GS}-V_{TN})v_{DS}-v_{DS}^2\right)$	② Triode mode: $i_D = K_p\left(2(V_{SG}+V_{TP})v_{SD}-v_{SD}^2\right)$
③ Saturation mode: $v_{DS} = V_{GS}-V_{TN}$, $i_D = K_n(V_{GS}-V_{TN})^2$	③ Saturation mode: $v_{SD} = V_{SG}+V_{TP}$, $i_D = K_p(V_{SG}+V_{TP})^2$

Example: NMOS Inverter:



Q1: Determine v_o for $v_I = 5V$ and $v_I = 1.5V$.

Specification: $V_{DD} = 5V$, $R_D = 20K\Omega$, $V_{TN} = 0.5V$, $K_n = 0.3mA/V^2$

Sol^n: ⓐ $v_I = 5V$. $v_G = v_I = 5V$, $v_S = 0V$.

Reasoning:

Since this circuit will act like an inverter the higher the input voltage, the smaller the output voltage. $\boxed{V_{GS} - V_{TN} = 5 - 0.5 = 4.5V > 0}$. Thus $v_o < V_{GS} - V_{TN}$

So the M_1 might operate in triode region.

Assumption: $M_1 \rightarrow$ triode region.

$$i_D = K_n\left[2(V_{GS}-V_{TN})v_{DS} - v_{DS}^2\right] = \frac{V_{DD}-v_o}{R_D}$$

$$\Rightarrow 0.3m\left[2(5-0.5)v_o - v_o^2\right] = \frac{5-v_o}{20K}$$

$$\Rightarrow \underbrace{20K \times 0.3m}_{6}\left[9v_o - v_o^2\right] = 5 - v_o \Rightarrow 6v_o^2 - 55v_o + 5 = 0$$

$$v_o = \begin{cases} 9.074V \longrightarrow i_D = \frac{5-v_o}{20K} < 0 \text{ which is impossible.} \\ 0.092V \end{cases}$$

Thus. $\boxed{v_o = 0.092V}$

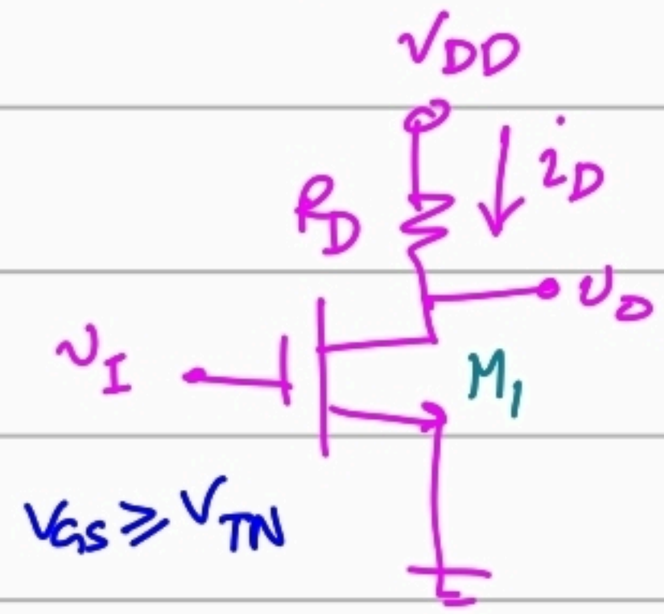
verification:

$$v_o = v_{DS} = 0.092 < 4.5 = (V_{GS} - V_{TN})$$

Therefore our assumption is valid.

(b). $v_I = 1.5V$. Assumption: $M_1 \rightarrow$ saturation.

$$i_D = K_n[(V_{GS}-V_{TN})]^2$$
$$= 0.3[1.5-0.5]^2 = 0.3mA$$
$$i_D = \frac{V_{DD}-v_o}{R_D} = \frac{5-v_o}{20k} = 0.3m$$
$$\Rightarrow v_o = -1V$$



$$v_{DS} = v_o = -1V < (V_{GS}-V_{TN}) = 1V$$

This contradicts our assumption that $V_{DS} \geq V_{GS}-V_{TN}$ (saturation)

Therefore. M_1 must be in triode/ linear mode.

$$i_D = \frac{5-v_o}{20} = 0.3[2(1.5-0.5)v_o - v_o^2]$$
$$\Rightarrow 0.3v_o^2 + 0.65v_o - 0.25 = 0$$
$$v_o = \begin{cases} 1.6667V \rightarrow V_{DS} > (V_{GS}-V_{TN}) = 1V \\ \boxed{0.5V} \end{cases}$$

This can not be the answer because M_1 must be in triode mode.

Therefore. $\boxed{v_o = 0.5V}$

Verification: $v_{DS} = 0.5 < (V_{GS}-V_{TN}) = 1V$

Thus our answer is not wrong.

Q3

April. 2. Classtime: 3:30-5:00pm

Online/Offline: UB80402

proctore.

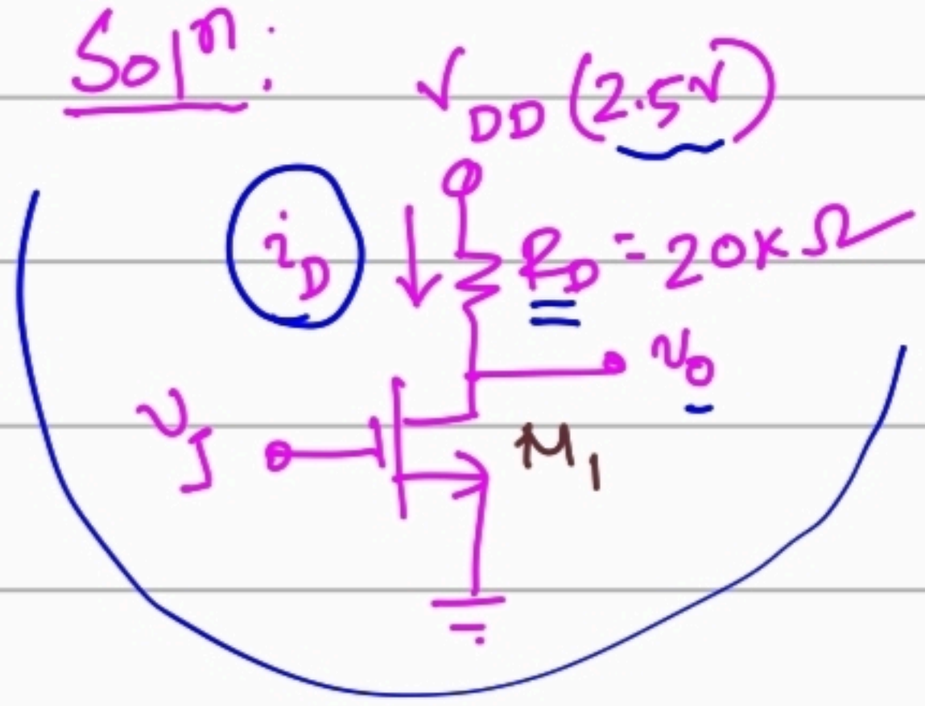
Syllabus: ECL logic family.

Lecture 13: MOS logic family. CMOS logic-circuit

Example: Determine the transition point, maximum drain current and maximum power dissipation of an NMOS inverter with resistor.

Specification: $V_{DD} = 2.5V$, $R_D = 20K\Omega$, $V_{TN} = 0.5V$, $K_n = 0.3mA/V^2$

Sol^n:



Observation: When output (v_o) has the smallest value then $i_D = \frac{V_{DD} - v_o}{R_D}$ would have a maximum value. Therefore, maximum input voltage is needed to produce this output value.

We can take maximum value of input voltage at 2.5V. $v_I = 2.5V$. [$M_1 \rightarrow$ triode]

$$i_D = \left(\frac{2.5 - v_o}{20K}\right) = 0.3m\,[2(2.5 - 0.5)v_o - v_o^2]$$

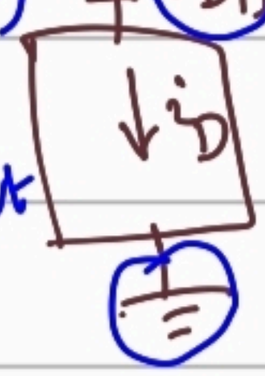
$$\Rightarrow 6v_o^2 - 25v_o + 2.5 = 0. \qquad v_o = \begin{cases} 0.1025V \\ 4.064V \end{cases}$$

$v_o \neq 4.064V$ because that will produce negative i_D.

[$v_o = 0.1025V$]. [verify: $0.1025 < (V_{GS} - V_{TN}) = 2V$]

$V_{DS} \leq (V_{GS} - V_{TN})$

$$i_D = \frac{2.5 - 0.1025}{20K} = \boxed{0.1198\,mA}$$ ← max drain current



$$P = \Delta V I = (V_{DD} - 0)\,i_D = 2.5 \times 0.1198$$

maximum power dissipation $= \boxed{0.3\,mW}$

Transition point: [$\cancel{V_{DS}}^{v_o} = \cancel{V_{GS}}^{v_I} - V_{TN}$]

at transition point, $i_D = K_n(V_{GS} - V_{TN})^2$

$$i_D = \left(\frac{V_{DD} - v_o}{R_D}\right) = K_n(\cancel{V_{GS}}^{v_I} - V_{TN})^2 = K_n v_o^2 v_I$$

$$\Rightarrow \frac{2.5 - v_o}{20K} = 0.3m \cdot v_o^2 \Rightarrow 6v_o^2 + v_o - 2.5 = 0 \checkmark$$

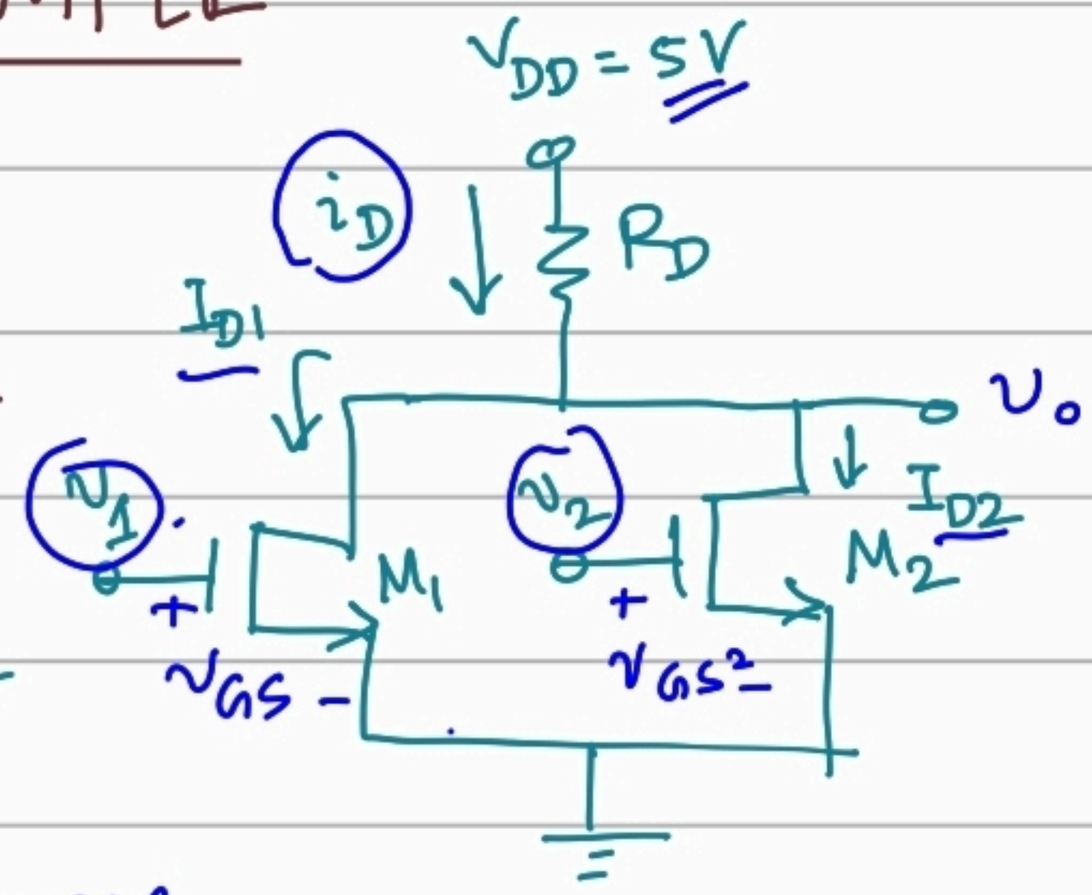
$v_o = \begin{cases} 3.4051\ V \\ 0.5675\ V \end{cases}$ → if it were the sol^n, i_D would be negative.

∴ At transition point $\boxed{v_o = 0.5675\ V}$

$v_o = v_I - V_{TN}$ $\boxed{v_I = v_o + V_{TN} = 1.0675\ V}$

NMOS NOR GATE EXAMPLE

Objective: Determine the current and voltages in this gate for different input conditions:



$R_D = 20K\Omega$, $K_n = 0.1mA/V^2$

$V_{TN} = 0.8V$.

Sol^n: ① Case 1: $V_1 = V_2 = 0V$.

For M_1 we have $v_{GS1} = V_{G1} - V_{S1} = 0 - 0 = 0 < 0.8V$

" M_2 " " $v_{GS2} = V_{G2} - V_{S2} = 0 < 0.8V$

Therefore, M_1 and M_2 are in cutoff mode.

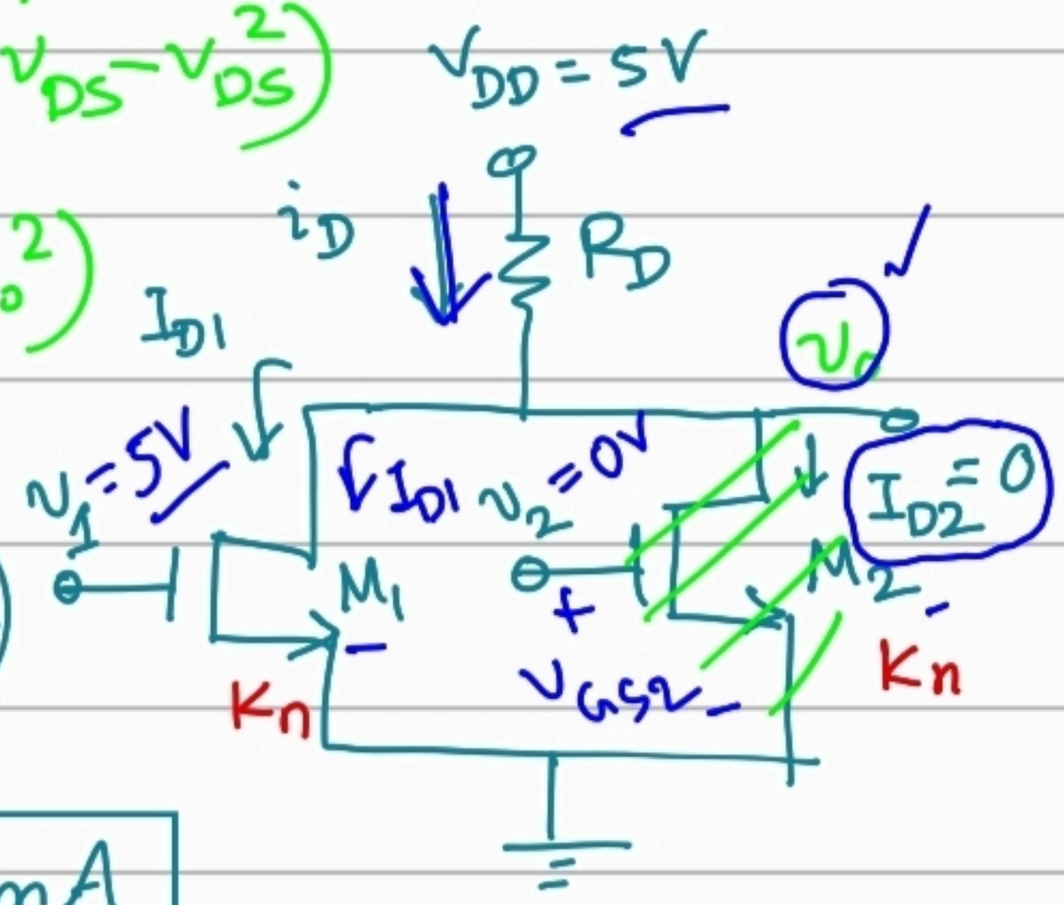
$\boxed{I_{D1} = I_{D2} = i_D = 0. \quad v_o = V_{DD} = 5V}$.

② Case 2: $V_1 = 5V$ and $V_2 = 0V$.

Since $V_{GS2} = 0 < 0.8$, M_2 must be in cutoff. $\boxed{I_{D2} = 0}$

So, we can assume M_1 is operating in triode region

$$i_D = \frac{V_{DD} - v_o}{R_D} = K_n\left(2(V_{GS} - V_{TN})v_{DS} - v_{DS}^2\right)$$



$$\Rightarrow \left(\frac{5 - v_o}{20K}\right) = 0.1m\left(2(5 - 0.8)v_o - v_o^2\right)$$

$$\Rightarrow 2v_o^2 - 9.4v_o + 5 = 0$$

$v_o = \begin{cases} 8.6V \rightarrow (i_D < 0, \text{ impossible}) \\ 0.29V \end{cases}$ ∴ $\boxed{v_o = 0.29V}$

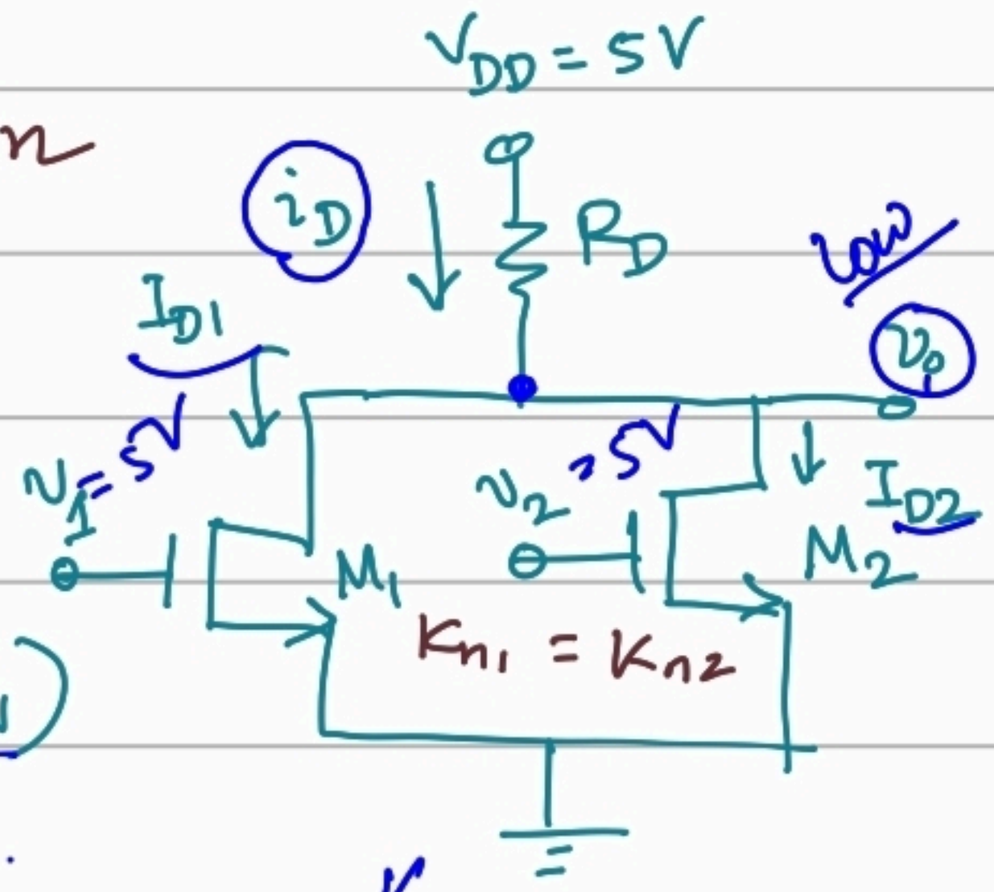
$$\boxed{i_D = I_{D1} = \frac{5 - 0.29}{20} = 0.2354\ mA}$$

Case: ③. $V_1 = 0V$, $V_2 = 5V$. $M_1 \rightarrow$ cutoff, $M_2 \rightarrow$ Triode,

$v_o = 0.29V$, $i_D = 0.2354$ mA $[K_{n1} \neq K_{n2}]$

$I_{D1} = 0$ mA, $I_{D2} = 0.2354$ mA. $\left[\begin{matrix} V_{TN1} \neq V_{TN2} \\ K_{n1} \neq K_{n2} \end{matrix}\right]$

Case ④ $V_1 = V_2 = 5V$



Assuming, M_1 and M_2 are in triode region.

Reasoning: Because both inputs are high we might expect very low output voltage or drain voltage. ($v_{DS} < v_{GS} - V_{TN}$)

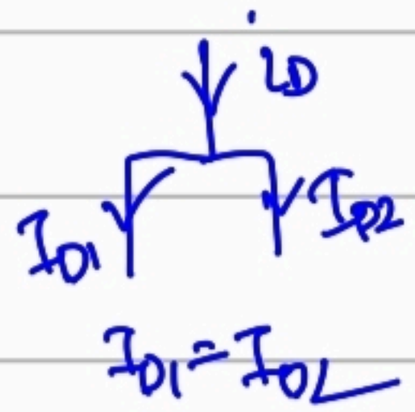
$i_D = I_{D1} + I_{D2}$ ← using KCL.

$\Rightarrow \frac{5 - v_o}{20K} = 0.1m\left[2 \times (5 - 0.8)v_o - v_o^2\right] \times 2$

$\Rightarrow 8v_o^2 - 34.6v_o + 5 = 0$. $v_o = \begin{cases} \boxed{9.17V} \\ 0.149V \end{cases}$ → Check yourself!

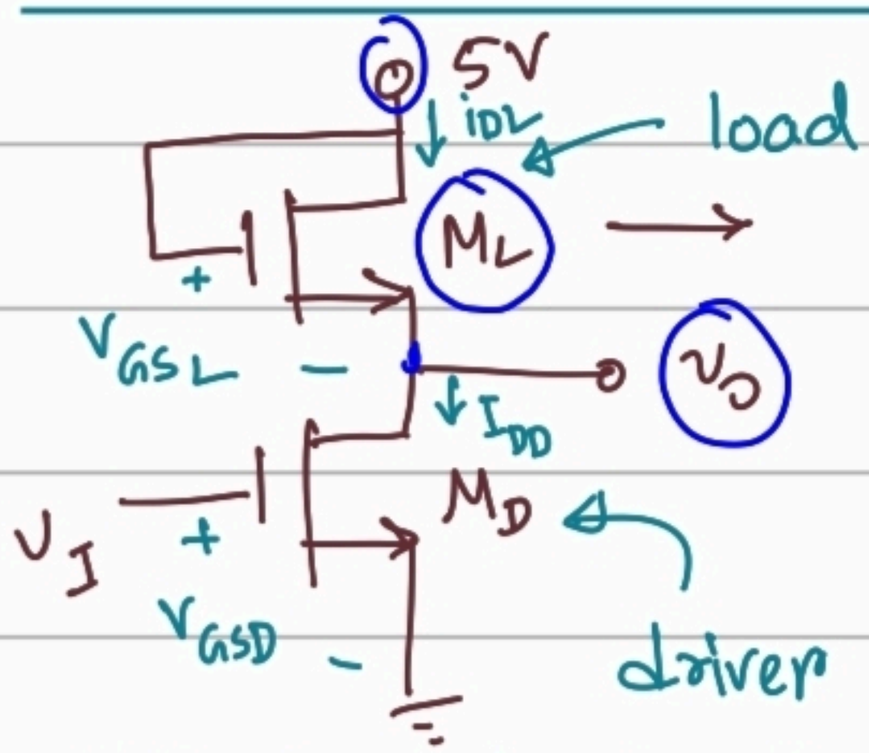
$v_o \neq 4.17V$ because, $v_{DS} = 4.17V$ which is much large value

$\boxed{v_o = 0.149V}$ $i_D = \frac{5 - 0.149}{20K} = \boxed{0.243 mA}$



$I_{D1} = I_{D2} = \frac{i_D}{2} = \boxed{0.121 mA}$

NMOS INVERTER with ENHANCEMENT LOAD



load nMOS is going to be enhancement type.

Determine the DC currents and voltages in the circuit containing enhancement load.

This is only true for MOSFET

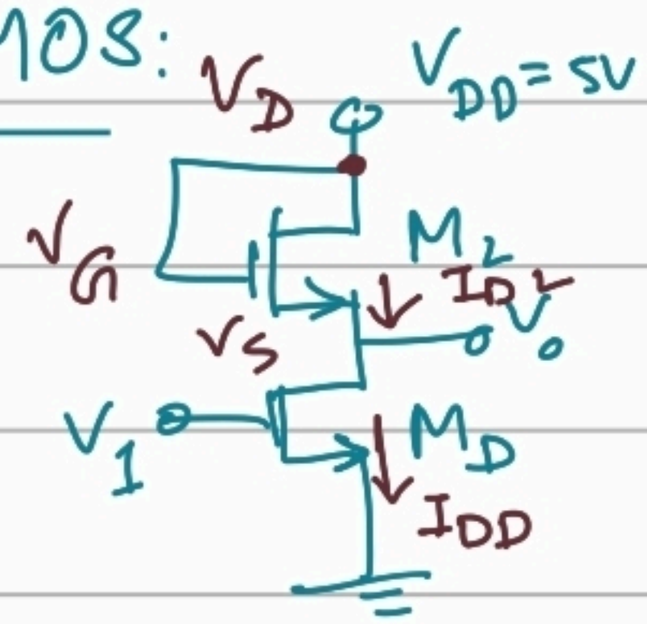
Specifications: $V_{TND} = V_{TNL} = 1V$, $K_{nD} = 50 \mu A/V^2$

$K_{nL} = 10 \mu A/V^2$. Determine v_o, when $v_I = 5V$ and $v_I = 1.5V$.

Lecture 14 CMOS logic family (Inverter)

Sol^n: Case: 1 $V_1 = 1.5V$.

Observation regarding load nMOS:



For M_L, we can see that

$V_{G(L)} = V_{DL} = 5V$. Therefore,

$$V_{DSL} = V_{DL} - V_{SL} = V_{GL} - V_{SL}$$

$$\Rightarrow V_{DL} - V_{SL} \geq (V_{GL} - V_{SL}) - V_{TNL}$$

$$\Rightarrow V_{DSL} \geq (V_{GSL}) - V_{TNL}$$

Therefore M_L satisfies saturation condition regardless of input and output voltage.

Thus, M_L must be in saturation mode for all cases.

Now for M_D, we are assuming saturation mode. [We are expecting output voltage or V_{DSD} is high compared to $V_{GSD} - V_{TND}$]

Using KCL. $I_{DL} = I_{DD}$

$$\Rightarrow K_{nL}(V_{GSL} - V_{TNL})^2 = K_{nD}(V_{GSD} - V_{TND})^2$$

$$\Rightarrow 0.01(5 - V_o - 1)^2 = 0.05(1.5 - 0 - 1)^2$$

$$\Rightarrow V_o = 2.88V. \Rightarrow V_{DSD} = 2.88 > \underbrace{V_{GSD} - V_{TND}}_{0.5}$$

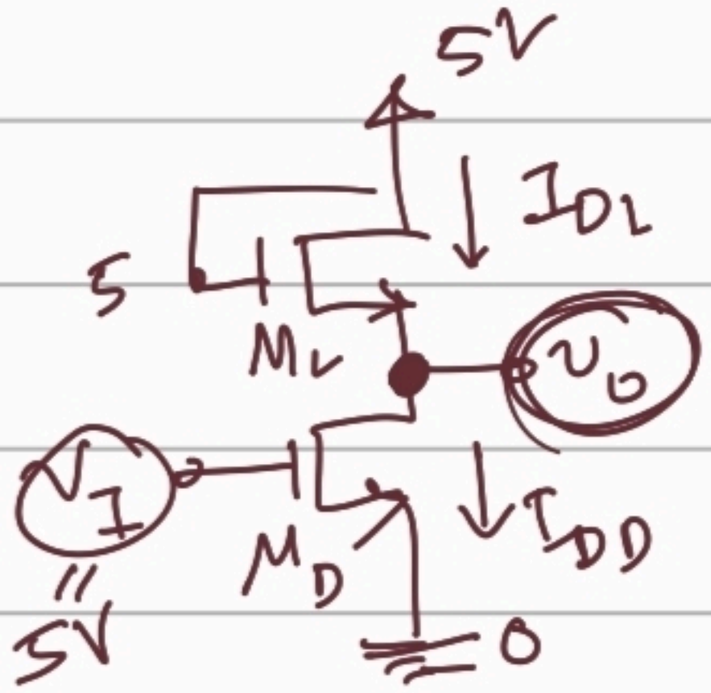
Our assumption is valid.

$$\therefore I_{DL} = I_{DD} = 0.05(1.5 - 1)^2 = \boxed{12.5\mu A}$$

$$= \boxed{1.25 \times 10^{-2} mA}$$

Case ②: $v_I = 5V$. [Because input is high we are expecting to get small output voltage, thus drain voltage is small therefore it might be less than $V_{GS}-V_{TN}$]

So we are assuming M_D is in triode mode



$$I_{DL} = I_{DD}$$

$$K_{nL}(V_{GSL}-V_{TNL})^2 = K_{nD}\left(2(V_{GSD}-V_{TND})\cdot V_{DSD} - V_{DSD}^2\right)$$

$$\Rightarrow \frac{10}{1000}(5-v_o-1)^2 = \frac{50}{1000}\left(2(5-0-1)v_o - v_o^2\right)$$

$$\Rightarrow 6v_o^2 - 48v_o + 16 = 0$$

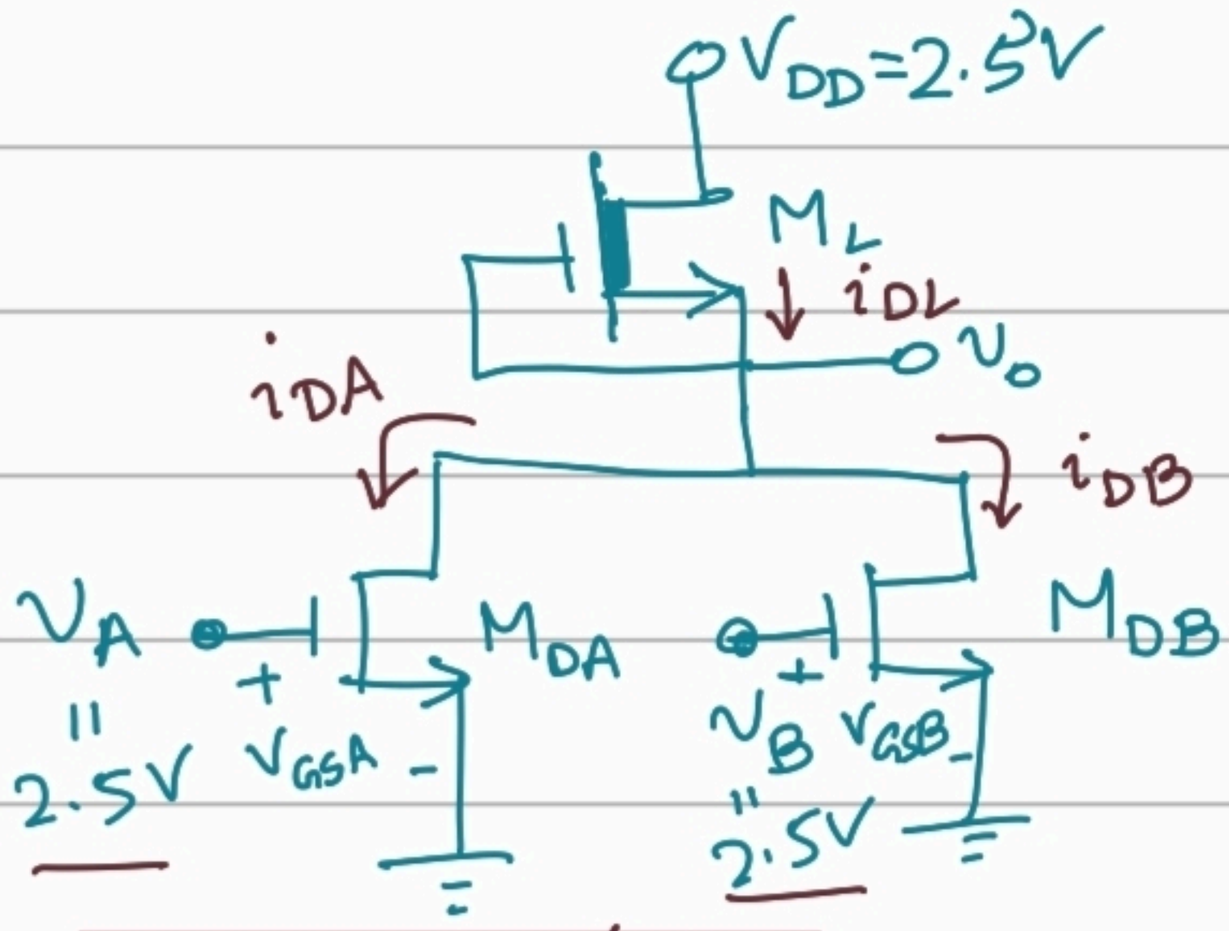
$$\Rightarrow v_o = \begin{cases} 7.65\,V \\ 0.34\,V \end{cases}$$

$\Rightarrow$ Here $7.65V > 5V = V_{DD}$ which is impossible

Therefore, $v_o = 0.34V$. $I_D = \frac{10}{1000}m(5-0.34-1)^2$

$$\boxed{I_{DL} = I_{DD} = 0.133\,mA}$$

(Quiz 4) NMOS NOR GATE with Depletion Load



Q: Determine the output voltage of NMOS NOR gate.

$k_n' = 100\mu A/V^2 = 0.1\,mA/V^2$

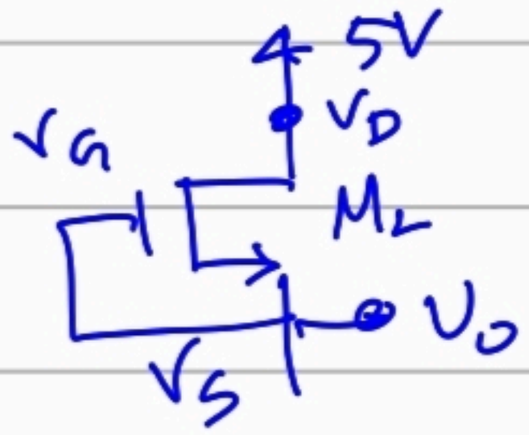
$V_{TND} = V_{TNA} = V_{TNB} = 0.4V$

$V_{TNL} = -0.6V$

$\left(\frac{W}{L}\right)_D = 4$, $\left(\frac{W}{L}\right)_L = 1$.

$$\boxed{K_n = k_n'\left(\frac{W}{L}\right)}$$

Sol^n: Observation: As this is a NOR gate when two input voltages are high, output voltage is low. Therefore v_o is small.



For M_L depletion type NMOS we have $V_{GSL} = V_{GL} - V_{SL} = 0V$

$V_{DSL} = V_{DL} - V_{SL} = 5 - v_o \rightarrow$ this value is large.

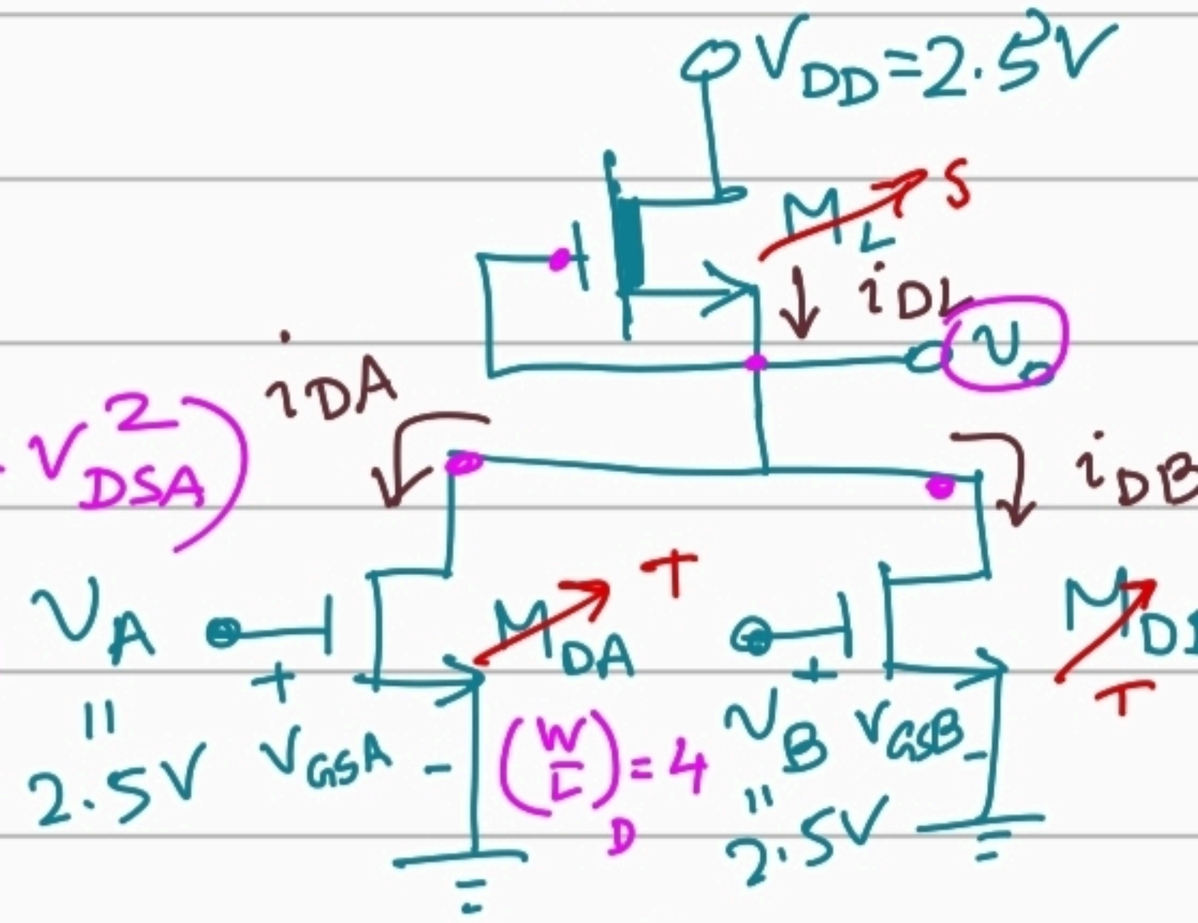
Thus. $V_{DSL} \geq V_{GSL} - V_{TNL} = 0 - (-0.6) = 0.6$

$5 - v_o \geq 0.6$ [Because we expect v_o to be small]

Hence, for this particular input condition we can deduce that M_L must be in saturation mode.

We are also expecting M_{DA} and M_{DB} to be in triode mode because v_o or drain voltage is smaller than gate voltage minus threshold voltage.

$$i_{DL} = i_{DA} + i_{DB}$$



$$\Rightarrow K_{nL}(V_{GSL} - V_{TNL})^2$$

$$= K_{nA}\left(2(V_{GSA} - V_{TNA})V_{DSA} - V_{DSA}^2\right) + K_{nB}\left(2(V_{GSB} - V_{TNB})V_{DSB} - V_{DSB}^2\right)$$

$$\Rightarrow \cancel{k_n'}\left(\frac{W}{L}\right)_L^{1}(0 - (-0.6))^2$$

$$= \cancel{k_n'}\left(\frac{W}{L}\right)_D^{4}\left(2(2.5 - 0 - 0.4)v_o - v_o^2\right) + \cancel{k_n'}\left(\frac{W}{L}\right)_D^{4}\left(2(2.5 - 0.4)v_o - v_o^2\right)$$

$\Rightarrow 4v_o^2 - 16.8v_o + 0.36 = 0$

$\underline{v_o} = \begin{cases} 4.178V \rightarrow v_o \geq 2.5 = V_{DD} \text{ which is not possible.} \\ \underline{0.02153V} \end{cases}$

Finally, the solution. $v_o = 0.02153V$.

$$i_{DL} = k_n' \left(\frac{W}{L}\right)_L (V_{GSL} - V_{TNL})^2$$

$$= \frac{100}{1000} \times 1 (0 - (-0.6))^2 = \boxed{0.036mA}$$

$$i_{DA} = k_n' \left(\frac{W}{L}\right)_D \left(2(V_{GSA} - V_{TNA}) V_{DSA} - V_{DSA}^2\right)$$

$$= \frac{10}{1000} \times 4 \left(2(2.5 - 0.4) 0.02153 - 0.02153^2\right)$$

$$= \boxed{0.018mA}$$

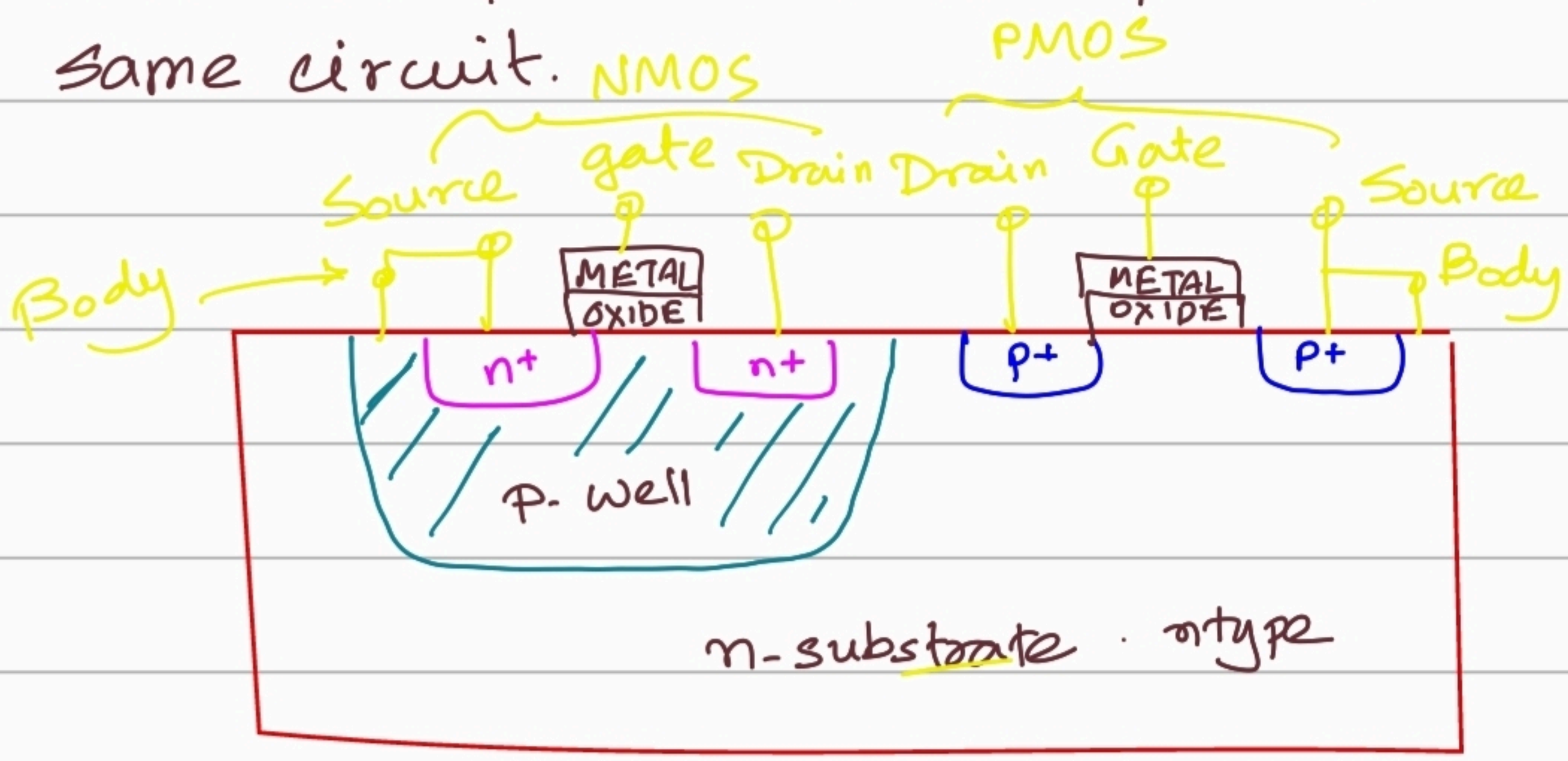
$$i_{DB} = k_n' \left(\frac{W}{L}\right)_D \left(2(V_{GSB} - V_{TNB}) V_{DSB} - V_{DSB}^2\right)$$

$$= \boxed{0.018mA}$$

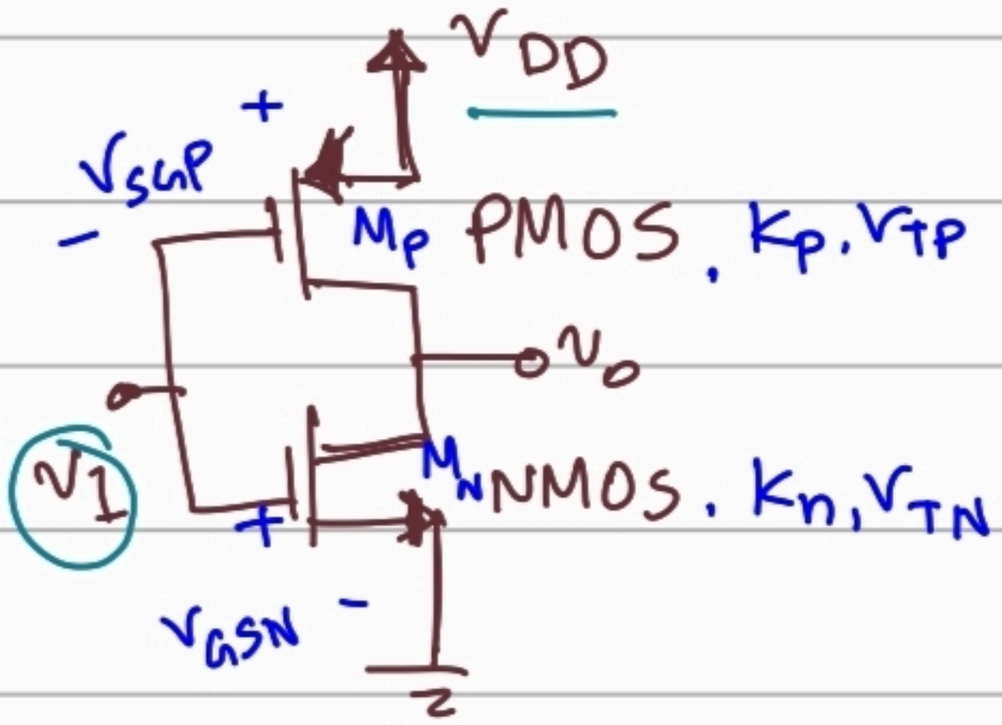
INTRODUCTION TO CMOS LOGIC FAMILY

CMOS → complementary MOSFET.

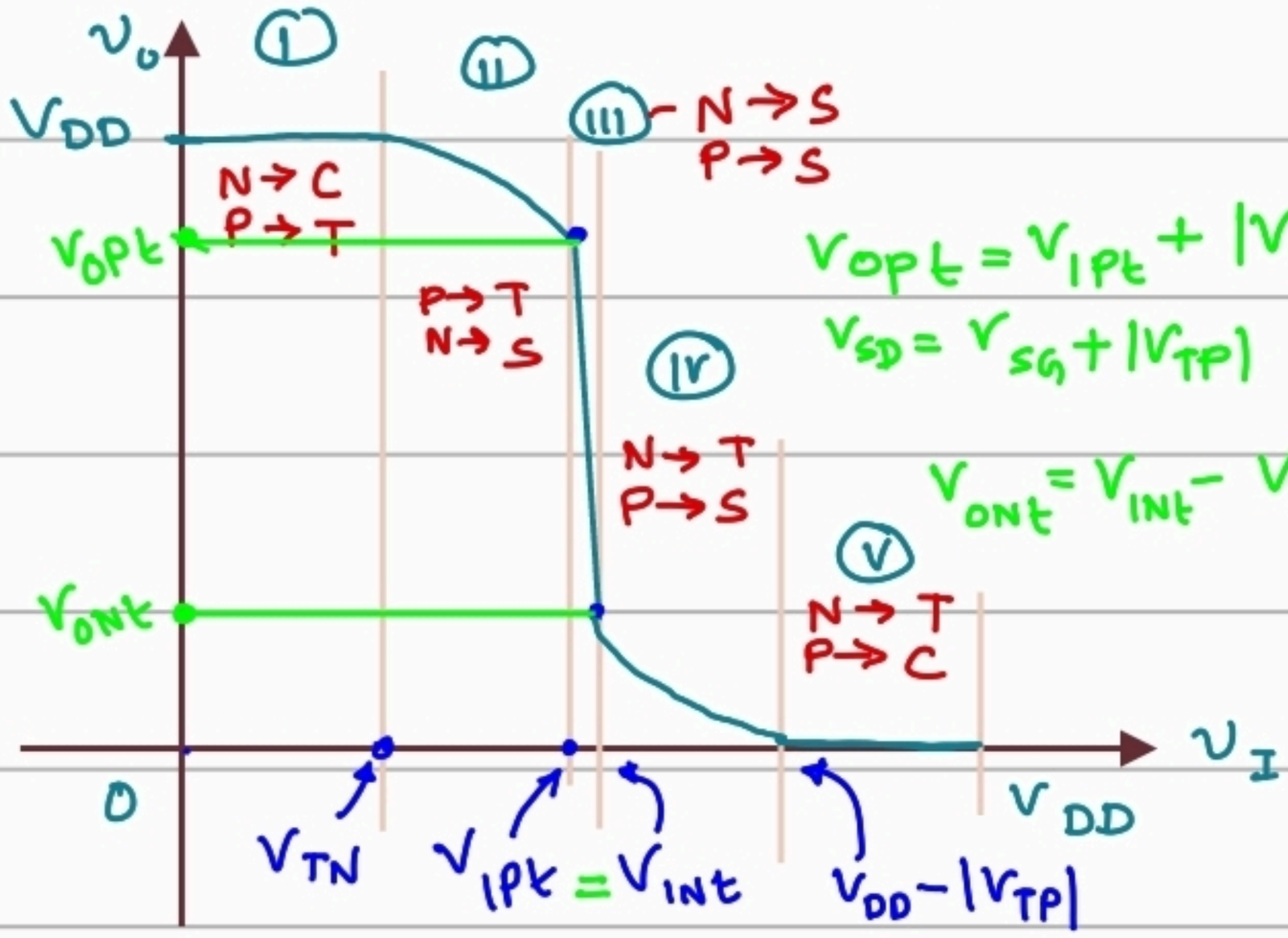
nMOS and pMOS both are present in same circuit.



Basic CMOS inverter :



Transfer characteristics of CMOS inverter



$V_{OPt} = V_{IPt} + |V_{TP}|$

$V_{SD} = V_{SG} + |V_{TP}|$

$V_{ONt} = V_{INt} - V_{TN}$

Region 1: $0 \le V_I \le V_{TN}$, $M_N \rightarrow$ cutoff, $M_P \rightarrow$ triode

$v_o \approx V_{DD}$

Region 2: $V_{TN} \le V_I \le V_{IPt}$ = transistion voltage of PMOS

$M_N \rightarrow$ saturation. $M_P \rightarrow$ triode.

Region 3: $V_{IPt} \le V_I \le V_{INt}$ = transition voltage of NMOS

$M_N \rightarrow$ saturation. $M_P \rightarrow$ saturation.

Region 4: $V_{INt} \le V_I \le V_{DD} - |V_{TP}|$

$M_N \rightarrow$ triode. $M_P \rightarrow$ saturation

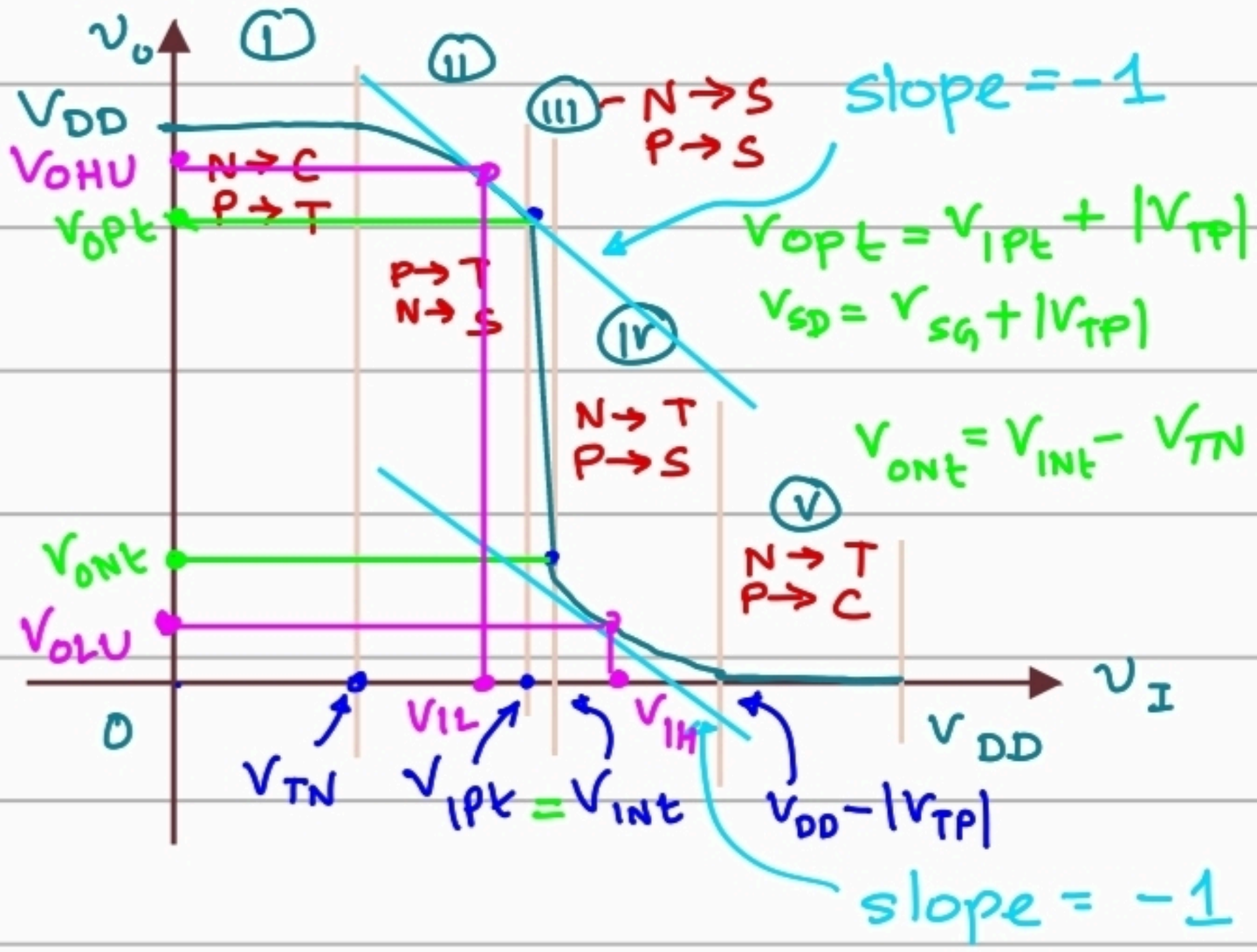
Region 5: $V_{DD} - |V_{TP}| \le V_I \le V_{DD}$

$M_N \rightarrow$ triode. $M_P \rightarrow$ cutoff. $v_o = 0V$.

CMOS inverter NOISE MARGIN:

For CMOS inverter it is best practice to consider unit gain noise margin.

definition: differential gain $= \dfrac{dv_o}{dv_I}$



We take the (v_O, v_I) points for noise margin calculation where the curve has slope -1 or $\frac{dv_O}{dv_I} = -1$

$\left|\frac{dv_O}{dv_I}\right| = 1$ = unit gain

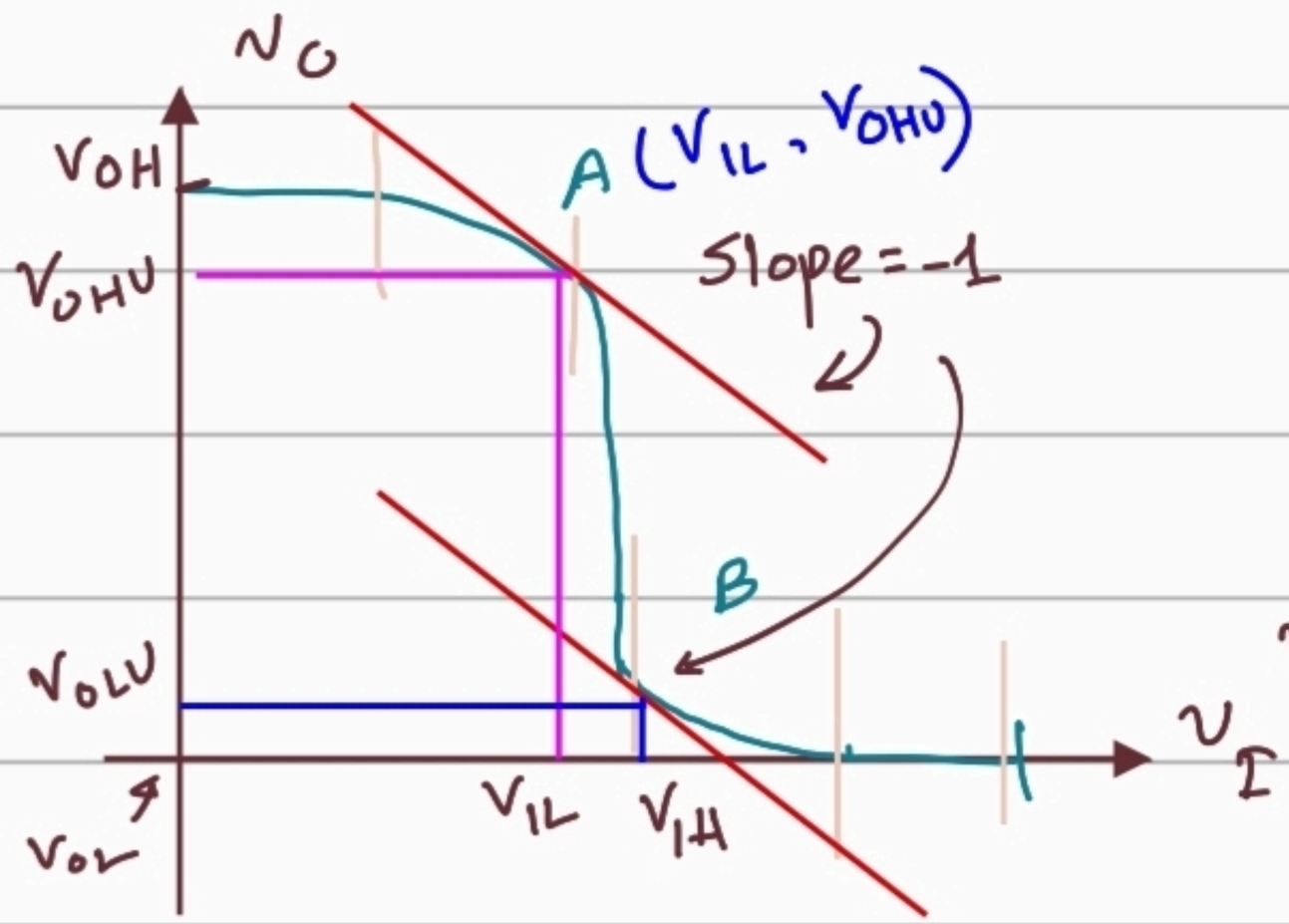
Noise margin low. $NM_L = V_{IL} - V_{OLU}$

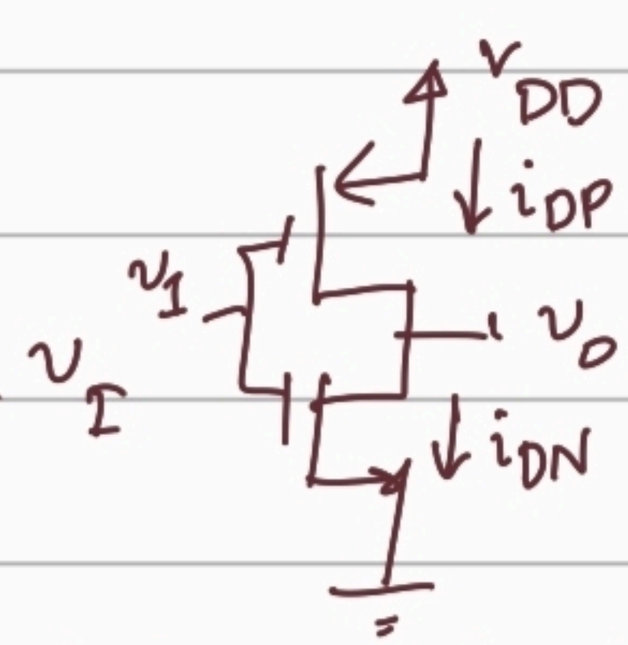
Noise margin high. $NM_H = V_{OHU} - V_{IH}$

Noise margin. $NM = \min(NM_H, NM_L)$.

Lecture 15: CMOS logic family

CMOS INVERTER NOISE MARGIN CALCULATION





Example: 16.9

Determine the noise margin of CMOS inverter.

Specifications:

$V_{DD} = 3.3V$

$k_n = k_p$

$V_{TN} = -V_{TP} = 0.4V$

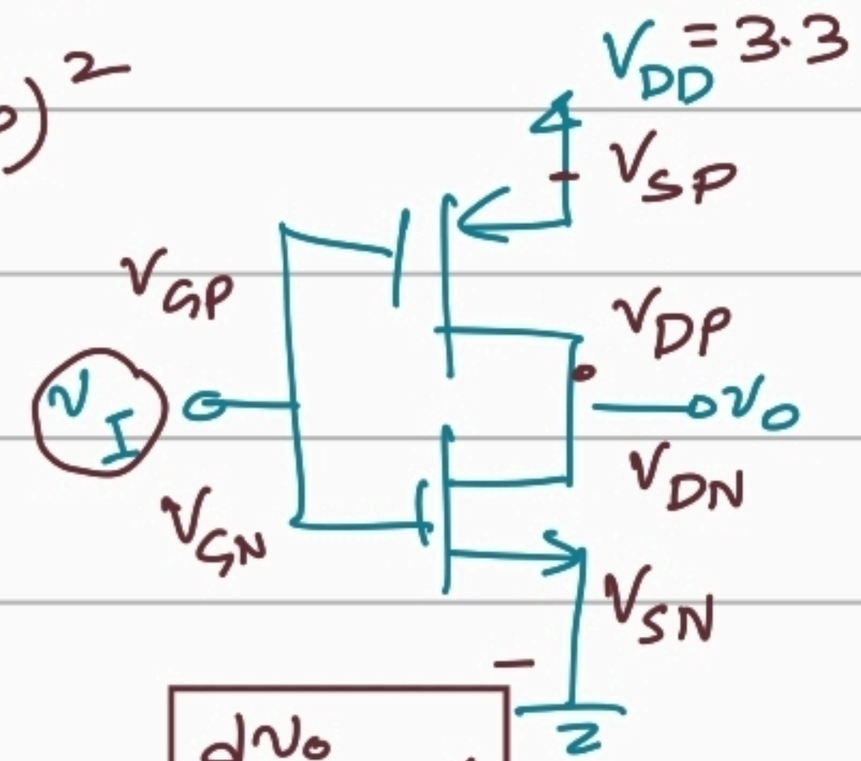
Sol^n: V_{OHU} and V_{IL} calculation: It is clear from transfer characteristics curve that (V_{IL}, V_{OHU}) lies in region II. where NMOS → Sat, PMOS → triode.

Using KCL we can write $i_{DP} = i_{DN}$

$$\Rightarrow \cancel{k_p}\left(2(V_{SGP}+V_{TP})V_{SDP} - V_{SDP}^2\right) = \cancel{k_n}\left(V_{GSN}-V_{TN}\right)^2$$

$$\Rightarrow 2(V_{SP}-V_{GP}+V_{TP})(V_{SP}-V_{DP}) - (V_{SP}-V_{DP})^2$$

$$= (V_{GN}-V_{SN}-V_{TN})^2$$



$$\Rightarrow 2(3.3-v_I-0.4)(3.3-v_o) - (3.3-v_o)^2$$

$$= (v_I - 0 - 0.4)^2$$

$$\boxed{\frac{dv_o}{dv_I} = -1}$$

Let, $v_I - 0.4 = X \Rightarrow \boxed{v_I = X + 0.4}$

$3.3 - v_o = Y \Rightarrow \boxed{v_o = 3.3 - Y}$

(X, Y)

$$\Rightarrow 2(3.3-(X+0.4)-0.4)Y - Y^2 = X^2$$

$$\Rightarrow 2(2.5-X)Y - Y^2 = X^2 \Rightarrow \boxed{X^2+Y^2+2XY-5Y=0}$$

$$\frac{dY}{dX} = \cancel{\left(\frac{dY}{dv_o}\right)}^{(-1)}\cancel{\left(\frac{dv_o}{dv_I}\right)}^{(-1)}\cancel{\left(\frac{dv_I}{dX}\right)}^{1} \quad \therefore \boxed{\frac{dY}{dX} = 1}$$

$$\frac{dY}{dv_o} = \frac{d}{dv_o}(3.3 - v_o) = -1 \quad \Big| \quad \frac{dv_I}{dX} = \frac{d}{dX}(X+0.4) = 1$$

Now our task is to find (X, Y) where

$\boxed{X^2+Y^2+2XY-5Y=0}$ equation satisfies $\frac{dY}{dX} = 1$.

$$\frac{d}{dX}(X^2+Y^2+2XY-5Y) = 0$$

$$\Rightarrow 2X + 2Y\frac{dY}{dX} + 2.Y + 2X\frac{dY}{dX} - 5\frac{dY}{dX} = 0$$

$$\Rightarrow 2X + 2Y + 2Y + 2X - 5 = 0$$

$$\Rightarrow \boxed{Y = 5/4 - X}$$

$$\frac{dY^2}{dX} = \frac{dY^2}{dY}\cdot\frac{dY}{dX} = 2Y\cdot\frac{dY}{dX}$$

$$\frac{d}{dx}(fg) = f\frac{dg}{dx} + g\frac{df}{dx}$$

$$\Rightarrow (5/4 - X)^2 + X^2 + 2X(5/4 - X) - 5(5/4 - X) = 0$$

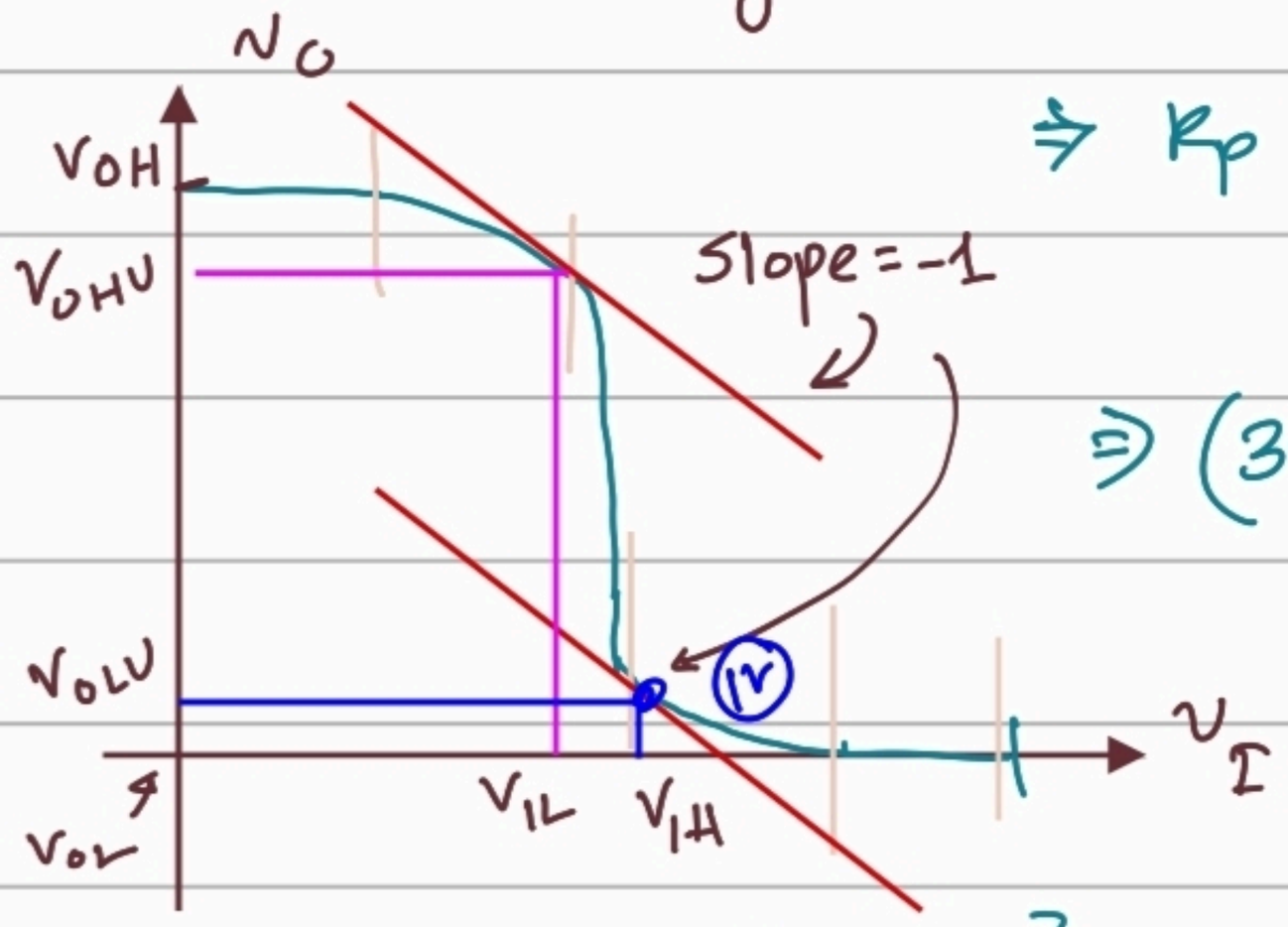
$$\Rightarrow X = \frac{15}{16}, \quad Y = 5/4 - X = 5/16$$

$v_{IL} = v_T = X + 0.4 = 1.3375$, $V_{OHU} = v_o = 3.3 - Y = 2.9875V$

② V_{IH} and V_{OLU} calculation:

For this scenario we have our operating point at region IV, where NMOS is operating in triode and PMOS is operating in saturation.

Using KCL we can deduce, $i_{DP} = i_{DN}$



$$\Rightarrow k_p\left[V_{SGP} + V_{TP}\right]^2 = k_n\left[2(V_{GSN} - V_{TN})V_{DSN} - V_{DSN}^2\right]$$

$$\Rightarrow (3.3 - v_I - 0.4)^2 = 2(v_I - 0.4)v_o - v_o^2$$

Suppose, $X = v_I - 0.4$

$Y = v_o$

$$\Rightarrow (3.3 - (X + 0.4) - 0.4)^2 = 2XY - Y^2$$

$$\Rightarrow \boxed{X^2 + Y^2 - 2XY - 5X + 6.25 = 0} \quad ⓐ$$

$$\frac{dY}{dX} = \frac{dY}{dv_o}\cdot\frac{dv_o}{dv_I}\cdot\frac{dv_I}{dX} = 1.(-1)\cdot 1$$

$$\boxed{\frac{dY}{dX} = -1}$$

$$\Rightarrow 2X + 2Y\frac{dY}{dX} - 2Y - 2X\frac{dY}{dX} - 5 = 0$$

[differentiate w.r.t X]

$$\Rightarrow 2X - 2Y - 2Y + 2X - 5 = 0$$

$$\Rightarrow \boxed{X = Y + 5/4}$$ putting this to eq^n ⓐ

$$(Y + 5/4)^2 + Y^2 - 2(Y + 5/4)Y - 5(Y + 5/4) + 6.25 = 0$$

$$\Rightarrow Y = 0.3125 = v_o = \boxed{v_{OLU} = 0.3125\,V}$$

$$X = Y + 5/4 \Rightarrow v_I = X + 0.4 = \boxed{v_{IH} = 1.9625\,V}$$

$$NM_L = V_{IL} - V_{OLU} = 1.3375 - 0.3125 = 1.025\,V$$

$$NM_H = V_{OHU} - V_{IH} = 2.9875 - 1.9625 = 1.025\,V$$

Noise margin, $NM = \min(NM_L, NM_H)$

$$\boxed{NM = 1.025\,V}$$

Logic circuits using CMOS

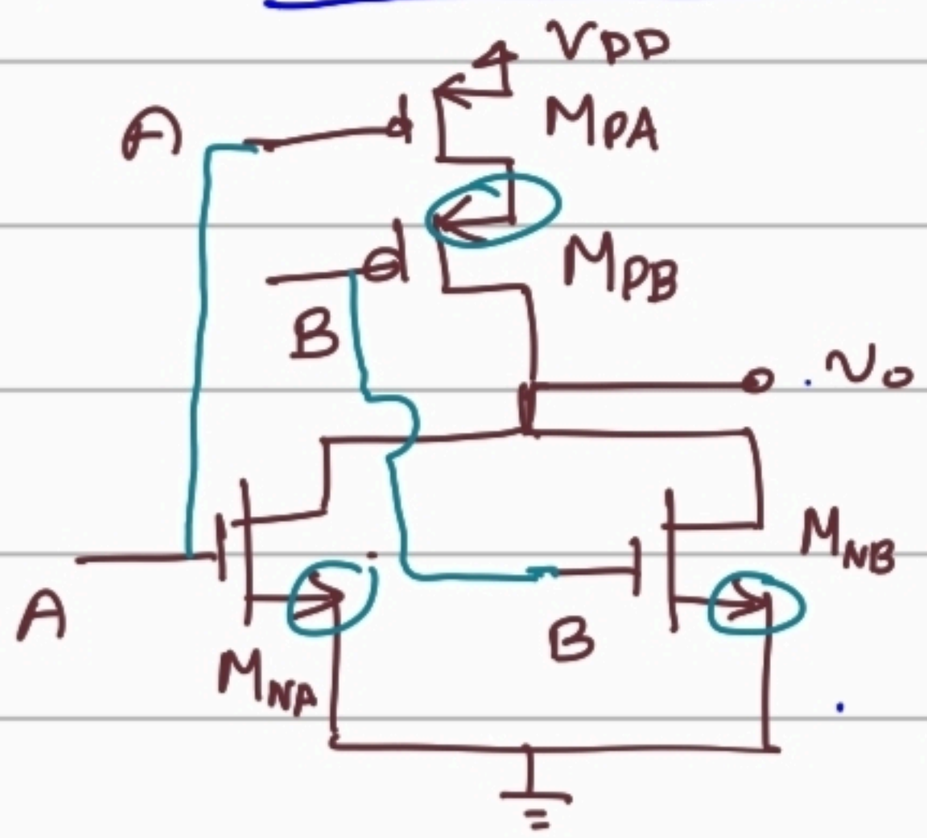
Rule 1: If the gate voltage is high/low then NMOS will turn ON/OFF and PMOS will turn OFF/ON. If any MOSFET turns on then drain and source terminal would be short circuited.

Rule 2: Conduction complement: We will design "pull-up network" using PMOS as the conduction complement of "pull-down network" using CMOS.

- Conduction complement means if NMOS are in series/parallel connection then PMOS are going be in parallel/series.
- Pull-up network rises the output level to the logical high voltage.
- Pull down networks declines the output level to the logical low voltage.

Example: CMOS NOR GATE:

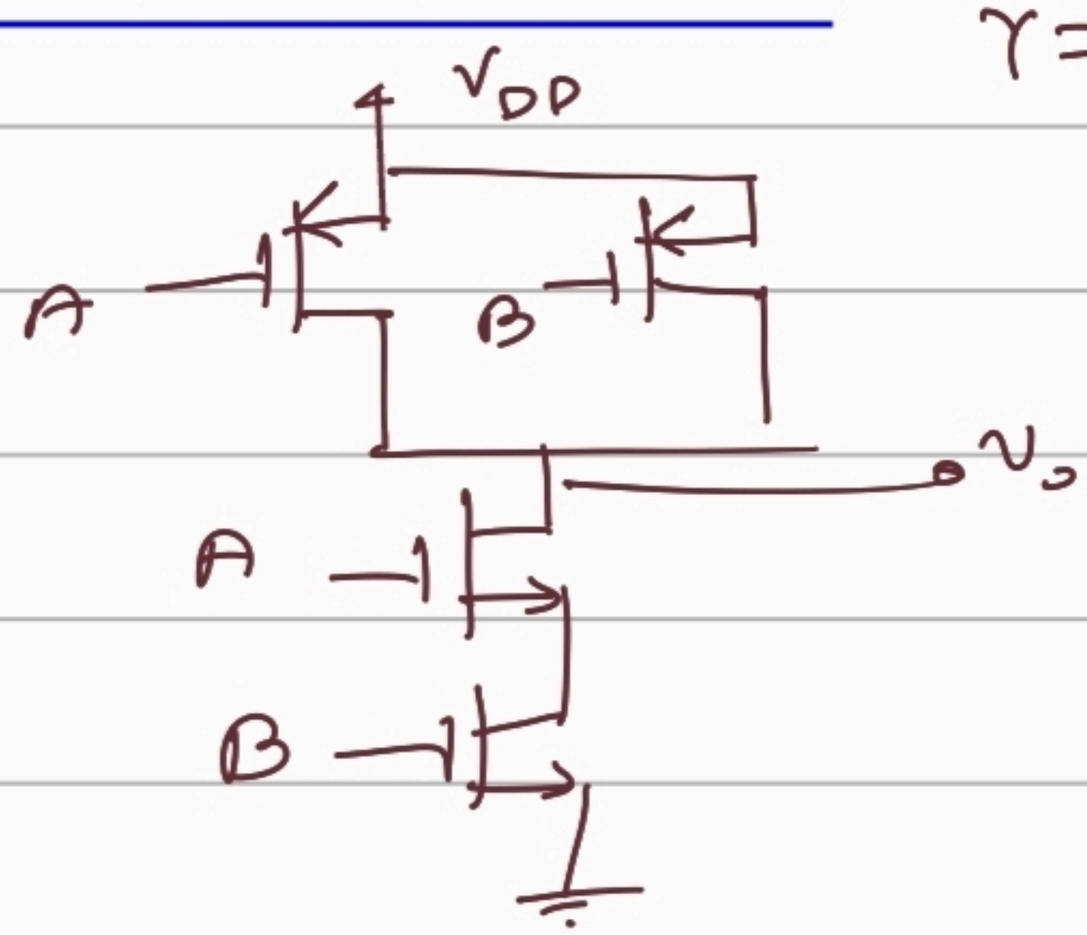
$$Y = \overline{A+B}$$



A	B	M_{PA}	M_{PB}	M_{NA}	M_{NB}	v_o
0	0	ON	ON	OFF	OFF	V_{DD}
0	V_{DD}	ON	OFF	OFF	ON	0
V_{DD}	0	OFF	ON	OFF	ON	0
V_{DD}	V_{DD}	OFF	OFF	ON	ON	0

CMOS NAND GATE

$Y = \overline{AB}$



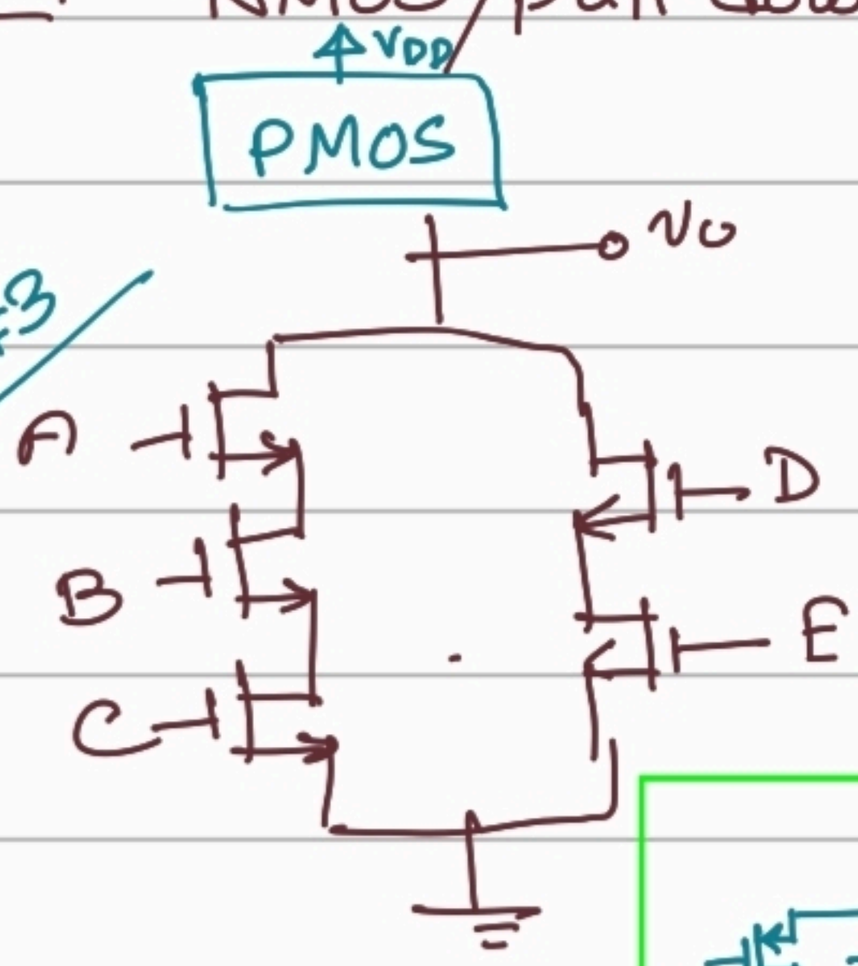
You can easily verify this works like a NAND gate.

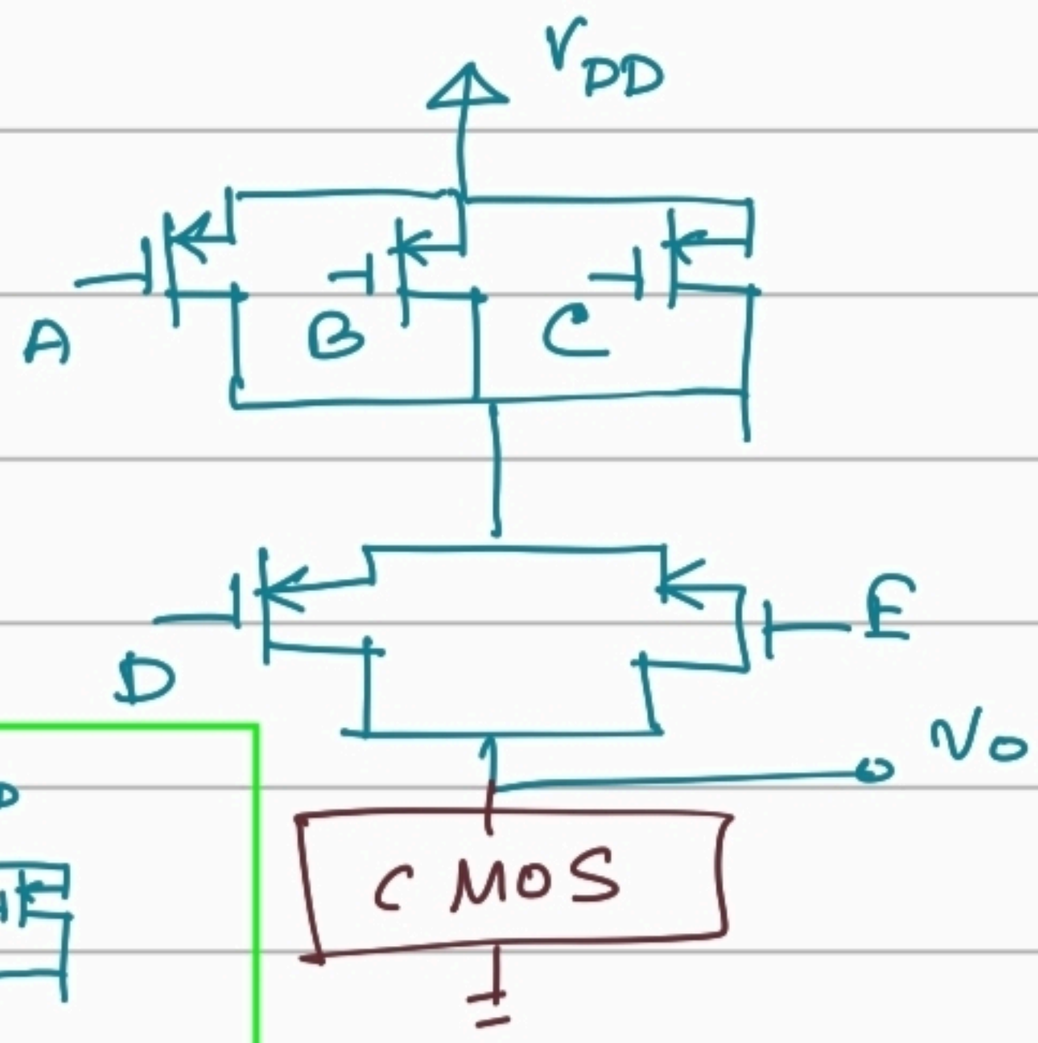
#Rule 3 : In order to design pull-down network we must use series NMOS connection for AND logic and parallel NMOS connection for OR logic under the whole inverse sign.

Example: $Y = \overline{ABC + DE}$

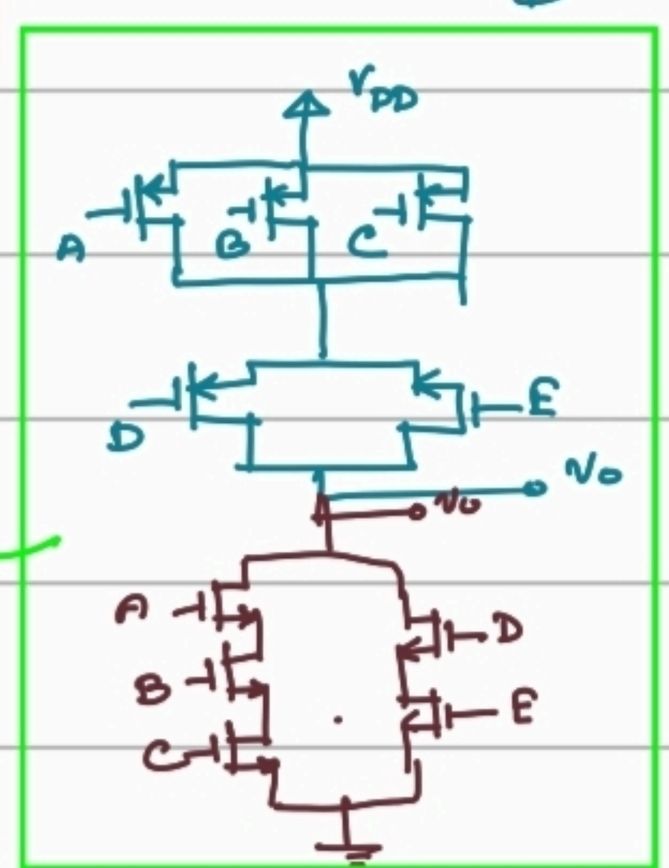
Sol^n: NMOS/pull down network:

using Rule #3





Total circuit.

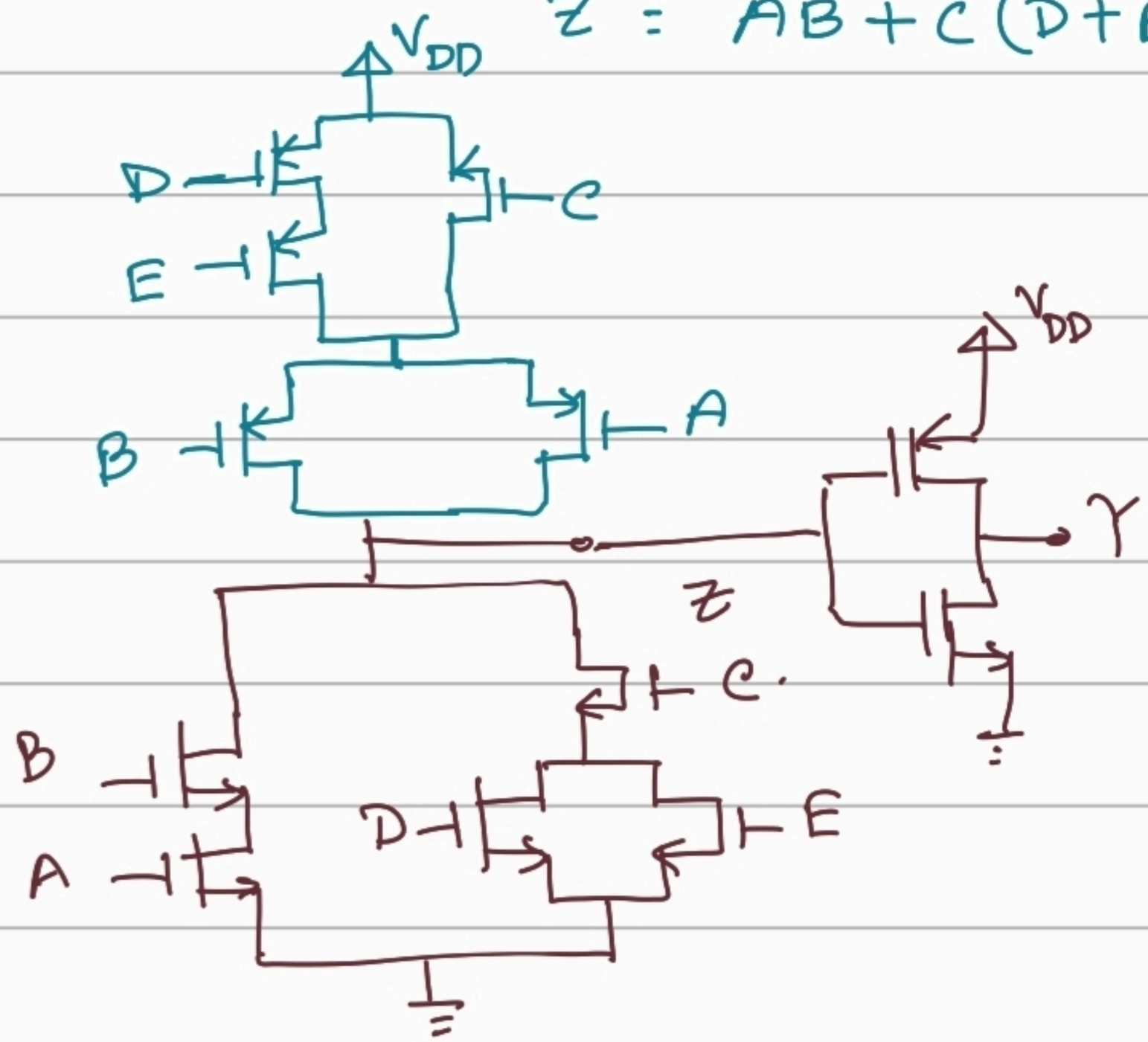


Example: 16.11

$$Y = AB + C(D+E)$$

$$Y = \overline{Z}$$

$$Z = \overline{AB + C(D+E)}$$



Switching up series connections doesn't change output.

April - 16, Quiz 4. Question has been announced.

"NMOS NOR gate with DEPLETION LOAD"

Lecture 16: ADC and DAC.

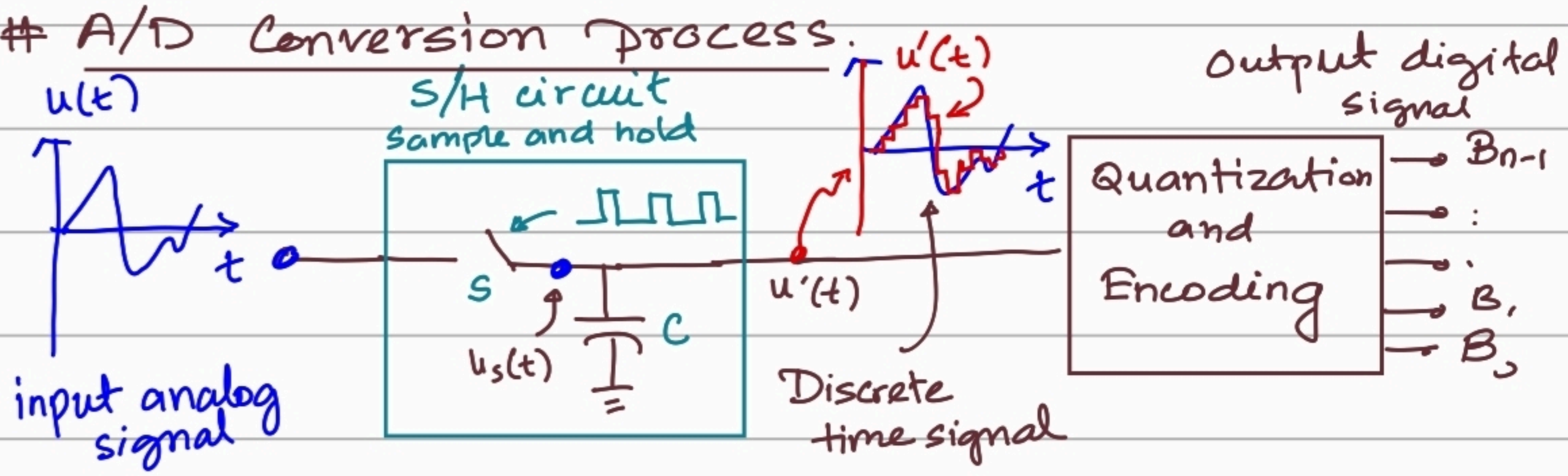
Physical world's informations are analog. Analog means data could take any real value at each instant of time.

In order to store/process we use digital data in our computers and microprocessor. Digital data means binary bit of strings.

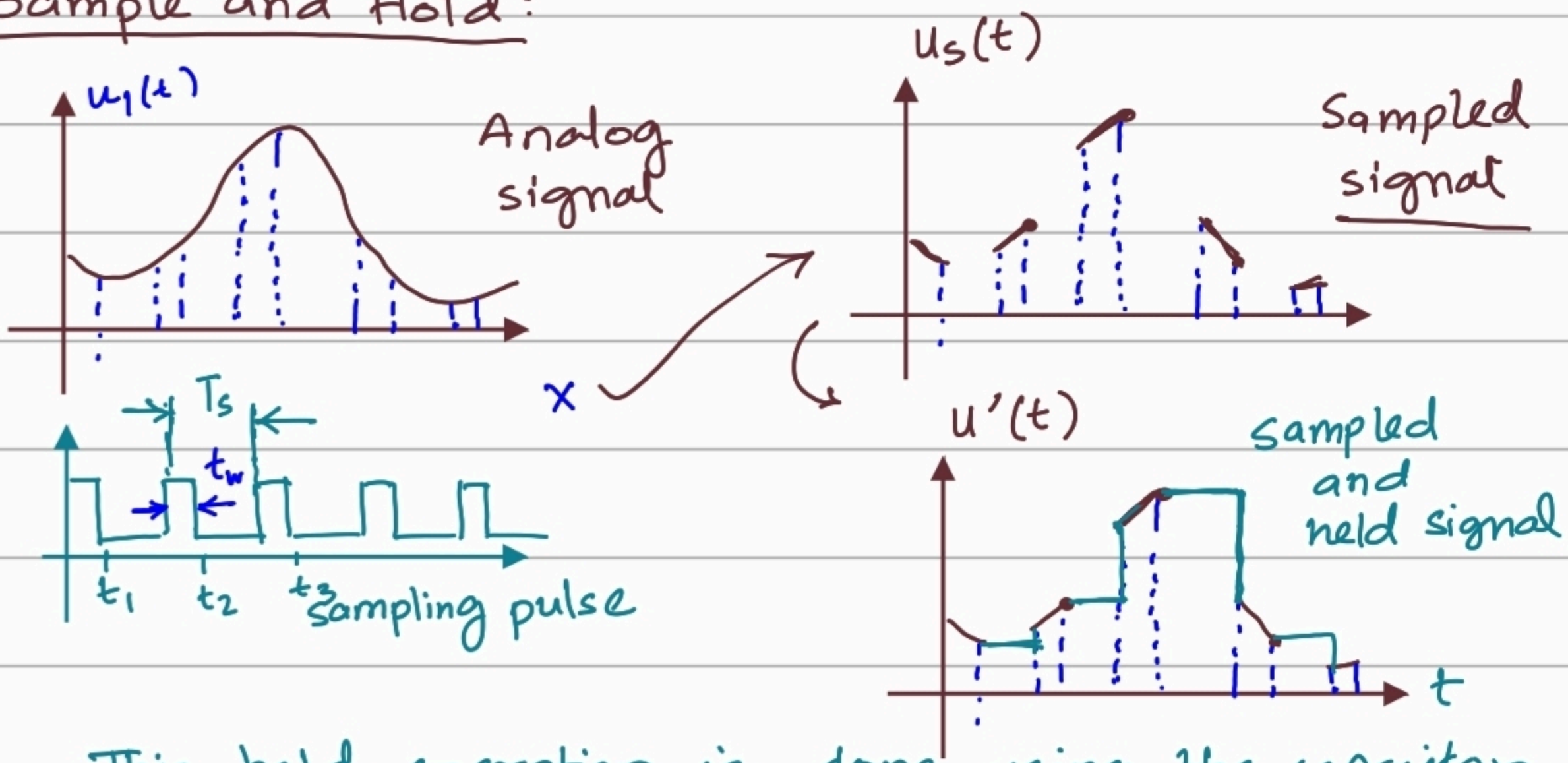
Environment → Transducer → Computer → speaker

A/D D/A

A/D Conversion Process.



Sample and Hold:



This hold operation is done using the capacitor.

Quantization:

Quantization is process by which we assign sampled and hold signal data to some fixed preassigned values.

N = number bits we want as digital output

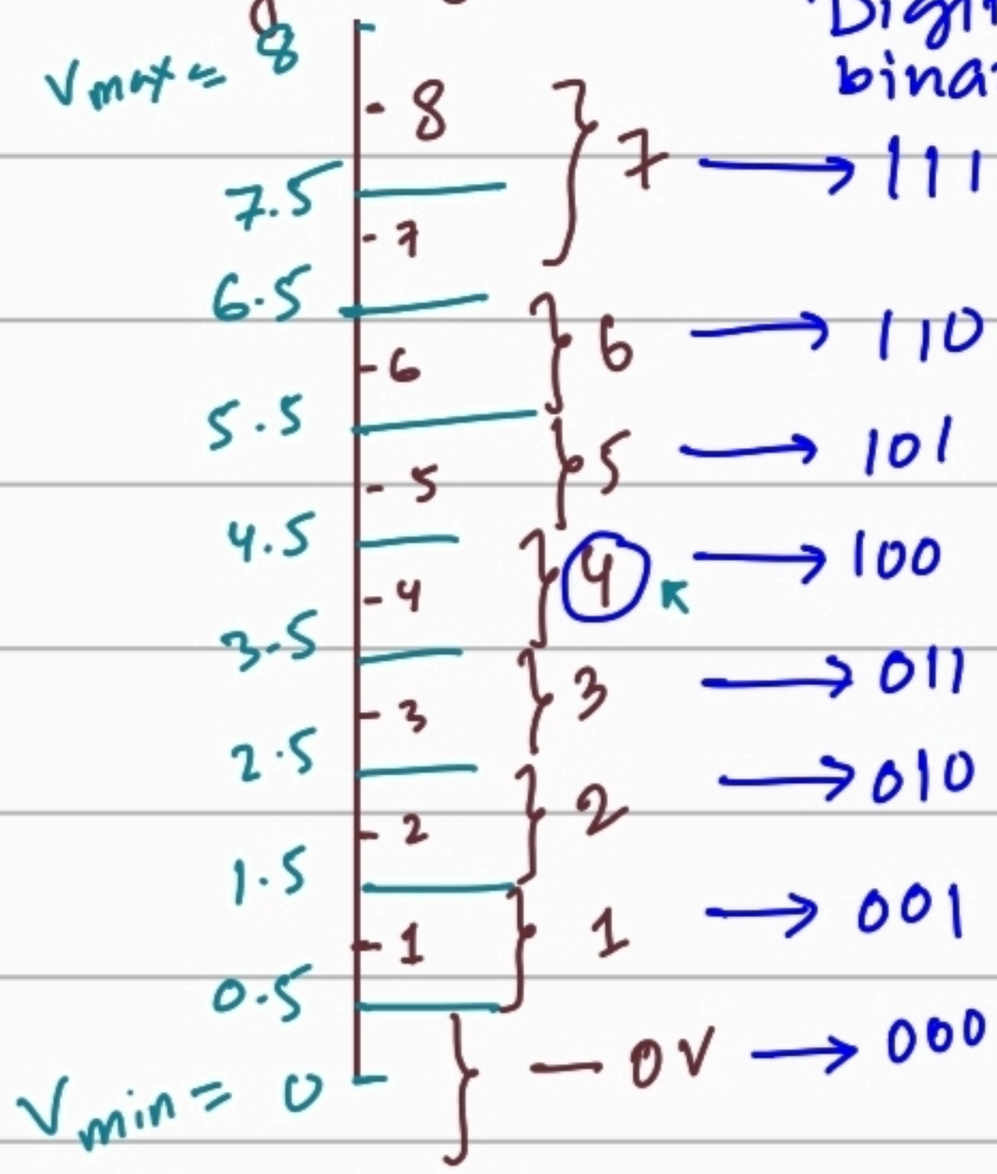
Δ = resolution $= \dfrac{V_{max} - V_{min}}{2^N}$

2^N = number of levels.

V_{max} / V_{min} = maximum/minimum possible value of analog signal.

Encoding: We can choose binary values for each quantized levels.

Analog signal.



$\dfrac{V_{max} + V_{min}}{2} = 4$

4 V is a quantization level so it is actually midtread quantization.

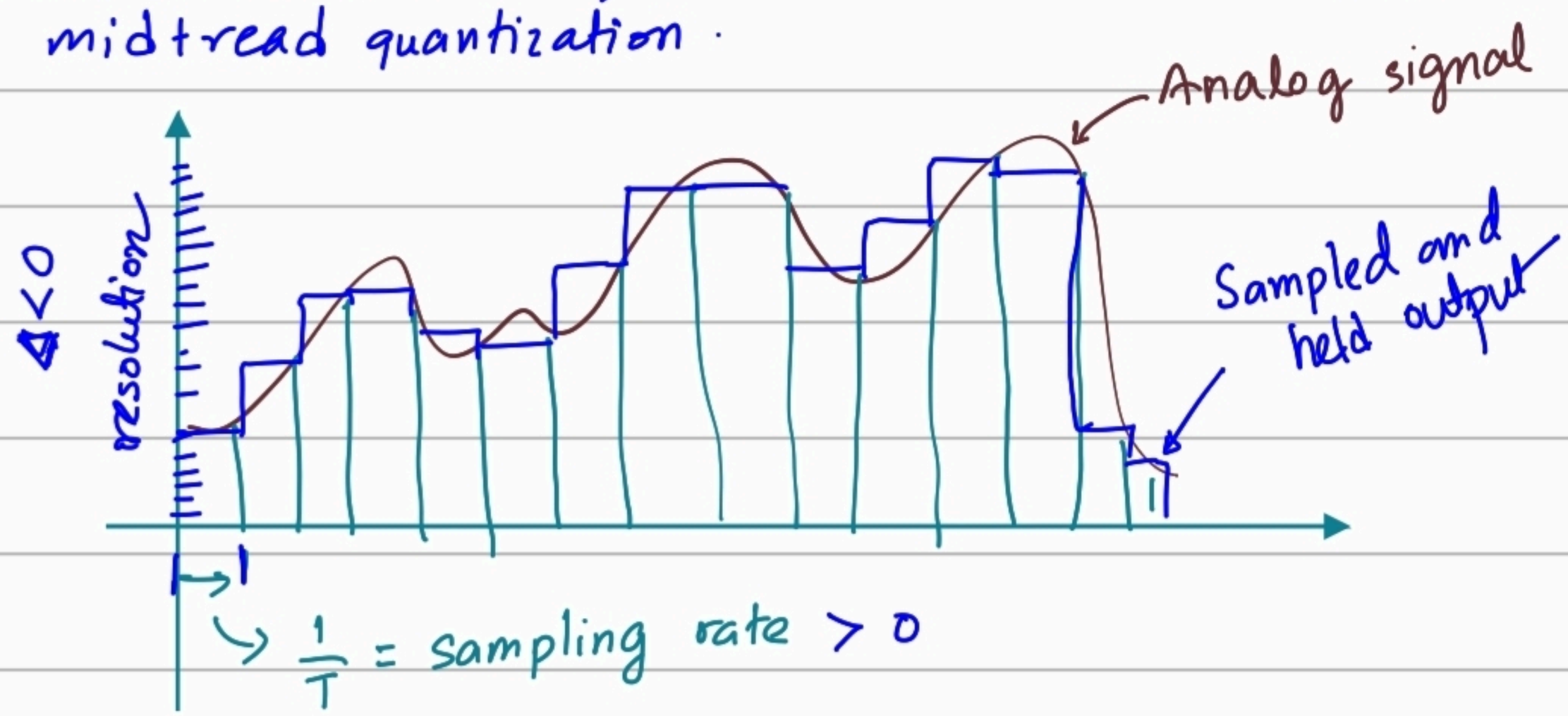
$N=3, 2^N=8$

Midrise quantization

$V_{max} = 10V, \quad V_{min} = 0V$

000	0 – 1.25V	→ 0.675	Δ 1.25
001	1.25 – 2.5	→ 1.875	
010	2.5 – 3.75	→ 3.125	
011	3.75 – 5.0	→ 4.375	
100	5.0 – 6.25	→ 5.625	
101	6.25 – 7.5	→ 6.875	
110	7.5 – 8.75	→ 8.125	
111	8.75 – 10.0	→ 9.375	

$\dfrac{V_{min} + V_{max}}{2} = 5V$ ↑ Voltage levels



Flash A/D Converter:

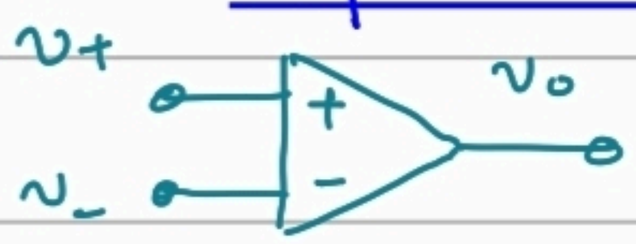
Ad. # This converter is very fast. It requires one clock cycle to convert the analog to digital data.

Dis. # It requires a lot component.

$N = 3.\ 2^N = 8$

Midrise quantization:

Comparators



$v_+ > v_-$, v_o = High ✓

$v_+ < v_-$, v_o = Low ✓

$V^+_{ref} = 9.375\,V$

$V^-_{ref} = -0.675\,V$

$I = \left(\frac{V^+_{ref} - V^-_{ref}}{8R}\right) = \frac{10}{8R}$

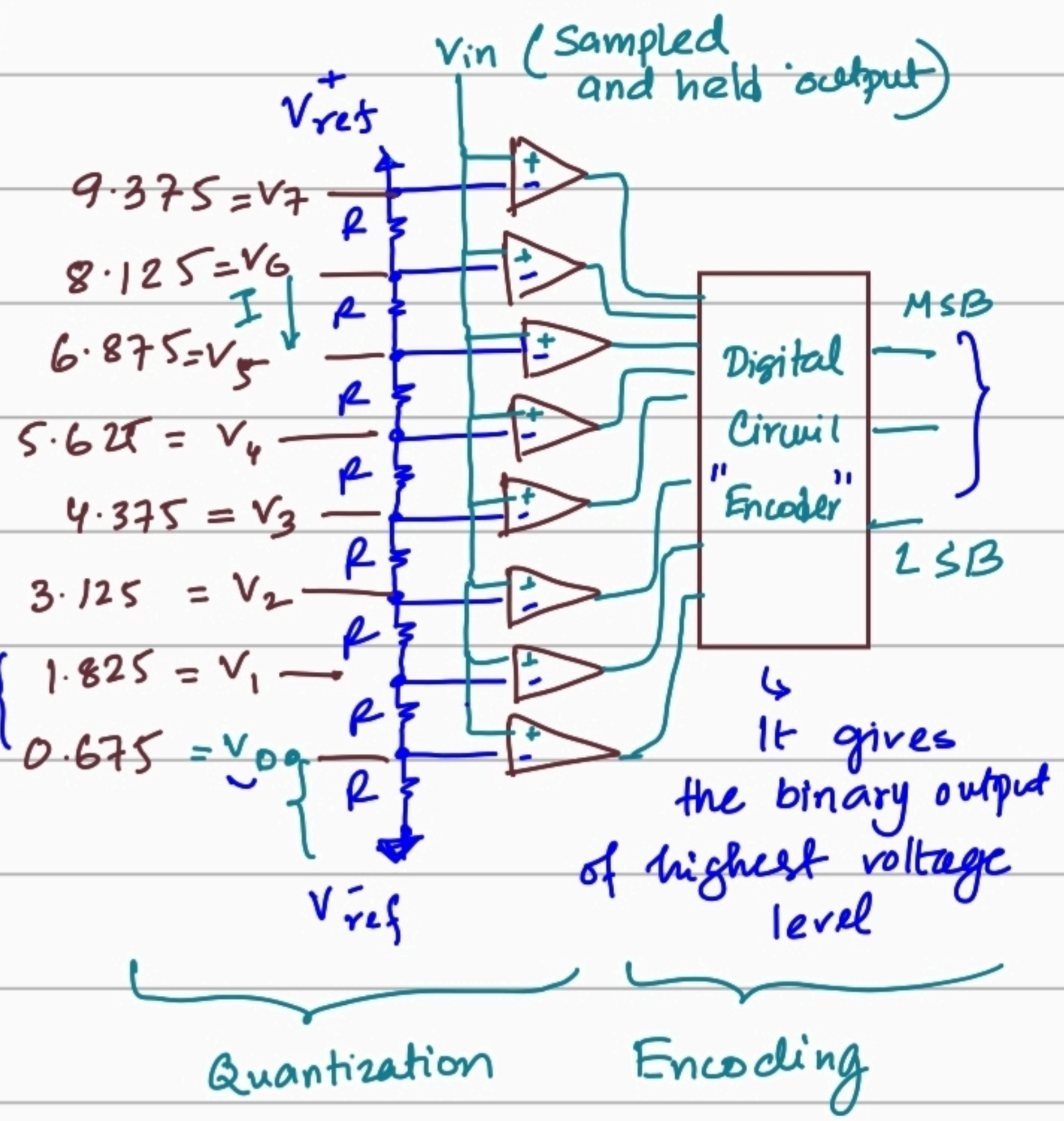
$IR = v_o - V^-_{ref}$

$\Rightarrow v_o = V^-_{ref} + IR$

$= -0.675 + \frac{10}{8}$

$= 0.675$

$V_1 = V_o + IR = 1.825\,V$ ✓

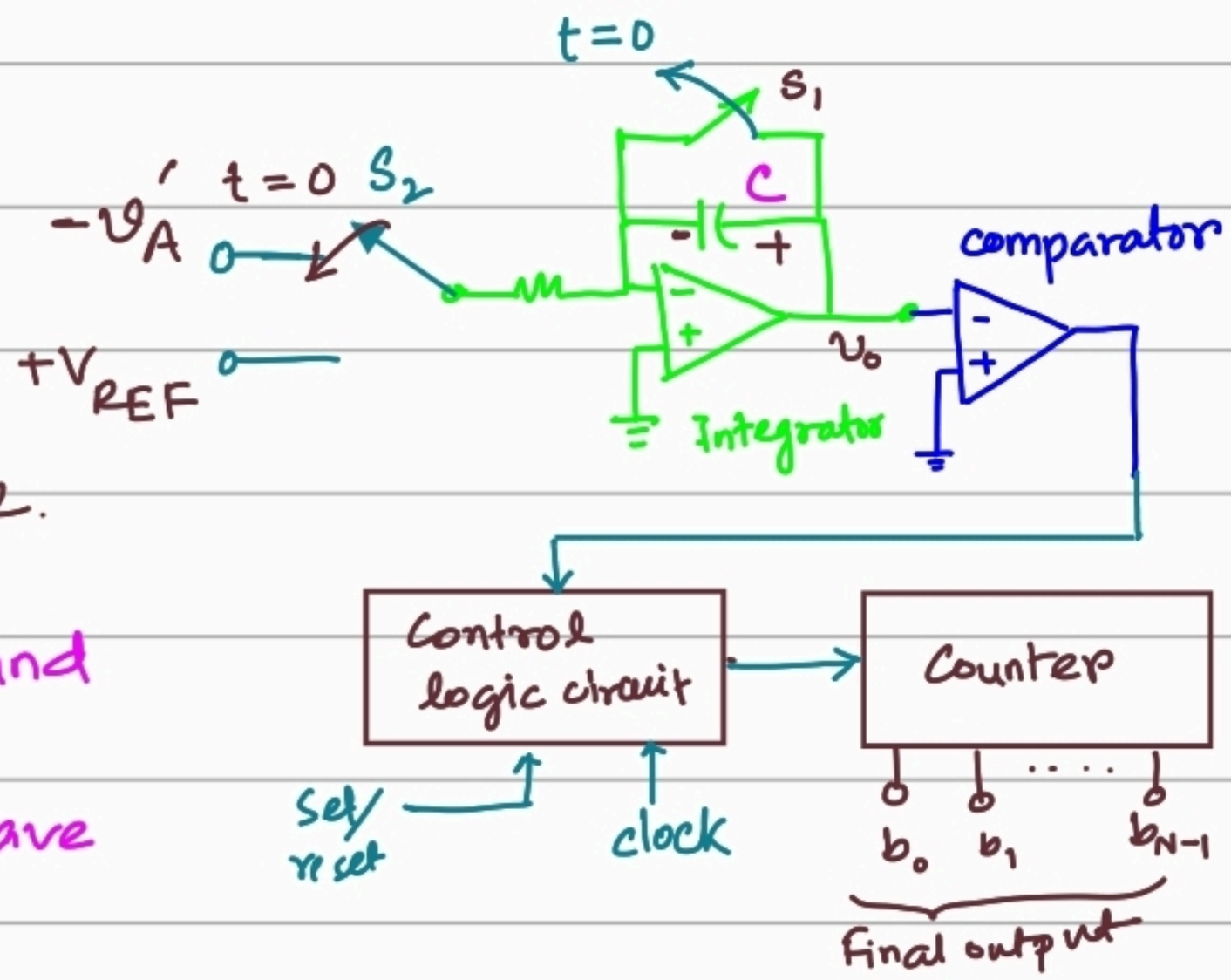


Dual Slope converter:

Adv: It requires small amount of circuit components. We can use many levels for quantization.

Disadvantage: Relatively slow.

Circuit:



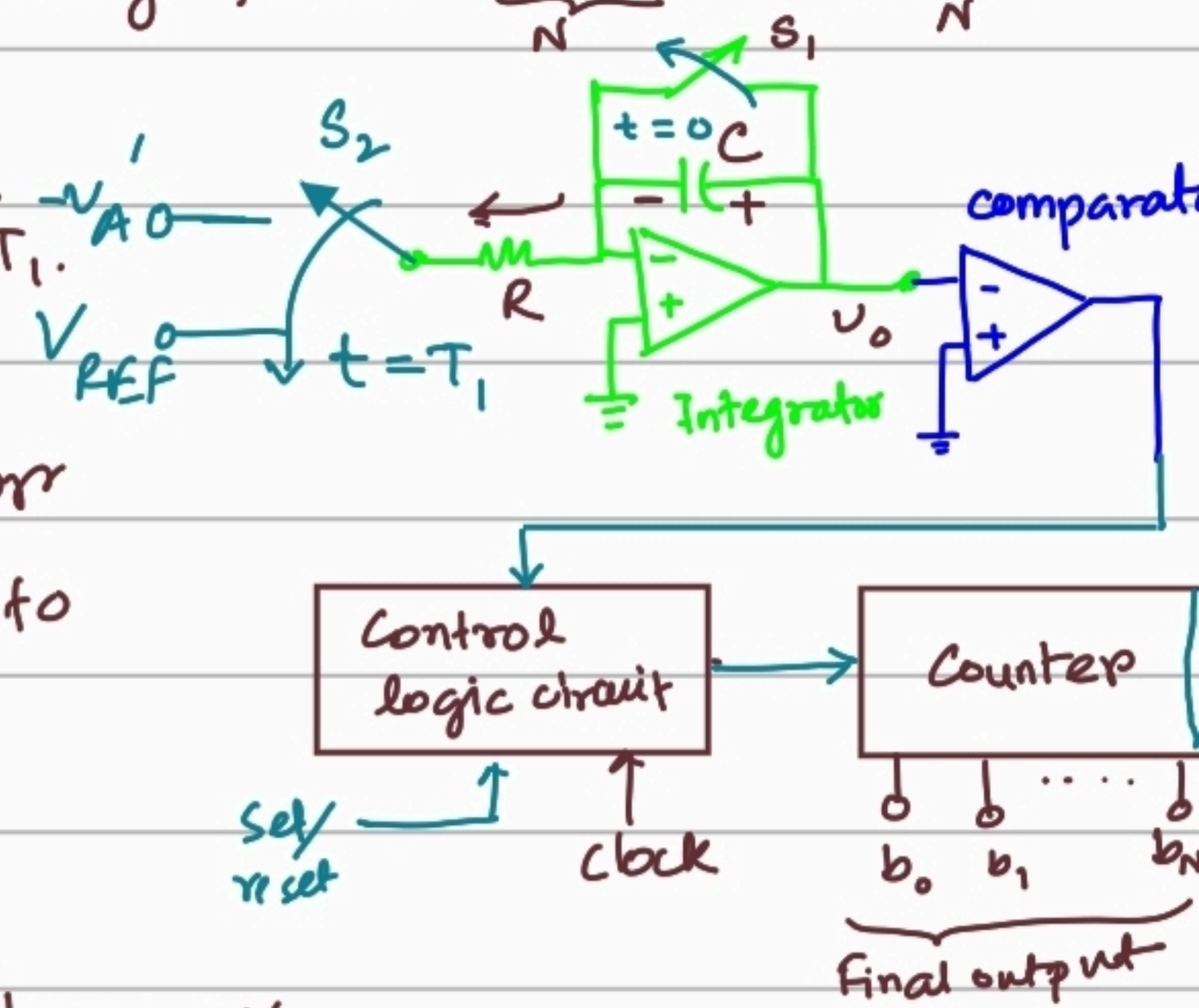
v_A' = Sampled and held signal

V_{REF} = preassigned value.

- $(t<0)$ S_1 is closed and S_2 is open.
  # Capacitor doesn't have any charge.

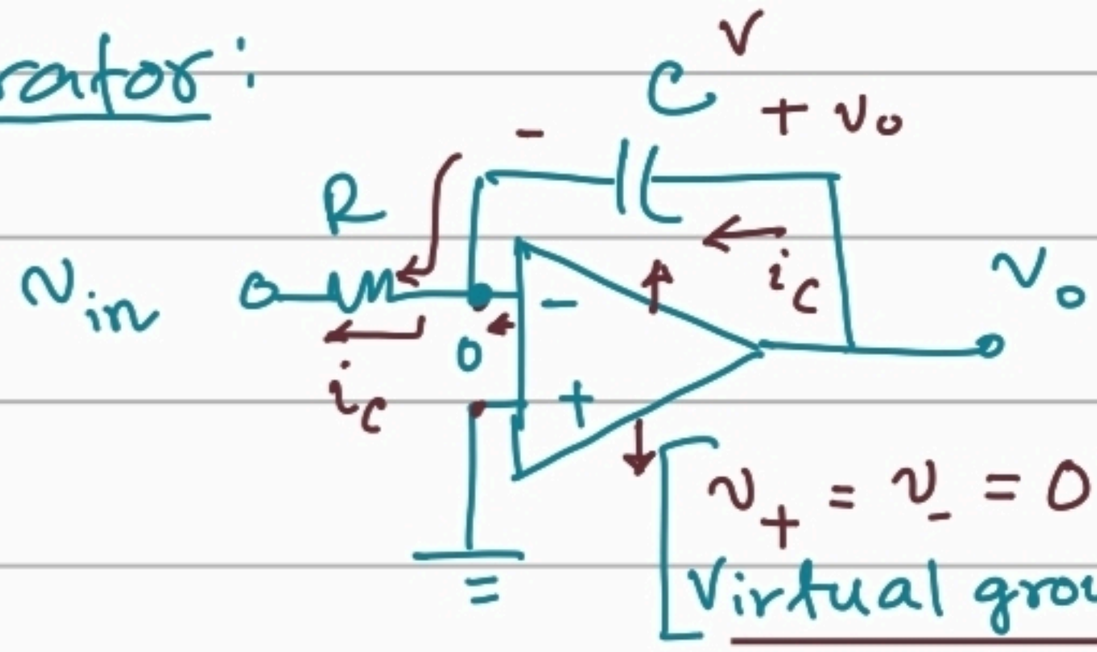
- $t=0$, S_1 is open. S_2 is now connected to v_A'.
  capacitor is charging in a way that v_o increases.
  counter starts counting from $\underbrace{000..0}_{N}$ to $\underbrace{1111\ 1}_{N}$.

- $t \geq T_1$. Counter finishes counting from 0 to 2^N-1. at $t=T_1$.
  S_2 is now connected to V_{REF}. From then capacitor discharges and v_o starts to decline.



- $t = T_2$ (not fixed time)
  v_o output level decreases below 0V.
  Now comparator output changes from low to high.
  At that moment control circuit stops the counter
  Then the output of the counter is the digital output we want.

Integrator:



$v_+ = v_- = 0V$
Virtual ground

Q = stored charge in capacitor.

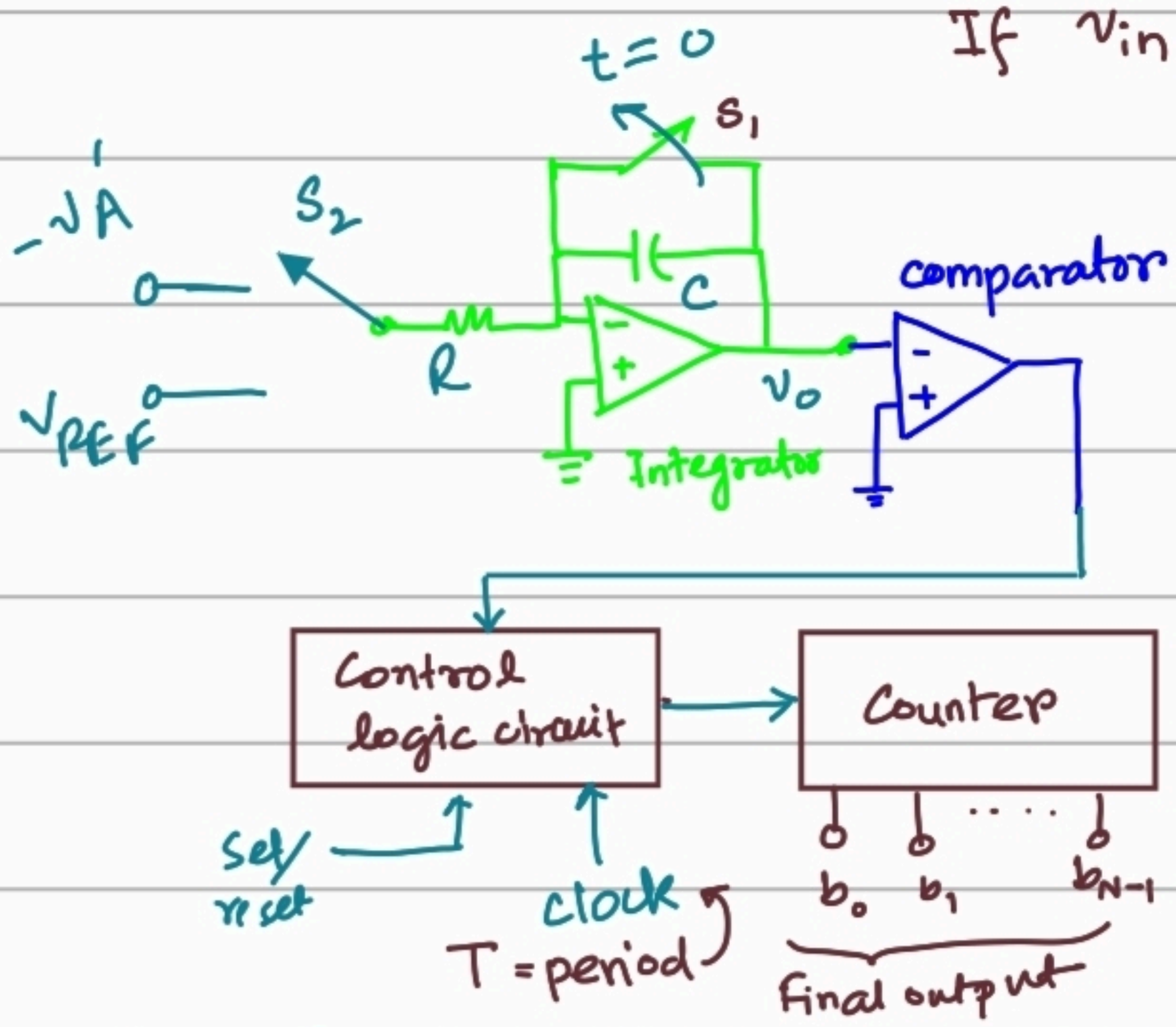
$v_o = V =$ voltage across the capacitor.

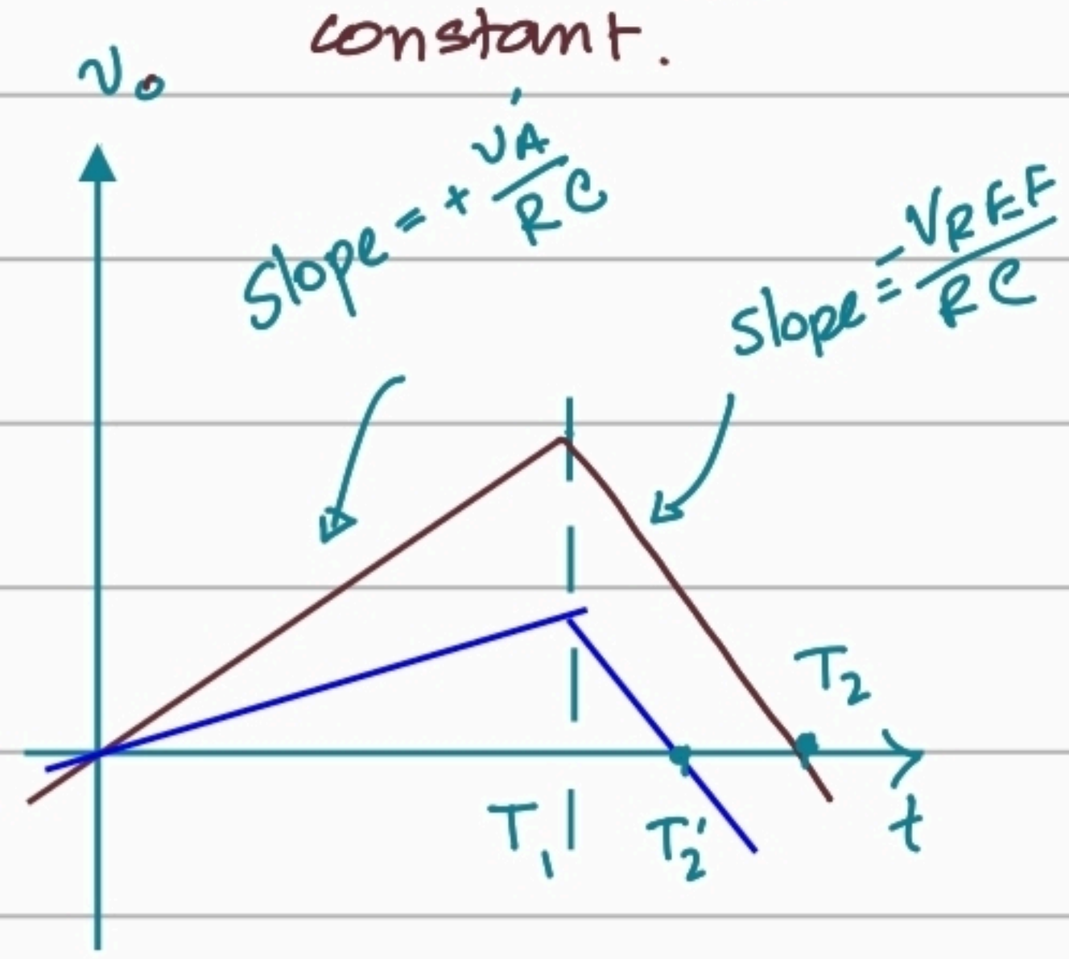
$Q = CV$

$\therefore \frac{dQ}{dt}$ = current through the capacitor

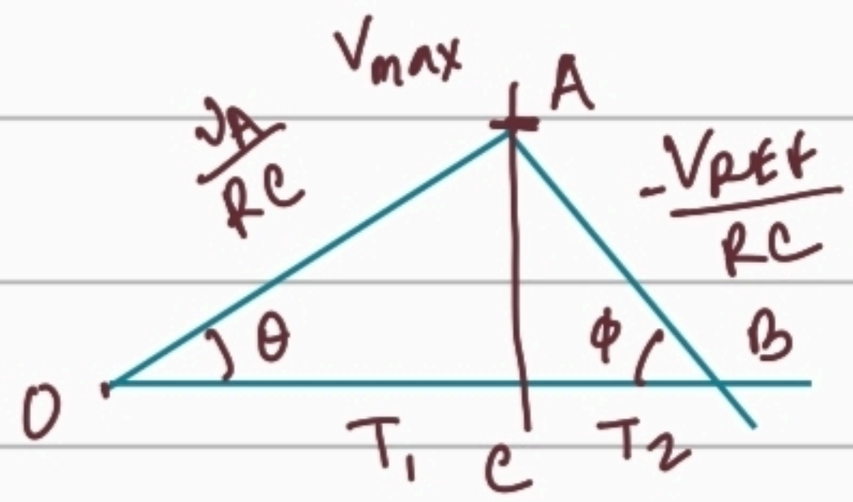
$$= C \cdot \frac{dV_o}{dt} = i_c = \frac{0 - v_{in}}{R} \Rightarrow \boxed{\frac{dV_o}{dt} = -\frac{v_{in}}{RC}}$$

If v_{in} is constant then $\frac{dv_o}{dt}$ is constant.





Say final output is binary representation of the number n.



$$\tan\theta = \frac{V_A}{RC} = \frac{AC}{OC} = \frac{V_{max}}{T_1}$$

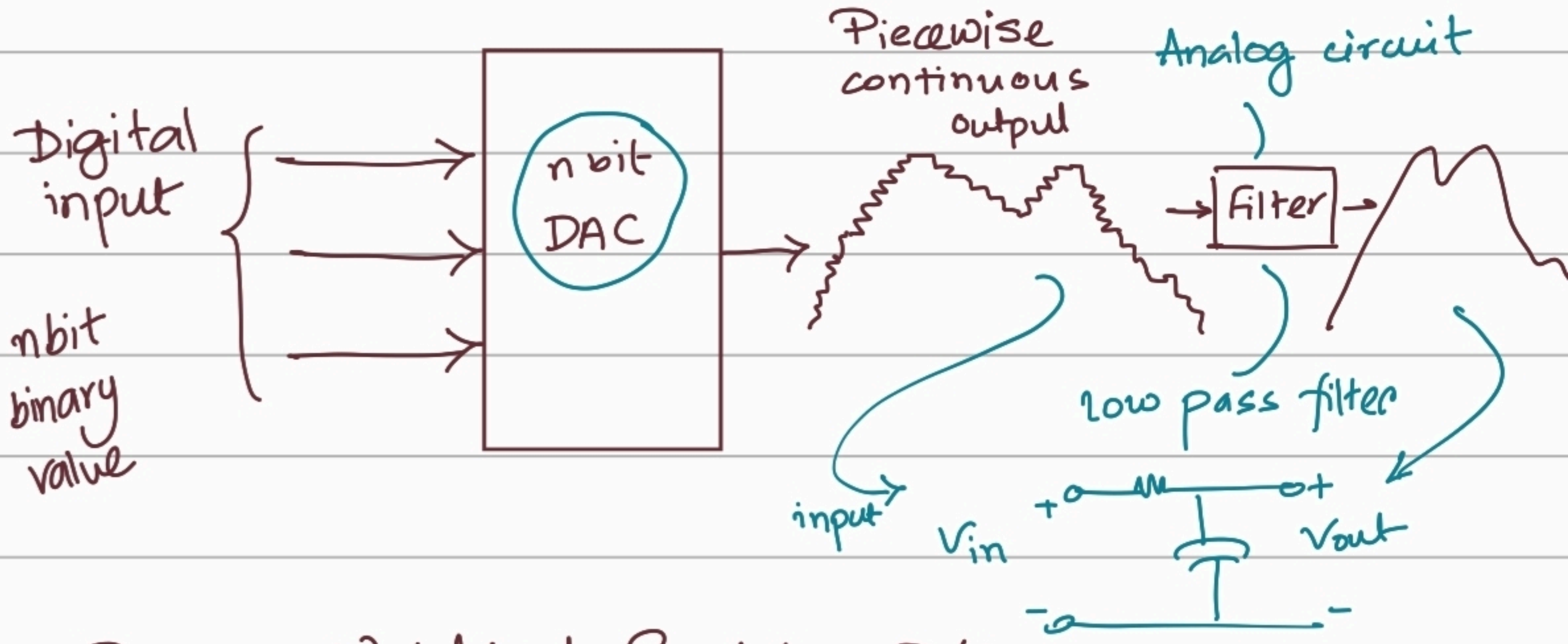
$$\tan\phi = \frac{V_{REF}}{RC} = \frac{AC}{BC} = \frac{V_{max}}{T_2}$$

$$\frac{V_{max}/T_1}{V_{max}/T_2} = \frac{V_A}{V_{REF}} = \frac{T_2}{T_1} = \frac{nT}{2^N T}$$

$$\boxed{n = V_A \frac{2^N}{V_{REF}}} \Leftarrow \boxed{V_A = \frac{n}{2^N} V_{REF}}$$

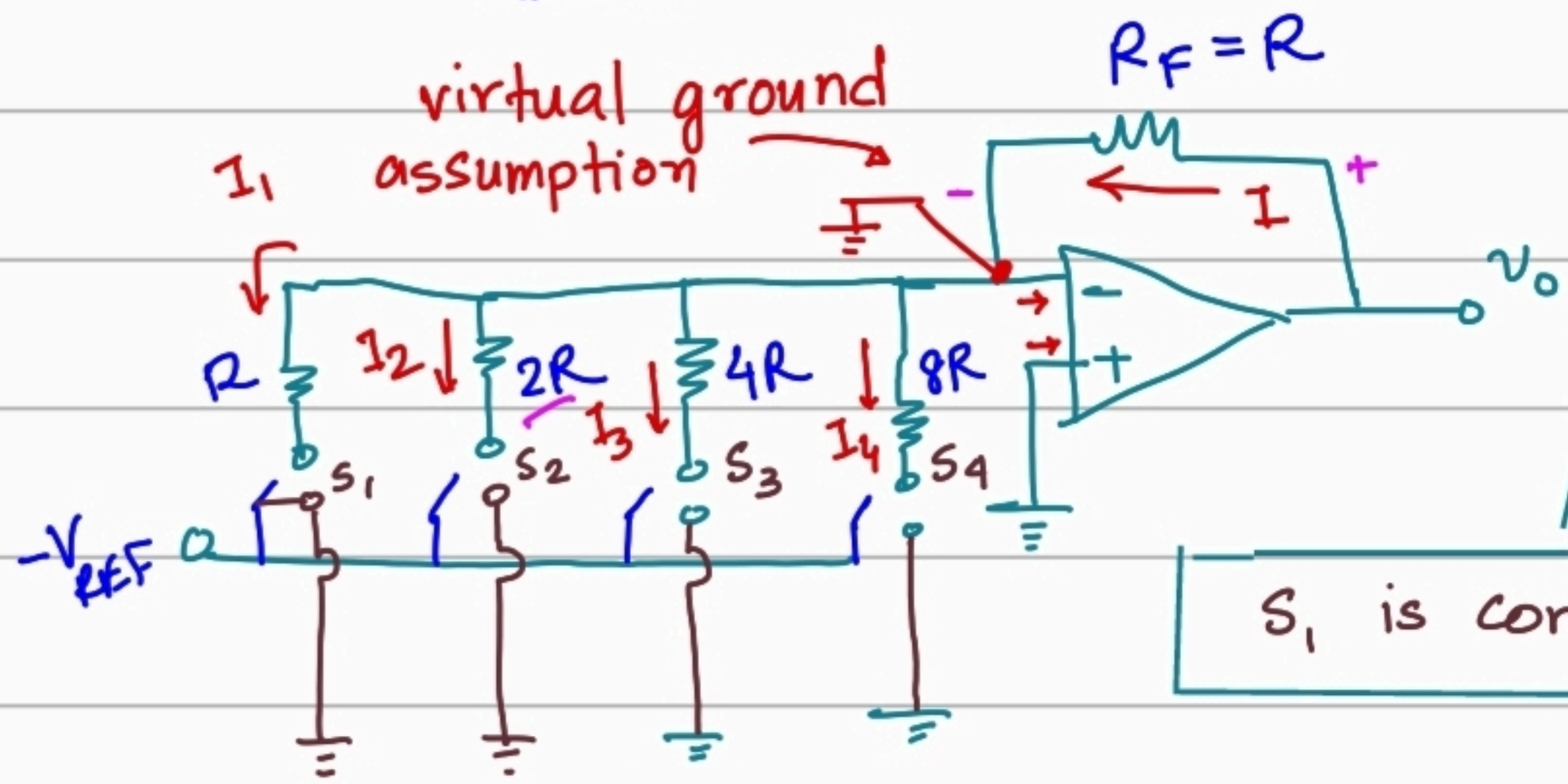
Lecture 17: D/A and A/D converter

Digital to Analog Conversion



Binary Weighted Resistor D/A

4 bit



Input: $b_1 b_2 b_3 b_4$

4 bit string

If b_1 is 1, S_1 is connected to the resistor, if b_1 is 0, S_1 is connected to ground.

Same rules applies to S_2, S_3 and S_4.

$$I = I_1 + I_2 + I_3 + I_4 = \frac{V_o - 0}{R_F} = \frac{V_o}{R_F}$$

	I_1	I_2	I_3	I_4
switch is connected to resistor	$\frac{0-(-V_{REF})}{R} = \frac{V_{REF}}{R}$	$\frac{V_{REF}}{2R}$	$\frac{V_{REF}}{4R}$	$\frac{V_{REF}}{8R}$
switch is connected to ground	0 because the path is open	0	0	0

$$\frac{v_o}{R_F} = b_1 \frac{V_{REF}}{R} + b_2 \frac{V_{REF}}{2R} + b_3 \frac{V_{REF}}{4R} + b_4 \frac{V_{REF}}{8R}$$

$$\Rightarrow \boxed{v_o = V_{REF}\left(b_1 + b_2/2 + b_3/4 + b_4/8\right)}$$

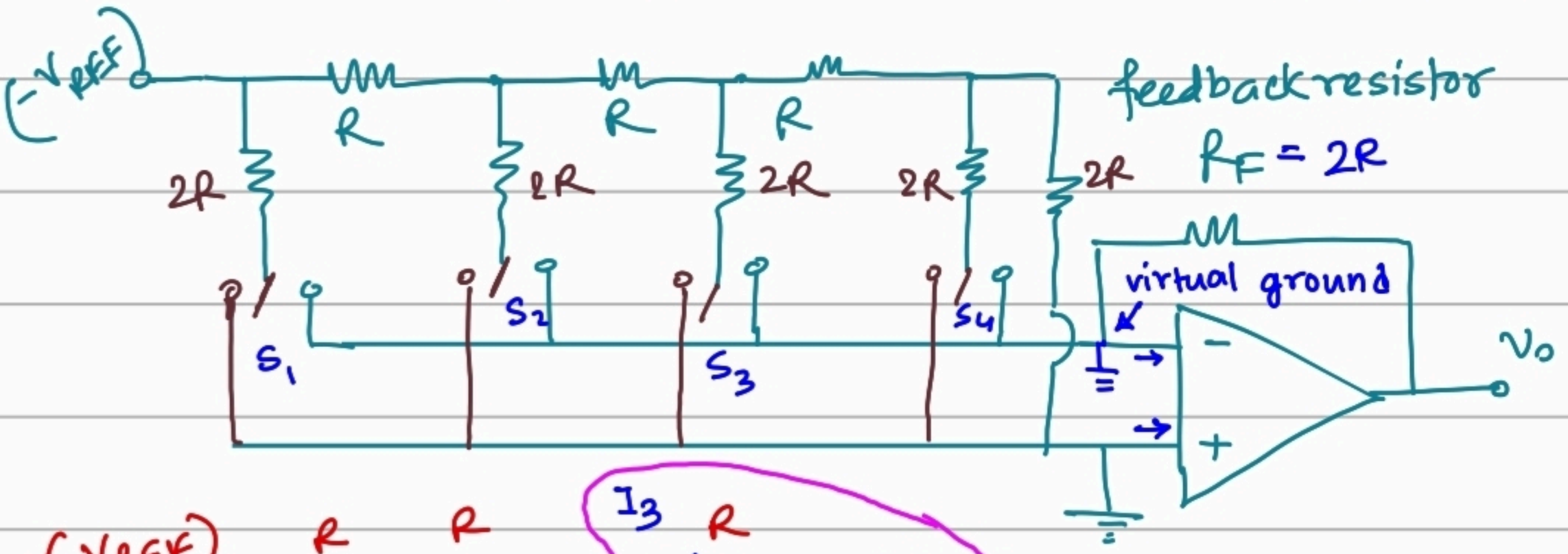
Design 6 bit BWR D/A where $V_{max} = 10V$.

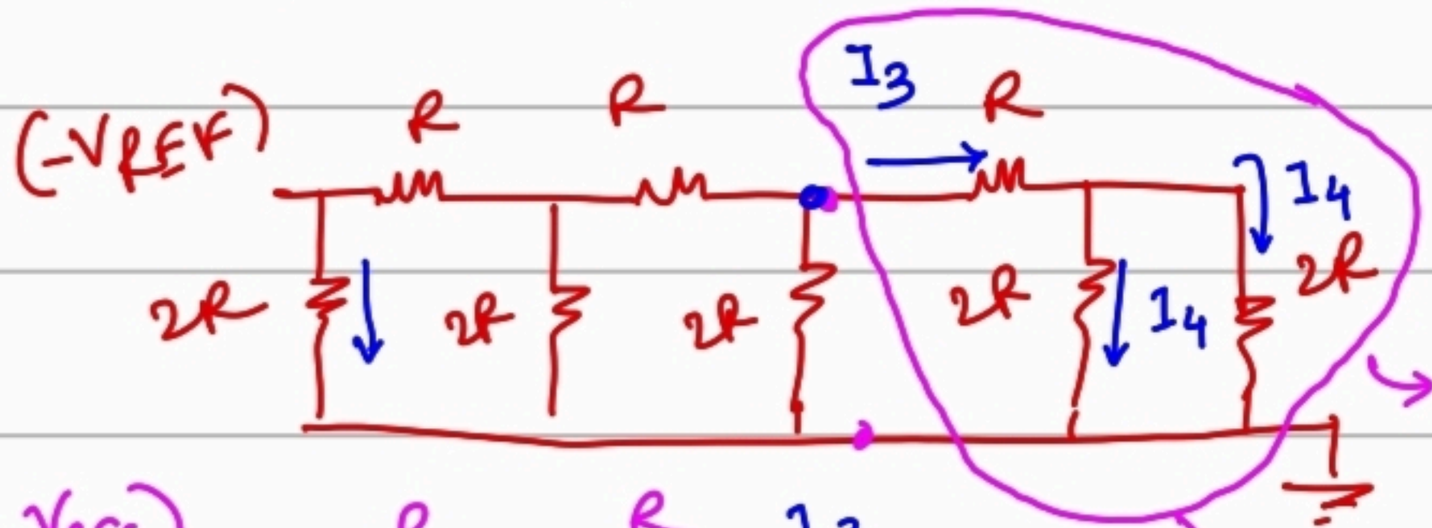
$$v_o = V_{max} = V_{REF}\left(1 + \tfrac{1}{2} + \tfrac{1}{4} + \tfrac{1}{8} + \tfrac{1}{16} + \tfrac{1}{32}\right)$$

$V_{REF} \approx 5V$

Dis: Output is dependent on value of the resistors and it is hard to find resistor in this much variations.

R-2R ladder: 4 bit R-2R Ladder

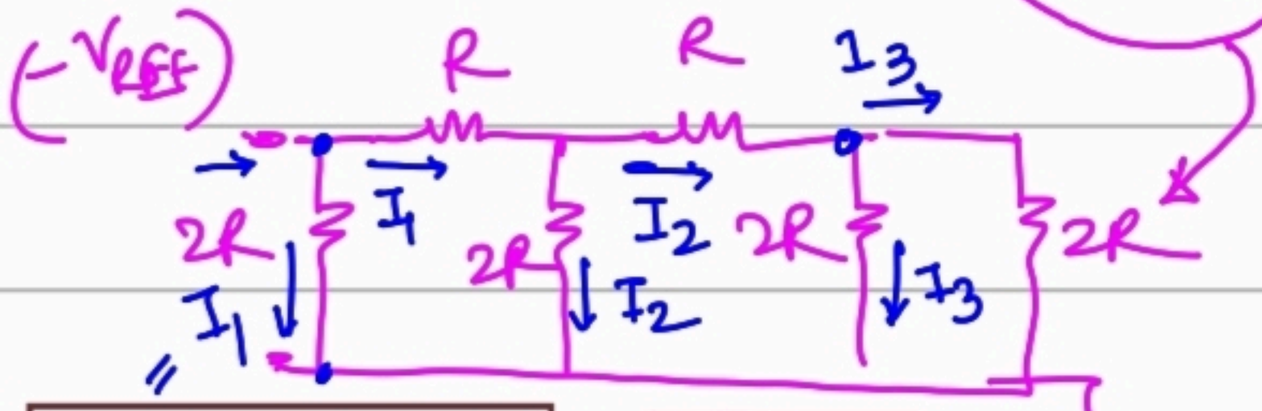




$2I_4 = I_3$

equivalent resistance

$(2R \| 2R) + R = 2R$

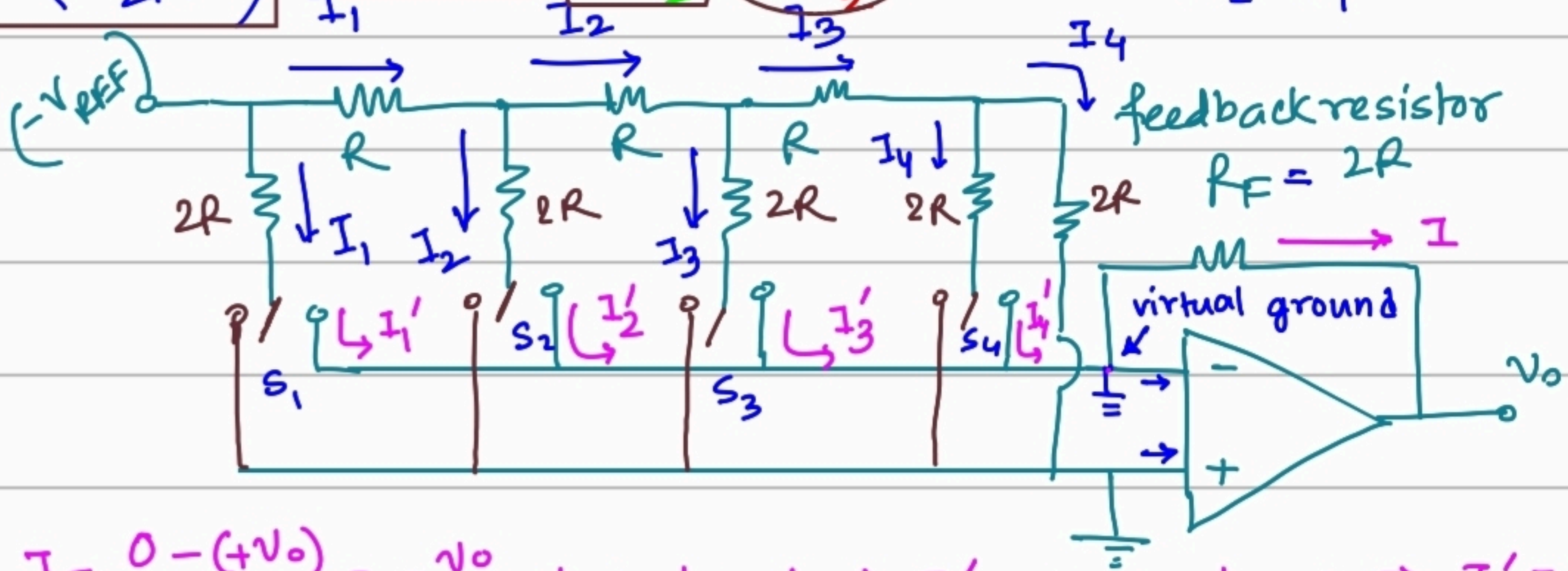


$2I_3 = I_2$

Similary if we continue this arguments, then we will get,

$2I_2 = I_1$

$$\boxed{I_1 = \left(\frac{-V_{REF} - 0}{2R}\right)} \cdot \boxed{I_2 = \frac{I_1}{2}} \cdot \boxed{I_3 = \frac{I_2}{2}} \cdot I_4 = \frac{I_3}{2}$$



$$I = \frac{0 - (+v_o)}{R_F} = -\frac{v_o}{R_F}, \text{ here } b_1 = 1 \Rightarrow I_1' = I_1 \text{ or } b_1 = 0 \Rightarrow I_1' = 0.$$

So $I_1' = b_1 I_1$, similarly $I_2' = b_2 I_2$, $I_3' = b_3 I_3$, $I_4' = b_4 I_4$

Thus. $I = I_1' + I_2' + I_3' + I_4' = b_1 I_1 + b_2 \frac{I_1}{2} + b_3 \frac{I_1}{4} + b_4 \frac{I_1}{8}$

$$I = -\frac{v_o}{\cancel{R_F}\ 2R} = I_1\left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8}\right) = -\frac{V_{REF}}{2R}\left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8}\right)$$

$$\Rightarrow \boxed{v_o = V_{REF}\left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8}\right)}$$

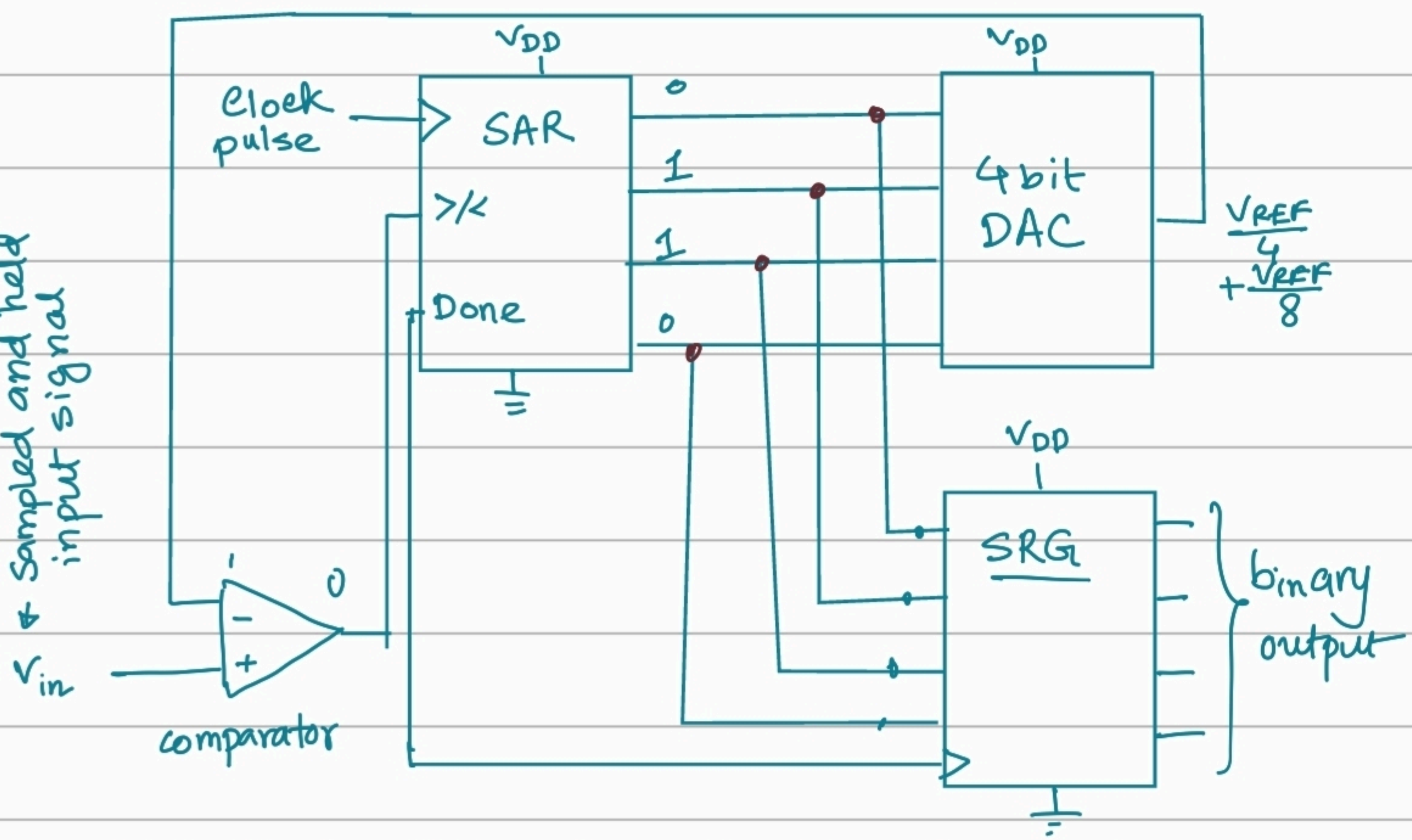
Performance specifications.

1. Resolution (Δ) [Homework, chapter 16 Neamen]
2. Reference voltage
3. Settling time
4. Linearly
5. Speed
6. Error

Successive Approximation ADC

* It requires less components compared to flash A\D and it is very faster compared to dual slope A\D.

Binary search is the main working principle here.



SAR → Successive Approximation Register

SRG → Shift resister generator

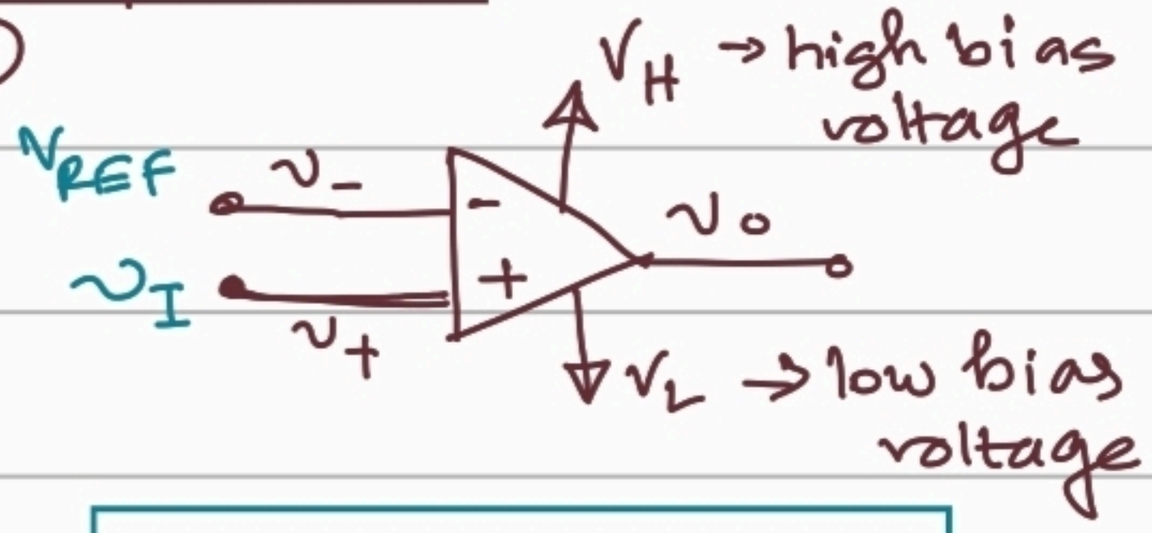
Example: 10 bit SADAC problem (See Homework 7 also).

Lecture 18: Schmitt Trigger Circuit

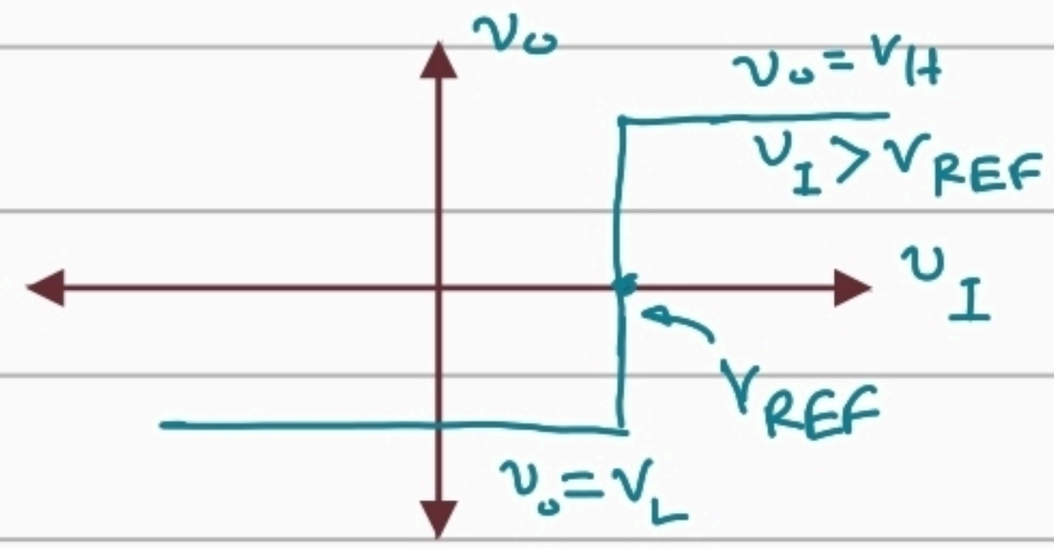
Otto H. Schmitt (1934) envisioned this circuit.

Comparators:

①



Transfer characteristics

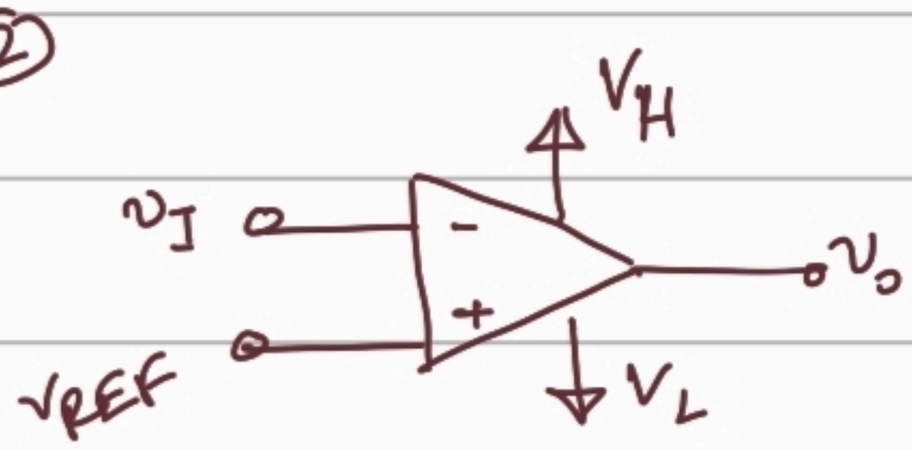


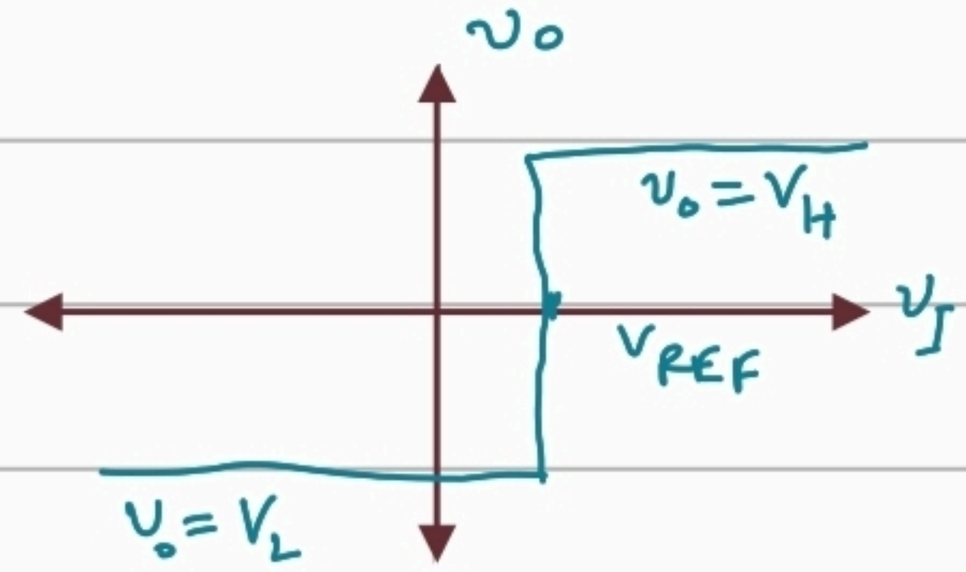
$$\boxed{\begin{array}{l} v_+ > v_- \Rightarrow v_o = V_H \\ v_+ < v_- \Rightarrow v_o = V_L \end{array}}$$

$v_+ = v_I > V_{REF} = v_- \Rightarrow v_o = V_H$

$v_+ = v_I < V_{REF} = v_- \Rightarrow v_o = V_L$

②



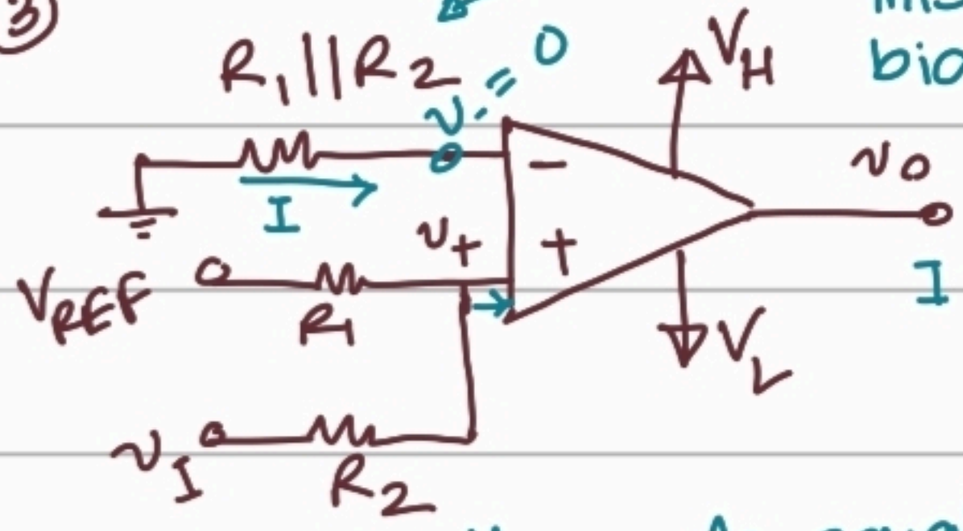


$v_+ = V_{REF} > v_I = v_- \Rightarrow v_o = V_H$

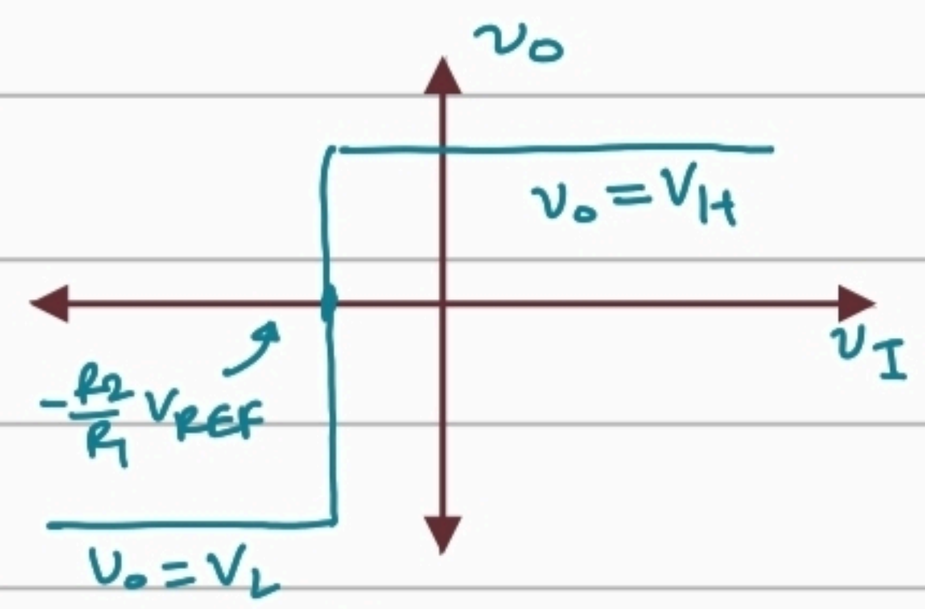
$v_+ = V_{REF} < v_I = v_- \Rightarrow v_o = V_L$

③

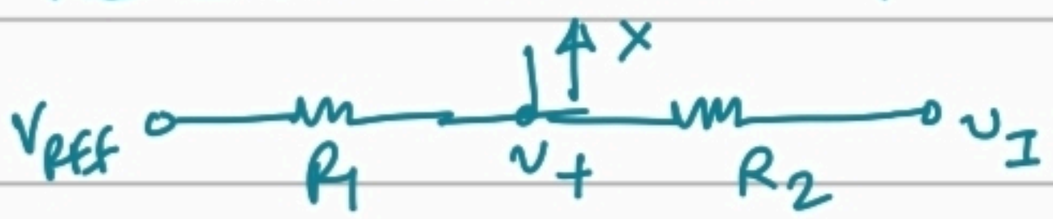
This prevent DC bias effect inside op-amp.



$I = 0$, $v_- = 0$ Always.



We can write node equation at "+" terminal



$$\frac{v_+ - V_{REF}}{R_1} + \frac{v_+ - v_I}{R_2} = 0$$

$$\Rightarrow \boxed{\begin{array}{l} v_+ = V_{REF}\left(\frac{R_2}{R_1+R_2}\right) + V_I\left(\frac{R_1}{R_1+R_2}\right) \\ v_- = 0 \end{array}}$$

$v_+ > v_-$

$$\Rightarrow \frac{v_I R_1}{R_1+R_2} + \frac{V_{REF} R_2}{R_1+R_2} > 0$$

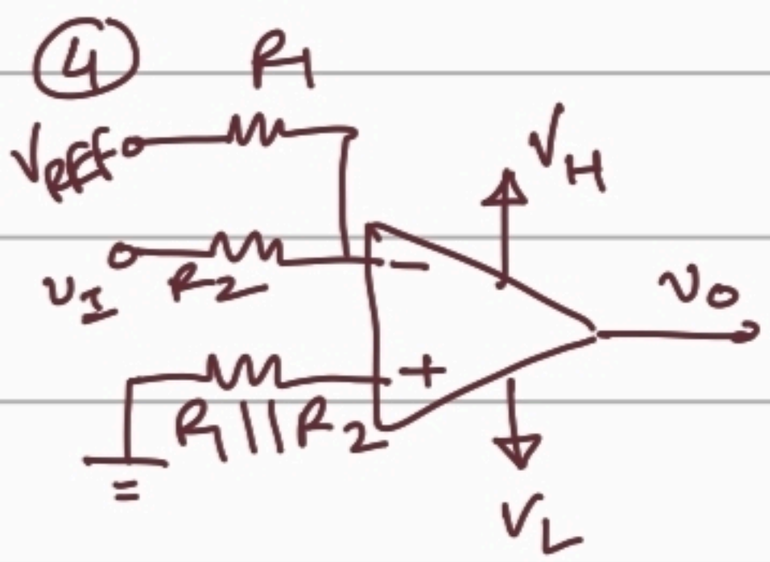
$$\Rightarrow v_I > \left(-\frac{R_2}{R_1}\right) V_{REF}$$

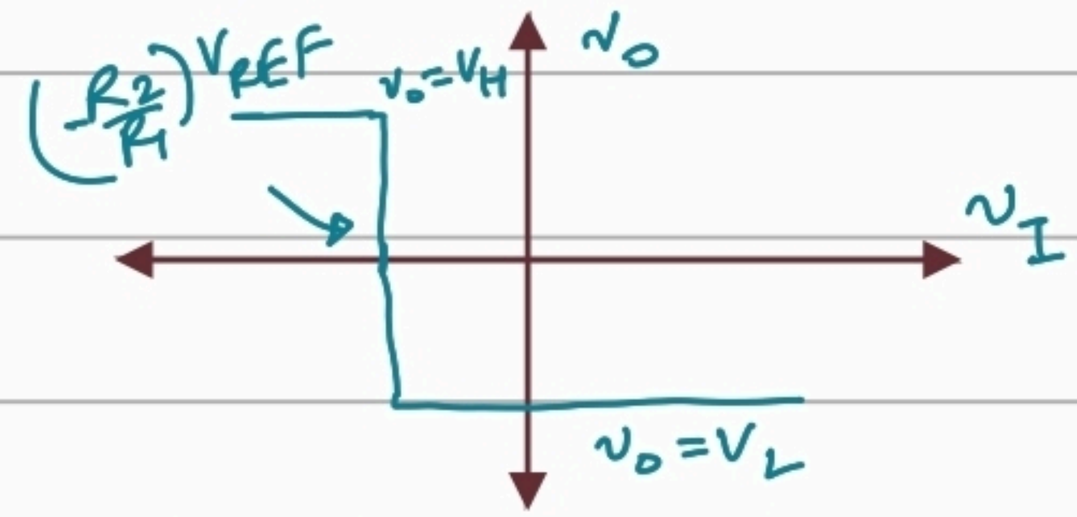
$\Rightarrow v_o = V_H$

or $v_I < \left(-\frac{R_2}{R_1}\right) V_{REF}$

$\Rightarrow v_o = V_L$

④





$v_+ = 0$

and $v_- = v_I \dfrac{R_1}{R_1+R_2} + V_{REF}\dfrac{R_2}{R_1+R_2}$

$\Rightarrow v_+ > v_-$

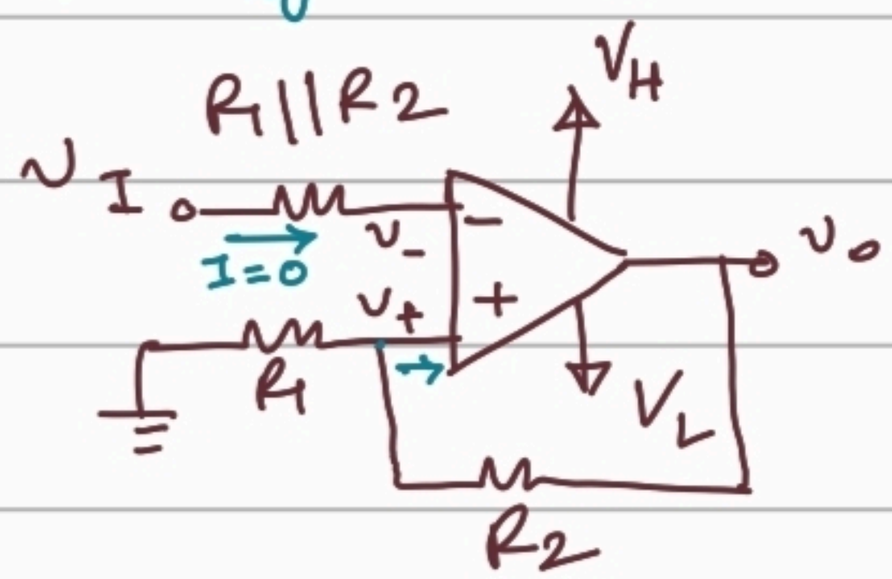
$\Rightarrow v_I < \left(-\dfrac{R_2}{R_1}\right)V_{REF}$

$\Rightarrow v_o = V_H$

otherwise, $v_o = V_L$

Schmitt Trigger

Inverting S.T.



$$\boxed{\begin{aligned} v_- &= v_I \\ v_+ &= v_o \frac{R_1}{R_1+R_2} \end{aligned}}$$

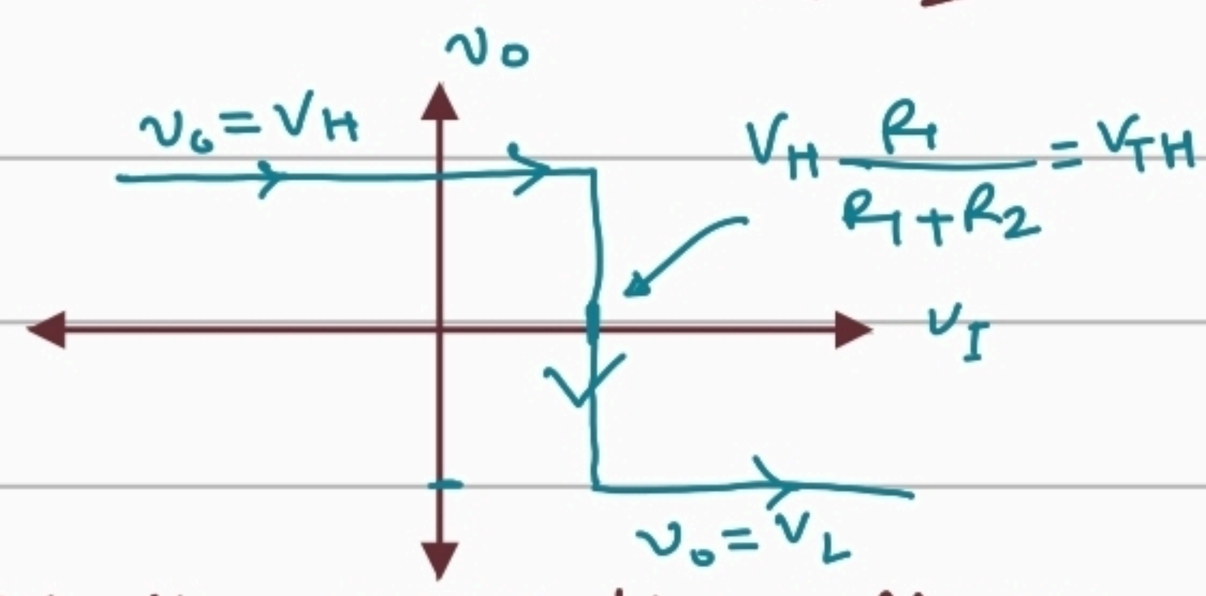
[use node eq^n at "+" terminal]

Output depends on the initial condition of the input.

<u>Case 1</u>: $|v_I| \gg 0$ but v_I is <u>negative</u>

We can expect, $v_+ > v_-$

$\Rightarrow v_o = V_H$ and $v_+ = V_H \dfrac{R_1}{R_1+R_2}$

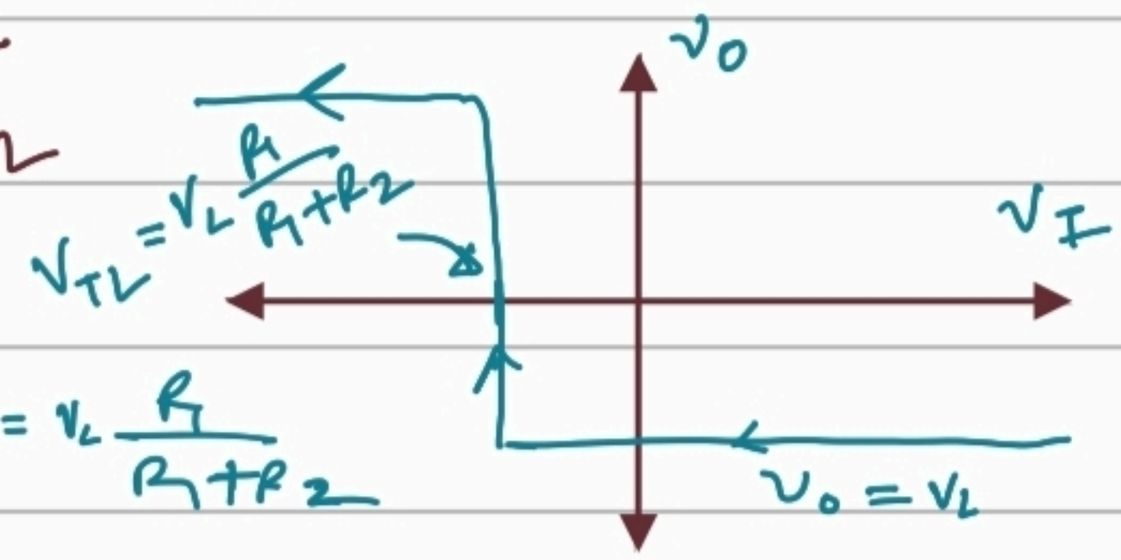


We can increase $v_I = v_-$ until it crosses the voltage of $v_+ = \dfrac{R_1 V_{REF}}{R_1+R_2}$. After that output changes to V_L.

So $V_{REF} \cdot \dfrac{R_1}{R_1+R_2}$ is denoted as higher threshold voltage. V_{TH}

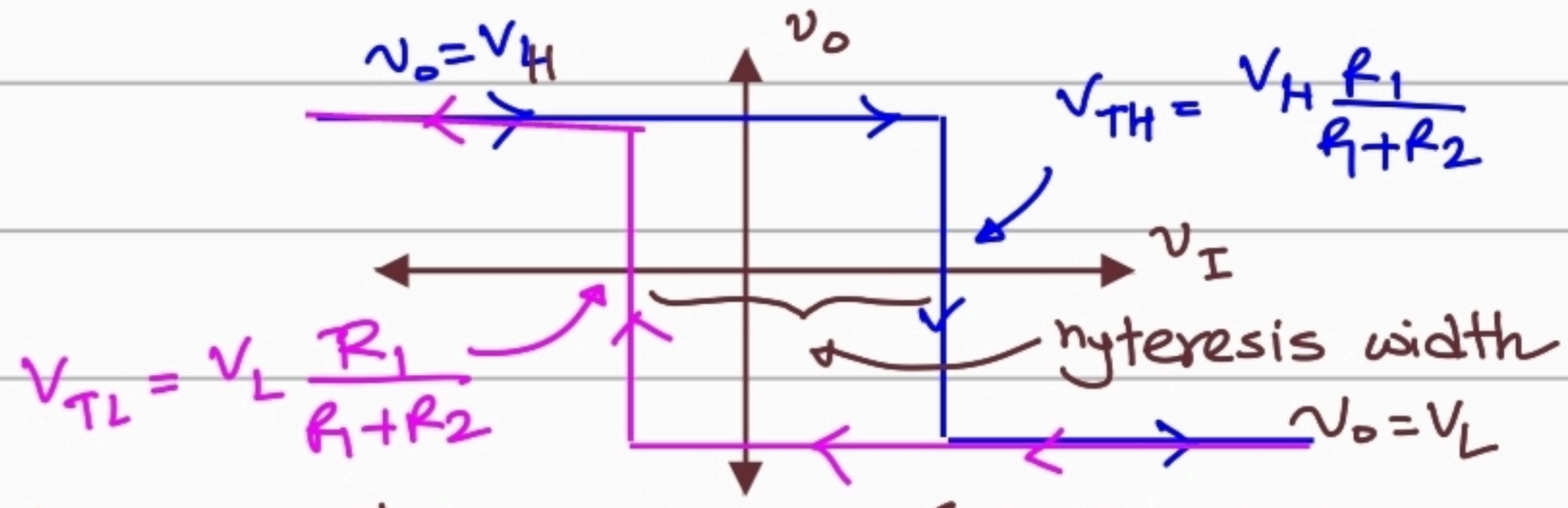
<u>Case 2</u>: $|v_I| \gg 0$ but v_I is positive. We can expect that $v_- > v_+$ and $v_o = V_L \Rightarrow v_+ = V_L \dfrac{R_1}{R_1+R_2}$.

When v_I decreases below the $v_+ = V_L \dfrac{R_1}{R_1+R_2}$, v_o changes from V_L to V_H.



Lower threshold voltage. $V_{TL} = V_L \dfrac{R_1}{R_1+R_2}$

Combined transfer characteristics.



Bistable multivibrator = Schmitt trigger

It has two stable output states. $v_o = V_H / V_L$

Example 15.6 Neamann

Determine the hysteresis width of a particular Schmitt trigger.

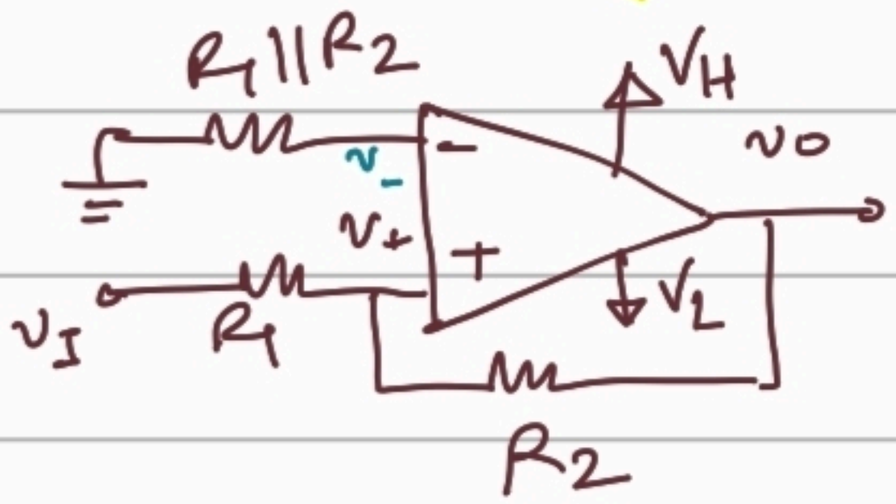
$R_1 = 10k\Omega$, $R_2 = 90k\Omega$, $V_H = 10V$ and $V_L = -10V$.

Sol^n:

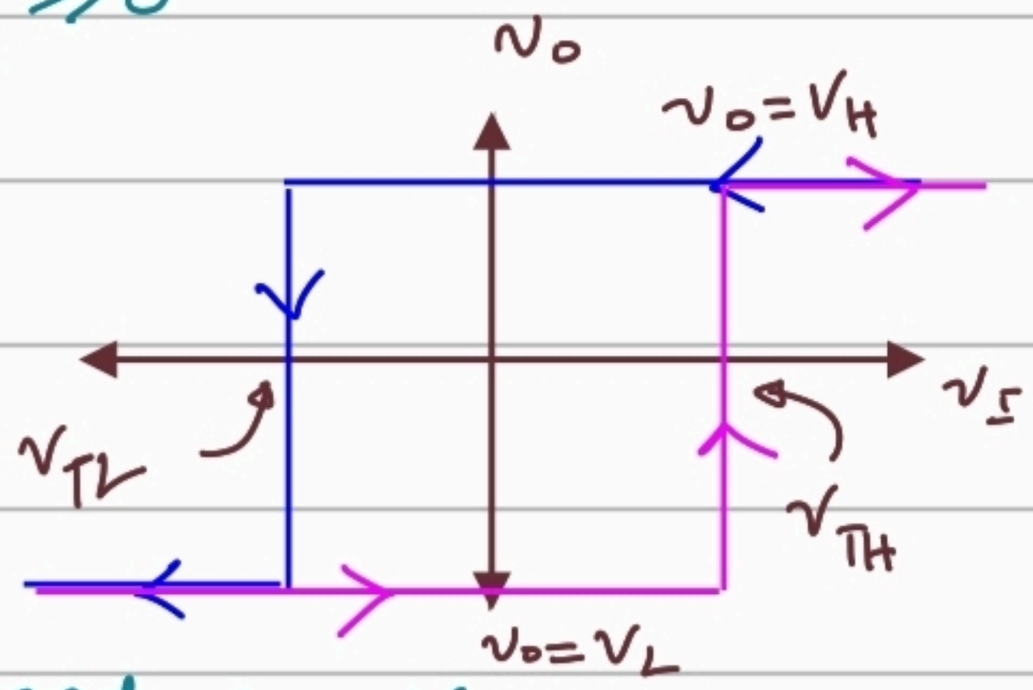
Hysteresis width $= V_{TH} - V_{TL}$

$$\Rightarrow V_{TH} - V_{TL} = V_H \frac{R_1}{R_1+R_2} - V_L \frac{R_1}{R_1+R_2} = (V_H - V_L)\frac{R_1}{R_1+R_2} = 20 \times \frac{10}{100} = 2V$$

Non-inverting Schmitt Trigger Circuit:



Consider the two cases just like before and use $|v_I| >> 0$



$$\boxed{\begin{aligned} v_- &= 0 \\ v_+ &= v_o \frac{R_1}{R_1+R_2} + v_I \frac{R_2}{R_1+R_2} \end{aligned}}$$

At transition point $v_+ = v_-$ and for V_{TH} we can say from transfer characteristics that $v_o = V_L$

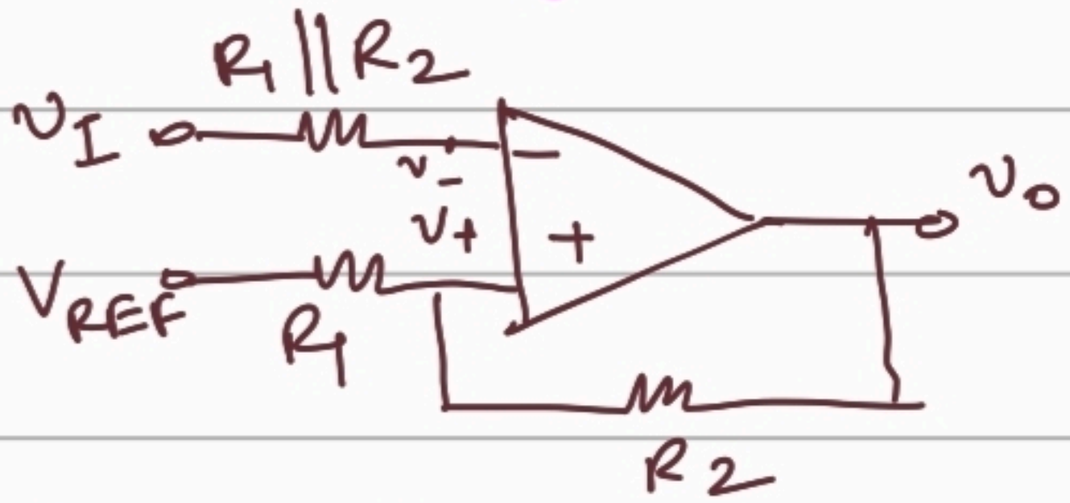
$$0 = V_L \frac{R_1}{R_1+R_2} + V_{TH} \frac{R_2}{R_1+R_2} \Rightarrow \underline{V_{TH}} = \left(-\frac{R_1}{R_2}\right)\underline{V_L}$$

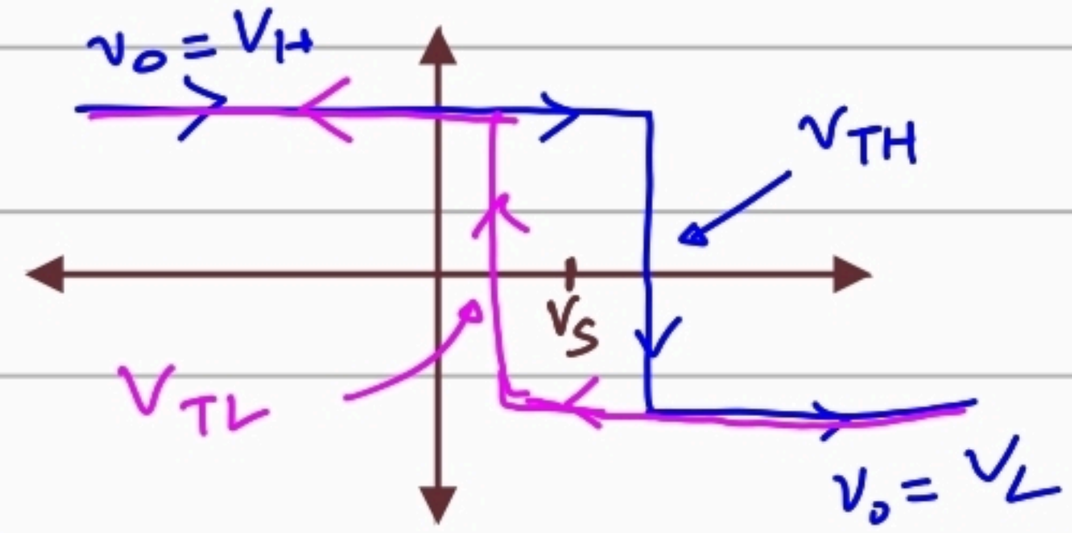
Similarly, we can get. $\underline{V_{TL}} = \left(-\frac{R_1}{R_2}\right)\underline{V_H}$

$v_I \uparrow \Rightarrow v_o \uparrow$ when $|v_I| >> 0$

Schmitt Trigger with Applied Voltage:

Inverting S.T.





$$\boxed{\begin{aligned} v_- &= v_I \\ v_+ &= V_{REF}\frac{R_2}{R_1+R_2} + v_o\frac{R_1}{R_1+R_2} \end{aligned}}$$

V_s = shift voltage.

Now. $v_- = v_+ \; (v_o = V_H, V_I = V_{TH})$

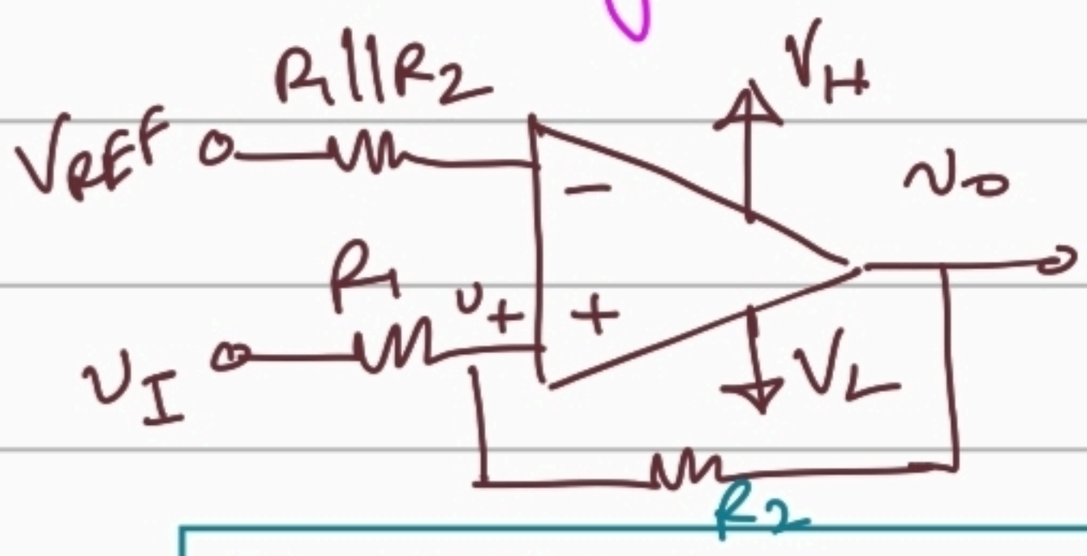
$$\Rightarrow V_{TH} = \underbrace{V_{REF}\left(\frac{R_2}{R_1+R_2}\right)}_{v_s} + V_H\left(\frac{R_1}{R_1+R_2}\right)$$

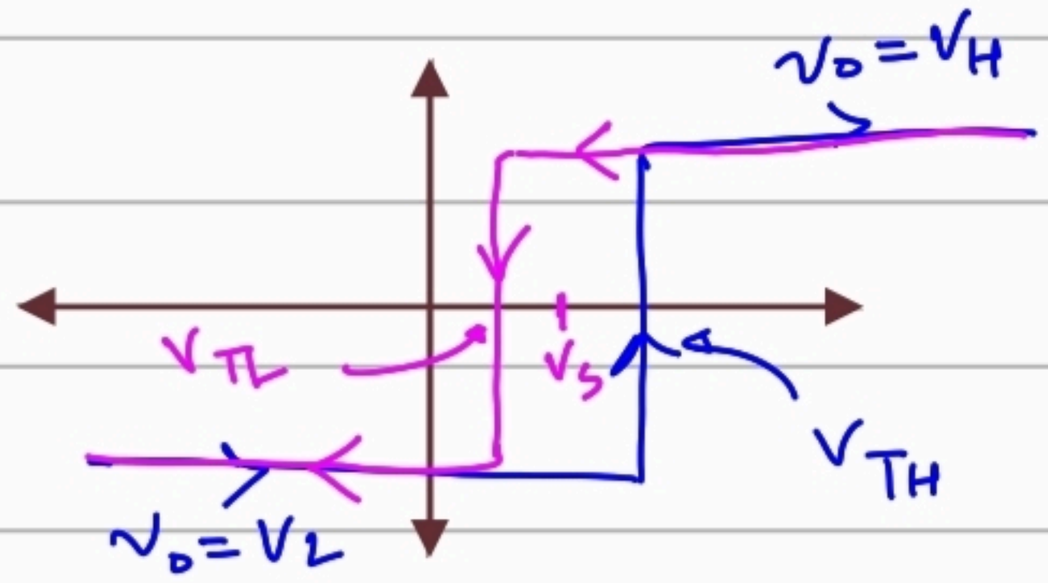
Similarly. $v_- = v_+ \; (v_o = V_L, v_I = V_{TL})$

$$\Rightarrow V_{TL} = \underbrace{V_{REF}\left(\frac{R_2}{R_1+R_2}\right)}_{v_s} + V_L\left(\frac{R_1}{R_1+R_2}\right)$$

So shift/ voltage. switching $\boxed{V_s = V_{REF}\frac{R_2}{R_1+R_2}}$

Noninverting S.T.





$$\boxed{\begin{aligned} v_- &= V_{REF} \\ v_+ &= v_I\frac{R_2}{R_1+R_2} + v_o\frac{R_1}{R_1+R_2} \end{aligned}}$$

$$V_{TH} = \left(\frac{R_1+R_2}{R_2}\right)V_{REF} + \left(-\frac{R_1}{R_2}\right)V_L$$

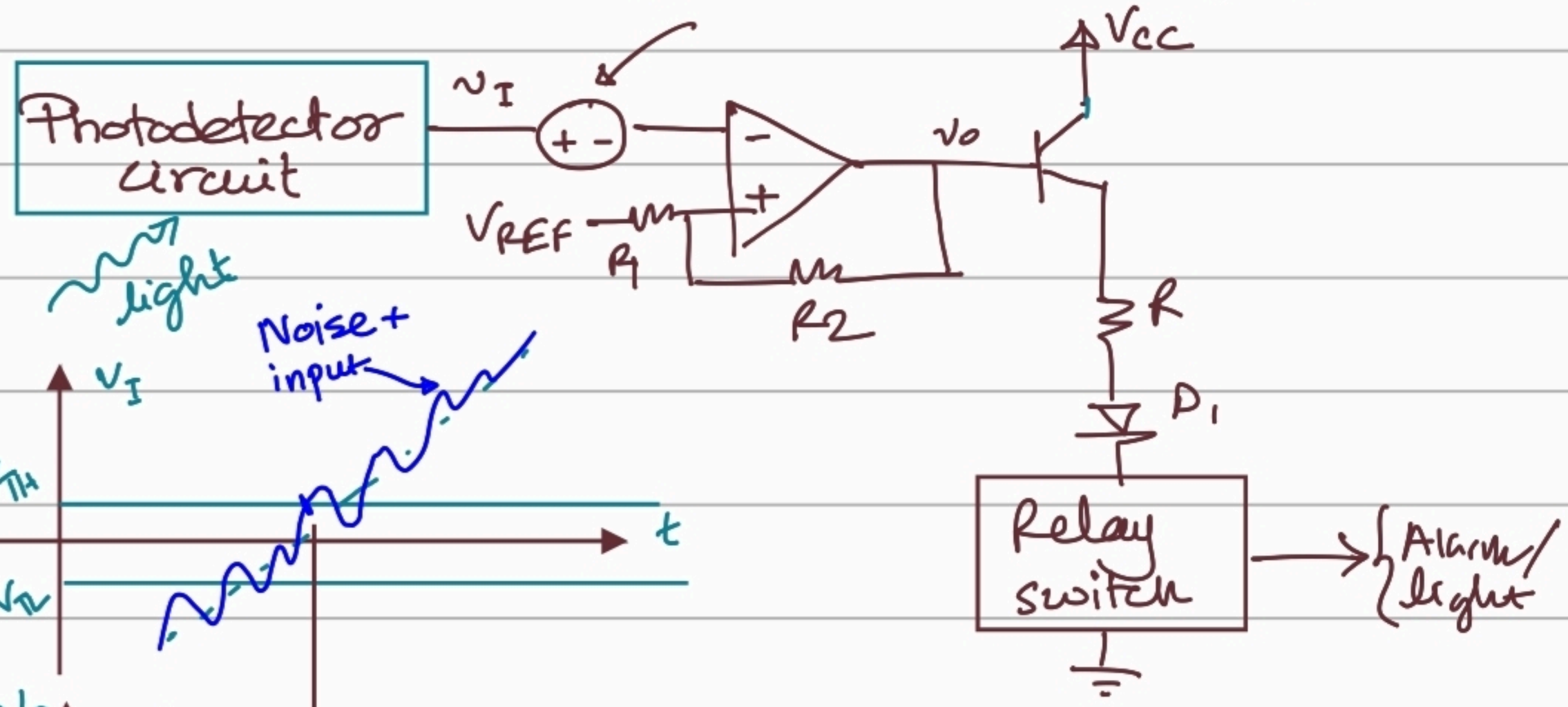
$$V_{TL} = \left(\frac{R_1+R_2}{R_2}\right)V_{REF} + \left(-\frac{R_1}{R_2}\right)V_H$$

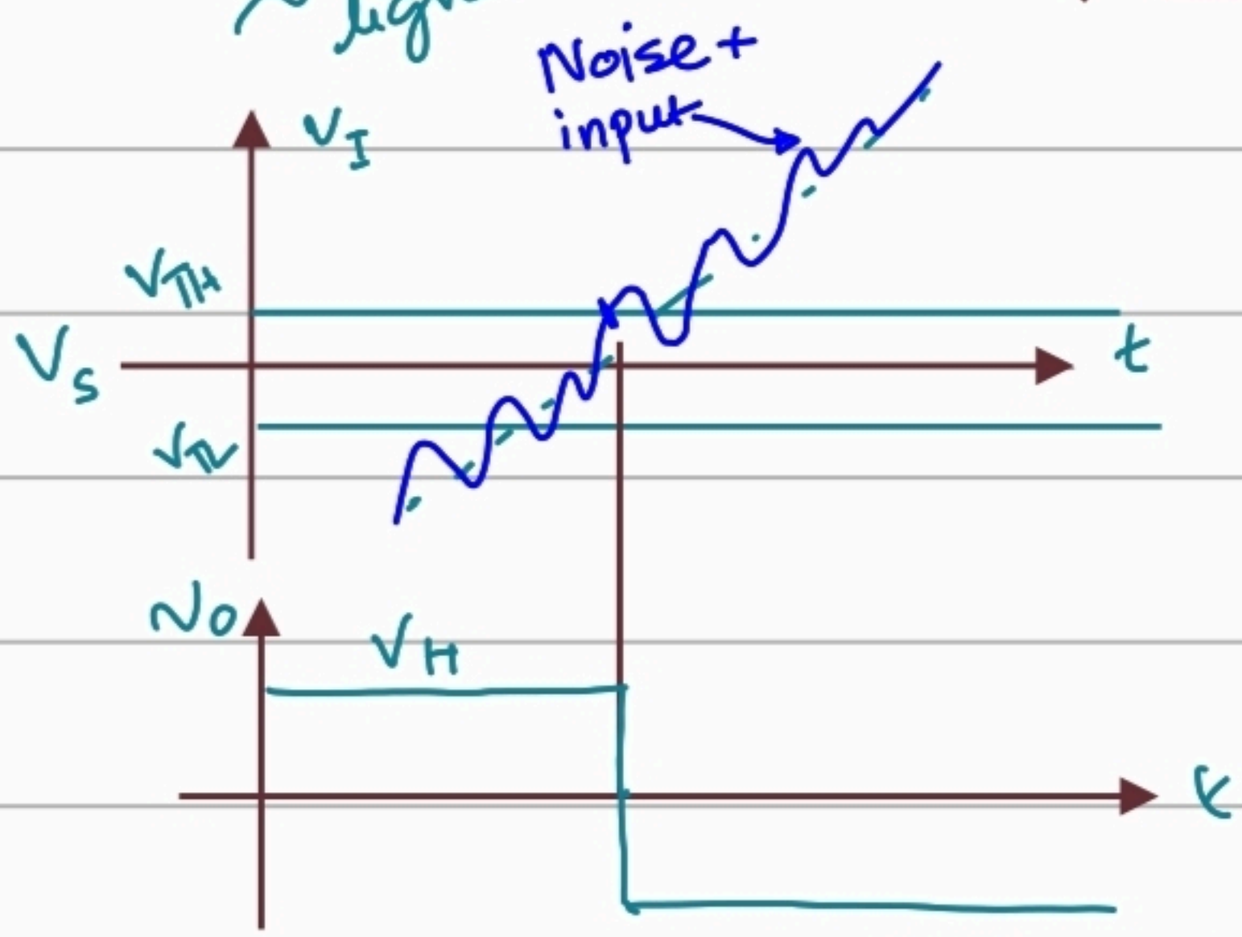
Shift/voltage. switching $V_s = \left(\frac{R_1+R_2}{R_2}\right)V_{REF}$

Application:

- ☐ Smoke Detector
- ☐ Street light Control

Noise source: Chattering effect

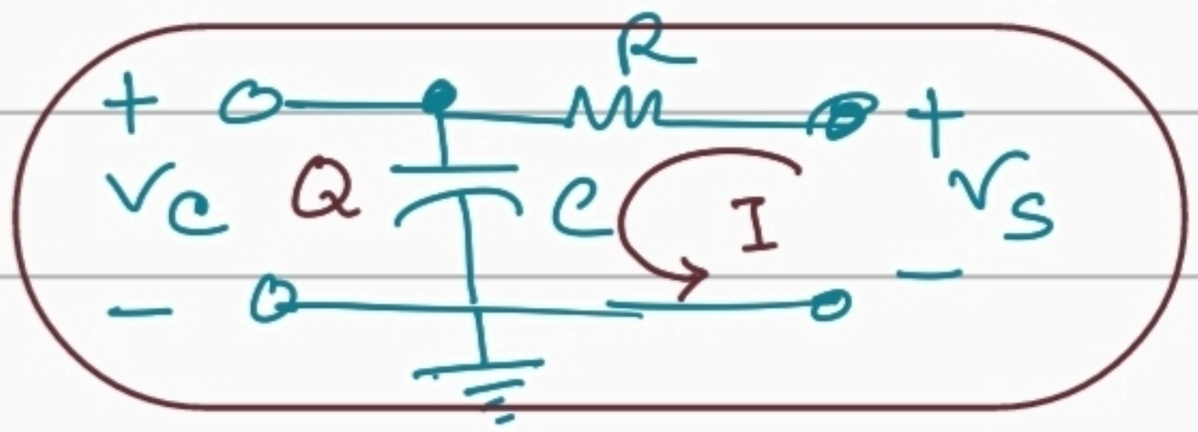




Design problem 15.7 (Practice | Final Exam)

Lecture 19: Signal Generators.

Basic R-C circuit:



Suppose, at initial time t_1 the capacitor has a voltage $v_c(t_1) = v_{initial}$.

If $v_s > v_c(t_1)$. Q ↑ and

if $v_s < v_c(t_1)$. Q ↓.

From the definition of current flow, we know that, $I = \frac{dQ}{dt}$

Using the definition of capacitance $\left(C = \frac{Q}{V}\right)$

$$I = \frac{dQ}{dt} = \frac{d}{dt}(Cv_c) = \boxed{C\frac{dv_c}{dt} = \frac{v_s - v_c}{R}}$$

We want to determine the voltage across capacitor for the time $t_1 < t < \infty$.

$$C\frac{dv_c}{dt} = \frac{v_s - v_c}{R} \Rightarrow \int_{v_c(t_1)}^{v_c(t)} \frac{dv_c}{v_s - v_c} = \int_{t_1}^{t} \frac{dt}{RC}$$

$$\Rightarrow -\ln|v_s - v_c|\Big|_{v_c(t_1)}^{v_c(t)} = \frac{t-t_1}{RC} \Rightarrow t - t_1 = RC \ln\left|\frac{v_s - v_c(t_1)}{v_s - v_c(t)}\right|$$

$$\Rightarrow \boxed{v_c(t) = v_s + (v_c(t_1) - v_s)\exp\left(-\frac{t-t_1}{RC}\right)}$$

$t \to \infty$. $v_c(\infty) = v_s$ because $\exp(-\infty) \to 0$.

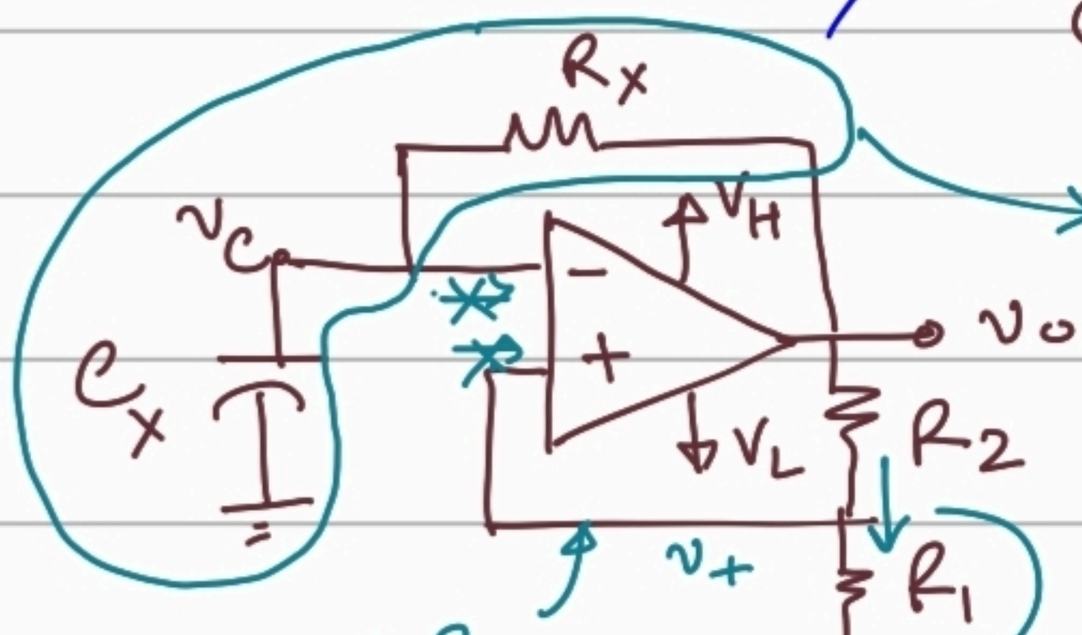
$v_c(\infty) = v_s = v_{final}$ and $v_c(t_1) = v_{initial}$.

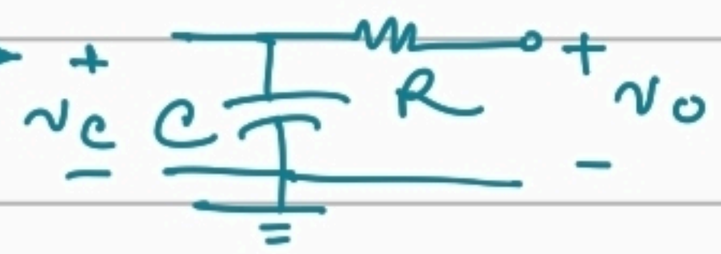
$\tau = RC$ = time constant.

$$\boxed{v_c(t) = v_{final} + (v_{initial} - v_{final})\exp\left(-\frac{t-t_1}{\tau}\right)}$$

Schmitt Oscillator / Astable Multivibrator:

↳ There is no stable state.





$$v_c(t) = v_o + (v_{initial} - v_o)\exp\left(-\frac{t-t_1}{R_xC_x}\right)$$

$$v_+ = \frac{v_o R_1}{R_1 + R_2}$$

$$t - t_1 = \tau \ln\left|\frac{v_{final} - v_c(t_1)}{v_{final} - v_c(t_2)}\right|$$

($v_{final} \to v_o$)

We already know the threshold voltages.

$$v_{TH} = V_H \frac{R_1}{R_1 + R_2} \quad \text{and} \quad v_{TL} = V_L \frac{R_1}{R_1 + R_2}$$

Coughline. Chapter 6.

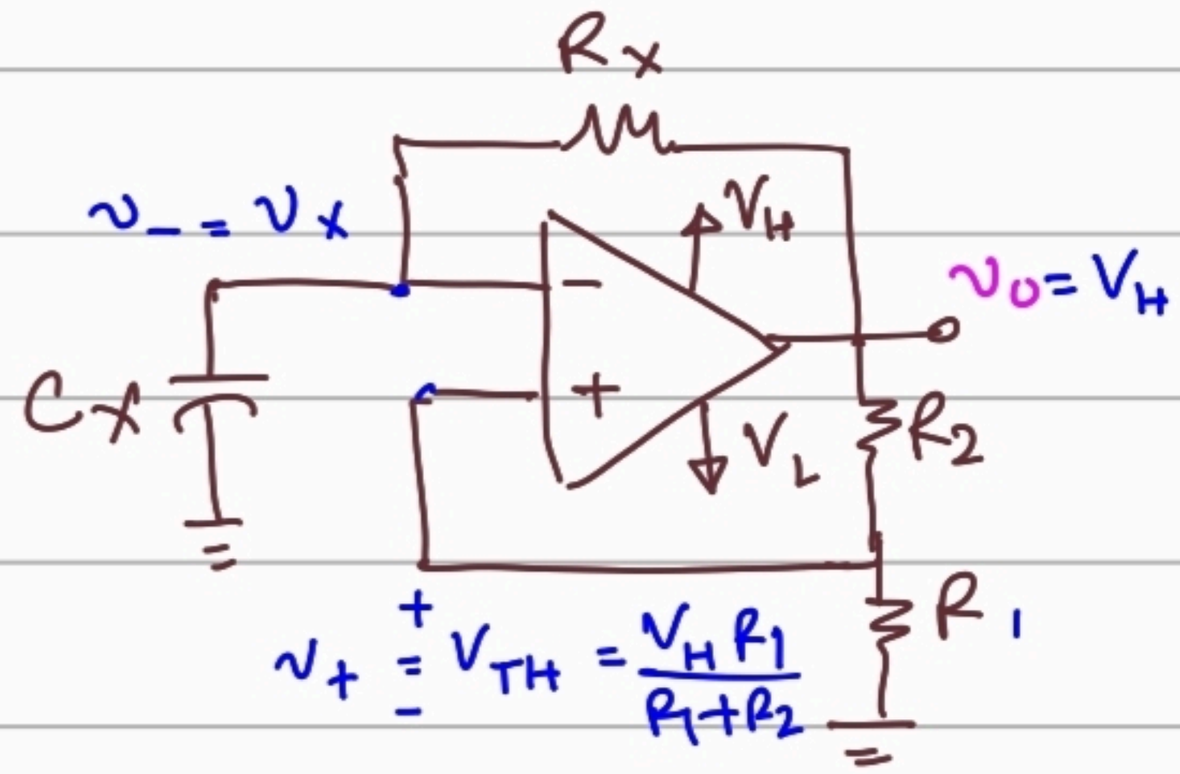
$v_{TH} \to V_{UT}$ = upper threshold voltage

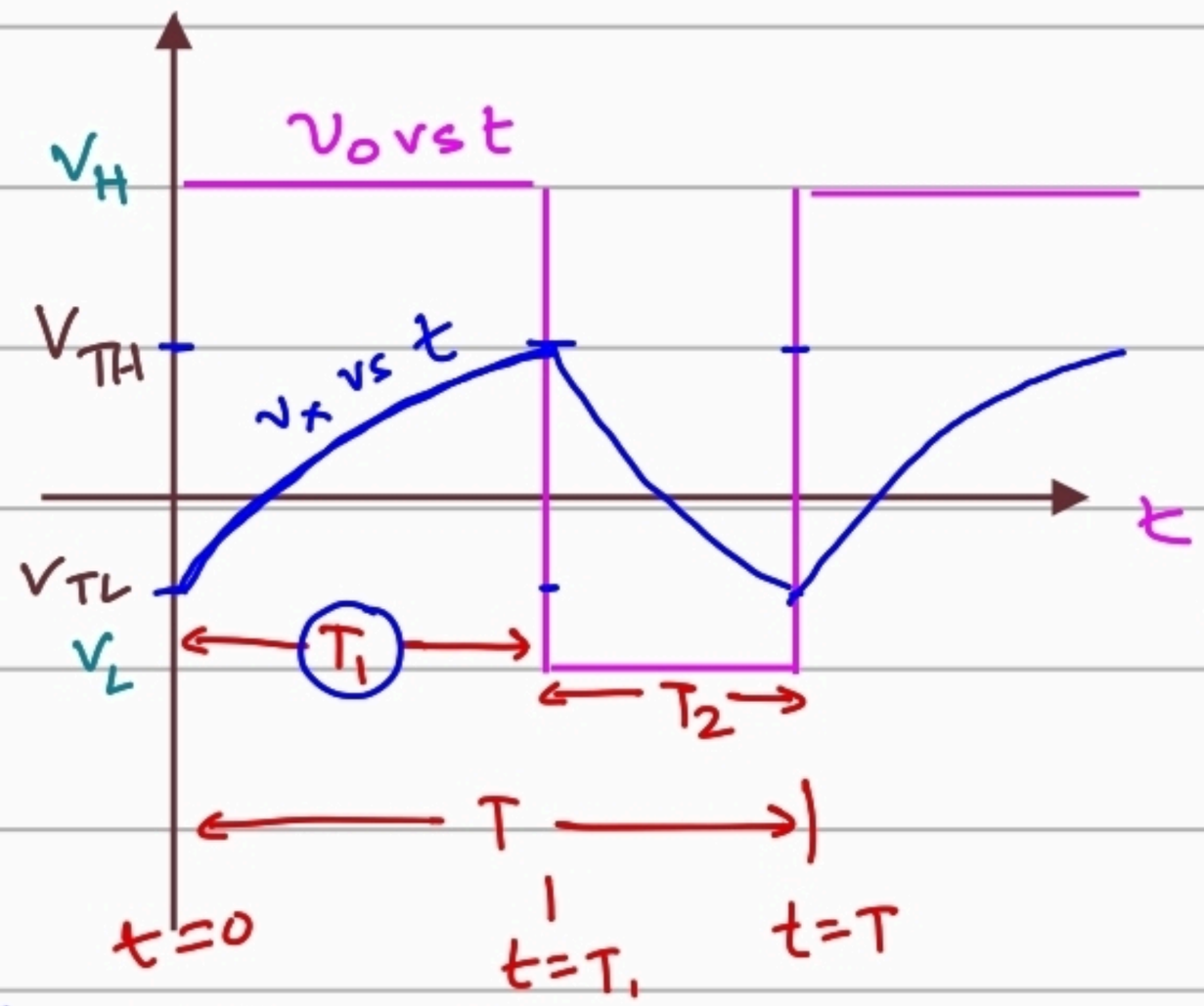
$v_{TL} \to V_{LT}$ = lower threshold voltage

$V_H \to V_{sat}$, $V_L \to -V_{sat}$, $|V_{sat}| \neq |-V_{sat}|$

Square Wave Generator: (Steady state analysis)

① **Case 1:** $0 < t < T_1$





Initial condition: $v_x = V_{TL}$ and $v_o = V_H$

The output v_o will remain at same value until $v_o = v_x$ crosses the voltage V_{TH}. $[v_+ > v_-, v_o = V_H]$

$$\boxed{v_c = v_x(t) = V_H + (V_{TL} - V_H)\exp\left(-\frac{t-0}{R_x C_x}\right)}$$

At $t = T_1$, $v_x(T_1) = V_{TH}$. Using this condition we can determine the value of T_1

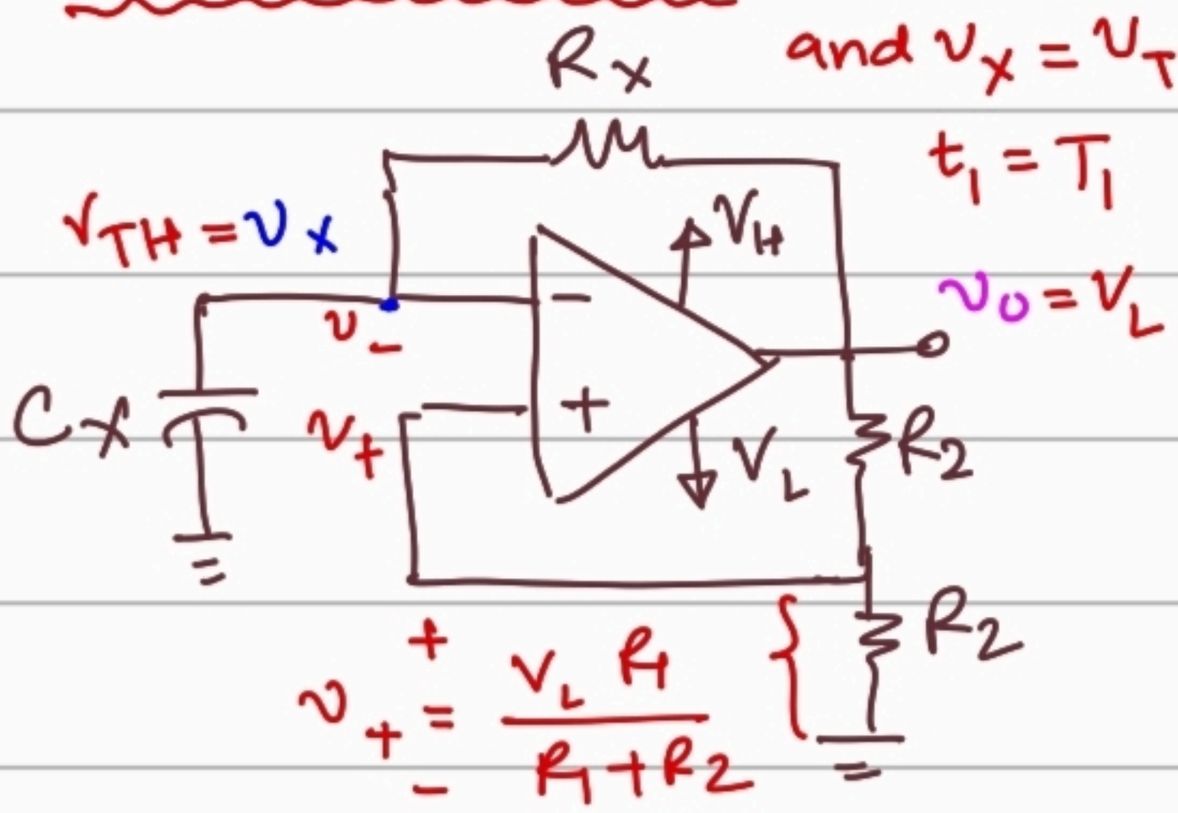
$$v_x(T_1) = V_{TH} = V_H + (V_{TL} - V_H)\exp\left(-\frac{T_1}{R_x C_x}\right)$$

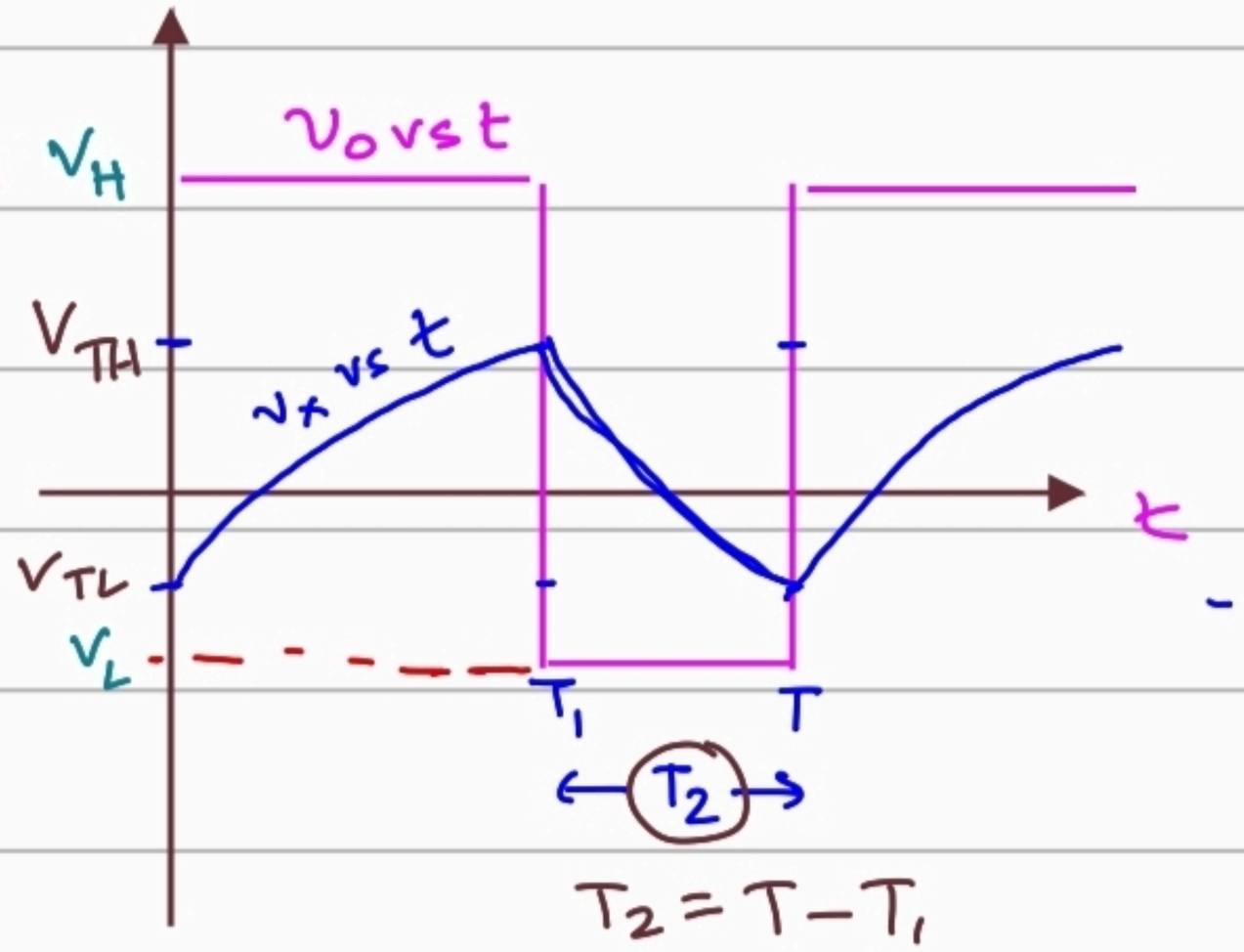
$$\Rightarrow \boxed{T_1 = R_x C_x \ln\left|\frac{V_H - V_{TL}}{V_H - V_{TH}}\right|}$$

② **Case 2:** $T_1 < t < T$

Initial condition: $v_o = V_L$ and $v_x = v_{TH}$

$t_1 = T_1$





$T_2 = T - T_1$

$(v_+ < v_-)$ Now output will remain at $v_o = V_L$ until v_x crosses V_{TL}.

$$\boxed{v_c = v_x(t) = V_L + (V_{TH} - V_L)\exp\left(-\frac{t - T_1}{R_x C_x}\right)}$$

At $t = T$ time $v_x(T) = V_{TL}$. So using this we find.

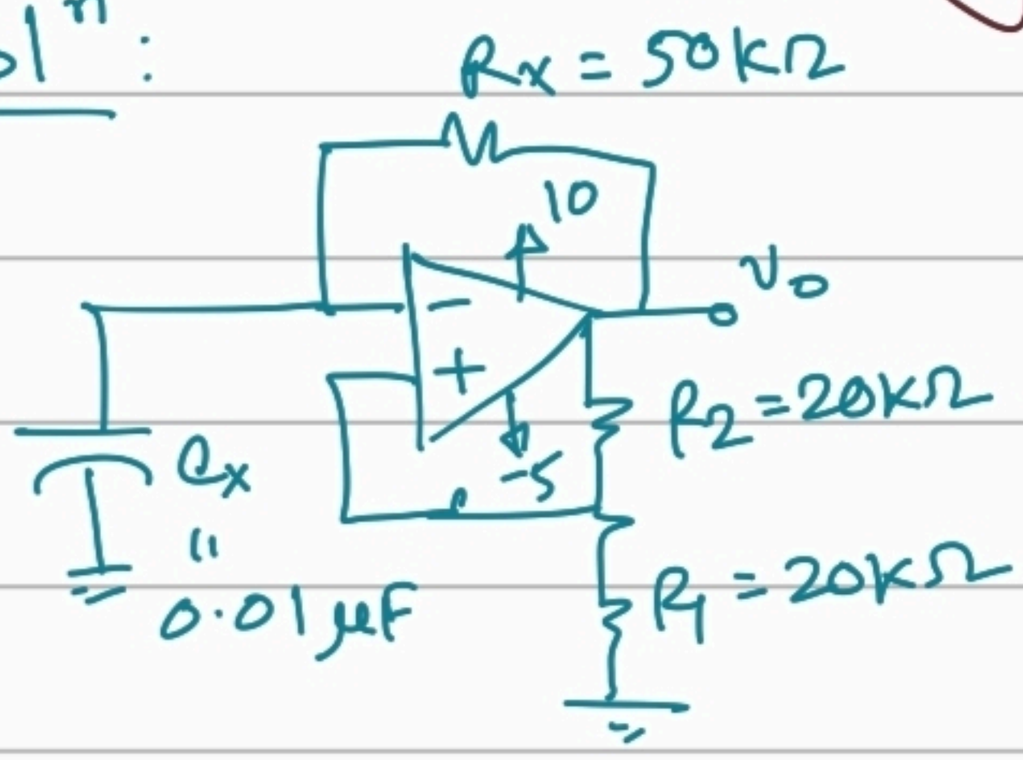
$$V_x(T) = V_{TL} = V_L + (V_{TH} - V_L)\exp\left(-\frac{\cancel{(T - T_1)}\ T_2}{R_x C_x}\right)$$

$$\Rightarrow \boxed{T_2 = R_x C_x \ln\left|\frac{V_L - V_{TH}}{V_L - V_{TL}}\right|}$$

← Just swap $H \leftrightarrow L$ to get T_1.

<u>Neamann's Exercise 15.8</u>. For the Schmitt trigger Oscillator, the saturation output voltages are +10V and −5V. $R_1 = R_2 = 20\,K\Omega$, $R_x = 50\,K\Omega$ and $C_x = 0.01\,\mu F$. Determine the frequency and duty cycle.

<u>Sol^n</u>:



$$V_{TH} = \frac{V_H R_1}{R_1 + R_2} = \frac{10 \times 20}{20 + 20} = 5\,V$$

$$V_{TL} = \frac{V_L R_1}{R_1 + R_2} = \frac{-5 \times 20}{20 + 20} = -2.5\,V$$

$$\tau = R_x C_x = 50 \times 10^3 \times 0.01 \times 10^{-6}\ \Omega F$$
$$= 0.5 \times 10^{-3}\,s$$
$$= 0.5\,ms$$

Time duration of high output, $T_1 = \tau \ln\left|\frac{V_H - V_{TL}}{V_H - V_{TH}}\right|$

$$T_1 = 0.5\,ms \times \ln\left|\frac{10 - (-2.5)}{10 - 5}\right| = 0.5 \ln(2.5)\ ms$$

Time duration of low output, $T_2 = \tau \ln\left|\frac{V_L - V_{TH}}{V_L - V_{TL}}\right|$

$$T_2 = 0.5\,ms \times \ln\left|\frac{-5 - 5}{-5 - (-2.5)}\right| = 0.5 \ln(4)\ ms$$

Total time period, $T = T_1 + T_2 = 0.5 \ln(2.5 \times 4)$
$$= 0.5 \ln(10)$$

frequency. $f = \frac{1}{T} = \frac{1}{0.5\ln(10)\,mS} = 0.868\,KHz$

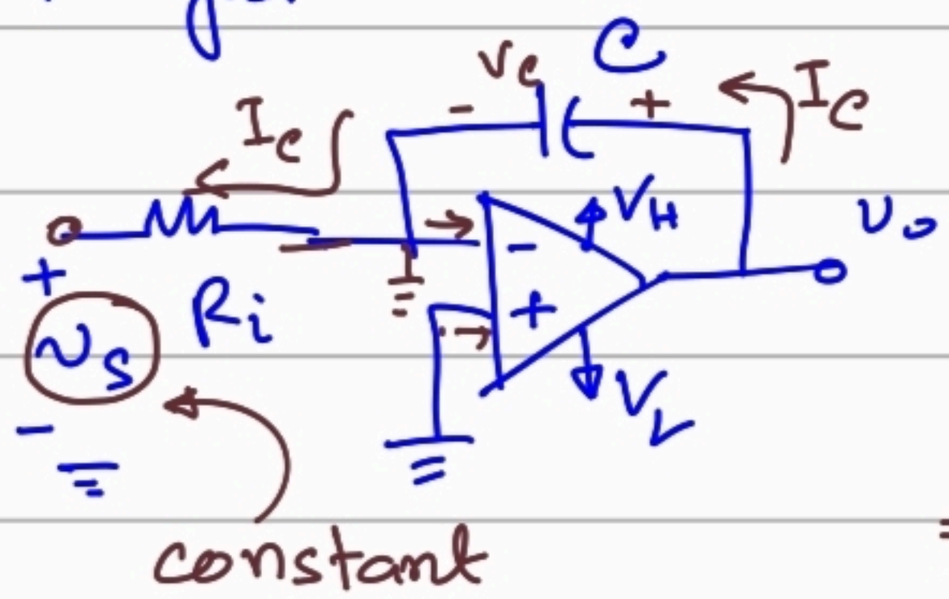
$= \boxed{868\,Hz}$

Duty cycle = % of time output voltage is high with a time period

$$= \frac{T_1}{T} \times 100\% = \frac{\ln(2.5)}{\ln(10)} \times 100\% = \boxed{39.1\%}$$

Triangular Wave Generator:

Integrator :



We are assuming virtual ground is present here.

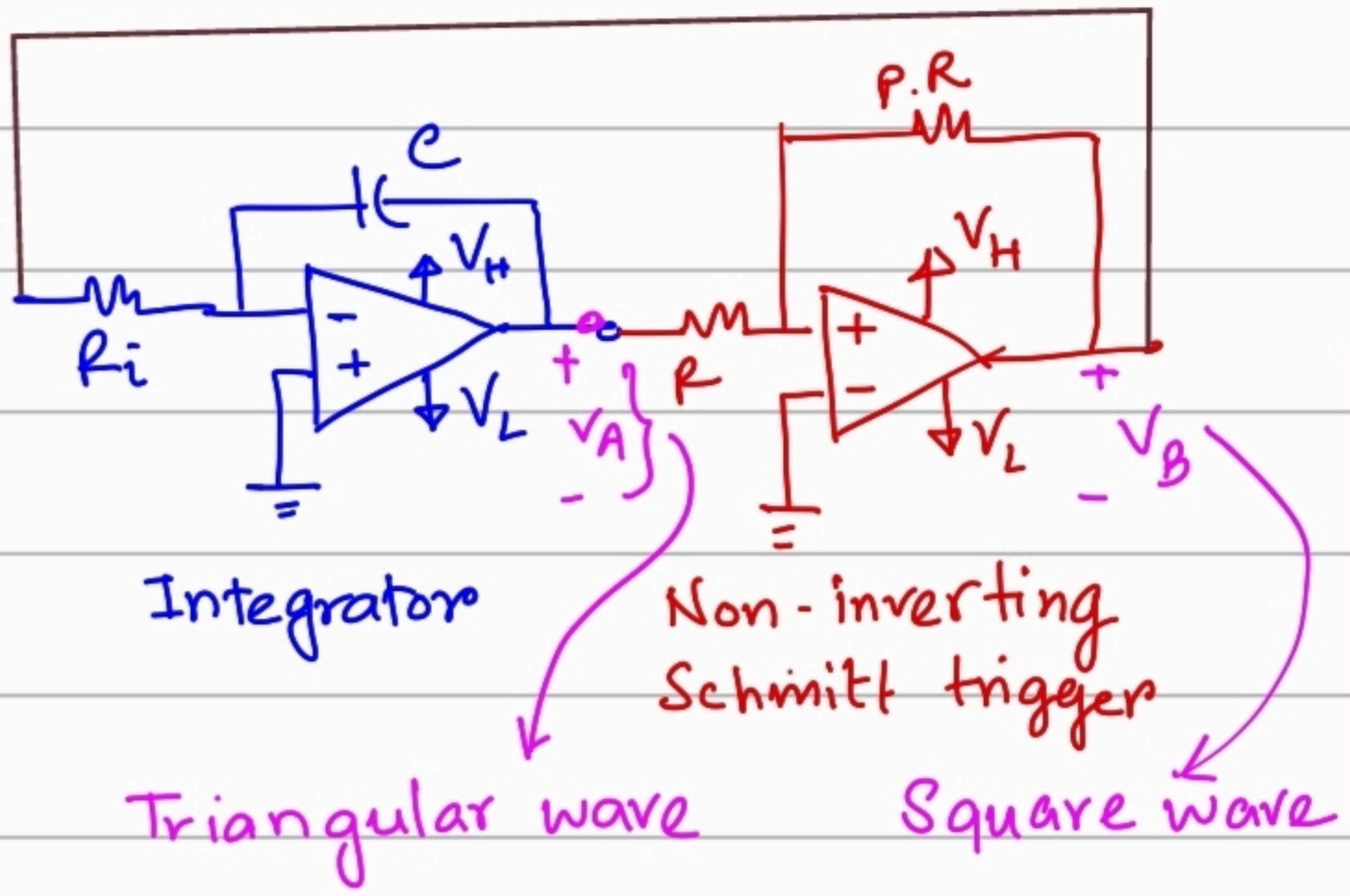
$$I_c = C\frac{dv_c}{dt} = \frac{0 - v_s}{R_i}$$

$$\Rightarrow \int_{v_c(t_1)}^{v_c(t)} dv_c = -\frac{v_s}{R_iC}\int_{t_1}^{t} dt$$

$$\Rightarrow v_c(t) - v_c(t_1) = -\frac{v_s}{R_iC}(t - t_1)$$

$$\Rightarrow \boxed{v_c(t) = v_c(t_1) - \frac{v_s}{R_iC}(t - t_1)}$$

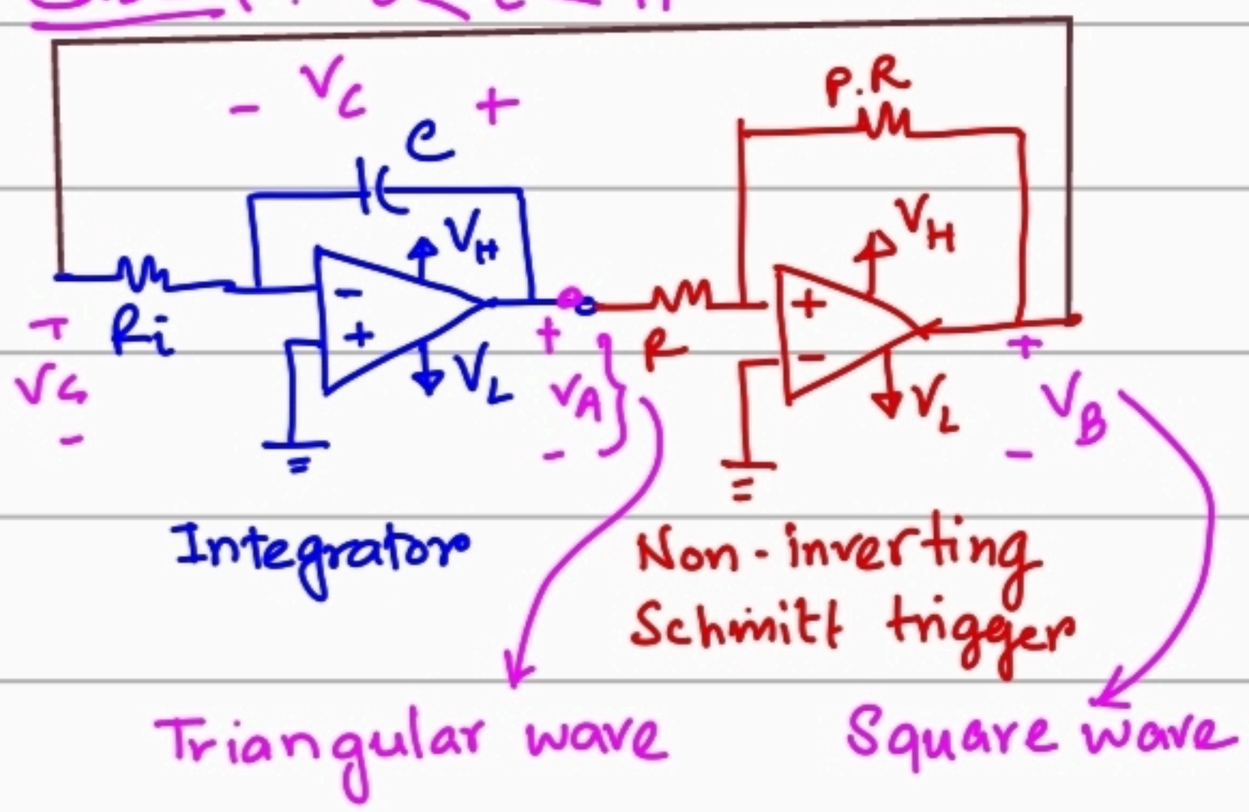
$v_c(t_1) = V_{initial}$

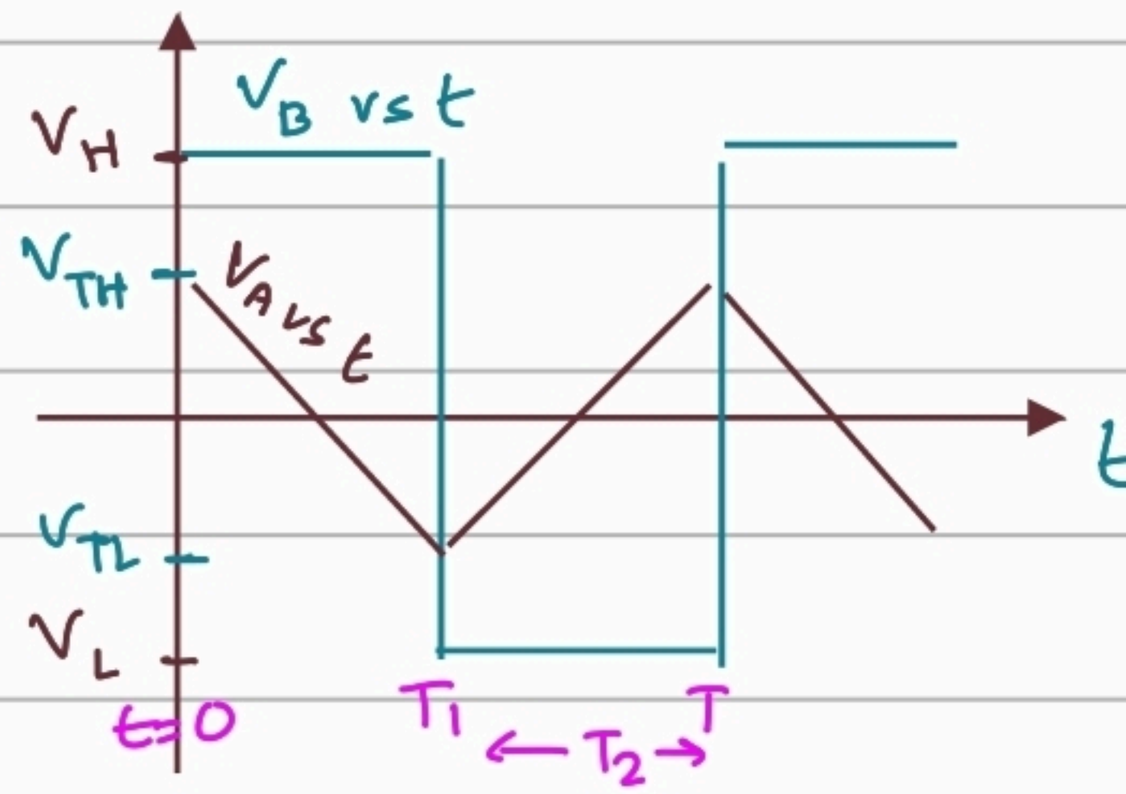


$$V_{TL} = V_H\left(-\frac{R}{PR}\right)$$

$$\boxed{\begin{aligned} V_{TL} &= -\frac{V_H}{P} \\ V_{TH} &= -\frac{V_L}{P} \end{aligned}}$$

Case 1 : $0 < t < T_1$





Initial condition: $v_B = V_H$ and $V_A = V_{TH}$, $t_{initial} = 0$

$$v_C(t) = v_A(t) = V_{initial} - \frac{V_s}{R_i C}(t - t_{initial}) \quad [V_s = V_B = V_H]$$

$$\Rightarrow V_A(t) = V_{TH} - \frac{V_H}{R_i C}(t - 0)$$

Because $V_A(T_1) = V_{TL}$, we can find.

$$\boxed{T_1 = R_i C \left(\frac{V_{TH} - V_{TL}}{V_H} \right)}$$

Case 2 : $T_1 < t < T$. Using similar analysis like square wave we can derive,

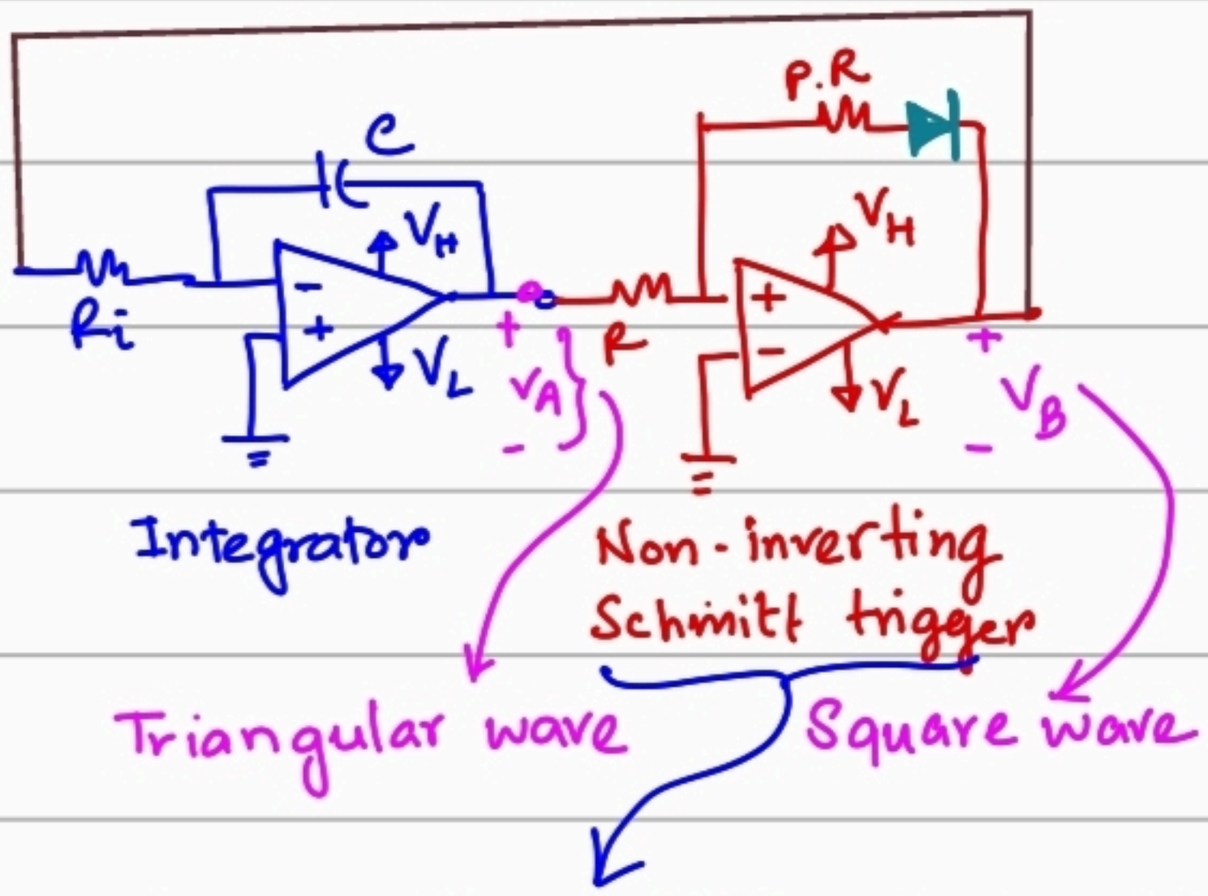
$$\boxed{T_2 = R_i C \left(\frac{V_{TL} - V_{TH}}{V_L} \right)} \qquad H \leftrightarrow L$$

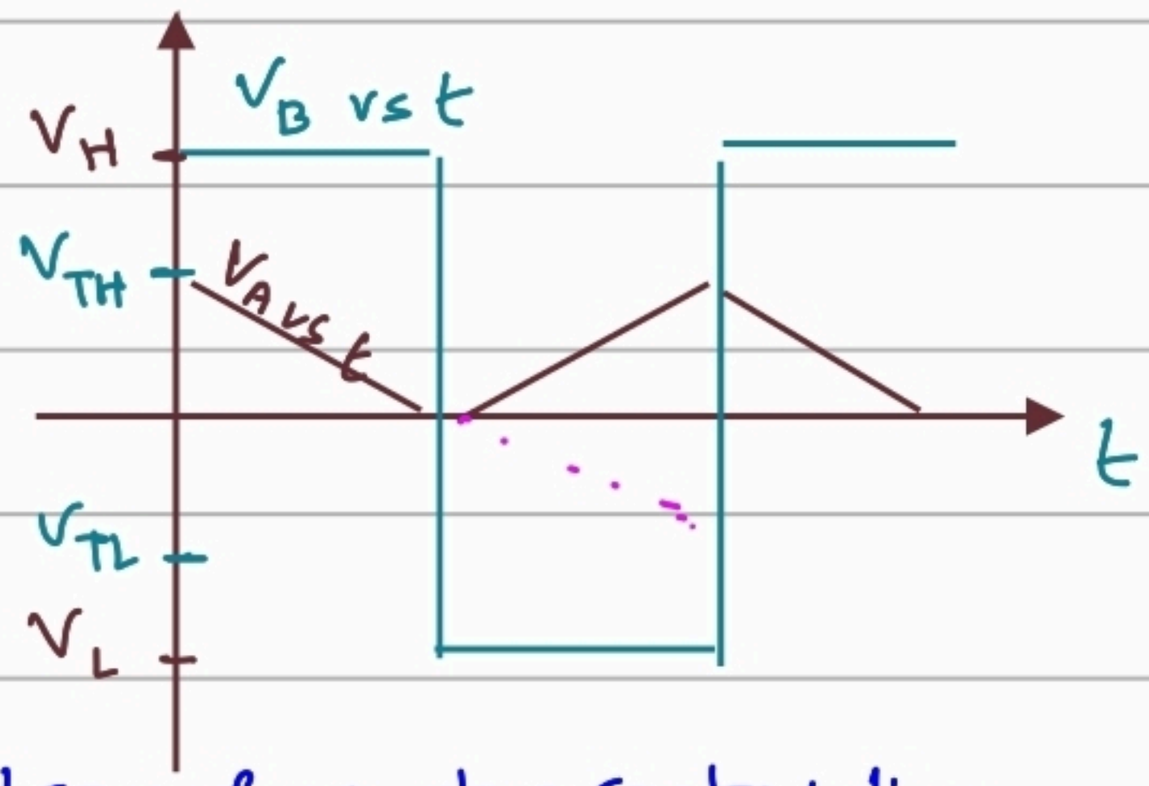
Total time period, $T = T_1 + T_2$. frequency, $f = \frac{1}{T}$

Special case: $\boxed{V_L = -V_H}$ $\quad V_{TH} = -\frac{V_L}{P}$, $V_{TL} = -\frac{V_H}{P}$

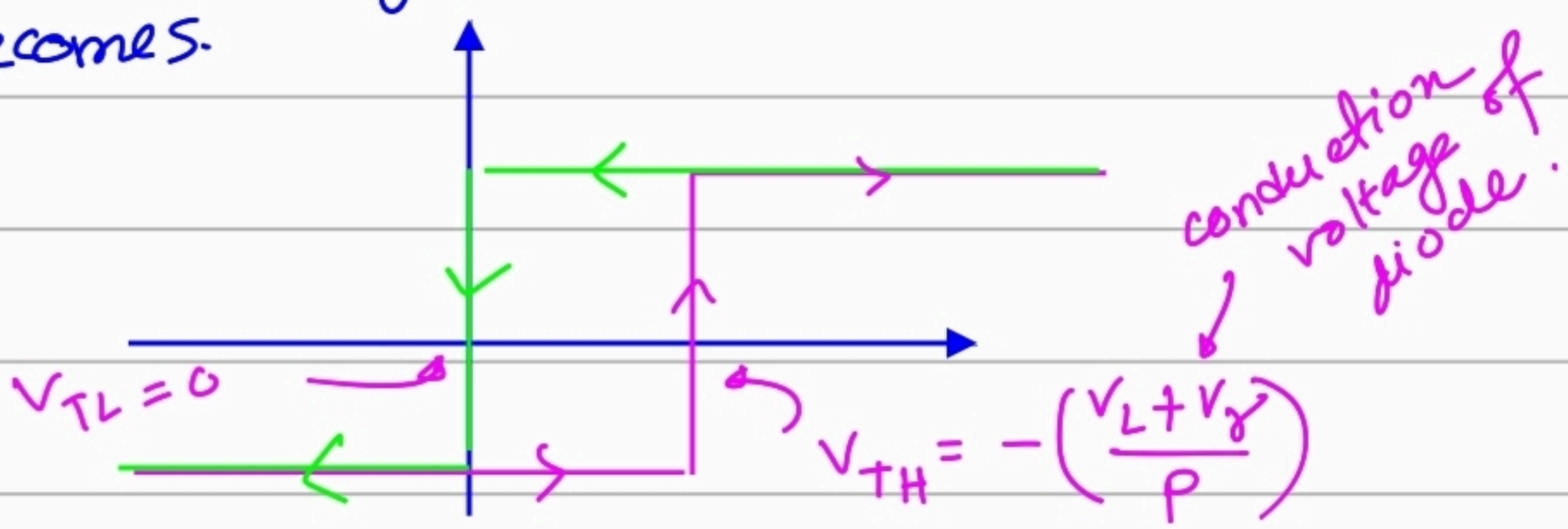
$$\boxed{f = \frac{P}{4R_i C}}$$

Unipolar Triangular Wave Generator





After putting this diode the transfer characteristics becomes.



Assuming. $V_H = -V_L$, we will get

$$\boxed{f = \frac{P}{2RC}}$$