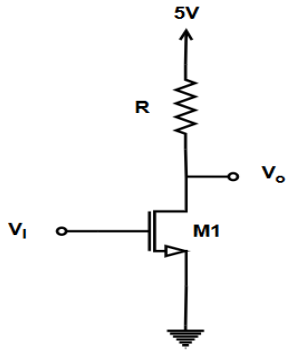
Question 01.

Following is the circuit of a N-MOS NOT gate. Given $V_{TN} = 0.5\ V,\ R = 20\ k\Omega$

$V_{DD} = 5V,\ K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 0.3\ mA/V^2$

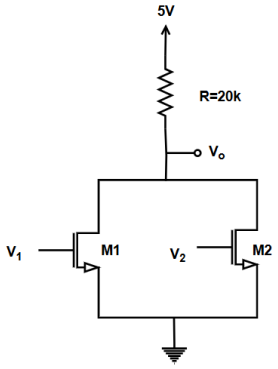


(a)	Find the output voltage of the inverter for the input voltage 5 V and 1.5 V.
(b)	Find the transition voltage (Saturation to triode) of the inverter.
(c)	Suppose, the input logic high and input logic low values of the NOT gate are 5V and 0V. Find the average power of the NOT gate.

Question 02.

Here, $V_{TN} = 0.8\ V\ and\ K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 0.1\ mA/V^2$

Value of the logic high is 5 V and logic low is 0V.



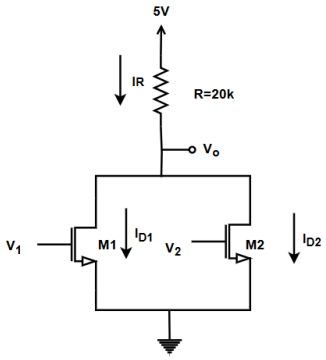
(a)	Identify the logic gate and make a truth table of the logic gate.
(b)	Find the output voltage of the logic gate for all possible case.
(c)	What will be the maximum and minimum power of the logic gate.

Question 03

Here, $V_{TN1} = 0.8\ V, V_{TN2} = 0.7\ V\ and\ K_{n1} = 0.1\ \ mA/V^2\ , K_{n2} = 0.2\ mA/V^2$

$Here, K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$

Value of the logic high is 5 V and logic low is 0V.



(a)	What will be the value of V_o and I_R of the circuit if both inputs are high.
(b)	Find the output of the NOR gate for the case $V_1 = 5\ V, V_2 = 0\ V$ and $V_1 = 0\ V, V_2 = 5\ V$. Why the values of the output voltage are different for the above two cases?