# CSE 350
# Digital Electronics and Pulse Techniques

## NMOS NOT and NOR without load
## CMOS Logic Circuit Design

BRAC UNIVERSITY
Inspiring Excellence

**Course Instructor**: Shomen Kundu (SDU)

Mail: shomen.kundu@bracu.ac.bd
Desk: 4N166

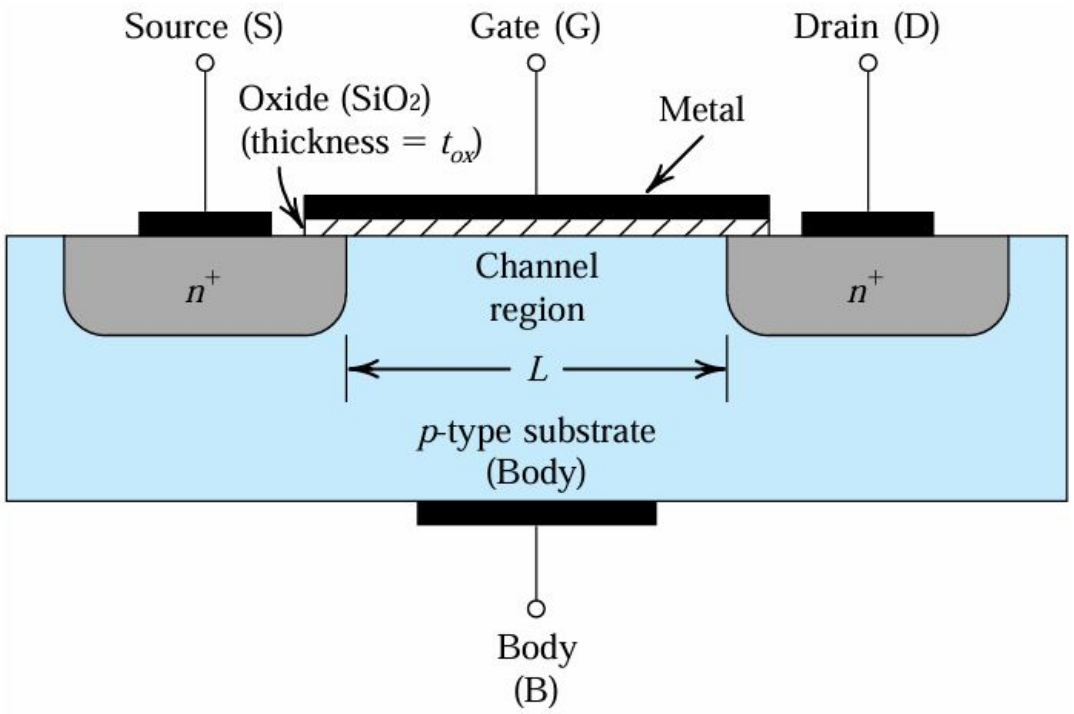
# MOS Logic family

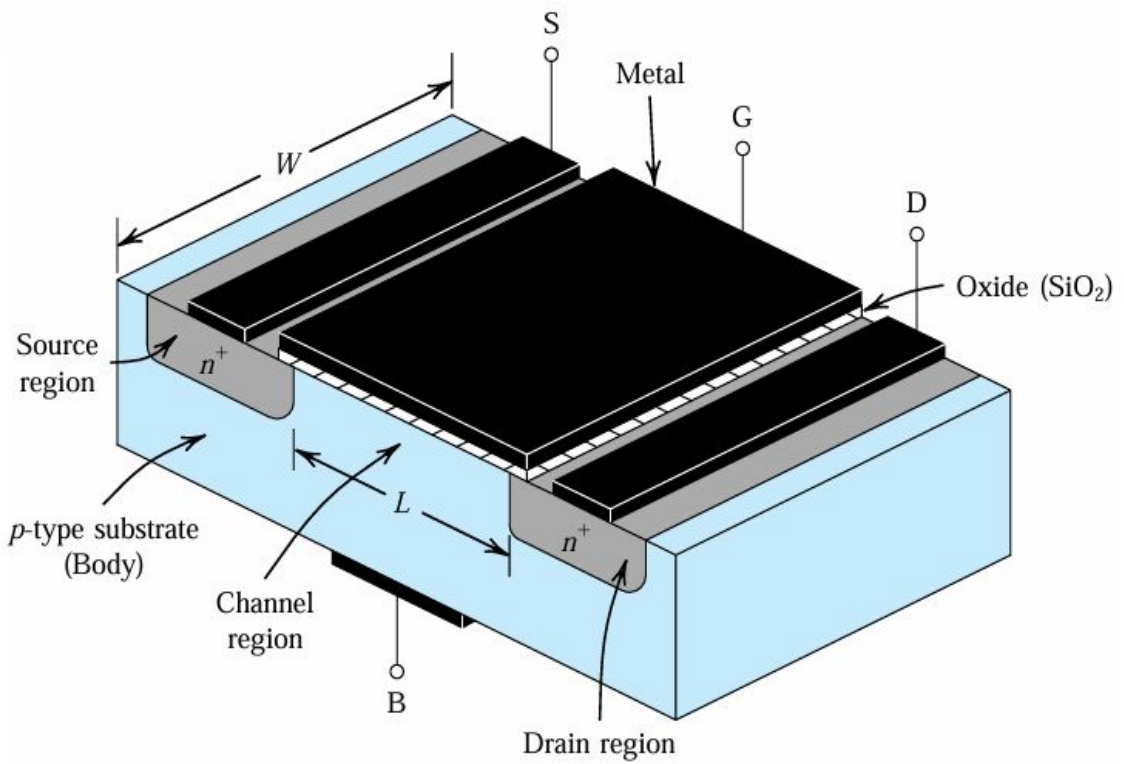
**Unipolar logic family:** current conduction is done by one type of charge carriers.

e.g. electron or hole

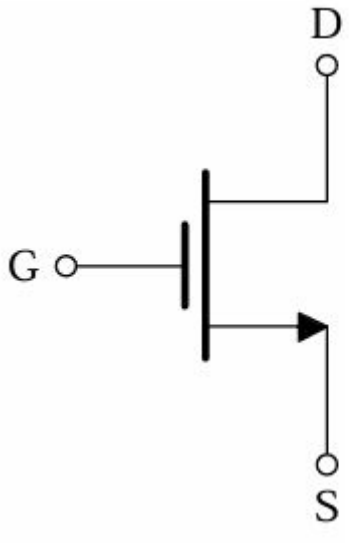
# Basic Internal Structure

If some MOSFET is fabricated identically then source and body might be shorted.

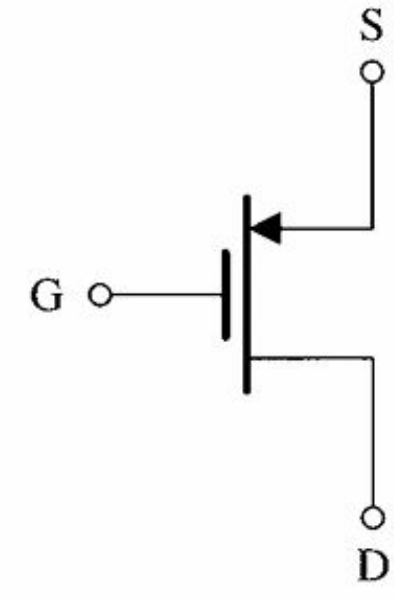


# Circuit Symbol




N-MOS




p-MOS

# Basic Operation

If we apply voltage in the gate terminal.

Accumulation: If $V_G$ is less than zero, holes inside p-type semiconductor might accumulate underneath the oxide layer.

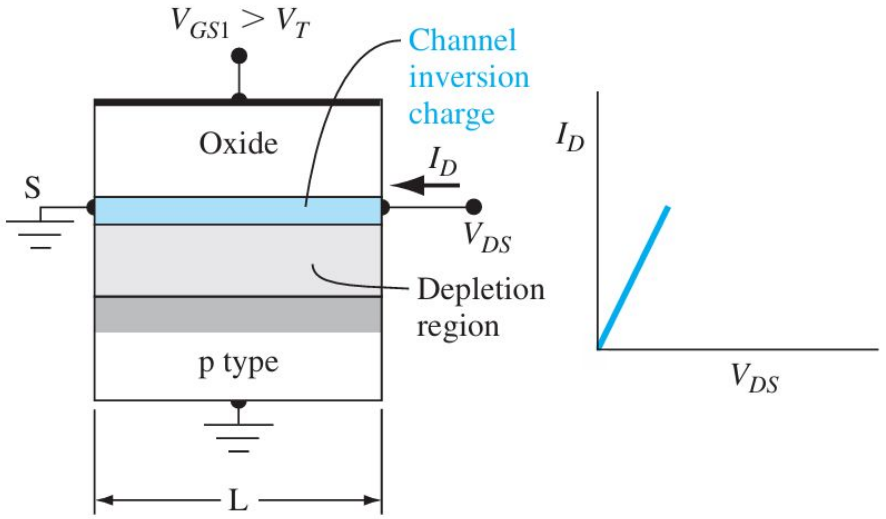
Deplation: If $0 < V_G < V_{TN}$, then deplation layer forms beneath the oxide layer.

Inversion: If $V_G > V_{TN}$ , then an inversion layer would emerge under the oxide layer.

BRAC UNIVERSITY
Inspiring Excellence

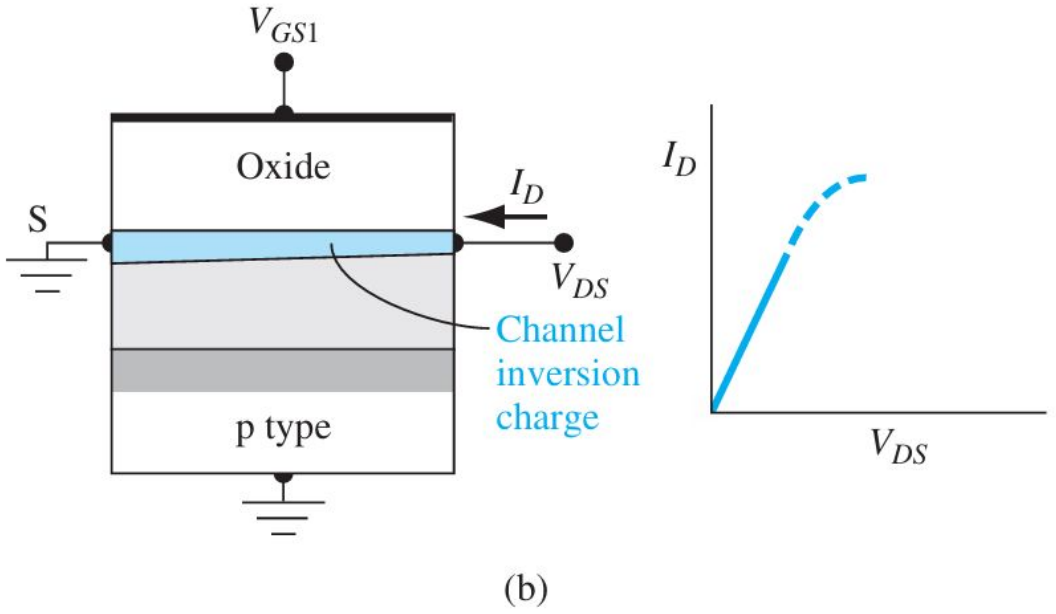
# Basic Operation

Now if we apply $V_{GS} > V_{TN}$, a channel forms.




(a)

NMOS for small $V_{DS}$

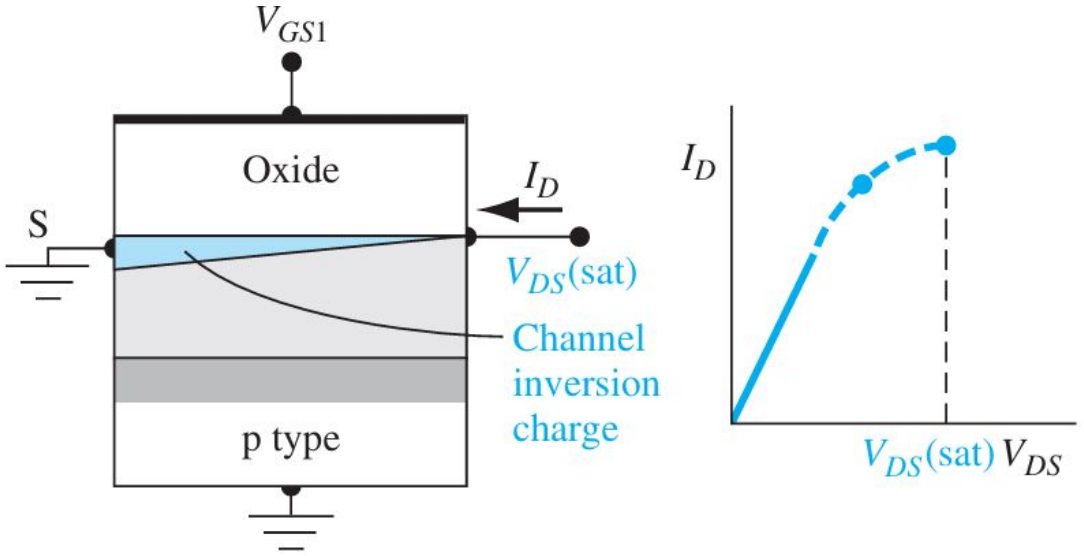



(b)

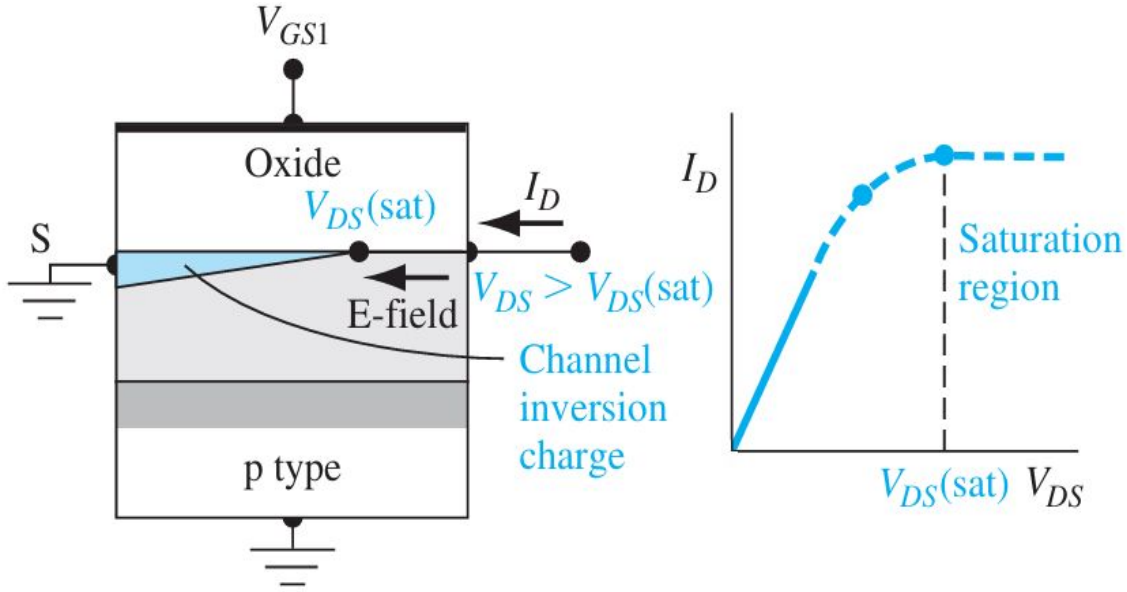
NMOS for increased $V_{DS}$

# Basic Operation

Now if we apply $V_{GS} > V_{TN}$, a channel forms.




(c)




(d)

Edge of Saturation, $V_{DS} = V_{GS} - V_{TN}$

Saturation, $V_{DS} > V_{GS} - V_{TN}$

# Operating modes of MOSFET

Operating modes of n-MOSFET,

- Cut-off

$$V_{GS} < V_{TN}, I_D = 0$$

- Triode/Linear

$$V_{GS} > V_{TN} \; and \; V_{DS} < \; V_{GS} - V_{TN}$$

$$I_D = K_n( \, 2(V_{GS} - V_{TN})V_{Ds} - V_{DS}^2 \, )$$

- Saturation

$$V_{GS} > V_{TN} \; and \; V_{DS} > \; V_{GS} - V_{TN}$$

$$I_D = K_n(V_{GS} - V_{TN})^2$$

**Note:** $\boldsymbol{K_n = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}}$

BRAC UNIVERSITY
Inspiring Excellence

# N-MOS Logic

**Pull up network:** High resistance

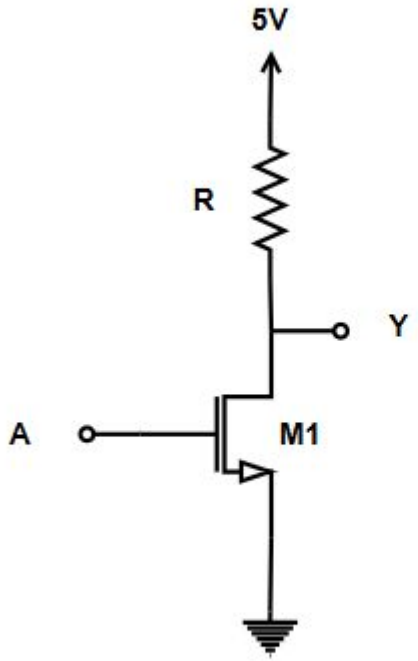
**Pull down network:** n-MOS

**Logic design techniques:**

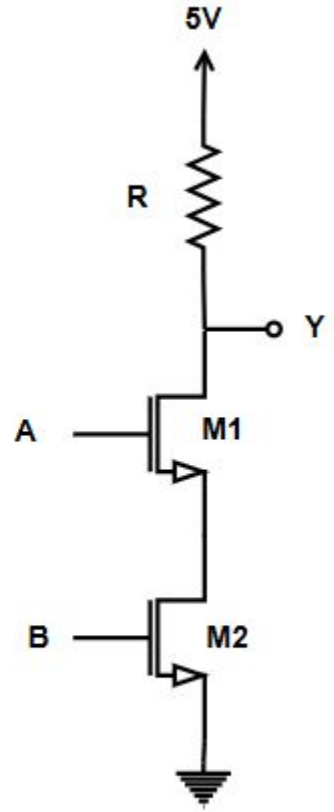
- Series n-MOS indicates AND
- Parallel n-MOS indicates OR
- Overall n-MOS logic is inverted

BRAC UNIVERSITY
Inspiring Excellence

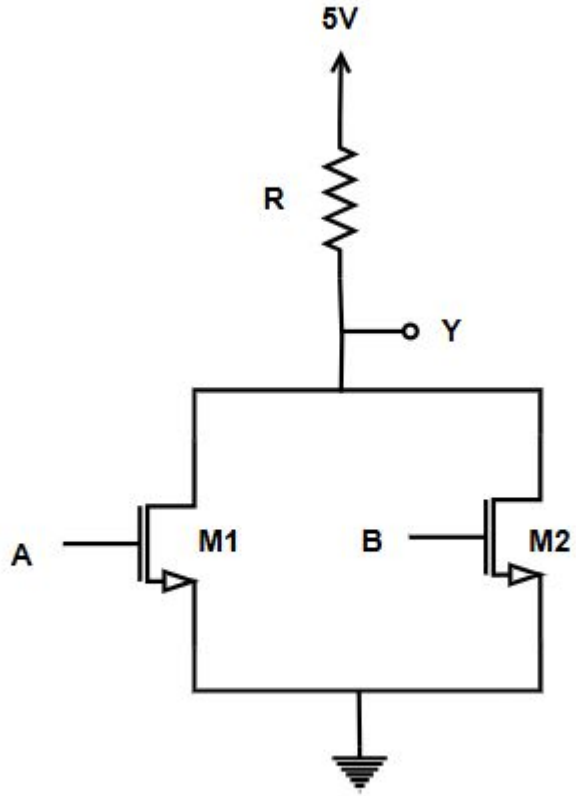
# N-MOS Logic




NOT




NAND

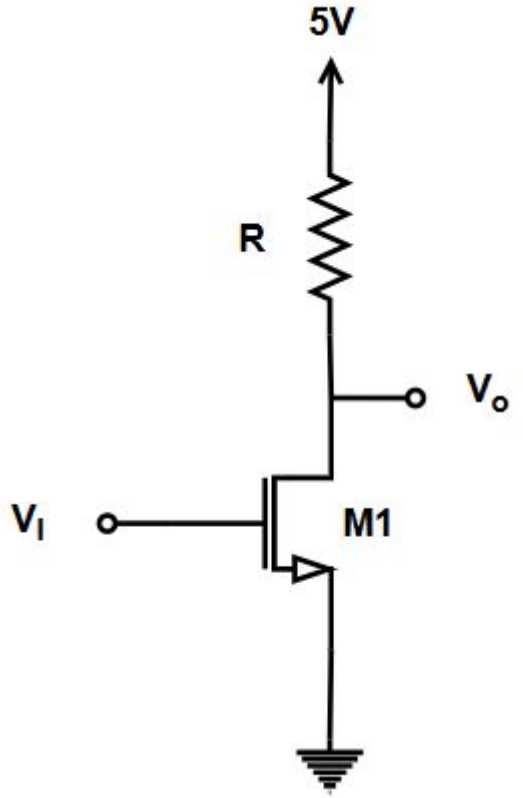



NOR

# N-MOS NOT gate/Inverter

Find the output of the inverter for the input volta
5 V and 1.5 V. Given $V_{TN} = 0.5\ V, R = 20\ k,$

$$V_{DD} = 5V, K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 0.3\ mA/V^2$$



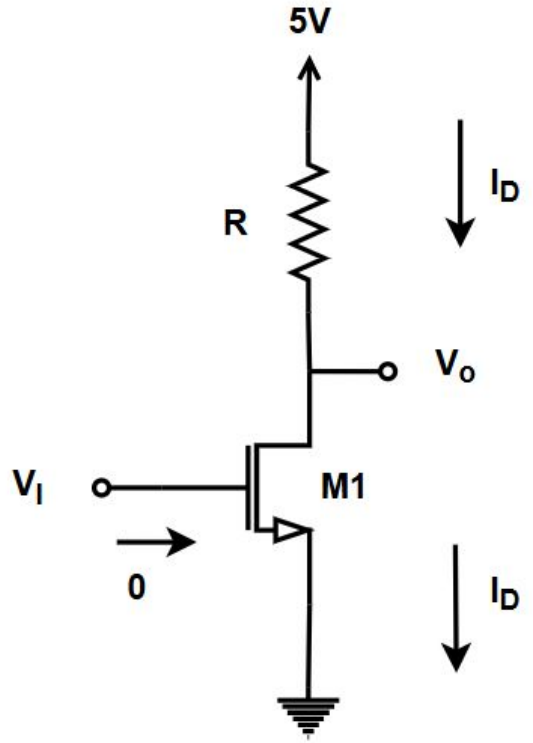
# N-MOS NOT gate/Inverter

When $V_I = 5\ V$
$V_{GS} = 5\ V > V_{TN}$,

MOSFET M1 is in Saturation / Triode region.

Assumption: Triode mode

$$I_D = K_n(\ 2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2)$$
$$I_D = 0.3\ (\ 2\ *(\ 5\ - 0.5)V_o\ - V_o^2)$$
$$= 0.3\ (9V_o\ - V_o^2)$$
$$I_D = \frac{5 - V_o}{20}$$



# N-MOS NOT gate/Inverter

$$I_D = 0.3\,(9V_o - V_o^2)$$

$$I_D = \frac{5 - V_o}{20}$$

So, we can write,

$$0.3\,(9V_o - V_o^2) = \frac{5 - V_o}{20}$$

Solving using calculator,

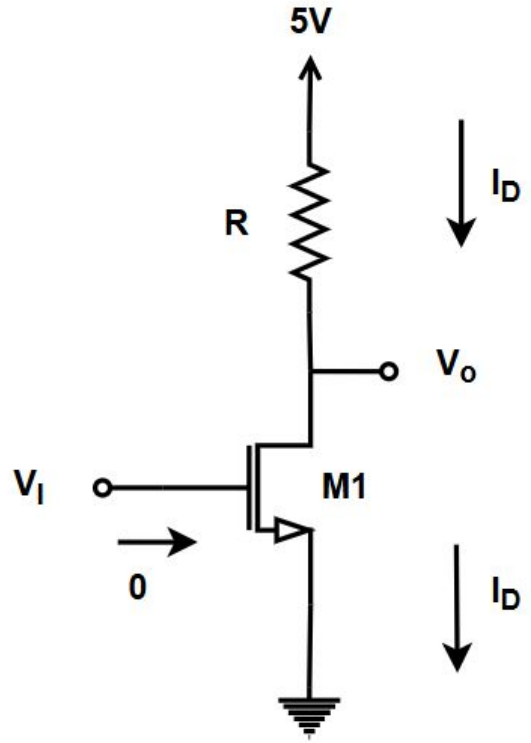
$V_o = 9.074\ V\ or\ 0.092\ V$

Acceptable value, $V_o = 0.092\ V$

Verification:

$V_{DS} = 0.092\ V\ and\ V_{GS} - V_{TN} = 4.5\ V$

As $V_{DS} < V_{GS} - V_{TN}$, Assumption correct.



# N-MOS NOT gate/Inverter

When $V_I = 1.5\ V$
$V_{GS} = 1.5\ V > V_{TN}$,

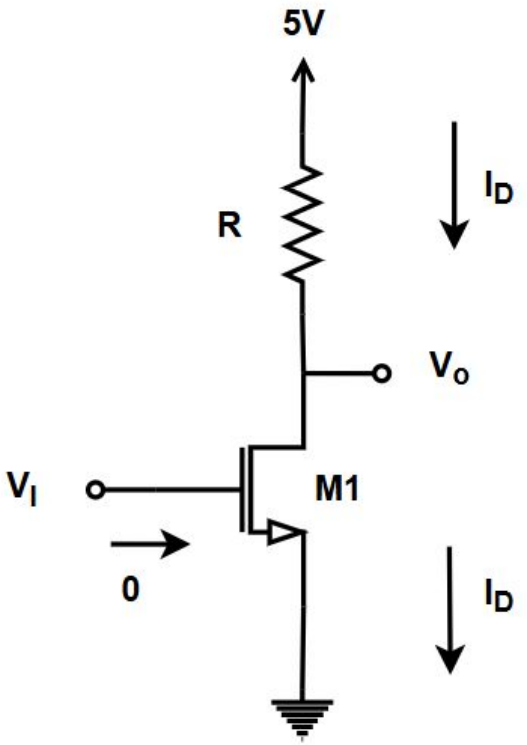
MOSFET M1 is in Saturation / Triode region.

Assumption: Saturation mode

$$I_D = K_n(V_{GS} - V_{TN})^2$$

$$I_D = 0.3(1.5 - 0.5)^2$$

$$I_D = \frac{5 - V_o}{20}$$



# N-MOS NOT gate/Inverter

So, we can write,

$$0.3\ (1.5 - 0.5)^2 = \frac{5 - V_o}{20}$$

Solving using calculator,

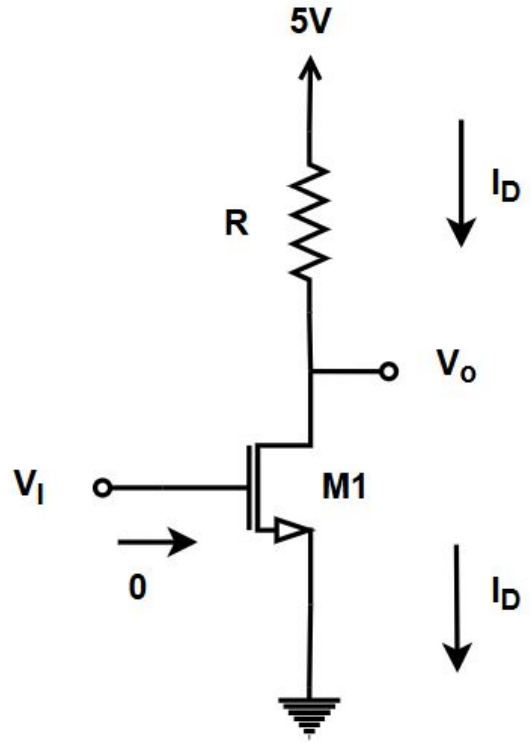
$V_o = -1\ V$

Verification:

$V_{DS} = -1V\ and\ V_{GS}\ - V_{TN} = 1\ V$

As $V_{DS} < V_{GS} - V_{TN}$, Assumption not correct.

We need to assume triode mode as saturation assumption is not correct.



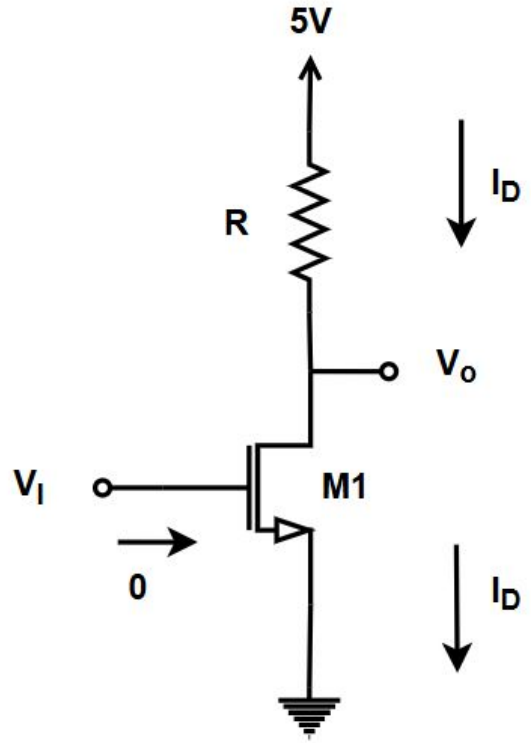
# N-MOS NOT gate/Inverter

$$I_D = K_n( 2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2)$$
$$I_D = 0.3 ( 2 * ( 1.5 - 0.5)V_o - V_o^2)$$
$$= 0.3 (2V_o - V_o^2)$$
$$I_D = \frac{5 - V_o}{20}$$

So, we can write,

$$0.3 (2V_o - V_o^2) = \frac{5 - V_o}{20}$$
$$\Rightarrow 12V_0 - 6V_o^2 = 5 - V_0$$

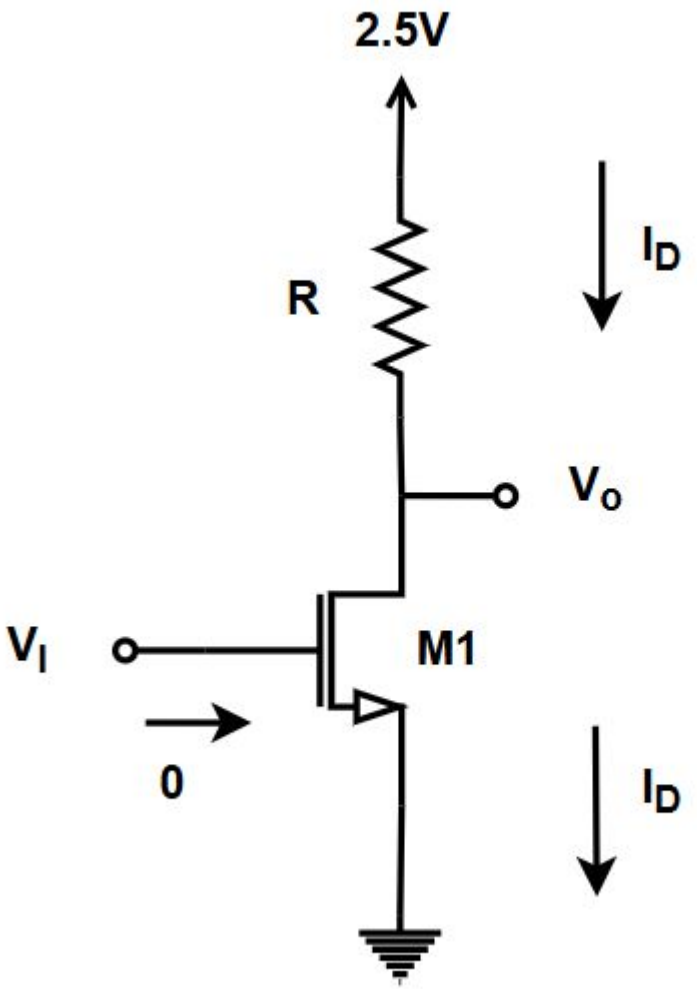
Now Solve and verify



# N-MOS NOT gate/Inverter

Find the transition voltage(Saturation to triode) of the inverter. Given

$V_{TN} = 0.5\,V, R = 20\,, K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 0.3\,mA/V^2$



# N-MOS NOT gate/Inverter

For transition, $V_{DS} = V_{GS} - V_{TN}$

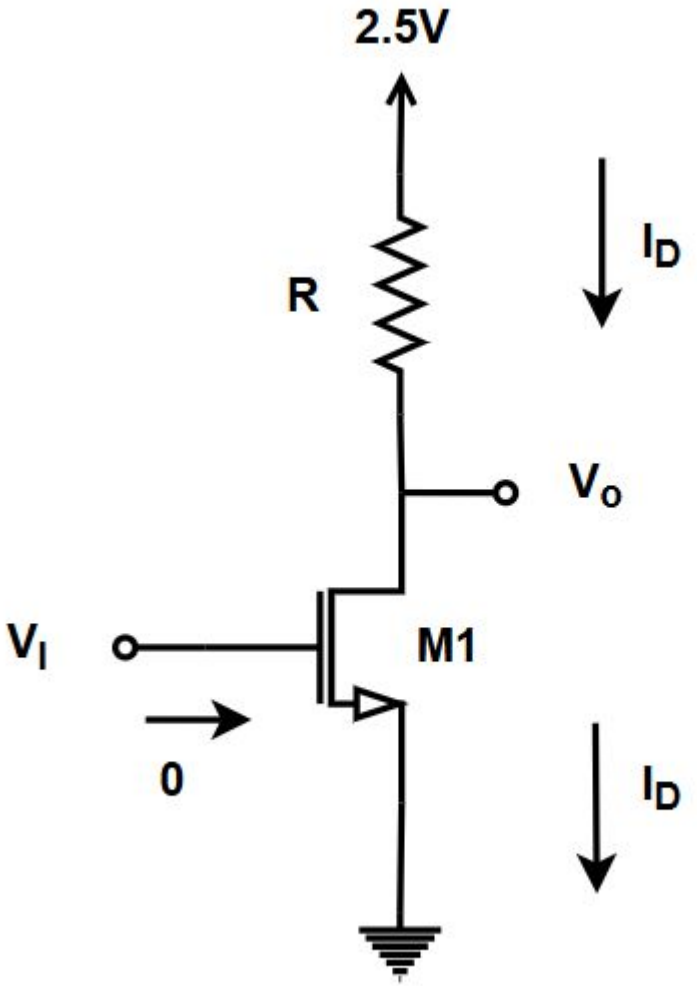
$$V_o = V_I - 0.5$$

Now, $I_D = 0.3\,(V_I - 0.5)^2 = \frac{5 - V_o}{20}$

$$\Rightarrow\ I_D = 0.3\,V_o^2 = \frac{5 - V_o}{20}$$

Solving, $V_o = 0.5675\,V$

$$V_I = V_o + 0.5 = 1.0675\,V$$



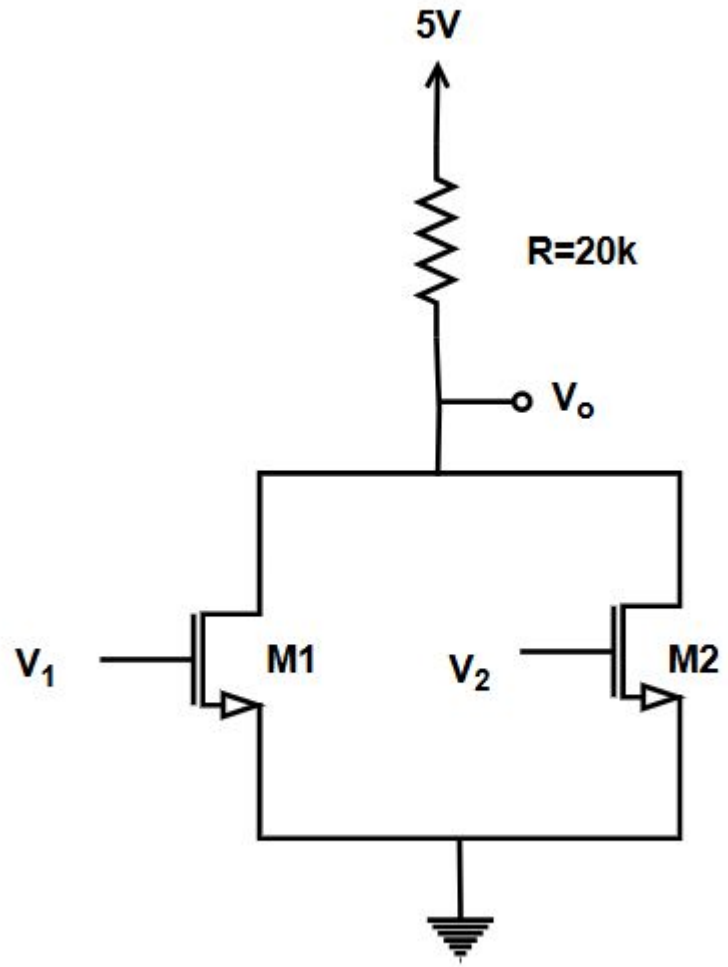
# N-MOS NOR gate

- Here, $V_{TN} = 0.8\,V \; and \; K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 0.1\,mA/V^2$

We can study this NOR gate, with four possible cases.

We need to find out $I_1, I_2, I, V_o \; and \; power$ of the NOR gate

| | | |
|---|---|---|
| 0 | 0 | |
| 0 | 5V | |
| 5V | 0 | |
| 5V | 5V | |



# N-MOS NOR gate

Case 01: $V_1 = V_2 = 0V$

$V_{GS1} = 0 < V_{TN}$,

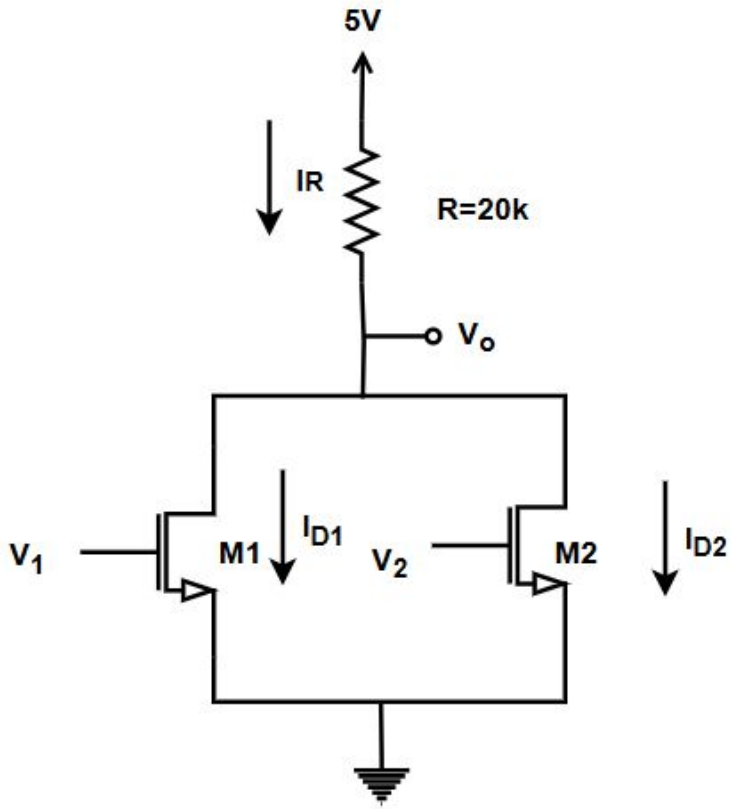
$M1 \rightarrow Cut\ off\ Mode, I_{D1} = 0\ mA$

$V_{GS2} = 0 < V_{TN}$

$M2 \rightarrow Cut\ off\ Mode, I_{D2} = 0\ mA$

$I = I_{D1} + I_{D2} = 0\ mA$

$V_o = 5\ V$



# N-MOS NOR gate

Case 02: $V_1 = 0V, V_2 = 5V$

$V_{GS1} = 0 < V_{TN}$,

$M1 \rightarrow Cut\ off\ Mode, I_{D1} = 0\ mA$

$V_{GS2} = 5 > V_{TN}$

*Assume M2 in Triode mode*

$I_{D2} = 0.1\ (2(5 - 0.8)V_o - V_o^2)$

$I = I_{D1} + I_{D2}$

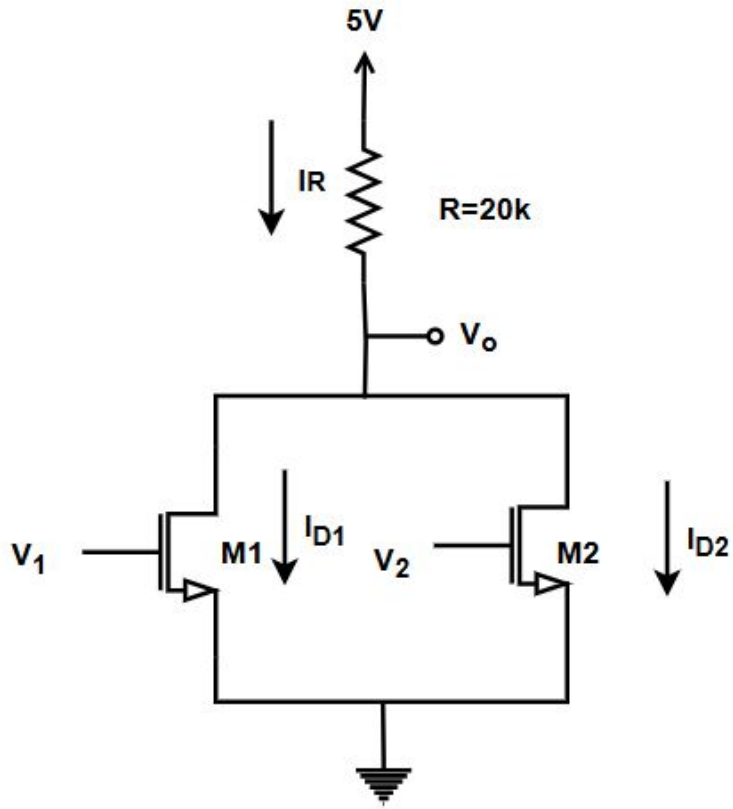
$$\frac{5 - V_o}{20} = 0.1\ (2(5 - 0.8)V_o - V_o^2)$$

Solving,

$V_o = 8.6\ V\ or\ 0.29\ V$( $8.6\ V\ is\ not\ acceptable$)

Verification: $V_{DS} = 0.29V\ and\ V_{GS} - V_{TN} = 4.2\ V$

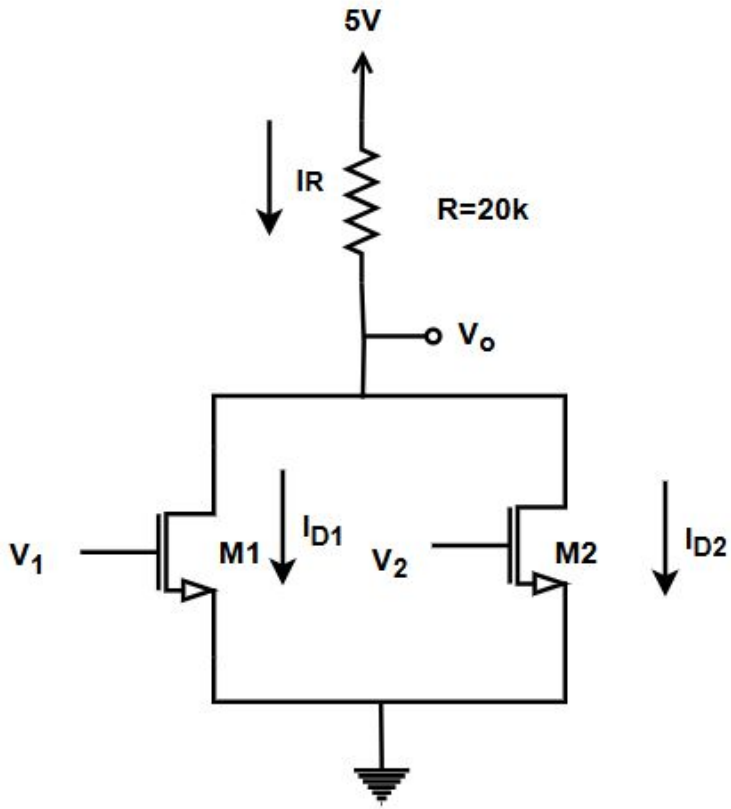
As, $V_{DS} < V_{GS} - V_{TN}, M2\ is\ in\ Triode$



# N-MOS NOR gate

Case 03: $V_1 = 5\ V,\ V_2 = 0V$

Similar to case 2,
$\Rightarrow V_o = 0.29\ V$



# N-MOS NOR gate

Case 04: $V_1 = V_2 = 5V$

$V_{GS1} = 5 > V_{TN}$,

$M1 \rightarrow Triode$

$V_{GS2} = 5 > V_{TN}$

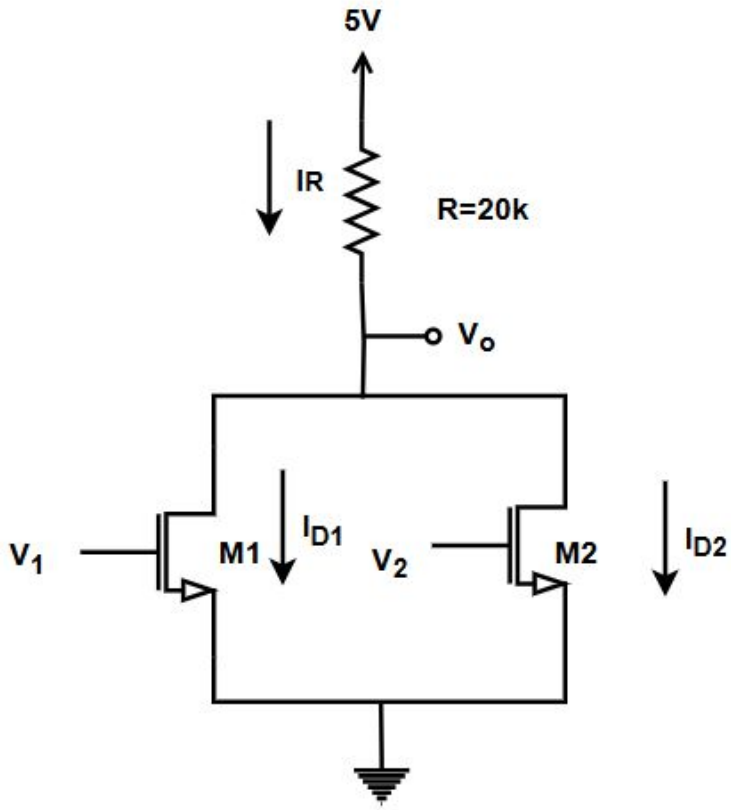
$M2 \rightarrow Triode$

$I = I_{D1} + I_{D2}$

$$\Rightarrow \frac{5 - V_o}{20} = 2 * 0.1\,(2(5 - 0.8)V_o - V_o^2)$$

$V_o = 0.149\,V\ or\ 4.17\,V(\ 4.17\,V\ is\ not\ acceptable)$

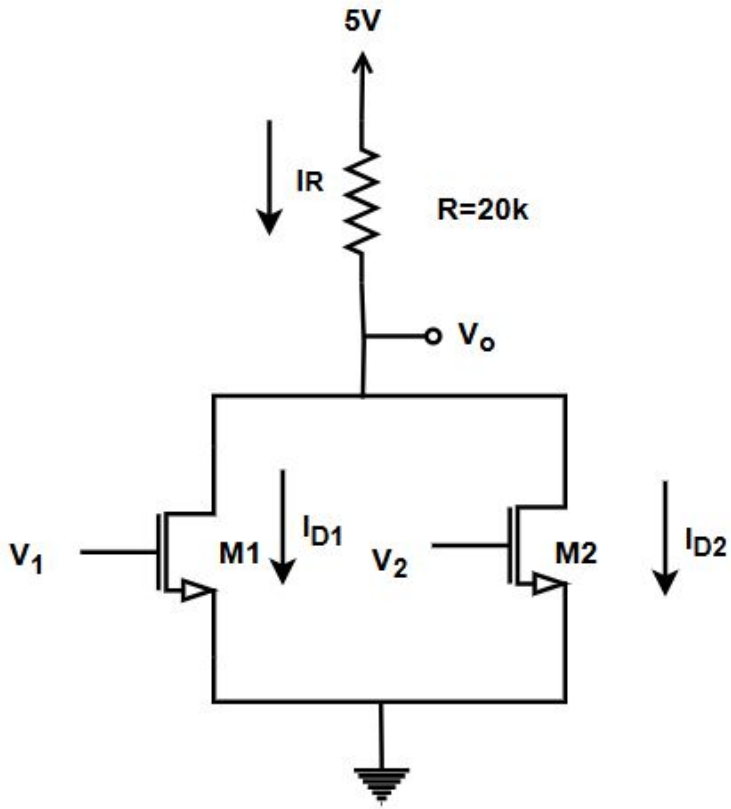
$\Rightarrow V_o = 0.149\,V$



# Exercise:

For the Given NMOS find the power for all possible input cases. Also find it's average power.

Given: $K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = 100\frac{\mu A}{V^2}, V_{TN} = 1\,V. Logic\ High = 5\,V\ and\ Logic\ Low = 0V$



# CMOS

Complementary MOS circuit design

Features,

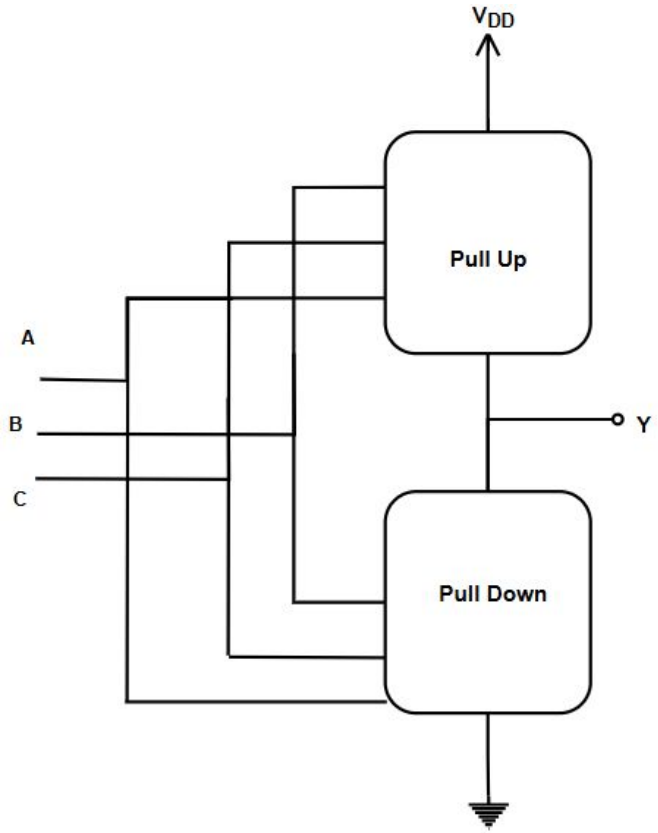
I. In CMOS circuit there are two network, one is pull up and other is pull down.

II. At a time either pull-up or pull-down network is on.

III. Logic is high when pull up is on.

IV. Logic is Low when pull down is on.

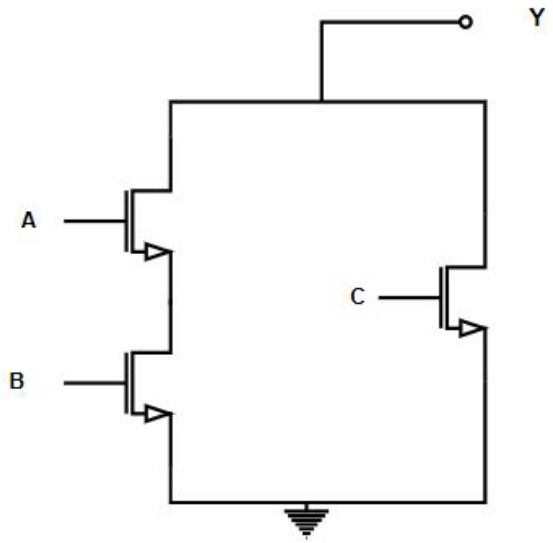
V. Pull down consist of N-MOS, Pull up consist of P-MOS.



# CMOS Pull Down Network Design

. $\rightarrow AND\ can\ be\ implemented\ by\ series\ of\ two\ NMOS$
$+ \rightarrow OR\ can\ be\ implemented\ by\ Parallel\ NMOS$
$lower\ part\ will\ be\ connected\ with\ GND$
$Upper\ part\ will\ be\ connected\ to\ the\ Output$

Example: $Y = \overline{AB + C}$



# CMOS Pull Up Network Design

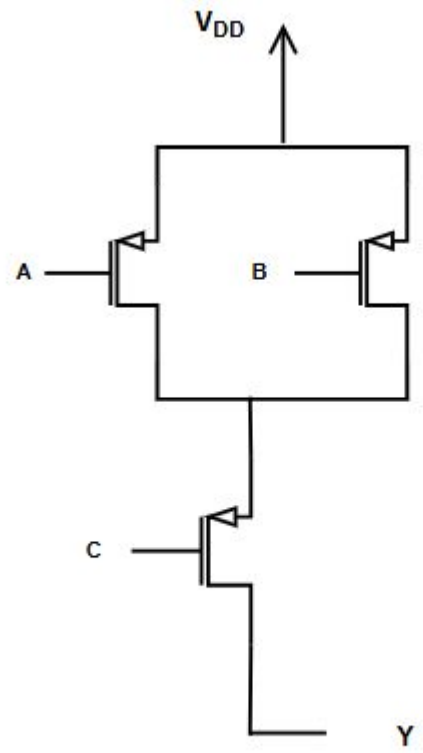
$\cdot \rightarrow AND\ can\ be\ implemented\ by\ parallel\ of\ two\ PMOS$

$+ \rightarrow OR\ can\ be\ implemented\ by\ Parallel\ NMseries\ of\ two\ NMOS$

$Lower\ part\ will\ be\ connected\ to\ the\ Output$

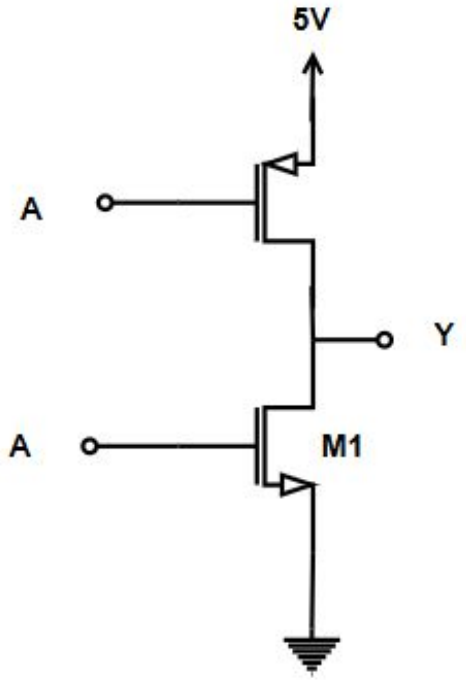
$Upper\ part\ will\ be\ connected\ with\ V_{DD}$

Example: $Y = \overline{AB + C}$



# NOT Gate

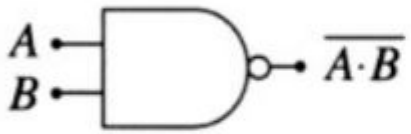
- $Y = \bar{A}$




NOT

# NAND Gate

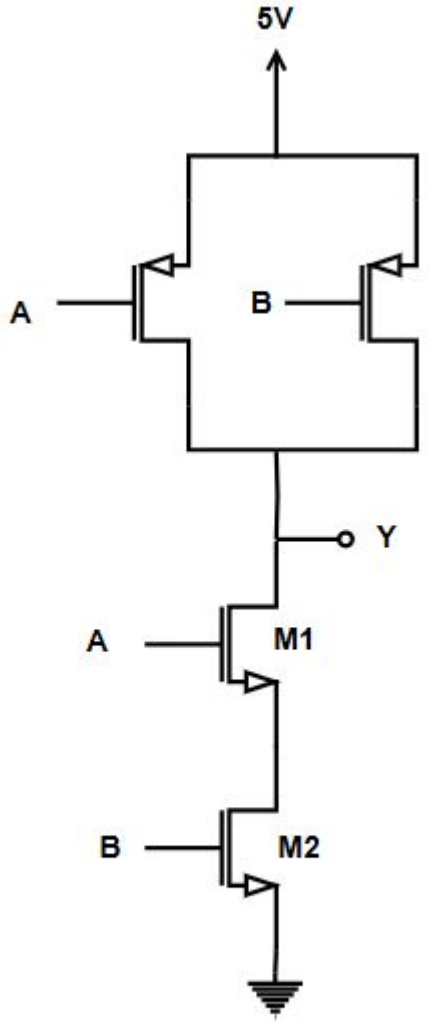
- $Y = \overline{AB}$




(a) Symbol

| $A$ | $B$ | $\overline{A \cdot B}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

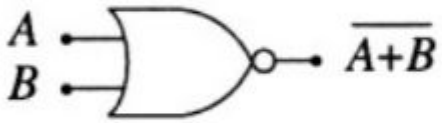
(b) Truth table




NAND

# NOR Gate

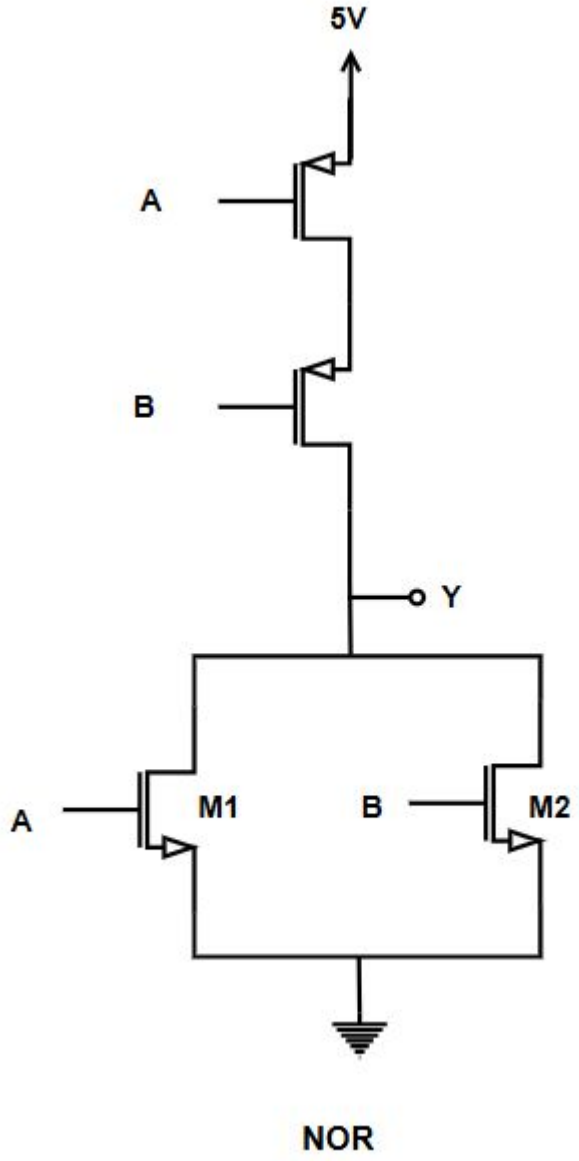
- $Y = \overline{A + B}$




(a) Symbol

| A | B | $\overline{A+B}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

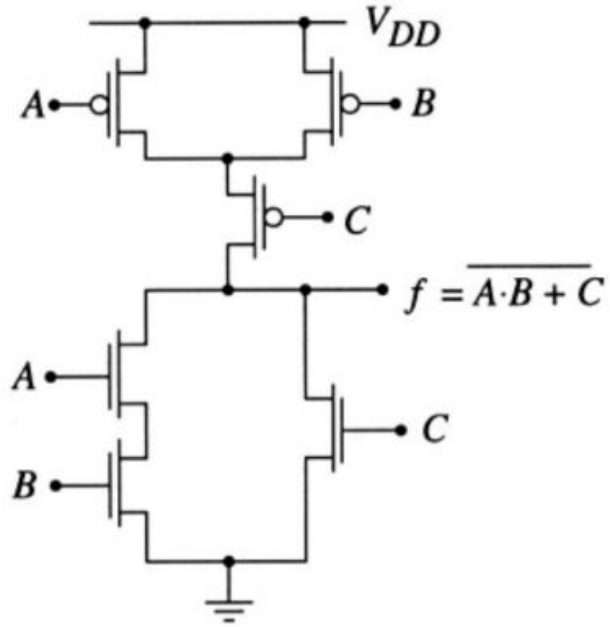
(b) Truth table




NOR

# Example:

$$Y = \overline{AB + C}$$



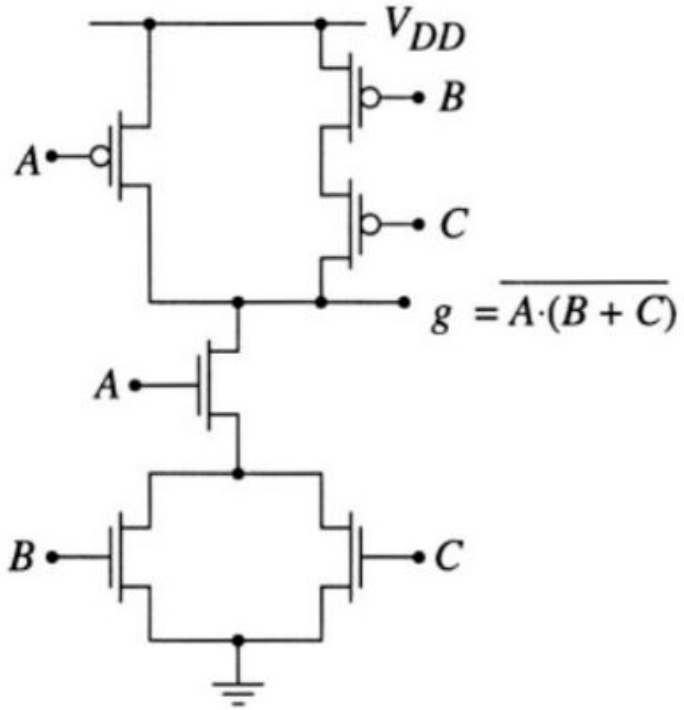

(a) Logic circuit

| A | B | C | f | |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | |
| 0 | 0 | 1 | **0** | ← C=1 |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | **0** | ← C=1 |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | **0** | ← C=1 |
| 1 | 1 | 0 | **0** | ← A·B =1 |
| 1 | 1 | 1 | **0** | ← C=1 |

(b) Function table

# Example:

$$Y = \overline{A(B + C)}$$



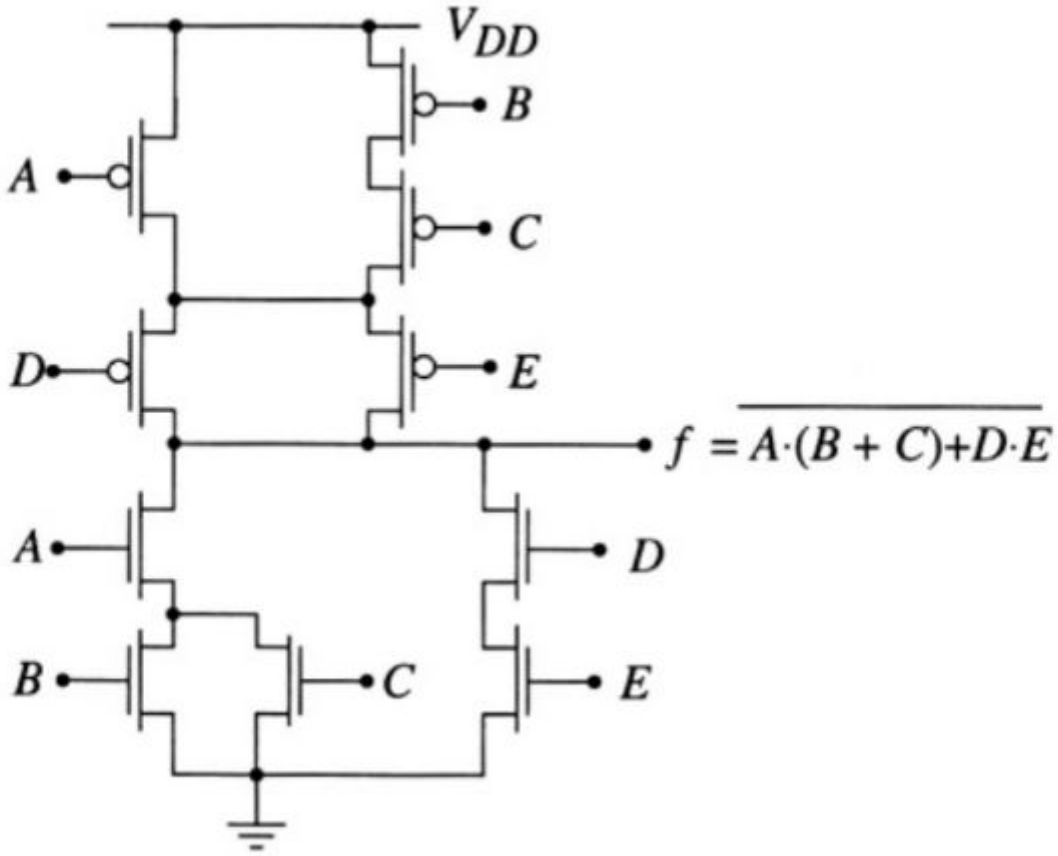

(a) Logic circuit

| A | B | C | g | |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | **0** | ← $A \cdot C = 1$ |
| 1 | 1 | 0 | **0** | ← $A \cdot B = 1$ |
| 1 | 1 | 1 | **0** | ← $A \cdot (B+C) = 1$ |

(b) Function table

# Example:

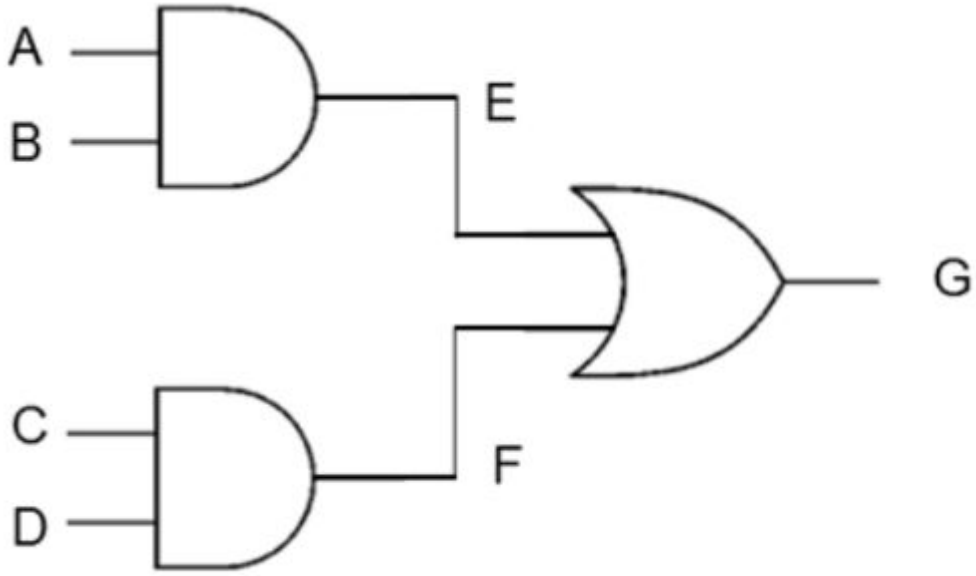
$$Y = \overline{A(B + C) + DE}$$



# Exercise:

Design a CMOS logic circuit to implement the given compound gate in Figure below. First derive

the logical expression of output Y and then design the CMOS network.



# Exercise:

Design a CMOS circuit that will follow the given truth table.

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# Exercise:

Design static CMOS circuit for the following expression,

$$Y = AB + C$$

$$Y = (A+B)C$$

$$Y = (A+B)(C+D)$$

$$Y = \overline{AB + CD}$$

$$Y = \overline{AB + C}$$

$$Y = \overline{(A + B)C}$$

$$Y = \overline{(A + B)(C + D)}$$

$$Y = \overline{A} + \overline{B} + \overline{C}$$