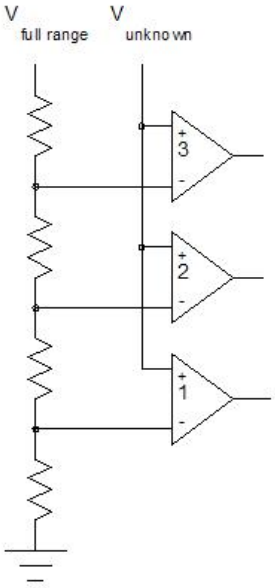
ADC and DAC practice problem

1. An analog signal in the range of -5V to 5V is to be converted to a digital signal. Suppose a 2 bit quantization will be implemented.
   a. What is the step size of the ADC circuit?
   b. How many quantization levels are there ?
   c. Find the maximum value of the quantization error.
   d. Calculate the number of resistors and OP-AMP required for the Flash ADC circuit.
   e. Make a table with quantization range, quantization level and encoded binary value.
   f. At some instances the signal values of the ADC circuit are 3.35V, -2.67V and 1.14 V. Find corresponding encoded binary value.
   g. Explain the input and output relationship osf the Encoder with a table.

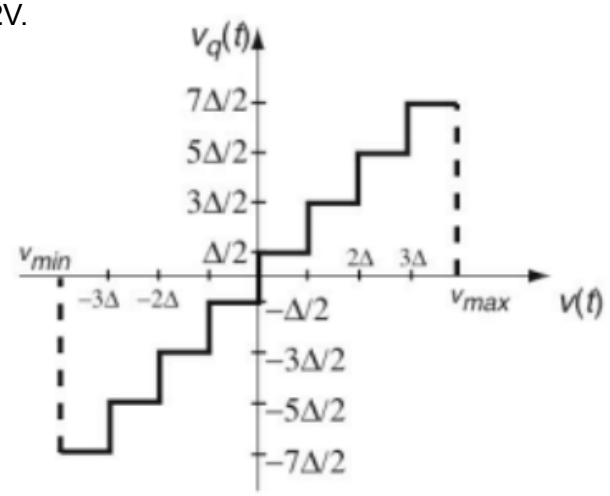
2.



Here,
R = 10 k, Vfullrange = 10 V. (Reference Voltage)
   a. What will be the output binary bits line for the above circuit?
   b. Draw the quantization level vs Input signal plot.
   c. If Vunknown = 3.5 V, what will be the quantization error for this case? (Quantization error = Actual value - Quantized value)

3. x(t) = 5 + 5 sin (2*pi * f *t) V
Where f = 2 k Hz.
Above signal will be converted to a digital signal through an ADC circuit.
   a. What will be the minimum required sampling frequency for this signal?
   b. Suppose, the sampling frequency is set at 10 kHz. Find the first 5 sampling values as well as their corresponding quantized value and encoded value.

4. The following plot is the relationship between input and output of a midrise quantizer. Where the step size is 2V.

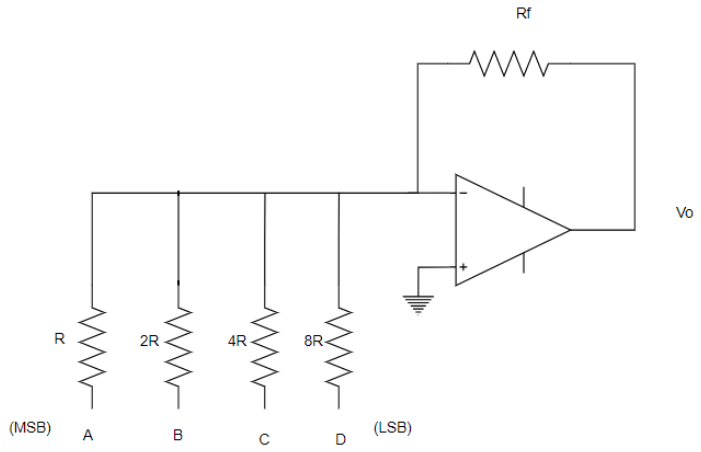


midrise quantizer

a. What is the number of binary bits required to express the quantization levels?
b. Find the corresponding quantized value if the inputs of the quantizer are -5.6 V and 7.34 V.
c. What will be the maximum value of the quantization error?
d. Design a full ADC circuit consisting of maximum current of the circuit should not exceed 0.1 mA.

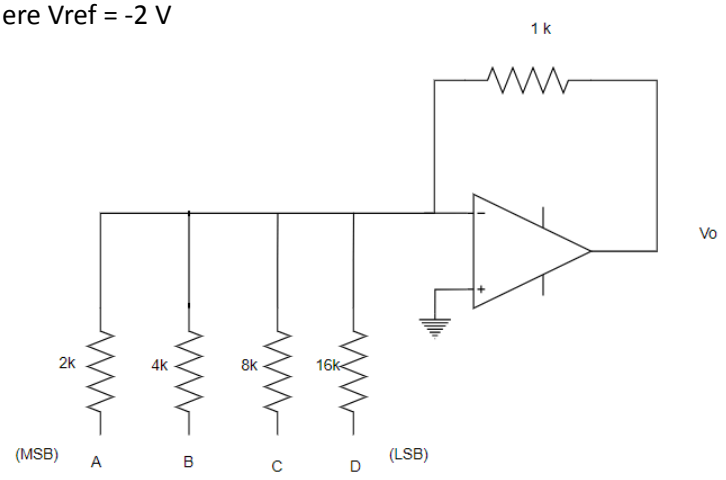
5. Design a 4 binary weighted DAC circuit with reference voltage of 5 V and maximum output voltage of 15V.

6. Here Rf = 2 kΩ and R = 4 kΩ, Vref = -5 V.



a. What will be the maximum and minimum output voltages?
b. What is the step size of this DAC circuit?
c. What is the resolution of this DAC scheme?
d. Make a table for all the combinations of inputs and outputs.
e. Find the output value for the binary inputs 1101, 0001 and 1110, 0001, 1000

7. Here Vref = -2 V



a. Calculate the output value for 1111 and 1010 input value.
b. What will be the resolution of this circuit?
c. Redesign the circuit by changing the value of the feedback resistor so that maximum output voltage will be 7.5 V.