CSE 350
Digital Electronics and Pulse Techniques

DTL - NAND Gate

BRAC UNIVERSITY
Inspiring Excellence

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DTL

DTL : Diode Transistor Logic

Bipolar :

Saturated (Switching transistor will be operating in cutoff or saturation mode)

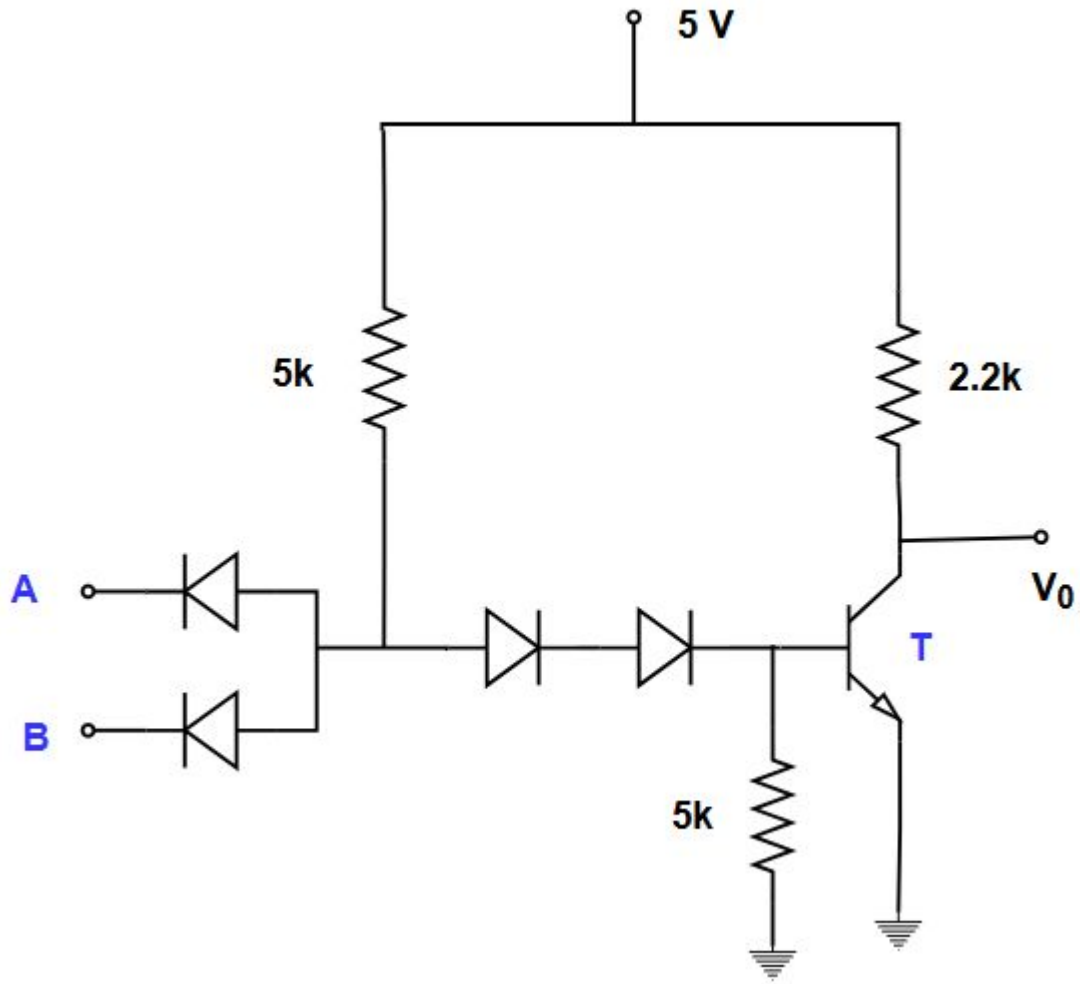
Input terminals connect through a diode to a transistor’s base terminal.

DTL NAND Gate

Basic Operation:

DTL NAND Gate

2 input AND gate + Inverter



DTL NAND Gate

Basic Operation:

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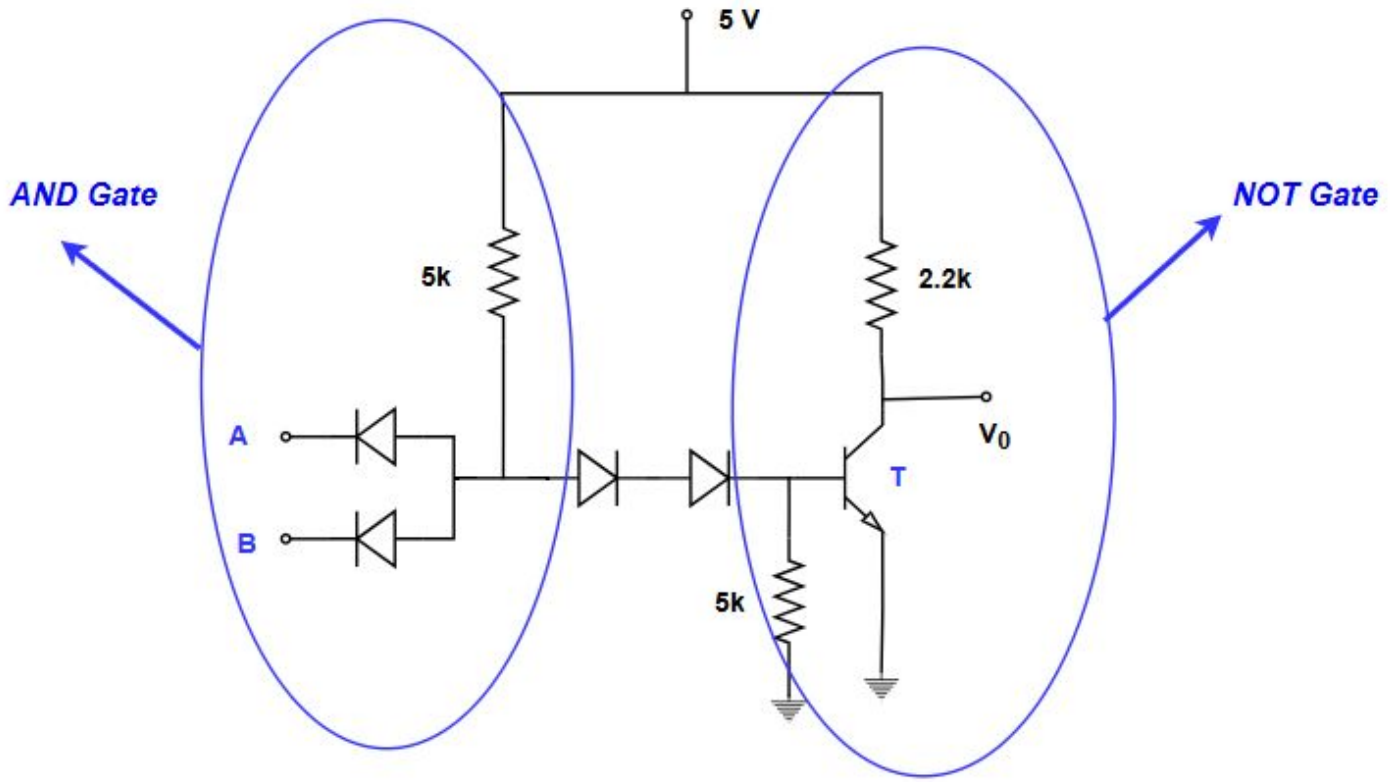
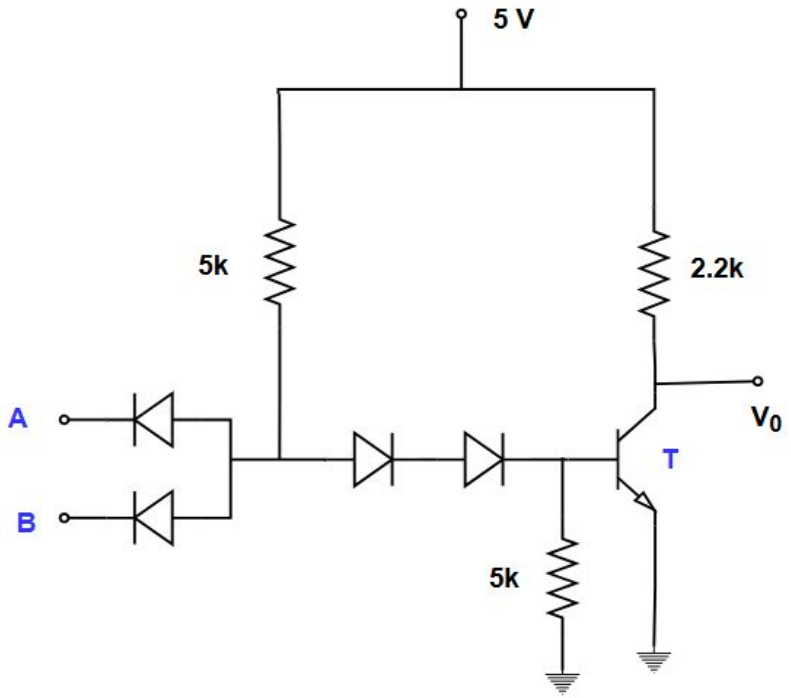


DTL NAND Gate

Example: Calculate the currents and node voltages for the following DTL gate. Verify it is a NAND gate. Input of the DTL NAND gate might be connected to the output of other DTL NAND gate.



DTL NAND Gate

V_A	V_B	V_o
0.2	0.2	
0.2	5	
5	0.2	
5	5	

DTL NAND Gate

Case 01:

$V_A = low = 0.2\ V$

$V_B = low = 0.2\ V$

Assume ,

The anode voltage Vp might be higher than the cathode voltages of D1 and 2 diode.

D1 and D2 are conducting , Thus $V_{D1} = 0.7\ V, V_{D2} = 0.7\ V$

According to the assumption, $V_P = 0.2 + 0.7 = 0.9\ V$

DTL NAND Gate

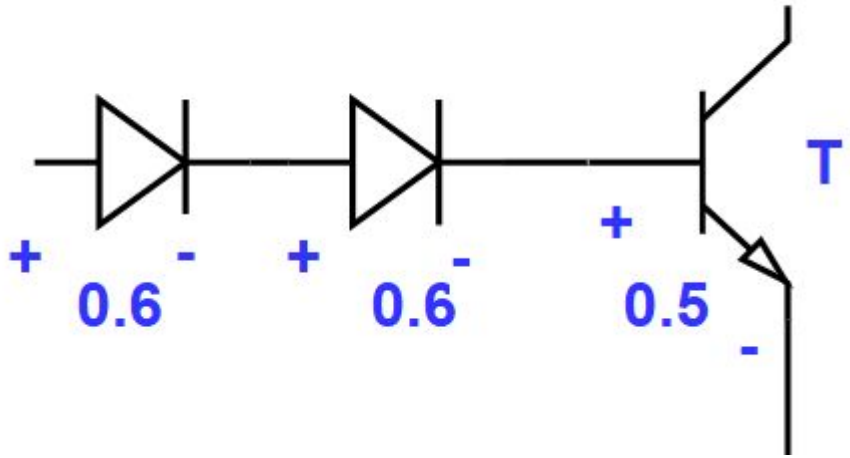
In order for T transistor to turn on we need to have V_{BE} = 0.5 (cut in voltage of transistors) , we also need to have VD3 = VD4 = 0.6 V (Cut in voltage for diode)

As a total we require,

VD3 + VD4 + V_{BE} = 0.6 + 0.6 + 0.5 = 1.7 V at p node to turn on the right side of the circuits.

Necessary condition to turn the transistor T.

If V_P = 0.9 V, then T can not turn on. This justifies our assumption.



DTL NAND Gate

Now we can calculate the current and voltages.

T → cutoff

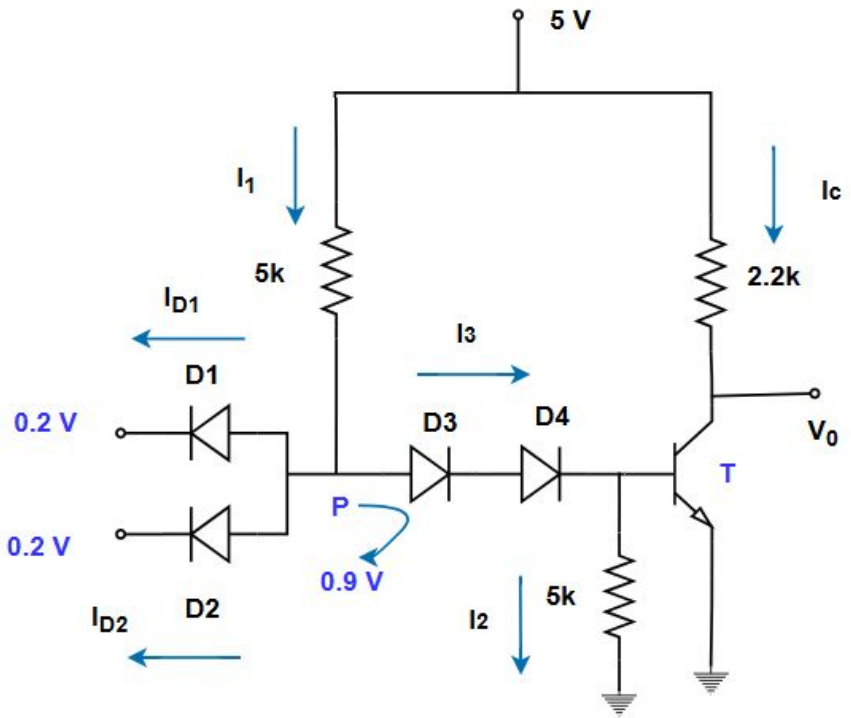
D1, D2 → conducting

D3, D4 → off,

$V_p = 0.9\ V$, $I_C = I_B = 0$, $Vo = 5\ V$

$I_3 = 0$, $I_2 = 0$

$$I_1 = \frac{5 - 0.9}{5k} = 0.82\ mA$$



$I_{D1} = I_{D2}$ *because both of the branches are identical*

$$I_{D1} = \frac{I_1}{2} = 0.41\ mA = I_{D2}$$

DTL NAND Gate

Case 2:

$V_A = 0.2\ V$

$V_B = 5\ V$

Assume, $D1$ is conducting and $D2$ is off.

This implies,

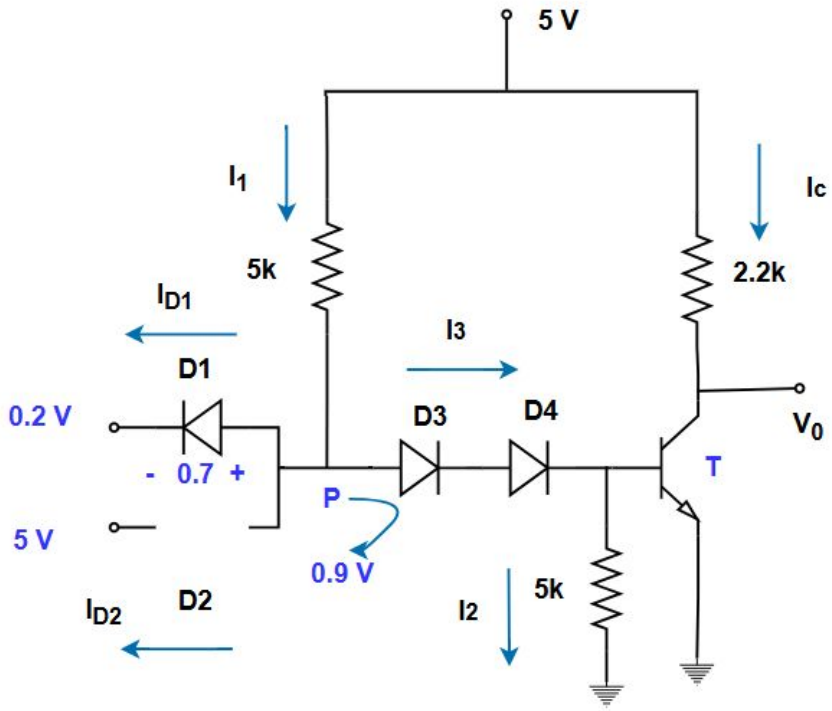
$V_p = 0.9\ V$

we need at least $V_p < 1.7\ V$ to turn on T transistor. It again justifies our assumption.

$I_c = I_B = I_3 = I_2 = 0\ mA, I_1 = 0.82\ mA$

$I_{D2} = 0\ mA\ and\ I_{D1} = 0.82\ mA$

$V_o = 5\ V$



DTL NAND Gate

Case 3:

$V_A = 5\ V$

$V_B = 0.2\ V$

Assume, $D2$ is conducting and $D1$ is off.

This implies,

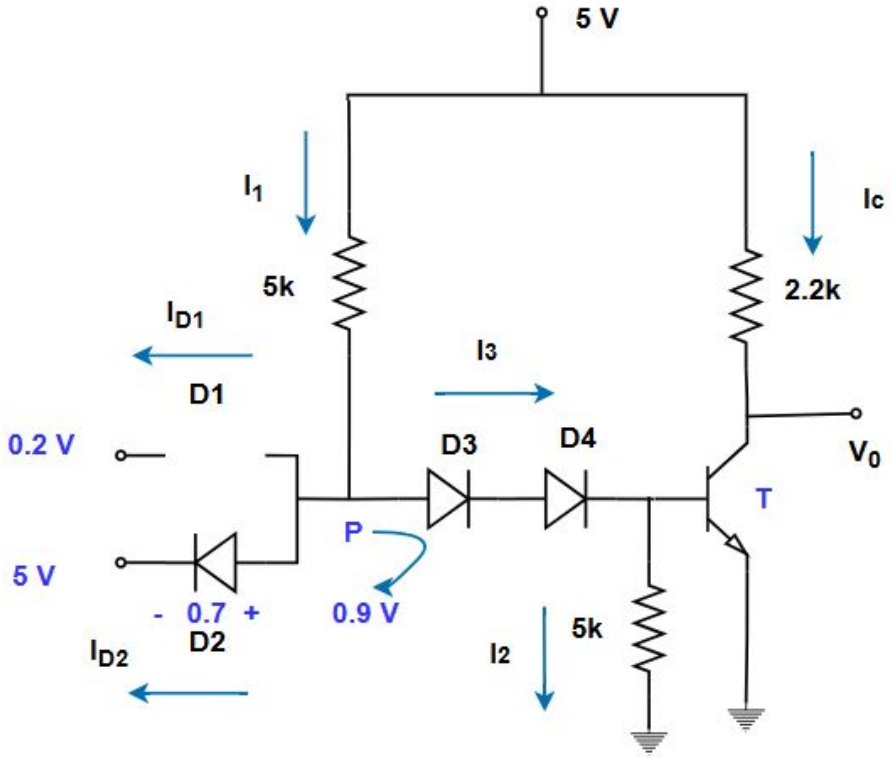
$V_p = 0.9\ V$

we need at least $V_p < 1.7\ V$ to turn on T transistor. It again justifies our assumption.

$I_c = I_B = I_3 = I_2 = 0\ mA, I_1 = 0.82\ mA$

$I_{D1} = 0\ mA\ and\ I_{D2} = 0.82\ mA$

$V_o = 5\ V$



DTL NAND Gate

Case 4:

$V_A = 5\ V$

$V_B = 5\ V$

Assume, $D1$ is off and $D2$ is off.

$$I_{D1} = I_{D2} = 0\ mA$$

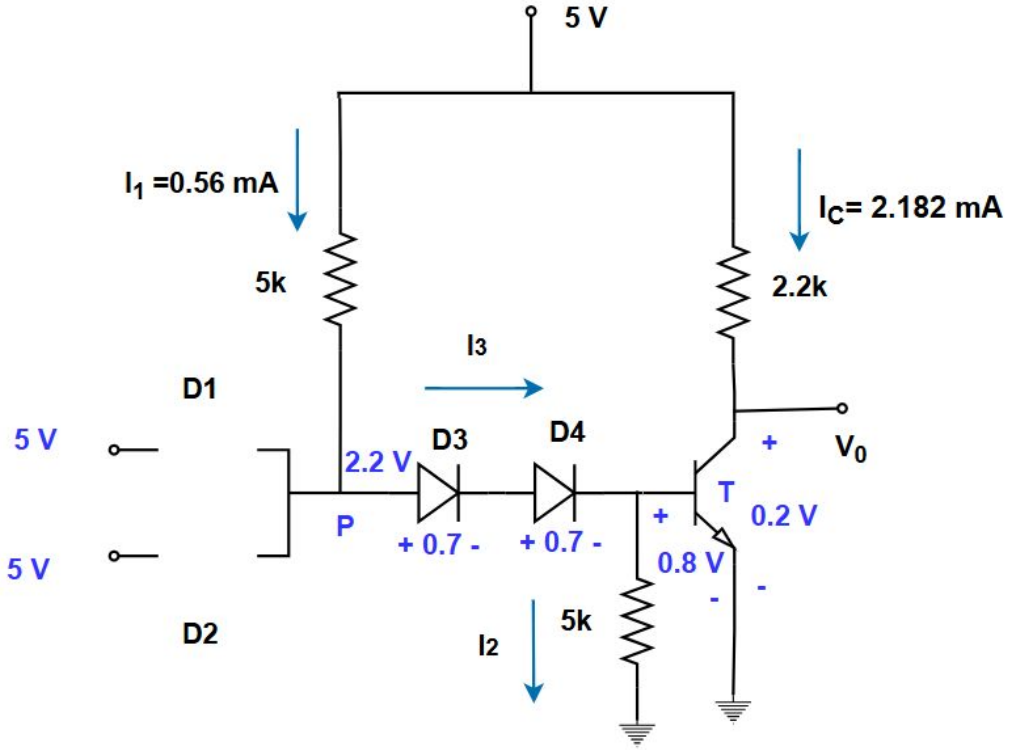
Therefore, D3, D4 , T must be ON.

Because it is a DTL circuit . The switching transistor must operate in saturation mode when it is turned on.

$$V_{CE} = 0.2\ V\ , V_{BE} = 0.8\ V$$

$$V_{D3} = V_{D4} = 0.7\ V$$

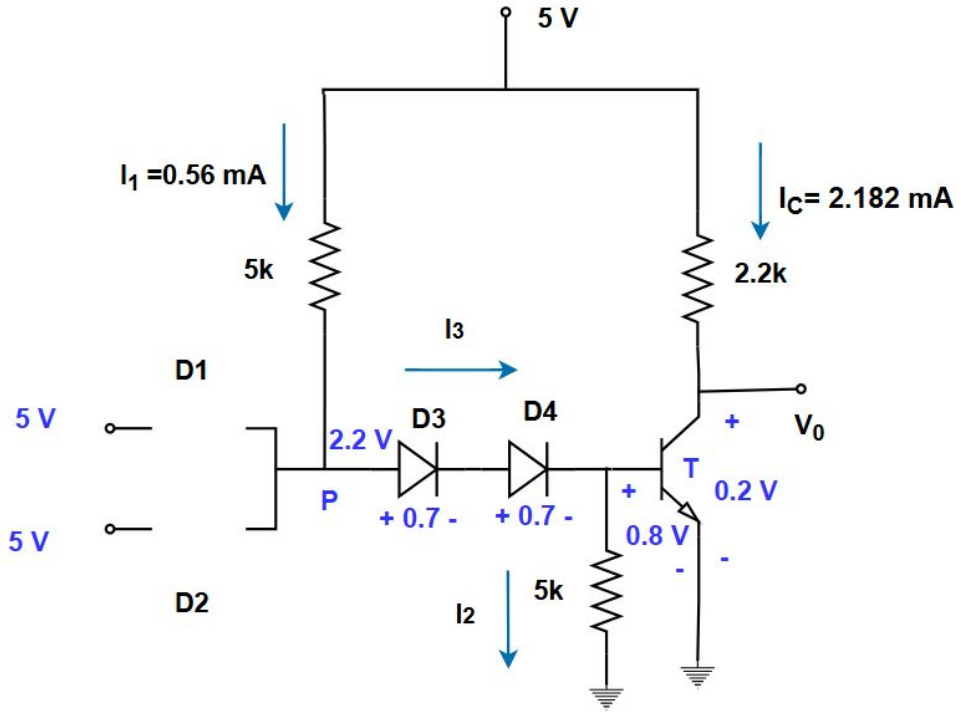
$$[\ Conduction\ voltage\ of\ diode]$$



DTL NAND

$$V_p = 0.7 + 0.7 + 0.8 = 2.2\ V$$

Finally we have anode voltage of D1 and D2 is smaller than cathode voltage. They justifies our assumption.



Current calculation

$$I_1 = \frac{5 - 2.2}{5k} = 0.56\ mA$$

$$I_2 = \frac{0.8 - 0}{5k} = 0.16\ mA$$

$$I_B = I_3 - I_2 = 0.4\ mA$$

$$I_C = \frac{5-0.2}{2.2k} = 2.182\ mA$$

DTL NAND

From the analysis we can get, the input output relationship. This indicates a NAND gate.

VA	VB	Vo
0.2	0.2	5
0.2	5	5
5	0.2	5
5	5	0.2