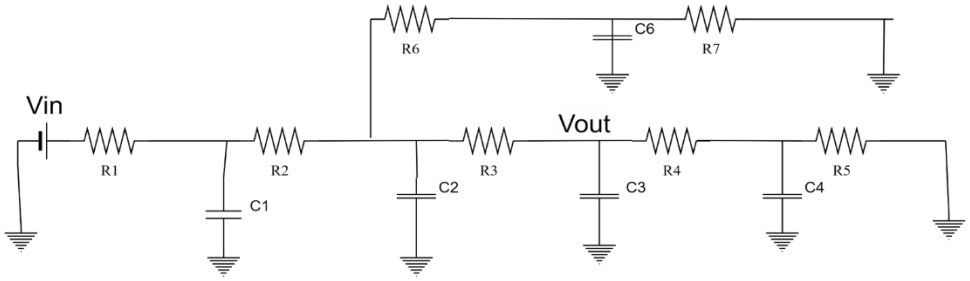
Delay

Q1.

Part1: The **Texas Instrument** company's analog engineers are designing a **CMOS 3- input NAND gate** considering delay and power consumption. They have chosen GaN semiconductor which has $\mu_n = 3\mu_p$.

They have **fixed** the width scaling factor $k_n = 2$ for **NMOS** transistors and want to meet **equal fall and rise resistance**. Later, they are informed that the **NAND gate** will drive a total load of **three NOT** gates and **two OR** gates.

Part 2: There is a **RC tree** network given below.



(a)	**Find** the **width** scaling factor for **PMOS (k_p)** to meet the rise and fall resistance specification.	[2]
(b)	**Draw** the **RC** equivalent circuit of the **NAND gate** considering the loads are not connected. **Use** the **Elmore delay** model to find the expressions for t_{cdr}, t_{pdr}, t_{cdf}, and t_{pdf}.	[7]
(c)	If each **NOT gate** and **OR gate** load contributes $3C$, $5C$ unit capacitance respectively, then after connecting the load estimate how many times slower the **NAND gate** output will operate compared to **load disconnected** condition considering **propagation delay rising** for both cases.	[3]
(d)	**In Part2**, if the R_1, R_2, R_3, R_4 and R_6 path is **on** then estimate the **worst case** rising delay using **Elmore delay** model associated with V_{in} to be propagated to V_{out}.	[3]