Department of Computer Science and Engineering (CSE)
BRAC University

Summer 2023
CSE460: VLSI Design

CMOS Delay

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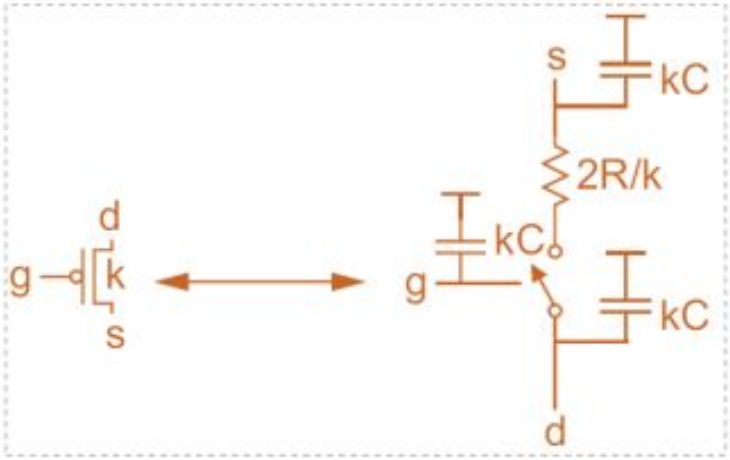
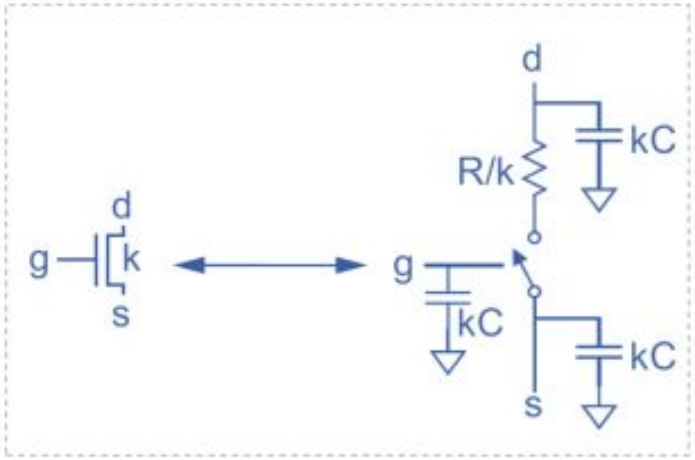
Lecturer

RC Delay Model





R unit resistance

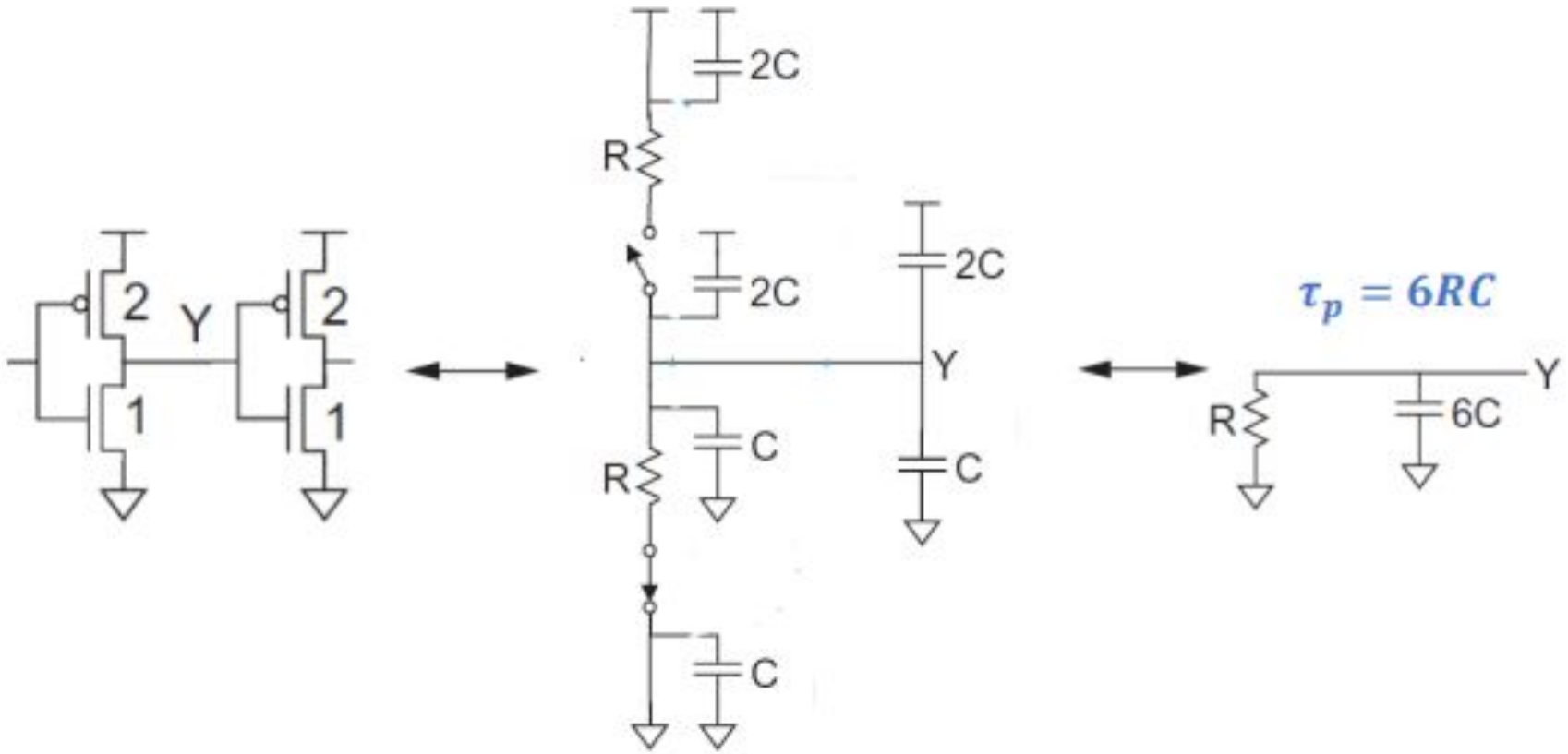
$$R = R_n$$

C unit capacitance

$$C = C_g = C_d$$

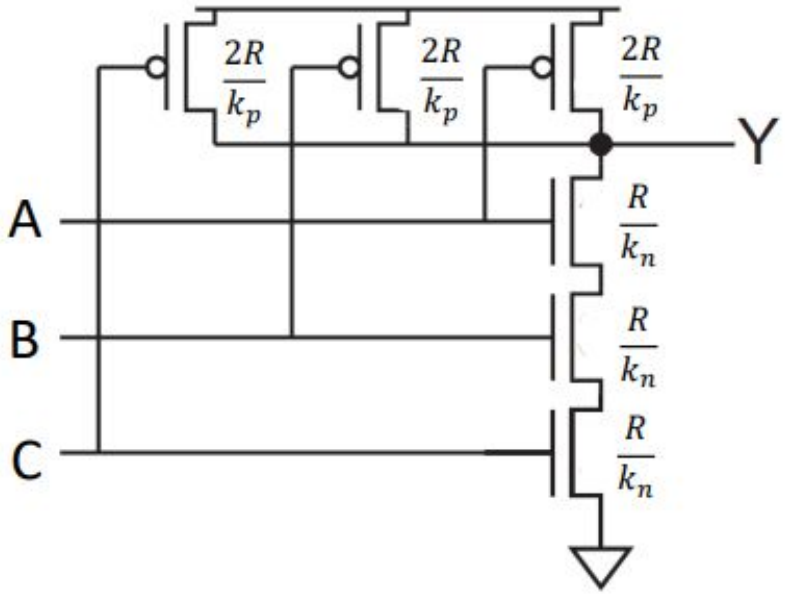
minimum sized nmos

Inverter Delay with 1 Inverter Load



3 Input NAND Gate

Choose transistor widths to achieve effective rise and fall resistance equal to that of a unit inverter (R).
consider, $\mu_n = 2\mu_p$



1. Find the fall/rise circuits

- Truth Table of NAND Gate

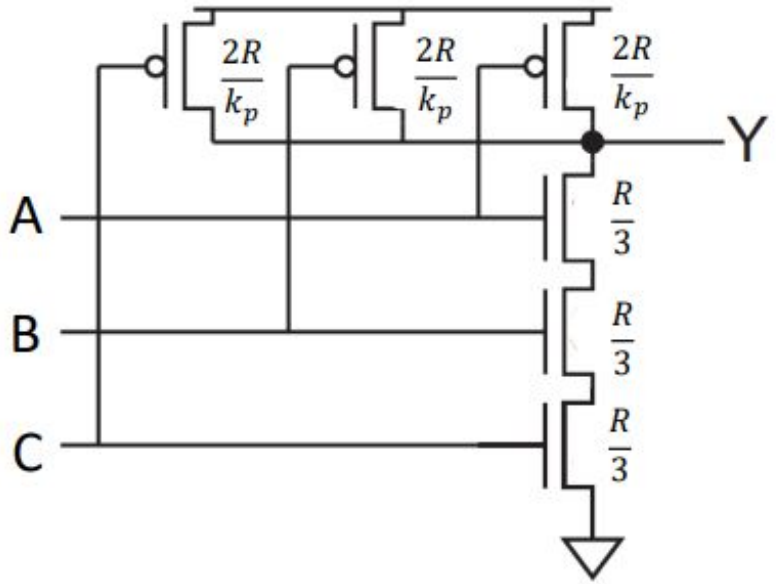
Input			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Discharges when all three NMOS are ON and PMOS off

$$\frac{3R}{\kappa_n} = R \quad \rightarrow \kappa_n = 3$$

3 Input NAND Gate

Choose transistor widths to achieve effective rise and fall resistance equal to that of a unit inverter (R).
consider, $\mu_n = 2\mu_p$



1. Find the fall/rise circuits

- Truth Table of NAND Gate

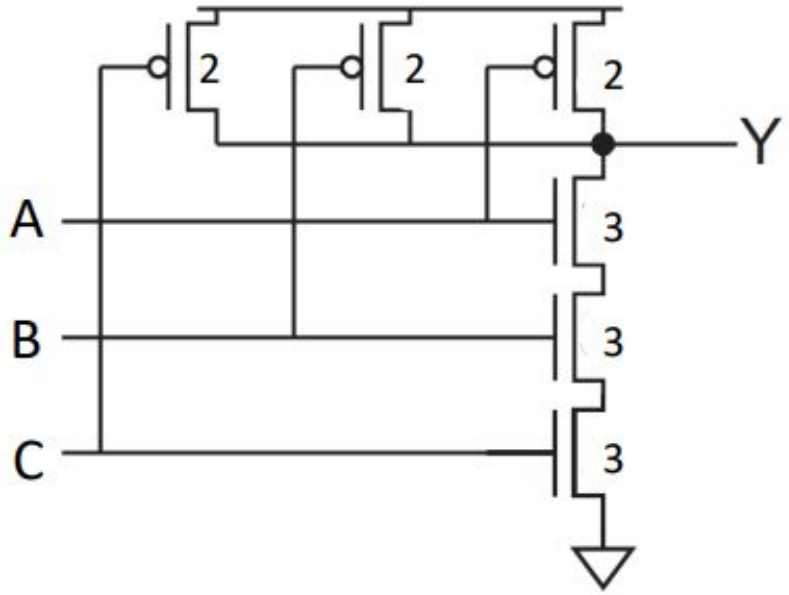
Input			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

charges back up when any of the input goes to zero
(1 PMOS on – 1 NMOS OFF)

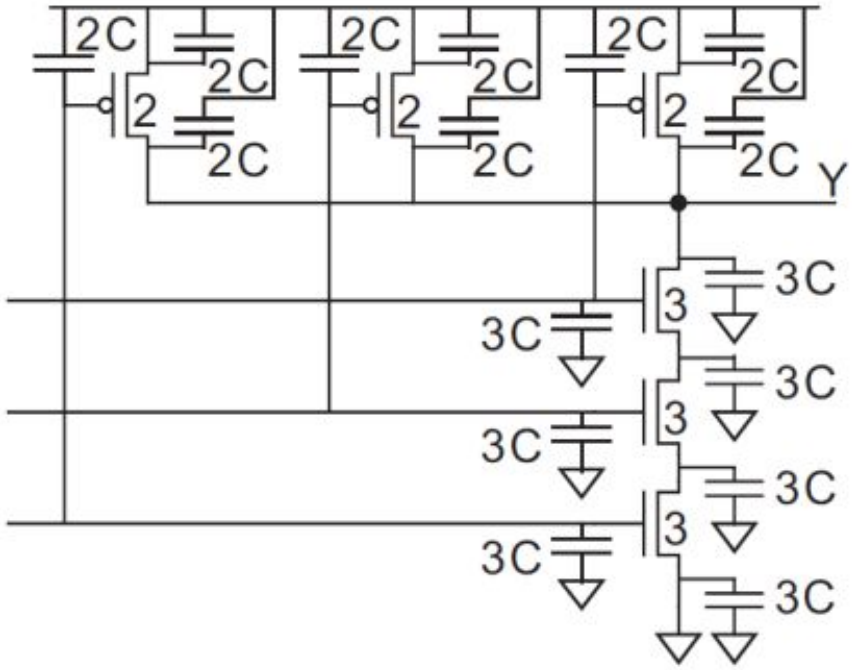
$$\frac{2R}{\kappa_p} = R \quad \rightarrow \kappa_p = 2$$

3 Input NAND Gate

Choose transistor widths to achieve effective rise and fall resistance equal to that of a unit inverter (R).
consider, $\mu_n = 2\mu_p$

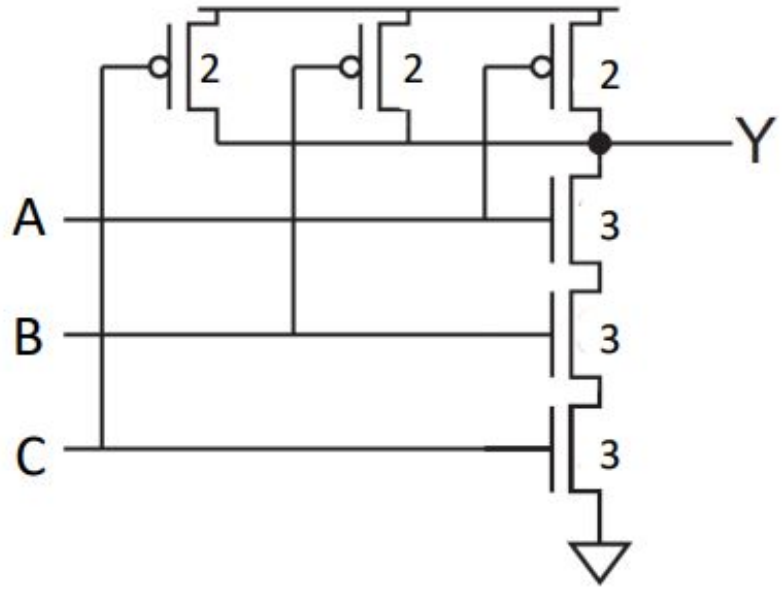


What is the effective Capacitance at input A,B,C and output Y?



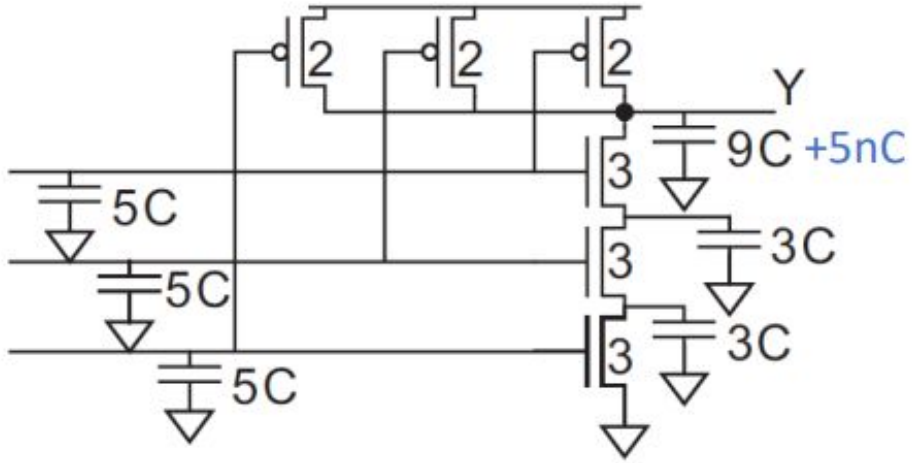
3 Input NAND Gate

Choose transistor widths to achieve effective rise and fall resistance equal to that of a unit inverter (R).
consider, $\mu_n = 2\mu_p$

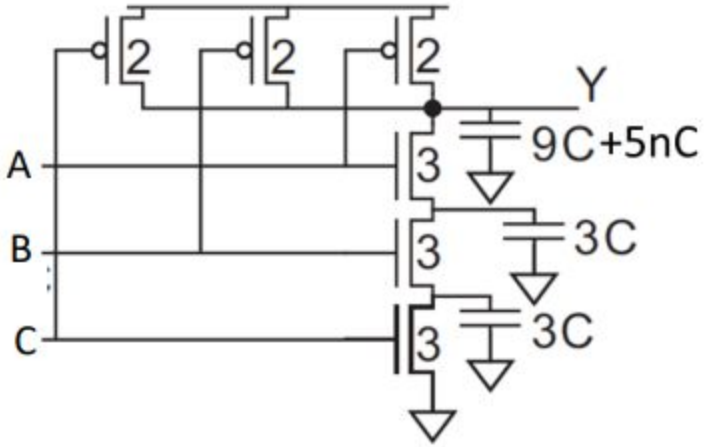


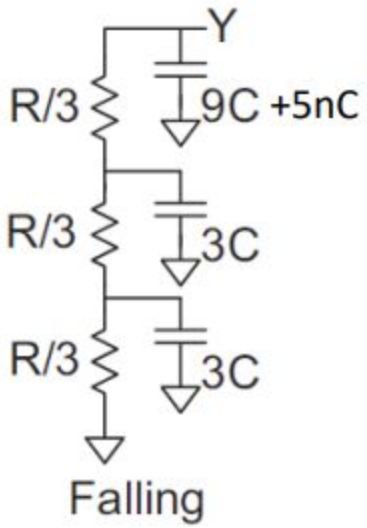
What is the effective Capacitance at input A,B,C and output Y?

3-NAND with connected to another n 3-NAND



Falling and Rising Equivalent Circuit





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A	B	C	Y
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0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
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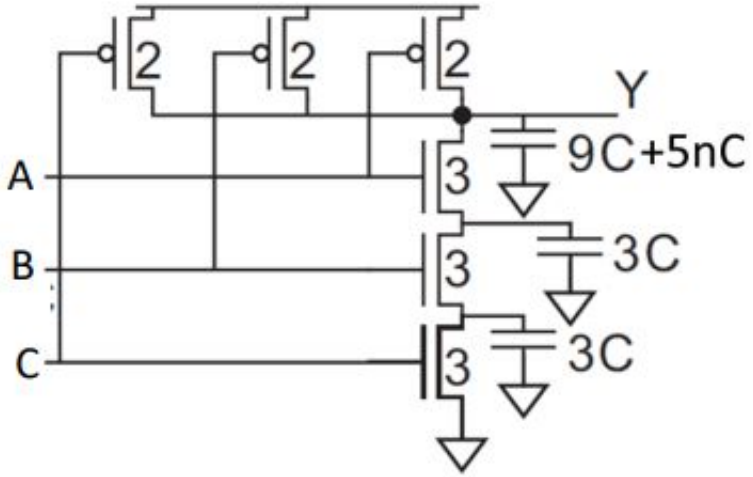
Falling and Rising Equivalent Circuit



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A	B	C	Y
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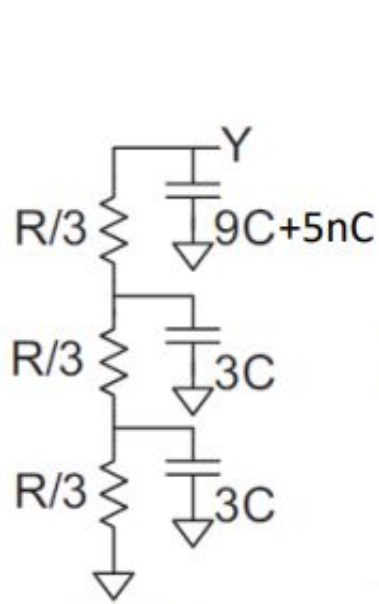
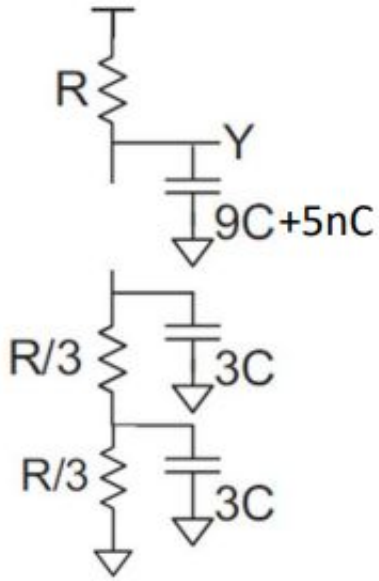
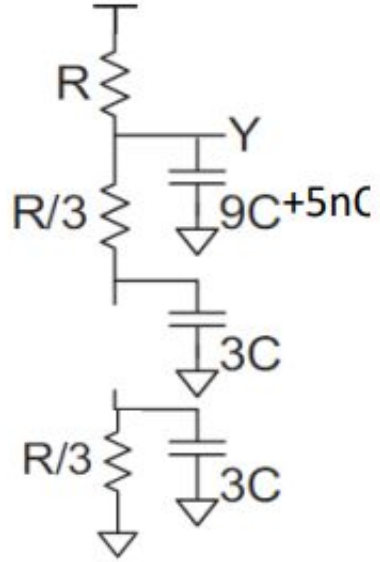


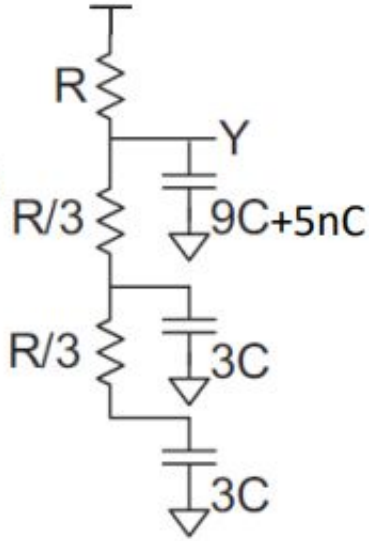
Falling



Rising

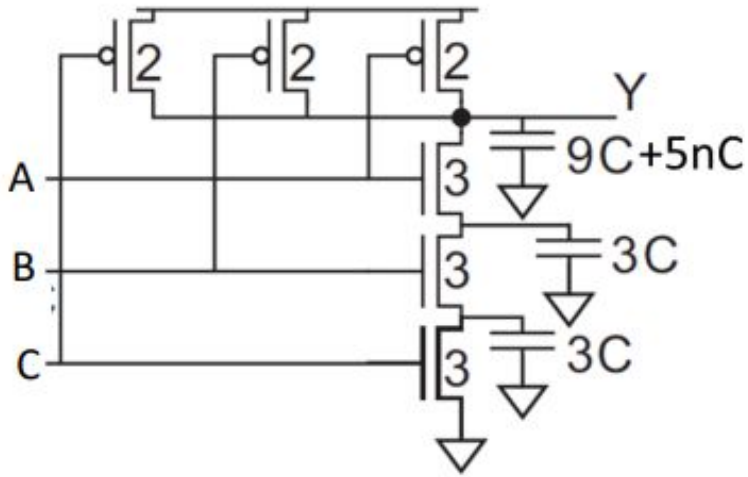


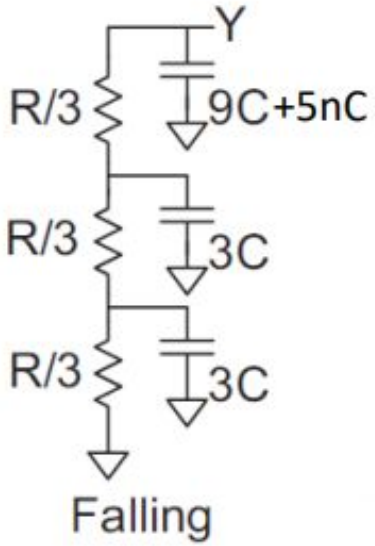
Rising

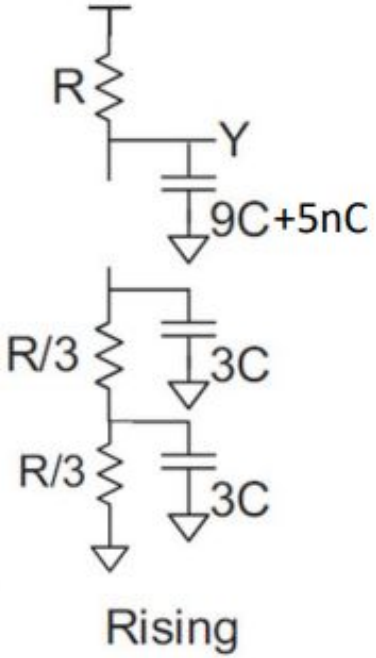


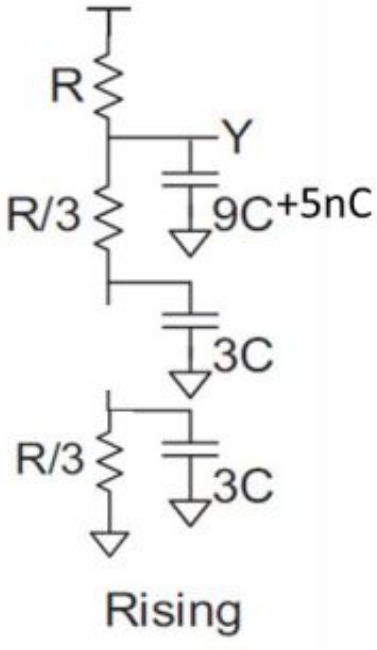
Rising

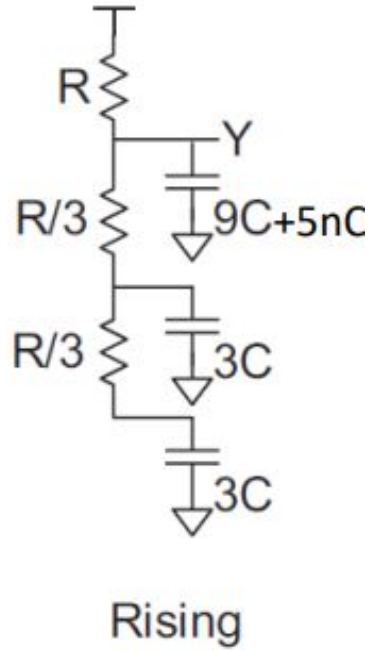
Calculating τ











$$\tau_{PHL} =$$

$$\tau_{PLH1} = R(9 + 5n)C$$

$$\tau_{PLH2} = R(12 + 5n)C$$

$$\tau_{PLH3} = R(15 + 5n)C$$

Elmore Delay

Elmore Delay

- Any digital circuit can be modeled as an RC circuit or an RC 'tree'
- Elmore Delay can approximated the delay of such trees

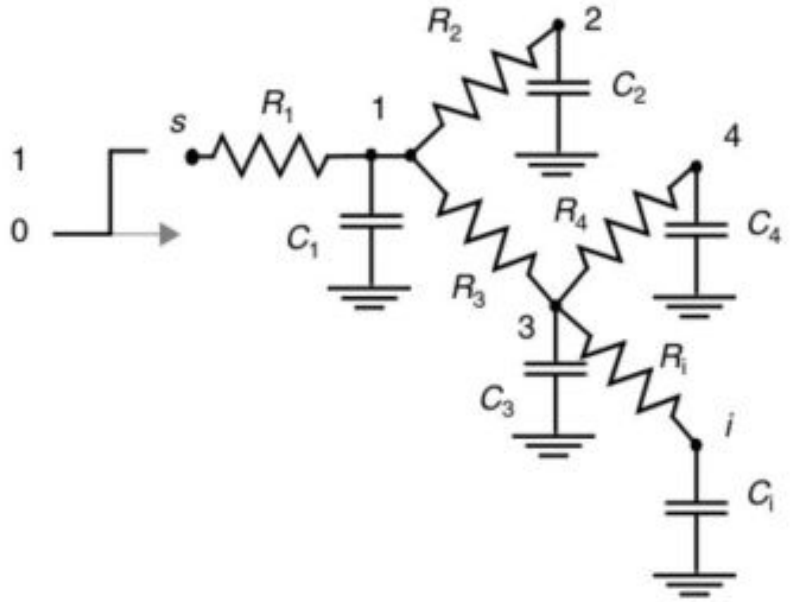
$$\tau_p = \sum_i R_{ik} C_i = \sum_{i=1}^{n} C_i \sum_{j=1}^{i} R_j$$ → sum of shared resistor to path

$$R_{ik} = \sum R_j \rightarrow R \in (paths\ source \rightarrow o/p) \cap (paths\ source \rightarrow k)$$

$n \rightarrow$ no of nodes

$C_i \rightarrow$ capacitor in RC network

$R_{ik} \rightarrow$ shared resistor to o/p on a path to C_i



Elmore Delay

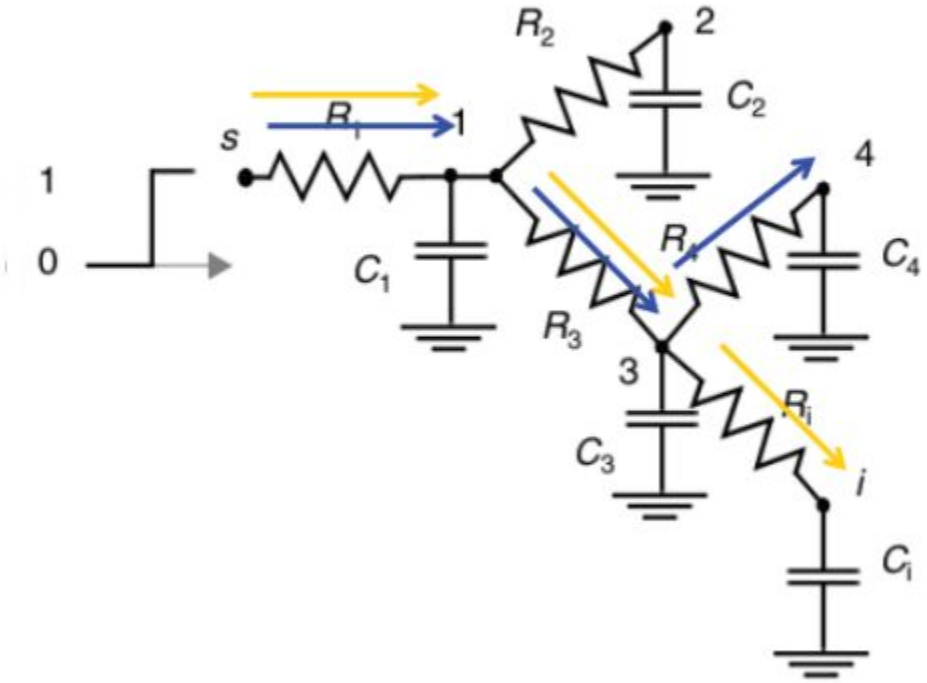
$$\tau_p = \sum_i R_{ik} C_i = \sum_{i=1}^{n} C_i \sum_{j=1}^{i} R_j$$

$$R_{ik} = \sum R_j \rightarrow R \in [(path\ source \rightarrow o/p) \cap (paths\ source \rightarrow k)]$$

$(path\ source \rightarrow o/p)$

$(path\ source \rightarrow k = 4)$

$$R_{i4} = R_1 + R_3$$



Elmore Delay

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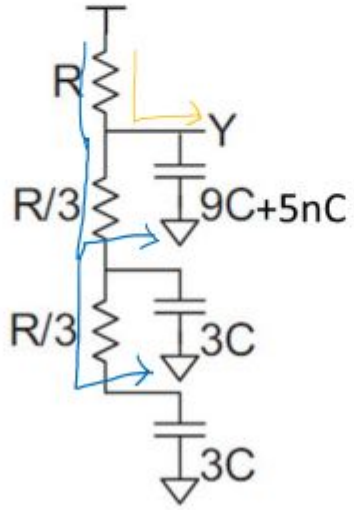
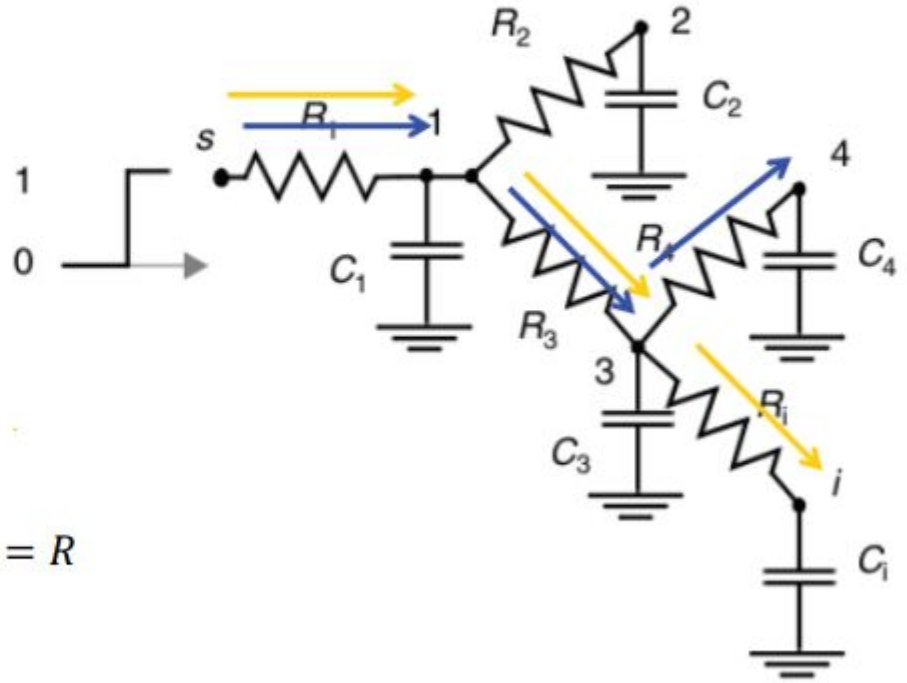


Rising



$R_{ik} = R$

Elmore Delay

$$\tau_p = \sum_i R_{ik} C_i = \sum_{i=1}^{n} C_i \sum_{j=1}^{i} R_j$$

$$R_{ik} = \sum R_j \rightarrow R \in [(path\ source \rightarrow o/p) \cap (paths\ source \rightarrow k)]$$

$$\tau_{Di} = (R_1 + R_3 + R_i) C_i$$

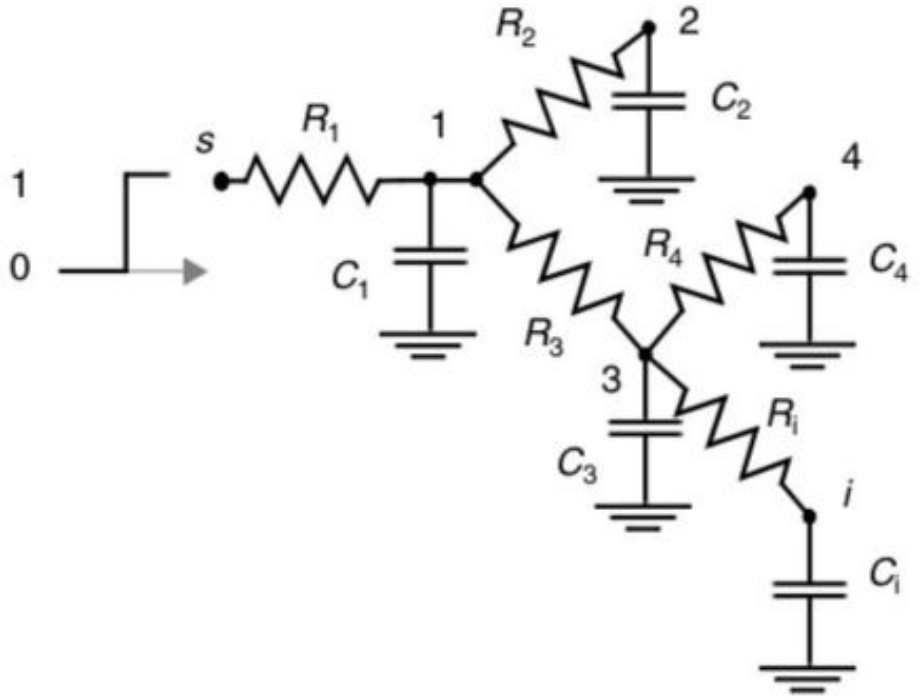
$$\tau_{D1} = R_1 C_1$$

$$\tau_{D2} = R_1 C_2$$

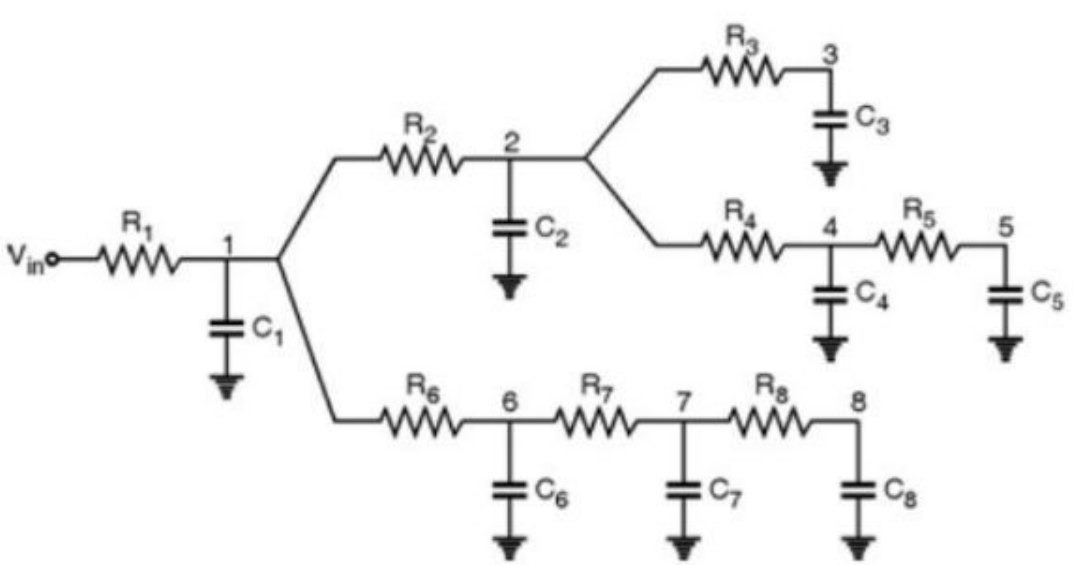
$$\tau_{D3} = (R_1 + R_3) C_3$$

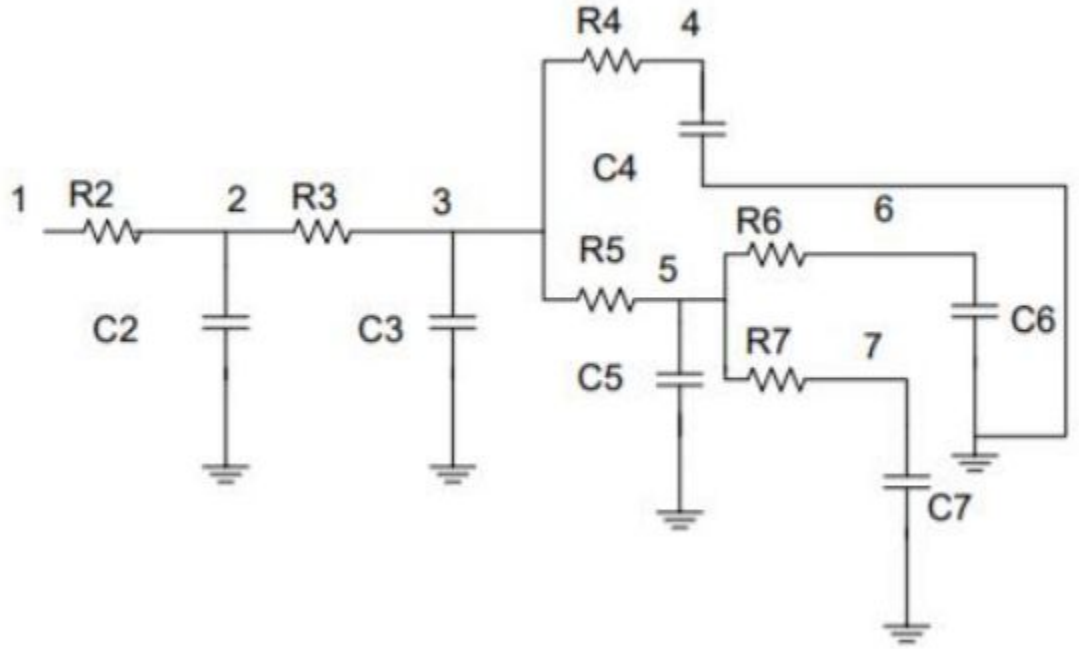
$$\tau_{D4} = (R_1 + R_3) C_4$$

$$\tau_p = \sum \tau_{Dk}$$



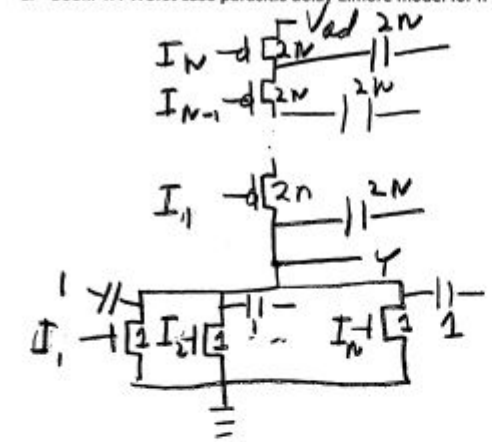
Elmore Delay: Practice





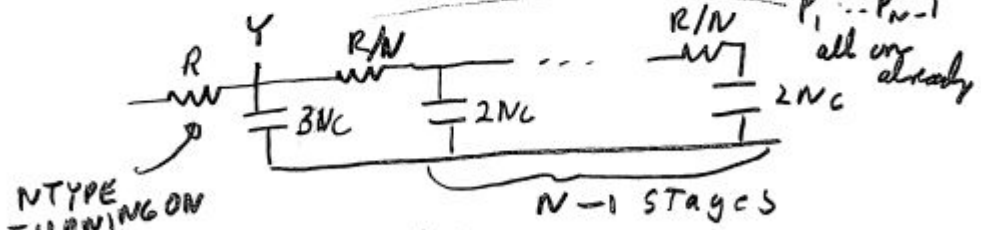
n Input NOR Gate

1. Book: 4.4 Worst case parasitic delay Elmore model for n-input NOR gate



Total of 2N+N.1C on Y = 3N

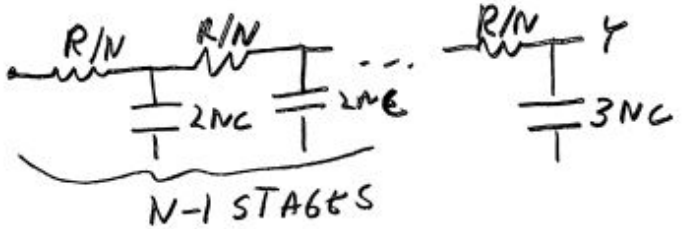
Worst case Fall Time: I_1-I_N all at 0
I_N goes from 0 to 1



Elmore model delay

$$R*\left(\sum_{i=1}^{N-1} 2NC + 3NC\right) = R(2N^2C + NC) = (2N^2+N)RC$$

Worst Case Rise Time
I_1-I_{n-1} at 0
I_N goes from 1 To 0



$$\frac{R}{N}2NC + \frac{2R}{N}2NC + \ldots \frac{(N-1)R}{N}2NC + R3NC$$

$$= RC(1 + \ldots N-1) + 3NRC$$

$$= RC\left(\frac{(N-1)N}{2}\right) + 3NRC$$

$$= RC(N^2-N) + 3NRC$$

$$= RC(N^2+2N)$$

Fall Time is worst