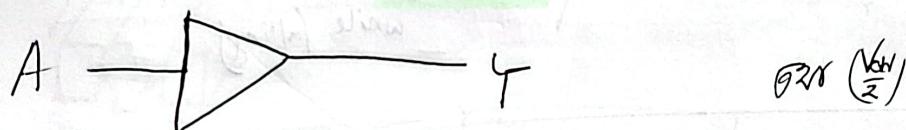


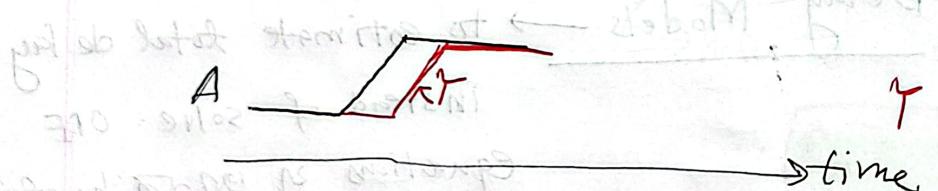
→ but by definition, 20% to 80% $\sqrt{10}$ time = t_p

(अमर्ति) 80/- to 20/- " " → df

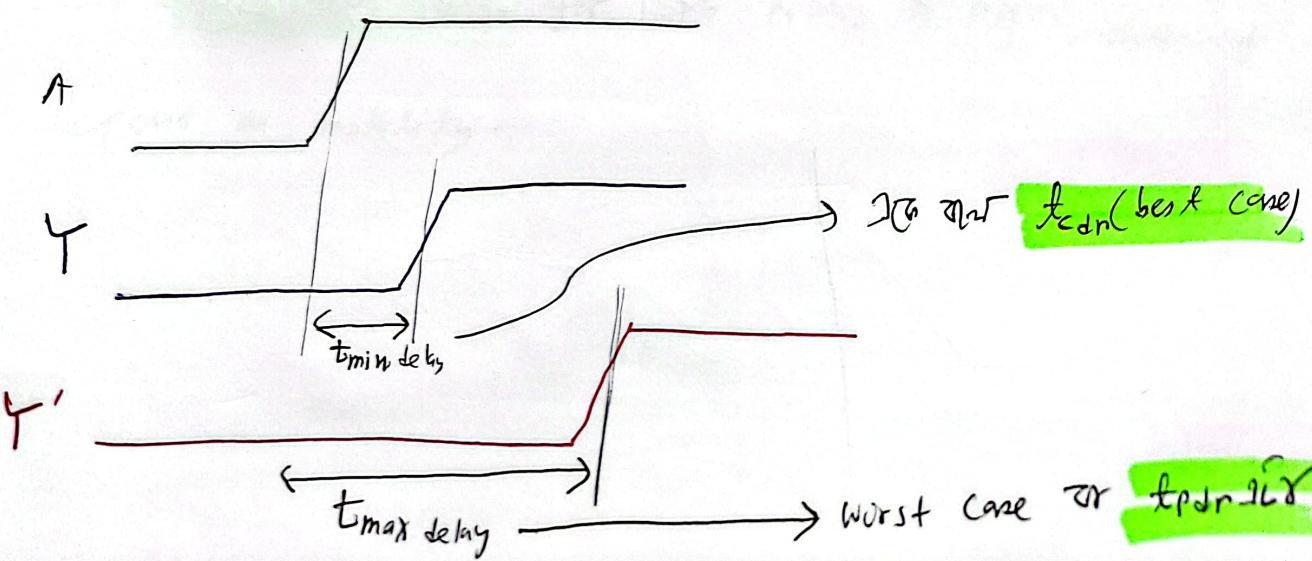
$\rightarrow t_r, t_f$ may be different.



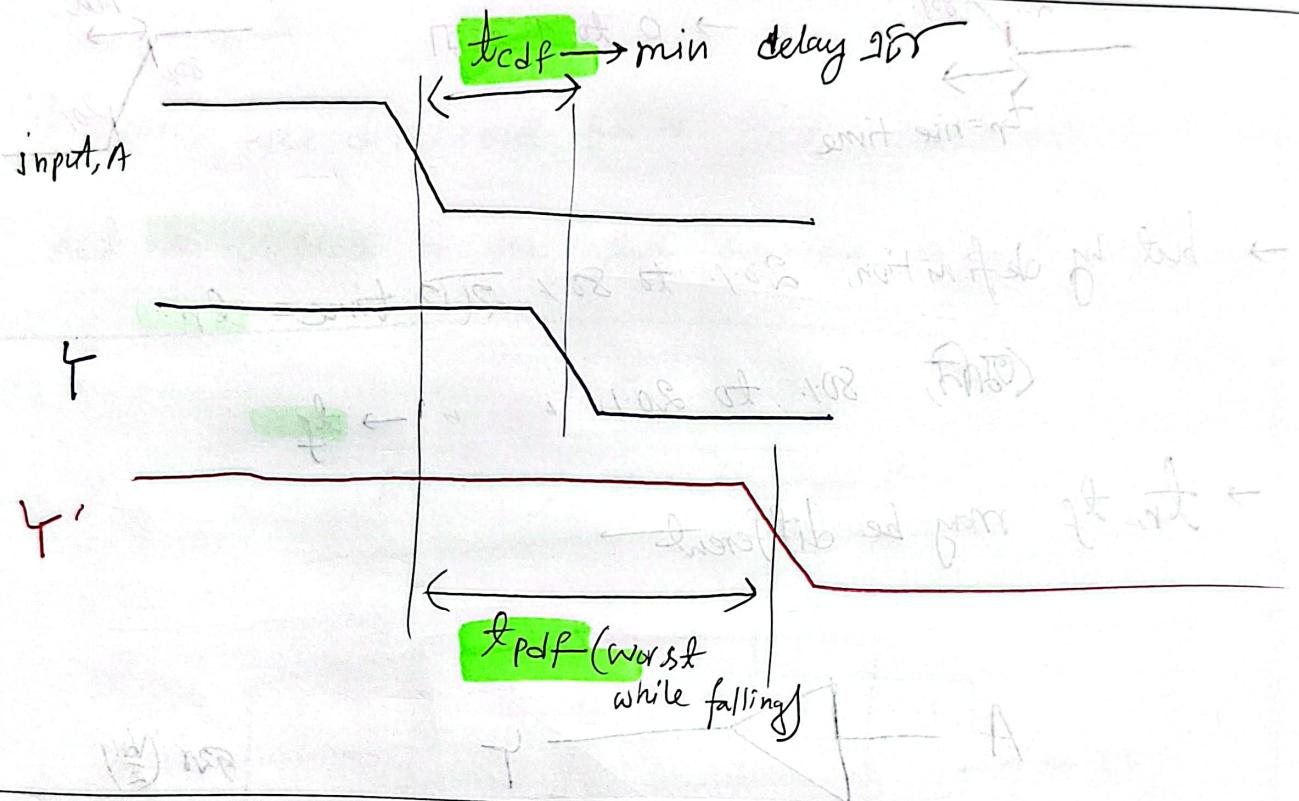
buffen



Output rising delay τ_{R}



We will focus on t_{pd} while designing ckts.



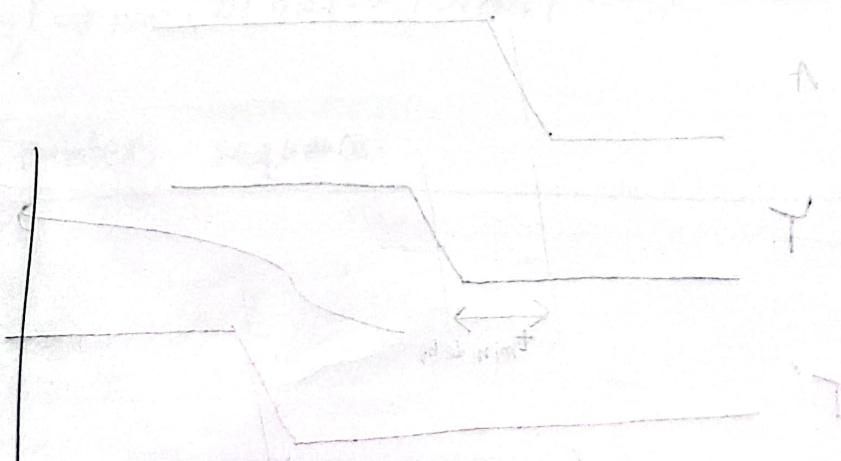
Delay Models → to estimate total delay

Instead of solve ODE
Equations are easier

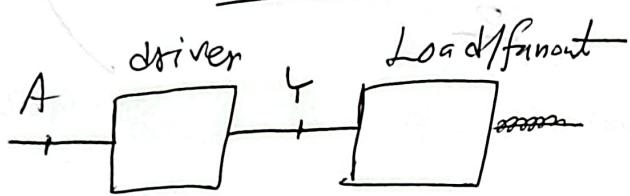
→ RC model

→ Elmore Model

fixed load, fixed time of

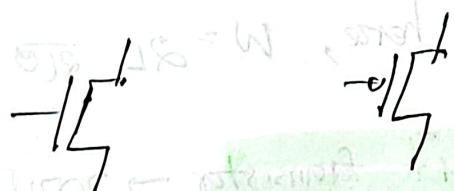
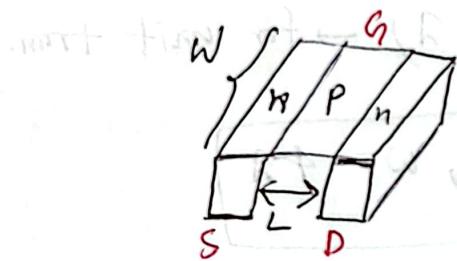


RC Model:



driver go input, A \rightarrow L, or op to signal (no faced)

$$\text{delay} = (\text{eff. resistance} \times \text{eff. capacitance})$$



$$M_n \approx 2 M_p \quad \text{normally}$$

hence, mobility ratio is constant

$$R_n = \left(\frac{R_p}{2} \right)$$

$$R = \frac{1}{M_n C_{ox} \left(\frac{W}{L} \right)}$$

but, capacitance same for both NMOS & PMOS, doesn't depend on mobility.

$$\lambda = \frac{\text{feature size OR channel length for MOSFET}}{2} \quad \text{unit}$$

+ transistors

$$= \left(\frac{L}{2} \right)$$

$$\Rightarrow L = (2\lambda) \rightarrow D-S \text{ distance } \text{unit}$$

but, width w , कम/मात्रा/ज्ञान अनुसारी still, unit width unit
प्राचीन वर्गमूल अनुमान अनुमान

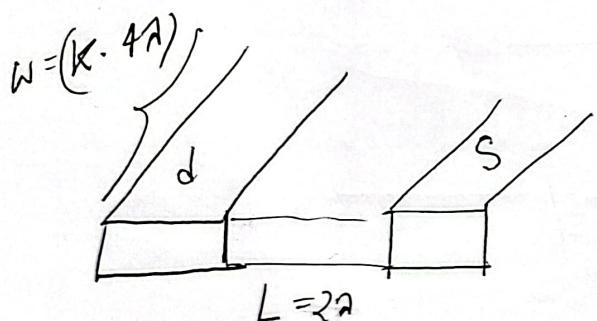
hence, $w = 2L$. $\sqrt{C_0 C_V} = (4\lambda) \rightarrow$ for unit tran.

unit transistor \rightarrow यदि $L = 2\lambda$, $w = 4\lambda$

⇒ aspect ratio, $\frac{w}{L} = \left(\frac{4\lambda}{2\lambda} \right)$

unit
let, nMOS resistance $\rightarrow R$, cap $\rightarrow C$

∴ unit pMOS " $\rightarrow (2R)\sqrt{C_0 C_V}$, cap- C_{pMOS}



I_{ds} flow \Rightarrow time \rightarrow if $w(\uparrow)$, $R(\downarrow)$ ~~assume~~ $\downarrow R = \rho \frac{L}{A(\uparrow)}$

$$A = w \cdot x$$

Reqd.: K width nMOS \Rightarrow resistance $= \left(\frac{R}{K} \right)$

" " pMOS " " $= \left(\frac{R}{K} \right) \cdot \text{area} \cdot \text{resistivity}$

but, as $C = \frac{A \cdot \epsilon}{d}$ ~~if~~ or area, $A(\uparrow)$, $C(\uparrow)$ hence

$C \propto$ width ie $C \propto K$

K width nMOS $\rightarrow KC$

" " pMOS $\rightarrow KC$

Summary.

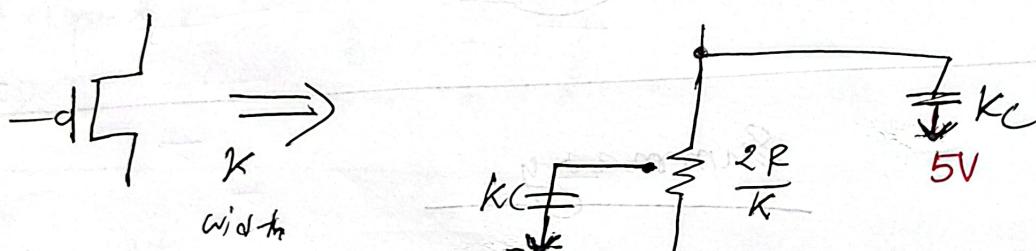
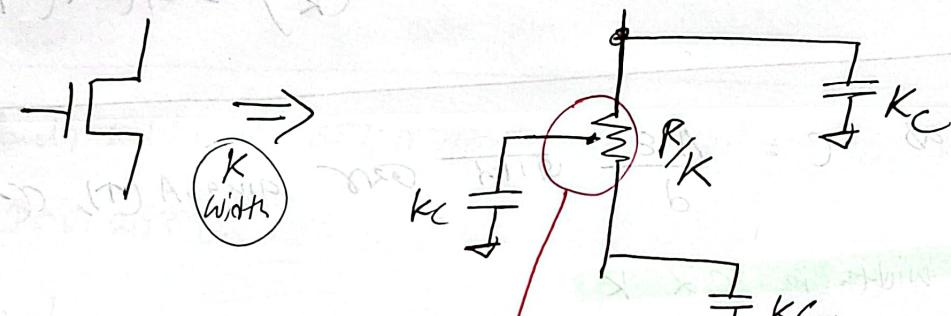
	nMOS	pMOS
unitsize	R, C	$2R, C$
$1 \rightarrow k$	$\frac{R}{k}, KC$	$\frac{2R}{k}, KC$

Time $=$ ~~time~~ \rightarrow unitsize

How R, C are organized in a transistor

→ Replace transistor with a resistor and 3 terminal \Rightarrow

$3\bar{C}$ capacitor add to gate

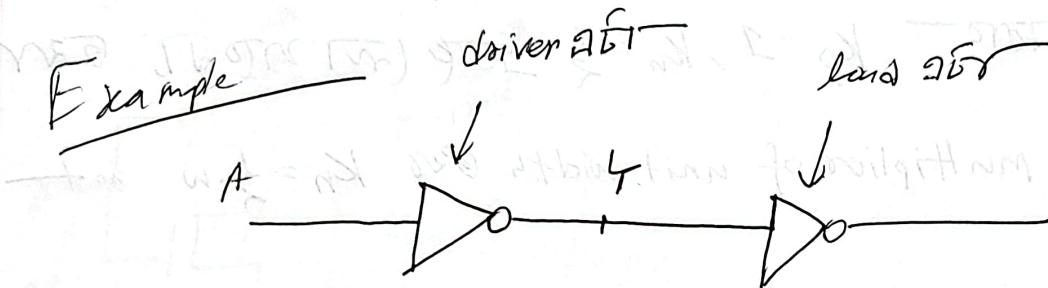


difference \rightarrow capacitor $\frac{1}{K} K_C$ $5V \Rightarrow$ $nMOS$

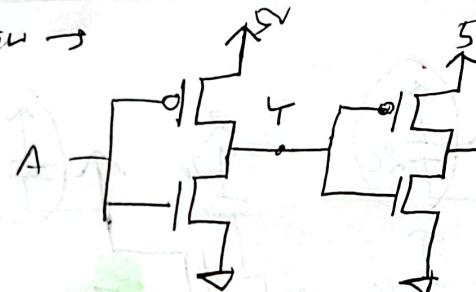
$nMOS \Rightarrow$ gnd fwd ,

Calculate the RC propagation delay for an unit inverter driving another unit inverter, each having equal fall and rise resistances (fanout-of-1 delay)

Example



\rightarrow CMOS draw \rightarrow



for equal fall, rise resistance as mentioned \Rightarrow

rise \rightarrow PUN \rightarrow hence PUN \Rightarrow resistance \propto $1/W$

fall \rightarrow PDN \rightarrow

PDN \Rightarrow

for an inverter $\rightarrow R_{\text{PUN}} = R_{\text{PDN}}$ \Rightarrow $R_{\text{PUN}} = R_{\text{PDN}}$ \Rightarrow $R_{\text{PUN}} = R_{\text{PDN}}$

if size of nMOS $\rightarrow K_n \cdot W$, pMOS $\rightarrow K_p \cdot W \Rightarrow$

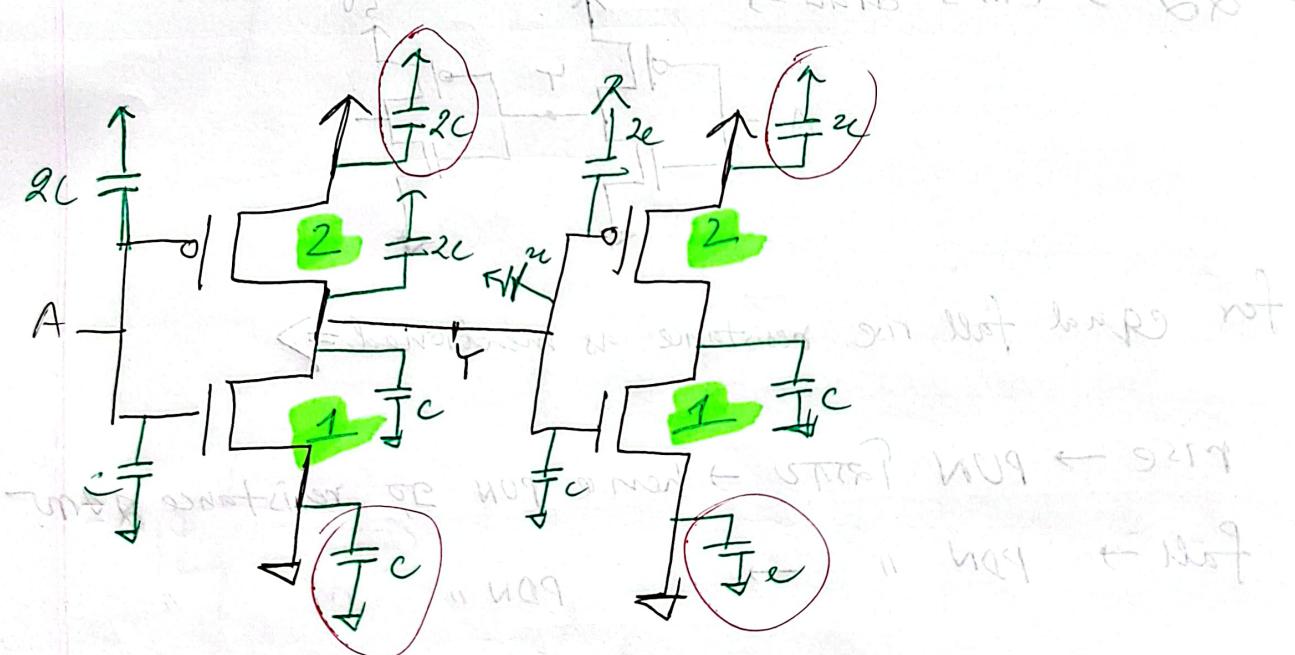
$$\text{hence, } R_{\text{PUN}} = R_{\text{PDN}}$$

$$\Rightarrow \left(\frac{R}{K_n} = \frac{2R}{K_p} \right)$$

$$\Rightarrow K_p = 2K_n$$

if $K_h = 1$, $K_p = 2$ \Rightarrow update now the size.

→ general answer $K_p = 1$, $K_h = \frac{1}{2}$ gate length must be \sqrt{w} or fraction multipliers of unit width \Rightarrow $K_h = \frac{1}{2} \cdot w$ not allowed.



∴ \forall capacitance \Rightarrow all terminals \Rightarrow voltage same -

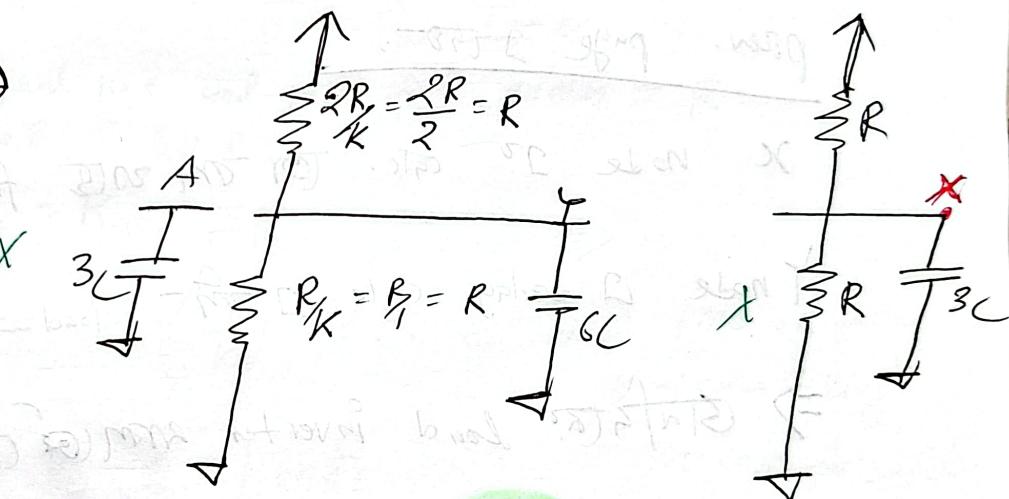
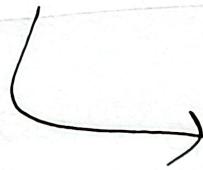
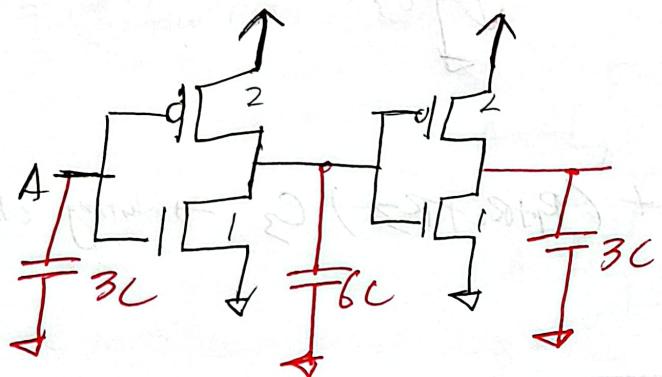
⇒ \forall nodes have same voltage so \Rightarrow total current flow is zero,

(Red mark \Rightarrow this is the point)

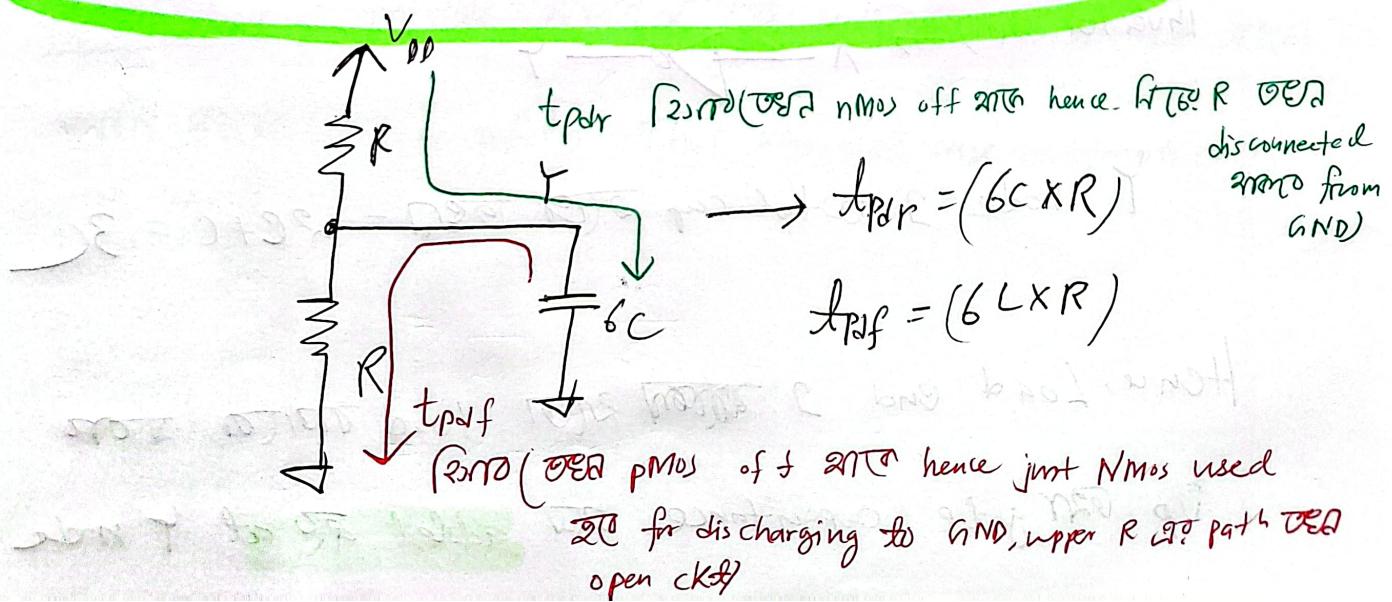
$$A \text{ node } \Rightarrow \text{total cap} = 2C + C = 3C$$

$$V_u + v + s = 2C + C + 2C + C = 6C$$

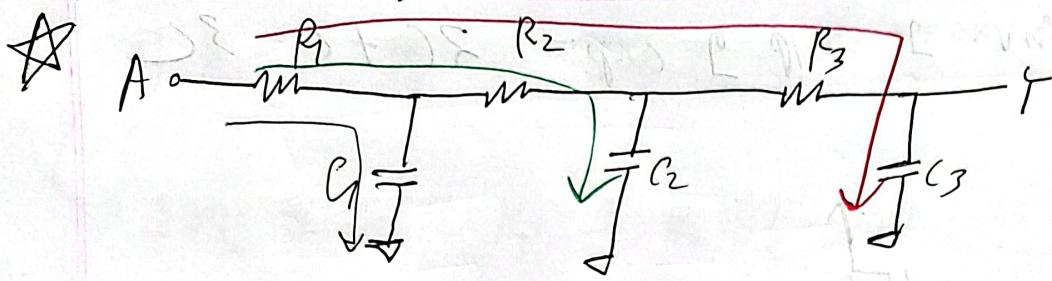
2nd inv. \Rightarrow $0IP \Rightarrow cap = 2C + C = 3C$



\leftarrow 2nd stage \Rightarrow connected by R_K to $3C$



Lec-17



$$t_d = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 \rightarrow \text{during charging}$$

prev. page 2 (50):

X node t_d calc. \rightarrow time from Y node or t_d \rightarrow X node

Y node \rightarrow delay calc. \rightarrow load \rightarrow total equivalent load?

\Rightarrow single load inverter equivalent to actual Y node

\therefore Cap = $6C$ means load inverter equivalent for a single

inverter only \rightarrow $A \rightarrow \text{Do} \rightarrow Y$

Y node \rightarrow total cap \rightarrow $2C + C = 3C$.

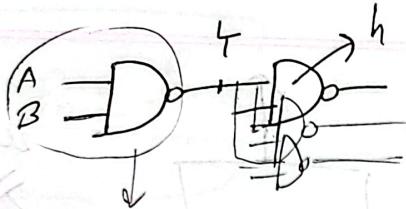
Hence, Load end \rightarrow total load inverter, stop

tip gate capacitance \rightarrow added to C at Y node

Sketch a NAND2 RC equivalent circuit with widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R)

Example:

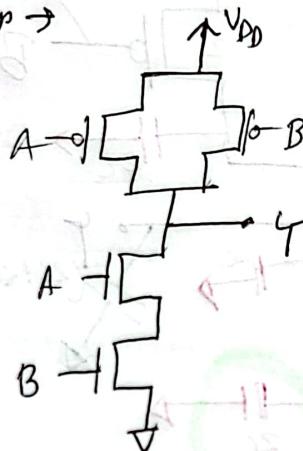
NAND2:



Sketch NAND gate to

drive twice 1st
NAND gate in

\Rightarrow (1) draw CMOS of driver \rightarrow



Here, in CMOS \rightarrow equal rise and fall ^{resistances} given $= R$

$\text{rise } R$ $\text{fall } R$ for

hence, $R_{\text{Pun}} = R_{\text{PON}} \equiv R$

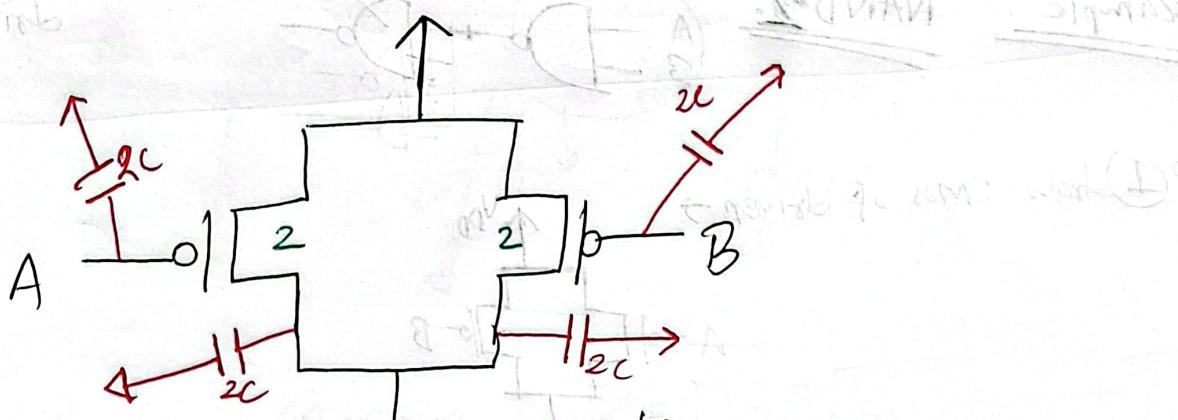
$$\Rightarrow \frac{2R}{K_p} = 2 \times \left(\frac{R}{K_n} \right) = R \quad [\text{only 1 PMOS on during rise} \rightarrow \text{taking worst case for safety}]$$

$$\therefore K_p = K_n = 2 \text{ m}^2/\text{V}$$

Thumb rule: parallel array of $1/2$ path of resistance \gg safety

पर्याप्त उत्तराधिकार for safety. That way, best case automatically

handled \Rightarrow यहाँ



$$\nabla \cdot (2c + 2c + 2c) = bc \text{ in } \bar{\Omega} \text{ on } \partial\Omega$$

$(2C + 2C) \times 3V$ (fito) but
diffusion opposite nodes are
contacted $2V_{DD}$ gets $2C$ fito
 nt came upper NMOS \rightarrow

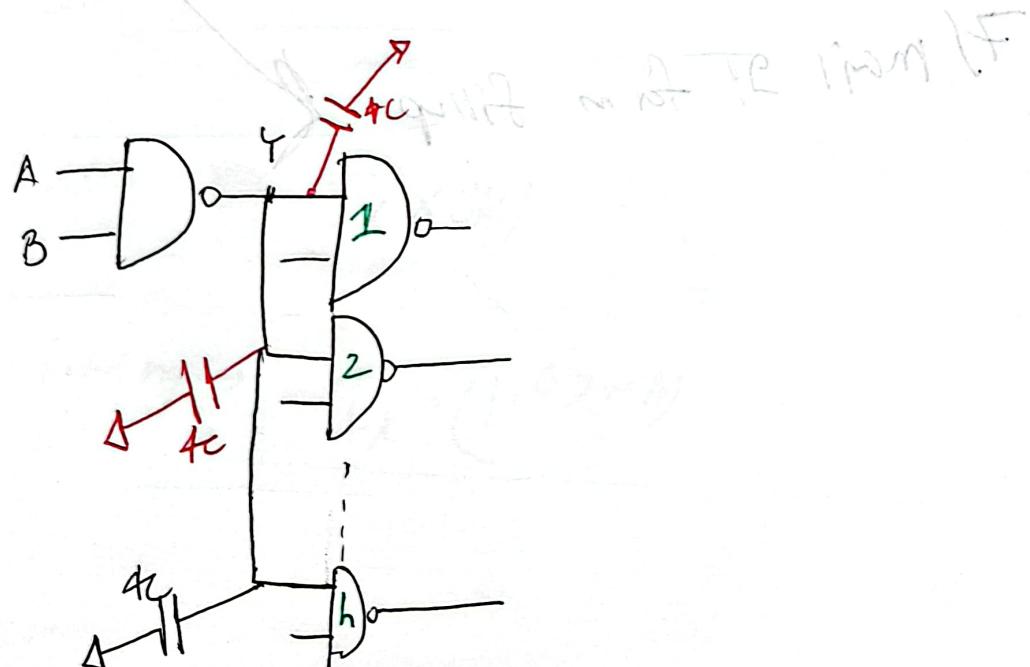
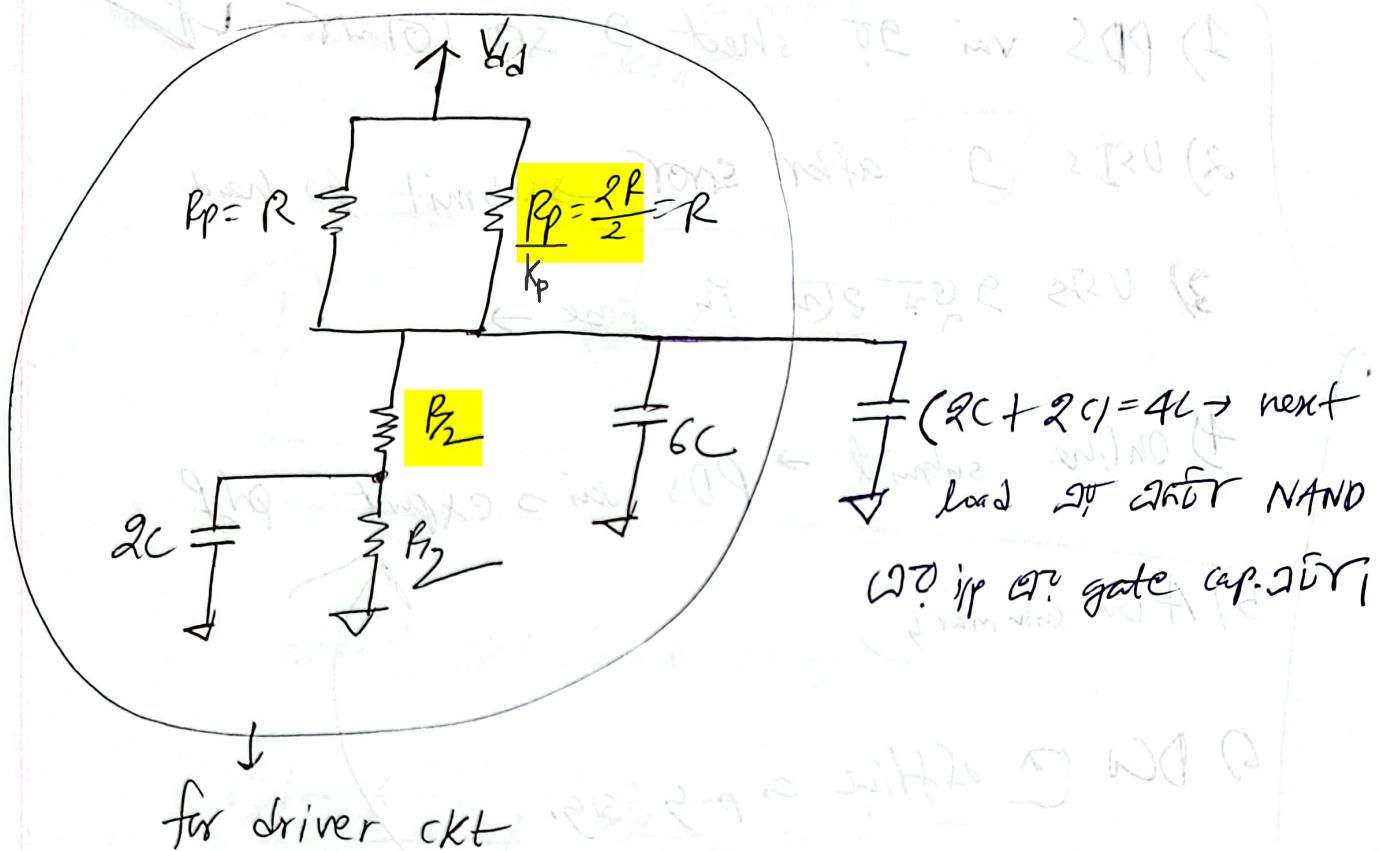
Source tie lower NMOS to drain
OTN not same here. Not contacted

$$\overline{TM}(25) \quad 2C + 2C = 4C \quad \text{从} \quad \overline{M}$$

Also FET. PMOS, NMOS एवं/3
एवं 'contacted' निर्माण करता
जैसे उत्तरी type MOS . 4C
निर्माण करता

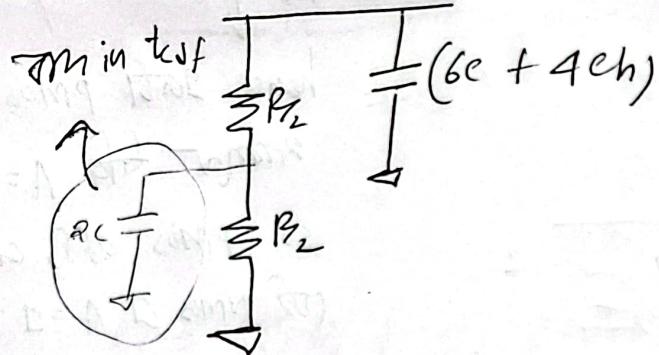
$$\frac{R_p}{K_p} = \frac{2R}{K_p} \quad \frac{R_n}{K_n} = \frac{R}{K_n}$$

Q1 for 1, $K_p = K_n = 2$ mS/ μA



hence, due to load $\rightarrow Y$ total cap = $(6C + 4Cxh)$

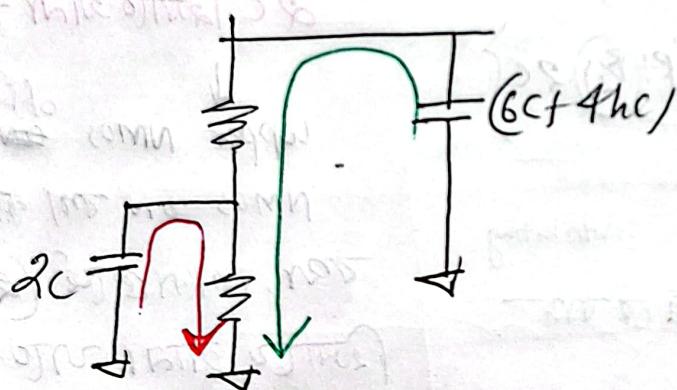
t_{CDf} Fwd \rightarrow parasitic cap, 2C to transistors, parasitic \rightarrow



$$\rightarrow t_{CDf} = (R_2 + R_2) \times (6C + 4Ch)$$

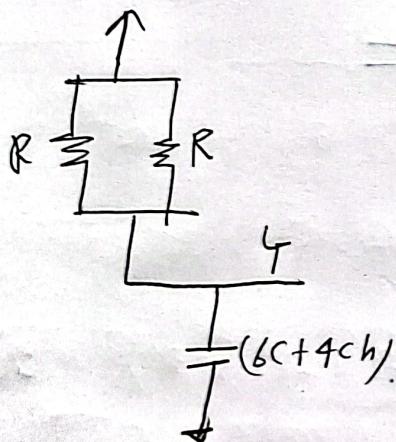
↓
best case

t_{PNF} \rightarrow worst case \rightarrow 9C parasitic cap Fwd \rightarrow Eq:



$$\rightarrow t_{PNF} = \{(6C + 4hc) \times (R_2 + R_2)\} + \{(2C) \times (R_2)\}$$

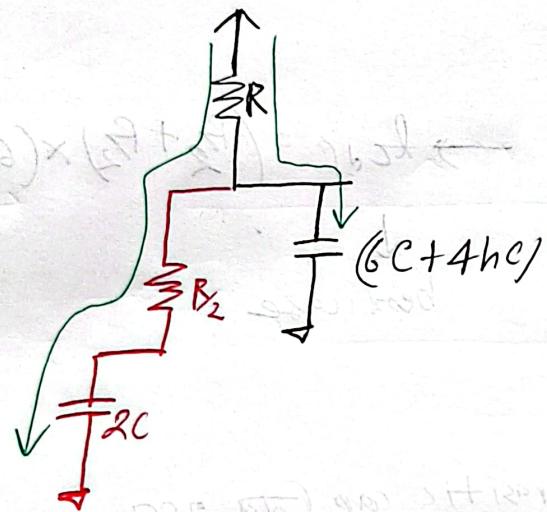
t_{CDr} \rightarrow best case \rightarrow 2 PMOS, ON trans:



$$\rightarrow t_{CDr} = \left(\frac{1}{R} + \frac{1}{R}\right)^{-1} \cdot (6C + 4Ch)$$

$$= \frac{R}{2} \times (6C + 4Ch)$$

$t_{pd,r} \rightarrow$ worst case rise \rightarrow at a time, only one PMOS



hence 90% PMOS off

$$2\pi f \tau \approx A = 0.1$$

so PMOS off, corresponding
10% NMOS $\Rightarrow A = 1$ \Rightarrow $t_{pd,r}$

ON राहि करना



worst case upper

NMOS ON करने पर parasitic
2C द्विगुणात्मक हैं

upper NMOS off ले lower

NMOS ON करने पर यह समी

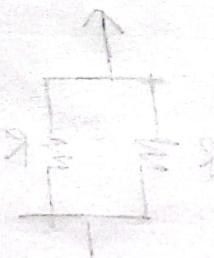
है, किन्तु (2C) के

प्रतिक्रिया द्वारा उत्पन्न दue to
disconnection.

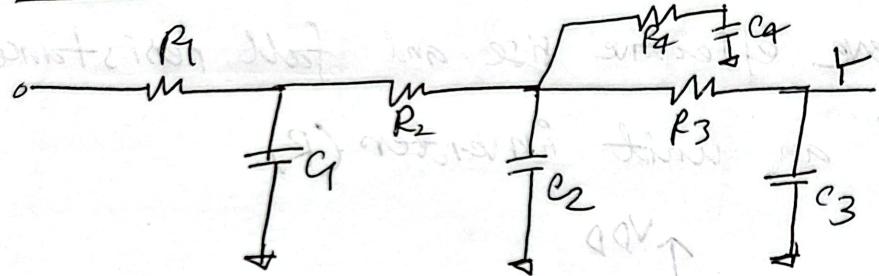
$$t_{pd,r} = \left\{ (6C + 4hc) \times R + (R + R_2) \cdot 2C \right\}$$

as this R_2 is not contributing
to Y node rise, it करने
में नहीं,

Delay राहि



a more generalized picture



$$T = G R_1 + C_2(R_1 + R_2) + C_3(R_1 + R_2 + R_3) + \dots$$

$C_4(R_1 + R_2 + R_3 + R_4)$ X

गढ़ रास्ते के नाम पर एक नोड के देले

कैलकुलेशन के नोड के R_4 का अनुपात

वितरण करें तो गढ़ रास्ते



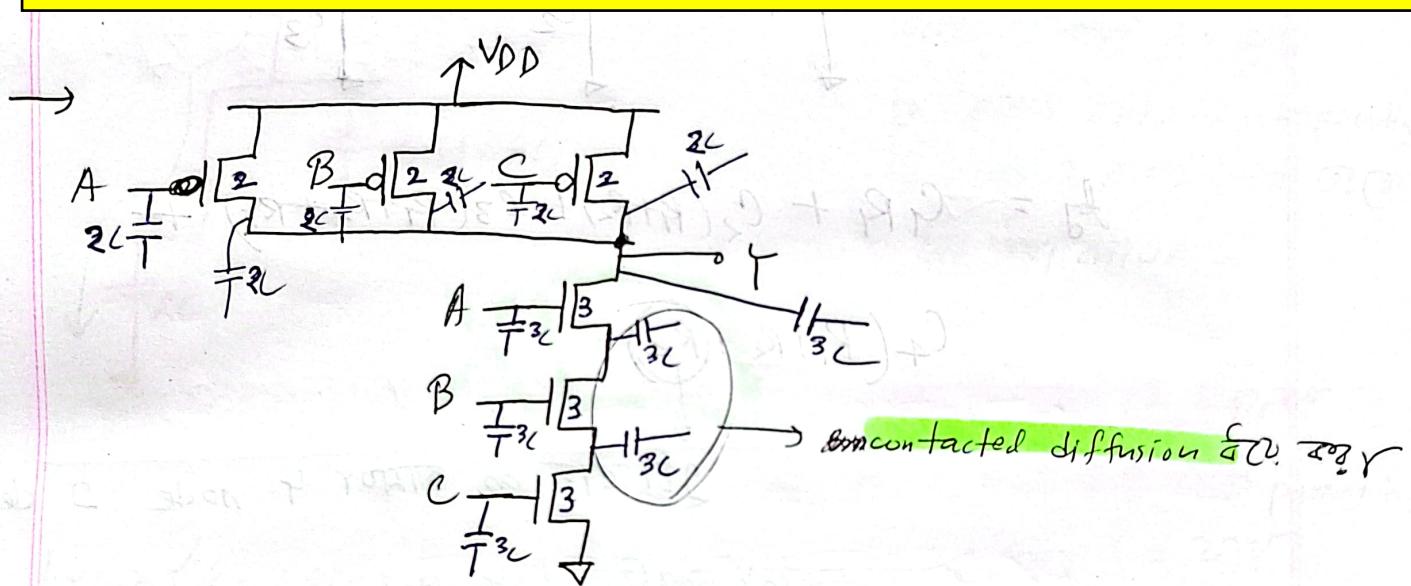
$$T = \left(\frac{R}{C} \right) \times S = \frac{R}{C} S$$

एक एक एलमोर डेले मॉडल के लिए

$$R = \left(\frac{C}{S} \right)^{-1} = \frac{1}{S C}$$

इसे एक एलमोर डेले मॉडल के लिए

Sketch a NAND3 RC equivalent circuit with widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R)



Fall resistance → PDN द्वारा

$$R_{PDN} = 3 \times \left(\frac{R}{K_h} \right) \equiv R$$

$$\Rightarrow K_n = 3$$

Rise Resistance \rightarrow PUN try

only 1 pmos on in worst case \rightarrow

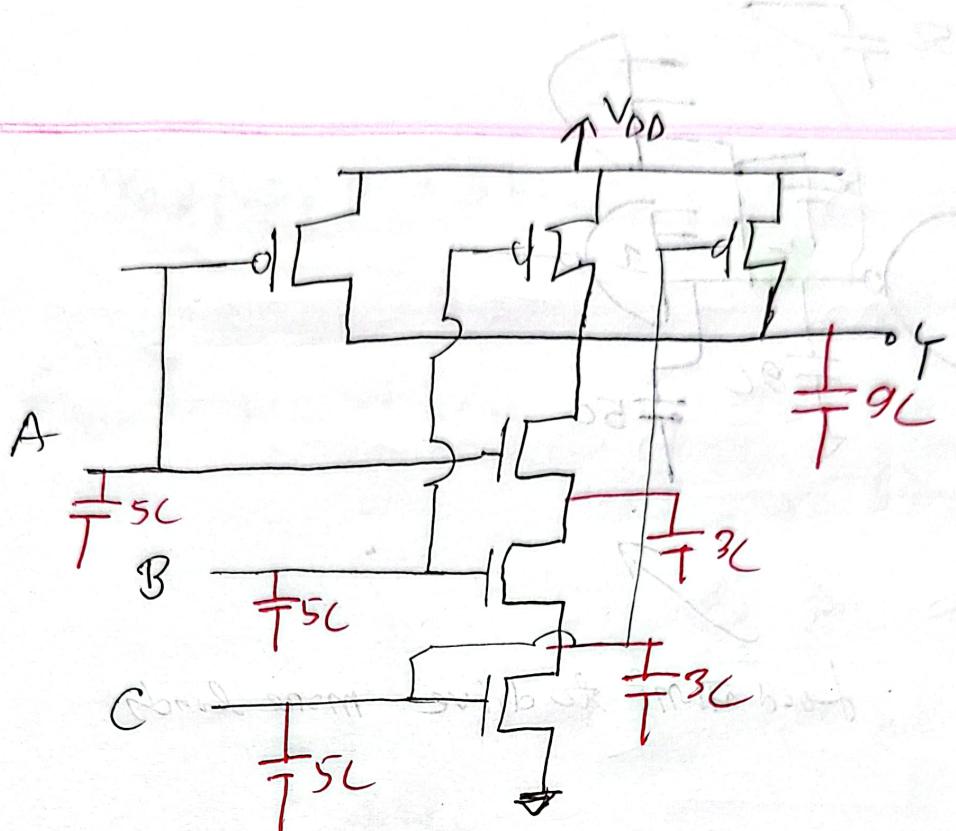
$$R_{PUN} = \left(\frac{2R}{K_p} \right) \equiv R$$

$$\Rightarrow K_P = 2$$

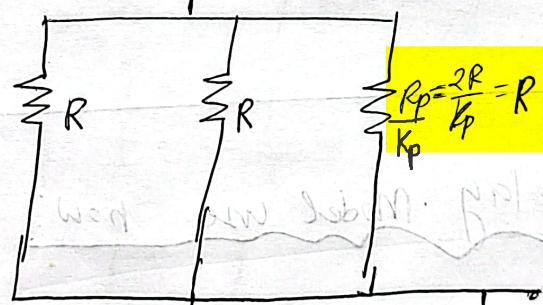
see here, A node $\square \rightarrow (2c + 3g) = 5c$ m²

$$B, C \text{ (OB same)} = 5 \text{ cm}^2$$

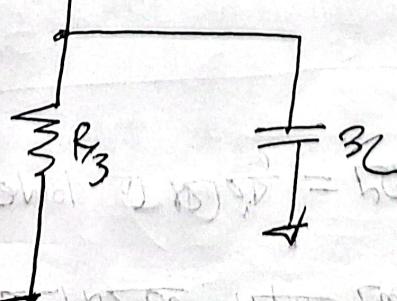
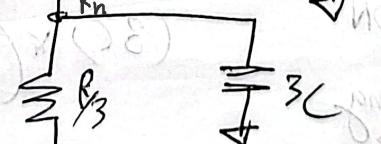
$$\text{node } \omega \rightarrow (2C + 2C + 2C + 3C) = 9C$$



$(\omega_c + d \times \beta_c) \rightarrow V_{DD}$

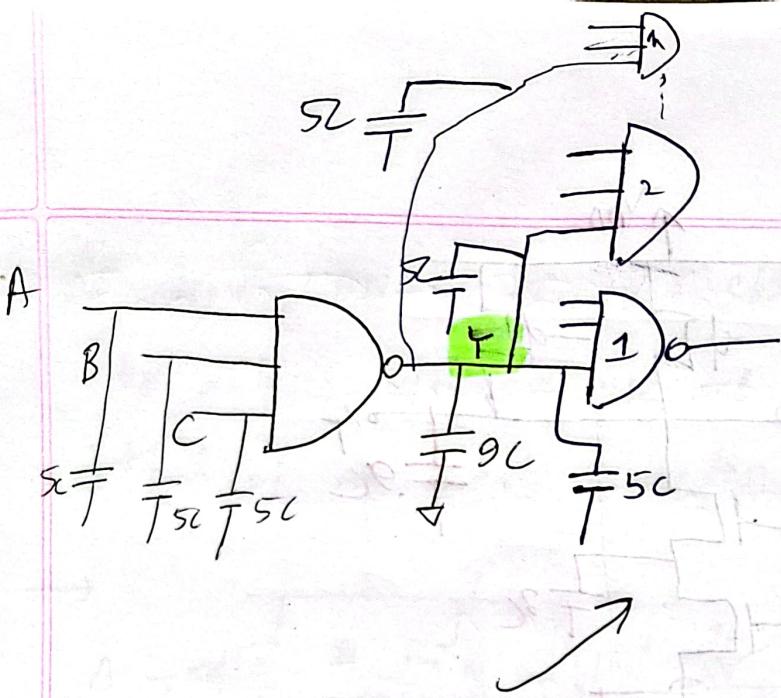


$$\frac{R_h}{K_n} = \frac{R_h}{K_n} = R_B$$



Diffusion resistance is the sum of the two resistances

$\rightarrow R_{BS} = R_h + R_B = R_h + R_h / K_n$



Load time to drive more loads

h SWING NAND gate drive time \rightarrow

$$T \text{ node } \cap \text{ total capacitance} = (5C \times h + 9C)$$

Elmore Delay Model use now:

$$t_{pdf} = \text{worst case} \rightarrow \sqrt{[(9C + 5Ch) \times (3 \times R_3) + (3C) \times (R_3 + R_3) + (3C) \times (R_3)]} = 5hRC + 12RC$$

3 NMOS - ON
for discharging

and corresponding pMOS- all are off hence

t_{cdf} = best case \rightarrow lower $(3C) \times (R_3)$ capacitor

already fall rate same as fall rate

$T \text{ fall time} (5Ch + 9C)$ fall rate

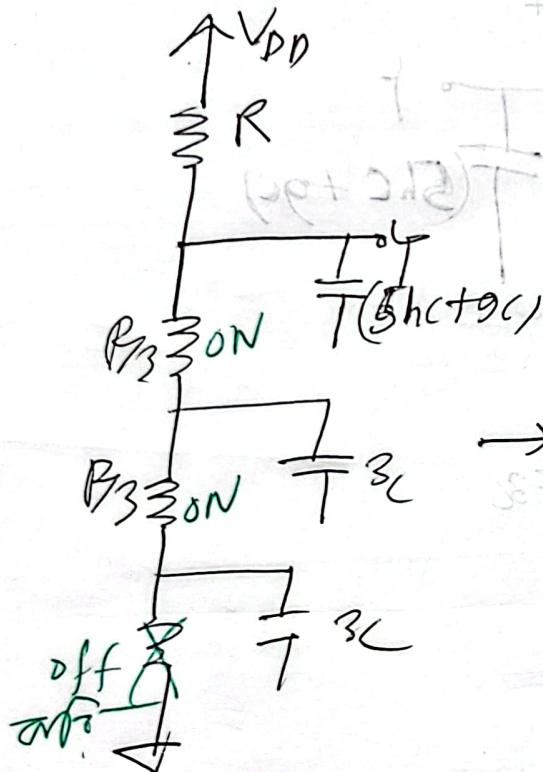
$$t_{CD} = (9C + 5hC) \times (3 \times R_3) = 9RC + 5hRC$$

t_{PDR} = worst case only 1 PMOS on for hence

one more nmos for NMOS

ON for two corresponding off

PMOS \rightarrow gate $\oplus 1$



$$\rightarrow t_{PDR} = \{(5hC + 9C) \times R\} +$$

$$(R + \cancel{R_B}) \times (3C) +$$

$$(R + \cancel{R_B} + \cancel{R_X}) \cdot (3C)$$

$$= 15RC + 5hRC$$

for $(3C)$ capacitance main node path

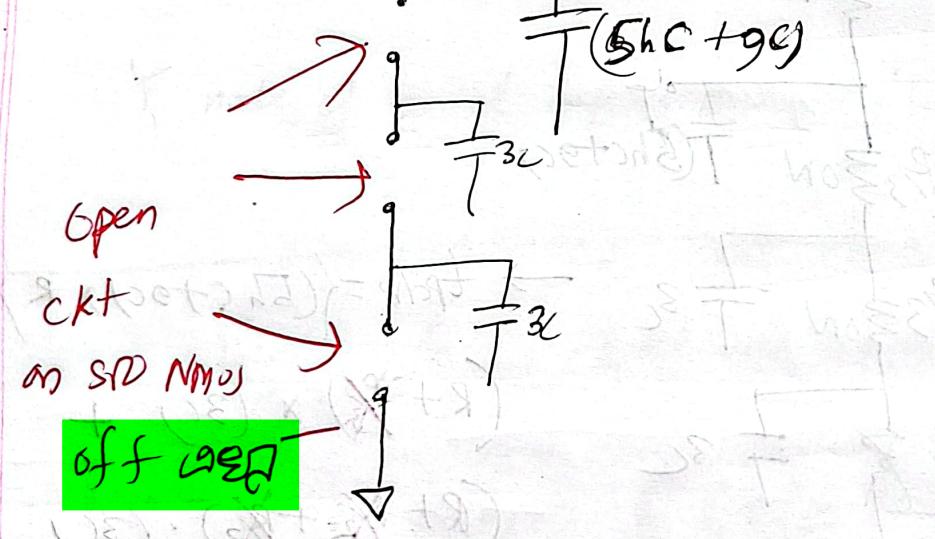
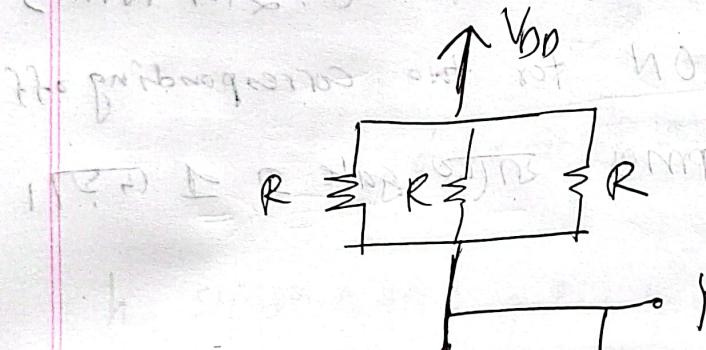
charging path \rightarrow resistance \rightarrow time

time \rightarrow 6 ns

t_{CDR} किसे \rightarrow 3 ए प्रॉजेक्शन वर फैटो? SD

NMOS ओवल वर फैटो. ला T_C (3C)

capacitance द्वारा देता है,



$$t_{CDR} = \left(\frac{1}{R} + \frac{1}{R} + \frac{1}{R} \right)^{-1} \cdot (5hC + 9C)$$

$$= \left(\frac{R}{3} \right) (5hC + 9C) \quad = 5hRC/3 + 3RC$$

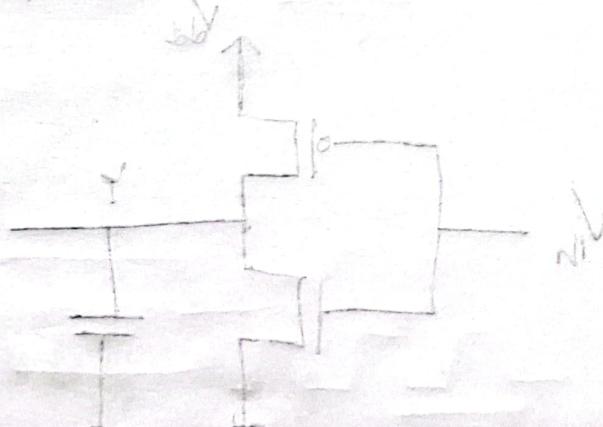
Delay components

Effort delay \rightarrow 'h' only gate delay component

\downarrow \downarrow needed
 $(5hRC)$ here time for a gate to drive
in t_{pd} the total load capacitance.

parasitic delay \rightarrow 'h' term 2 ($\frac{1}{2}$) =

\downarrow \downarrow
the time for a gate to drive its
own internal diffusion capacitance.
 $(12RC)$
in t_{pd}



A facility room has 3 temperature sensors placed at 3 corners, each with two output pins:

1. Analog temperature value pin (not considered here).
2. Green LED pin that indicates whether the sensor is functional:
 - o High (1): Sensor is functional, and the LED is on.
 - o Low (0): Sensor is not functional, and the LED is off.

If all three sensors (A, B, C) stop working simultaneously, an alarm must be triggered. Even if only one or two sensors stop working, the remaining functional sensors provide temperature data correctly.

Jim and Campbell are tasked to design a logic device that:

1. Triggers an alarm (output = HIGH) when all three LEDs are LOW.
2. Does nothing (output = LOW) otherwise.

Jim finally decided to implement a 3-input XOR gate, whereas Campbell chose a 3-input NOR gate to use as the alarm trigger. Take A, B, C as the inputs to the gates where A, B, C indicate the LED status(ie ON or OFF) of 1st, 2nd and 3rd sensor respectively.

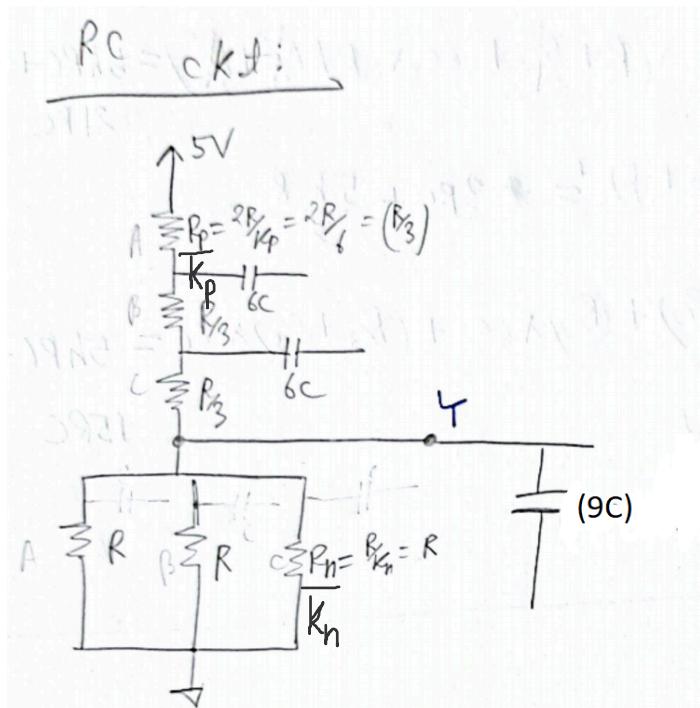
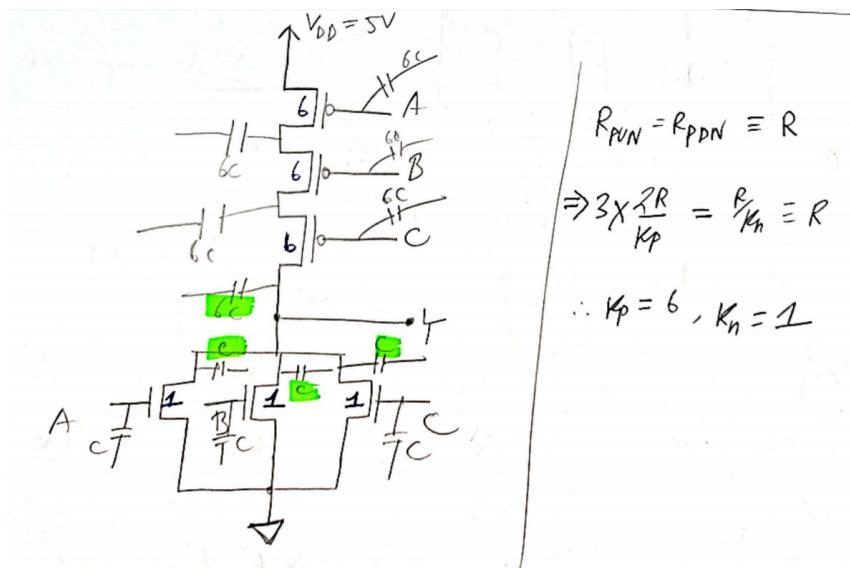
[Choose widths of PMOS and NMOS transistors to achieve worst-case effective rise and fall resistance equal to that of a unit inverter (R)]

(a)	Whose design is correct- Justify.	[1]
(b)	Draw the CMOS circuit of the correct logic function and derive the RC equivalent circuit.	[4]
(c)	Calculate t_{pdf} , t_{edf} , t_{pdr} , t_{cdr} for the circuit if the output is driving 'h' number of 2-input NAND gates as its load [Choose widths of PMOS and NMOS transistors to achieve effective rise and fall resistance equal to that of a unit inverter (R)]	[4]
(d)	Identify the parasitic and effort delay from the t_{pdf} .	[2]
(e)	For $\lambda = 10 \text{ nm}$, if $R = 5 \text{ k}\Omega.\mu\text{m}$, $C = 20 \text{ fF}/\mu\text{m}$, find the values of the delays whose expressions you found in (c). Take $h=5$.	[4]

NOR-3 delay model

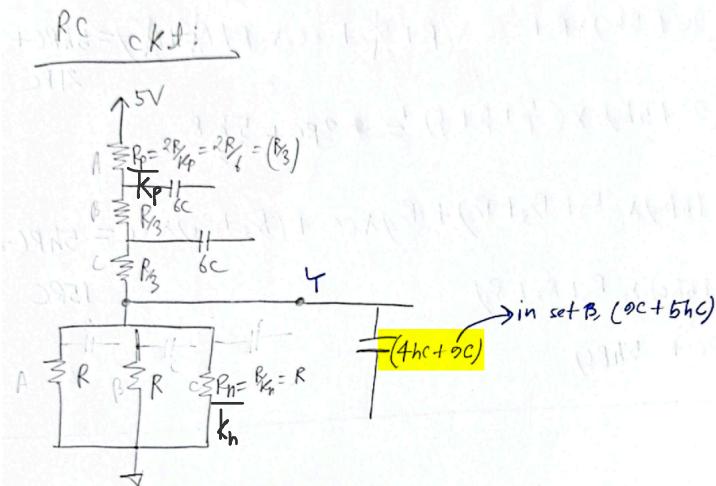
a. Campbell is correct.

b.



If output driven by no. of 2 ip NAND gates \rightarrow

$$\text{total capacitance at } y \text{ node} = (4hc + 9c)$$



t_{pdf} = worst fall \Rightarrow only $A = 1$ hence one NMOS on & PMOS also

ON due to $B = C = 0$. Hence upper 2 $6C$ will also discharge to GND.

$$t_{pdf} = (4hc + 9c) \times R + (6c)(R + R_3) + (6c)(R_3 + R) = (4hRC + 21RC)$$

t_{cdf} = best fall = all NMOS on ie $A = B = C = 1$ so all PMOS off

$$= (4hc + 9c) \times (R + R_3 + R) = \frac{4hCR}{3} + 3RC$$

$$t_{ppr} = \text{worst rise} = (4hc + 9c)(B_3 + R_3 + R_3) + (R_3) \times 6C + (R_3 + R_3) \times 6C \\ = 4hRC + 15RC$$

t_{cdr} = best rise = already t_{pdf} since $6C$ are charged \rightarrow

$$\therefore t_{cdr} = (4hc + 9c) \times (R_3 + R_3 + R_3) = (4hRC + 9RC)$$

c.

d. Effort delay = $4hRC$, Parasitic delay = $21RC$

20 nm technology \rightarrow hence $L_{eff} = 20 \text{ nm}$

$$\therefore \lambda = \frac{L_{eff}}{2} = (10 \text{ nm})$$

$$W = 4\lambda = 40 \text{ nm}$$

$$L = 2\lambda = 20 \text{ nm}$$

if $R = 5k\Omega \cdot \mu\text{m}$, $C = 20 \text{ fF}/\mu\text{m} \rightarrow$

$$R = \frac{5k\Omega \cdot \mu\text{m}}{W} = \frac{5k \cdot \mu\text{m}}{0.04 \mu\text{m}} = 125k\Omega$$

$$C = 20 \text{ fF}/\mu\text{m} \times W = (0.8 \text{ fF})$$

e.

Ans to e: tpdf=4.1ns, tcdf=0.967ns, tpdr=3.5ns, tcdr=2.9ns

A. Draw the CMOS level circuit to implement the following:

$$F = \overline{(AB + CD)}$$

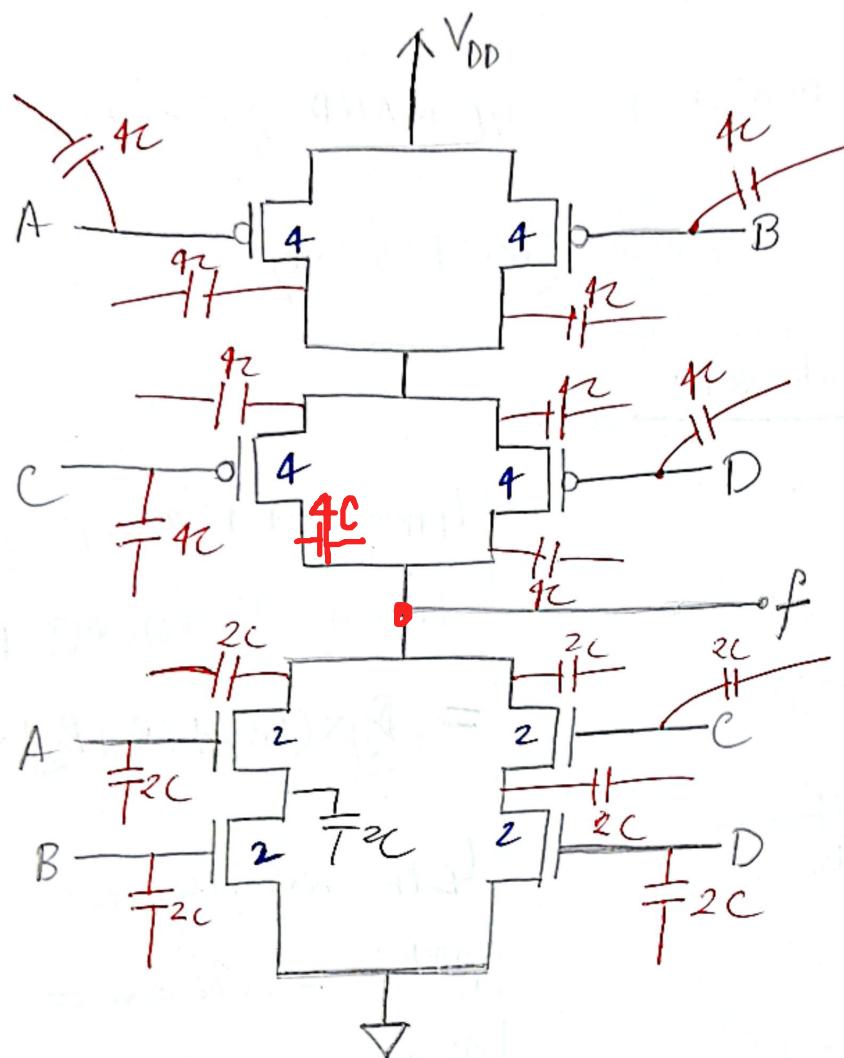
B. Now, sketch an RC equivalent circuit with widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R) .

C. Estimate t_{pdf} , t_{pdr} , t_{cdf} , and t_{cdr} for the circuit if the output is loaded with h identical 3 input NAND gates.

$$F = \overline{AB} + CD$$

can be used for XNOR
gate RC modelling

→ contacted diffusion here



for equal rise and fall resistance equal to unit inverter (R) \rightarrow

$$R_{PN} = R_{PD} \equiv R$$

$$\Rightarrow 2 \times \frac{2R}{K_p} = 2 \times \frac{R}{K_n} = R \quad [\text{given } \mu_n = 2\mu_p]$$

$$\therefore K_p = 4, K_n = 2$$

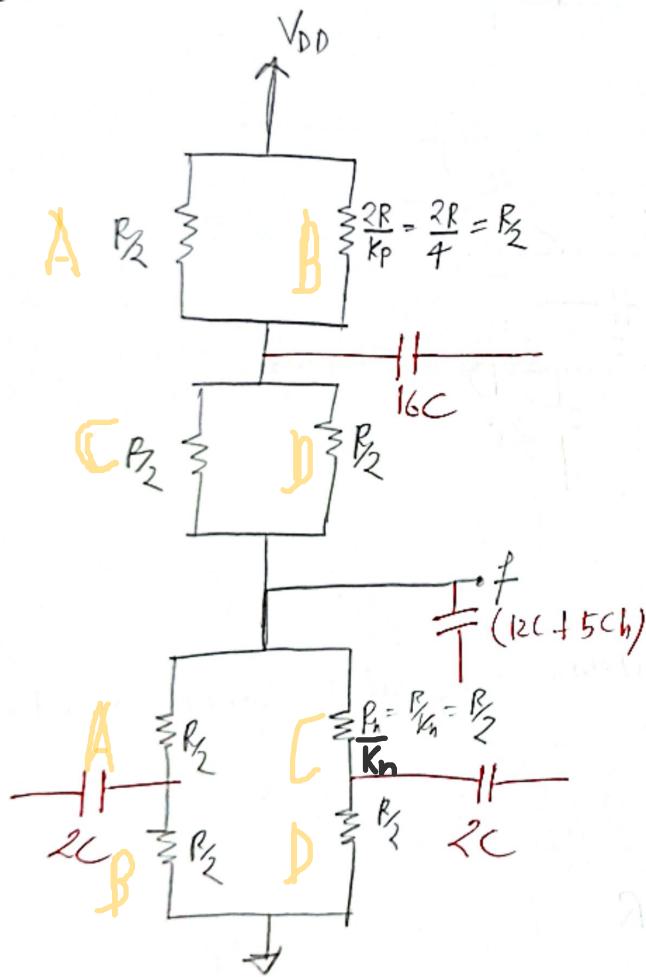
$$\text{total capacitance at } f = 2C + 2C + 4C + 4C = 12C$$

Set - A

if f drives h number of 3 input NAND gates \rightarrow

$$\text{total capacitance at f node} = (12C + 5Cxh)$$

RC equivalent ckt:



$$= (R_2) \times (16C) + (R_2 + R_2) \times (RC + 5HC)$$

$t_{RDR} = \text{best rise case} = \text{all pMOS are ON now} =$

$$\left(R_2 \parallel R_3 \right) \times 16C + \left\{ \left(R_1 \parallel R_2 \right) + \left(R_2 \parallel R_3 \right) \right\} \times \left(12C + 5hC \right)$$

t_{pdf} = worst fall = only $\frac{1}{200}$ —
NMOS branch ON

We should set $A=B=D=1, C=0 \rightarrow$

$$f_{PDF} = (12 + 54C) \times (R_2 + R_{\bar{2}}) + (16C) \times (\cancel{R_3} + R_2 + R_{\bar{2}}) +$$

$$2C(R_2) + 2Cx(\cancel{R_2}) =$$

left one *right one*

t_{Cdf} = best case fall = All NMOS are ON so all PMOS are off since $A=B=C=0=1$ now

$$\therefore t_{Cdf} = (RC + 5hc) \times \left\{ (R_2 + R_2) \parallel (R_2 + R_2) \right\}$$

[~~including 2C DM as we are assuming that in best case, these 2C are already discharged to zero.~~]

t_{PdR} = worst rise = only one PMOS from each parallel branch are ON \rightarrow let, ~~A~~ $B=0=0$ hence $A=C=1$.

$$\begin{aligned} \therefore t_{PdR} &= (RC + 5hc) \times (R_2 + R_2) + (16C) \times (R_2) + (2C) \times (R_2 + R_2) + (R_2) \\ &\quad + (2C) \times (R_2 + R_2) + (R_2) \end{aligned}$$

for C input NMOS
IT \rightarrow for DM
for A input NMOS

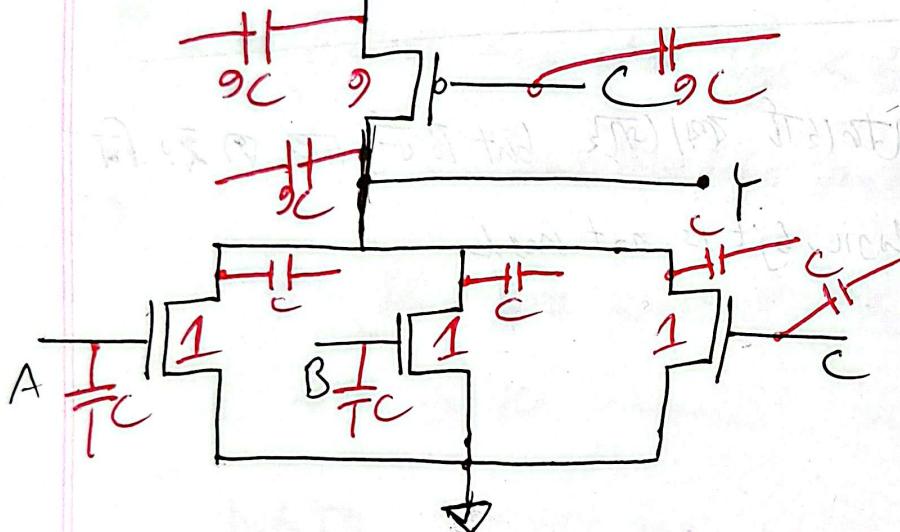
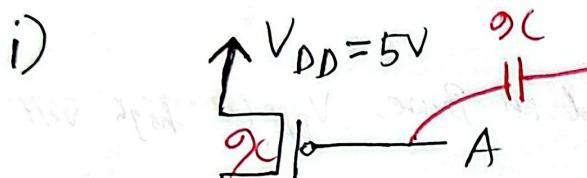
t_{CDR} = all PMOS ON hence all NMOS are off now; also assume that $16C$ is already charged to V_{DD} beforehand

$$= (RC + 5hc) \times \left\{ (R_2 \parallel R_2) + (R_2 \parallel R_2) \right\}$$

- i. Draw the CMOS circuit of 3 input NOR logic function and derive the final **RC equivalent circuit**. Note that electron mobility is three times the mobility of hole. [6]
- ii. Calculate t_{pdf} , t_{cdf} , t_{pdr} , t_{cdr} for the circuit if the output is driving ' h ' number of inverters as its load [Choose widths of PMOS and NMOS transistors to achieve effective rise and fall resistance equal to that of a unit inverter (R)] [8]
- iii. Identify the parasitic and effort delay from the t_{pdf} . [2]
- iv. For 50 nm technology, if $R = 20k\Omega.\mu m$, $C = 20fF/\mu m$, find the values of the delays whose expressions you found in ii. Take $h=10$. [4]

3 input NOR for $M_n = 3 \mu p$

As $M_n = 3 \mu p \rightarrow R_n = R = \frac{R_p}{3} \quad [\because R_x \propto \frac{1}{M_x}]$



here, as stated,

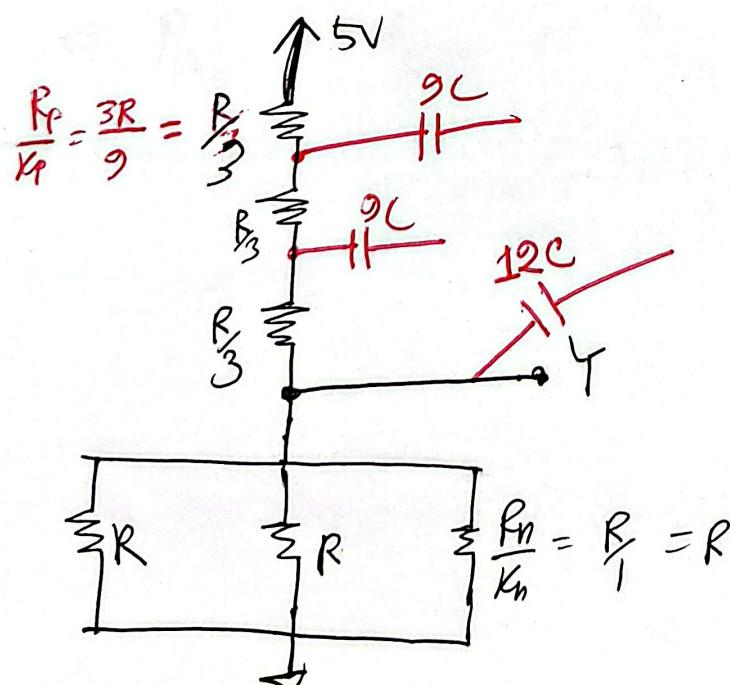
$$R_{PUN} = R_{PDN} = R$$

$$\Rightarrow 3 \times \frac{R_p}{K_p} = 1 \times \frac{R_n}{K_n} = R$$

$$\Rightarrow \frac{(9R)}{K_p} = \frac{(R)}{K_n} = R$$

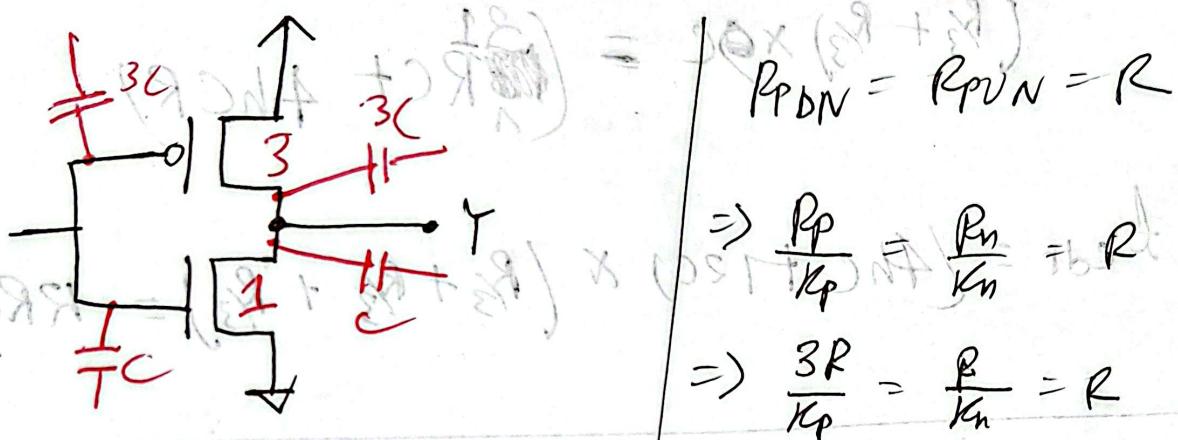
$$\therefore K_p = 9, K_n = 1$$

\Downarrow RC ckt drawn below



iii) Using $R_{PDN} = R_{PVN}$ for common inverter

$$\text{where } R_p = 3R_n = 3R \Rightarrow (S_1 + D_1) = 169 \Omega$$



$$\therefore K_p = 3, K_n = 1$$

hence, at gate, for each inverter, we get $(3C + C)$
 $= (4C)$ total.

hence at Y node, total capacitance $= (12C + 4C \times h)$

for driving h no. of inverters at load.

$$t_{PDF} = (12C + 4hC) \times R + 9C \times (R + R_b) + 9C \times (R + R_b)$$

$$= 30RC + 4RC_h$$

$$208.08 = 8.5 \mu s$$

Setup = pulse train, $208 \mu s$ = settling time

$$t_{Cdf} = (4hc + 12c) \times \left(\frac{1}{R} + \frac{1}{R_3} + \frac{1}{R} \right)^{-1} = \left(4Rc + \frac{4}{3}Rch \right)$$

$$t_{Pdr} = (4hc + 12c) \times (R_3 + R_3 + R_3) + R_3 \times \cancel{OC} +$$

$$(R_3 + R_3) \times \cancel{OC} = (\cancel{R}c + 4hcR)$$

$$t_{Cdr} = (4hc + 12c) \times (R_3 + R_3 + R_3) = RRc + 4hRC$$

i) $50 \text{ nm tech} \Rightarrow L = 50 \text{ nm} \quad \therefore A = \frac{L}{2} = 25 \text{ nm}$

$\omega = 4\lambda = 100 \text{ nm}$

$$R = \frac{20 \text{ k} \Omega \cdot \text{mm}}{\omega} = \frac{20 \text{ k} \Omega \cdot \text{mm}}{0.1 \text{ mm}} = 200 \text{ k} \Omega$$

$$C = \frac{20 \text{ fF}}{\text{mm}} \times \omega = \frac{20 \text{ fF}}{\text{mm}} \times 0.1 \text{ mm} = 2 \text{ fF}$$

$$\therefore t_{Pdr} = 28 \times 10^{-9} \text{ s} = 28 \text{ ns} = 7 \text{ bits}$$

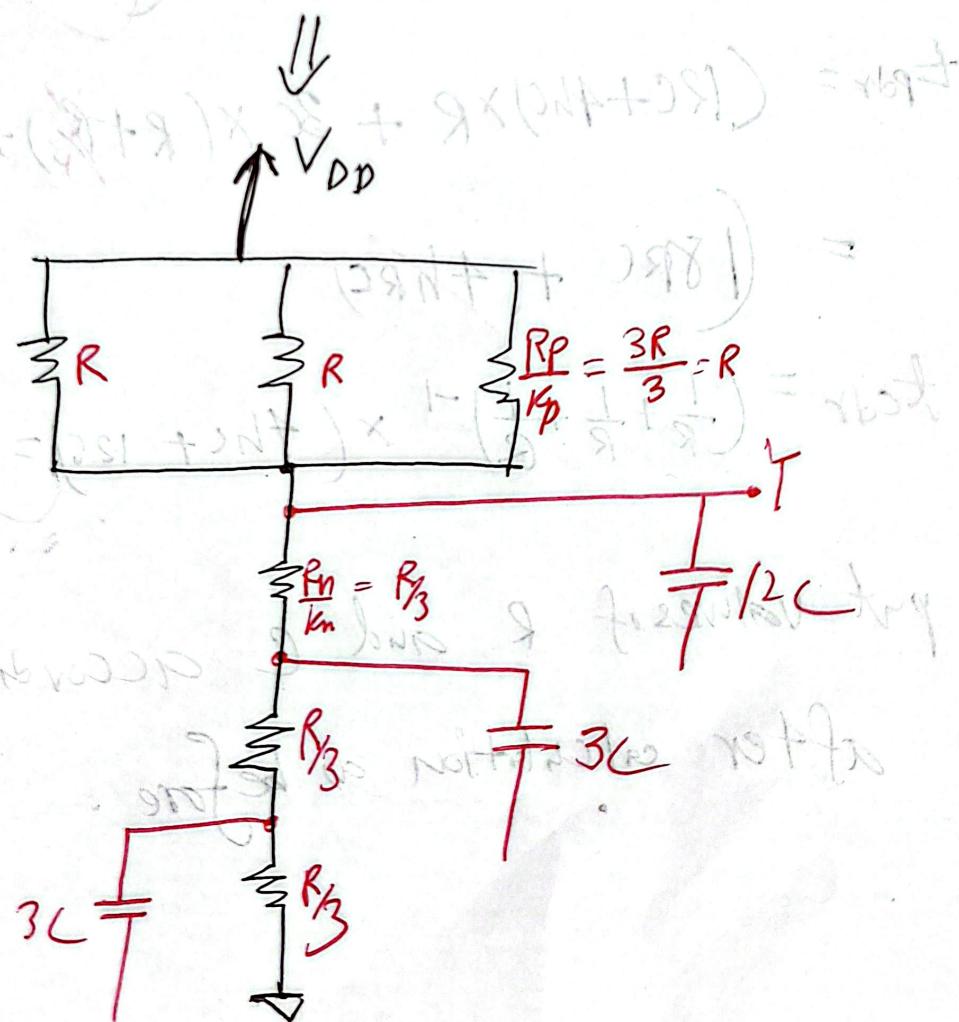
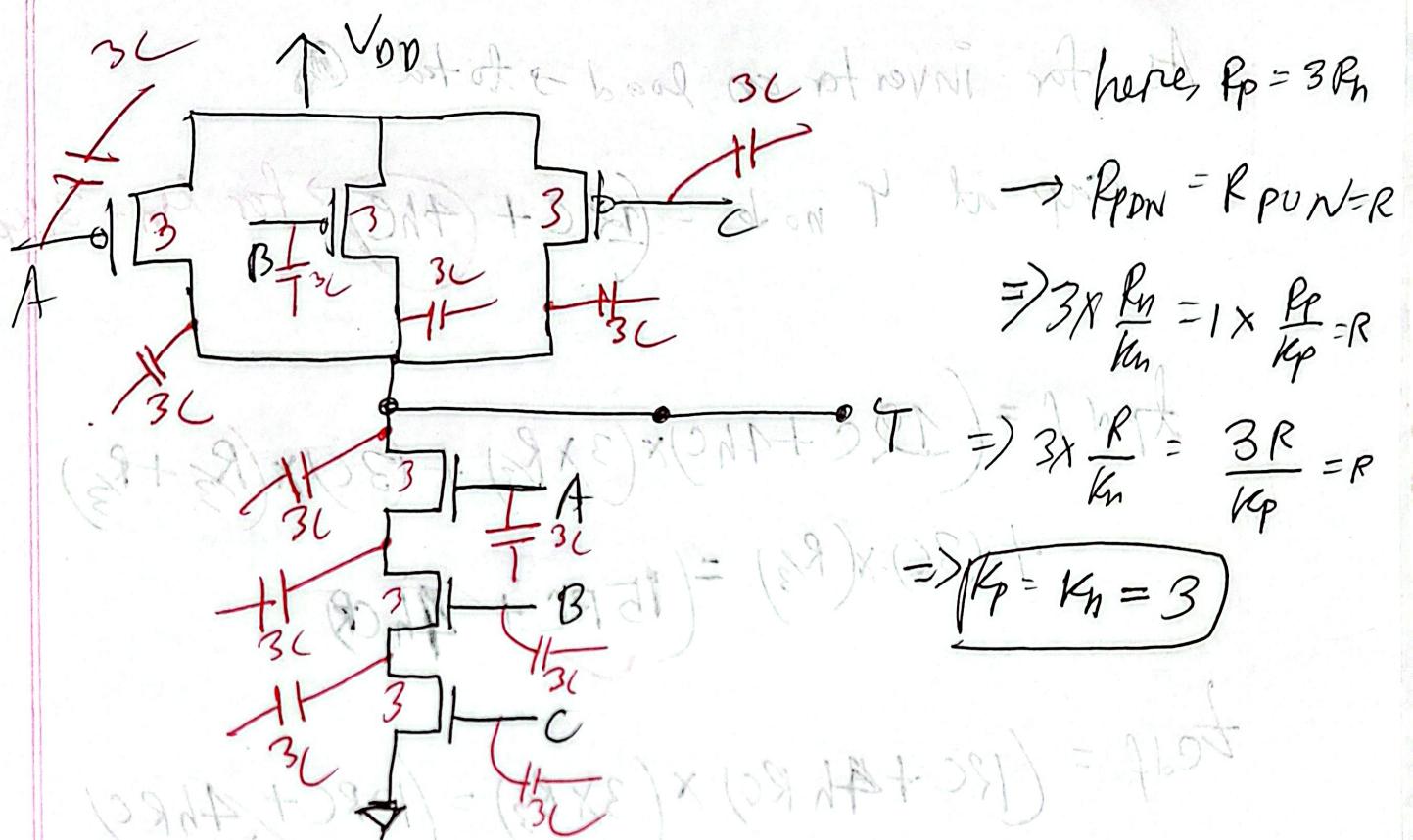
$$t_{Pdr} = 24.4 \text{ ns}$$

$$t_{Cdf} = 6.933 \text{ ns} \quad 1094 + 2908 =$$

$$t_{Cdr} = 20.8 \text{ ns}$$

ii) parasitic = ~~30~~ $30RC$, effort delay = $4hRC$

- i. Draw the CMOS circuit of 3 input NAND logic function and derive the final **RC equivalent circuit**. Note that electron mobility is three times the mobility of hole. [6]
- ii. Calculate t_{pdf} , t_{cdf} , t_{pdr} , t_{cdr} for the circuit if the output is driving ' h ' number of inverters as its load [Choose widths of PMOS and NMOS transistors to achieve effective rise and fall resistance equal to that of a unit inverter (R)] [8]
- iii. Identify the parasitic and effort delay from the t_{pdf} . [2]
- iv. For 50 nm technology, if $R = 40k\Omega.\mu m$, $C = 50fF/\mu m$, find the values of the delays whose expressions you found in ii. Take $h=10$. [4]



As for inverter as load \rightarrow total ~~total~~

$$\text{Cap at } Y \text{ node} = (12C + 4hC) \rightarrow \text{for } M_n = 3 \mu p$$

$$t_{pdif} = (12C + 4hC) \times (3 \times R_3) + (3C) \times (R_3 + R_3) \\ + (3C) \times (R_3) = (15RC + 4hRC)$$

$$t_{cdif} = (RC + 4hRC) \times (3 \times R_3) = (12RC + 4hRC)$$

$$t_{pdr} = (RC + 4hC) \times R + 3C \times (R + R_3) + 3C \times (R + R_3 + R) \\ = (18RC + 4hRC)$$

$$t_{cdr} = \left(\frac{1}{R} + \frac{1}{R} + \frac{1}{R} \right)^{-1} \times (4hC + 12C) = 4RC + \frac{4hRC}{3}$$

put values of R and C accordingly.

after calculation as before.