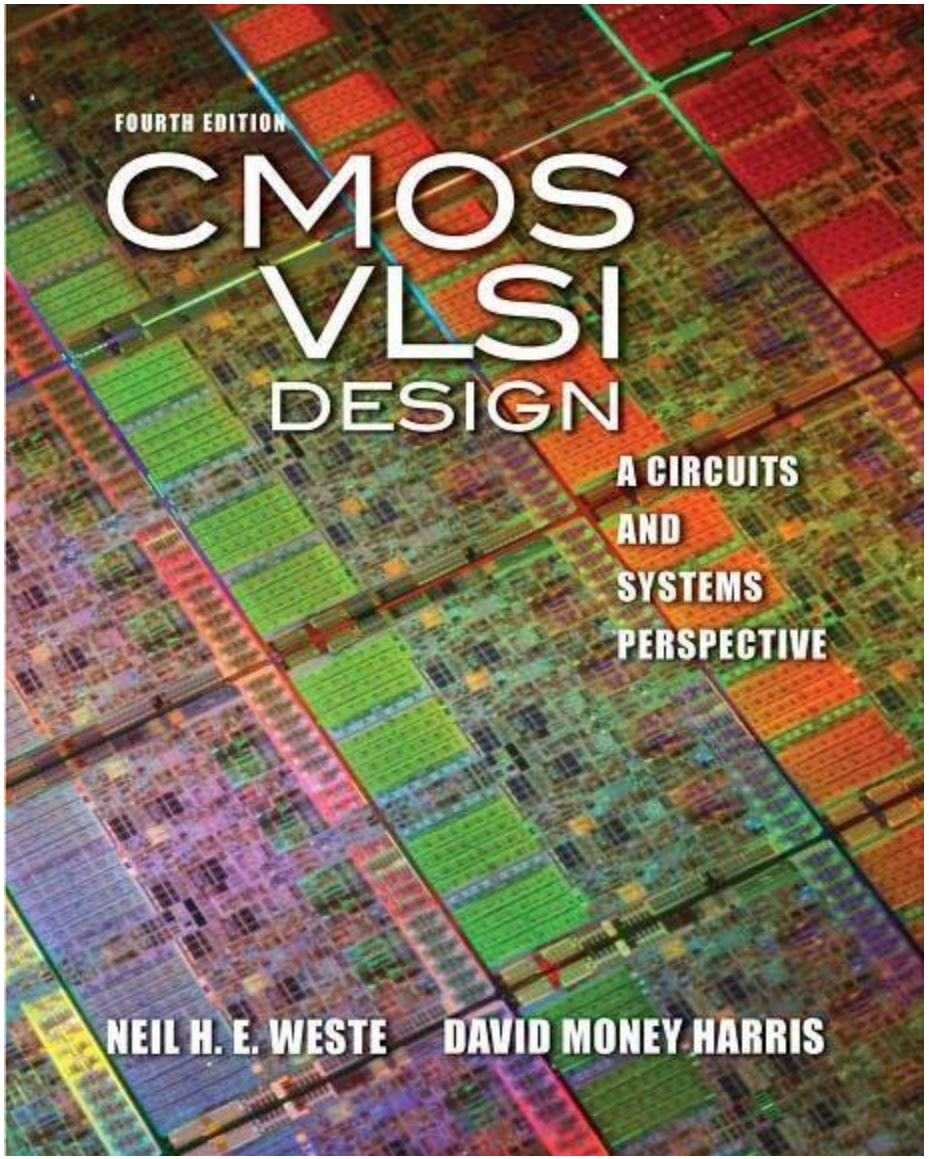
FOURTH EDITION
CMOS VLSI DESIGN
A CIRCUITS AND SYSTEMS PERSPECTIVE
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CMOS Power

Outline

- Power and Energy
- Dynamic Power
- Static Power

Power and Energy

- Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.
- Instantaneous Power: $P(t) = I(t)V(t)$
- Energy: $E = \int_0^T P(t)dt$
- Average Power: $P_{\text{avg}} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt$

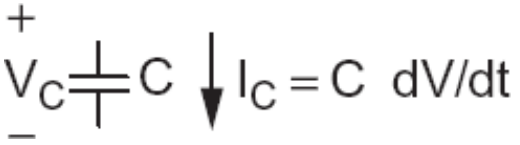
Power in Circuit Elements

$$P_{VDD}(t) = I_{DD}(t) V_{DD}$$

$$P_R(t) = \frac{V_R^2(t)}{R} = I_R^2(t) R$$

$$E_C = \int_0^\infty I(t) V(t) dt = \int_0^\infty C \frac{dV}{dt} V(t) dt$$

$$= C \int_0^{V_C} V(t) dV = \tfrac{1}{2} C V_C^2$$



Charging a Capacitor

- When the gate output rises
  - Energy stored in capacitor is

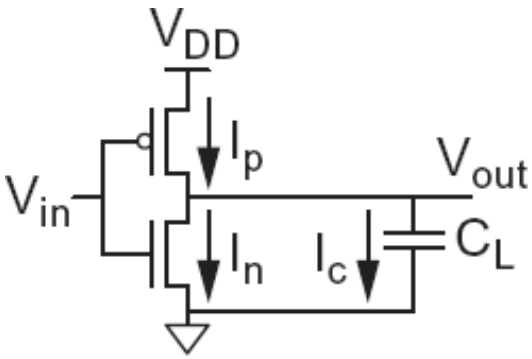
$$E_C = \tfrac{1}{2} C_L V_{DD}^2$$

  - But energy drawn from the supply is

$$E_{VDD} = \int_0^\infty I(t) V_{DD} dt = \int_0^\infty C_L \frac{dV}{dt} V_{DD} dt$$

$$= C_L V_{DD} \int_0^{V_{DD}} dV = C_L V_{DD}^2$$

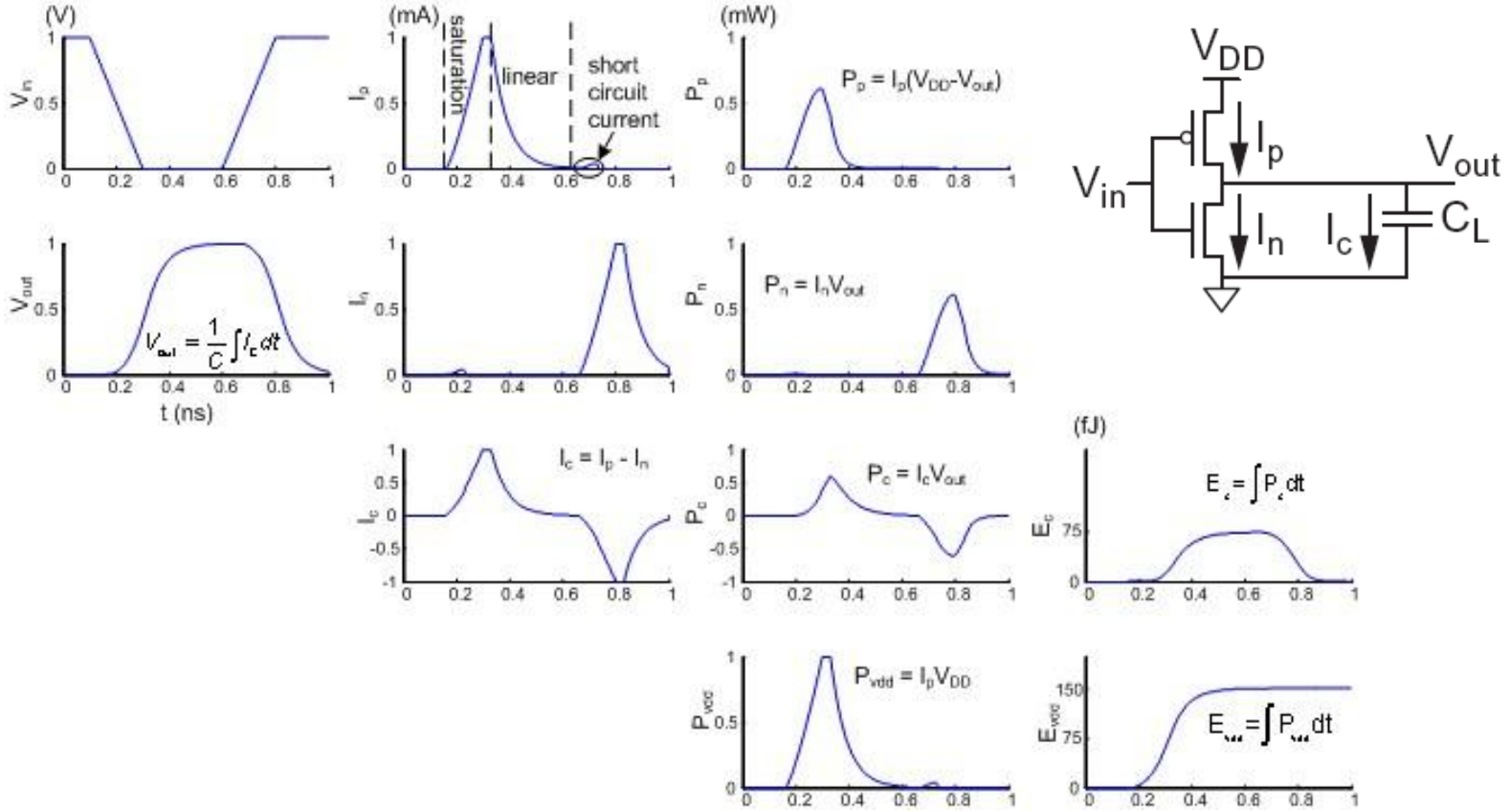
  - Half the energy from V_{DD} is dissipated in the pMOS transistor as heat, other half stored in capacitor



- When the gate output falls
  - Energy in capacitor is dumped to GND
  - Dissipated as heat in the nMOS transistor

Switching Waveforms

- Example: V_{DD} = 1.0 V, C_L = 150 fF, f = 1 GHz



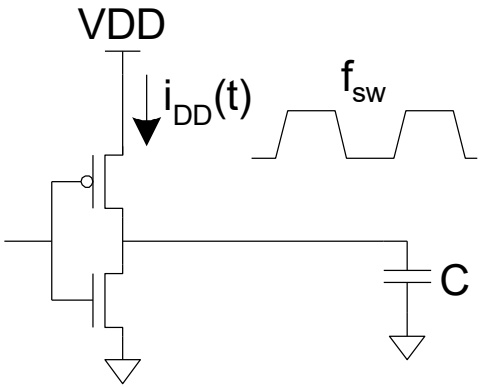
Switching Power

$$P_{\text{switching}} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt$$

$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$$

$$= \frac{V_{DD}}{T}\left[Tf_{\text{sw}}CV_{DD}\right]$$

$$= CV_{DD}{}^2 f_{\text{sw}}$$



Activity Factor

- Suppose the system clock frequency = f
- Let $f_{sw} = \alpha f$, where α = activity factor
  - If the signal is a clock, $\alpha = 1$
  - If the signal switches once per cycle, $\alpha = ½$

- Dynamic power:

$$P_{\text{switching}} = \alpha C V_{DD}^{\ 2} f$$

Short Circuit Current

- When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- Leads to a blip of “short circuit” current.
- < 10% of dynamic power if rise/fall times are comparable for input and output
- We will generally ignore this component

Power Dissipation Sources

- $P_{total} = P_{dynamic} + P_{static}$
- Dynamic power: $P_{dynamic} = P_{switching} + P_{shortcircuit}$
  - Switching load capacitances
  - Short-circuit current
- Static power: $P_{static} = (I_{sub} + I_{gate} + I_{junct} + I_{contention})V_{DD}$
  - Subthreshold leakage
  - Gate leakage
  - Junction leakage
  - Contention current

Dynamic Power Example

- 1 billion transistor chip
  - 50M logic transistors
    - Average width: 12 λ
    - Activity factor = 0.1
  - 950M memory transistors
    - Average width: 4 λ
    - Activity factor = 0.02
  - 1.0 V 65 nm process (with 50 nm drawn gate lengths and $\lambda = 25\ nm$)
  - C = 1 fF/μm (gate) + 0.8 fF/μm (diffusion)
- Estimate dynamic power consumption @ 1 GHz. Neglect wire capacitance and short-circuit current.

Solution

$$C_{\text{logic}} = \left(50\times10^{6}\right)\left(12\lambda\right)\left(0.025\mu m/\lambda\right)\left(1.8\,fF/\mu m\right) = 27\ \text{nF}$$
$$C_{\text{mem}} = \left(950\times10_{6}\right)\left(4\lambda\right)\left(0.025\mu m/\lambda\right)\left(1.8\,fF/\mu m\right) = 171\ \text{nF}$$

$$P_{\text{dynamic}} = \left\lfloor \left\lceil 0.1C_{\text{logic}} + 0.02C_{\text{mem}} \right\rceil \right\rfloor \left(1.0\right)^{2}\left(1.0\ \text{GHz}\right) = 6.1\ \text{W}$$

Alternative Solution

$P_{sw} = N \times \alpha C V_{DD}^2 f_{clk}$

Also, $C = C/\mu m * W\ (in\ \mu m)$

Switching Power

For Logic MOS

$W = 12\lambda, \lambda = 25\ nm = 0.025\ \mu m$

$$\boldsymbol{P_{sw}(Logic) = 50 \times 10^6 \times 0.1 \times 1.8 \times 10^{-15} F/\mu m \times 12 \times 0.025 \mu m \times (1V)^2 \times 10^9\ Hz}$$
$$= 2.7\ W$$

For Memory MOS

$$\boldsymbol{P_{sw}(Memory) = 950 \times 10^6 \times 0.02 \times 1.8 \times 10^{-15} F/\mu m \times 4 \times 0.025 \mu m \times (1V)^2 \times 10^9\ Hz}$$
$$= 3.42\ W$$

$$P_{sw} = 2.7 + 3.42 = 6.12\ W$$

Dynamic Power Reduction

- $P_{\text{switching}} = \alpha C V_{DD}^{\ 2} f$
- Try to minimize:
  - Activity factor
  - Capacitance
  - Supply voltage
  - Frequency

Example:

Example 5.1

A digital system-on-chip in a 1 V 65 nm process (with 50 nm drawn channel lengths and λ = 25 nm) has 1 billion transistors, of which 50 million are in logic gates and the remainder in memory arrays. The average logic transistor width is 12 λ and the average memory transistor width is 4 λ. The memory arrays are divided into banks and only the necessary bank is activated so the memory activity factor is 0.02. The static CMOS logic gates have an average activity factor of 0.1. Assume each transistor contributes 1 fF/μm of gate capacitance and 0.8 fF/μm of diffusion capacitance. Neglect wire capacitance for now (though it could account for a large fraction of total power). Estimate the switching power when operating at 1 GHz.

SOLUTION: There are $(50 \times 10^6$ logic transistors$)(12\ \lambda)(0.025\ \mu m/\lambda)((1 + 0.8)\ fF/\mu m) =$ 27 nF of logic transistors and $(950 \times 10^6$ memory transistors$)(4\ \lambda)(0.025\ \mu m/\lambda)((1 +$ 0.8) fF/μm) = 171 nF of memory transistors. The switching power consumption is $[(0.1)(27 \times 10^{-9}) + (0.02)(171 \times 10^{-9})](1.0\ V)^2(10^9\ Hz) = 6.1$ W.

Example:

Solution (5.1)

$P_{sw} = N \times \alpha C V_{DD}^2 f_{clk}$

Also, $C = C/\mu m * W$ ($in\ \mu m$)

Switching Power

For Logic MOS

$W = 12\lambda, \lambda = 25\ nm = 0.025\ \mu m$

$P_{sw}(Logic) = 50 \times 10^6 \times 0.1 \times 1.8 \times 10^{-15} F/\mu m \times 12 \times 0.025 \mu m \times (1V)^2 \times 10^9\ Hz$

$= 2.7\ W$

For Memory MOS

$P_{sw}(Memory) = 950 \times 10^6 \times 0.02 \times 1.8 \times 10^{-15} F/\mu m \times 4 \times 0.025 \mu m \times (1V)^2 \times 10^9\ Hz$

$= 3.42\ W$

$P_{sw} = 2.7 + 3.42 = 6.12\ W$

Example:

Example 5.4

Consider the system-on-chip from Example 5.1. Subthreshold leakage for OFF devices is 100 nA/μm for low-threshold devices and 10 nA/μm for high-threshold devices. Gate leakage is 5 nA/μm. Junction leakage is negligible. Memories use low-leakage devices everywhere. Logic uses low-leakage devices in all but 5% of the paths that are most critical for performance. Estimate the static power consumption.

SOLUTION: There are $(50 \times 10^6$ logic transistors$)(0.05)(12\ \lambda)(0.025\ \mu m/\lambda) = 0.75 \times 10^6$ μm of low-threshold devices and $[(50 \times 10^6$ logic transistors$)(0.95)(12\ \lambda) + (950 \times 10^6$ memory transistors$)(4\ \lambda)](0.025\ \mu m/\lambda) = 109.25 \times 10^6\ \mu$m of high-threshold devices. Neglecting the benefits of series stacks, half the transistors are OFF and contribute subthreshold leakage. Half the transistors are ON and contribute gate leakage. $I_{sub} = [(0.75 \times 10^6\ \mu m)(100\ nA/\mu m) + (109.25 \times 10^6\ \mu m)(10\ nA/\mu m)]/2 = 584$ mA. $I_{gate} = ((0.75 + 109.25) \times 10^6\ \mu m)(5\ nA/\mu m)/2 = 275$ mA. $P_{static} = (584\ mA + 275\ mA)(1\ V) = 859$ mW. This is 15% of the switching power and is enough to deplete the battery of a hand-held device rapidly.

Example:

Solution (5.4)

$P_{sub} = N * I_{sub} * V_{DD}$, $P_{gate} = N * I_{gate} * V_{DD}$

Also, $I_{sub} = I_{sub}/\mu m \ * W \ (in \ \mu m)$

Subthreshold leakage power

For Logic MOS

(5% $\rightarrow I_{sub}/um = 100 \ nA/\mu m$ and 95% $\rightarrow I_{sub}/um = 10 \ nA/\mu m$)

$W = 12\lambda, \lambda = 25 \ nm = 0.025 \ \mu m$

$$P_{sub}(Logic) = 0.05 \times 50 \times 10^6 \ * 100 \times 10^{-9} A/\mu m \ 12 \times 0.025 \mu m \times 1V$$
$$+0.95 \times 50 \times 10^6 \ * 10 \times 10^{-9} A/\mu m \ 12 \times 0.025 \mu m \times 1V$$
$$= 0.2175W$$

Example:

For Memory MOS (For all, $\rightarrow I_{sub}/um = 10\ nA/\mu m$

$W = 4\lambda, \lambda = 25\ nm = 0.025\ \mu m$

$P_{sub}(Mem\ ) = 950 \times 10^6 \times 10 \times 10^{-9} A/\mu m\ 4 \times 0.025 \mu m \times 1V = 0.95\ W$

$$\boldsymbol{P_{sub} = 0.2125 + 0.95 = 1.1675W}$$

Gate leakage power

For Logic ($I_{gate}/\mu m \rightarrow 5nA/\mu m$)

$W = 12\lambda$

$P_{gate}(logic\ ) = 50 \times 10^6 \times 5 \times 10^{-9} A/\mu m\ 12 \times 0.025 \mu m \times 1V = 0.075W$

For Memory ($I_{gate}/\mu m \rightarrow 5nA/\mu m$)

$P_{gate}(logic\ ) = 950 \times 10^6 \times 5 \times 10^{-9} A/\mu m\ 4 \times 0.025 \mu m \times 1V = 0.475\ W$

$$\boldsymbol{P_{gate} = 0.075 + 0.475 = 0.55W}$$

When Transistor are on, it consumes the gate leakage power and off, it consumes the sub threshold power. Let's assume 50% of them are off and 50% are on.

$$\boldsymbol{P_{Static} = 0.5 \times 1.1675 + 0.5 \times 0.55 = 0.85875W}$$

Example:

Suppose the technology you are using to design a VLSI system has $\lambda = 80$ nm, a clock frequency of **5 MHz**, and a supply is **5 V**. The chip you are designing has **5 million transistors**, of which 1 million remain **active** at any given time. The gate and diffusion capacitances are 12 fF/μm and 5 fF/μm, respectively. The gate width is **20λ**. You also obtain the following power consumption data:

- Short circuit power = 0.5 W
- Leakage power = 0.01 W
- Subthreshold power = 0.02 W

The **acceptable TOTAL power consumption** of a chip is **3 W.**

(a)	**Find** the activity factor and load capacitance of the system described above.	**[2]**
(b)	**Calculate** the switching power consumption of the chip.	**[3]**
(c)	**Calculate** the dynamic and static power of the chip. Thereafter calculate the **TOTAL** power consumption.	**[3]**
(d)	Is the **TOTAL** power consumption within the acceptable range? If not, **find** the maximum clock frequency to keep the **TOTAL** power within the acceptable range?	**[4]**

Example:

A chip contains 1 billion transistors made from a 0.7 V 120 nm technology with $\lambda = 60$ nm. Out of them, 100 million are logic gates, 200 million are never on, and the rest are memory arrays. Suppose that the logic gates operate at 1 GHz, the memory arrays operate at 3 GHz, and the clock frequency is 10 GHz. For all transistors, the gate and diffusion capacitance are 1.2 fF/um and 1.7 fF/um. The average width for logic gates and memory arrays are 4λ and 5λ, respectively. The following power data are given for the entire chip,

- Gate leakage power = 10 W
- Junction leakage power = 20 W
- Subthreshold power = 5 W
- Short circuit power of the logic gates = 60 W
- Short circuit power of the memory arrays = 70 W

The maximum acceptable power consumption of the chip is 1 kW.

(a)	**Find** the activity factor of the logic gates and the memory arrays.	**[2]**
(b)	**Find** the total switching power of each of the three kinds of transistors.	**[6]**
(c)	**Find** the static, dynamic, and total power of the entire chip.	**[3]**
(d)	Is the total power consumption within the acceptable range? If not, **find** the supply voltage that will keep it within range.	**[4]**