CSE 460: VLSI Design

Lecture 10: Finite State Machines (part 3)

Example-3: Swapping Contents of two registers

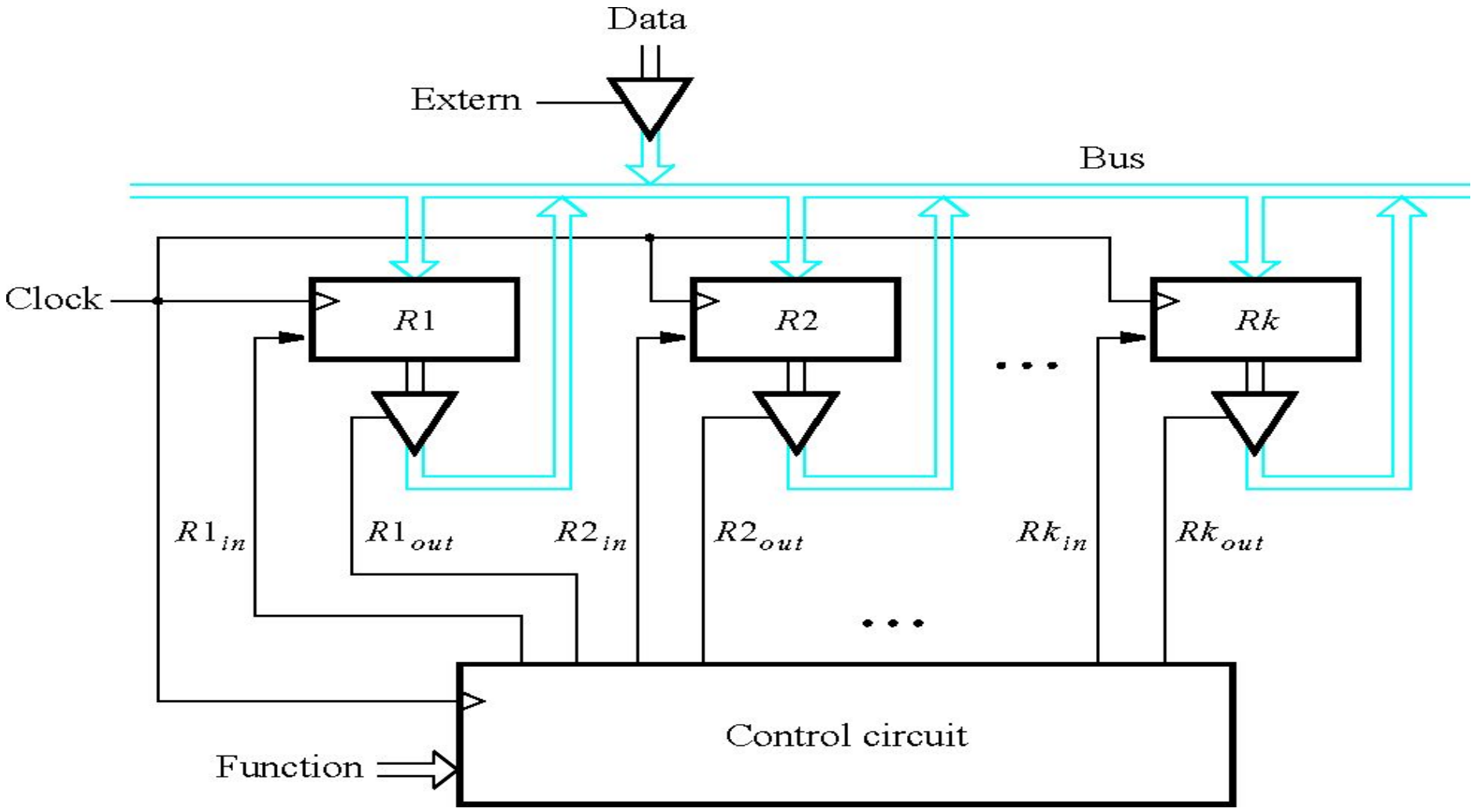


Figure 7.55. A digital system with *k* registers.

Example-3: Swapping Contents of two registers

Sometimes it is necessary to swap **the contents of two registers**. Typically, this is done by using a temporary location, which is usually a third register.

For example, suppose that we want to **swap the contents of registers R1 and R2**. We can achieve this by first transferring the contents of **R2** into the **third register, say R3**. Next, we transfer the contents of R1 into R2. Finally, we transfer the contents of R3 into R1.

Example-3: Swapping Contents of two registers

Task:

1. R2 -> R3
2. R1 -> R2
3. R3 -> R1

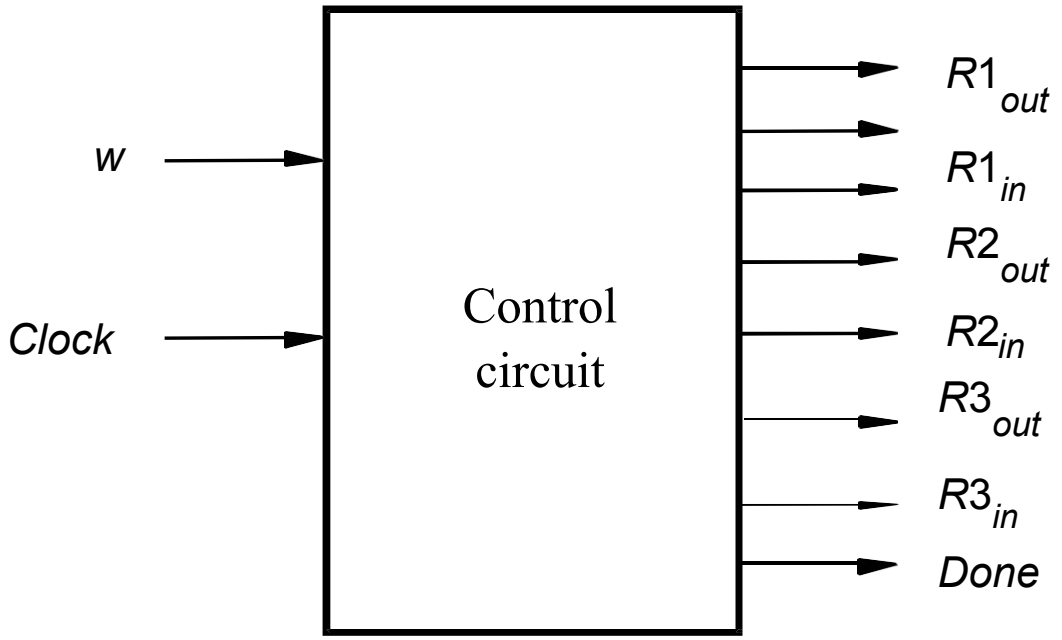


Figure 8.10. Signals needed in this example.

Example-3: Swapping Contents of two registers

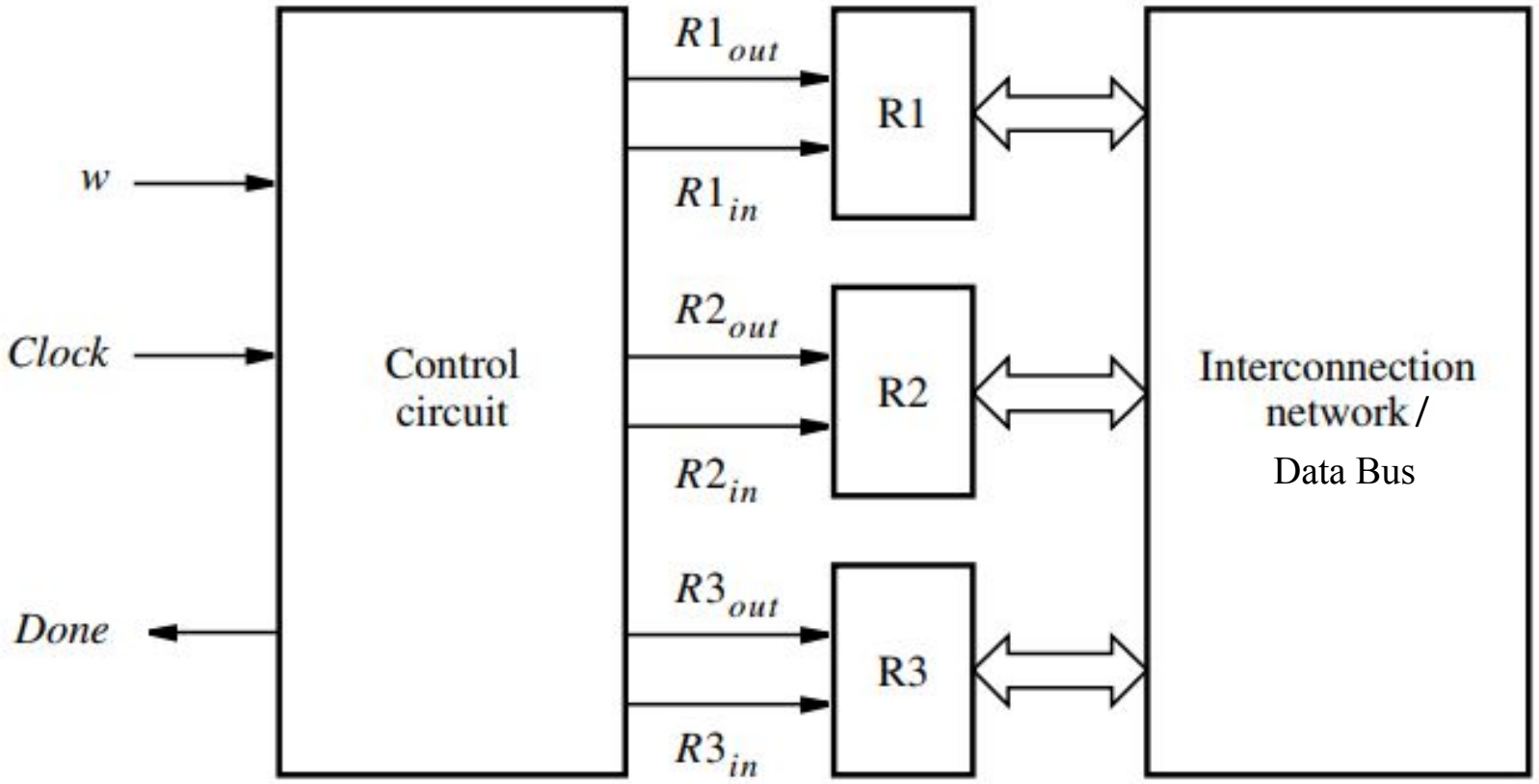
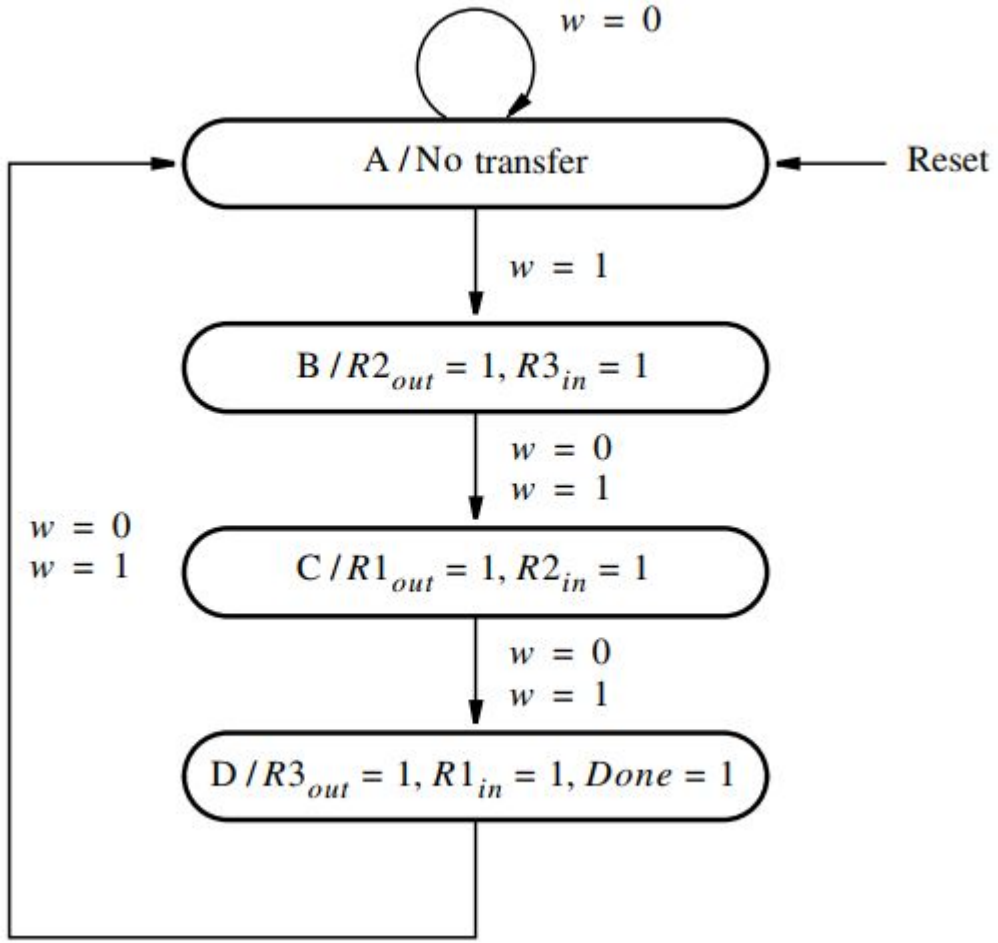


Figure 6.10 The whole system for this example

Example-3: Swapping Contents of two registers (Moore Type)

Once the swapping request arrives (w=1), w is neglected until the process ends (done=1)



Steps->

- ➢ **State diagram**
- ➢ State table
- ➢ State assigned table
- ➢ K-map
- ➢ Circuit

Figure 8.11. State diagram for this example.

Example-3: Swapping Contents of two registers

Present state	Next state		Outputs						
	$w = 0$	$w = 1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	$Done$
A	A	B	0	0	0	0	0	0	0
B	C	C	0	0	1	0	0	1	0
C	D	D	1	0	0	1	0	0	0
D	A	A	0	1	0	0	1	0	1

Figure 8.12. State table for Example 8.1.

Steps->

- State diagram
- **State table**
- State assigned table
- K-map
- Circuit

Example-3: Swapping Contents of two registers

	Present state	Next state		Outputs						
		$w = 0$	$w = 1$							
	y_2y_1	Y_2Y_1	Y_2Y_1	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	$Done$
A	00	00	0 1	0	0	0	0	0	0	0
B	01	10	1 0	0	0	1	0	0	1	0
C	10	11	1 1	1	0	0	1	0	0	0
D	11	00	0 0	0	1	0	0	1	0	1

Figure 8.13. State-assigned table for the sequential circuit in Figure 8.12.

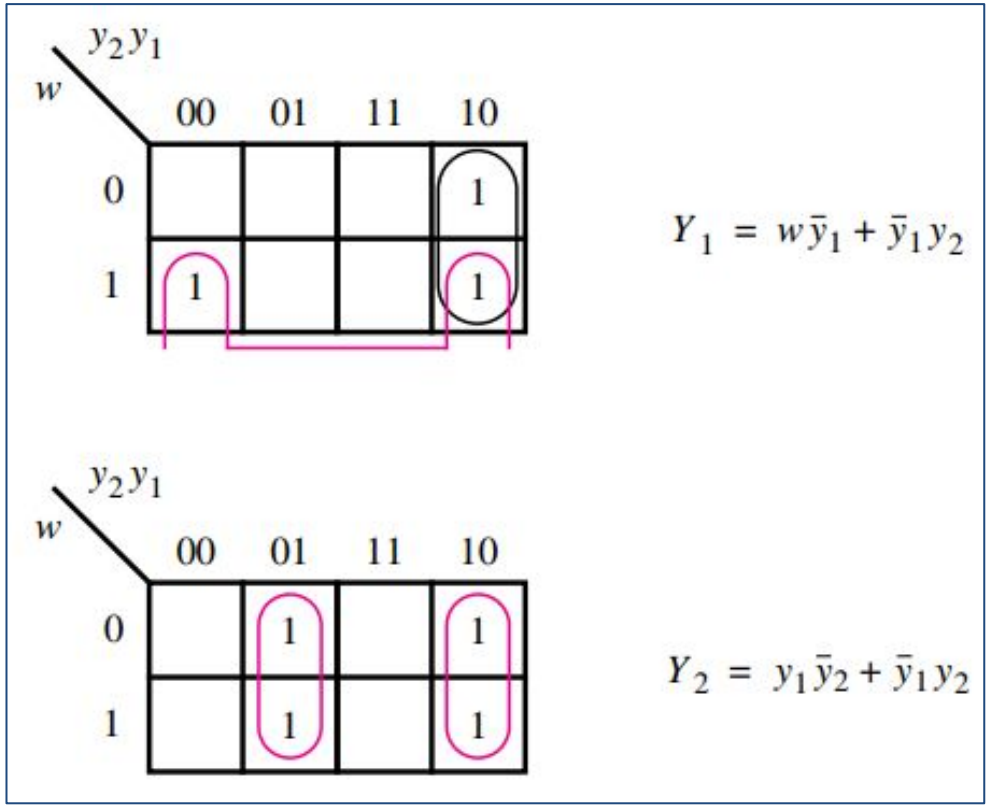
outputs = f(y_1,y_2)

$$R1_{out} = R2_{in} = \bar{y}_1 y_2$$
$$R1_{in} = R3_{out} = Done = y_1 y_2$$
$$R2_{out} = R3_{in} = y_1 \bar{y}_2$$

Steps->

- State diagram
- State table
- **State assigned table**
- K-map
- Circuit

Example-3: Swapping Contents of two registers



Steps->

- ➢ State diagram
- ➢ State table
- ➢ State assigned table
- ➢ **K-map**
- ➢ Circuit

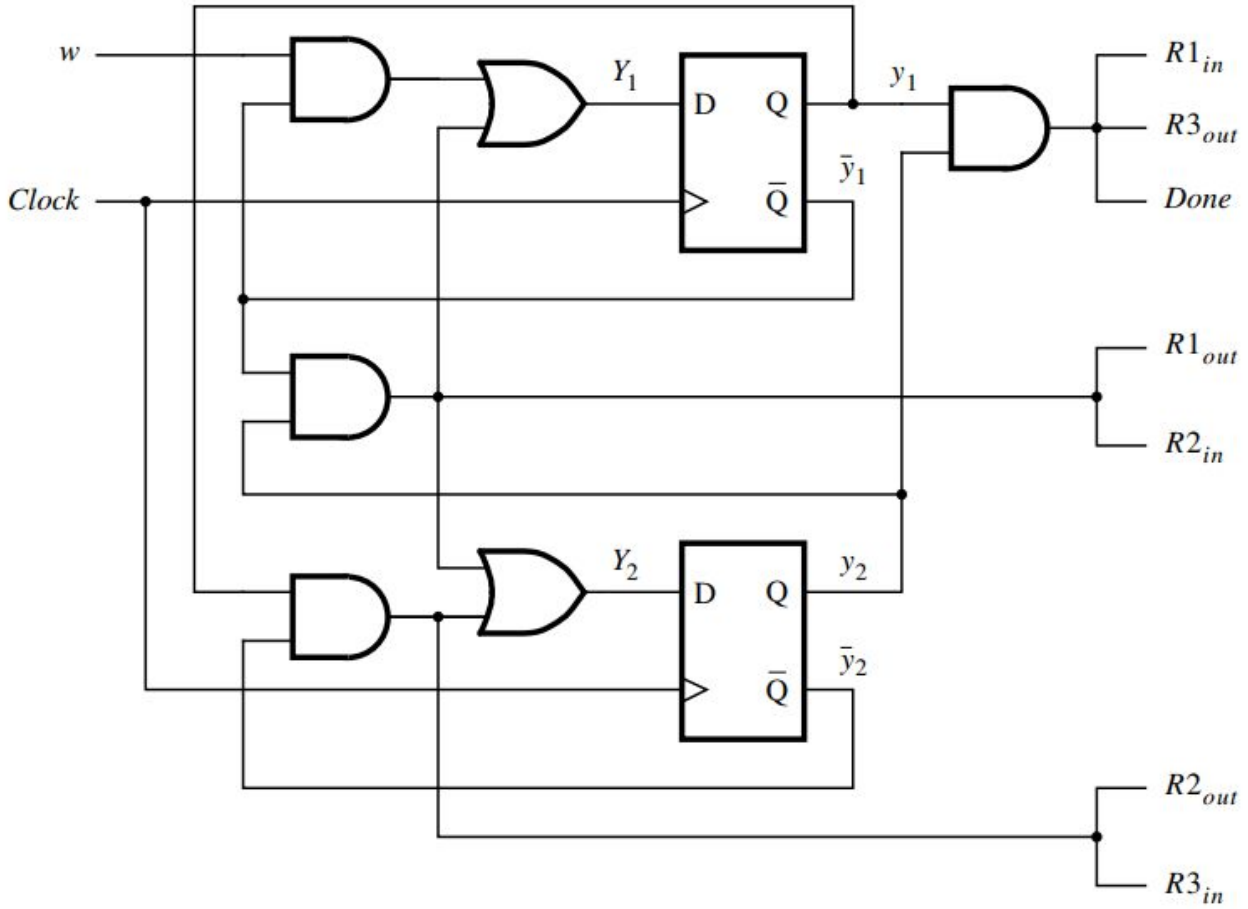
Note that, (Moore type)

- ➢ $Y = f(w, y_1, y_2)$
- ➢ outputs = $f(y_1, y_2)$

$$R1_{out} = R2_{in} = \bar{y}_1 y_2$$
$$R1_{in} = R3_{out} = Done = y_1 y_2$$
$$R2_{out} = R3_{in} = y_1 \bar{y}_2$$

How many flipflops are required? **Ans: 2**

Example-3: Swapping Contents of two registers



Steps->

- State diagram
- State table
- State assigned table
- K-map
- **Circuit**

Figure 8.15. Final implementation of sequential circuit in Figure 8.13.

Example-3: Swapping Contents of two registers

	Present state	Next state		Outputs						
		$w = 0$	$w = 1$							
	$y_4y_3y_2y_1$	$Y_4Y_3Y_2Y_1$	$Y_4Y_3Y_2Y_1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	$Done$
A	0001	0001	0010	0	0	0	0	0	0	0
B	0010	0100	0100	0	0	1	0	0	1	0
C	0100	1000	1000	1	0	0	1	0	0	0
D	1000	0001	0001	0	1	0	0	1	0	1

Steps->

- State diagram
- State table
- **State assigned table (One-hot encoding)**
- ~~K-map~~
- Circuit

$$R1_{out} = R2_{in} = y_3$$
$$R1_{in} = R3_{out} = Done = y_4$$
$$R2_{out} = R3_{in} = y_2$$

$$Y_1 = \overline{w}y_1 + y_4$$
$$Y_2 = wy_1$$
$$Y_3 = y_2$$
$$Y_4 = y_3$$

How many flipflops are required? **Ans: 4**

Example-4: Serial Adder

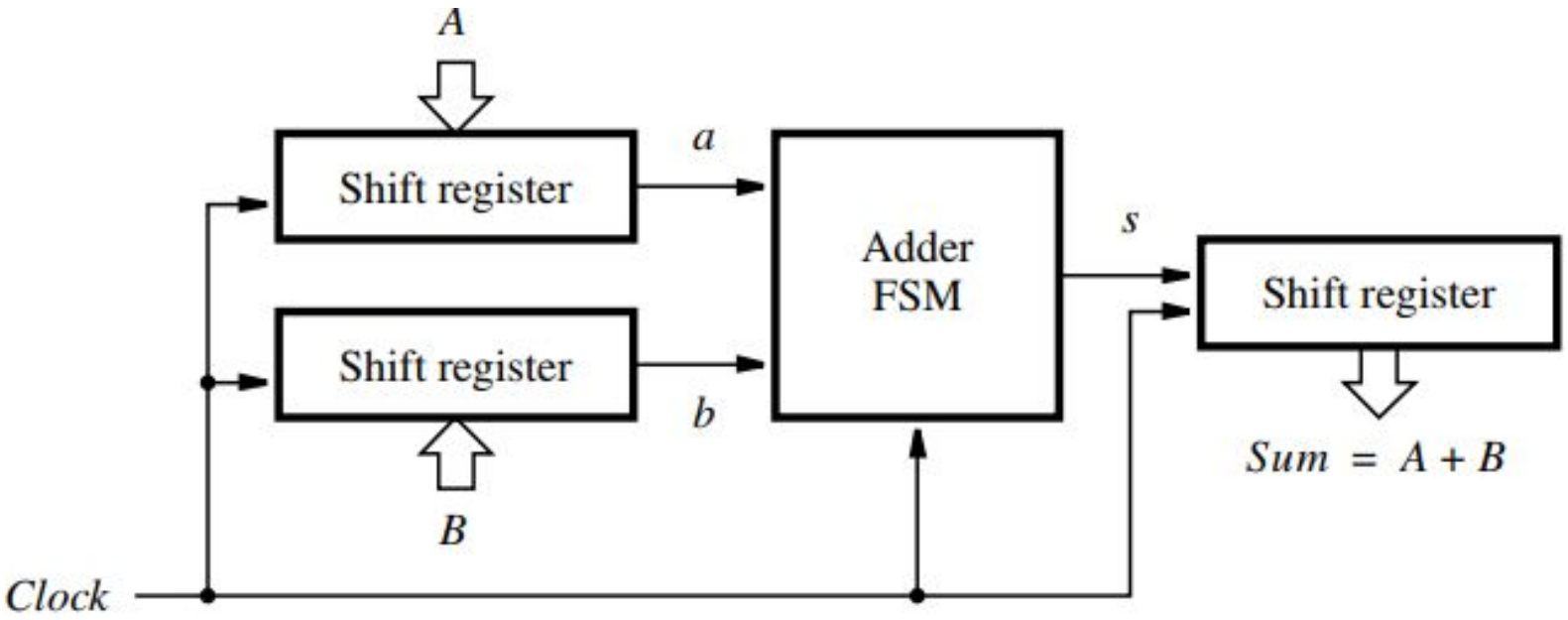
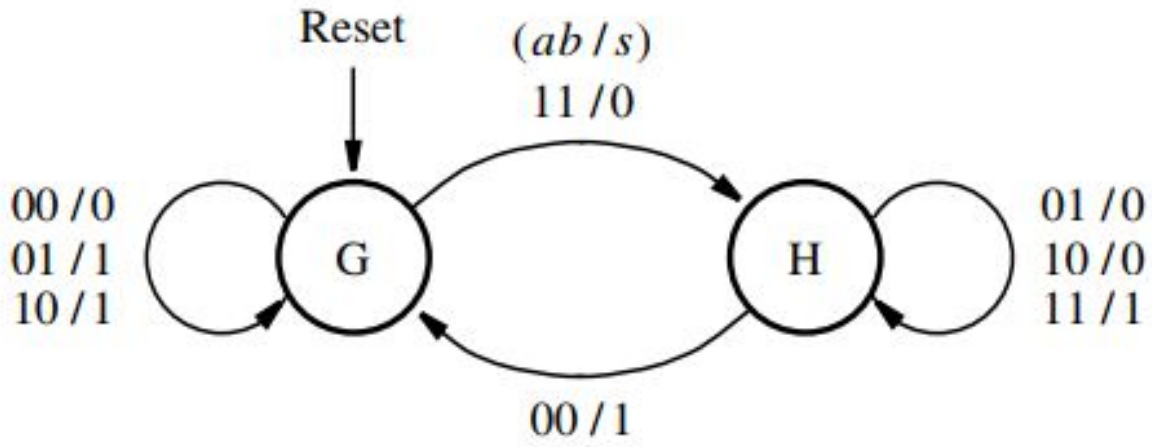


Figure 6.39 Block diagram for the serial adder.

Example-4: Serial Adder (Mealy Type)



G: carry-in = 0
H: carry-in = 1

Figure 6.40 State diagram for the serial adder FSM.

Example-4: Serial Adder (Mealy Type)

Present state	Next state				Output s			
	$ab = 00$	01	10	11	00	01	10	11
G	G	G	G	H	0	1	1	0
H	G	H	H	H	1	0	0	1

Figure 6.41 State table for the serial adder FSM.

$$Y = ab + ay + by$$
$$s = a \oplus b \oplus y$$

Present state	Next state				Output			
	$ab = 00$	01	10	11	00	01	10	11
y	Y				s			
0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

Figure 6.42 State-assigned table for Figure 6.41.

Example-4: Serial Adder (Mealy Type)

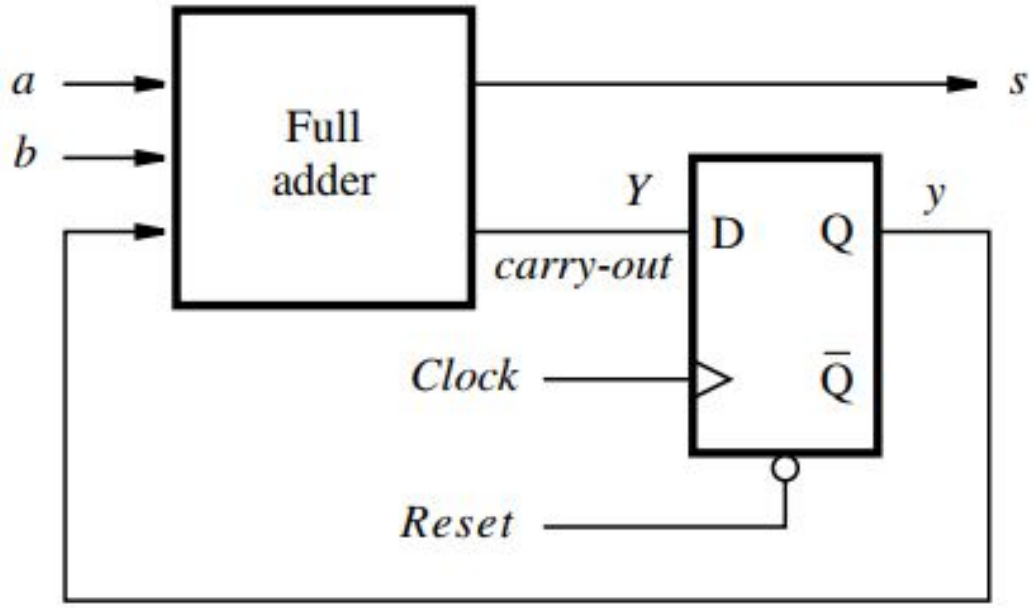
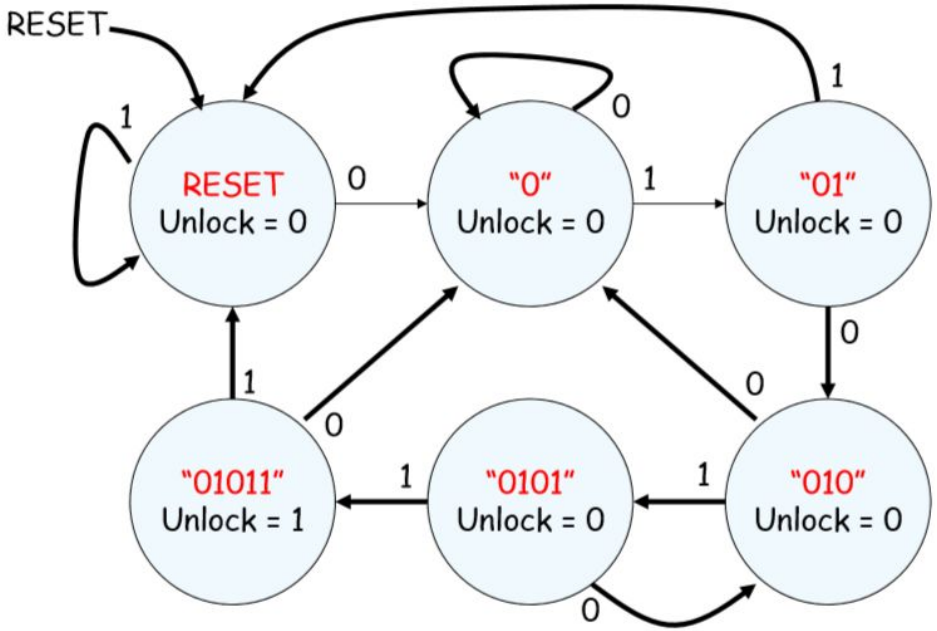


Figure 6.43 Circuit for the adder FSM in Figure 6.39.

More Examples-

- Electronic Lock: The combination- 01011



- 3 bit binary counter (Modulo-8 counter)