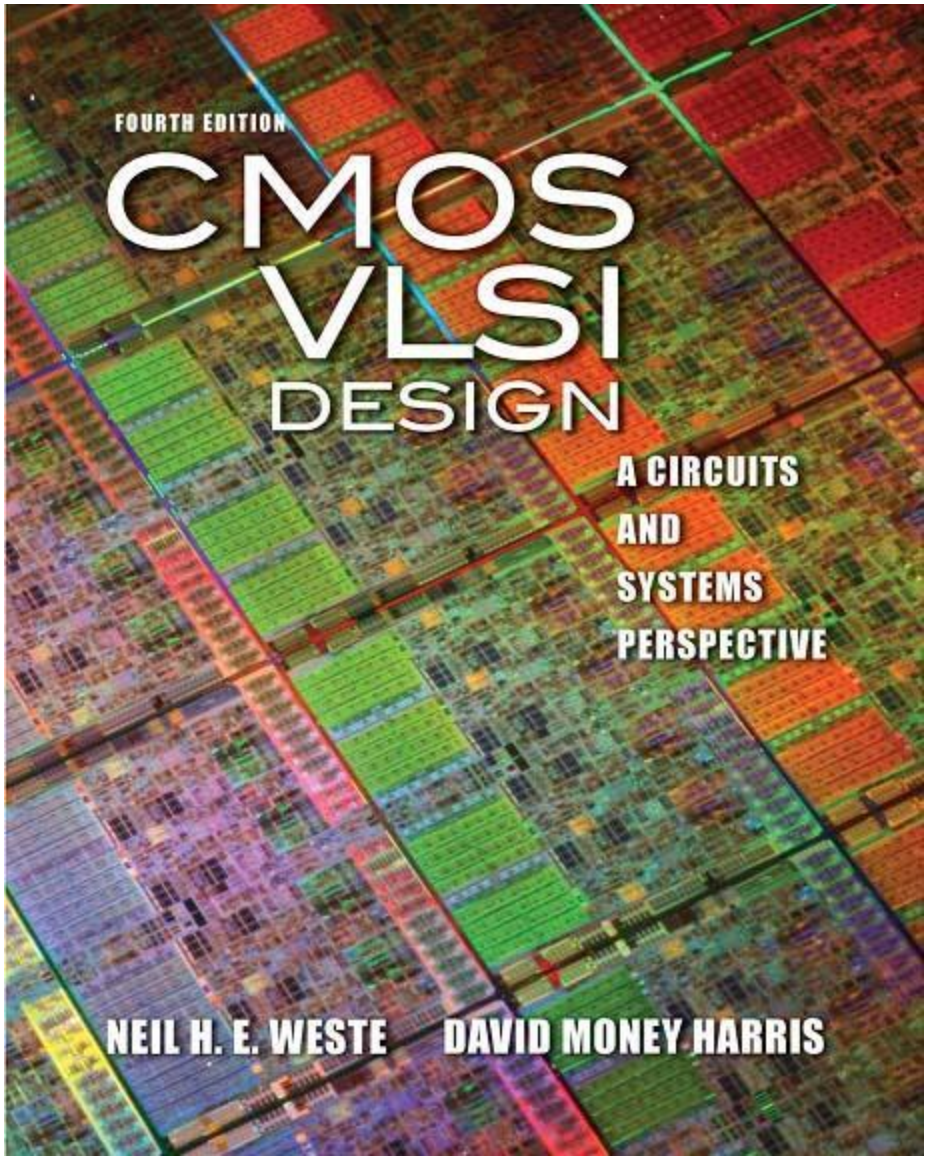
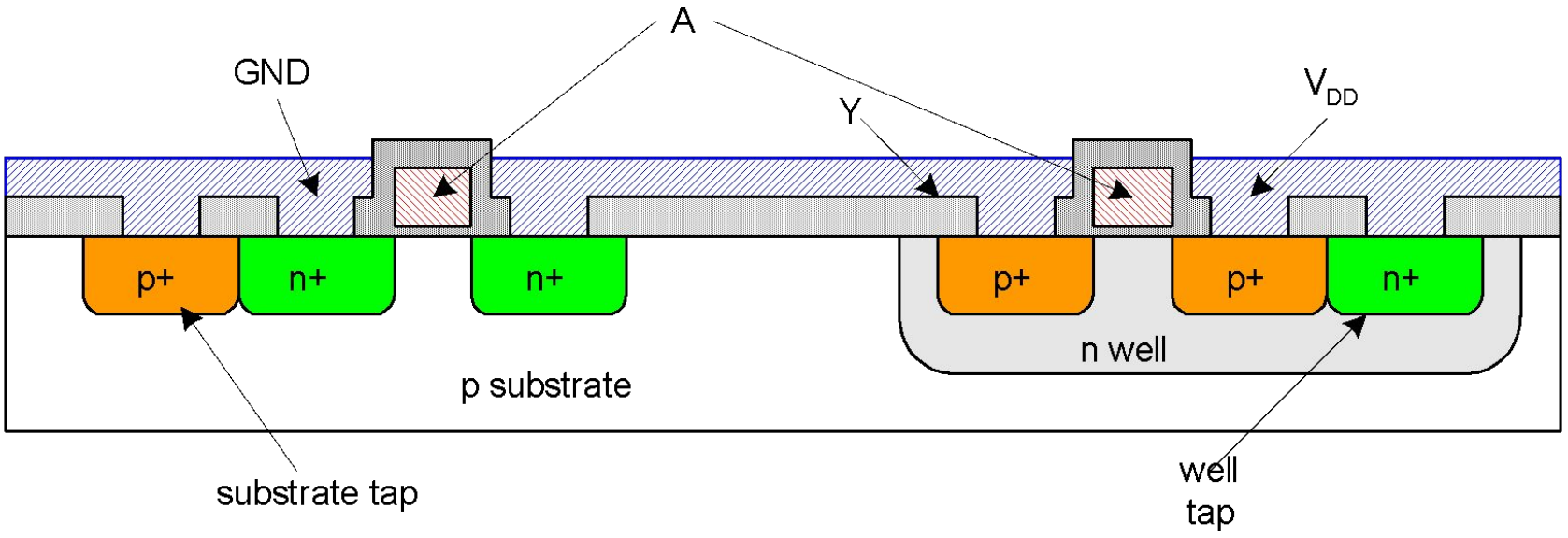


Lecture 12: Layout & Stick Diagrams

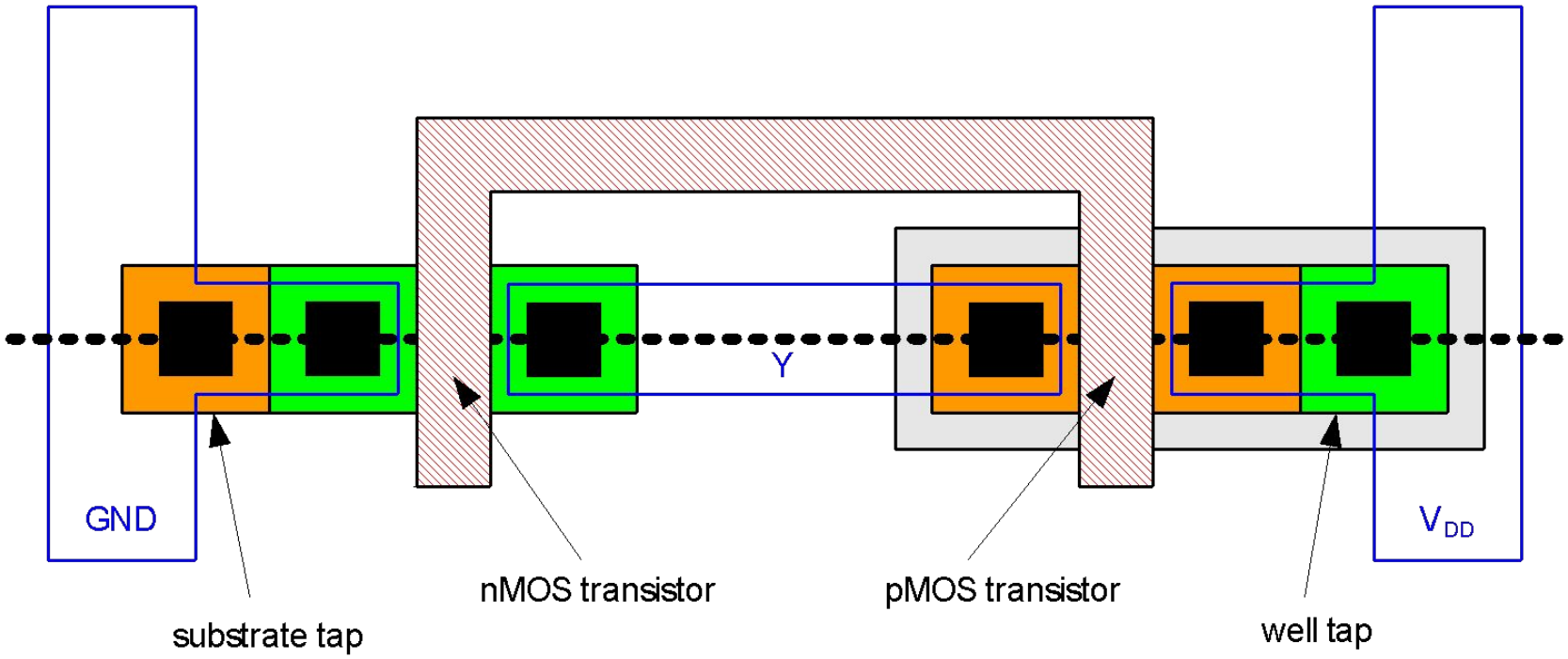
Inverter Cross-section

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps

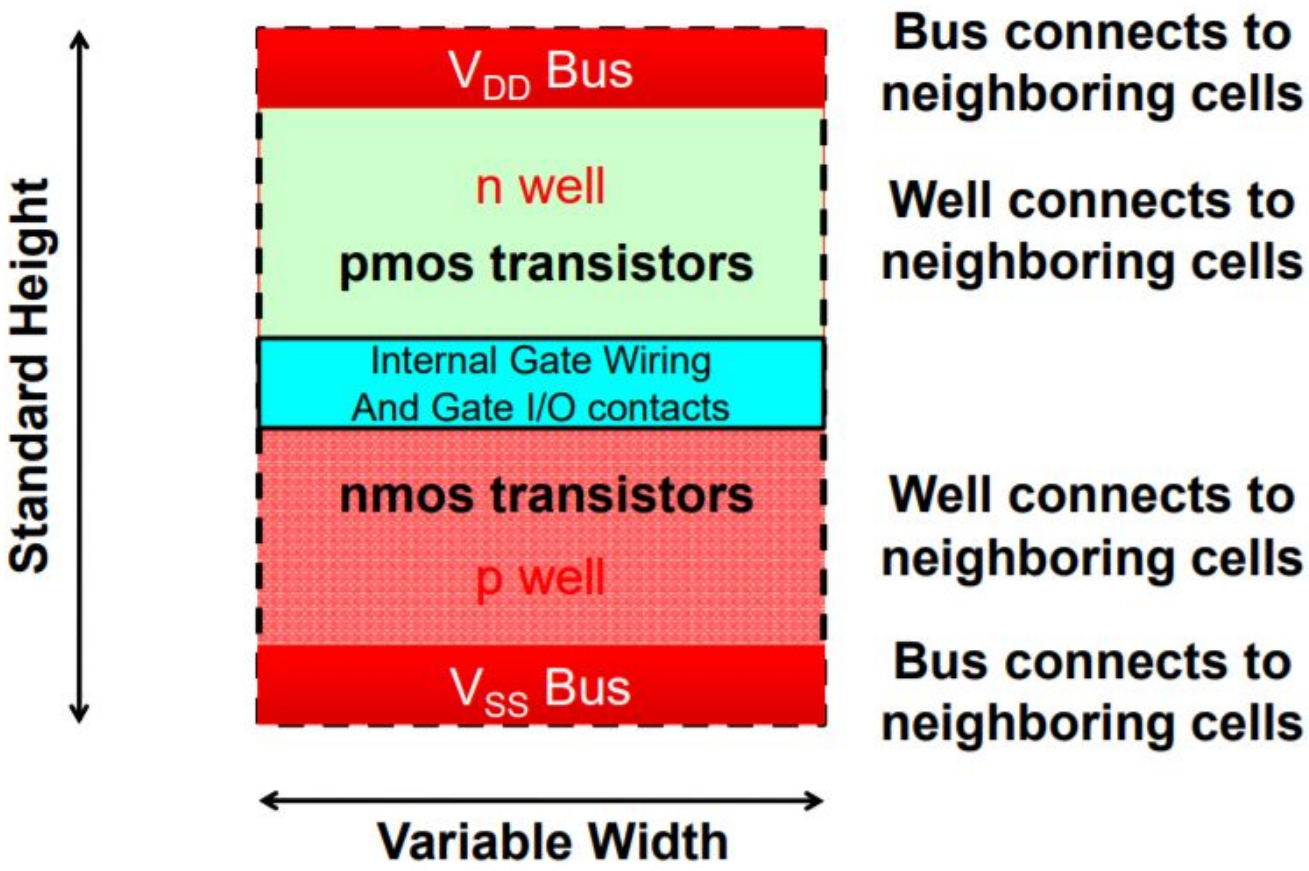


Inverter Top View

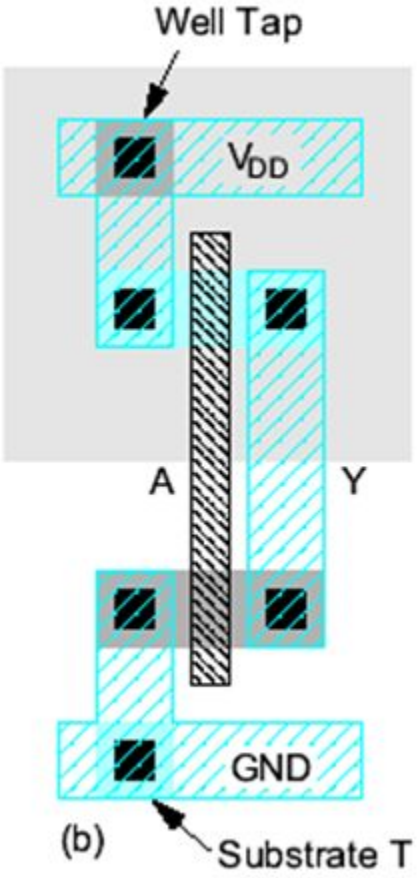
- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Standard Cell Layout



Example: Inverter



Gate Layout

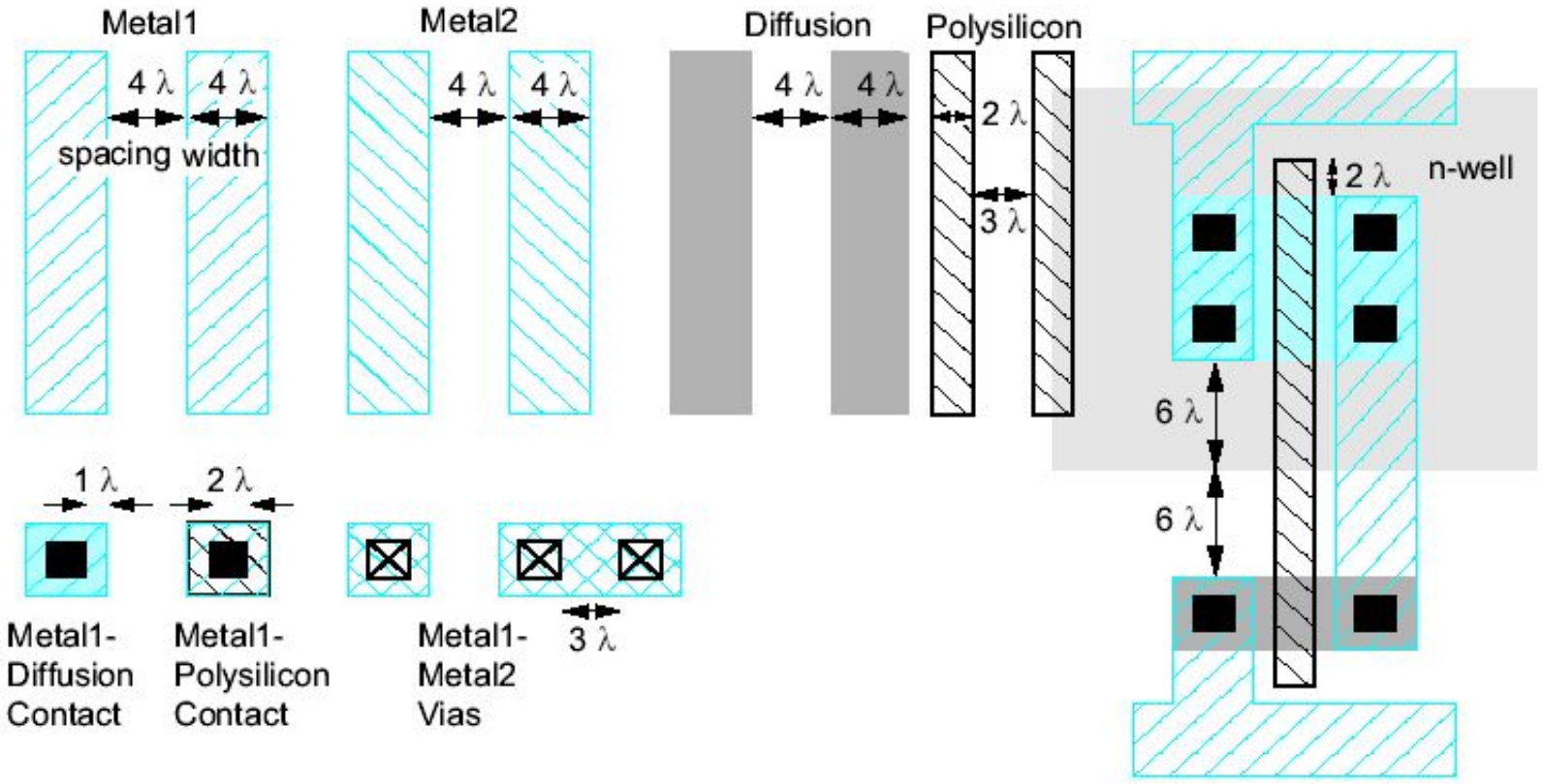
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should be about standard height
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

Simplified Design Rules

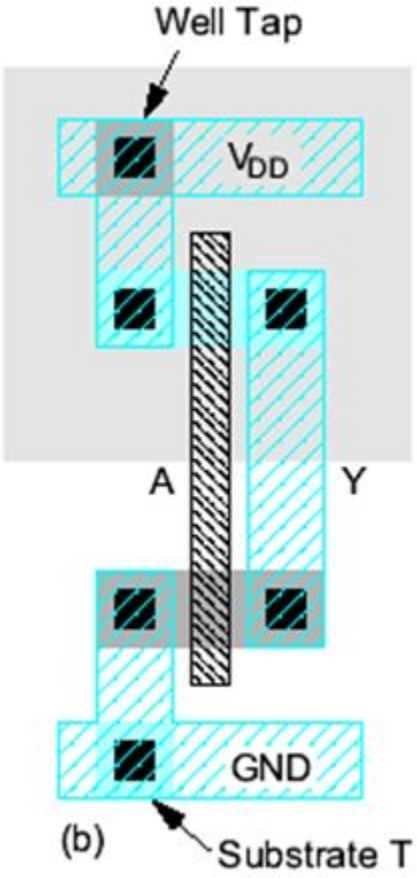
- Conservative rules to get you started



Source and Drain

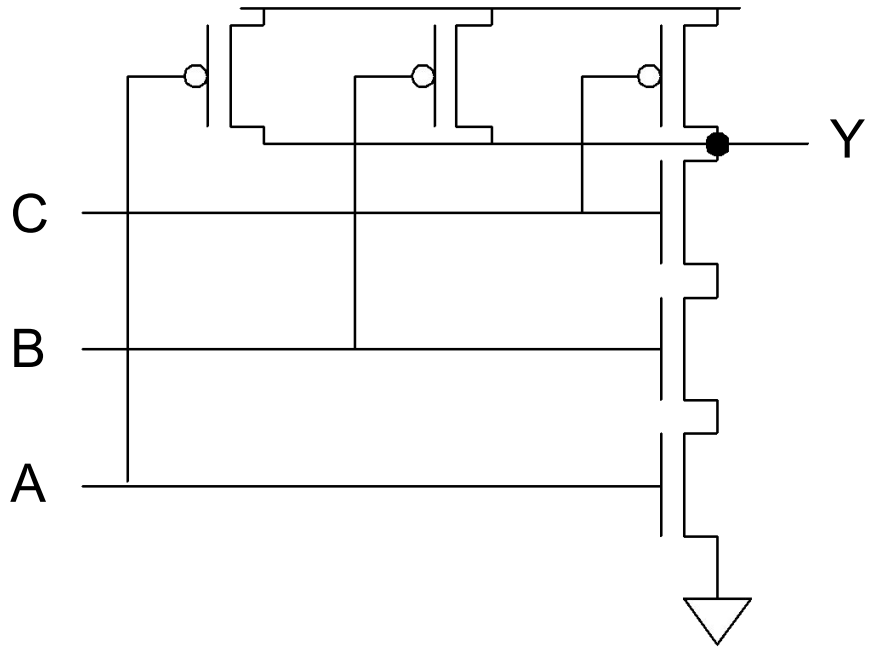
- We will follow the convention: current always flows from top to bottom in an electronic circuit
  - For pMOS transistor:
    - Carrier: holes (+)
    - Top node: Source
    - Bottom node: Drain
  - For nMOS transistor:
    - Carrier: electrons (-)
    - Top node: Drain
    - Bottom node: Source

Example: Inverter

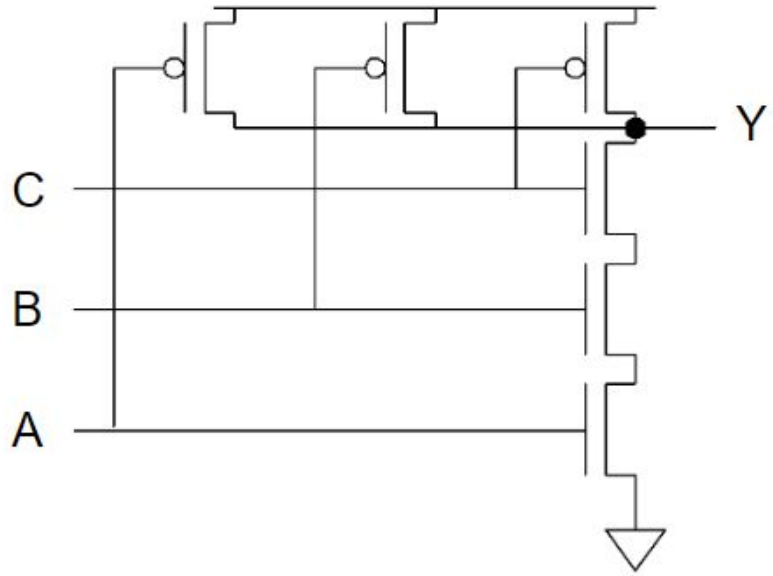


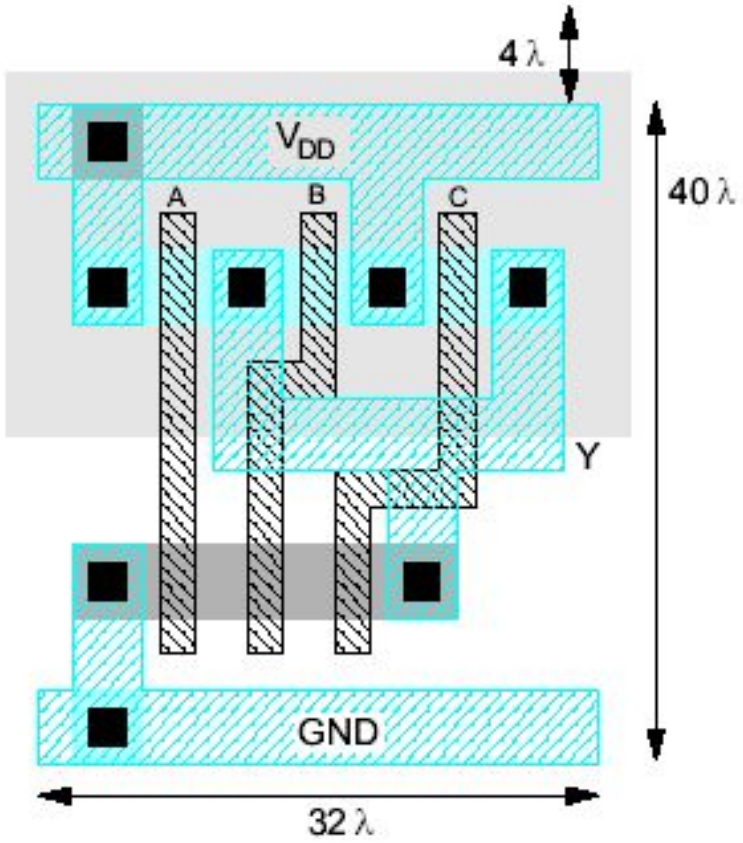
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



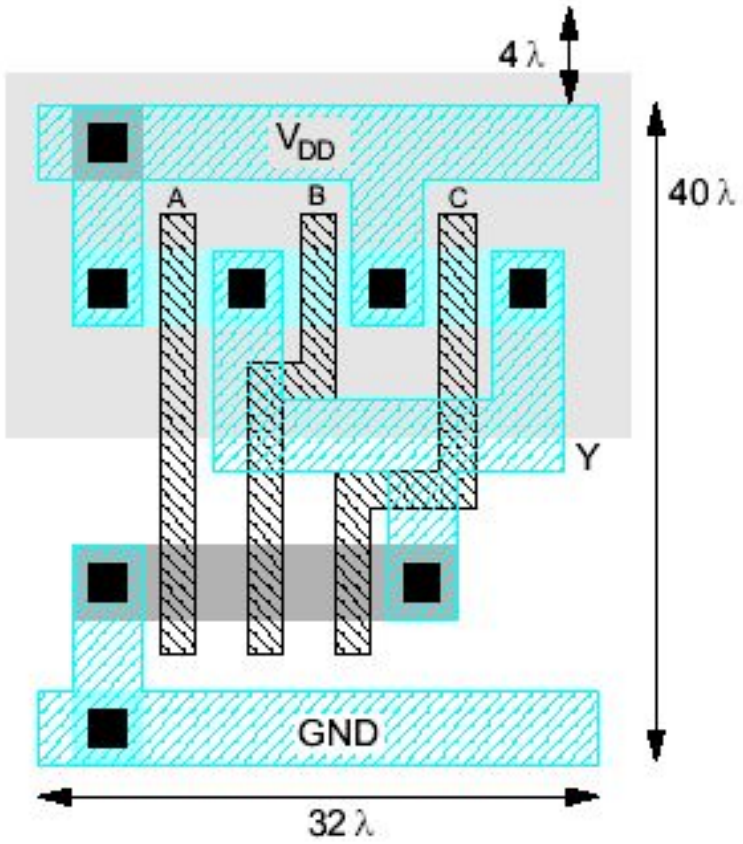
Example: NAND3



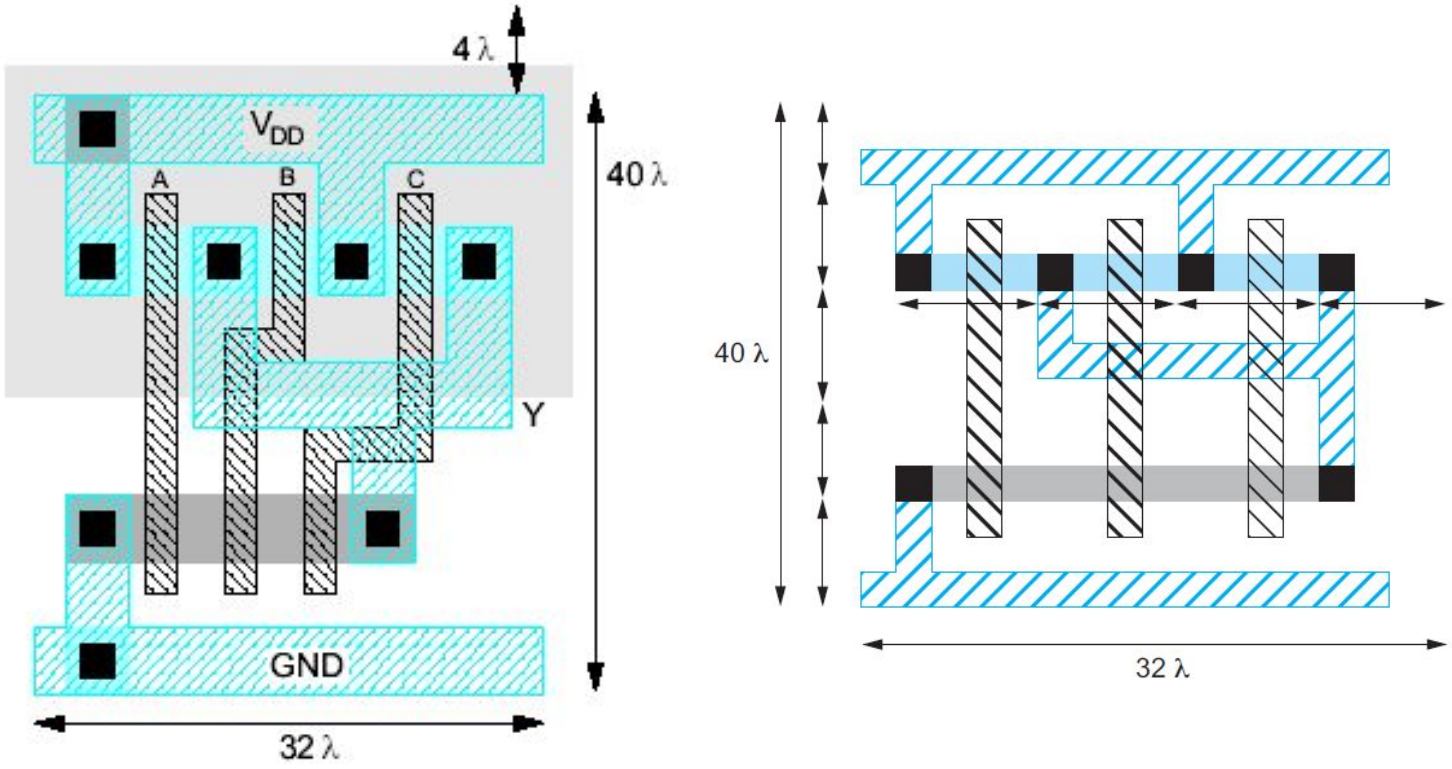


Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ

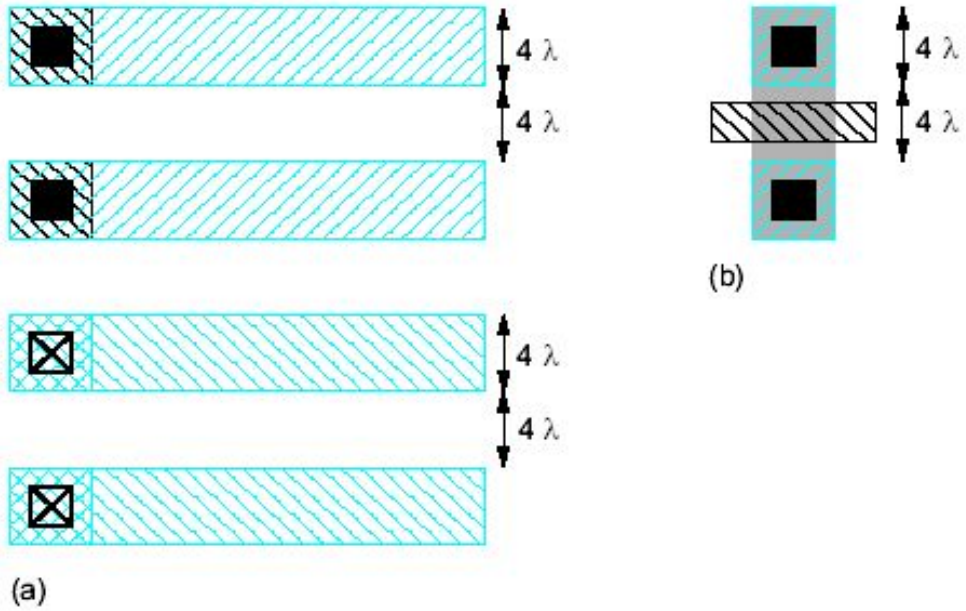


Example: NAND3



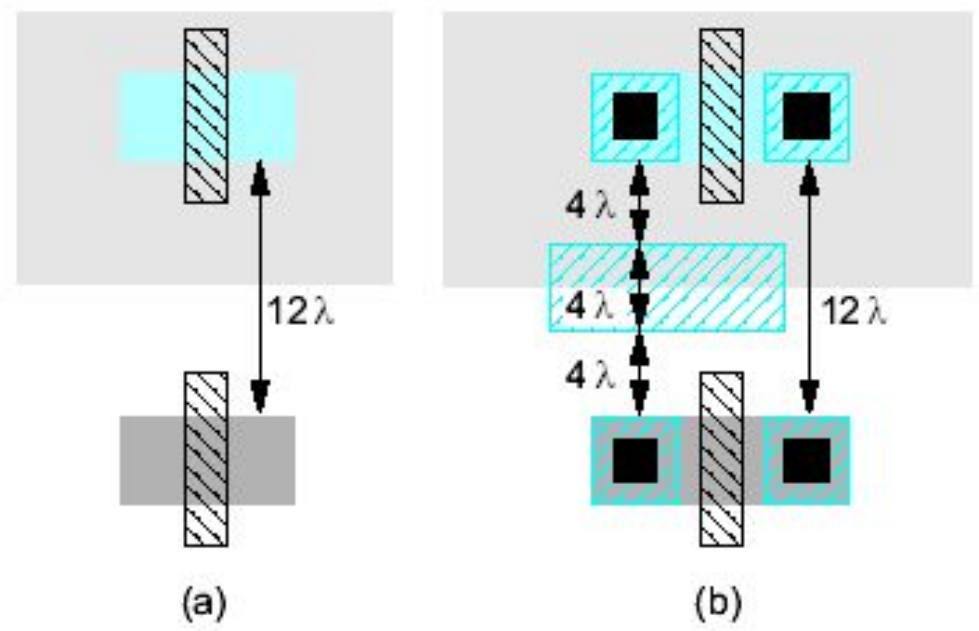
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



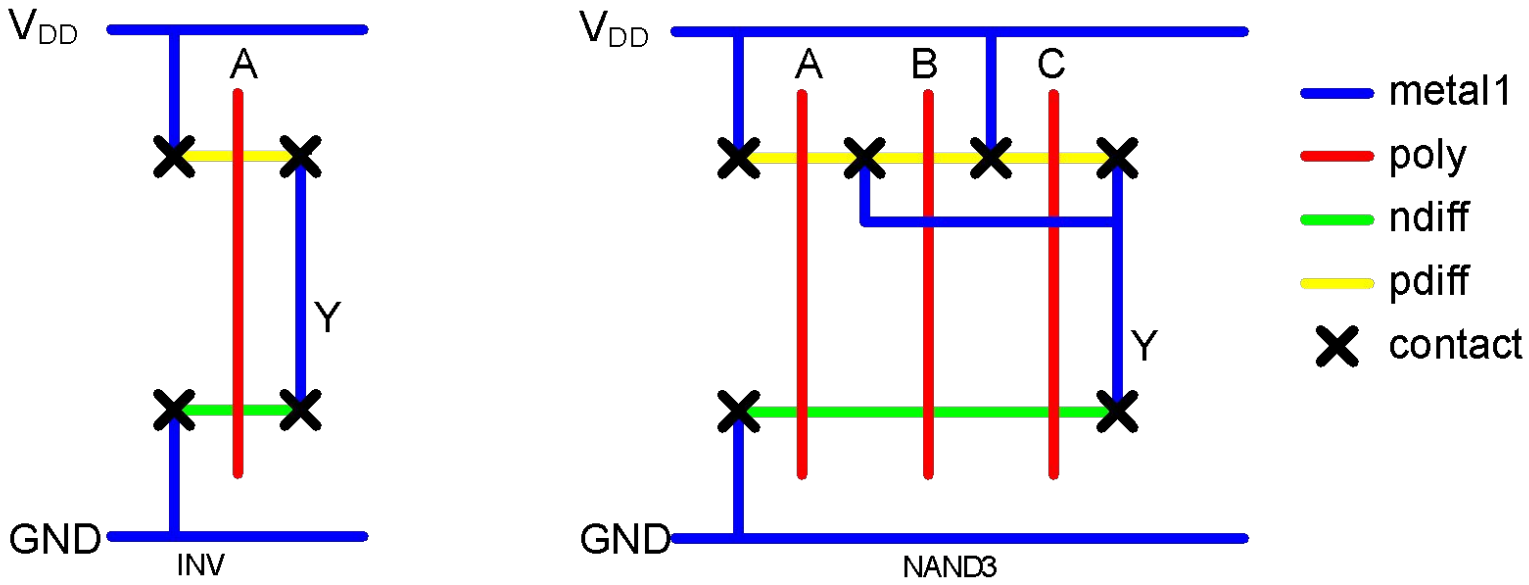
Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

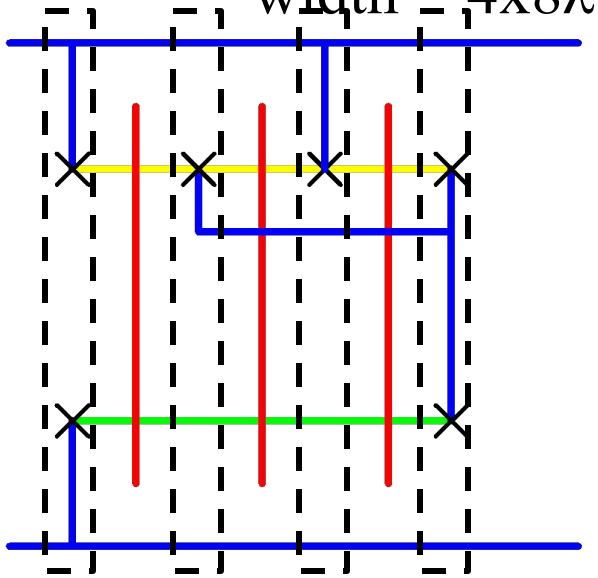


Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ

Parallel tracks along the width = 4 metals

width ≡ 4x8λ = 32 λ

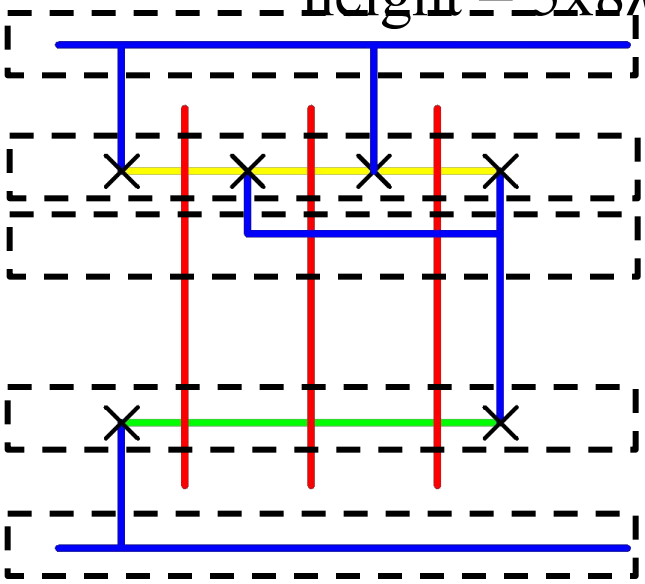


Area Estimation

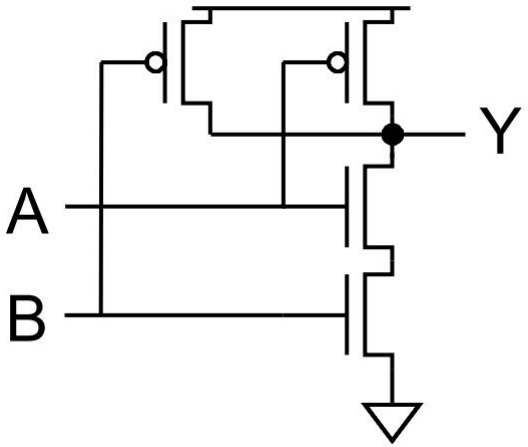
- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ

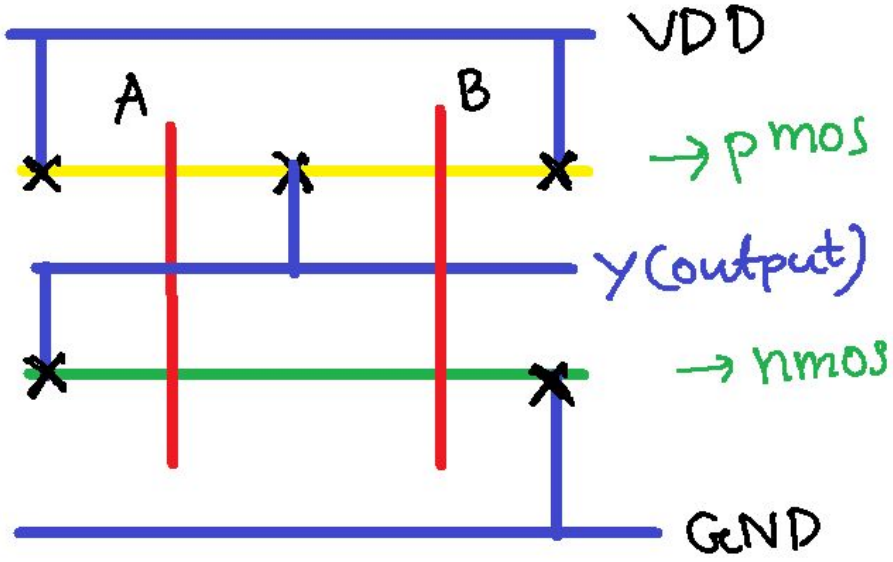
Parallel tracks along the height = 3 metals + 2 diff

height = 5x8λ = 40 λ



$Y = \overline{AB}$ (2 NAND)

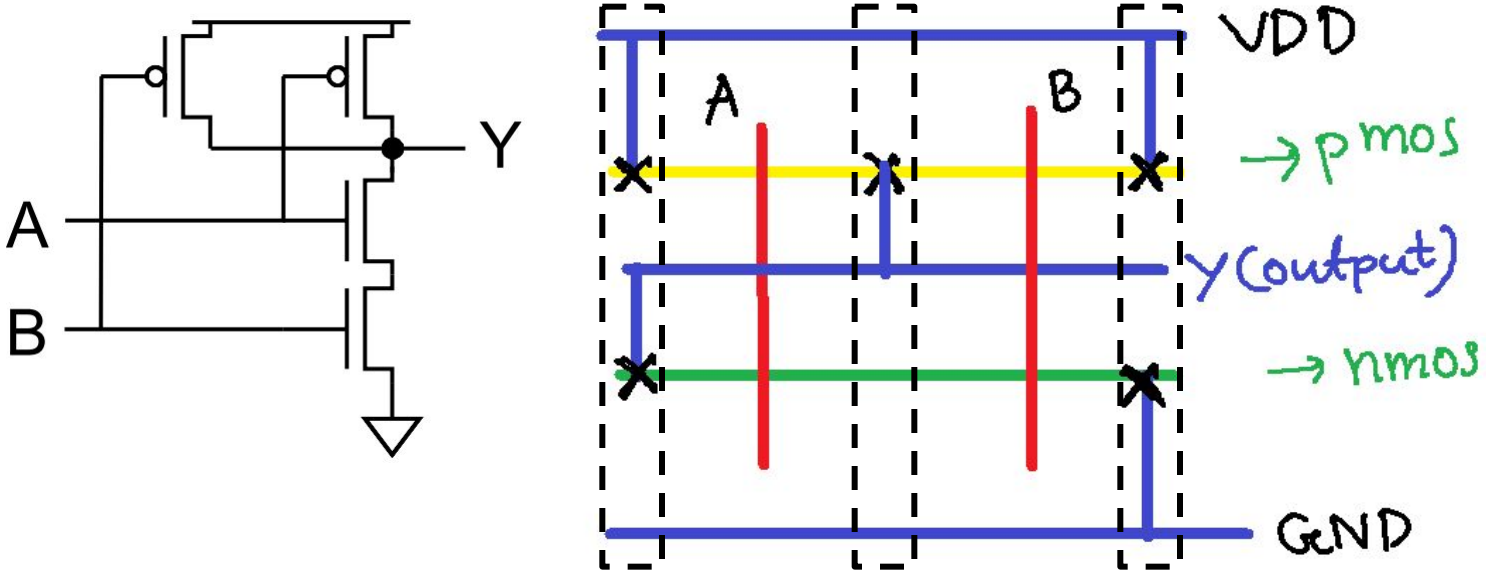




$Y = \overline{AB}$ (2 NAND)

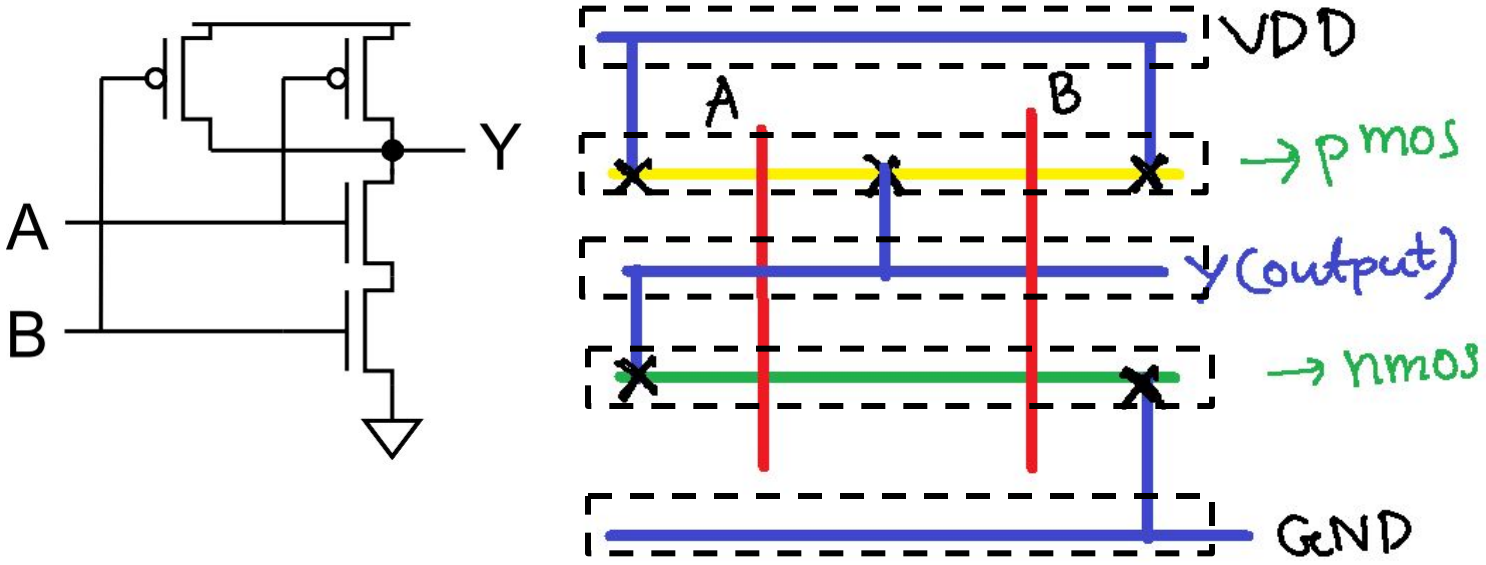
Parallel tracks along the width = 3 metals

width = 3x8λ = 24 λ

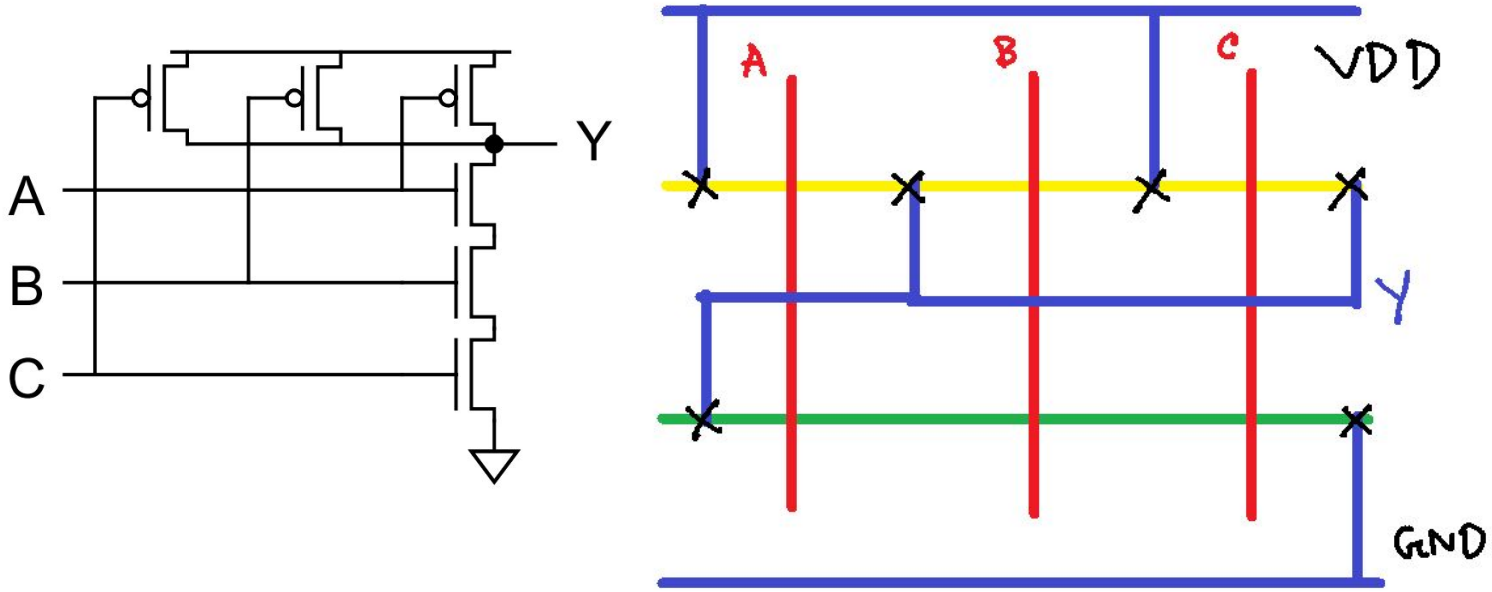


$Y = \overline{AB}\ (2\ NAND)$

Parallel tracks along the height = 3 metals + 2 diff
height = 5x8λ = 40 λ



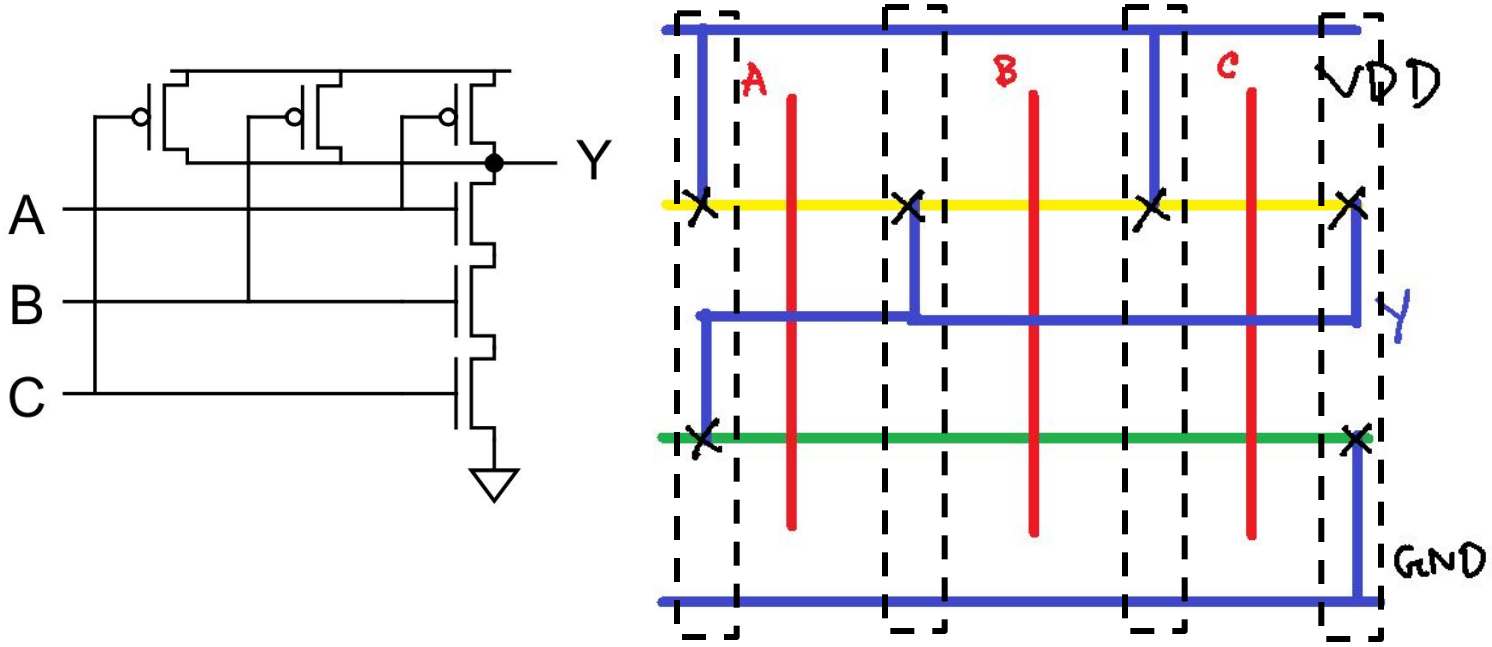
$Y = \overline{ABC}$ (3 NAND)



$Y = \overline{ABC}$ (3 NAND)

Parallel tracks along the width = 4 metals

width = 4x8λ = 32 λ



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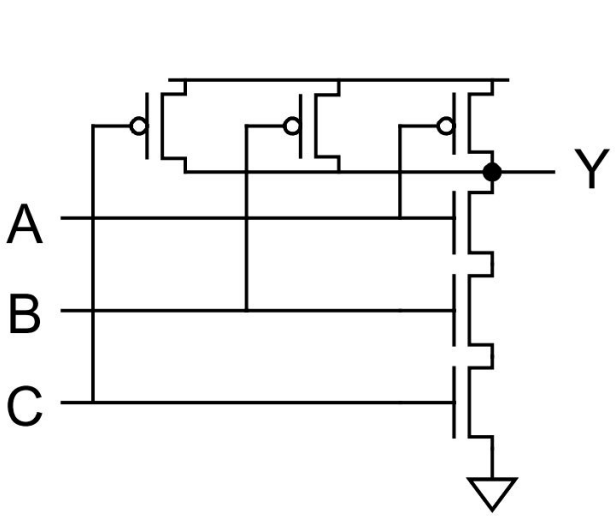
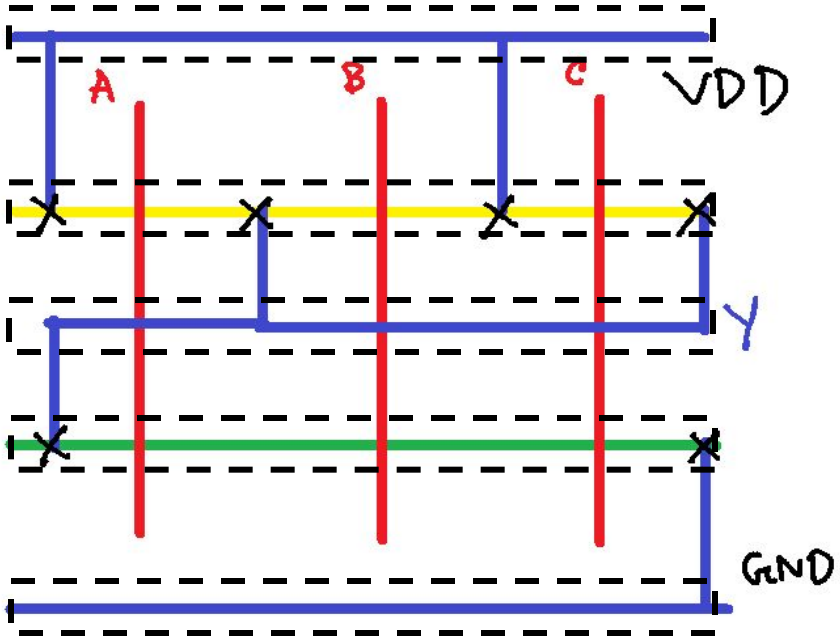
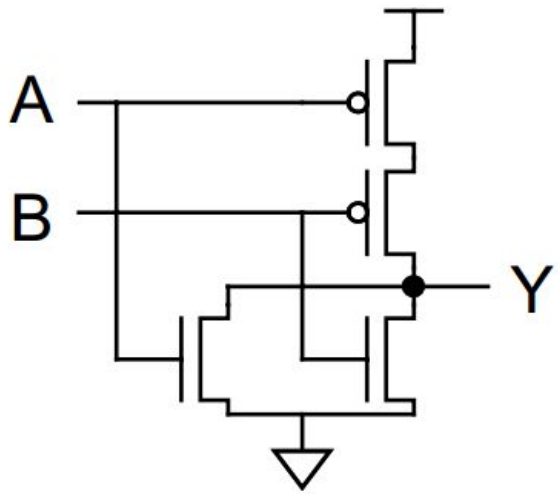
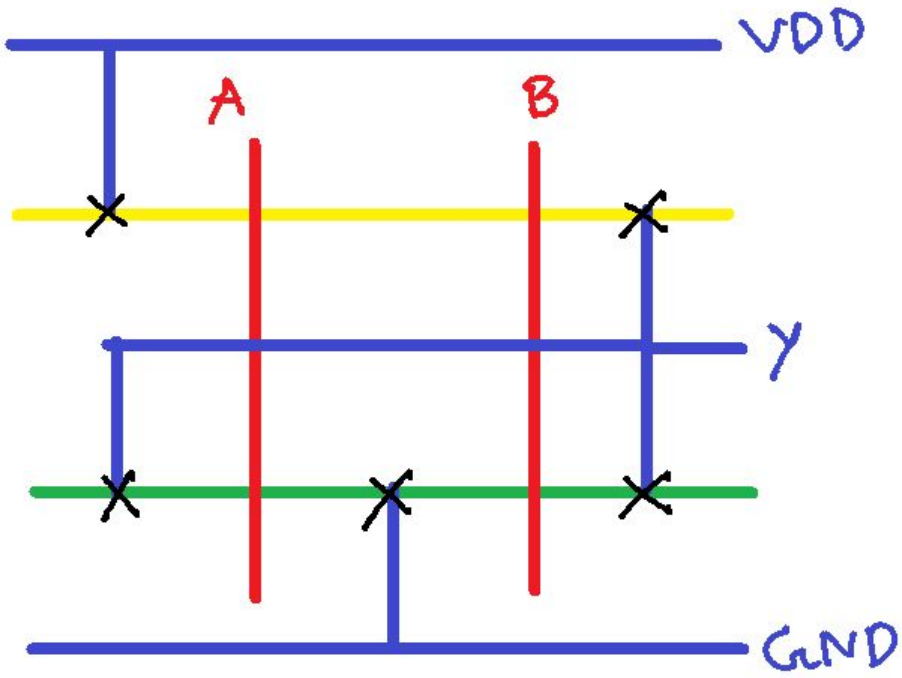




$$Y = \overline{A + B}\ (2\ NOR)$$

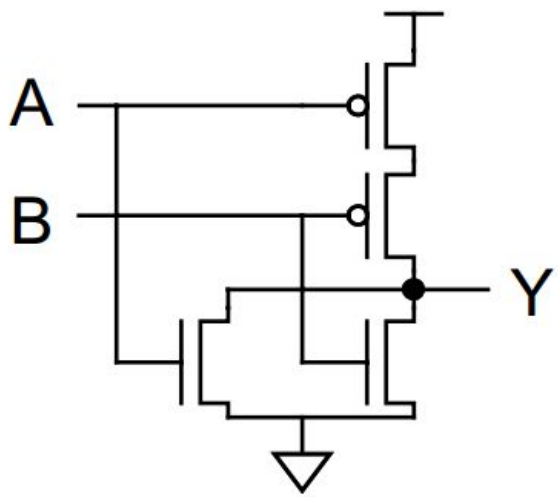


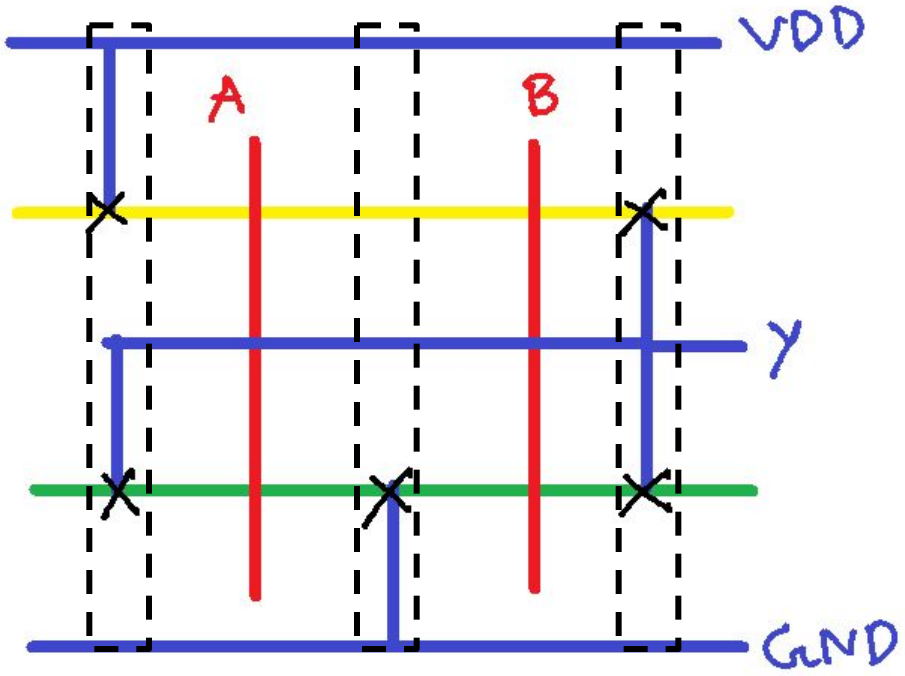


$$Y = \overline{A + B}\ (2\ NOR)$$

Parallel tracks along the width = 3 metals

width = 3x8λ = 24 λ

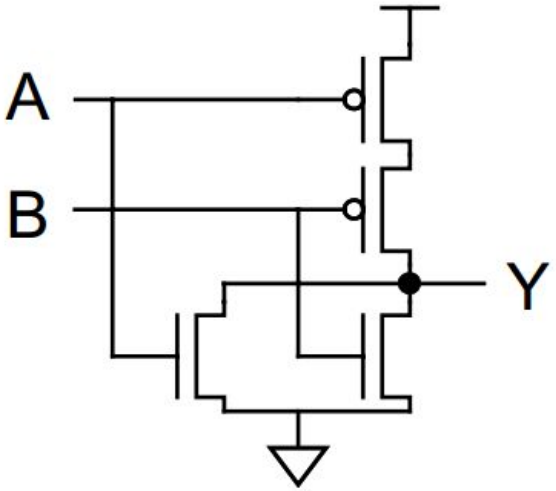


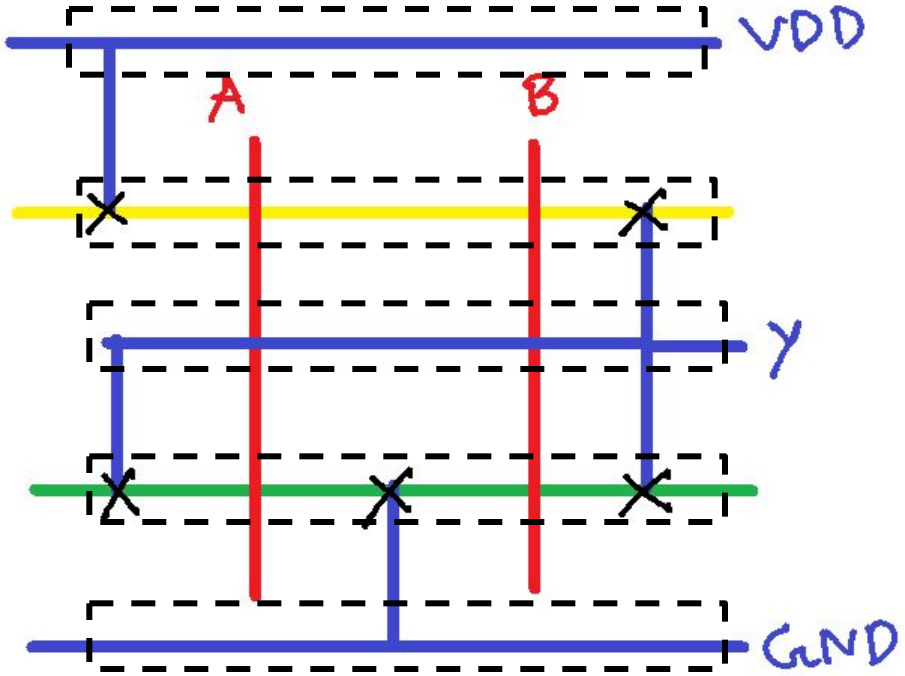


$$Y = \overline{A + B}\ (2\ NOR)$$

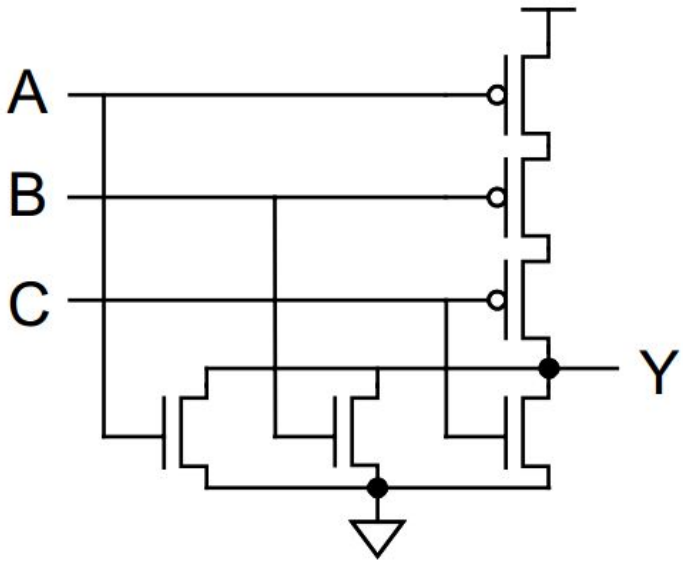
Parallel tracks along the height = 3 metals + 2 diff

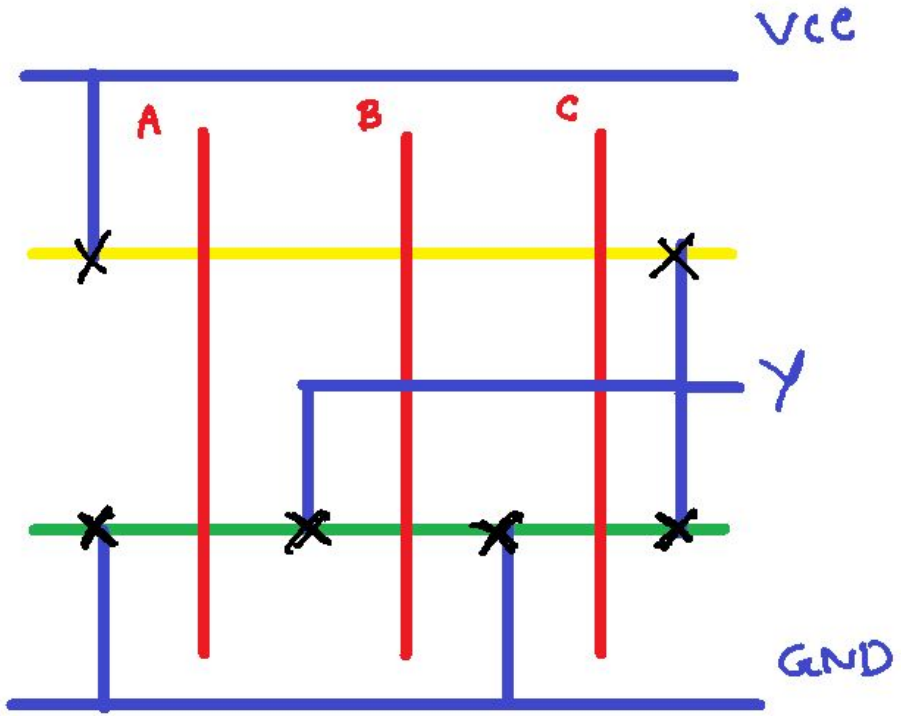
width = 5x8λ = 40 λ





$$Y = \overline{A + B + C}\ (3\ NOR)$$

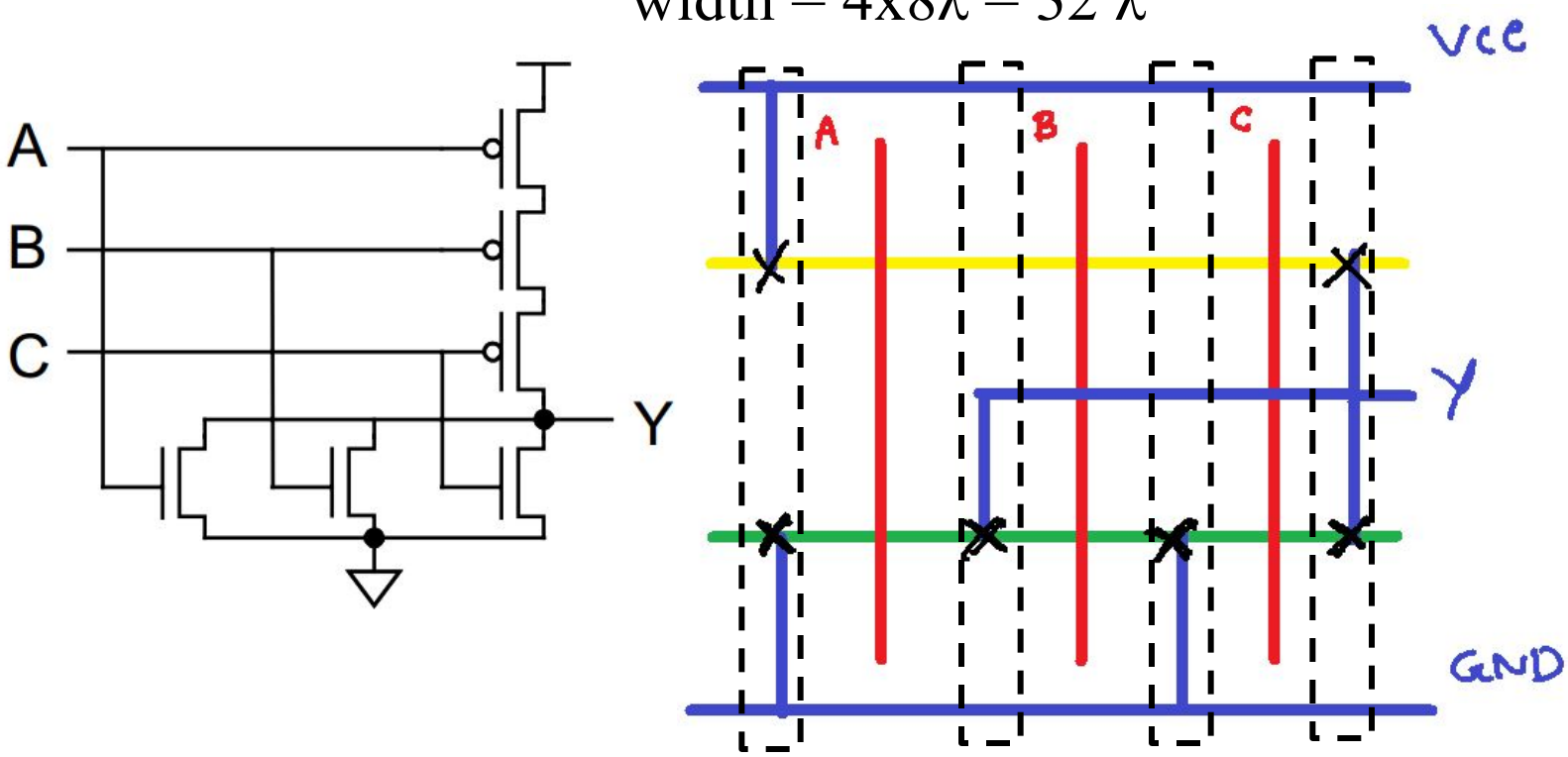




$$Y = \overline{A + B + C}\ (3\ NOR)$$

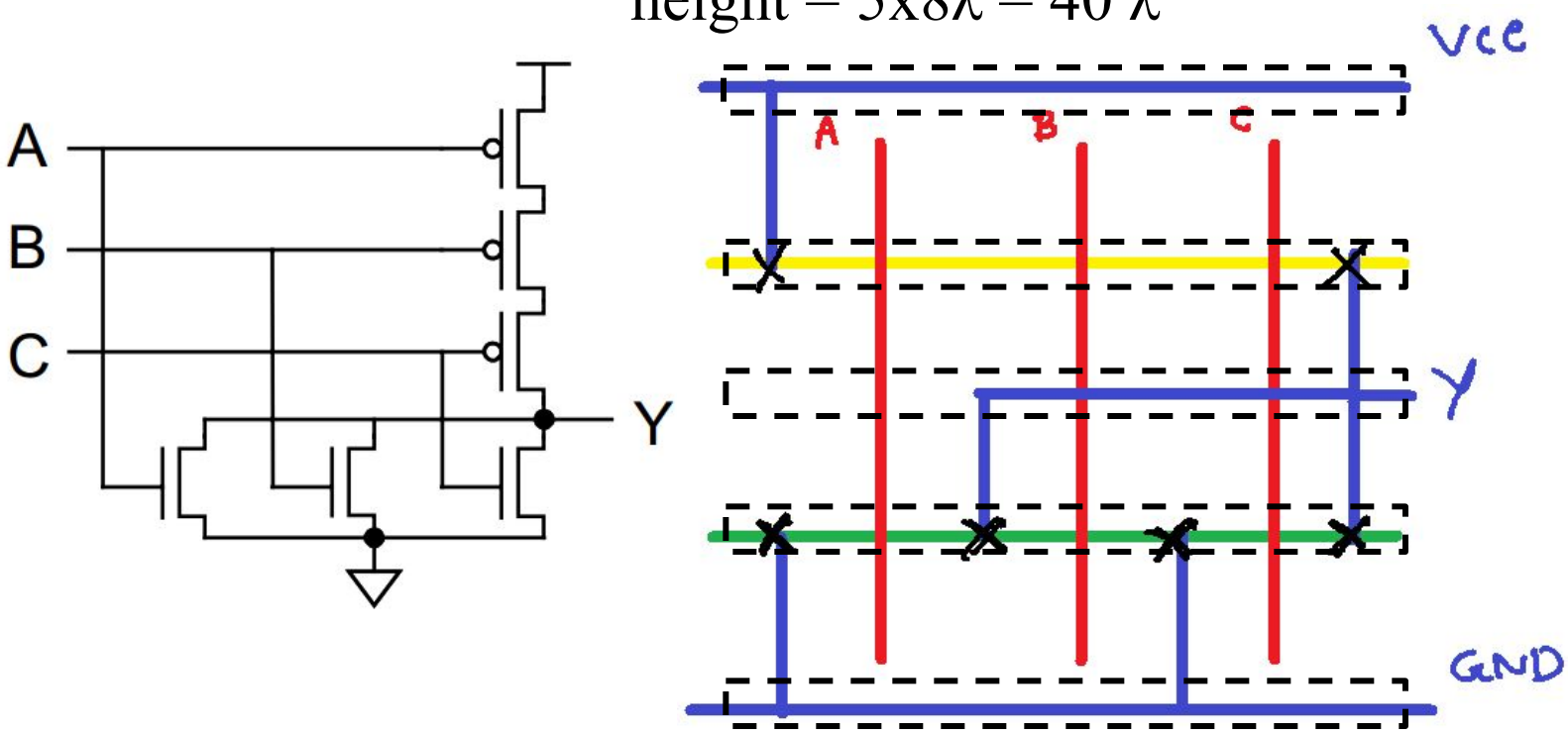
Parallel tracks along the width = 4 metals

width = 4x8λ = 32 λ

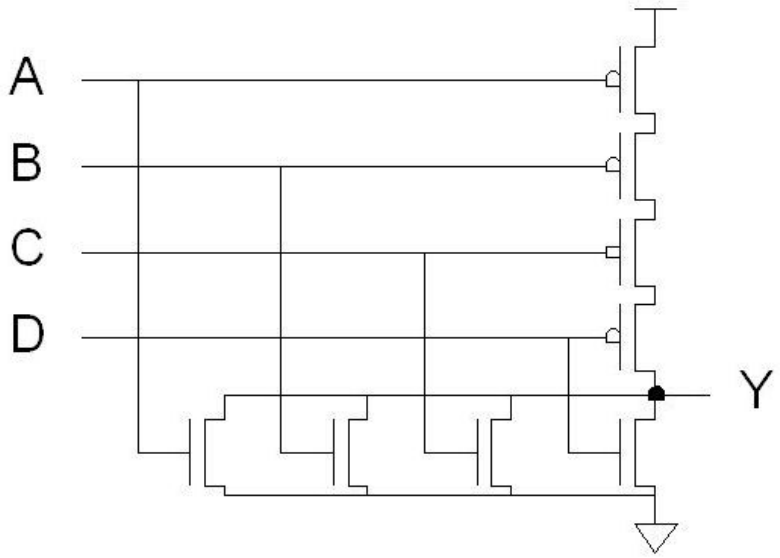


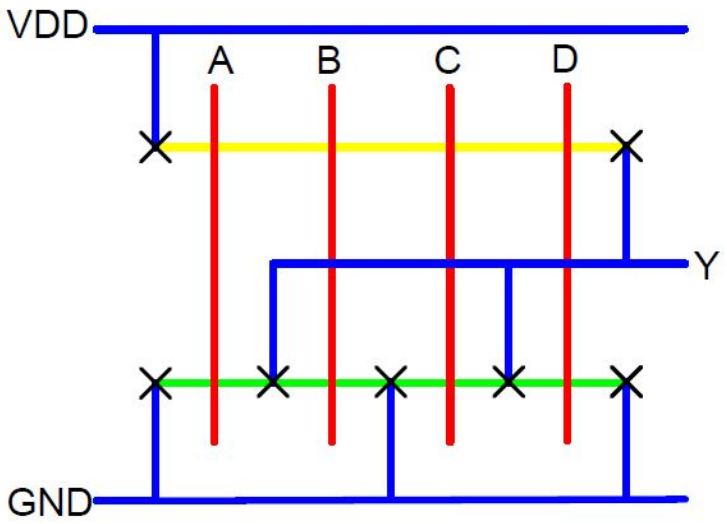
$$Y = \overline{A + B + C}\ (3\ NOR)$$

Parallel tracks along the height = 3 metals + 2 diff
height = 5x8λ = 40 λ



$$Y = \overline{A + B + C + D} \; (4\,NOR)$$

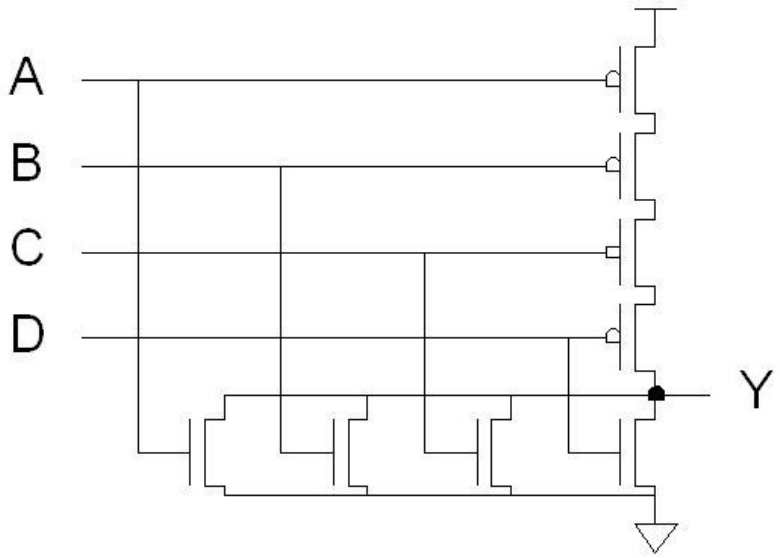


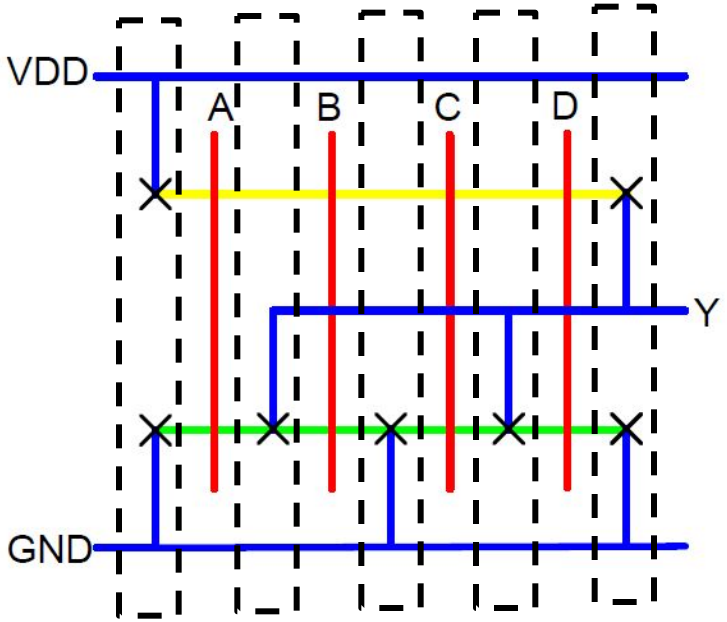


$$Y = \overline{A + B + C + D}\ (4\ NOR)$$

Parallel tracks along the width = 5 metals

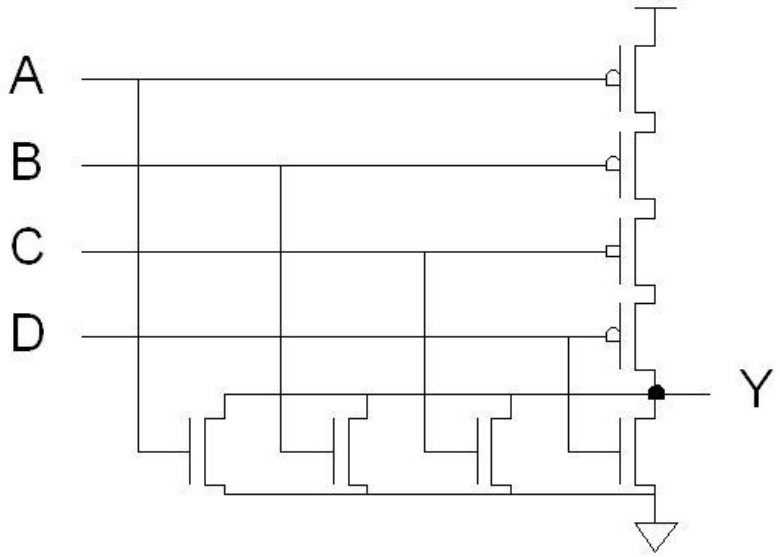
width = 5x8λ = 40 λ

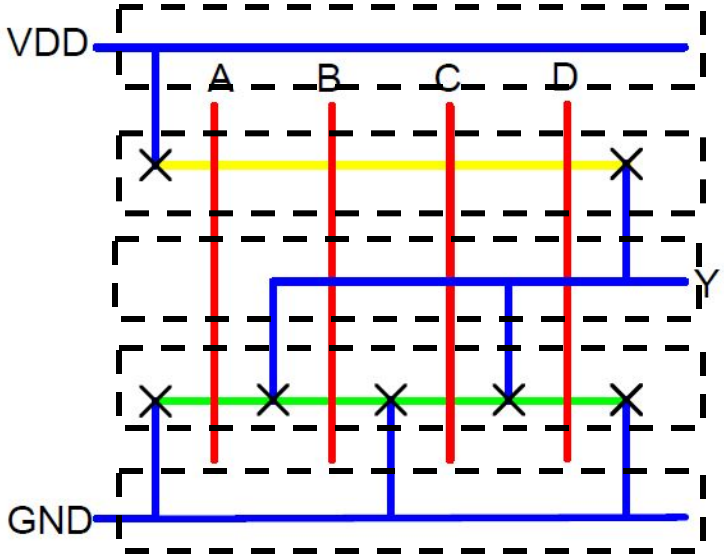




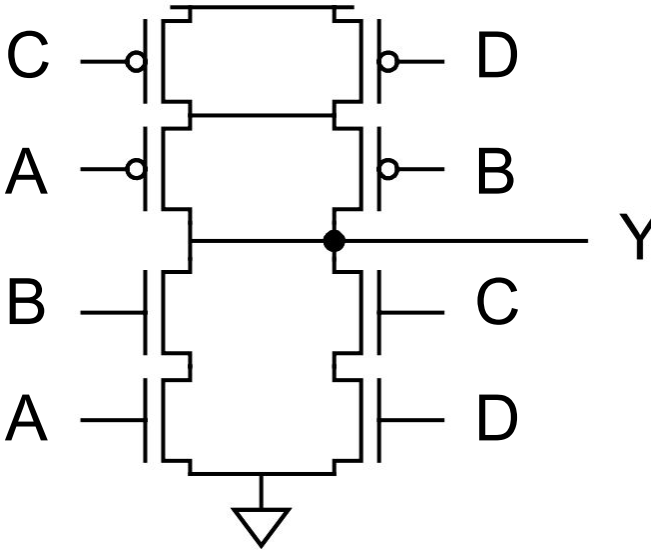
$$Y = \overline{A + B + C + D}\ (4\ NOR)$$

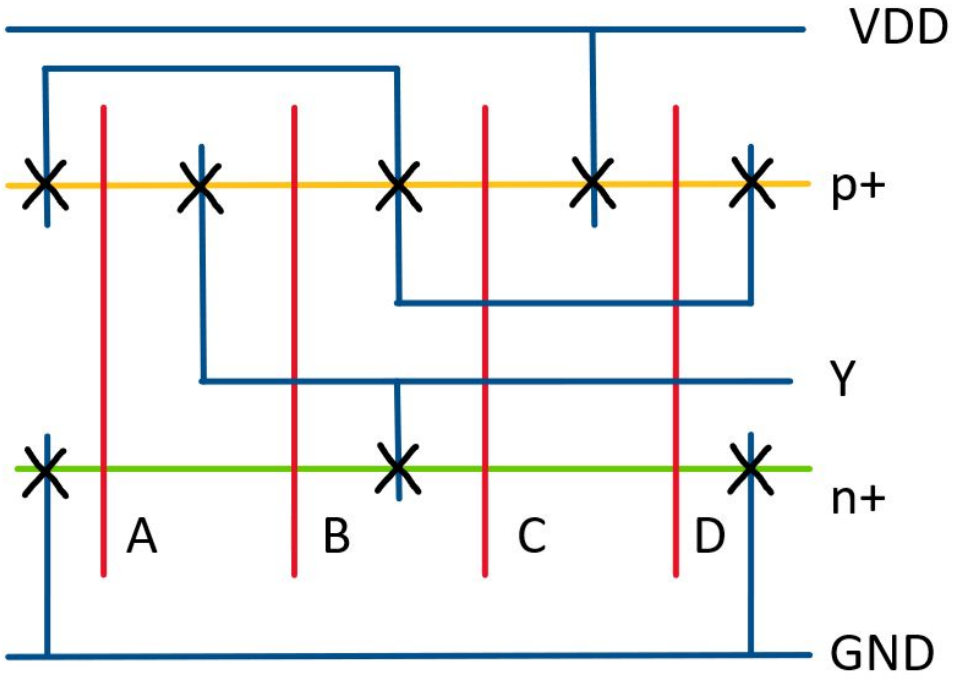
Parallel tracks along the height = 3 metals + 2 diff
height = 5x8λ = 40 λ





$$Y = \overline{AB + CD}$$

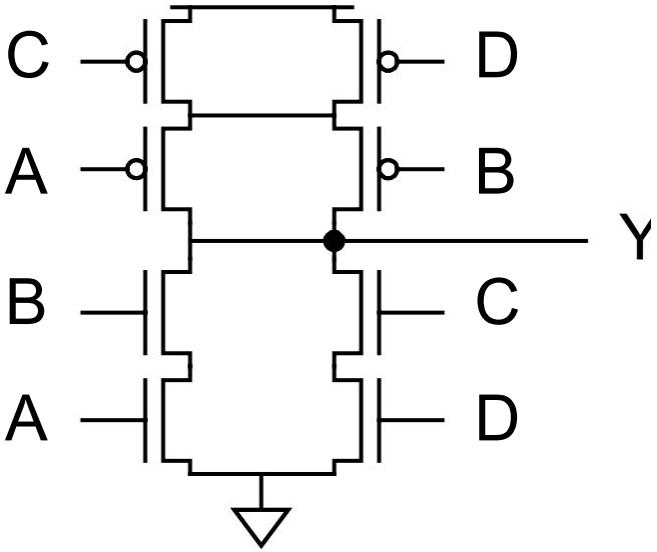


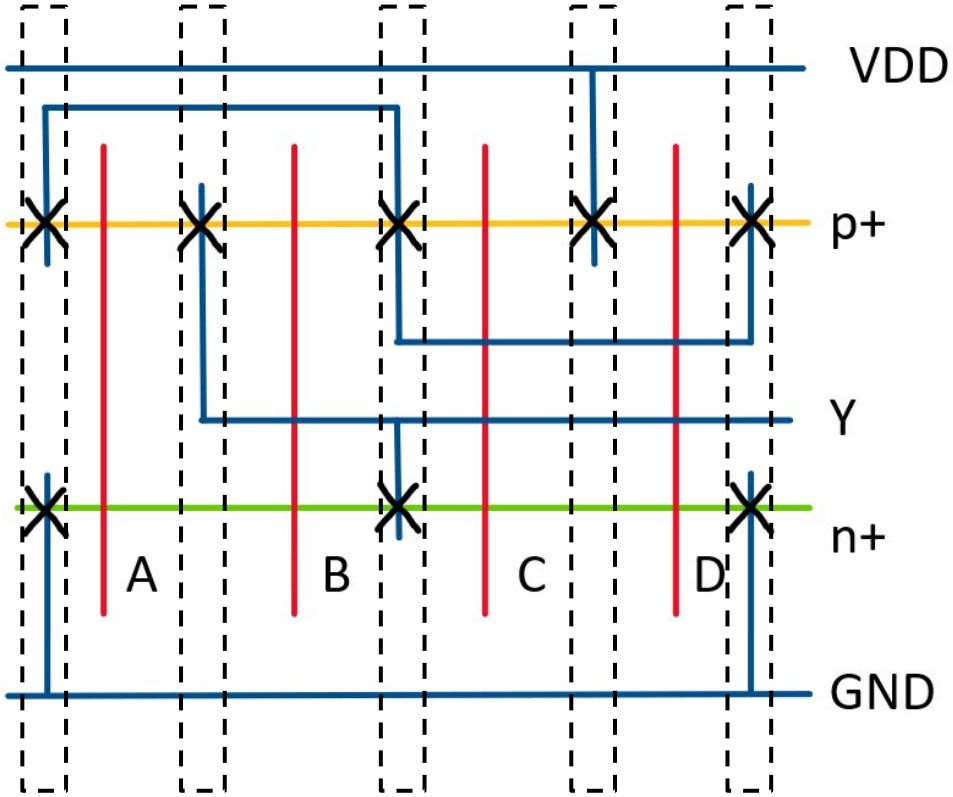


$$Y = \overline{AB + CD}$$

Parallel tracks along the width = 5 metals

width = 5x8λ = 40 λ

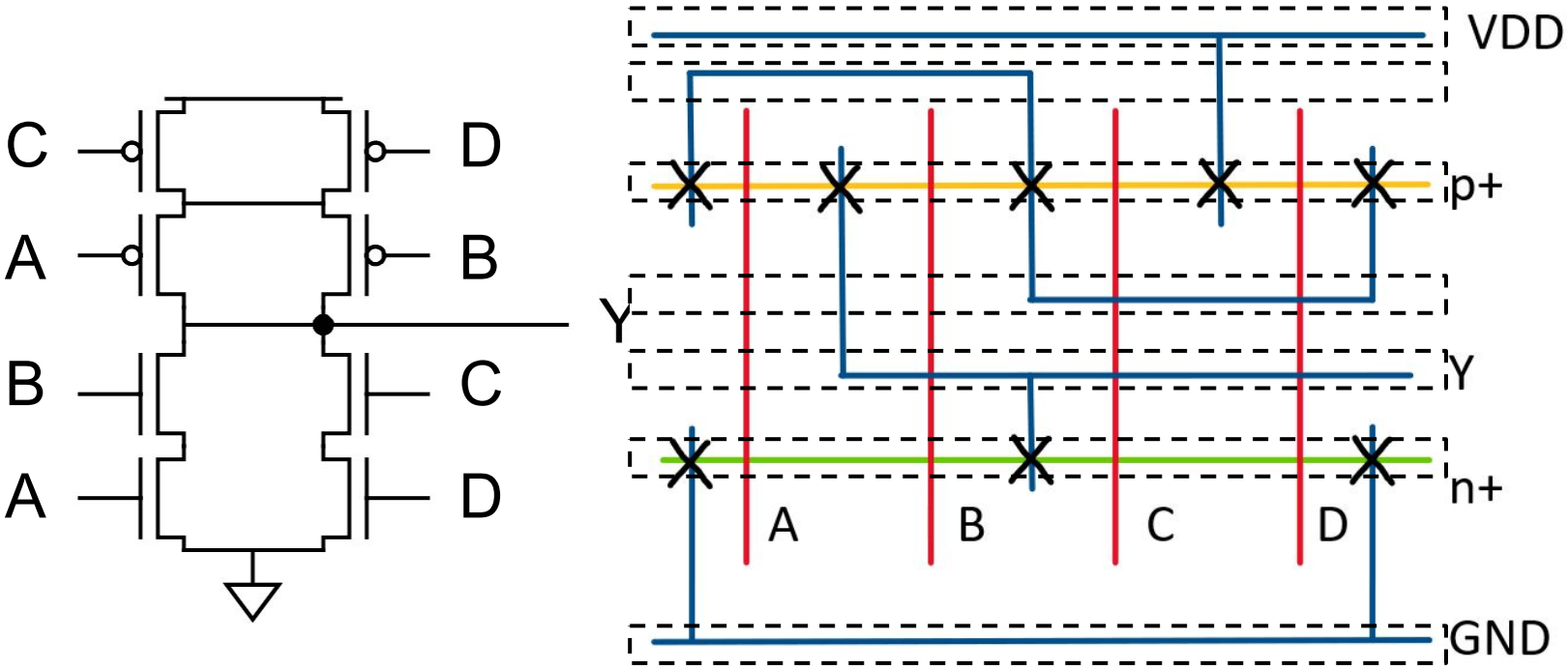




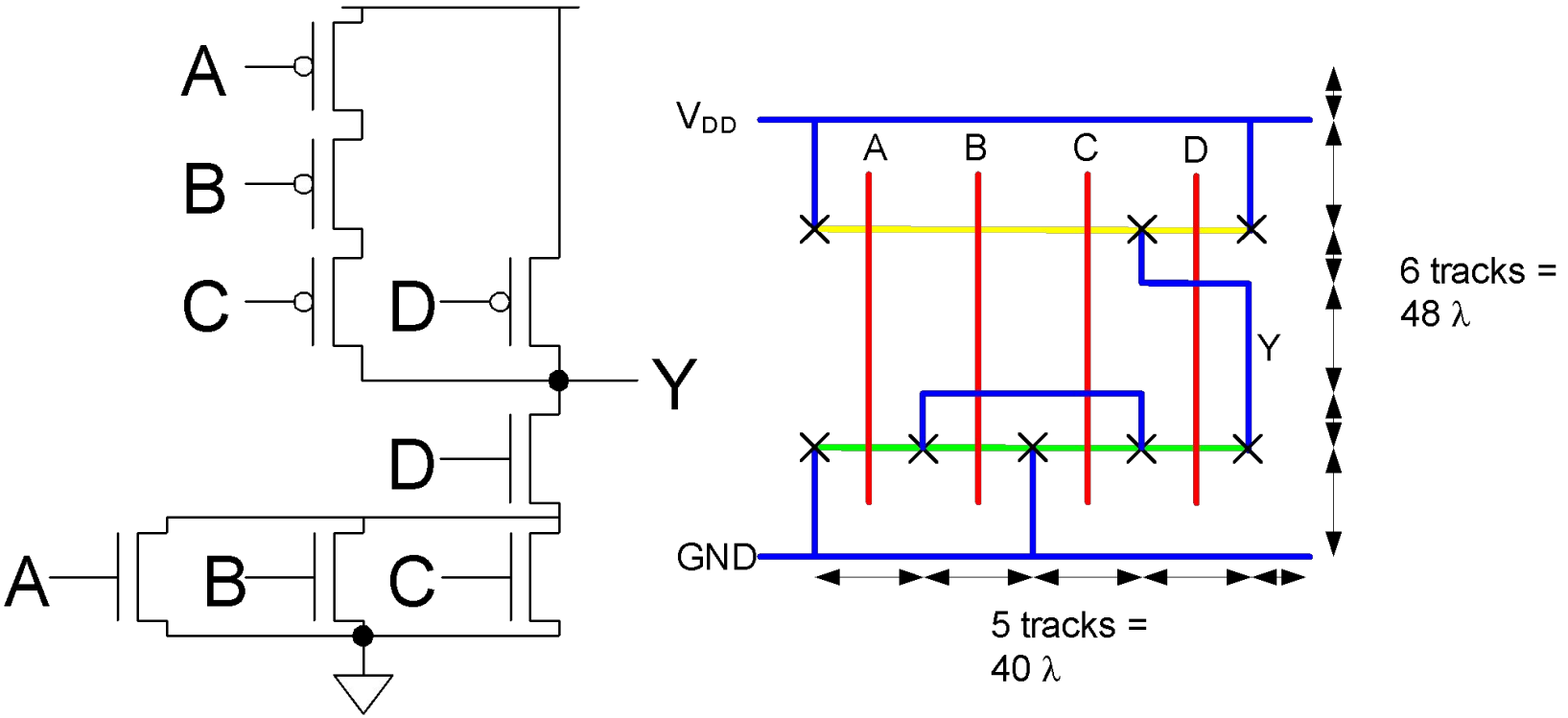
$$Y = \overline{AB + CD}$$

Parallel tracks along the height = 5 metals + 2 diff

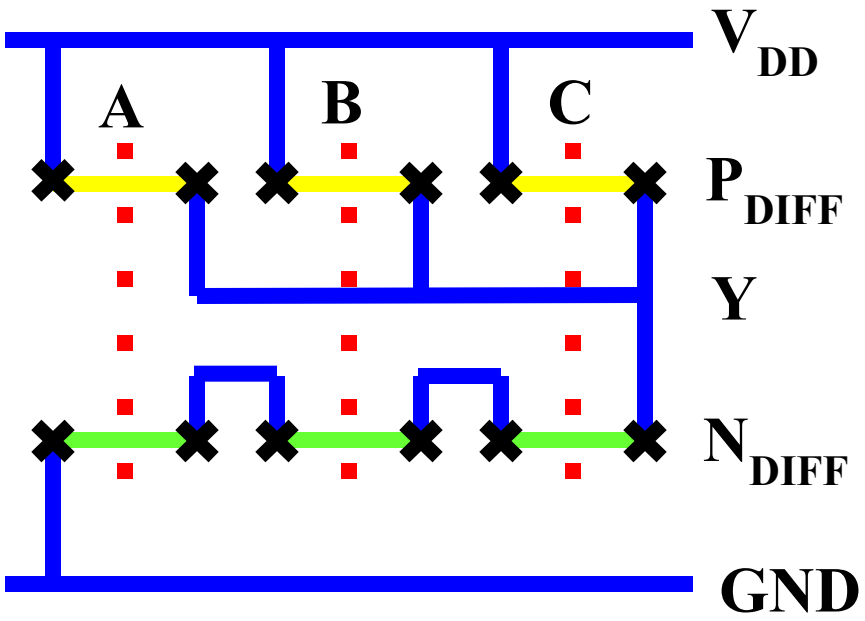
width = 7x8λ = 56 λ



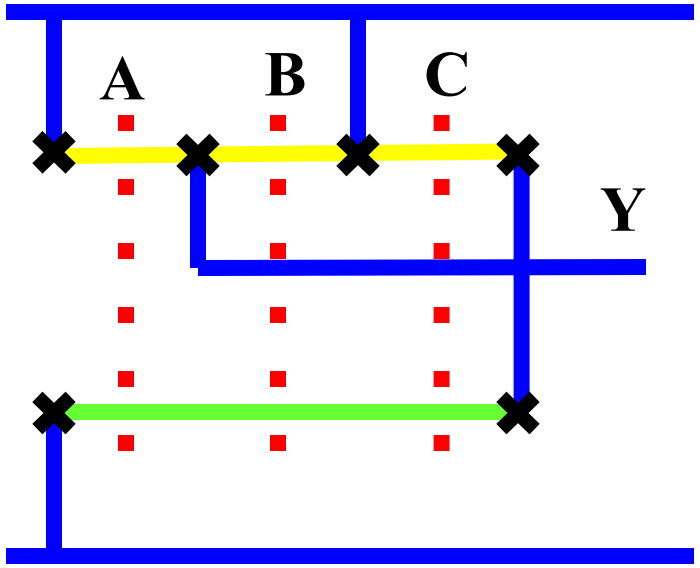
$$Y = \overline{(A + B + C)D} \; (O3AI)$$



Stick Diagram Optimization

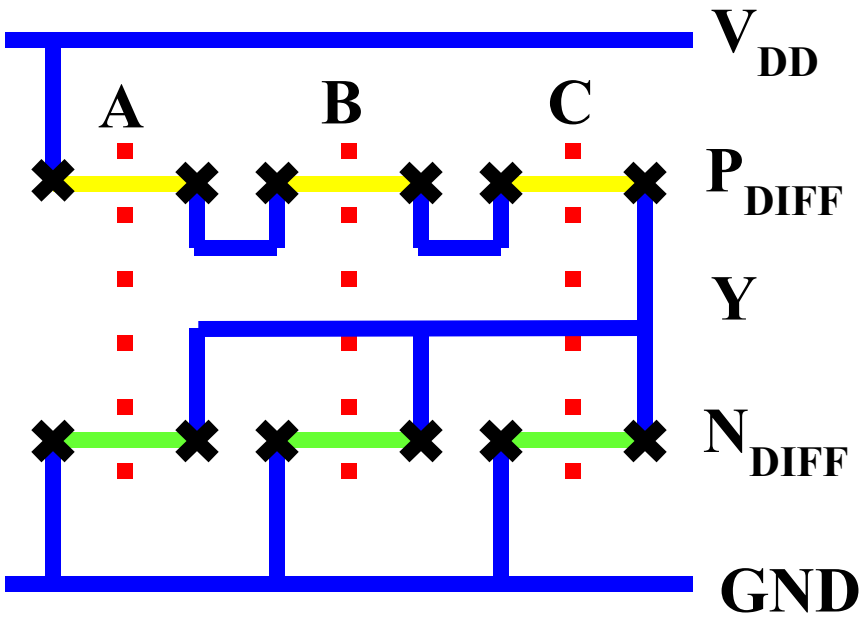


3-NAND

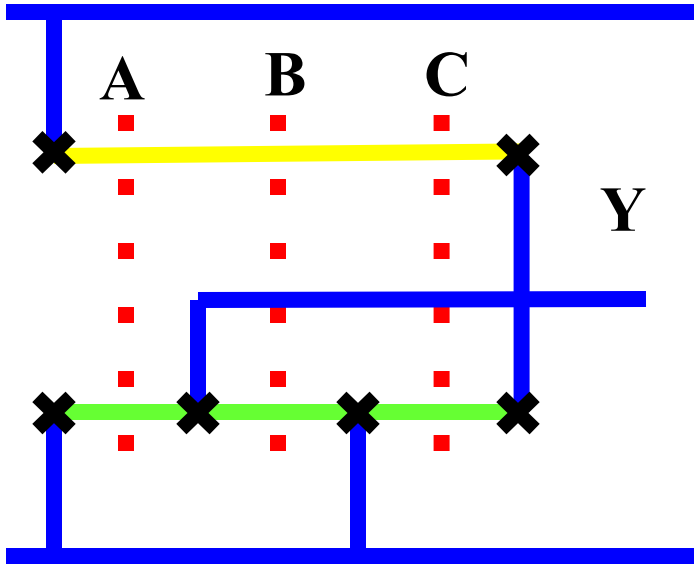


After Optimization

Stick Diagram Optimization



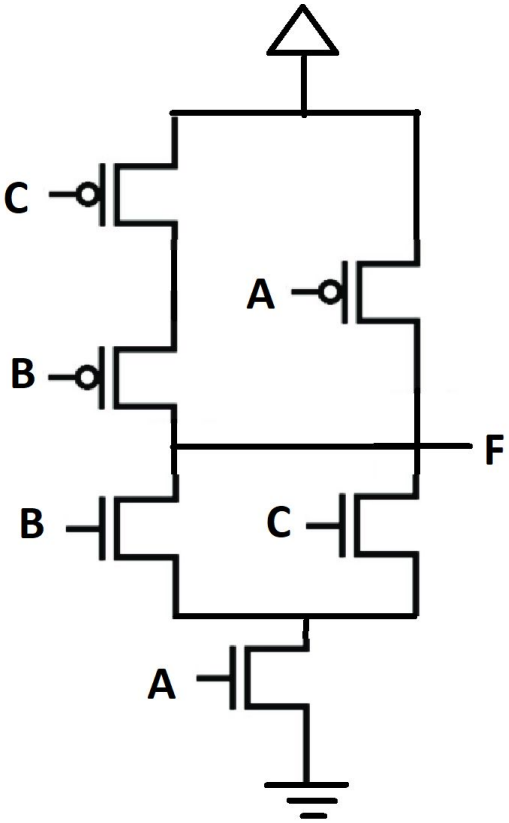
3-NOR

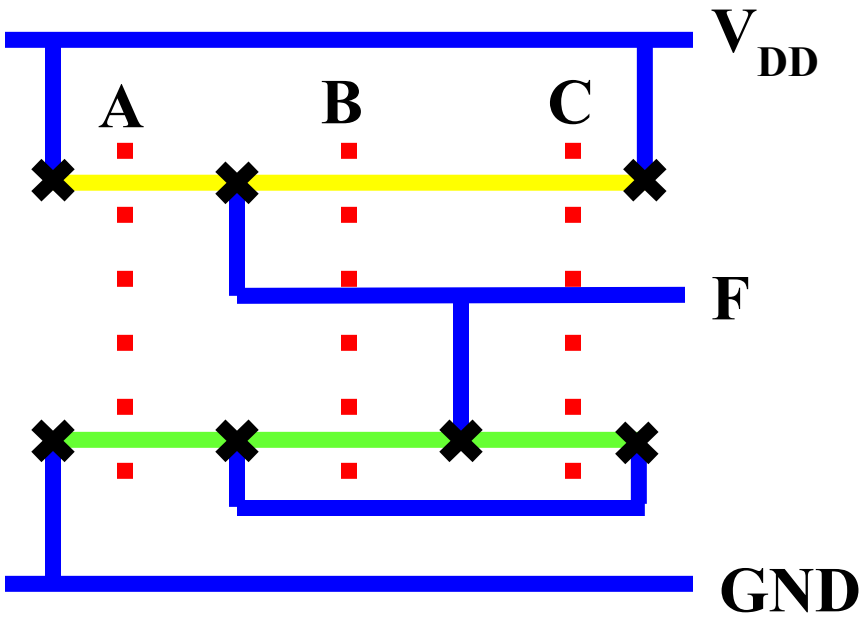


After Optimization

Alternate Representations

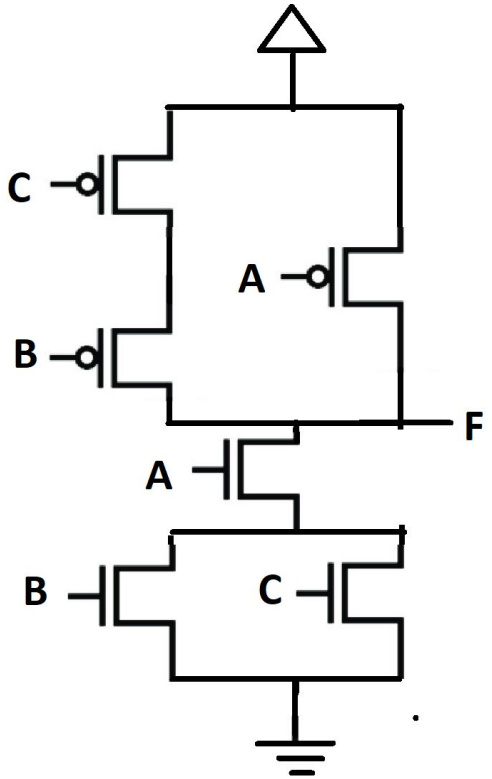
$$\overline{A(B+C)}$$

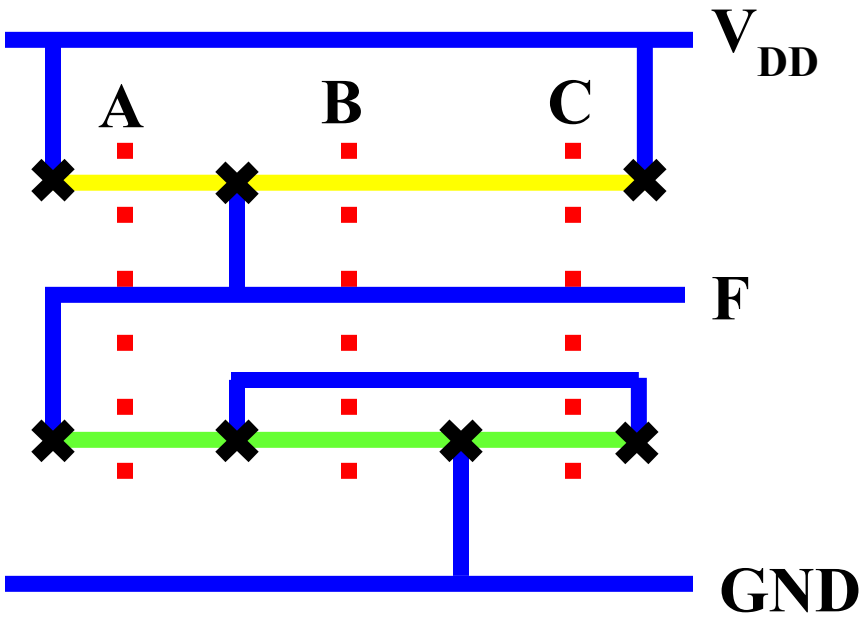




Alternate Representations

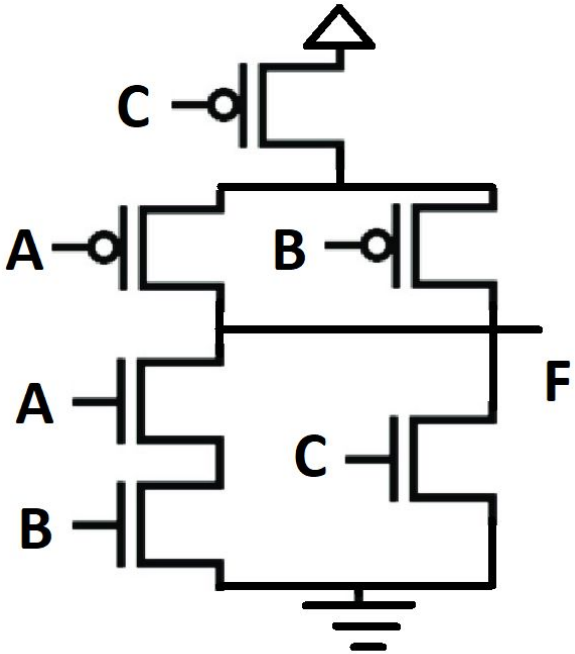
$$\overline{A(B+C)}$$

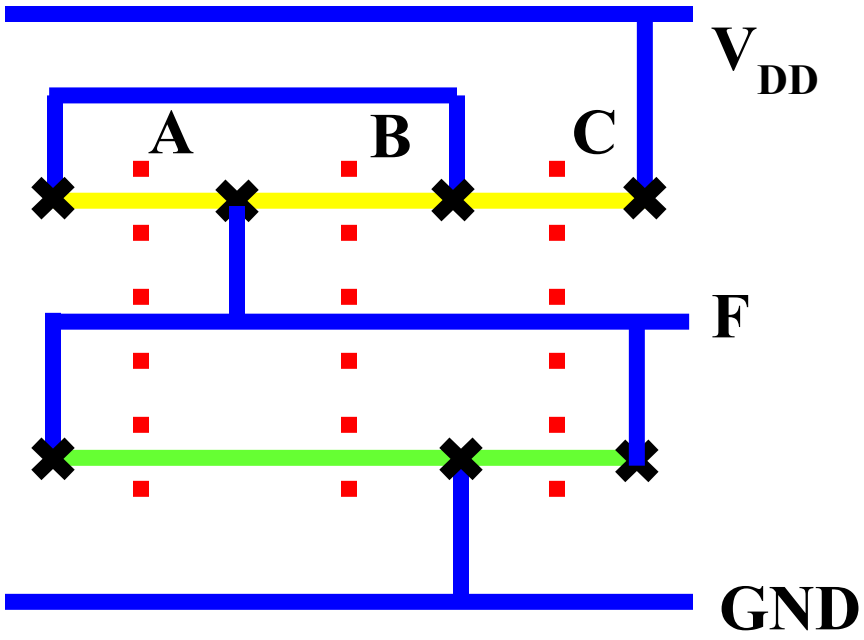




Alternate Representations

$$\overline{AB + C}$$





Alternate Representations

$$\overline{AB + C}$$