CSE460: VLSI Design

A. Course General Information:

Course Code:	CSE460
Course Title:	VLSI Design
Credit Hours (Theory+Lab):	3 + 0
Contact Hours (Theory+Lab):	3 + 3
Category:	Program Core/Elective
Type:	Required, Engineering, Lecture + Laboratory
Prerequisites:	CSE260 Digital Logic Design

B. Course Catalog Description (Content):

Introduction to VLSI (Very Large Scale Integration) design: history, IC trends, technology & design approaches. Moore's law. Review of digital logic design.

Introduction to logic circuit families: n-MOS, p-MOS, pseudo n-MOS and CMOS technologies. Introduction to CMOS logic. Pull-up and pull-down networks, implementation using series and parallel MOSFETs. Combinational logic circuit design using CMOS. Complex gate design using CMOS such as And-Or-Invert or Or-And-Invert. Implementation of different circuit elements like basic gates. Multiplexers, encoder, latch, flip-flops using CMOS.

Introduction to FSM (Finite State Machine): Moore type & Mealy type FSM hardware implementation. State encoding & minimization techniques.

DC Response of CMOS gates: n-MOS & p-MOS pass transistors. Logic levels and noise margins. DC transfer characteristics.

CMOS Power: instantaneous and average power, energy. Power analysis of circuit elements (R, C, DC Supply). Switching waveforms of an inverter. Static power and Dynamic power. Activity factor. Power reduction techniques: Clock gating, Power gating, Dynamic voltage scaling.

Transient response of CMOS gates. Delay definitions: rise time, fall time, propagation delay and

contamination delay, RC delay model. Effective resistance & capacitance. Elmore delay. Parasitic and effort delay. Fan-in and fan-out. Layout comparisons.

Physical design of ICs: floorplanning, partitioning, routing, clock tree synthesis, KL Algorithm for partitioning, Lee's algorithm for global routing.

C. Course Objective:

a. The objectives of this course are to give a brief introduction to the complete process of chip designing
b. provide background knowledge to design, simulate and implement combinational & sequential CMOS circuits
c. teach theoretical concepts to critically analyze the cost & performance of an IC
d. expose the students to the physical design aspects of CMOS IC design
e. introduce the necessary programming language/softwares such as: Verilog (programming language), Quartus II, Microwind & DSCH2 to design, simulate, visualize and verify CMOS logic circuits and layouts

D. Course Outcomes (COs):

Upon successful completion of this course, students will be able to

Sl.	CO Description	Weightage (%)
CO1	**Design** combinational and sequential circuits in CMOS by demonstrating the current voltage relationship and the dc response, and compute the noise margin of CMOS circuits.	30%
CO2	**Construct** system design process using finite state machines and hardware description language.	25%
CO3	**Analyze** the power dissipation and propagation delay of CMOS circuits.	25%
CO4	**Devise** algorithms to design and optimize the physical layout of an IC.	20%

E. Mapping of CO-PO-Taxonomy Domain & Level- Delivery-Assessment Tool:

Sl.	CO Description	PLOs	Bloom's taxonomy domain/level	Delivery methods and activities	Assessment tools
CO1	**Design** combinational and sequential circuits in CMOS by demonstrating the current voltage relationship and the dc response, and compute the noise margin of CMOS circuits.	PLO2	Cognitive/Evaluate	Lectures, Notes, Labs, Assignments	Quiz, Exam, Assignments, Lab Assessment
CO2	**Illustrate** the system design process using finite state machines and **construct** them using a hardware description language.	PLO5	Cognitive/Evaluate	Lectures, Notes, Labs, Assignments	Quiz, Exam, Assignments, Lab Assessment
CO3	**Analyze** the power dissipation and propagation delay of CMOS circuits.	PLO1	Cognitive/Analyze	Lectures, Notes, Assignments	Quiz, Exam, Assignments
CO4	**Devise** algorithms to design and optimize the physical layout of an IC.	PLO4	Cognitive/Create	Lectures, Notes, Assignments	Quiz, Exam, Assignments

F. Course Materials:

i. Text and Reference Books:

Sl.	Title	Author(s)	Publication Year	Edition	Publisher	ISBN
1	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste & David Money Harris	2011	4th ed.	Addison-Wesley	ISBN 13: 978-0-321-54774-3
2	Fundamentals of Digital Logic with Verilog Design	Stephen Brown & Zvonko Vranesic	2014	3rd ed.	McGraw-Hill	ISBN 978–0–07–338054–4
3	Algorithms for VLSI Physical Design Automation	Naveed A. Sherwani	1998	3rd ed.	Springer	ISBN 978-1-4757-2219-2

ii. Other materials (if any)

a. Lecture notes and presentation slides
b. Class notes
c. Lab handouts and presentation slides
d. Softwares: Quartus II, DSCH2

G. **Lesson Plan:**

i. Theory (2 lectures/week, 1 hour 20 minutes each)

No	Topic	Week/Lecture#	**Related CO (if any)**
1	● Introduction to VLSI (Very Large Scale Integration) design: history, IC trends, technology & design approaches. Moore's law. ● Review of digital electronics	Week 1/Lecture 1-2	CO1
2	● Logic circuit families: n-MOS, p-MOS, pseudo n-MOS and CMOS technologies. Introduction to CMOS logic. Pull-up and pull-down networks, implementation using series and parallel MOSFETs. ● Implementation of combinational logic blocks and sequential elements in CMOS technology	Week 2/Lecture 3-4	CO1
3	● Pass transistor DC characteristics ● Complex gate design and Implementation of different circuit elements like basic gates, multiplexers, encoders, latch, flip-flops using CMOS pass transistors and transmission gates. ● Quiz 1	Week 3/Lecture 5-6	CO1
4	● FSM Introduction ● FSM moore and mealy type machine	Week 4/Lecture 7-8	CO2

5	• System design using Moore and Mealy type finite state machines • Different hardware implementation techniques • Quiz 2	Week 5/Lecture 9-10	CO2
6	Reserved for Quiz 1+2	Week 6	CO1, CO2
7	Midterm Exam	Week 7	CO1, CO2
8	• Physical design: floor planning, partitioning, routing, clock tree synthesis. KL algorithm for partitioning.	Week 8/Lecture 11-12	CO4
9	• Lee's maze algorithm for global routing	Week 9/Lecture 13-14	CO4
10	• Transient response of CMOS gates. Delay definitions: rise time, fall time, propagation delay and contamination delay, RC delay model. Effective resistance. MOS Capacitance. • Quiz 3	Week 10-/Lecture 15-16	CO3
11	• Elmore delay. Parasitic and effort delay. Fan-in and fan-out. Layout comparisons	Week 11/Lecture 17-18	CO3
12	• CMOS Power: Instantaneous and Average power, Energy. Power in circuit elements analysis (R, C, DC Supply). Switching waveforms of an inverter. Static power and Dynamic power. Activity factor. Power reduction techniques: Clock gating, Power gating, Dynamic voltage scaling. • Quiz 4	Week 12/Lecture 19-20	CO3
13	Reserved for Quiz 3+4	Week 13	CO3, CO4
14	Final Exam	Week 14	CO3, CO4

ii. Lab (1 lecture/week, 2 hours 20 minutes each)

No	Topic	Week/Lecture#	Related CO (if any)
1	No lab	Week 1	-
2	Experiment 1: CMOS Schematic Circuit Design in DSCH2	Week 2	CO1
3	Experiment 2: Introduction to Verilog; Verilog Design Part 1 (combinational logic)	Week 3	CO1
4	Experiment 3: Verilog Design Part 2 (sequential logic)	Week 4	CO1
5	Midterm		
6	Lab Test-1	Week 5	CO1
7	Experiment 4: Verilog Design Part 3 (FSMs)	Week 6	CO2
8	Experiment 5: Verilog Design Part 4 (FSMs)	Week 7	CO2
9	Lab Test-2	Week 8	CO2
10	No lab	Week 9	

H. Assessment Tools:

Assessment Tools	Weightage (%)
Class Performance & Attendance	5
Assignments	5
Quizzes	15
Lab	25
Midterm Exam	25
Final Exam	25

I. CO Assessment Plan:

Assessment Tools	Course Outcomes			
	CO1	CO2	CO3	CO4
Quizzes	√	√	√	√
Assignments	√	√	√	√
Lab	√	√		
Midterm exam	√	√		
Final Exam			√	√