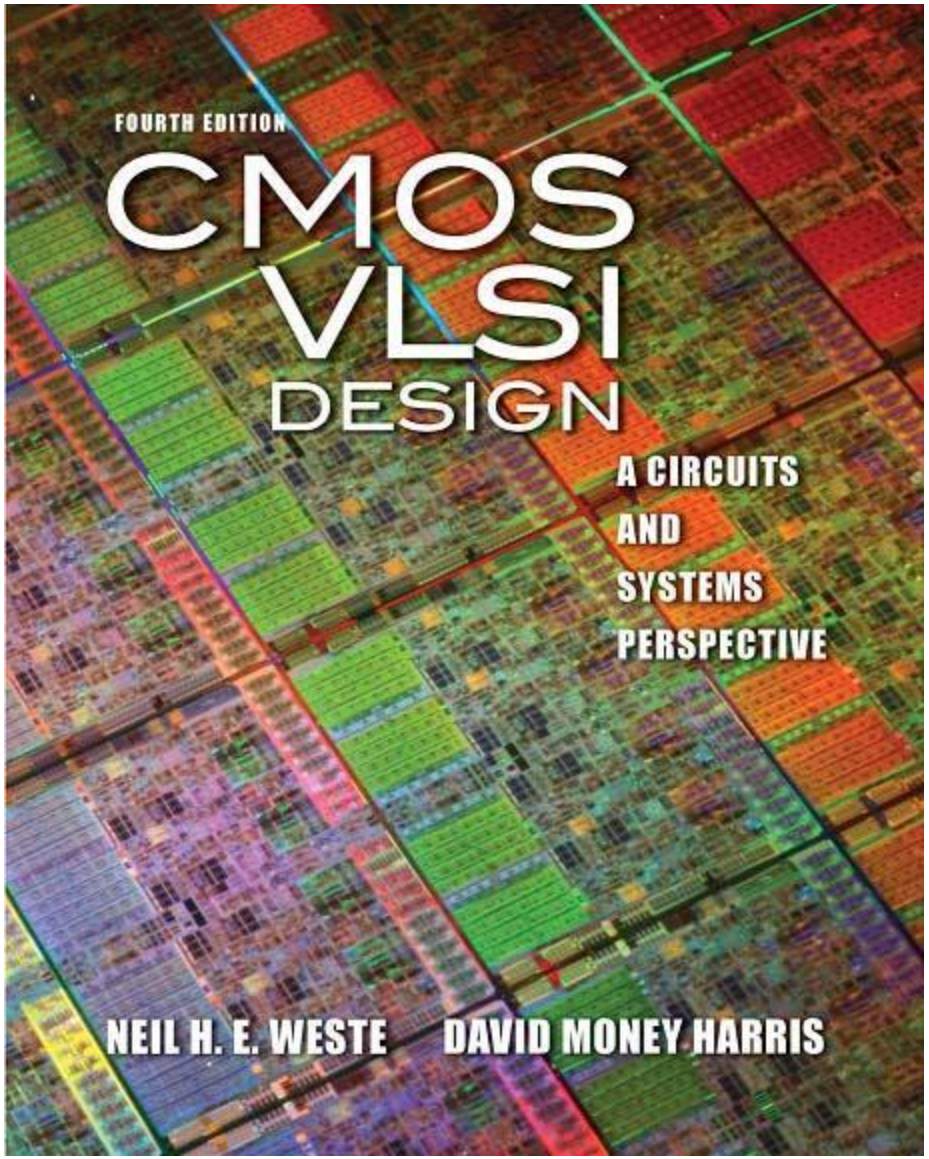
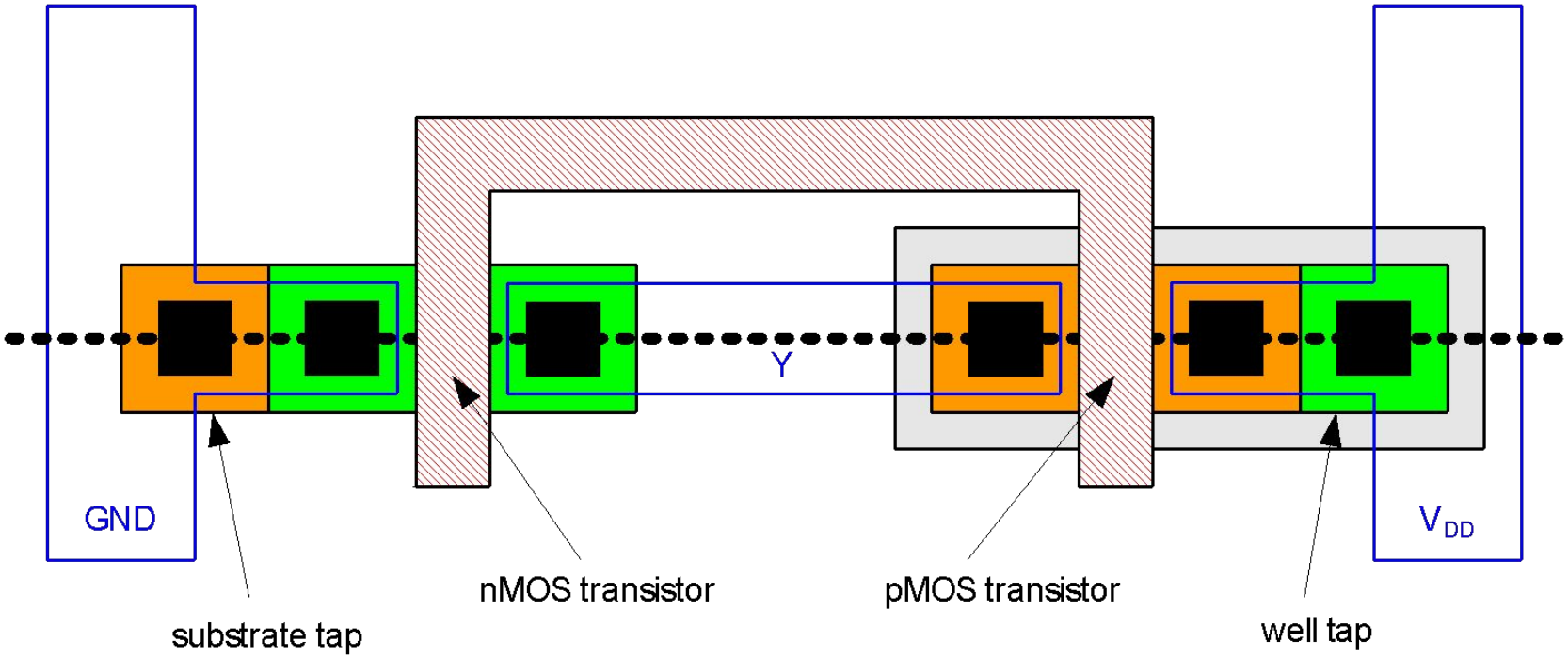


Lecture 10: Layout & Stick Diagrams

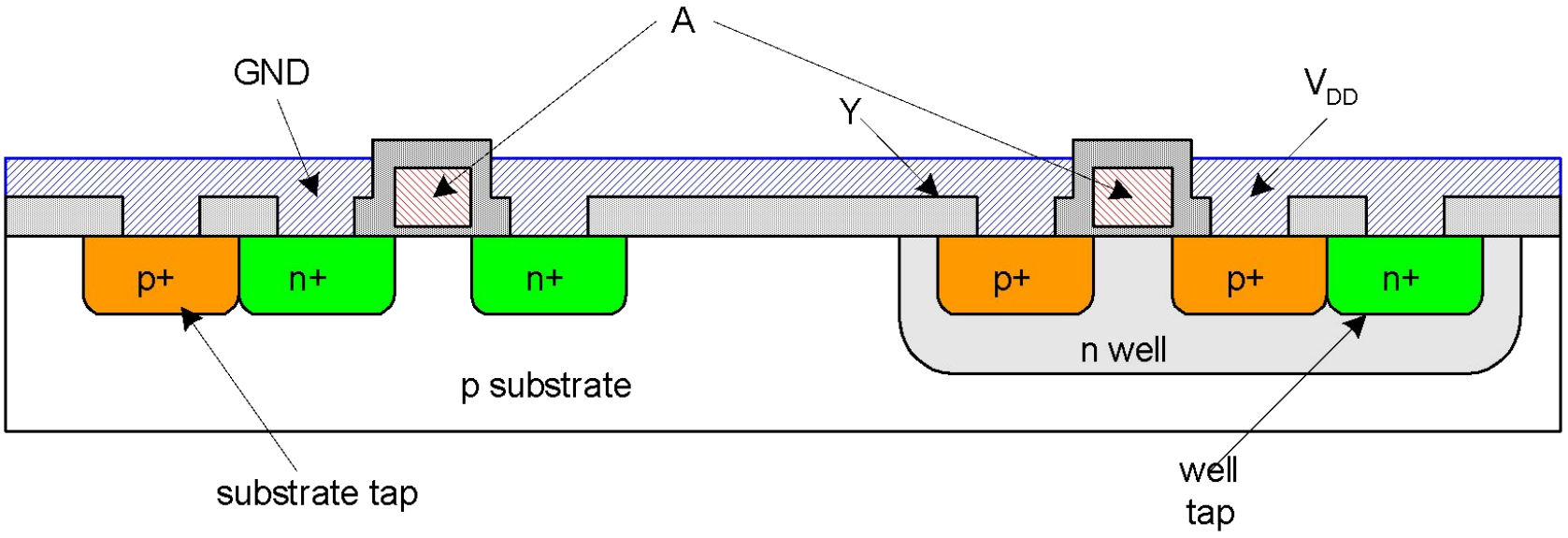
Inverter Top View

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Inverter Cross-section

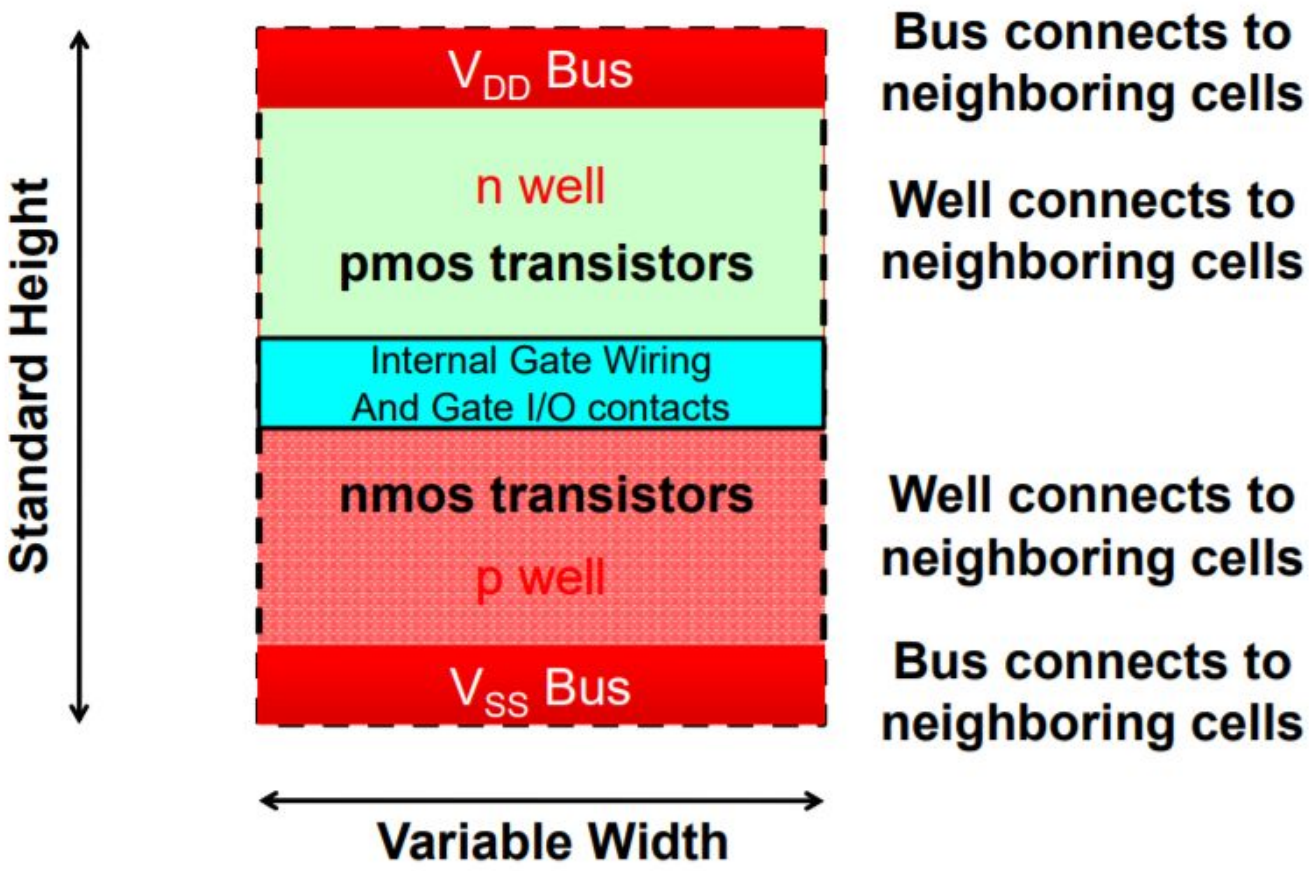
- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



Gate Layout

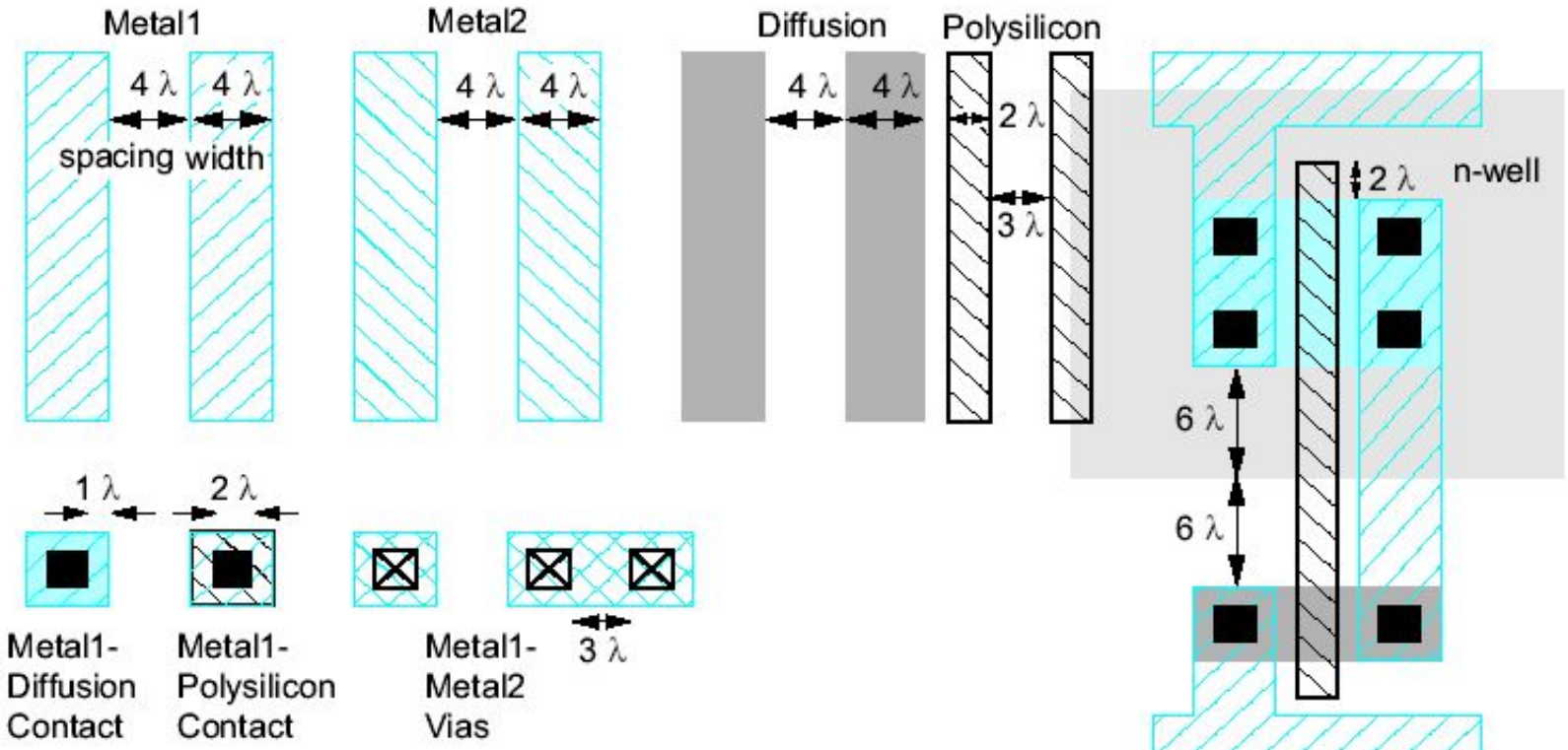
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

Standard Cell Layout



Simplified Design Rules

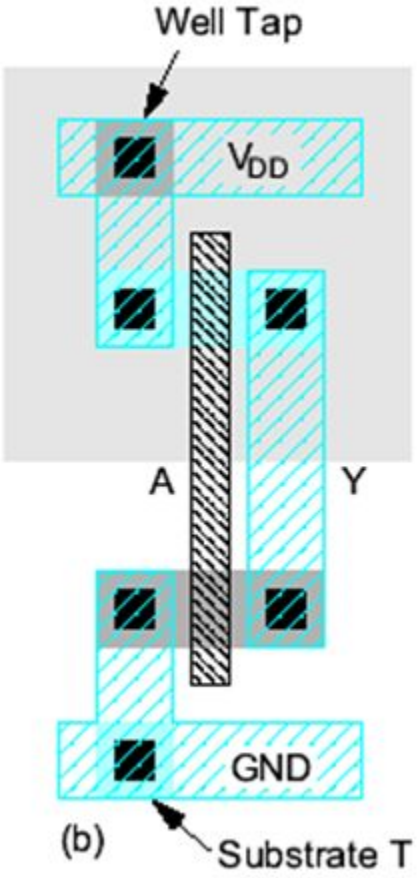
- Conservative rules to get you started



Source and Drain

- We will follow the convention: current always flows from top to bottom in an electronic circuit
  - For pMOS transistor:
    - Carrier: holes (+)
    - Top node: Source
    - Bottom node: Drain
  - For nMOS transistor:
    - Carrier: electrons (-)
    - Top node: Drain
    - Bottom node: Source

Example: Inverter

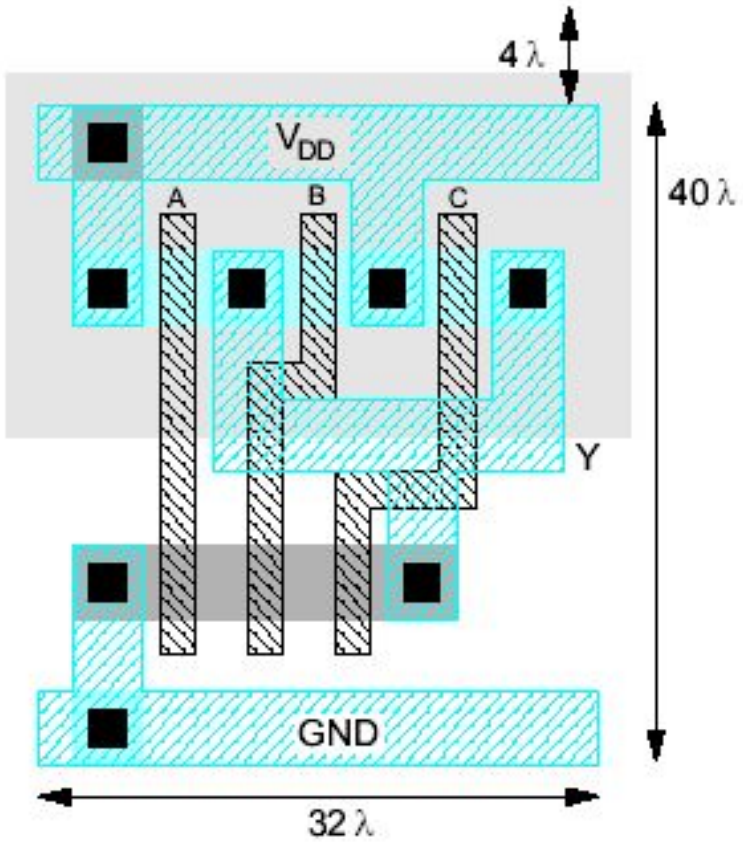


3-input NAND Gate

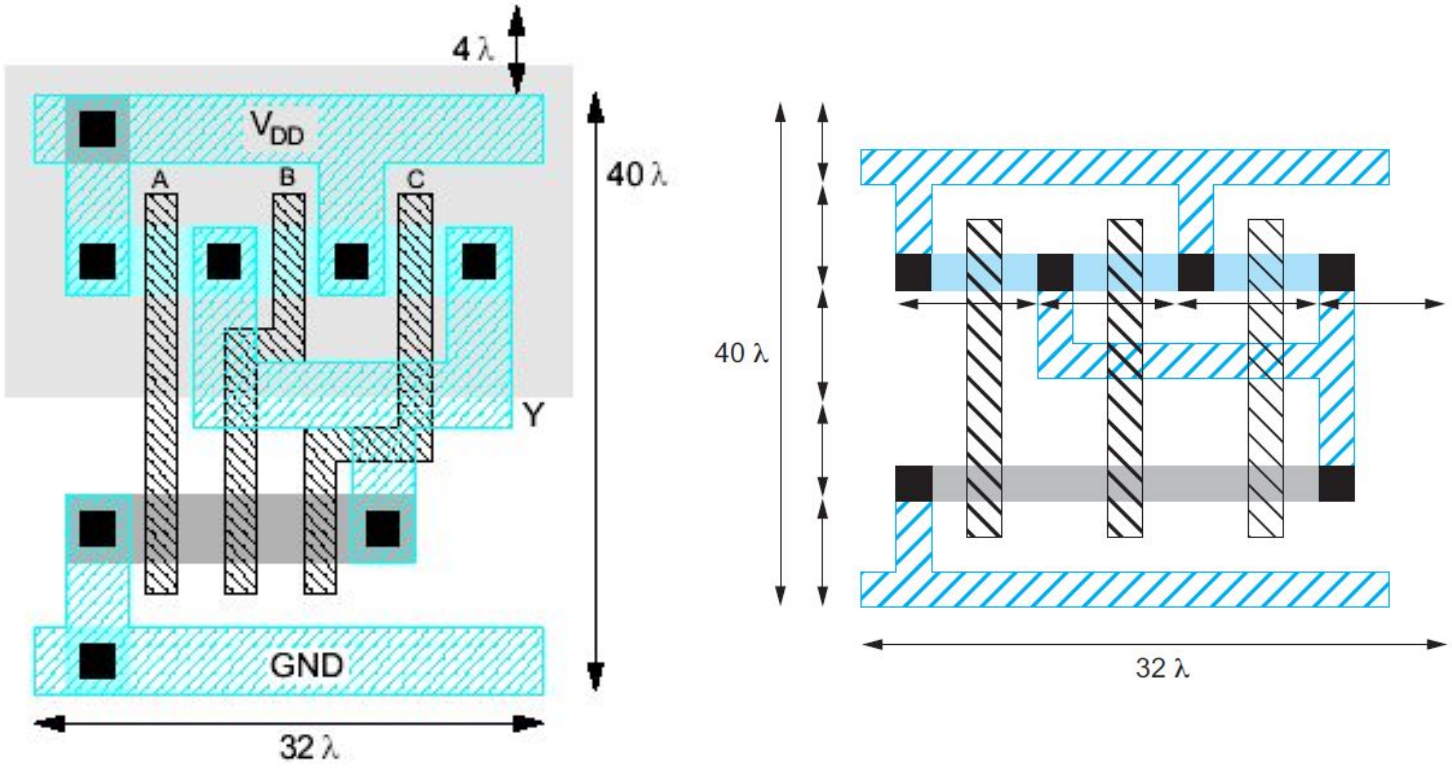
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ

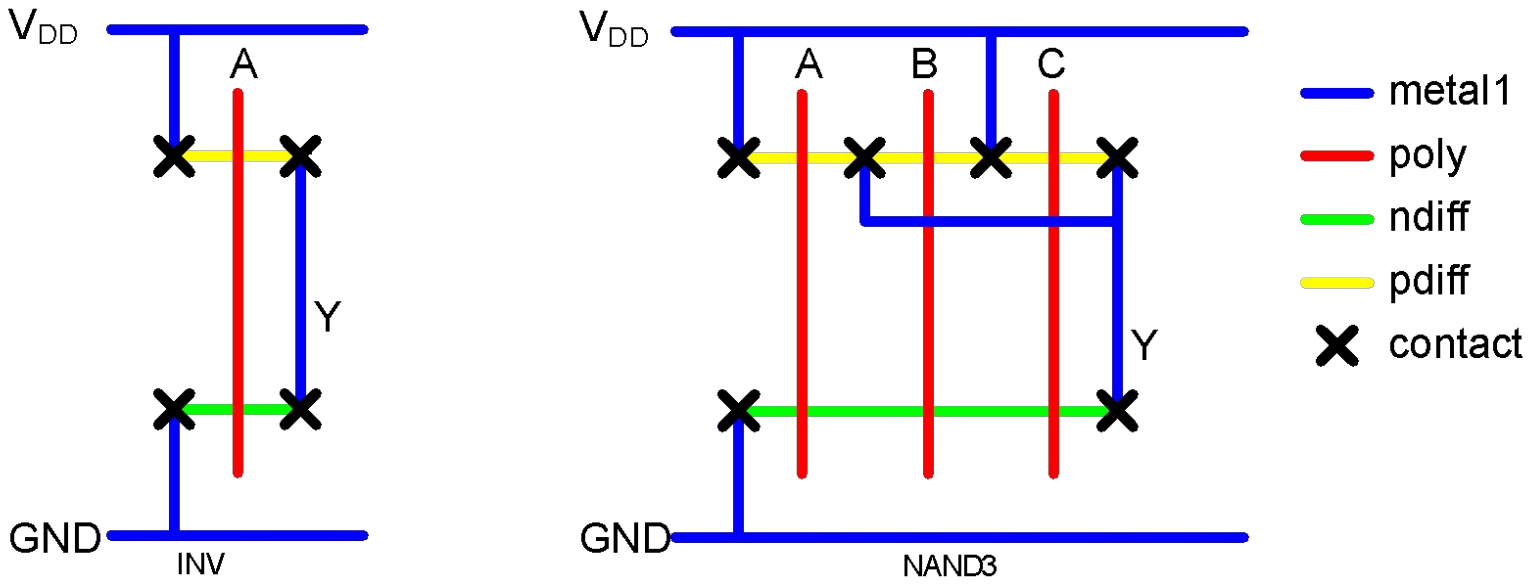


Example: NAND3



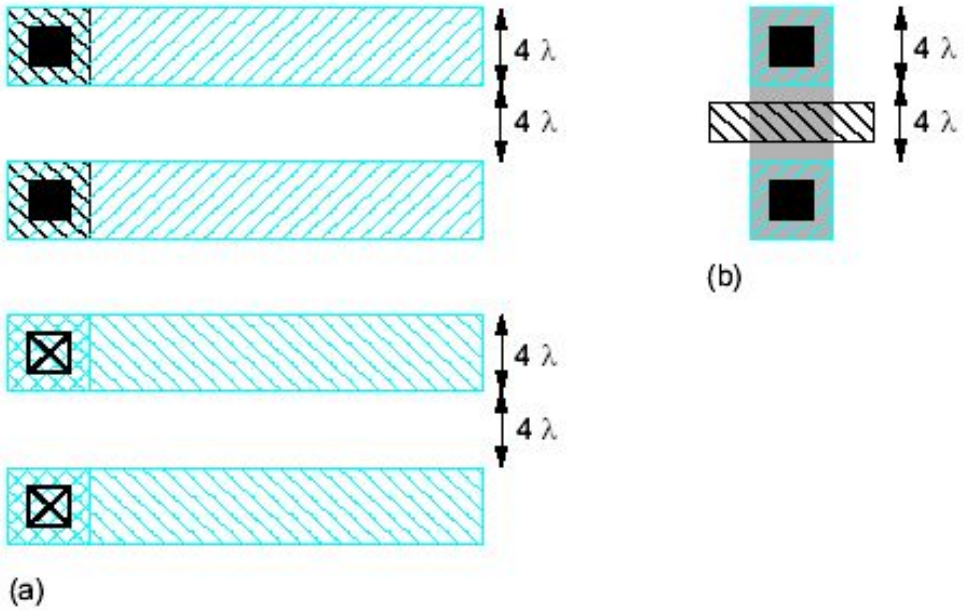
Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers



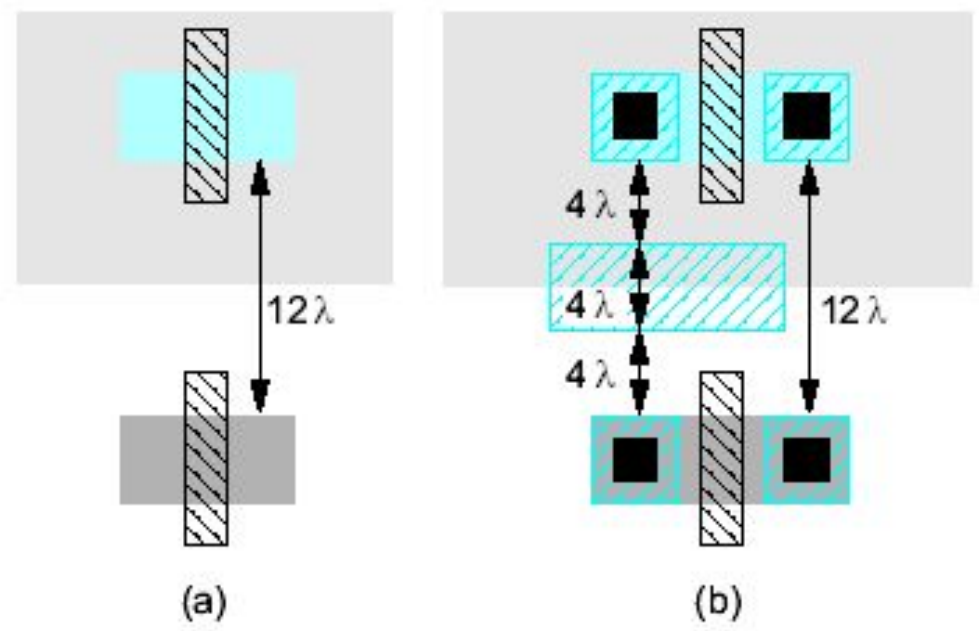
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



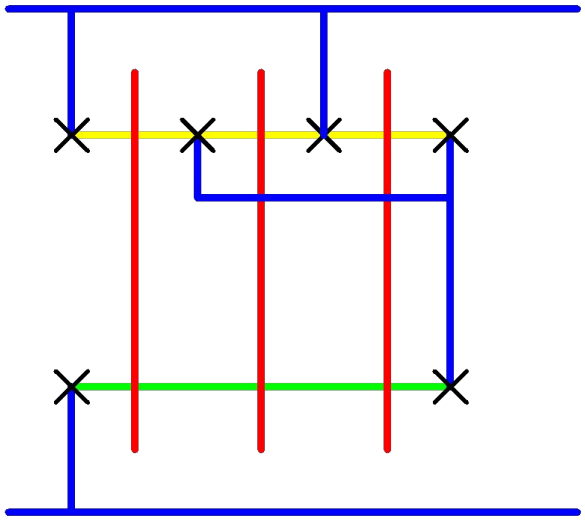
Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



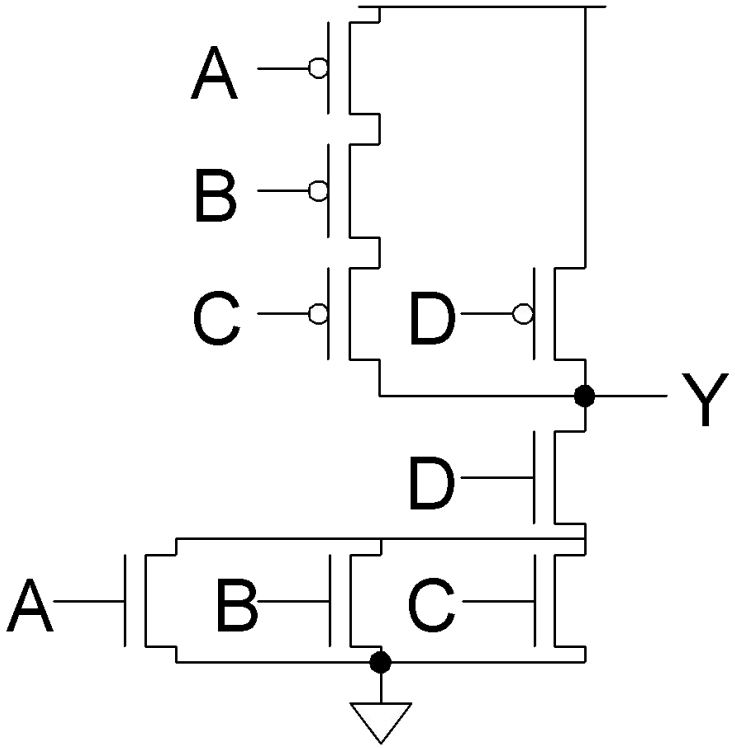
Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ



Example: O3AI

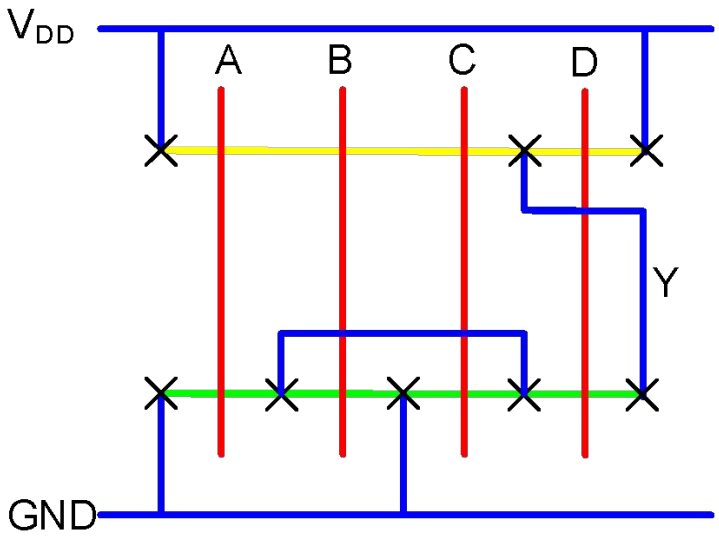
- $Y = \overline{(A + B + C)D}$



Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

$$\overline{Y = (A + B + C)D}$$



Example: NOR4

Example: NOR4