CSE460: VLSI Design (Summer 2025)

Practice problems for exams

[At the end of each lecture there is a "Reading" section in buX. After watching/attending the lectures and reading the corresponding texts, try to solve the following problems. The final questions in the exam will be conceptual & analytical (theoretical and problem solving).]

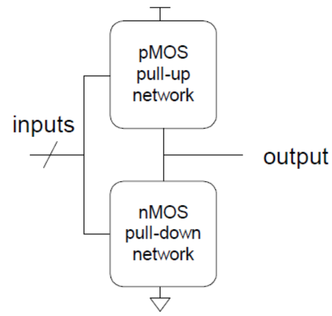
More problems will be added to this doc as we progress through the semester.

Introduction to VLSI Design, History and Timeline

1. Comparison between FET and other types of transistors.
2. How do MOSFETs allow us high levels of integration in IC design?
3. What is Moore's law? Briefly explain using appropriate diagrams.
4. Describe different levels of design abstraction.
5. Suppose, you are building a digital system that has 4 inputs (x1, x2, x3, x4) and you want to produce the output 1 only if the combination of the inputs are 0, 1, 0, 1, respectively. Design a circuit that implements the system using logic gates.
6. Design the simplest circuit that has three inputs, x1, x2, and x3, which produces an output value of 1 whenever two or more of the input variables have the value 1; otherwise, the output has to be 0. (Using karnaugh maps)
7. Design a circuit with output f and inputs x1, x0, y1, and y0. Let X = x1x0 and Y = y1y0 represent two 2-digit binary numbers. The output f should be 1 if the numbers represented by X and Y are equal. Otherwise, f should be 0.
8. Practice designing different logic circuits using logic gates for arbitrary logic functions.

Introduction to CMOS technology and CMOS circuits

1. Why do we use impure (doped) silicon as our substrate for building MOS transistors?
2. What is the conduction complement rule?
3. Explain the following general structure of a CMOS logic gate, mentioning the different behaviours for different combinations of the networks:



4. Design CMOS compound gates that implements the following functions:
    a. Y = (A.B+C.D).E
    b. Y = (A+B).(C+D)
    c. Y = (A.B.C) + D
    d. Y = $\overline{A.(B + C).D}$
5. What is signal strength? Explain the behavior of MOS transistors as pass transistors while mentioning which transistors produce which type of strong and weak signals.
6. Explain restoring and non-restoring properties of a device with the help of different kinds of CMOS tristate devices.
7. Explain how the complexity, cost and area requirement for a 2:1 MUX can be reduced by orders of magnitude by going from gate-level implementation to CMOS transmission gate/CMOS tristate inverter implementation.
8. Design a 2:1 MUX using CMOS tristate inverters and explain its working principle.
9. Design a positive level triggered D latch and explain its working principle.
10. Design a positive edge triggered D flip flop and explain its working principle using a suitable timing diagram.
11. <u>Practice designing CMOS logic gates for arbitrary logic functions.</u>

CMOS Transistor Theory

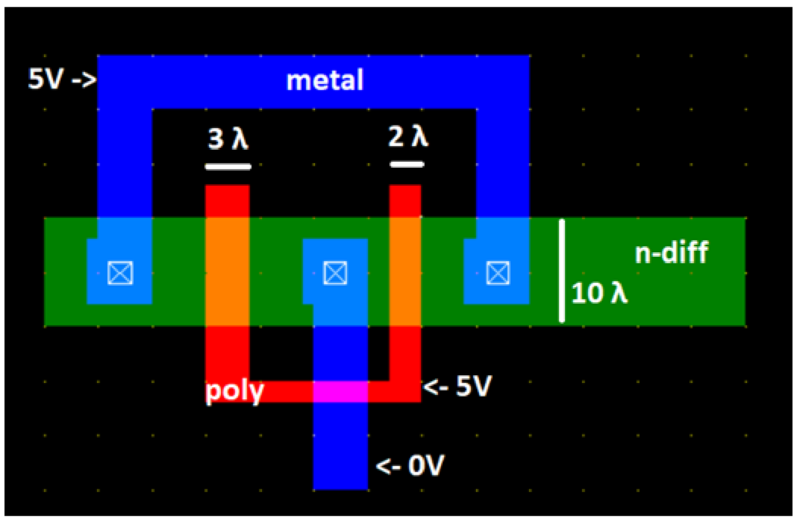
1. What is a MOS capacitor? Explain the different operating modes of the MOS capacitor.
2. Explain the different operating regions of the nMOS transistor and mention the behavior of the transistor current in those regions.
3. Summarize the nMOS and pMOS operating regions based on the terminal voltage differences.
4. Briefly describe the different capacitances associated with an nMOS/pMOS transistor. Mention the advantages and disadvantages of each of the categories of those capacitances.
5. Practice some numerical examples shown in class:
    a. Consider an n-channel MOSFET with the following parameters:
       Vt = 0.4 V, W = 20 μm, L = 0.8 μm, μn = 650 cm2/V–s, tox = 200 Å, and εox = (3.9)(8.85 × 10-14) F/cm. Calculate β. Then determine the operating mode and the current through the transistor (Ids) for the following cases:
       (a) Vgs = 0.8 V & Vds = 0.2 V

(b) Vgs = 1.6 V & Vds = 2.0 V

b. For a 0.8-μm process technology, tox = 15 nm, μ = 275 cm2/V.s, εox = (3.9)(8.85 × 10-14) F/cm and Vt = - 0.7 V.
(a) Judging from the value of Vt and μ, comment on whether the MOSFET is NMOS or PMOS
(b) Calculate Cox
(c) For a MOSFET with W/L = 20 calculate the values of β, Vsg and Vsd(min) needed to operate the transistor in the saturation region with a dc current of Id = 0.1 mA.

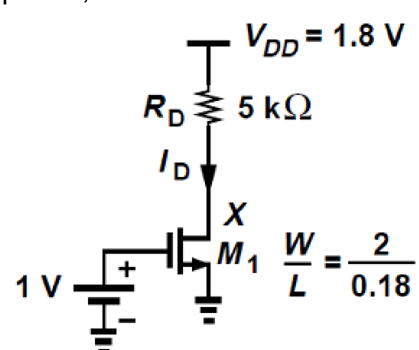
c. Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm (λ = 25 nm). Let W/L = 4/2 λ (i.e. 0.1/0.05 μm). In this process, the gate oxide thickness is 10.5 Å. Estimate the high-field mobility of electrons to be 80 cm2/V· s at 70 ºC. The threshold voltage is 0.3 V. Plot Ids vs. Vds for Vgs = 0, 0.2, 0.4, 0.6, 0.8, and 1.0 V using the long-channel model.

d. Using the figure given below, answer the following questions:



(a) Draw the schematic diagram of the circuit (that results in this layout) and then clearly mark the length and width of each of the transistors.
(b) Find the current flowing through each of the transistors, if μnCox = 120 μA/V2, Vt = 1 V

e. Calculate the drain current Id through the transistor M1 in the following figure, assuming μnCox = 100 μA/V2, Vt = 0.4 V.

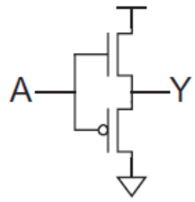


(Hint: assume linear/saturation region and try to find Id. Verify (if your initial assumption is correct or not) by checking if the conditions for the linear/saturation region hold(/ are violated) for the calculated value of Id. Answer: 0.2 mA)

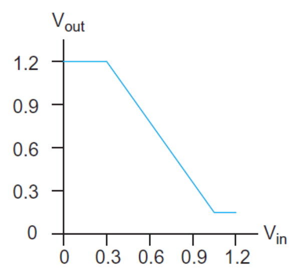
DC Response and Introduction to FSMs

DC Response

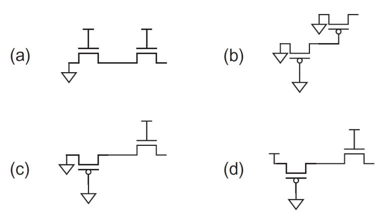
1. Peter Pitfall is offering to license to you his patented noninverting buffer circuit shown in the following figure. Graphically derive the transfer characteristics for this buffer. Assume $\beta n = \beta p = \beta$ and $Vtn = |Vtp| = Vt$. Why is it a bad circuit idea?



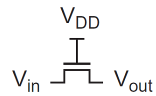
2. Find the ratio of hole mobility to electron mobility of a CMOS inverter given that the beta ratio of pull-up network to pulldown network is 1.5 (Assume that W/L ratio of pMOS is 3 times greater than that of nMOS and all other parameters are same for both)
Assuming the supply voltage to be 3V draw a suitable DC transfer characteristic curve of the CMOS inverter. (Assume any practical value of the threshold voltage, i.e. 0.1 * supply voltage or 0.2 * supply voltage.)
3. A novel inverter has the transfer characteristics shown in the figure. What are the values of VIL, VIH, VOL, and VOH that give best noise margins? What are these high and low noise margins?



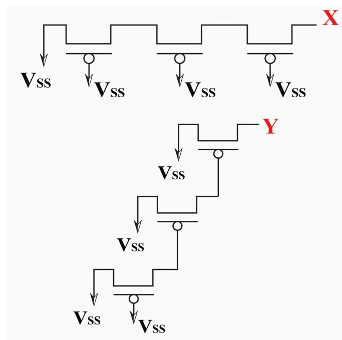
4. Derive analytic expressions for Vout as a function of Vin for regions B and D of the DC transfer function. Let $|Vtp| = Vtn$ and $\beta n = \beta p$.
5. Repeat the previous problem if the thresholds and betas of the two transistors are not necessarily equal.
6. Derive analytic expressions for Vout as a function of Vin for region C of the DC transfer function where both transistors are saturated.
7. Give an expression for the output voltage for the pass transistor networks:



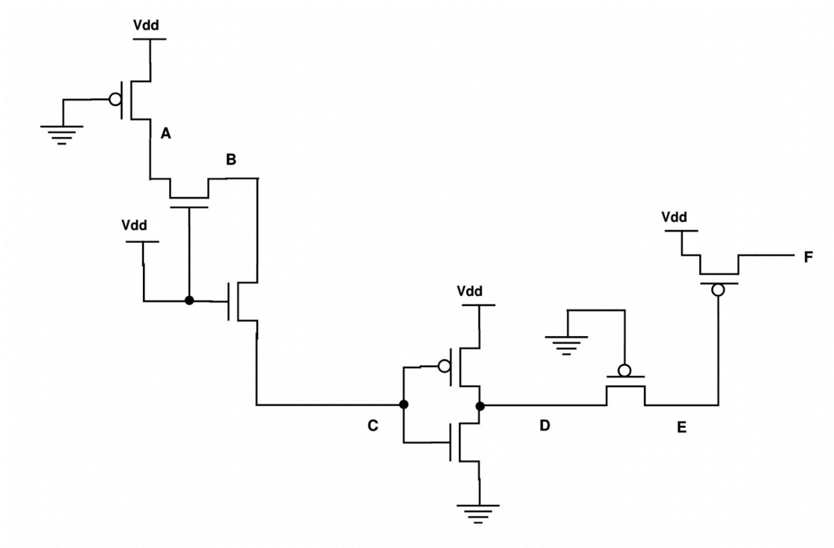
8. Suppose VDD = 1.2 V and Vt = 0.4 V. Determine Vout for the following cases:
   a) Vin = 0 V -> 0V
   b) Vin = 0.6 V -> 0.6V
   c) Vin = 0.9 V ->
   d) Vin = 1.2 V.



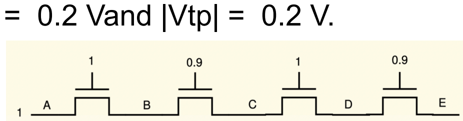
9. From the following figure, find the value of the voltages at points X and Y if VSS = 0 V and Vtp = - 0.3 V. Why do X and Y differ?

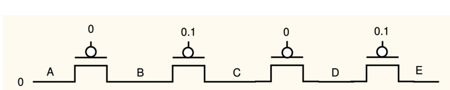


10. From the following figure, find the voltages at each of the nodes, A, B, C, D, E and F. Assume, Vdd = 5 V, Gnd = 0V, Vtn = 0.5 Vand |Vtp| = 1.5 V.



11. From the following figures, find the voltages at each of the nodes, A, B, C, D, E. Assume, Vdd = 1 V, Gnd = 0V, Vtn = 0.2 Vand |Vtp| = 0.2 V.



12. 

<u>Introduction to Finite State Machines</u>

13. What is a sequential circuit? Give a few practical examples of finite state machines.
14. Using a block diagram, explain the working mechanism of a general sequential circuit.
15. What is the difference between a Moore type FSM and a Mealy type FSM?

Finite State Machines

1. Derive the <u>Moore type</u> state diagram, state table, state assigned table and the final circuit for the following systems:
    a. A modulo-6 up counter (i.e. a counter that counts 0,1,2,3,4,5,0,1,2,...).
        i. It should have a 1-bit input w, a clock signal and a multi-bit output z.
        ii. The machine should increase its count whenever w = 1, and hold its previous count otherwise.
        iii. At each counting step the machine should output the value of the count in binary.
    b. A machine that detects the following pattern in its input (w) : 1, 0, 1.
        i. Repeating and overlapping sequences should be detected.
        ii. The machine should generate the output z = 1 if in the past 3 clock cycles 101 pattern was detected, and z = 0 otherwise.
    c. A machine that has the following state table:

Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

    d. An FSM that has an input w and an output z. The machine has to generate z = 1 when the previous four values of w were 1001 or 1111; otherwise, z = 0. Overlapping input patterns are allowed. An example of the desired behavior is:

$$w : 010111100110011111$$
$$z : 000000100100010011$$

1. Explain different types of encoding schemes for FSMs mentioning their advantages and disadvantages.
2. <u>Practice designing Moore type state diagrams for different scenarios.</u>
3. How one-hot encoded sequential circuits can be faster than moore/mealy type sequential circuits?

Fabrication; Layout and Stick Diagram

1. Draw the typical cross-section of an nMOS/pMOS transistor carefully denoting each terminal and their constituent materials.
2. Draw the cross-section of a CMOS inverter in an n-well process (carefully denote each terminal and their constituent materials).
3. Draw the cross-section of a CMOS inverter in a p-well process (carefully denote each terminal and their constituent materials).
4. What are well and substrate taps and why are they necessary?
5. Describe the fabrication process steps briefly.
6. What is the photolithography process?
7. Why do we need contacts?
8. Explain briefly: CVD process, Diffusion process, Ion Implantation process.
9. Discuss some of the basic simplified rules for layout design and using the rules, derive the dimensions of an unit transistor (in terms of λ).
10. In 6 separate figures, draw the set of 6 layout layer masks (n-well, polysilicon, n+ diffusion, p+ diffusion, contact, metal) for the following CMOS inverter layout: (Fig. 1)
11. Draw the cross-sectional view of fig. 1 along Line 1 and 2.

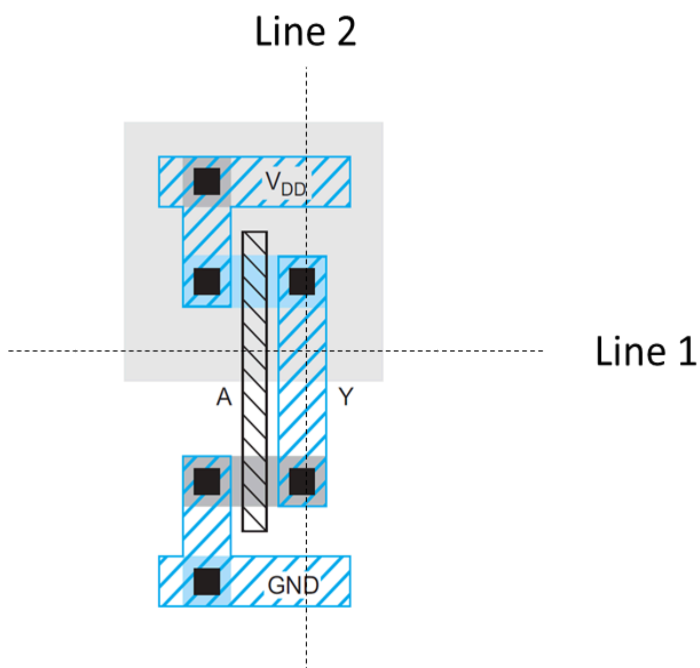


Fig. 1. Draw a set of 6 layout masks and draw the cross-sectional view

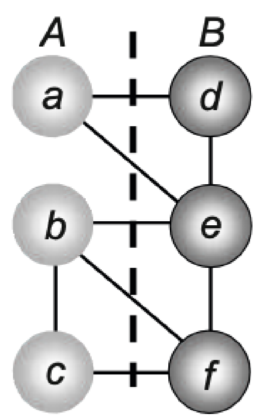
12. Briefly discuss the properties of a standard cell layout.
13. Draw the layout of an isolated nMOS/pMOS transistor.
14. Design the layout of a NAND3/NOR3 gate and determine the area.
15. Explain the "Well-spacing" rule for Lambda based design approach.
16. Define "Wiring Tracks" and derive its dimensions.

17. Explain how one can estimate the area of a layout by counting the vertical and horizontal wiring tracks from its corresponding stick diagram.
18. Practice drawing stick diagrams and estimating the area of different CMOS inverting logic functions/gates.
19. Draw the CMOS architecture and the stick diagram of the following function. Estimate the area.

$$Y = \overline{AB + CD + E}$$

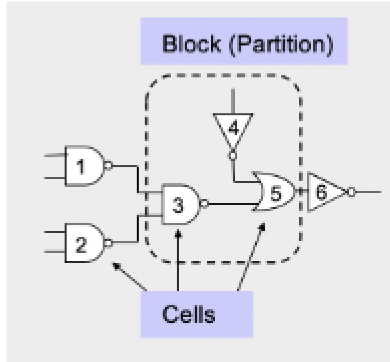
VLSI Physical Design-I

1. What is the difference between floor-planning and placement?
2. The graph below (nodes *a-f*) can be optimally partitioned using the Kernighan-Lin algorithm. Perform the first pass of the algorithm. The dotted line represents the initial partitioning. Assume all nodes have the same weight and all edges have the same priority.

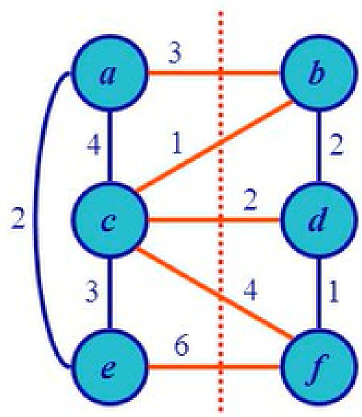


Note: Clearly describe each step of the algorithm. Also, show the resulting partitioning (after one pass) in graphical form.

3. The circuit below (nodes *1-6*) can be optimally partitioned using the Kernighan-Lin algorithm. Transform the following circuit to its equivalent graph representation (**gates to nodes**) and perform the first iteration (swap) of the algorithm and compare the cut cost with the initial one. The dotted line represents the initial partitioning with block A (1,2,6) and B (3,4,5).



4. The graph below (nodes a-f) can be optimally partitioned using the **Kernighan-Lin** algorithm. Perform the first pass of the algorithm. The dotted line represents the initial partitioning. Assume the numbers in the figure are the weights of the corresponding conections.

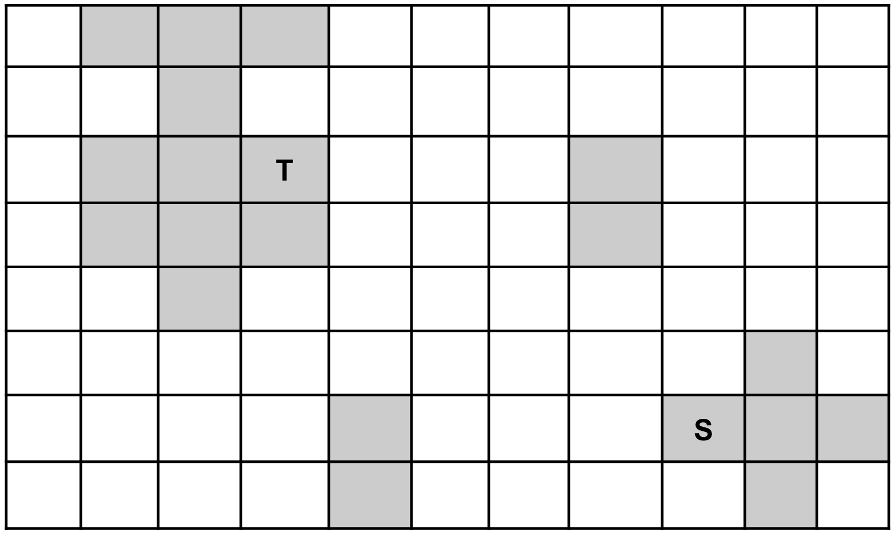


[Hint: Initial cut cost = 3+1+2+4+6 = 16,
Ec(a) = 3, Enc(a) = 6,
D(a) = 3-6 = -3,
D(b) = (3+1)-2 =2,
c(a,b) = 3,
g(a,b) =D(a) + D (b) - 2c(a,b) = -3 + 2 - 2.(3) = -7]

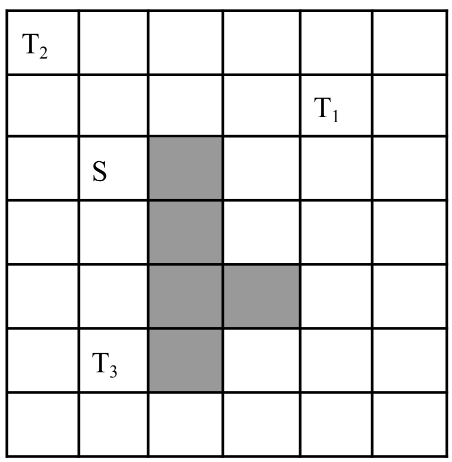
5. What are the different types of routing?
6. What are the goals of Clock Tree Synthesis (CTS)?

VLSI Physical Design-II(Lee's Maze Algorithm)

1. Find the shortest routing path from Source (S) to Target (T) using Lee's Maze algorithm. Find the memory requirements for the calculation. Dark regions are obstacles or components.



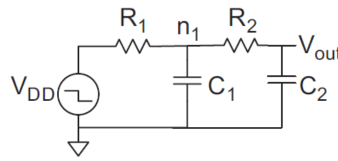
2. i. Find the shortest path for each target using Lee’s maze routing.
   ii. Calculate the total memory usage.



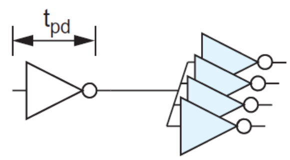
Delay

1. What are the origins of delay in CMOS circuits?
2. What are the major two delays that characterize combinational logic circuits?
3. Define tpdf, tpdr, tcdf, and tcdr using a suitable timing diagram.
4. Describe how one can compute the delay using transient response.
5. Come up with the equivalent nMOS & pMOS RC circuits for the RC delay model.
6. Sketch a 3-input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R). Annotate the gate with its gate and diffusion capacitances. Assume all diffusion nodes are contacted. Then sketch equivalent circuits for the falling output transition and for the worst-case rising output transition.

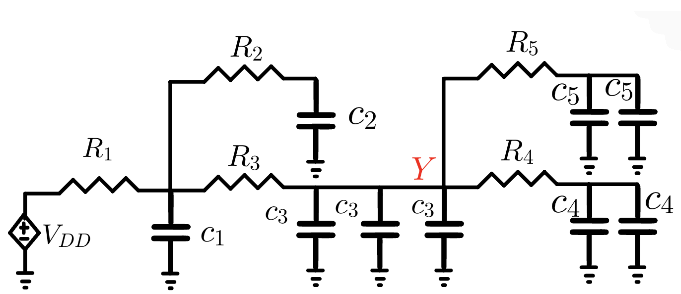
7. Estimate tpdf, tpdr, tcdf, and tcdr for the 3-input NAND gate from the previous problem if the output is loaded with h number of identical NAND gates.
8. Compute the Elmore delay for Vout in the 2nd order RC system:



9. Estimate tpd for a unit inverter driving m identical unit inverters.
10. Repeat the previous problem if the driver is w times unit size.
    If a unit transistor has R = 10 kΩ and C = 0.1 fF in a 65 nm process, compute the delay, in picoseconds, of the inverter shown with a fanout of h = 4. Repeat the problem for h = 10.



11. Exercises 4.1 4.2, 4.3, 4.4, 4.5, 4.6, 4.9, 4.18, 4.19.
12. Calculate all the propagation and contamination delays for a 4-input NOR gate if it drives two inverter and a 3-input NAND gate. Assume all diffusion nodes are contacted and worst case rise and fall resistances are equal to that of a unit inverter (R). [Draw the circuit with gate symbols at first and then, CMOS architecture to derive RC equivalent circuit]
13. Draw the simplified RC network and determine the expression for the Elmore delay, t_{pdr} for node Y.



Power

1. A digital system-on-chip in a 1 V 65 nm process (with 50 nm drawn channel lengths and λ = 25 nm) has 1 billion transistors, of which 50 million are in logic gates and the remainder in memory arrays. The average logic transistor width is 12 λ and the average memory transistor width is 4 λ. The memory arrays are divided into banks and only the necessary bank is activated so the memory activity factor is 0.02. The static CMOS logic

gates have an average activity factor of 0.1. Assume each transistor contributes 1 fF/μm of gate capacitance and 0.8 fF/μm of diffusion capacitance. Neglect wire capacitance for now (though it could account for a large fraction of total power). Estimate the switching power when operating at 1 GHz.

2. Consider the system-on-chip from the previous problem. Subthreshold leakage for OFF devices is 100 nA/μm for low-threshold devices and 10 nA/μm for high-threshold devices. Gate leakage is 5 nA/μm. Junction leakage is negligible. Memories use low-leakage devices everywhere. Logic uses low-leakage devices in all but 5% of the paths that are most critical for performance. Estimate the static power consumption.

3. You are synthesizing a chip composed of random logic with an average activity factor of 0.1. You use a standard cell process with an average switching capacitance of 450 pF/mm^2. Estimate the dynamic power consumption of your chip if it has an area of 70 mm^2 and runs at 450 MHz at VDD = 0.9 V.
4. You are manufacturing a chip composed of random logic and memory units with average activity factors of 0.1 & 0.05 respectively. You use a standard cell process with an average switching capacitance of 450 pF/mm^2. Estimate the dynamic power consumption of your chip if it has an area of 200 mm^2 of which 60% is occupied by the logic circuit and runs at 450 MHz at VDD = 0.9 V.

5. You are considering lowering VDD to try to save power in a static CMOS gate. You will also scale Vt proportionally to maintain performance. Will dynamic power consumption go up or down?
Determine the activity factor for the signal shown. The clock rate is 1 GHz.