FOURTH EDITION

CMOS VLSI DESIGN

A CIRCUITS AND SYSTEMS PERSPECTIVE
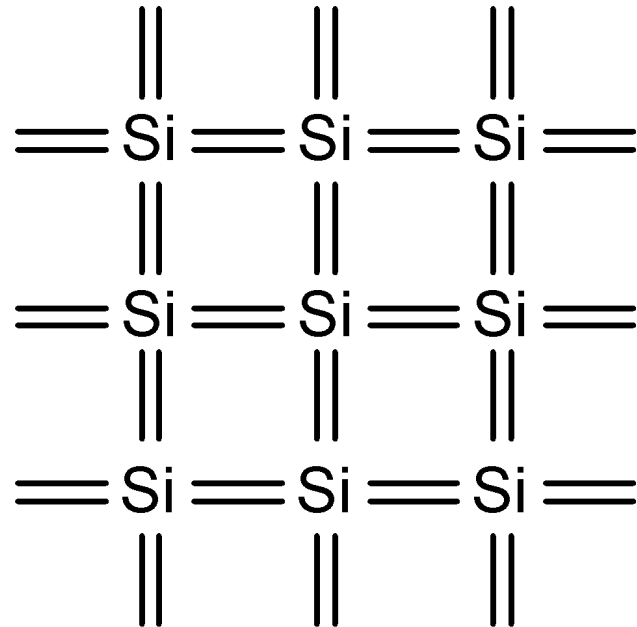
**NEIL H. E. WESTE**   **DAVID MONEY HARRIS**

Lecture 9: Fabrication

Silicon Lattice

❑ Transistors are built on a silicon substrate

❑ Silicon is a Group IV material

❑ Forms crystal lattice with bonds to four neighbors

$$\begin{array}{ccc}
\| & \| & \| \\
=\mathrm{Si}= & \mathrm{Si}= & \mathrm{Si}= \\
\| & \| & \| \\
=\mathrm{Si}= & \mathrm{Si}= & \mathrm{Si}= \\
\| & \| & \| \\
=\mathrm{Si}= & \mathrm{Si}= & \mathrm{Si}= \\
\| & \| & \|
\end{array}$$

Dopants

❑ Silicon is a semiconductor

❑ Pure silicon has no free carriers and conducts poorly

❑ Adding dopants increases the conductivity

❑ Group V: extra electron (n-type)
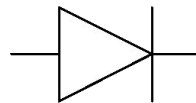
❑ Group III: missing electron, called hole (p-type)
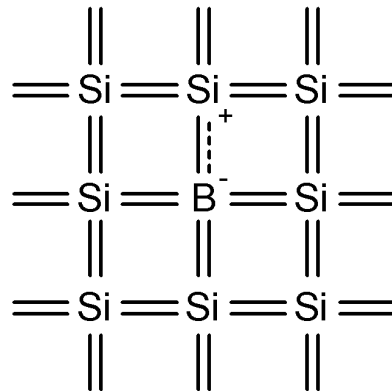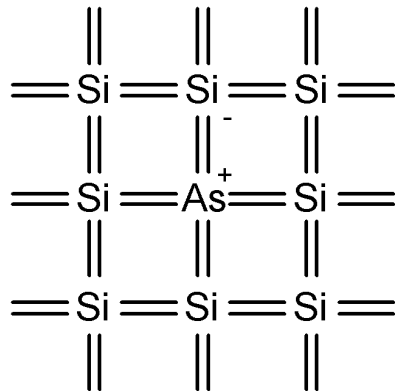
p-n Junctions

❑ A junction between p-type and n-type semiconductor forms a diode.

❑ Current flows only in one direction
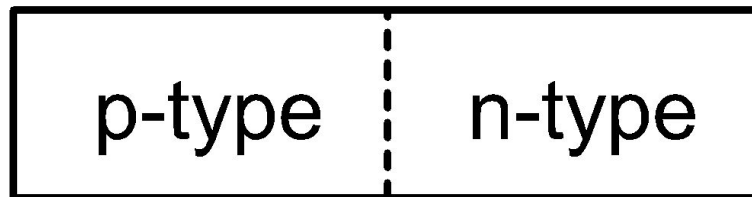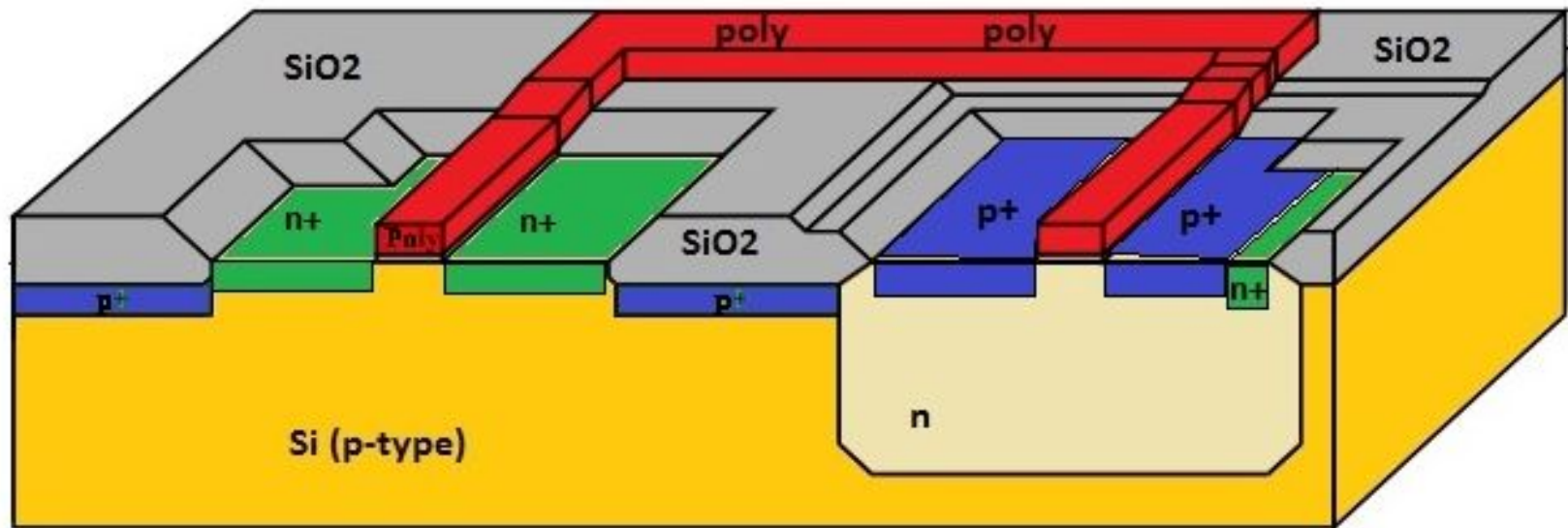
Cross sectional View

3D view

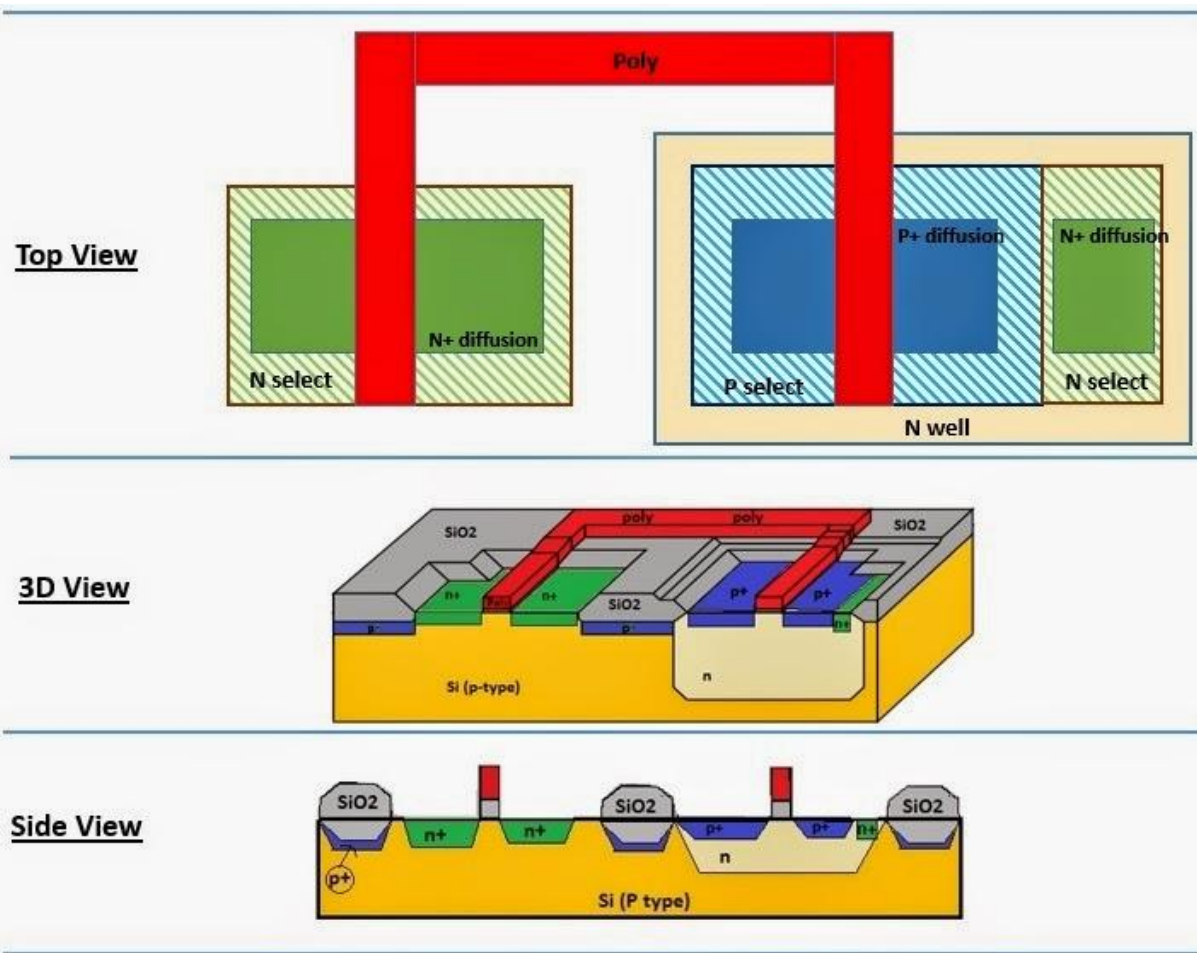**Section**
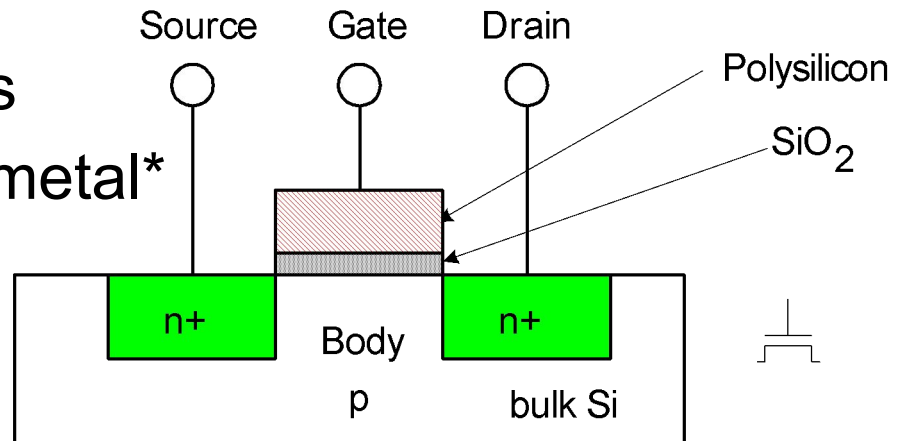
Cross-sectional view

CMOS 3D View

3D view of silicon wafer. Now we have PMOS and NMOS Device.

CMOS Inverter

nMOS Transistor

❑ Four terminals: gate, source, drain, body

❑ Gate – oxide – body stack looks like a capacitor

   – Gate and body are conductors

   – SiO_2 (oxide) is a very good insulator

   – Called metal – oxide – semiconductor (MOS) capacitor

   – Even though gate is no longer made of metal*

* Metal gates are returning today!

Source   Gate   Drain

Polysilicon

SiO_2

n+   n+

Body

p   bulk Si

pMOS Transistor

❑ Similar, but doping and voltages reversed
- – Body tied to high voltage (V_{DD})
- – Gate low: transistor ON
- – Gate high: transistor OFF
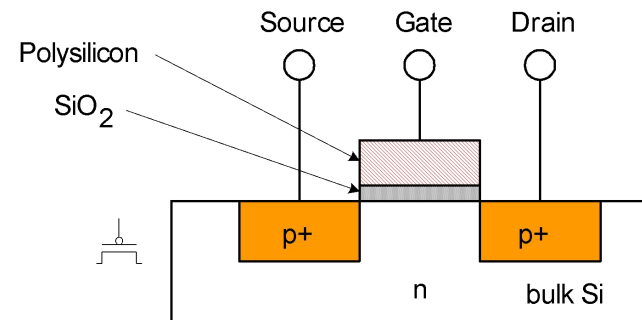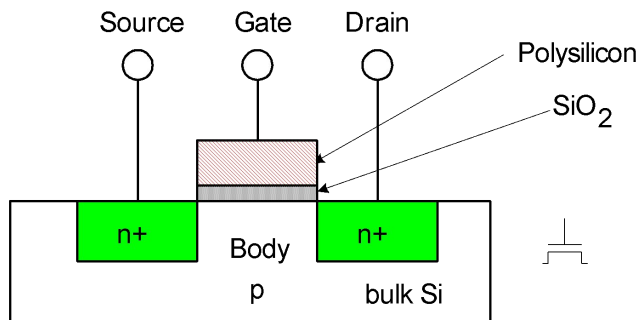- – Bubble indicates inverted behavior
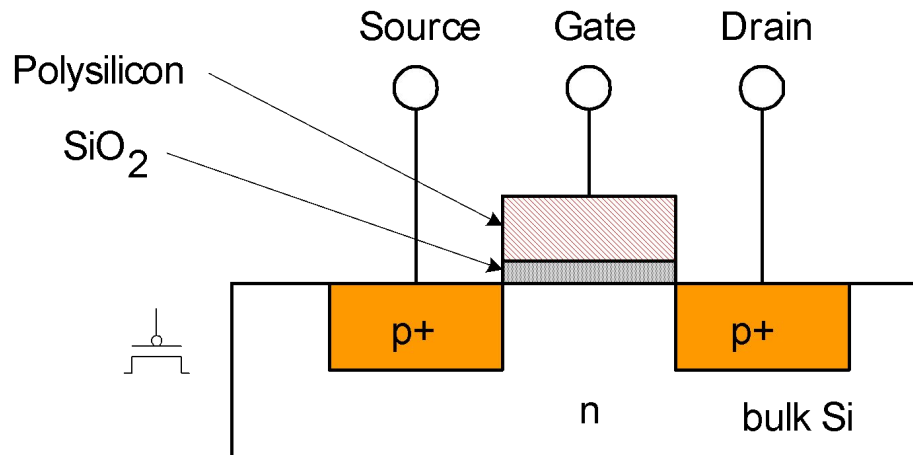
CMOS Fabrication

❑   CMOS transistors are fabricated on silicon wafer

❑   Lithography process similar to printing press

❑   On each step, different materials are deposited or etched

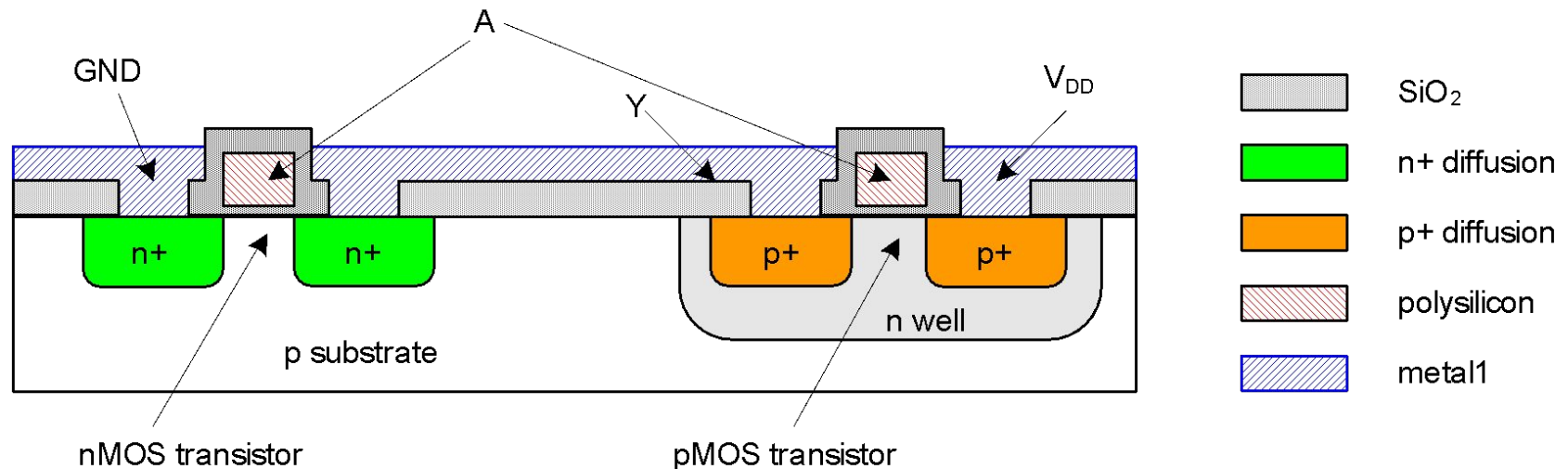❑   Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Intuition (1)

Intuition (2)

Inverter Cross-section

❑ Typically use p-type substrate for nMOS transistors
❑ Requires n-well for body of pMOS transistors
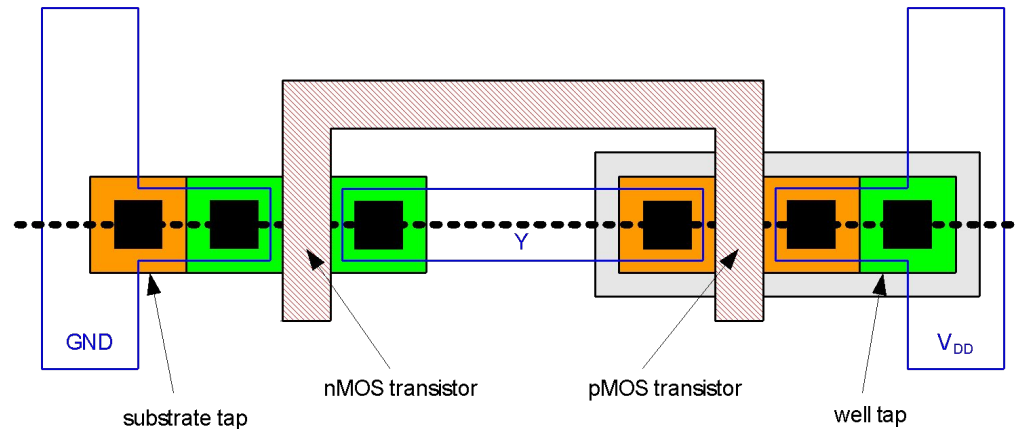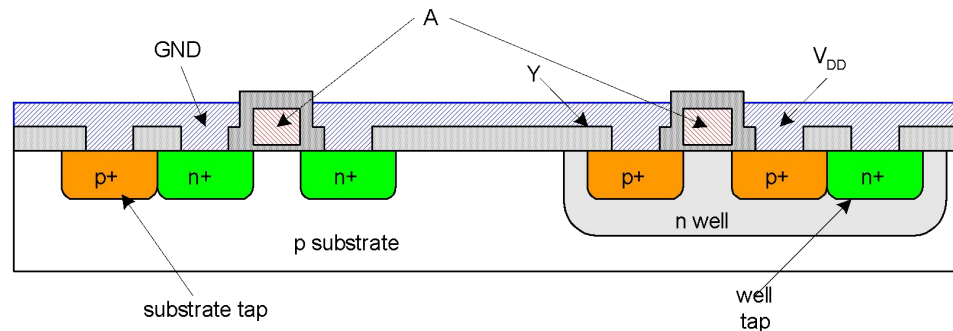
CMOS Inverter
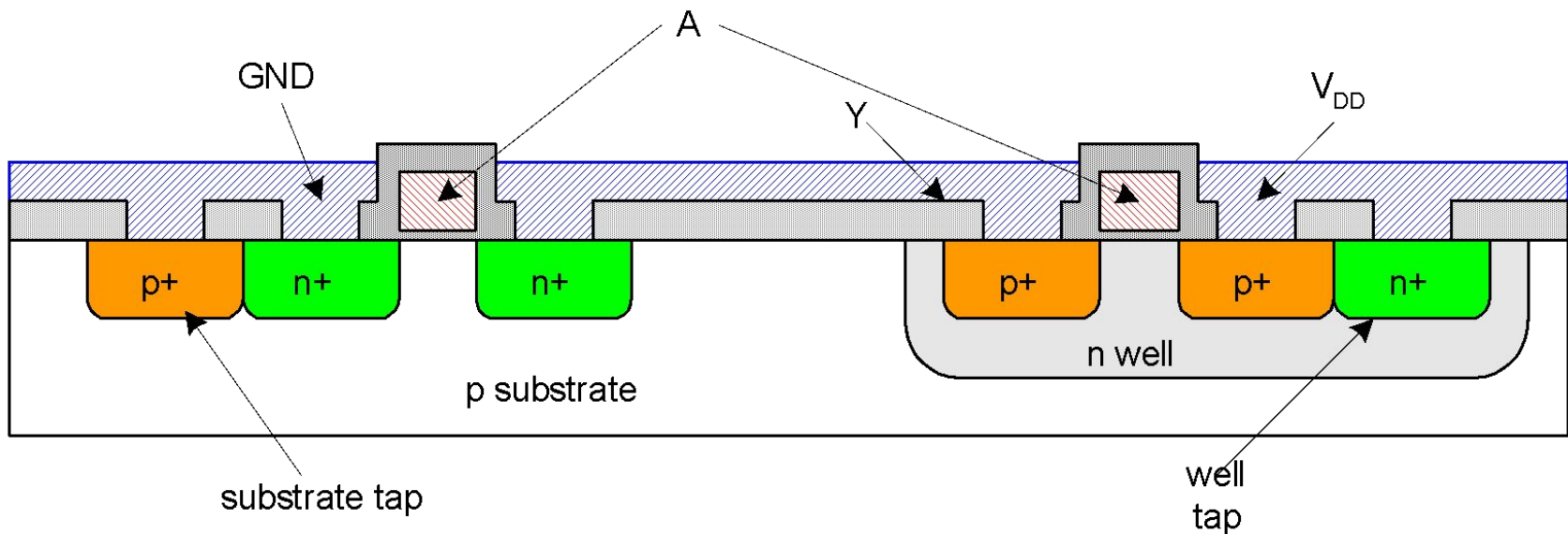

Figure (a): Top view

Figure (b): Cross-section about the dashed line

Well and Substrate Taps
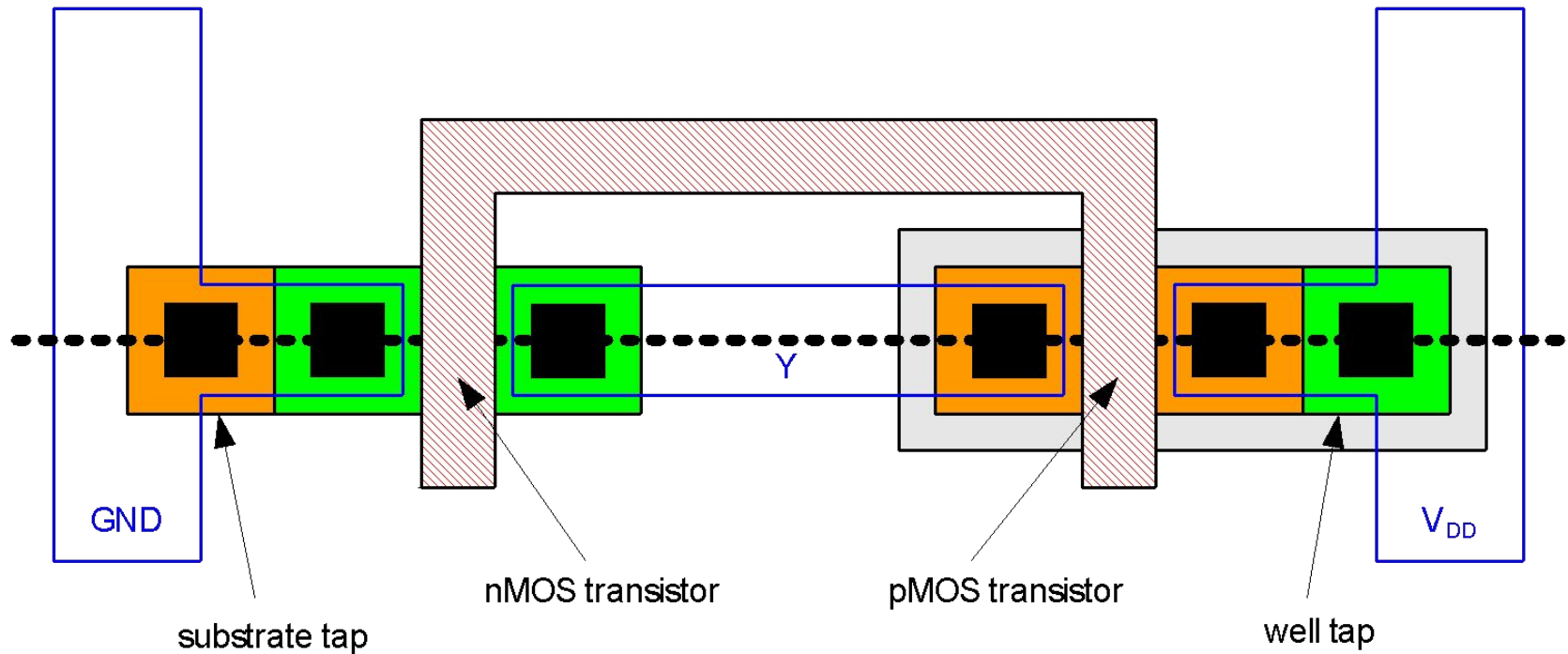
❑   Substrate must be tied to GND and n-well to V_{DD}

❑   Metal to lightly-doped semiconductor forms poor connection called Shottky Diode

❑   Use heavily doped well and substrate contacts / taps

Inverter Mask Set

❑ Transistors and wires are defined by *masks*

❑ Cross-section taken along dashed line

GND

Y

V_{DD}

substrate tap

nMOS transistor

pMOS transistor

well tap

Detailed Mask Views

❑ Six masks
  – n-well
  – Polysilicon
  – n+ diffusion
  – p+ diffusion
  – Contact
  – Metal

n well

Polysilicon

n+ Diffusion

p+ Diffusion

Contact

Metal
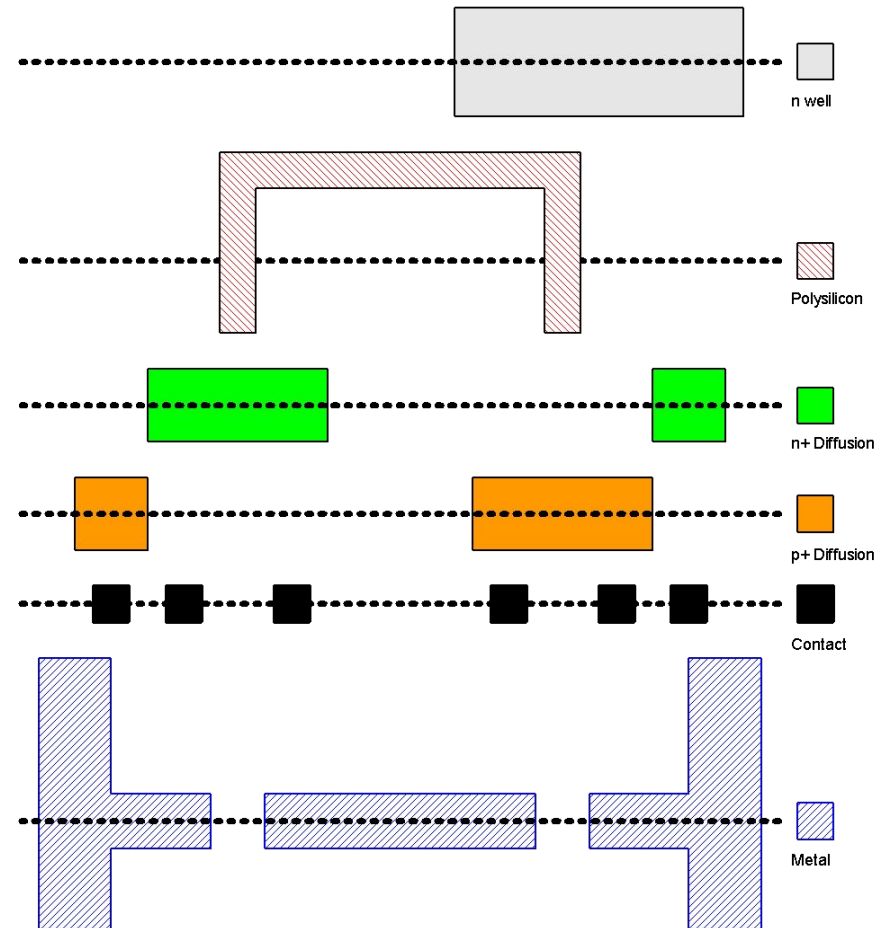
Fabrication

❏ Chips are built in huge factories called fabs

❏ Contain clean rooms as large as football fields

Courtesy of International
Business Machines Corporation.
Unauthorized use not permitted.

Fabrication Steps

❑ Start with blank wafer

❑ Build inverter from the bottom up

❑ First step will be to form the n-well

– Cover wafer with protective layer of SiO_2 (oxide)

– Remove layer where n-well should be built

– Implant or diffuse n dopants into exposed wafer

– Strip off SiO_2

p substrate

Oxidation

❑ Grow SiO_2 on top of Si wafer
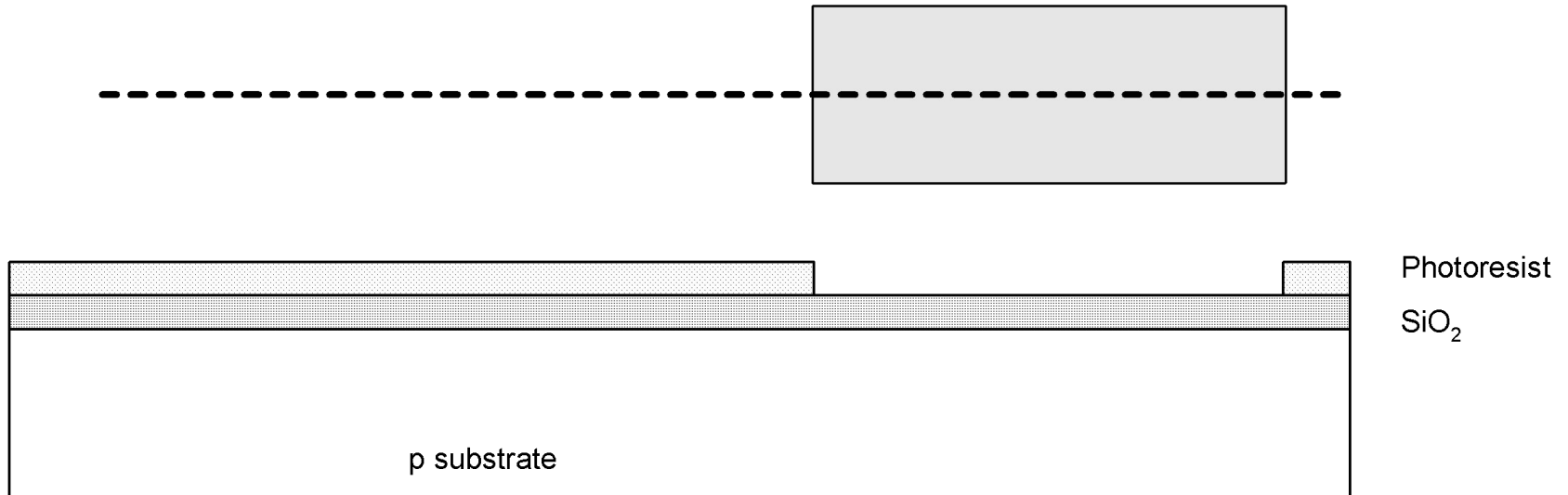 – 900 – 1200 C with H_2O or O_2 in oxidation furnace

SiO_2

p substrate
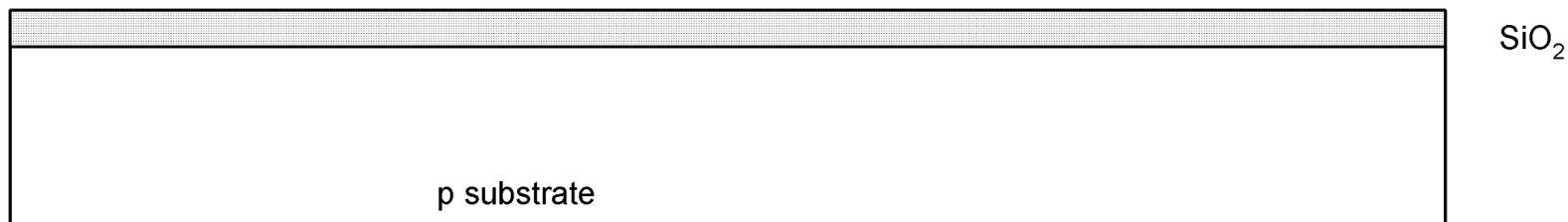
Photoresist

❑ Spin on photoresist
- – Photoresist is a light-sensitive organic polymer
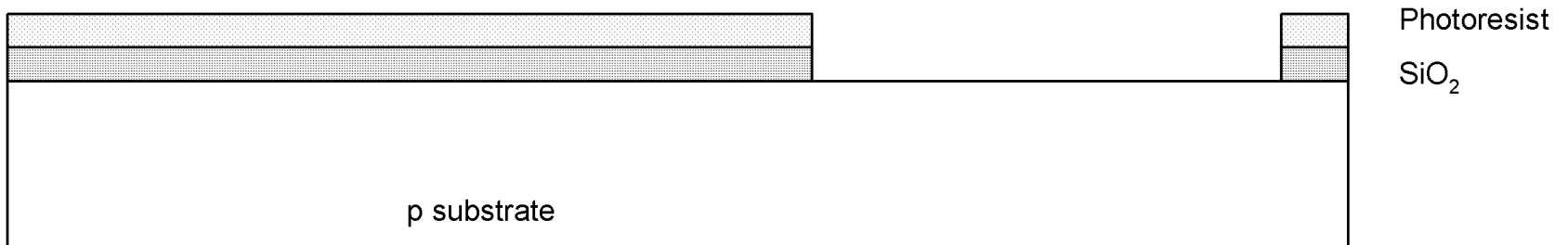- – Softens where exposed to light

Photoresist

SiO$_2$

p substrate

Lithography

❑ Expose photoresist through n-well mask

❑ Strip off exposed photoresist

Photoresist

SiO$_2$

p substrate

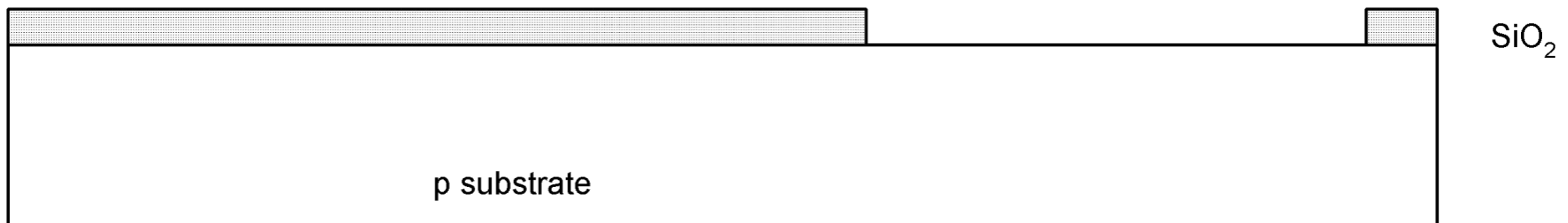# Etch

❑ Etch oxide with hydrofluoric acid (HF)
  – Seeps through skin and eats bone; nasty stuff!!!
❑ Only attacks oxide where resist has been exposed

Photoresist

SiO_2

p substrate

Strip Photoresist

❑ Strip off remaining photoresist
  – Use mixture of acids called piranha etch
❑ Necessary so resist doesn't melt in next step

SiO_2

p substrate

n-well

❑   n-well is formed with diffusion or ion implantation

❑   Diffusion

–   Place wafer in furnace with arsenic gas

–   Heat until As atoms diffuse into exposed Si

❑   Ion Implantation

–   Blast wafer with beam of As ions

–   Ions blocked by SiO_2, only enter exposed Si

SiO_2
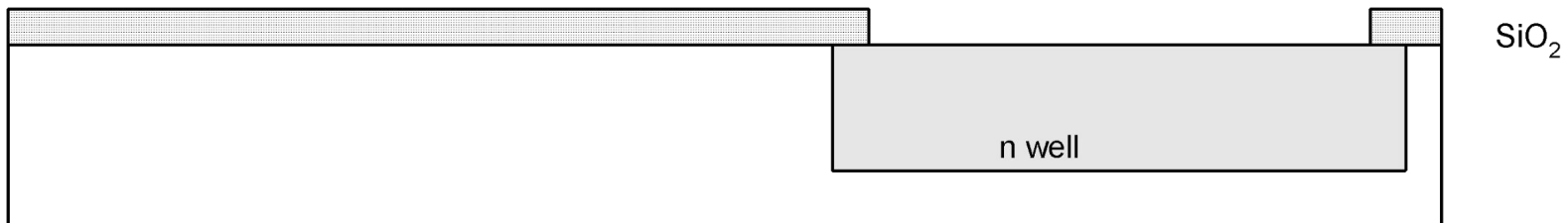
n well

Strip Oxide

❑   Strip off the remaining oxide using HF

❑   Back to bare wafer with n-well

❑   Subsequent steps involve similar series of steps

n well

p substrate

Polysilicon

❑ Deposit very thin layer of gate oxide
  – < 20 Å (6-7 atomic layers)
❑ Chemical Vapor Deposition (CVD) of silicon layer
  – Place wafer in furnace with Silane gas (SiH_4)
  – Forms many small crystals called polysilicon
 – Heavily doped to be good conductor

Polysilicon
Thin gate oxide

n well

p substrate
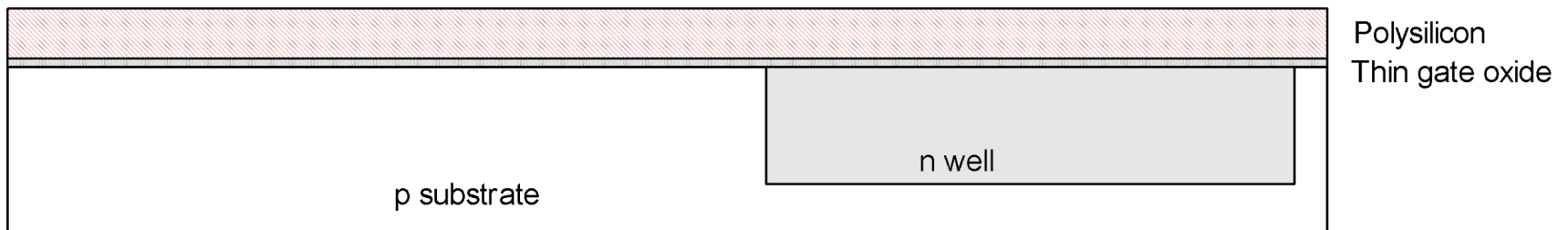
Polysilicon Patterning

❑ Use same lithography process to pattern polysilicon

Polysilicon

Polysilicon
Thin gate oxide

n well

p substrate
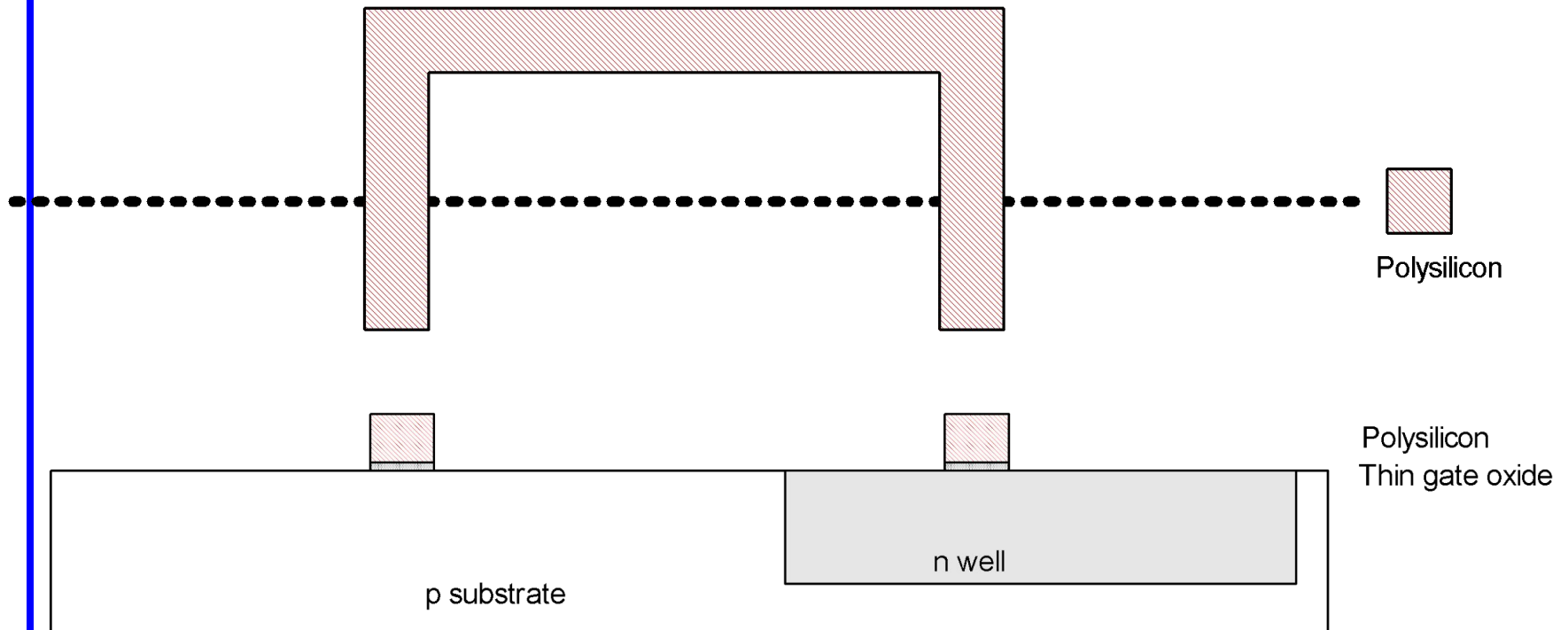
Self-Aligned Process

❑ Use oxide and masking to expose where n+ dopants should be diffused or implanted

❑ N-diffusion forms nMOS source, drain, and n-well contact

p substrate

n well
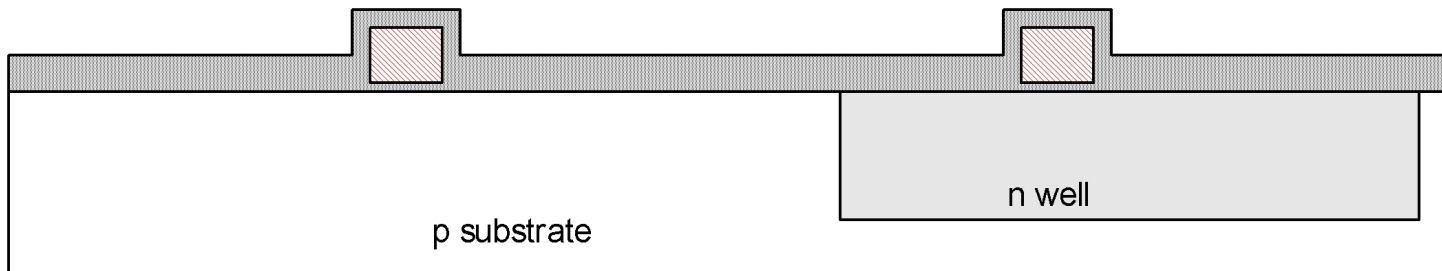
N-diffusion

❑ Pattern oxide and form n+ regions

❑ *Self-aligned process* where gate blocks diffusion

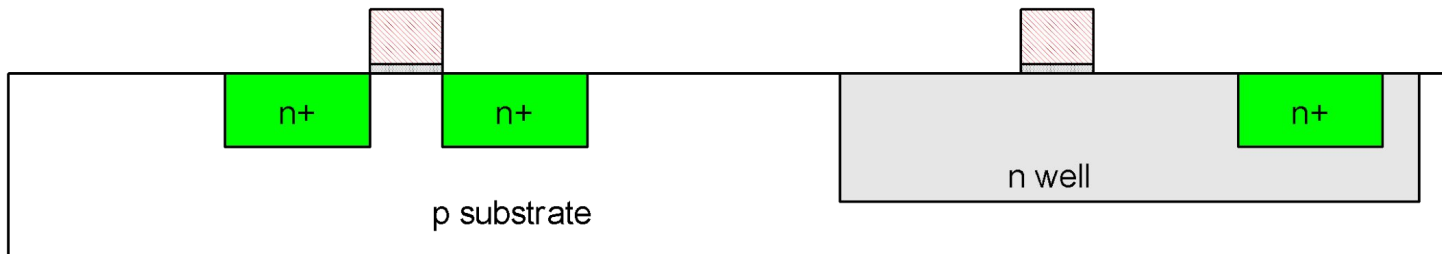❑ Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing

n+ Diffusion

n well

p substrate
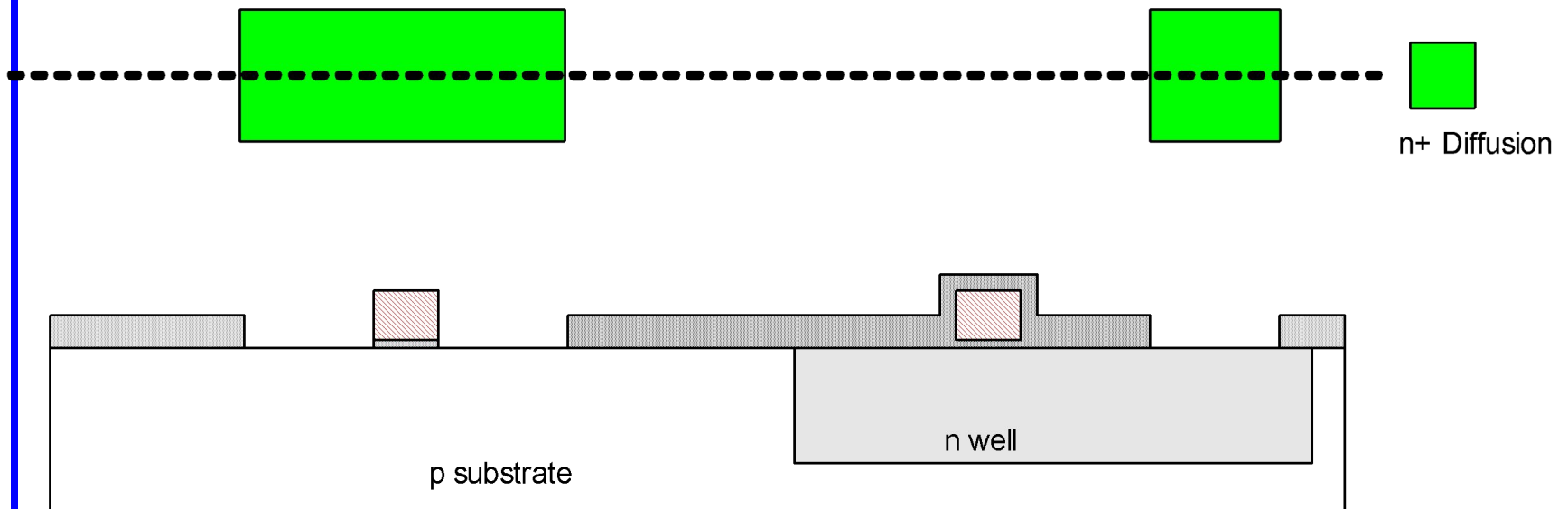
N-diffusion cont.

❏ Historically dopants were diffused

❏ Usually ion implantation today

❏ But regions are still called diffusion

n+   n+   n+
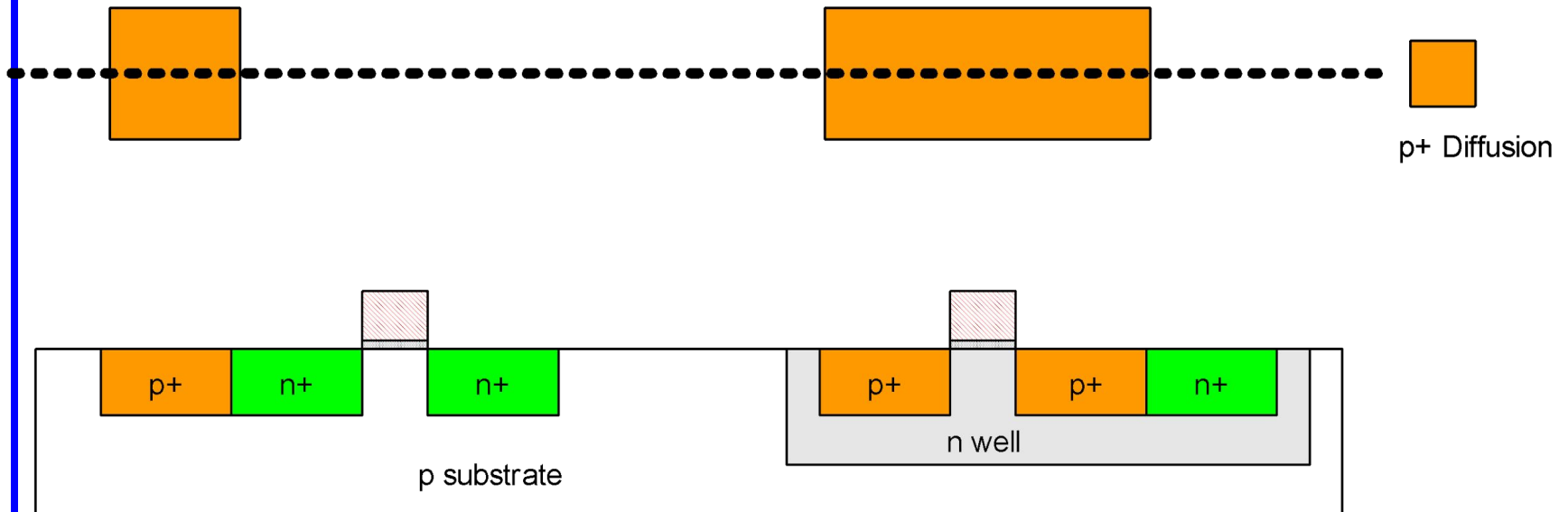
n well
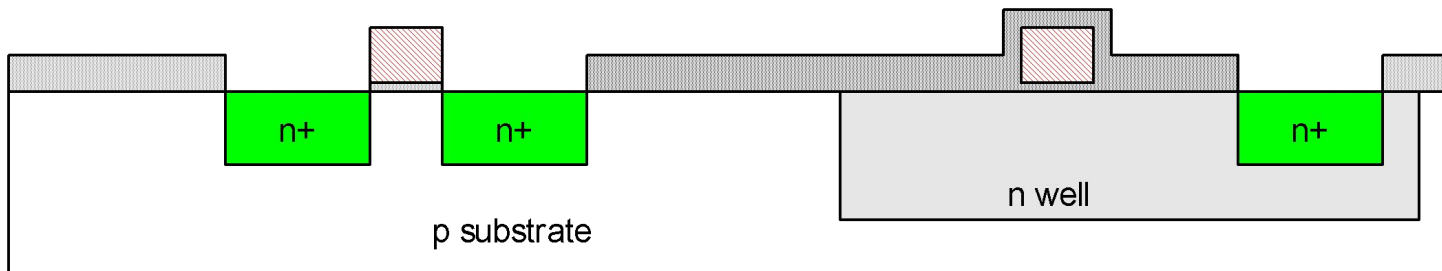
p substrate

# N-diffusion cont.

❑ Strip off oxide to complete patterning step

P-Diffusion

❑ Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact

p+ Diffusion

p+ | n+ | n+

p+ | p+ | n+

n well

p substrate

Contacts

❑ Now we need to wire together the devices
❑ Cover chip with thick field oxide
❑ Etch oxide where contact cuts are needed

Contact

Thick field oxide

| p+ | n+ | | n+ | | | p+ | | p+ | n+ |

n well

p substrate
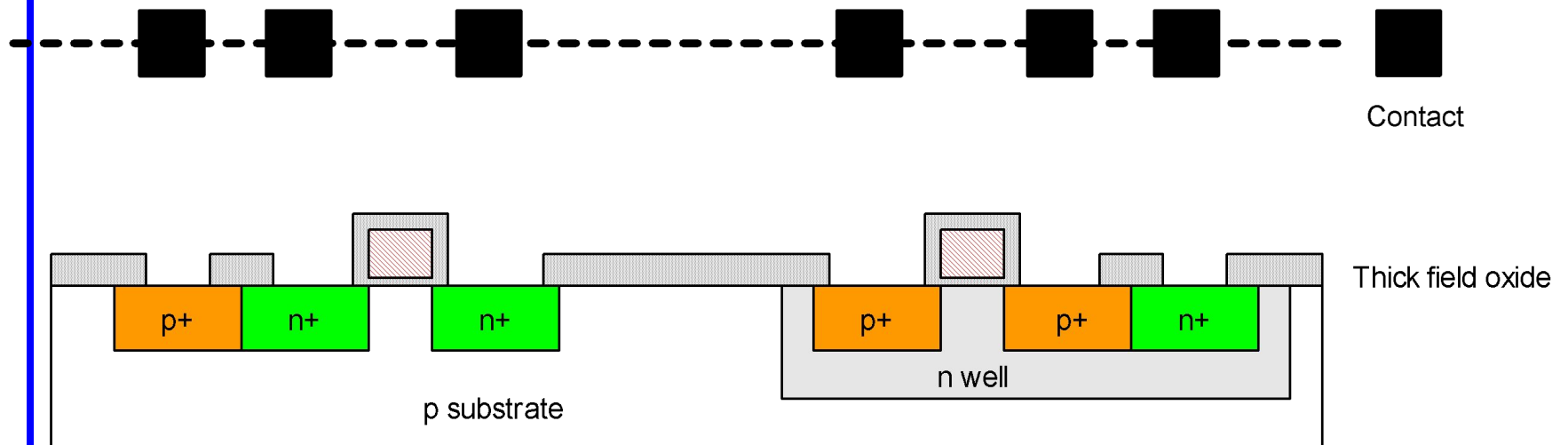
Metalization

❑ Sputter on aluminum over whole wafer
❑ Pattern to remove excess metal, leaving wires

Metal

Metal
Thick field oxide

p+   n+   n+   p+   p+   n+

n well

p substrate
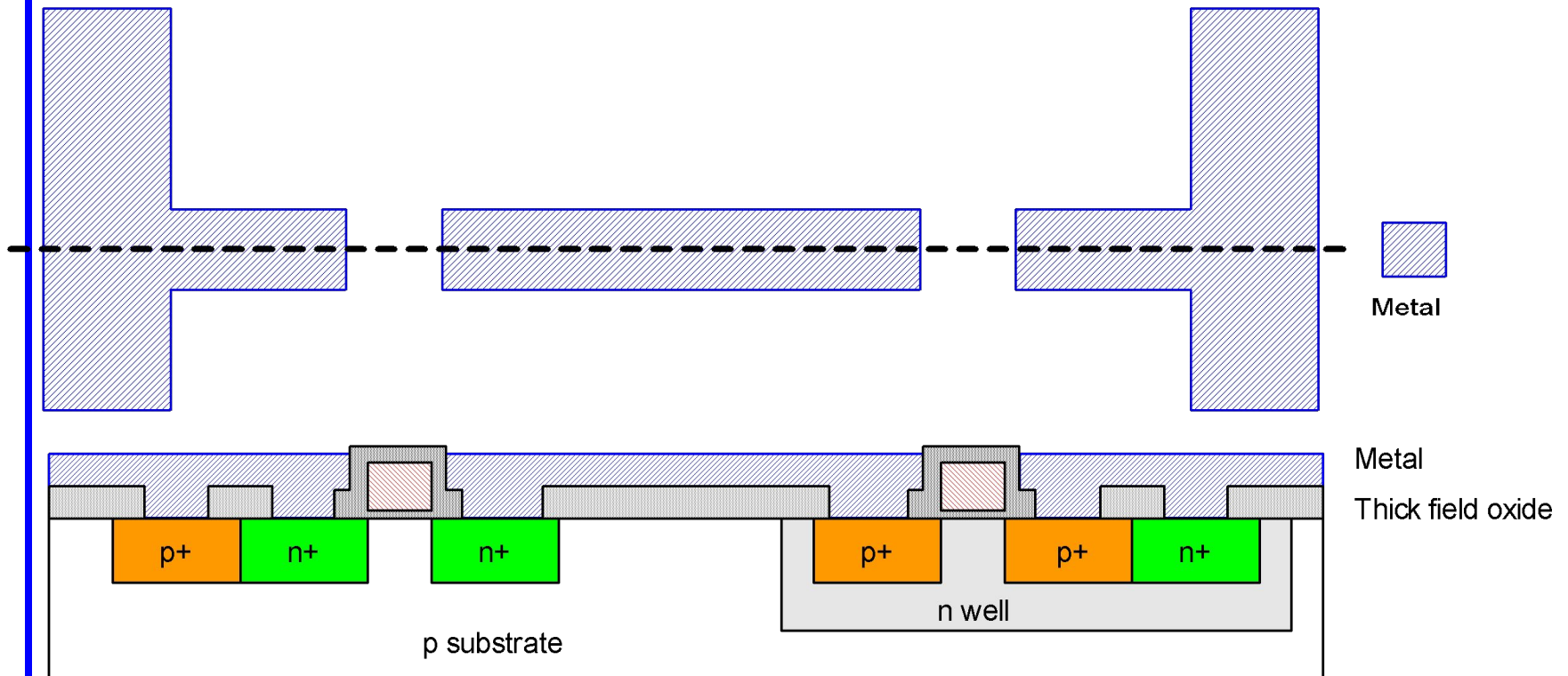
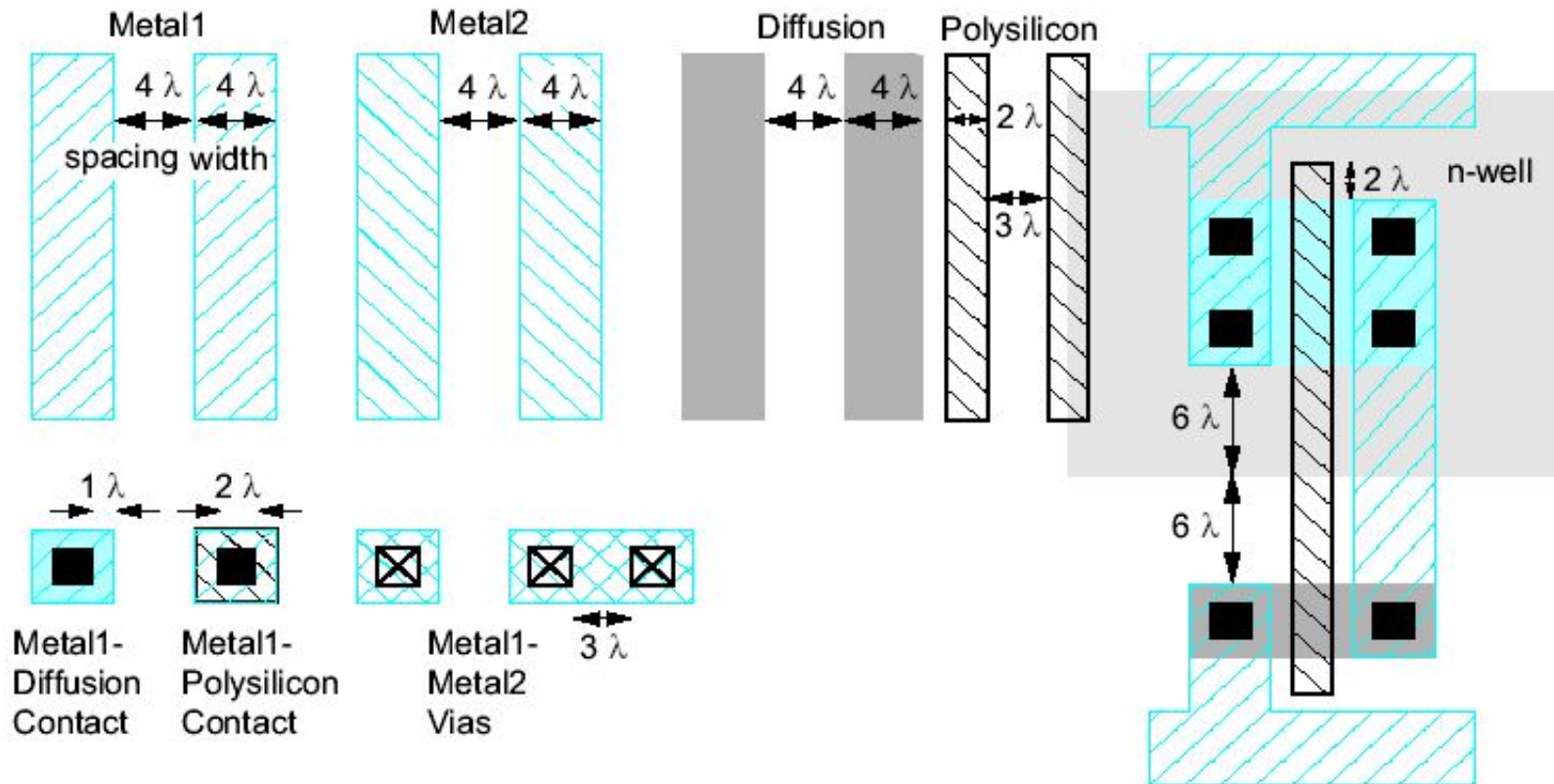# Layout

❑ Chips are specified with set of masks

❑ Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)

❑ Feature size f = distance between source and drain
  – Set by minimum width of polysilicon

❑ Feature size improves 30% every 3 years or so

❑ Normalize for feature size when describing design rules

❑ Express rules in terms of $\lambda = f/2$
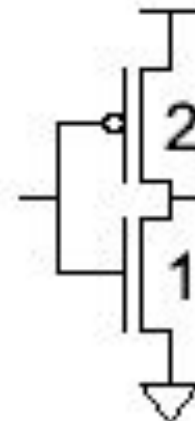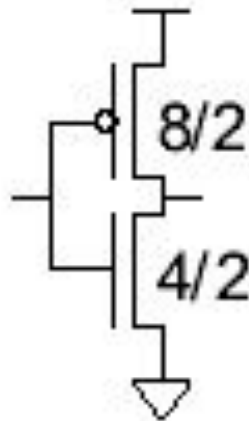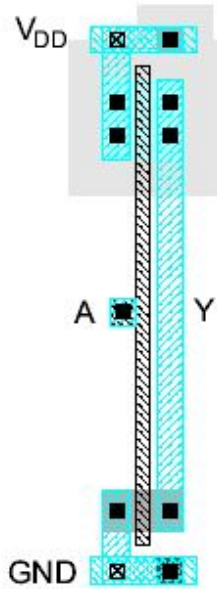 – E.g. $\lambda = 0.3\ \mu m$ in $0.6\ \mu m$ process

Simplified Design Rules

❑ Conservative rules to get you started

Inverter Layout

❑ Transistor dimensions specified as Width / Length
  – Minimum size is 4λ / 2λ, sometimes called 1 unit
  – In f = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long

Summary

❑ MOS transistors are stacks of gate, oxide, silicon

❑ Act as electrically controlled switches

❑ Build logic gates out of switches

❑ Draw masks to specify layout of transistors

❑ Now you know everything necessary to start designing schematics and layout for a simple chip!