Power

Q1.

TSMC are planning to design a new chip in a $1.1\,V,\ 22\,nm\ (\lambda = 10\,nm)$ technology which has 200 million transistors, of which 25% are used for building logic gates and the rest are used for memory arrays. The average **logic transistor** width is **6λ** and the average **memory transistor** width is **4λ**. Other information of the device is given below

i. The gate and diffusion capacitances are $1.2\ fF/\mu m$ and $0.6\ fF/\mu m$
ii. The system clock frequency is $3.5\,GHz$. In every $100\,clock\,cycles$, the number of **switching** for the **logic** and **memory** transistors are 10 and 2 respectively.
iii. For both of the transistors, each transistor contributes the gate leakage, junction leakage and subthreshold leakage currents of approximately $20\,pA,\ 15\,pA$ **and** $25\,pA$ respectively. The total short circuit power is $0.05\,W$. The total accepted power consumption is $3\,W$.

(a)	**Discuss** in brief how the **short circuit power** and **subthreshold leakage power** dissipate in the device.	[3]
(b)	**Calculate** the **activity factor** and **switching frequency** for each type of transistors.	[2]
(c)	**Calculate** the **dynamic power** and **static power** consumption.	[6]
(d)	**Verify** the statement that "By lowering the device **speed** by 10% we can meet the power consumption limit".	[4]