Pontifícia Universidade Católica do Rio Grande do Sul

Faculdade de Engenharia

Programa de Graduação em Engenharia da Computação

LAB3 – Layout de um Inversor utilizando Cadence

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Porto Alegre

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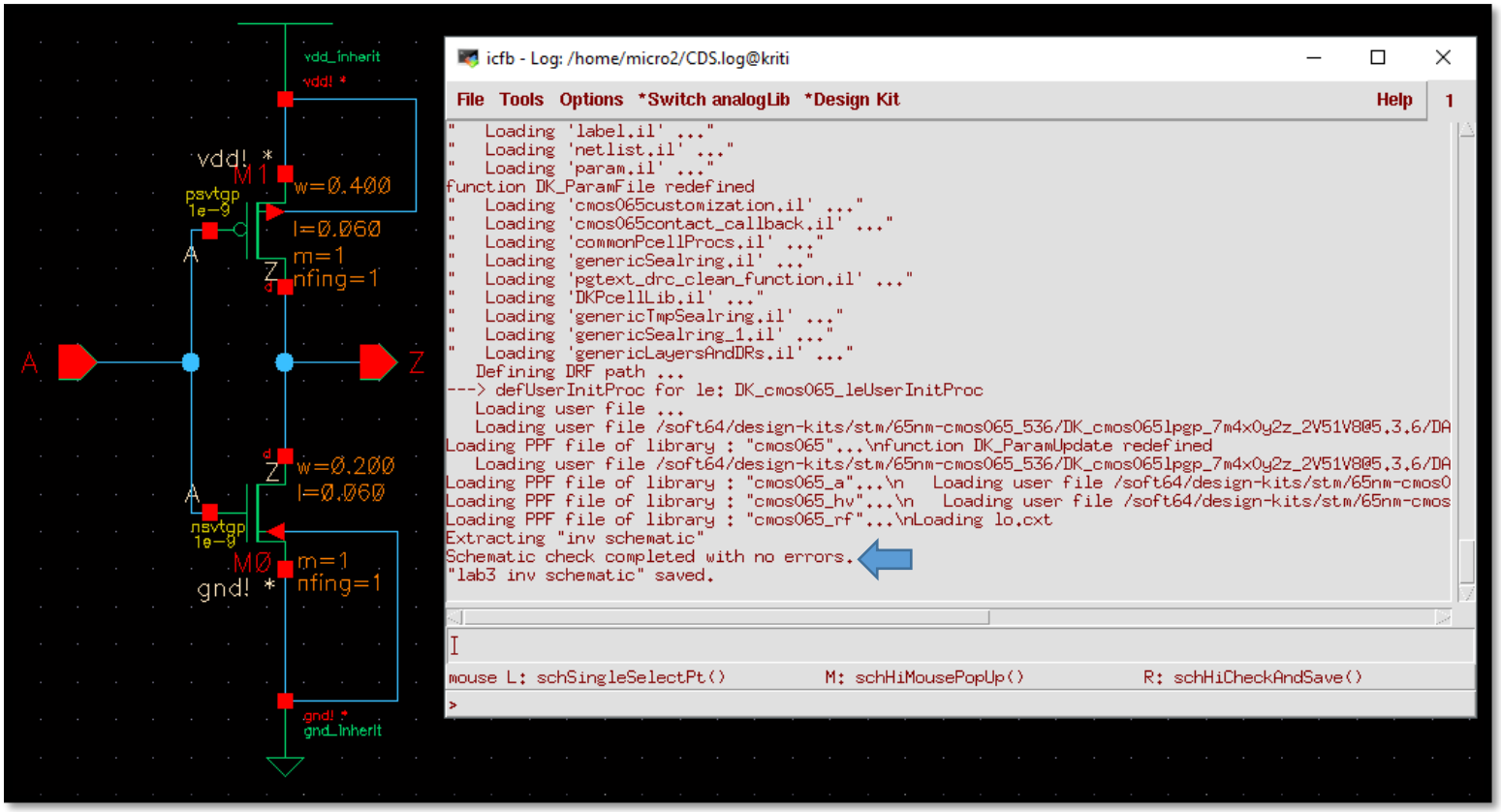
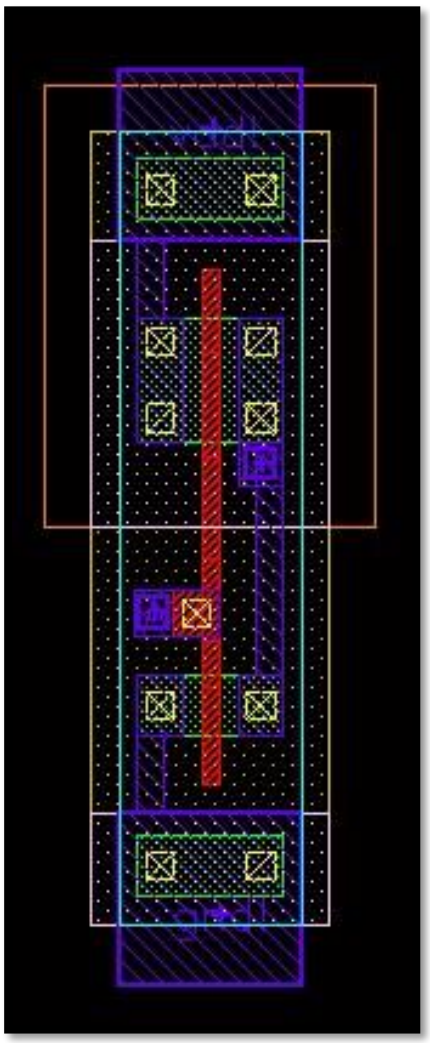
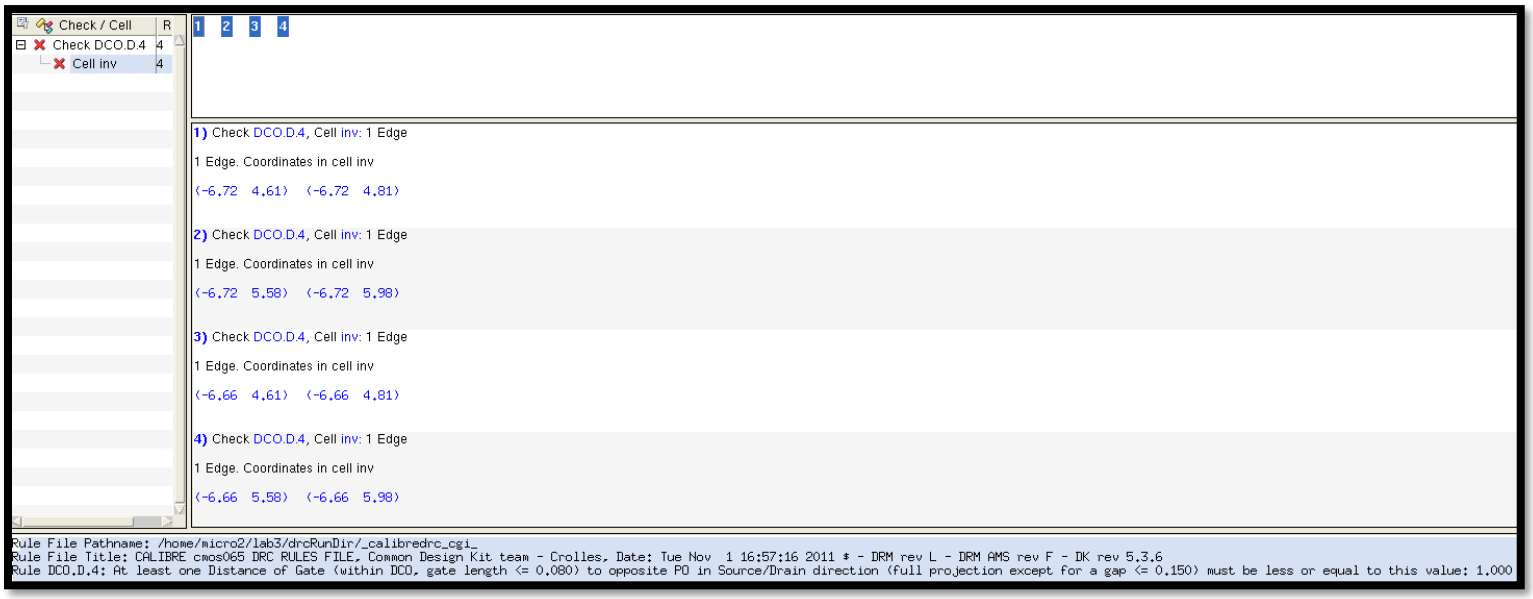
1) Layout do Esquemático do Inversor:



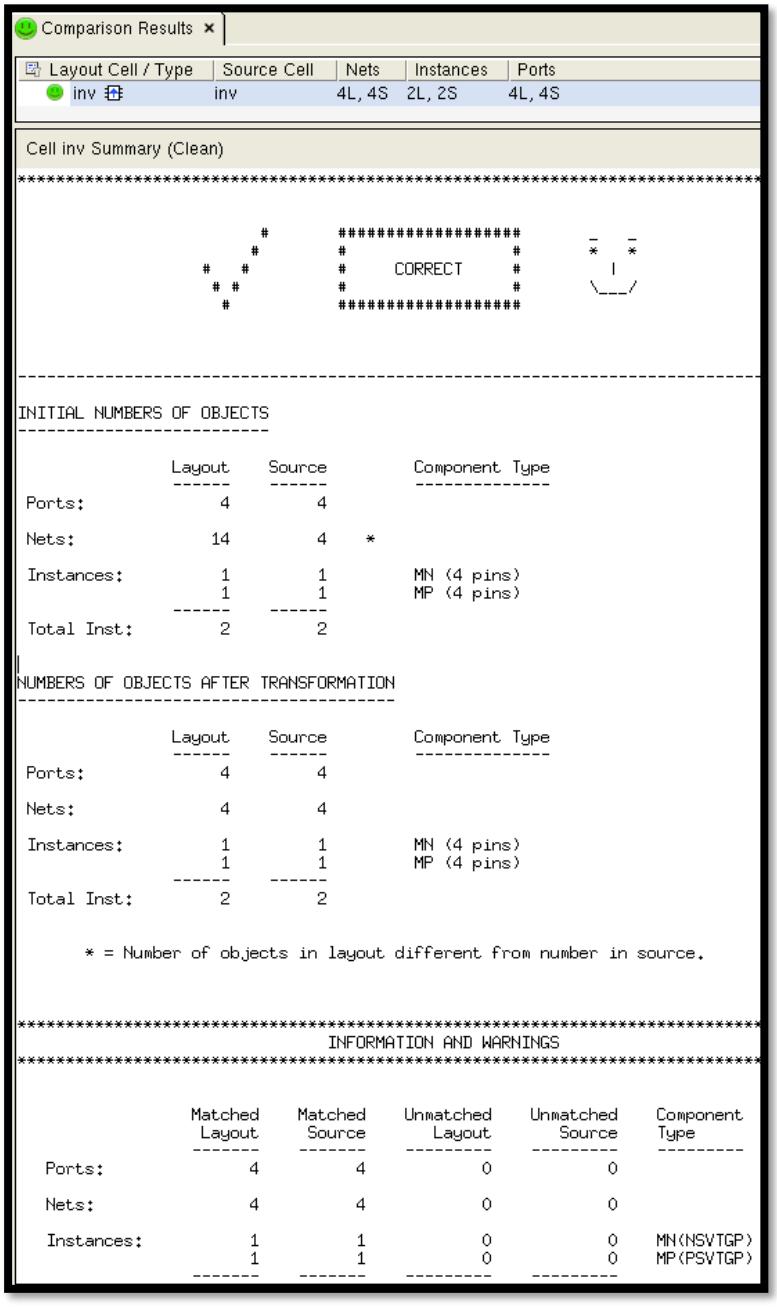
2) Layout do Inversor:



3) Relatório do DRC:



4) Relatório do LVS:



5) Relatório da Extração Elétrica e Netlist Extraído:

inv

No.	Layout Net	Source Net	CC Total (F)	C+CC Total (F)
1	A	A	2.79195E-16	2.79195E-16
2	gnd!	gnd!	2.47282E-16	2.47282E-16
3	vdd!	vdd!	1.83504E-16	1.83504E-16
4	Z	Z	2.39401E-16	2.39401E-16

- inv.pex.spi:

```
* File: inv.pex.spi
* Created: Sun Sep  4 16:51:10 2016
* Program "Calibre xRC"
* Version "v2011.3_29.20"
*
.subckt inv  A Z
*
XM1 Z A vdd! vdd! psvtgp L=0.06 W=0.4 NFING=1 M=1 AS=0.0864 AD=0.0864 PS=0.832
+ PD=0.832 PO2ACT=0.21 NGCON=1 lpe=1
XM0 Z A gnd! gnd! nsvtgp L=0.06 W=0.2 NFING=1 M=1 AS=0.0434 AD=0.0434 PS=0.634
+ PD=0.634 PO2ACT=0.21 NGCON=1 lpe=1
X2_noxref gnd! vdd! dnwps  AREA=1.566 PJ=5.06
*
.include "inv.pex.spi.inv.pxi"
*
.ends
*
*
```

- inv.pex.spi.inv.pxi

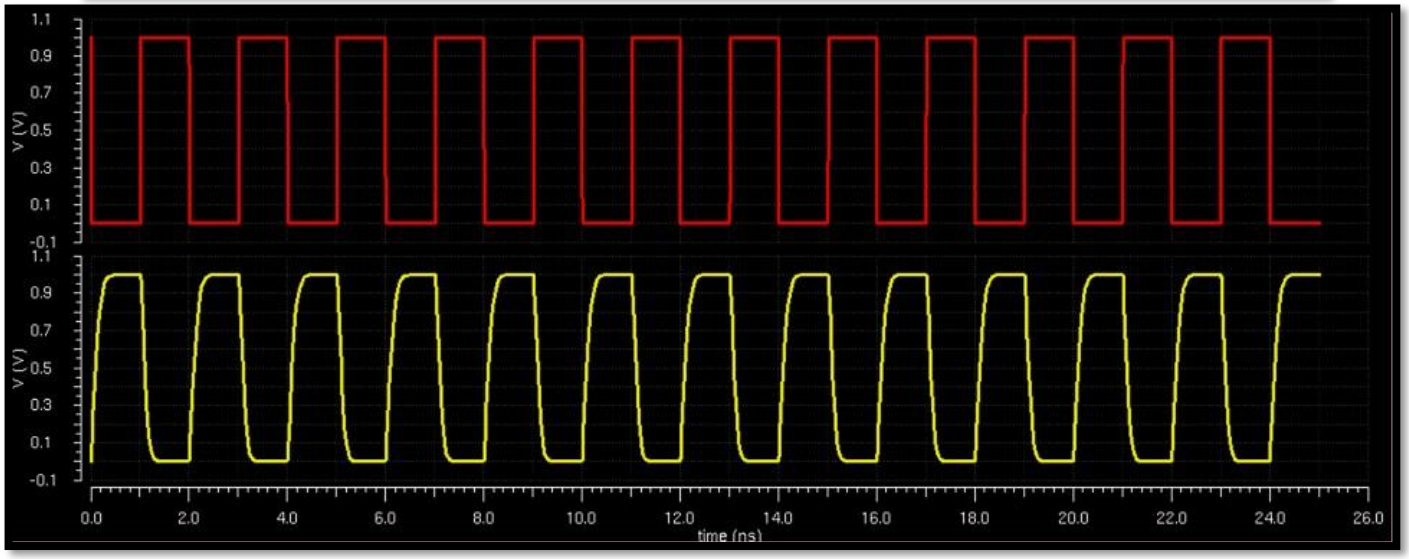
```
* File: inv.pex.spi.inv.pxi
* Created: Sun Sep  4 16:51:10 2016
*
cc_1 A gnd! 0.123346f
cc_2 A vdd! 0.0667007f
cc_3 A Z 0.0891483f
cc_4 gnd! vdd! 0.045243f
cc_5 gnd! Z 0.0786928f
cc_6 vdd! Z 0.0715603f
```

- inv.src.net

```
* Library Name:  lab3
* Top Cell Name: inv
* View Name:     schematic
* Netlisted on:  Sep  4 16:50:46 2016
********************************************************************************

*.EQUATION
*.SCALE METER
*.MEGA
.PARAM

*.GLOBAL gnd!
+        vdd!

*.PIN gnd!
*+    vdd!

********************************************************************************
* Library Name: lab3
* Cell Name:    inv
* View Name:    schematic
********************************************************************************

.SUBCKT inv A Z
*.PININFO A:I Z:O
MM1 Z A vdd! vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MM0 Z A gnd! gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
.ENDS
```

6) Simulação Elétrica:

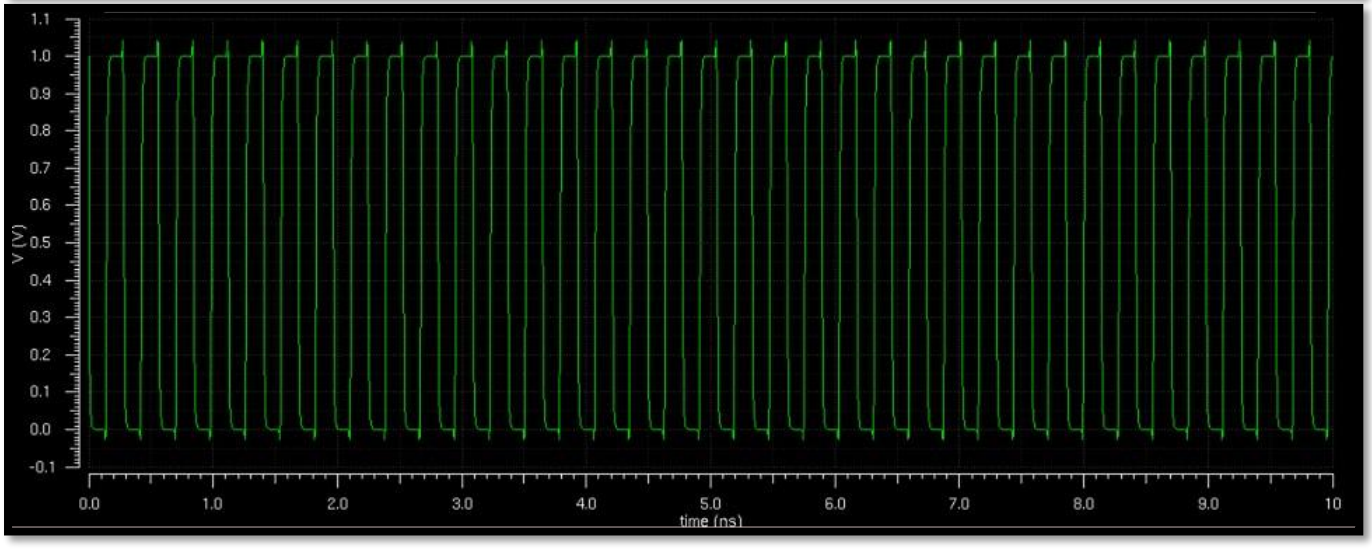
```
Exported variables from results directory:  ./inv.raw/

date                :  5:14:24 PM, Sun Sep 4, 2016
design              :  * inversor - simulação do circuito extraído do layout projetado
simulator           :  spectre
version             :  15.1.0.257


Measurement Name    :  transient1
Analysis Type       :  tran
td              = 84.6126
tdescida        = 8.46126e-11
ts              = 91.9674
tsubida         = 9.19674e-11
```



Simulação do Anel do Inversor:

```
Exported variables from results directory:  ./anel.raw/

date                :  5:17:04 PM, Sun Sep 4, 2016
design              :  * inversores em anel para cálculo de frequência com inversor extraído
simulator           :  spectre
version             :  15.1.0.257


Measurement Name    :  transient1
Analysis Type       :  tran
freq_ghz        = 3.56484
periodo         = 0.280517
tf              = 6.28216e-12
tr              = 1.2419e-11
```

Frequência: freq_ghz = 3.56484

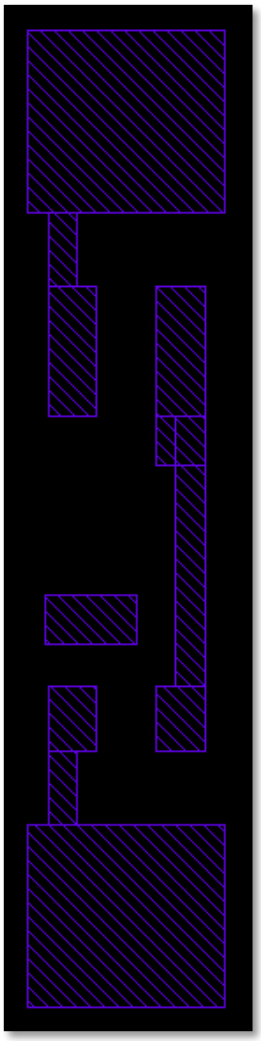


7) Layout da View Abstract:

- Inv.lef:

```
#******
# Preview export LEF
#
#    Preview sub-version 5.10.41_USR5.90.69
#
# REF LIBS: lab3
# TECH LIB NAME: cmos065
# TECH FILE NAME: techfile.cds
#******

VERSION 5.5 ;
NAMESCASESENSITIVE ON ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;

UNITS
    DATABASE MICRONS 1000  ;
END UNITS

 MANUFACTURINGGRID    0.005000 ;
SITE CORE
    SYMMETRY Y  ;
    CLASS CORE  ;
    SIZE 0.200 BY 2.600 ;
END CORE
```

1



```
MACRO inv
    CLASS CORE ;
    FOREIGN inv 0.21 0.39 ;
    ORIGIN -0.210 -0.390 ;
    SIZE 0.600 BY 2.600 ;
    SYMMETRY X Y ;
    SITE CORE ;
    PIN A
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT  0.260 1.305 0.540 1.455 ;
        END
    END A
    PIN Z
        DIRECTION OUTPUT ;
        PORT
        LAYER M1 ;
        RECT  0.600 1.855 0.750 2.405 ;
        RECT  0.660 0.975 0.750 2.405 ;
        RECT  0.600 0.975 0.750 1.175 ;
        END
    END Z
    PIN vdd!
        DIRECTION INOUT ;
        USE POWER ;
        SHAPE ABUTMENT ;
        PORT
        LAYER M1 ;
        RECT  0.210 2.630 0.810 3.190 ;
        RECT  0.270 2.005 0.420 2.405 ;
        RECT  0.270 2.005 0.360 3.190 ;
        END
    END vdd!
    PIN gnd!
        DIRECTION INOUT ;
        USE GROUND ;
        SHAPE ABUTMENT ;
        PORT
        LAYER M1 ;
        RECT  0.210 0.190 0.810 0.750 ;
        RECT  0.270 0.975 0.420 1.175 ;
        RECT  0.270 0.190 0.360 1.175 ;
        END
    END gnd!
END inv
END LIBRARY
```

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8) Caracterização Elétrica:

inv_datasl Library

Cell Groups
INV

INV

inv_datasheet Cell Library: Process , Voltage 1.00, Temp 25.00

Truth Table

INPUT	OUTPUT
A	Z
0	1
1	0

Pin Capacitance Information

Cell Name	Pin Cap(pf)	Max Cap(pf)
	A	Z
inv	0.00103	0.08000

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
inv	0.00000	12.92730	17.05510

Delay Information

Delay(ns) to Z rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Mid	Max
inv	A->Z (FR)	0.00808	0.08154	0.37332

Delay(ns) to Z falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Mid	Max
inv	A->Z (RF)	0.00768	0.07206	0.34224

Power Information

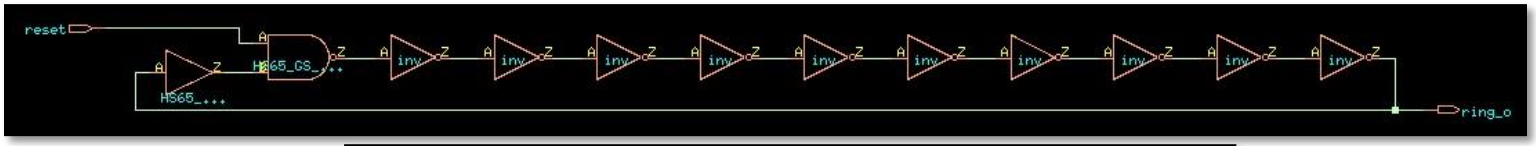
Internal switching power(pJ) to Z rising :

Cell Name	Input	Power(pJ)		
		min	mid	max
inv	A	0.00000	0.00000	0.00000
	A	0.00048	0.00094	0.00089

Internal switching power(pJ) to Z falling :

Cell Name	Input	Power(pJ)		
		min	mid	max
inv	A	0.00000	0.00000	0.00000
	A	0.00000	0.00036	0.00030

9) Síntese Lógica:



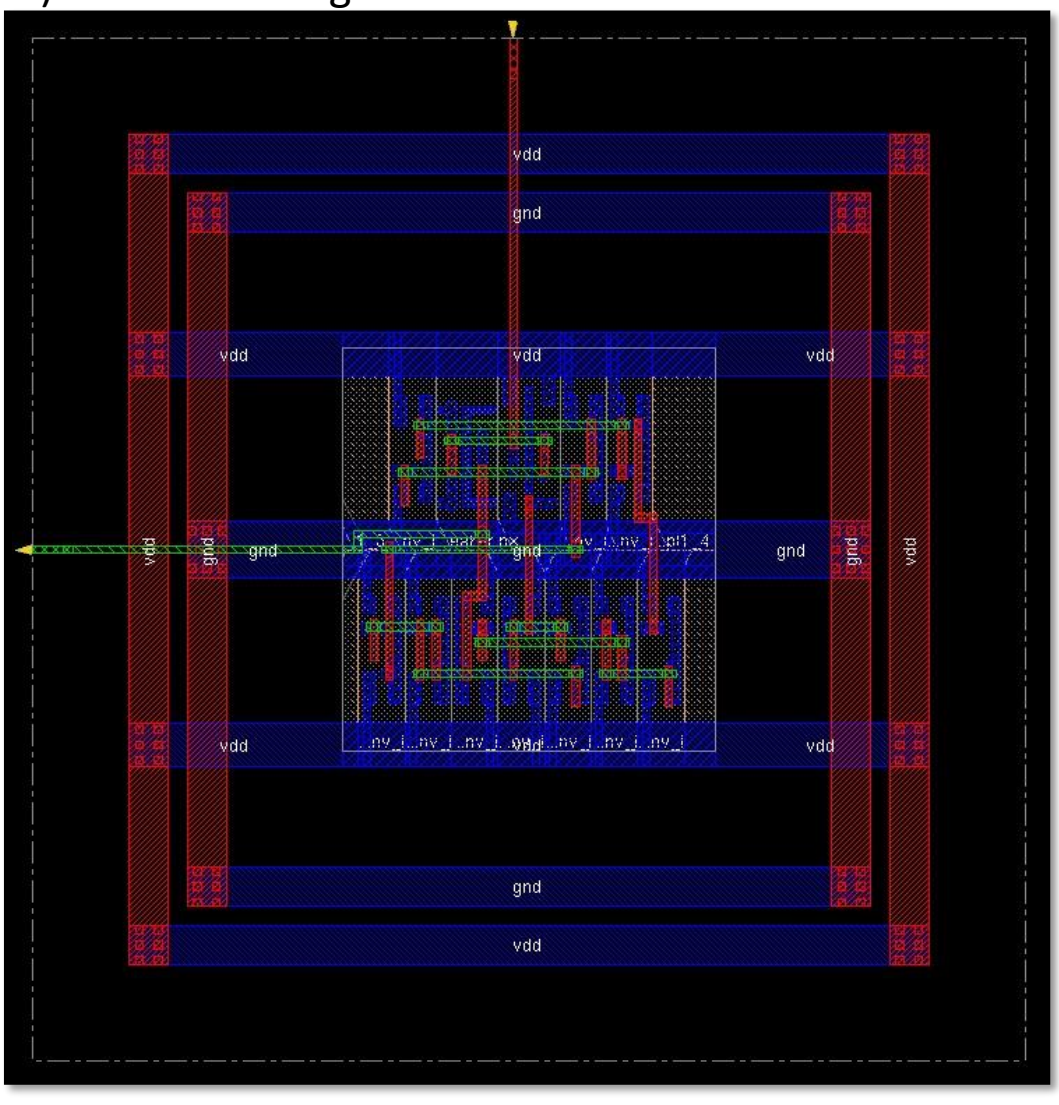

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution GENUS15.20 - 15.20-p004_1
  Generated on:           Sep 01 2016  06:45:05 pm
  Module:                 anel
  Interconnect mode:      global
  Area mode:              physical library
============================================================


      Gate       Instances   Area      Library
-------------------------------------------------------
HS65_GS_BFX2             1   2.080    CORE65GPSVT
HS65_GS_NAND2X2          1   2.080    CORE65GPSVT
inv                     10  15.600    inv
-------------------------------------------------------
total                   12  19.760


  Library   Instances  Area  Instances %
-----------------------------------------
CORE65GPSVT         2  4.160        16.7
inv                10 15.600        83.3


  Type   Instances  Area  Area %
---------------------------------
inverter        10 15.600   78.9
buffer           1  2.080   10.5
logic            1  2.080   10.5
---------------------------------
total           12 19.760  100.0
```

10) Síntese Lógica:



```
Checking routing tracks.....
Checking other grids.....
Checking FINFET Grid is on Manufacture Grid.....

Checking core/die box is on Grid.....

Checking snap rule ......

Checking Row is on grid......

Checking AreaIO row.....
Checking routing blockage.....
Checking components.....
Checking IO Pins.....
Checking constraints (guide/region/fence).....
Checking groups.....

Checking Ptn Pins .....
Checking Ptn Core Box.....

Checking Preroutes.....
No. of regular pre-routes not on tracks : 0
 Design check done.
Report saved in file checkDesign/anel.main.htm.ascii.
0
```

Depth	Name	#Inst	Area (um^2)
0	anel	12	19.76
1			