

Pontifícia Universidade Católica do Rio Grande do Sul Faculdade de Engenharia



S Programa de Graduação em Engenharia da Computação FENGPU

TF – Layout da Função Complexa F2

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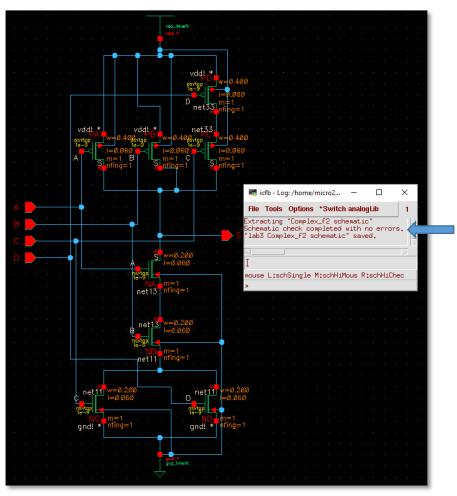
Porto Alegre

Novembro, 2016

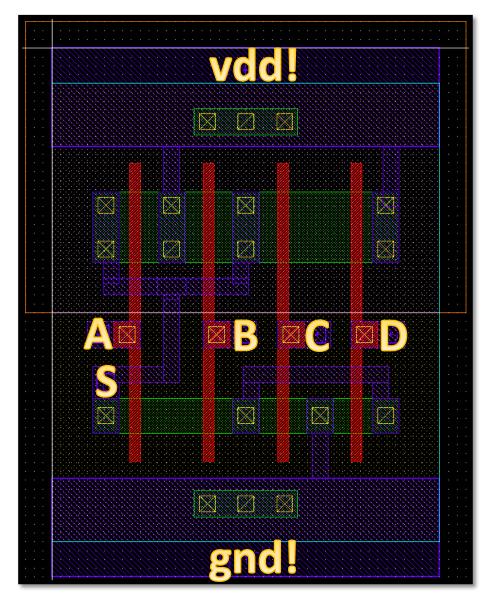
0) Tabela Verdade

Α	В	С	D	~(AABA(CVD))
1	1	1	1	0
1	1	1	0	0
1	1	0	1	0
1	0	1	1	1
0	1	1	1	1
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
0	0	0	0	1
1	1	0	0	1
0	0	1	1	1
1	0	0	1	1
0	1	1	0	1
1	0	1	0	1
0	1	0	1	1

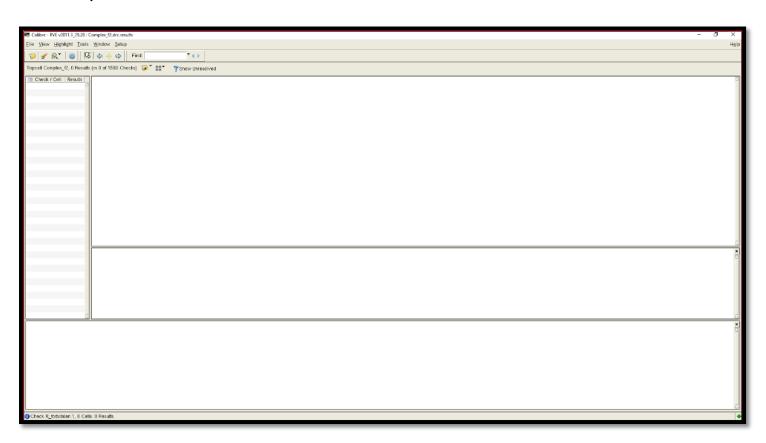
1) Esquemático:



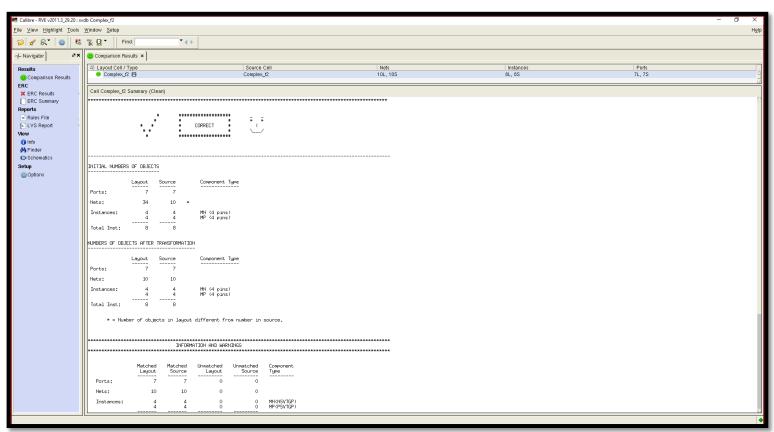
2) Layout:

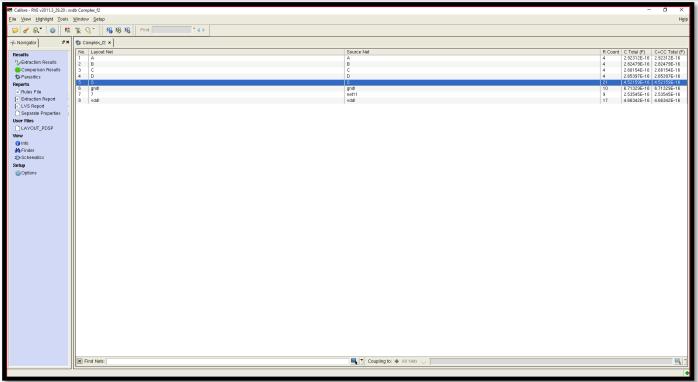


3) Relatório do DRC:



4) Relatório do LVS:





5) Relatório da Extração Elétrica e Simulação Elétrica:

Complex f2.pex.spi:

```
File: Complex f2.pex.spi
   Created: Tue Nov 29 22:47:43 2016
Program "Calibre xRC"
Version "v2011.3_29.20"
 .include "Complex_f2.pex.spi.pex"
 subckt Complex_f2 A B C D S
   vdd!
           vdd!
  gnd!
S S
           gnd!
 * D D
* B B
XPA N S XPA d N A XPA g N vdd! XPA s N vdd! X8 noxref minus psvtgp L=0.06 W=0.4
+ NFING=1 M=1 AS=0.0744 AD=0.0864 PS=0.372 PD=0.832 PO2ACT=0.3675 NGCON=1 lpe=3
XNB net13 N_B XNB g N net11 XNB s N gnd! X8 noxref plus nsvtgp L=0.06 W=0.2
+ NFING=1 M=1 AS=0.0374 AD=0.0374 PS=0.374 PD=0.374 PO2ACT=0.7875 NGCON=1 lpe=0
XNC N_net11_XNB_s N_C_XNC_g N_gnd!_XNC_s N_gnd!_X8_noxref_plus nsvtgp L=0.06
+ W=0.2 NFING=1 M=1 AS=0.0374 AD=0.0374 PS=0.374 PD=0.374 P02ACT=0.7875 NGCON=1
  lne=3
XND N net11_XND_d N_D_XND_g N_gnd!_XNC_s N_gnd!_X8_noxref_plus nsvtgp L=0.06
+ W=0.2 NFING=1 M=1 AS=0.0374 AD=0.0434 PS=0.374 PD=0.634 P02ACT=0.3675 NGCON=1
X8_noxref N_gnd!_X8_noxref_plus N_vdd!_X8_noxref_minus dnwps AREA=3.894 PJ=8.02
 .include "Complex_f2.pex.spi.Complex_f2.pxi"
 ends
```

Complex_f2.pex.spi.inv.pxi

```
* File: Complex_f2.pex.spi.Complex_f2.pxi
* Created: Tue Nov 29 22:47:43 2016

*

x_PM_Complex_f2_A N_A_XPA_g N_A_XNA_g A 0 PM_Complex_f2_A

x_PM_Complex_f2_B N_B_XPB_g N_B_XNB_g B 0 PM_Complex_f2_B

x_PM_Complex_f2_C N_C_XPC_g N_C_XNC_g C 0 PM_Complex_f2_C

x_PM_Complex_f2_D N_D_XPD_g N_D_XND_g D 0 PM_Complex_f2_D

x_PM_Complex_f2_S N_S_XNA_d S N_S_XPA_d N_S_XPB_d 0 PM_Complex_f2_S

x_PM_Complex_f2_gnd! N_gnd!_X8_noxref_plus_gnd! N_gnd!_XNC_s 0

+ PM_Complex_f2_gnd!

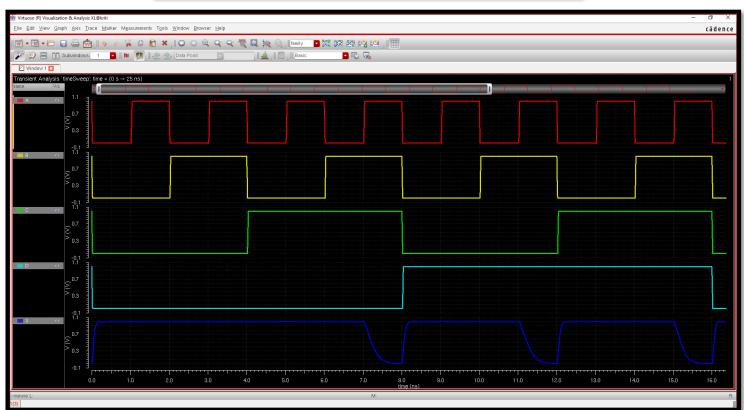
x_PM_Complex_f2_net11 N_net11_XND_d N_net11_XNB_s 0 PM_Complex_f2_net11

x_PM_Complex_f2_vdd! N_vdd!_XPA_s N_vdd!_X8_noxref_minus_vdd! N_vdd!_XPD_s 0

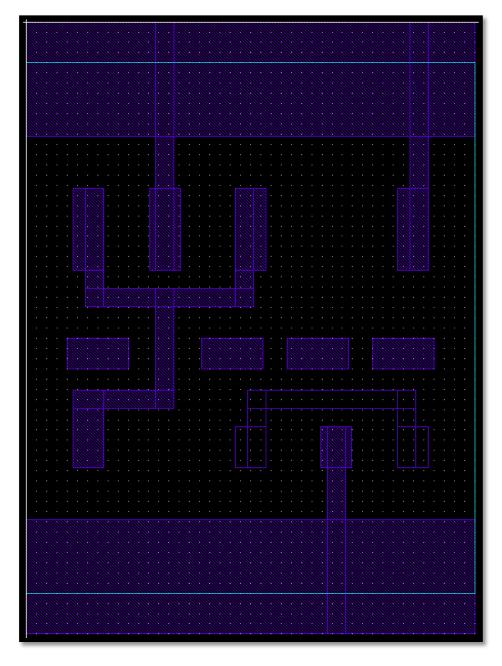
+ PM_Complex_f2_vdd!
```

Complex_f2.src.net

```
auCdl Netlist:
 Library Name: lab3
 Top Cell Name: Complex f2
* View Name:
                 schematic
* Netlisted on: Nov 29 22:47:20 2016
*.EQUATION
*.SCALE METER
* . MEGA
. PARAM
*.GLOBAL gnd!
        vdd!
*.PIN gnd!
     vdd!
* Library Name: lab3
* Cell Name: Complex_f2
* View Name:
                schematic
SUBCKT Complex_f2 A B C D S
*.PININFO A:I B:I C:I D:I S:O
MNA S A net13 gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MNB net13 B net11 gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MNC netl1 C gnd! gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MND net11 D gnd! gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPA S A vdd! vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPB S B vdd! vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPC S C net33 vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPD net33 D vdd! vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
ENDS
```



6) Layout da View Abstract:



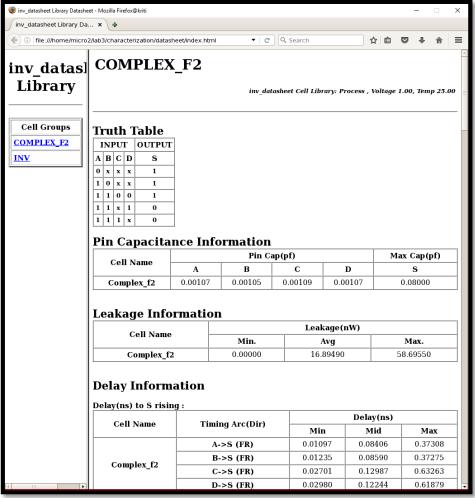
1

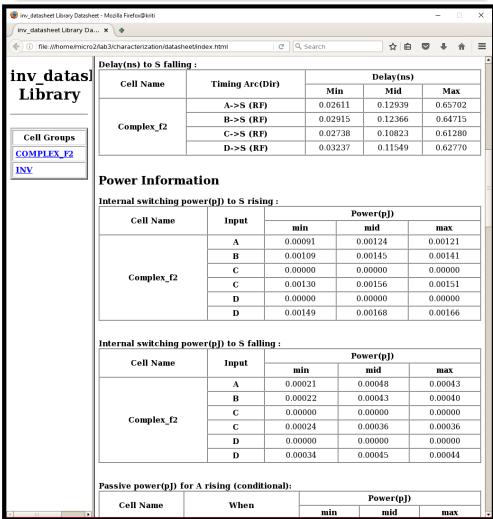
2

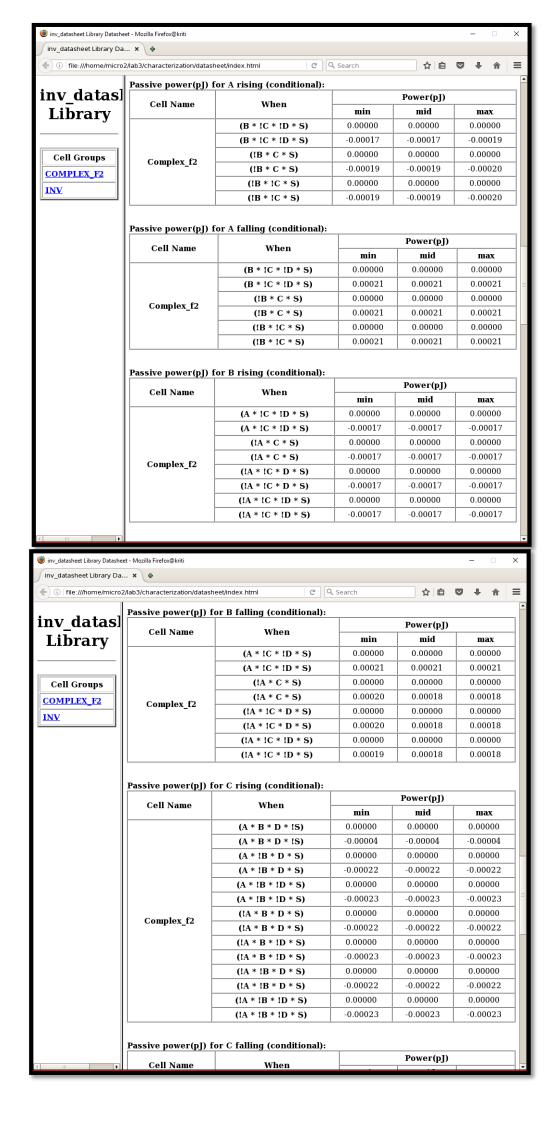
```
# Preview export LEF
     Preview sub-version 5.10.41_USR5.90.69
# REF LIBS: lab3
# TECH LIB NAME: cmos065
# TECH FILE NAME: techfile.cds
VERSION 5.5;
NAMESCASESENSITIVE ON ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]";
UNITS
   DATABASE MICRONS 1000 ;
END UNITS
MANUFACTURINGGRID
    SYMMETRY Y ;
    CLASS CORE
    SIZE 0.200 BY 2.600 ;
END CORE
MACRO Complex f2
    CLASS CORE ;
    FOREIGN Complex f2 0 -2.8;
    ORIGIN 0.000 2.800;
    SIZE 2.200 BY 2.600 ;
    SYMMETRY X Y ;
    SITE CORE ;
    PIN S
        DIRECTION OUTPUT ;
        PORT
        LAYER M1 ;
        RECT 1.025 -1.215 1.175 -0.815 ;
RECT 1.025 -1.395 1.115 -0.815 ;
        RECT 0.290 -1.395 1.115 -1.305;
        RECT 0.635 -1.895 0.725 -1.305 ;
        RECT 0.230 -1.895 0.725 -1.805;
        RECT 0.230 -1.215 0.380 -0.815;
        RECT 0.290 -1.395 0.380 -0.815;
        RECT 0.230 -2.185 0.380 -1.805;
        END
    END S
    PIN D
        DIRECTION INPUT ;
        PORT
        LAYER M1 :
        RECT 1.700 -1.700 2.000 -1.550;
    END D
    PIN C
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT 1.280 -1.700 1.580 -1.550;
        END
    END C
    PIN B
```

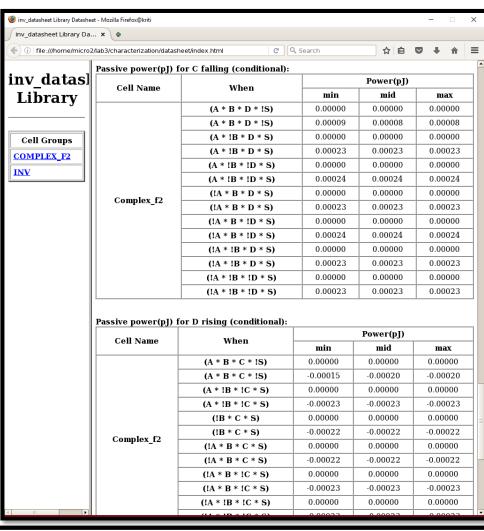
```
DIRECTION INPUT ;
         TAYER M1 :
         RECT 0.860 -1.700 1.160 -1.550;
         END
    END B
    PIN A
         DIRECTION INPUT ;
         PORT
         LAYER M1 :
         RECT 0.200 -1.700 0.500 -1.550;
         END
    END A
    PIN vdd!
         DIRECTION INOUT :
         USE POWER ;
         SHAPE ABUTMENT ;
         PORT
         LAYER M1 ;
         RECT 0.000 -0.560 2.200 0.000;
         RECT 1.880 -1.215 1.970 0.000;
         RECT 1.820 -1.215 1.970 -0.815 ;
         RECT 0.605 -1.215 0.755 -0.815 ;
RECT 0.635 -1.215 0.725 0.000 ;
    END vdd!
    PIN gnd!
         DIRECTION INOUT ;
         USE GROUND ;
         SHAPE ABUTMENT ;
         PORT
         LAYER M1 ;
         RECT 0.000 -3.000 2.200 -2.440 ;
RECT 1.445 -2.185 1.595 -1.985 ;
         RECT 1.475 -3.000 1.565 -1.985;
         END
    END gnd!
    OBS
         LAYER M1 ;
         RECT 1.025 -2.185 1.175 -1.985;
         RECT 1.820 -2.185 1.970 -1.985;
         RECT 1.085 -2.185 1.175 -1.805 ;
RECT 1.820 -2.185 1.910 -1.805 ;
RECT 1.085 -1.895 1.910 -1.805 ;
END Complex f2
END LIBRARY
```

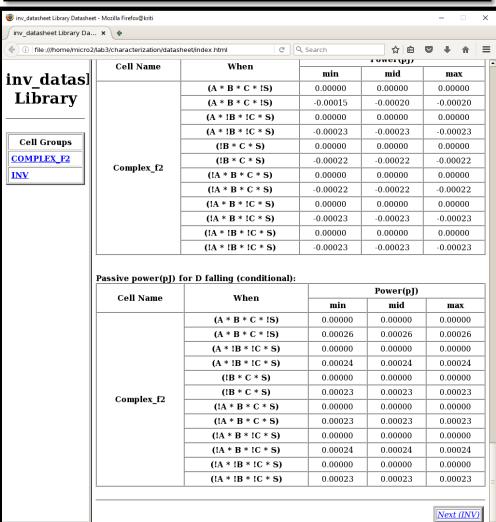
7) Caracterização Elétrica:



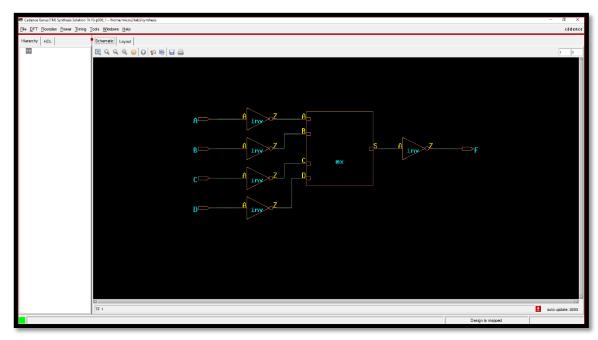


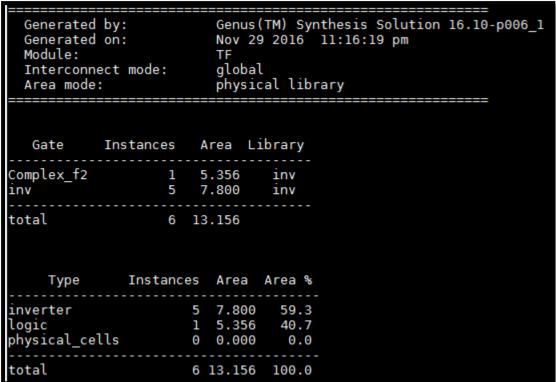




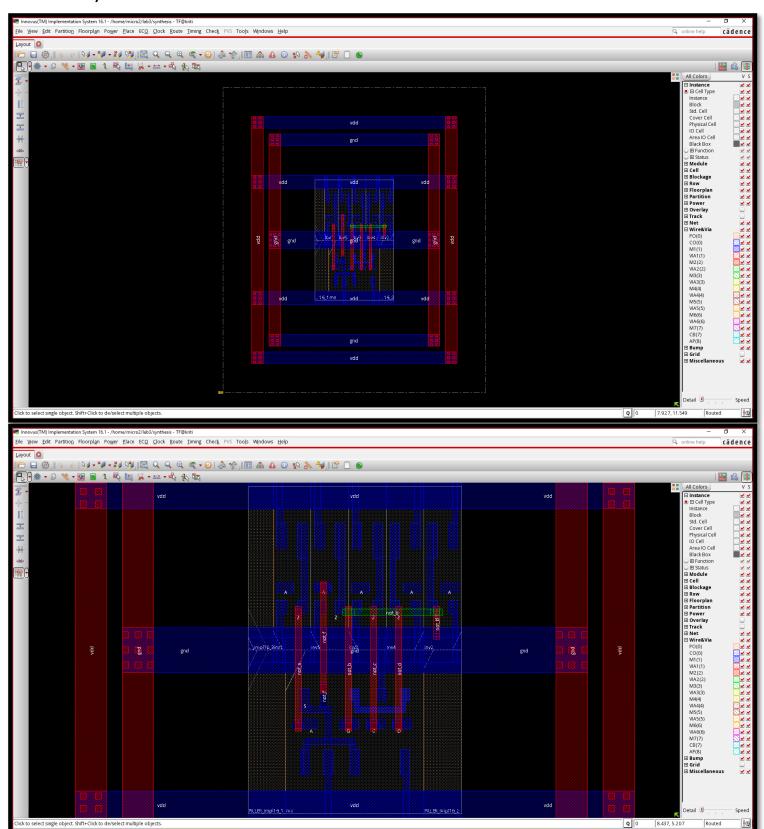


8) Síntese Lógica:





9) Síntese Física:



```
----- Design Statistics:
Number of Instances
Number of Non-uniquified Insts
Number of Nets
                                           : 17
Average number of Pins per Net : 1.18
Maximum number of Pins in Net : 2
  ----- I/O Port summary
Number of Primary I/O Ports
                                           : 5
Number of Input Ports
Number of Output Ports
Number of Bidirectional Ports
Number of Power/Ground Ports
                                           : 1
                                           : Θ
                                           : Θ
Number of Floating Ports
Number of Ports Connected to Multiple Pads
Number of Ports Connected to Core Instances
                                                               *: 0
                                                              *: 0
                                                                : 5
 ----- Design Rule Checking:
Number of Output Pins connect to Power/Ground *: 0
Number of Insts with Input Pins tied together ?: 0
Number of TieHi/Lo term nets not connected to instance's PG terms ?: 0
Number of Input/InOut Floating Pins : 0
Number of Output Floating Pins : 0
Number of Output Term Marked TieHi/Lo
                                                                *: 0
Number of nets with tri-state drivers
                                                                 : Θ
Number of nets with parallel drivers
                                                                 : 0
Number of nets with multiple drivers
                                                                 : 0
Number of nets with no driver (No FanIn)
Number of Output Floating nets (No FanOut)
Number of High Fanout nets (>50)
                                                                 : 0
                                                                 : 0
                                                                 : 0
Checking routing tracks.....
Checking other grids.....
Checking FINFET Grid is on Manufacture Grid.....
Checking core/die box is on Grid.....
Checking snap rule .....
Checking Row is on grid.....
Checking AreaIO row.....
Checking routing blockage.....
Checking components....
Checking IO Pins....
Unplaced Io Pins = 5
Checking constraints (guide/region/fence).....
Checking groups.....
Checking Ptn Pins .....
Checking Ptn Core Box.....
Checking Preroutes.....
No. of regular pre-routes not on tracks : 0
Design check done.
Report saved in file checkDesign/TF.main.htm.ascii.
*** Message Summary: 0 warning(s), 0 error(s)
```

Depth	Name	#Inst	Area (um^2)
Θ 1	TF	6	Area (um^2) 13.52