



Pontifícia Universidade Católica do Rio Grande do Sul

Faculdade de Engenharia

Programa de Graduação em Engenharia da Computação



TF – Layout da Função Complexa F2

Micro2: Maiki Buffet e Marcelo Pereira

Professor: Fernando Gehm Moraes

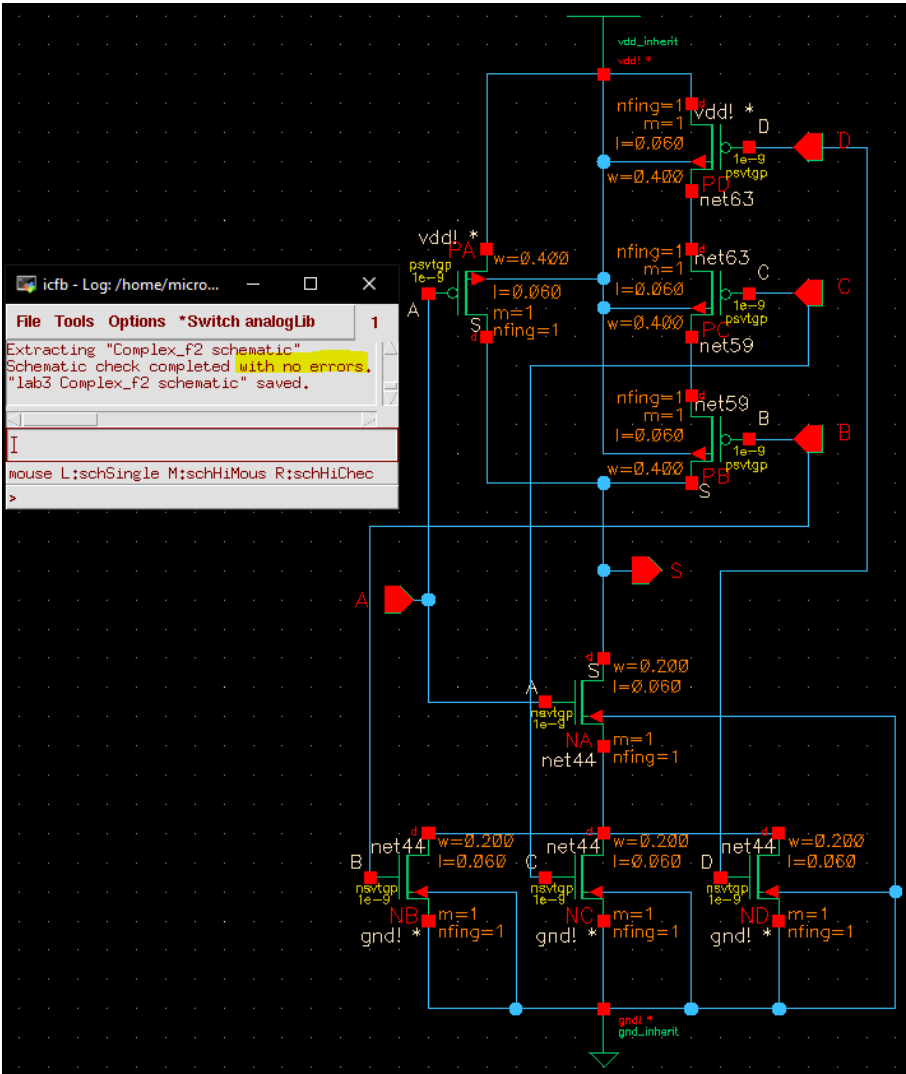
Porto Alegre

Junho, 2017

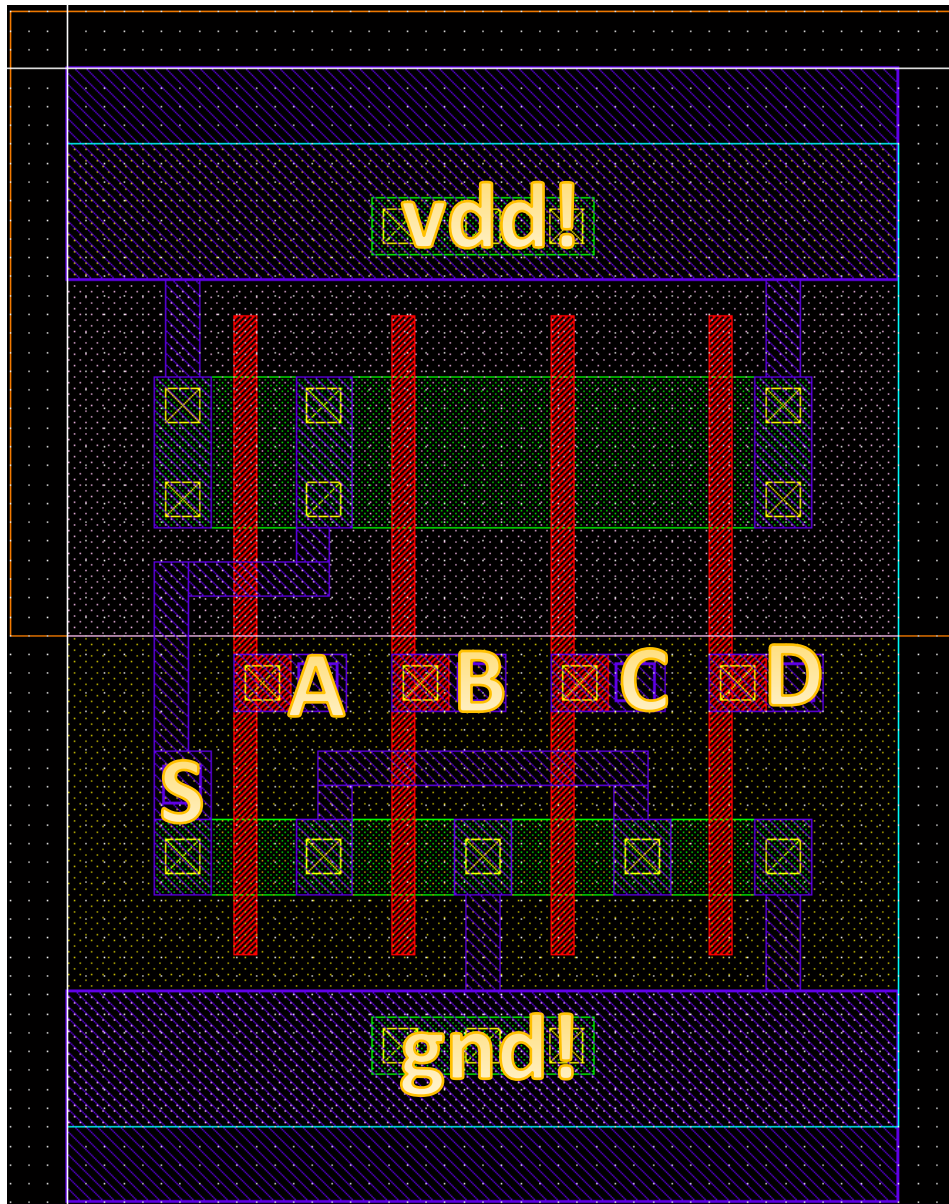
0) Tabela Verdade

A	B	C	D	$\sim(A \wedge (B \vee C \vee D))$
1	1	1	1	0
1	1	1	0	0
1	1	0	1	0
1	0	1	1	0
0	1	1	1	1
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
0	0	0	0	1
1	1	0	0	0
0	0	1	1	1
1	0	0	1	0
0	1	1	0	1
1	0	1	0	0
0	1	0	1	1

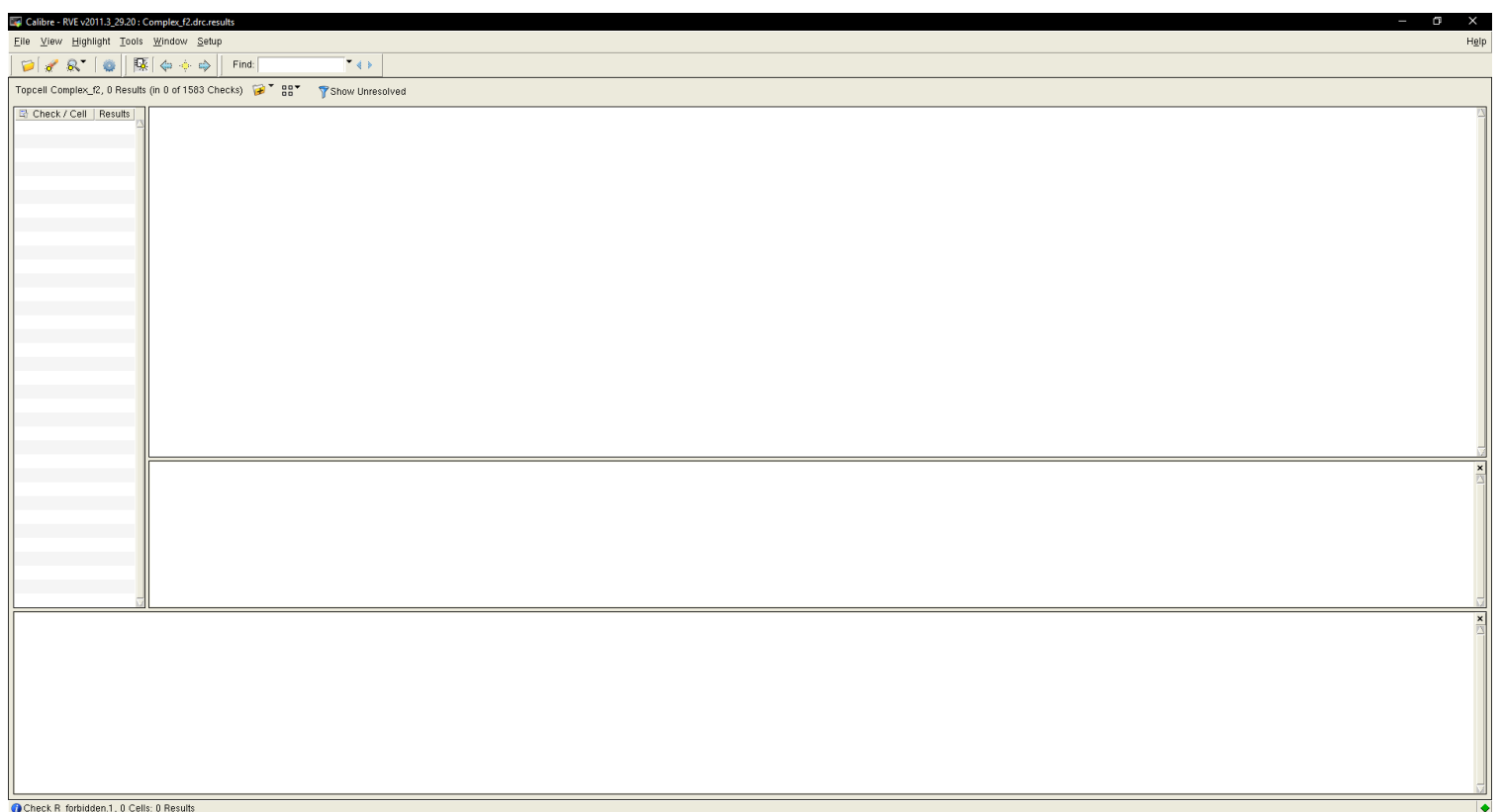
1) Esquemático:



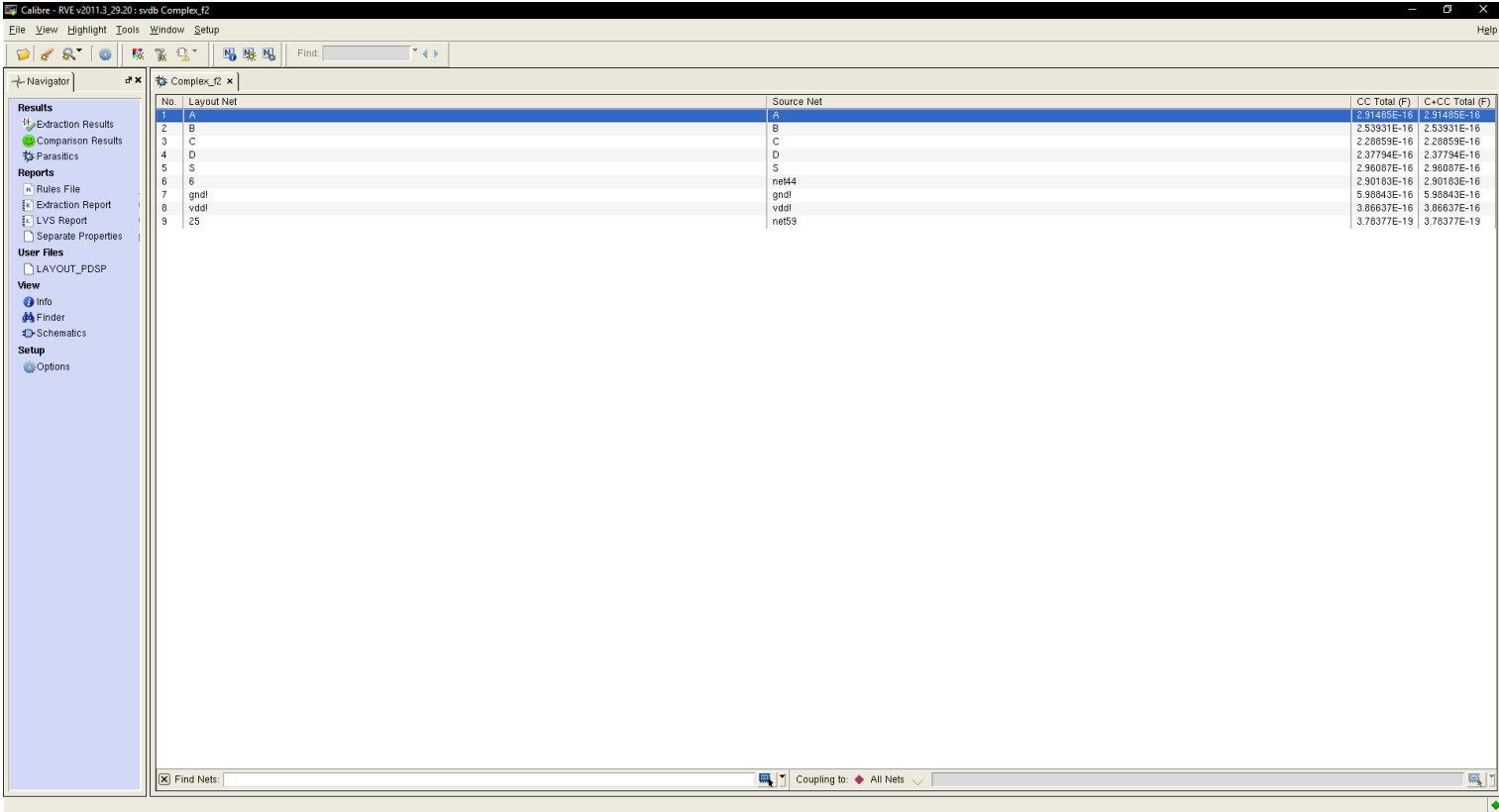
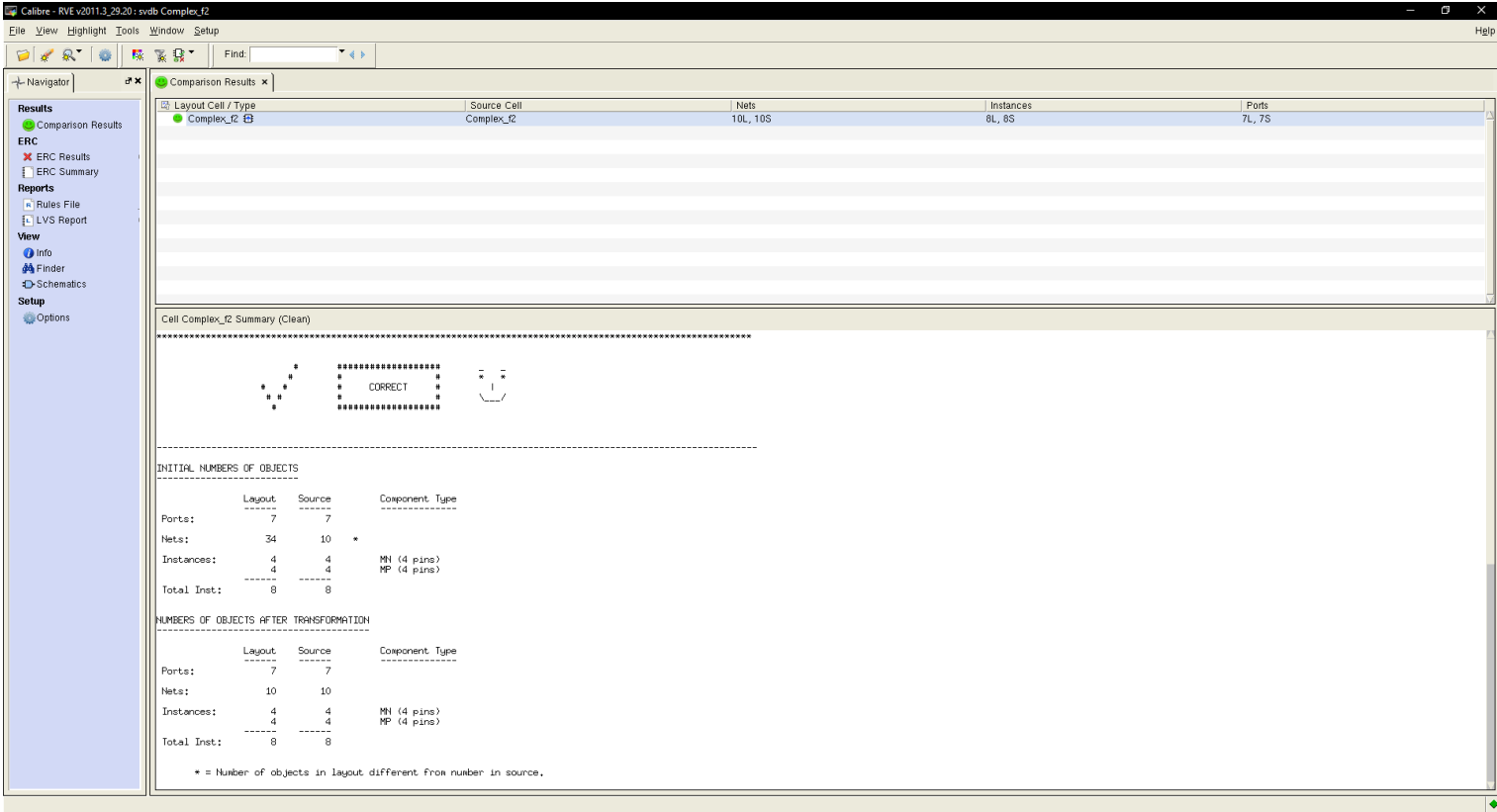
2) Layout:



3) Relatório do DRC:



4) Relatório do LVS:



5) Extração Elétrica e Simulação Elétrica:

- Complex_f2.pex.spi:

```
* File: Complex_f2.pex.spi
* Created: Sat Jun 17 00:29:45 2017
* Program "Calibre xRC"
* Version "v2011.3_29.20"
*
.subckt Complex_f2  A B C D S
*
XPA S A vdd! vdd! psvtgp L=0.06 W=0.4 NFING=1 M=1 AS=0.0864 AD=0.0744 PS=0.832
+ PD=0.372 P02ACT=0.3675 NGCON=1 lpe=1
XPB net59 B S vdd! psvtgp L=0.06 W=0.4 NFING=1 M=1 AS=0.0744 AD=0.0744 PS=0.372
+ PD=0.372 P02ACT=0.7875 NGCON=1 lpe=1
XPC net63 C net59 vdd! psvtgp L=0.06 W=0.4 NFING=1 M=1 AS=0.0744 AD=0.0744
+ PS=0.372 PD=0.372 P02ACT=0.7875 NGCON=1 lpe=0
XPD vdd! D net63 vdd! psvtgp L=0.06 W=0.4 NFING=1 M=1 AS=0.0744 AD=0.0864
+ PS=0.372 PD=0.832 P02ACT=0.3675 NGCON=1 lpe=0
XNA S A net44 gnd! nsvtgp L=0.06 W=0.2 NFING=1 M=1 AS=0.0374 AD=0.0434 PS=0.374
+ PD=0.634 P02ACT=0.3675 NGCON=1 lpe=1
XNB net44 B gnd! gnd! nsvtgp L=0.06 W=0.2 NFING=1 M=1 AS=0.0374 AD=0.0374
+ PS=0.374 PD=0.374 P02ACT=0.7875 NGCON=1 lpe=1
XNC net44 C gnd! gnd! nsvtgp L=0.06 W=0.2 NFING=1 M=1 AS=0.0374 AD=0.0374
+ PS=0.374 PD=0.374 P02ACT=0.7875 NGCON=1 lpe=1
XND net44 D gnd! gnd! nsvtgp L=0.06 W=0.2 NFING=1 M=1 AS=0.0434 AD=0.0374
+ PS=0.634 PD=0.374 P02ACT=0.3675 NGCON=1 lpe=1
X8_noxref gnd! vdd! dnwps AREA=4.125 PJ=8.3
*
.include "Complex_f2.pex.spi.Complex_f2.pxi"
*
.ends
*
*
```

- Complex_f2.pex.spi.inv.pxi

```
* File: Complex_f2.pex.spi.Complex_f2.pxi
* Created: Sat Jun 17 00:29:45 2017
*
cc_1 A B 0.0218022f
cc_2 A S 0.104658f
cc_3 A net44 0.0288087f
cc_4 A gnd! 0.0751774f
cc_5 A vdd! 0.0610379f
cc_6 B C 0.0218022f
cc_7 B S 0.0322689f
cc_8 B net44 0.05435f
cc_9 B gnd! 0.0868384f
cc_10 B vdd! 0.0368689f
cc_11 C D 0.0218022f
cc_12 C S 0.00229689f
cc_13 C net44 0.0540687f
cc_14 C gnd! 0.0871551f
cc_15 C vdd! 0.0417338f
cc_16 D net44 0.0196506f
cc_17 D gnd! 0.106861f
cc_18 D vdd! 0.0894793f
cc_19 S net44 0.0233323f
cc_20 S gnd! 0.0546151f
cc_21 S vdd! 0.0789157f
cc_22 net44 gnd! 0.109973f
cc_23 gnd! vdd! 0.0782225f
cc_24 vdd! net59 3.78377e-19
```

- Complex_f2.src.net

```
*****
* auCdl Netlist:
*
* Library Name: lab3
* Top Cell Name: Complex_f2
* View Name: schematic
* Netlisted on: Jun 17 00:29:26 2017
*****

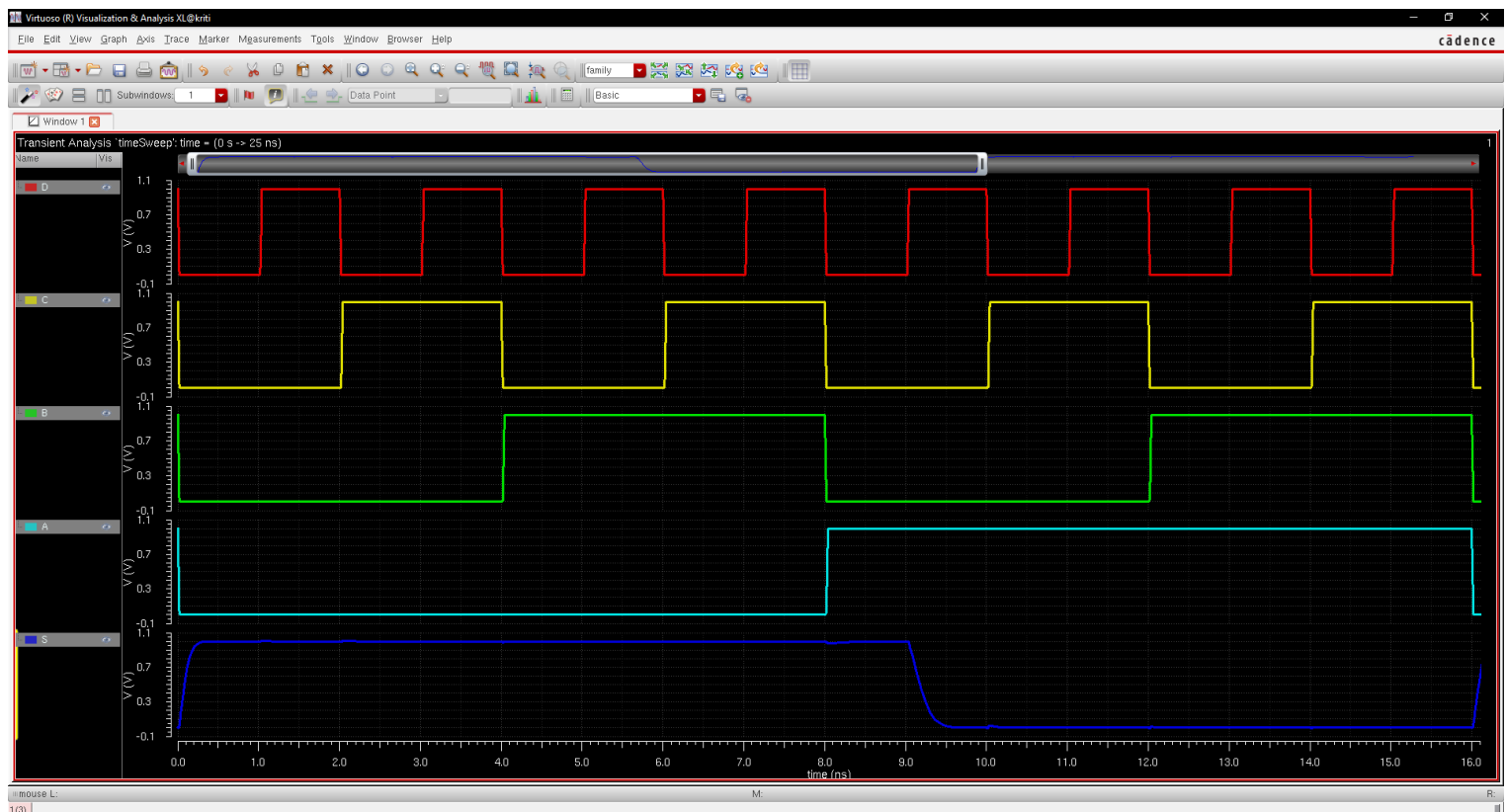
*.EQUATION
*.SCALE METER
*.MEGA
.PARAM

*.GLOBAL gnd!
+      vdd!

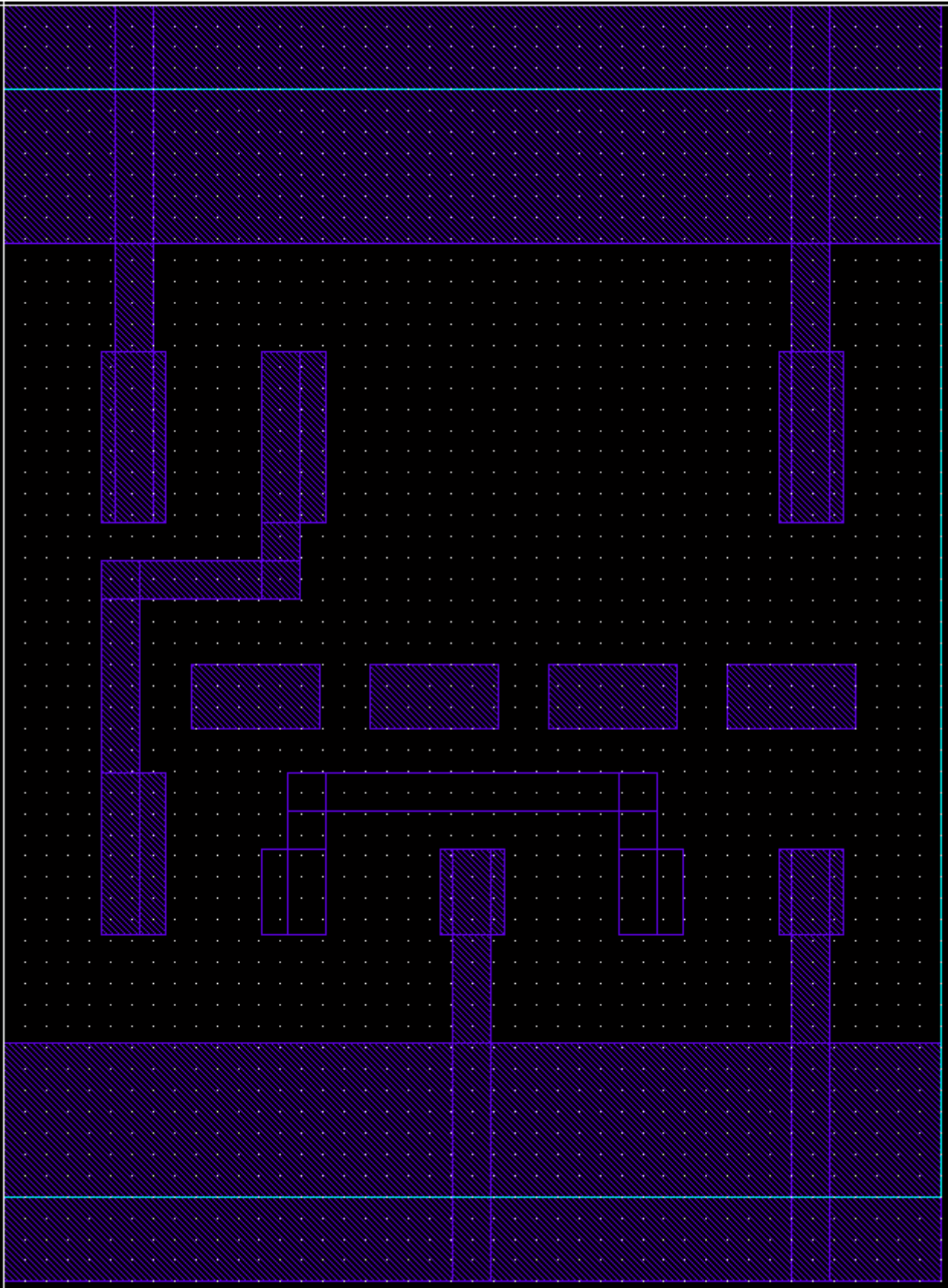
*.PIN gnd!
*+      vdd!

*****
* Library Name: lab3
* Cell Name: Complex_f2
* View Name: schematic
*****

.SUBCKT Complex_f2 A B C D S
*.PININFO A:I B:I C:I D:I S:0
MNA S A net44 gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MNB net44 B gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MNC net44 C gnd! gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MND net44 D gnd! gnd! nsvtgp w=0.2 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPA S A vdd! vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPB net59 B S vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPC net63 C net59 vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
MPD vdd! D net63 vdd! psvtgp w=0.4 l=0.06 nfing=1 sense=0 ngcon=1 m=1
+ accurateFlow=0
.ENDS
```



6) Layout da View Abstract:



- Complex_f2.lef

1

```
*****
# Preview export LEF
#
#       Preview sub-version 5.10.41_USR5.90.69
#
# REF LIBS: lab3
# TECH LIB NAME: cmos065
# TECH FILE NAME: techfile.cds
*****

VERSION 5.5 ;

NAMECASESENSITIVE ON ;

DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;

UNITS
    DATABASE MICRONS 1000 ;
END UNITS

    MANUFACTURINGGRID    0.005000 ;
SITE CORE
    SYMMETRY Y ;
    CLASS CORE ;
    SIZE 0.200 BY 2.600 ;
END CORE

MACRO Complex_f2
    CLASS CORE ;
    FOREIGN Complex_f2 0 -2.8 ;
    ORIGIN 0.000 2.800 ;
    SIZE 2.200 BY 2.600 ;
    SYMMETRY X Y ;
    SITE CORE ;
    PIN S
        DIRECTION OUTPUT ;
        PORT
        LAYER M1 ;
        RECT 0.605 -1.215 0.755 -0.815 ;
        RECT 0.605 -1.395 0.695 -0.815 ;
        RECT 0.230 -1.395 0.695 -1.305 ;
        RECT 0.230 -2.185 0.380 -1.805 ;
        RECT 0.230 -2.185 0.320 -1.305 ;
        END
    END S
    PIN D
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT 1.700 -1.700 2.000 -1.550 ;
        END
    END D
    PIN C
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT 1.280 -1.700 1.580 -1.550 ;
        END
    END C
END Complex_f2
```

2

```
    PIN B
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT 0.860 -1.700 1.160 -1.550 ;
        END
    END B
    PIN A
        DIRECTION INPUT ;
        PORT
        LAYER M1 ;
        RECT 0.440 -1.700 0.740 -1.550 ;
        END
    END A
    PIN vdd!
        DIRECTION INOUT ;
        USE POWER ;
        SHAPE ABUTMENT ;
        PORT
        LAYER M1 ;
        RECT 0.000 -0.560 2.200 0.000 ;
        RECT 1.820 -1.215 1.970 -0.815 ;
        RECT 1.850 -1.215 1.940 0.000 ;
        RECT 0.230 -1.215 0.380 -0.815 ;
        RECT 0.260 -1.215 0.350 0.000 ;
        END
    END vdd!
    PIN gnd!
        DIRECTION INOUT ;
        USE GROUND ;
        SHAPE ABUTMENT ;
        PORT
        LAYER M1 ;
        RECT 0.000 -3.000 2.200 -2.440 ;
        RECT 1.820 -2.185 1.970 -1.985 ;
        RECT 1.850 -3.000 1.940 -1.985 ;
        RECT 1.025 -2.185 1.175 -1.985 ;
        RECT 1.055 -3.000 1.145 -1.985 ;
        END
    END gnd!
    OBS
        LAYER M1 ;
        RECT 0.605 -2.185 0.755 -1.985 ;
        RECT 1.445 -2.185 1.595 -1.985 ;
        RECT 0.665 -2.185 0.755 -1.805 ;
        RECT 1.445 -2.185 1.535 -1.805 ;
        RECT 0.665 -1.895 1.535 -1.805 ;
        END
    END Complex_f2
END LIBRARY
```


7) Caracterização Elétrica:

inv_datasheet Library Datasheet - Mozilla Firefox@kriti

inv_datasheet Library Da... x

file:///home/micro2/lab3/characterization/datasheet/index.html

Search

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inv_datasheet Library

Cell Groups

[COMPLEX_F2](#)

[INV](#)

COMPLEX_F2

inv_datasheet Cell Library: Process , Voltage 1.00, Temp 25.00

Truth Table

INPUT				OUTPUT
A	B	C	D	S
0	x	x	x	1
1	0	0	0	1
1	0	x	1	0
1	x	1	x	0
1	1	x	x	0

Pin Capacitance Information

Cell Name	Pin Cap(pf)				Max Cap(pf)
	A	B	C	D	S
Complex_f2	0.00106	0.00099	0.00108	0.00106	0.08000

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
Complex_f2	0.00000	20.05870	40.10890

Delay Information

Delay(ns) to S rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Mid	Max
Complex_f2	A->S (FR)	0.00948	0.08306	0.37385
	B->S (FR)	0.03099	0.15990	0.88590
	C->S (FR)	0.03831	0.15994	0.88359

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inv_datasheet Library Datasheet - Mozilla Firefox@kriti

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inv_datasheet Library

Cell Groups

[COMPLEX_F2](#)

[INV](#)

D->S (FR)

0.04038

0.15221

0.86442

Delay(ns) to S falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Mid	Max
Complex_f2	A->S (RF)	0.01855	0.10584	0.49767
	B->S (RF)	0.01664	0.08813	0.47074
	C->S (RF)	0.02008	0.09232	0.47446
	D->S (RF)	0.02180	0.09690	0.48213

Power Information

Internal switching power(pJ) to S rising :

Cell Name	Input	Power(pJ)		
		min	mid	max
Complex_f2	A	0.00093	0.00132	0.00128
	B	0.00000	0.00000	0.00000
	B	0.00098	0.00121	0.00118
	C	0.00000	0.00000	0.00000
	C	0.00121	0.00137	0.00135
	D	0.00000	0.00000	0.00000
	D	0.00141	0.00154	0.00154

Internal switching power(pJ) to S falling :

Cell Name	Input	Power(pJ)		
		min	mid	max
Complex_f2	A	0.00008	0.00043	0.00037
	B	0.00000	0.00000	0.00000
	B	0.00014	0.00030	0.00030
	C	0.00000	0.00000	0.00000
	C	0.00023	0.00038	0.00037
	D	0.00000	0.00000	0.00000

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inv_datasheet Library Datasheet - Mozilla Firefox@krtb

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inv_datasheet Library

Cell Groups

[COMPLEX_f2](#)

[INV](#)

	D	0.00033	0.00045	0.00043
--	---	---------	---------	---------

Passive power(pj) for A rising (conditional):

Cell Name	When	Power(pj)		
		min	mid	max
Complex_f2	(IB * IC * ID * S)	0.00000	0.00000	0.00000
	(IB * IC * ID * S)	-0.00020	-0.00021	-0.00022

Passive power(pj) for A falling (conditional):

Cell Name	When	Power(pj)		
		min	mid	max
Complex_f2	(IB * IC * ID * S)	0.00000	0.00000	0.00000
	(IB * IC * ID * S)	0.00028	0.00028	0.00028

Passive power(pj) for B rising (conditional):

Cell Name	When	Power(pj)		
		min	mid	max
Complex_f2	(A * C * IS)	0.00000	0.00000	0.00000
	(A * C * IS)	-0.00005	-0.00005	-0.00005
	(A * IC * D * IS)	0.00000	0.00000	0.00000
	(A * IC * D * IS)	-0.00005	-0.00004	-0.00004
	(IA * C * S)	0.00000	0.00000	0.00000
	(IA * C * S)	-0.00019	-0.00020	-0.00020
	(IA * IC * D * S)	0.00000	0.00000	0.00000
	(IA * IC * D * S)	-0.00017	-0.00019	-0.00020
	(IA * IC * ID * S)	0.00000	0.00000	0.00000
	(IA * IC * ID * S)	-0.00020	-0.00020	-0.00020

Passive power(pj) for B falling (conditional):

Cell Name	When	Power(pj)		
		min	mid	max

0.00000

Pesquisar no Windows

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17/06/2021

inv_datasheet Library Datasheet - Mozilla Firefox@krti

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inv_datasheet
Library

Cell Groups

[COMPLEX_F2](#)

[INV](#)

Complex_f2	(A * C * !S)	0.00000	0.00000	0.00000
	(A * C * !S)	0.00006	0.00006	0.00006
	(A * !C * D * !S)	0.00000	0.00000	0.00000
	(A * !C * D * !S)	0.00008	0.00007	0.00007
	(!A * C * S)	0.00000	0.00000	0.00000
	(!A * C * S)	0.00021	0.00021	0.00021
	(!A * !C * D * S)	0.00000	0.00000	0.00000
	(!A * !C * D * S)	0.00021	0.00021	0.00021
	(!A * !C * !D * S)	0.00000	0.00000	0.00000
	(!A * !C * !D * S)	0.00023	0.00021	0.00021

Passive power(pj) for C rising (conditional):

Cell Name	When	Power(pj)		
		min	mid	max
Complex_f2	(A * B * D * !S)	0.00000	0.00000	0.00000
	(A * B * D * !S)	-0.00014	-0.00014	-0.00014
	(A * B * !D * !S)	0.00000	0.00000	0.00000
	(A * B * !D * !S)	-0.00017	-0.00023	-0.00023
	(A * !B * D * !S)	0.00000	0.00000	0.00000
	(A * !B * D * !S)	-0.00007	-0.00008	-0.00008
	(!A * B * D * S)	0.00000	0.00000	0.00000
	(!A * B * D * S)	-0.00015	-0.00015	-0.00015
	(!A * B * !D * S)	0.00000	0.00000	0.00000
	(!A * B * !D * S)	-0.00024	-0.00024	-0.00024
	(!A * !B * D * S)	0.00000	0.00000	0.00000
	(!A * !B * D * S)	-0.00024	-0.00024	-0.00024
	(!A * !B * !D * S)	0.00000	0.00000	0.00000
	(!A * !B * !D * S)	-0.00025	-0.00025	-0.00025

Passive power(pj) for C falling (conditional):

Cell Name	When	Power(pj)		

Pesquisar no Windows

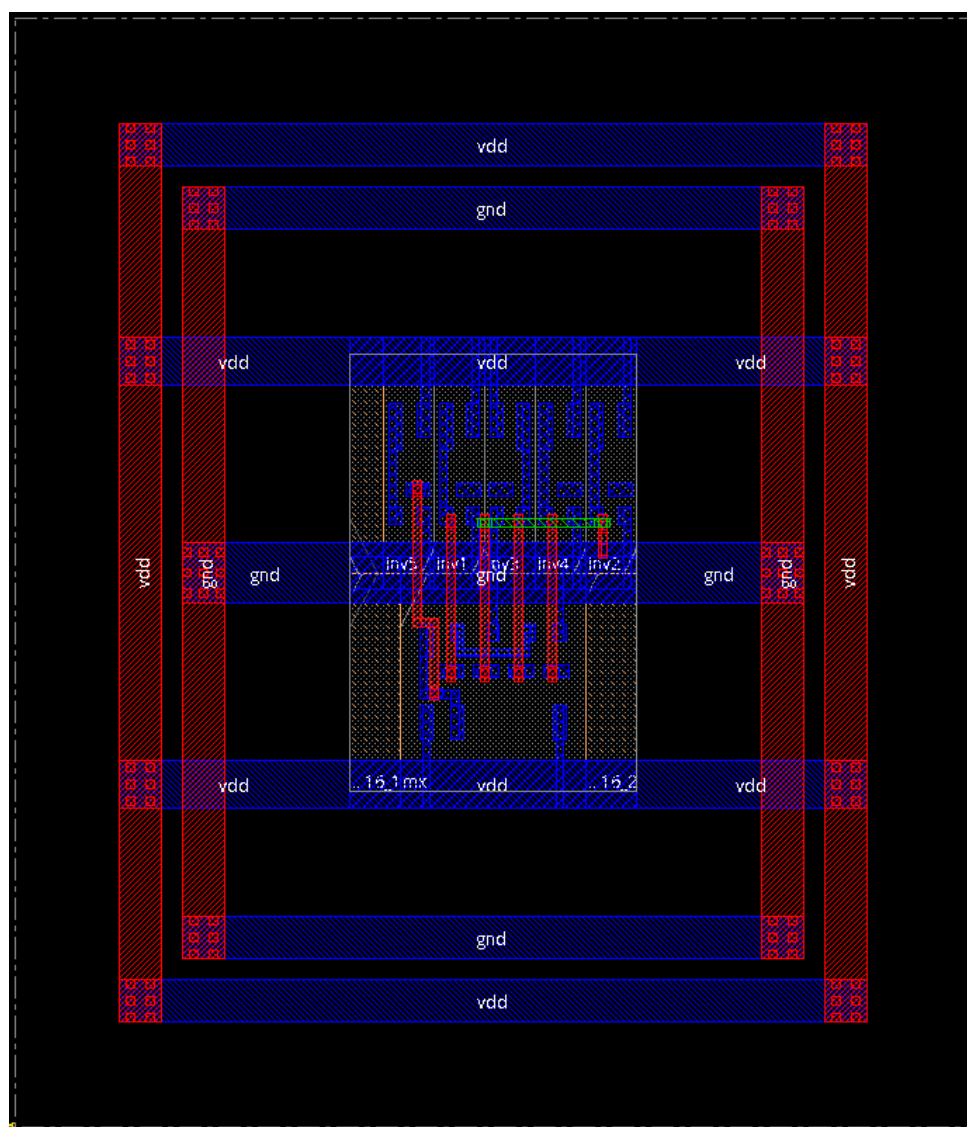
00:50
17/06/2019

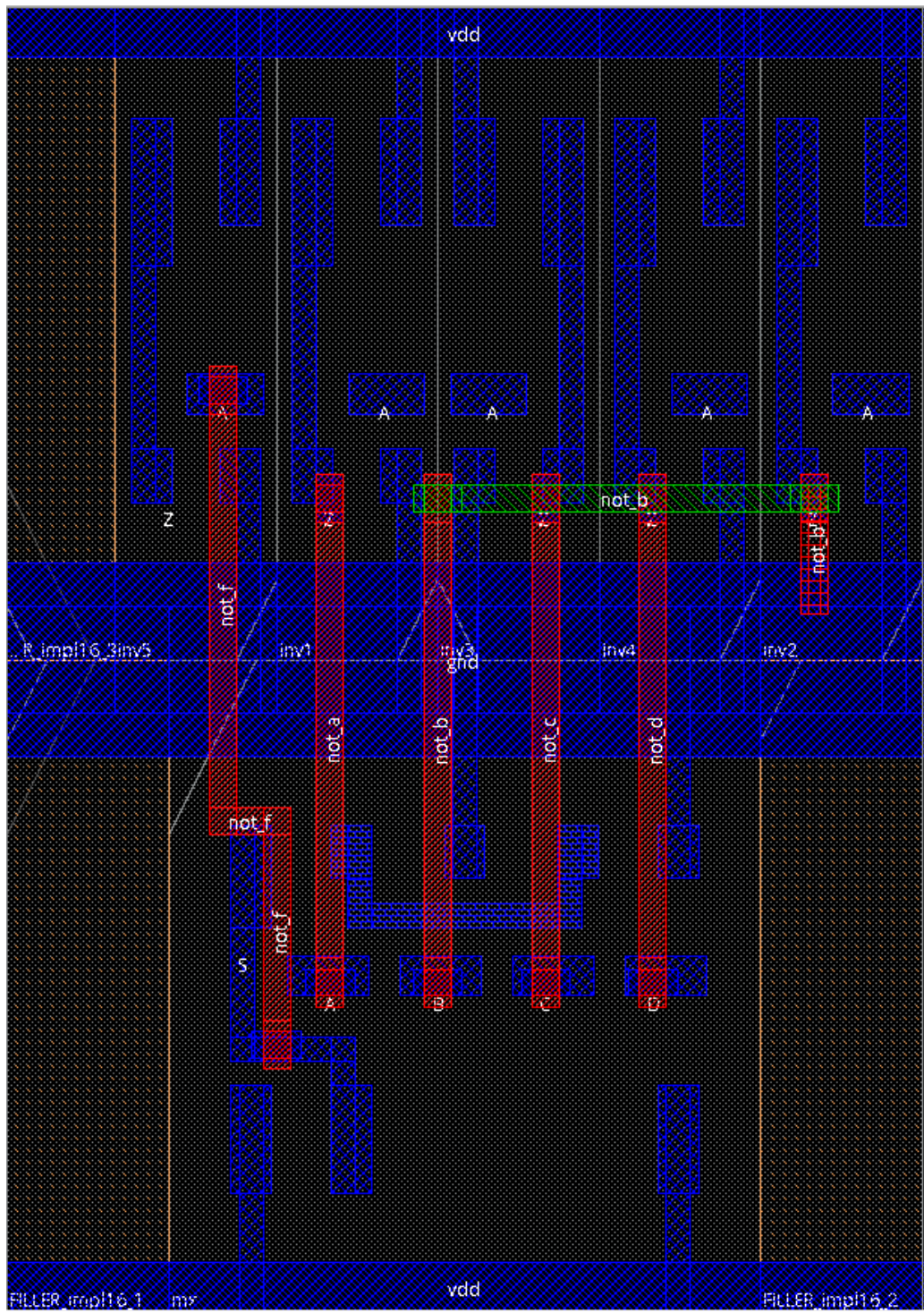
Generated by:	Genus(TM) Synthesis Solution 16.10-p006_1		
Generated on:	Jun 17 2017 12:55:32 am		
Module:	TF		
Interconnect mode:	global		
Area mode:	physical library		

Gate	Instances	Area	Library
Complex_f2	1	5.720	inv
inv	5	7.800	inv
total	6	13.520	

Type	Instances	Area	Area %
inverter	5	7.800	57.7
logic	1	5.720	42.3
physical_cells	0	0.000	0.0
total	6	13.520	100.0

9) Síntese Física:






```

Begin checking placement ... (start mem=1164.4M, init mem=1164.4M)
*info: Recommended don't use cell = 0
*info: Placed = 9
*info: Unplaced = 0
Placement Density:100.00%(18/18)
Placement Density (including fixed std cells):100.00%(18/18)
Finished checkPlace (cpu: total=0:00:00.0, vio checks=0:00:00.0; mem=1164.4M)
#####
# Innovus Netlist Design Rule Check
# Sat Jun 17 00:59:20 2017

#####
Design: TF

----- Design Summary:
Total Standard Cell Number      (cells) : 9
Total Block Cell Number         (cells) : 0
Total I/O Pad Cell Number       (cells) : 0
Total Standard Cell Area        ( um^2) : 17.68
Total Block Cell Area           ( um^2) : 0.00
Total I/O Pad Cell Area         ( um^2) : 0.00

----- Design Statistics:
Number of Instances              : 9
Number of Non-uniquified Insts  : 7
Number of Nets                  : 17
Average number of Pins per Net  : 1.18
Maximum number of Pins in Net   : 2

----- I/O Port summary
Number of Primary I/O Ports     : 5
Number of Input Ports           : 4
Number of Output Ports          : 1
Number of Bidirectional Ports   : 0
Number of Power/Ground Ports    : 0
Number of Floating Ports        *: 0
Number of Ports Connected to Multiple Pads *: 0
Number of Ports Connected to Core Instances : 5

----- Design Rule Checking:
Number of Output Pins connect to Power/Ground *: 0
Number of Insts with Input Pins tied together ?: 0
Number of TieHi/Lo term nets not connected to instance's PG terms ?: 0
Number of Input/InOut Floating Pins           : 0
Number of Output Floating Pins                 : 0
Number of Output Term Marked TieHi/Lo         *: 0

Number of nets with tri-state drivers          : 0
Number of nets with parallel drivers           : 0
Number of nets with multiple drivers           : 0
Number of nets with no driver (No FanIn)       : 0
Number of Output Floating nets (No FanOut)     : 0
Number of High Fanout nets (>50)              : 0
Checking routing tracks.....
Checking other grids.....
Checking FINFET Grid is on Manufacture Grid....
Checking core/die box is on Grid.....

```

```

checking snap rule .....

checking Row is on grid.....

checking AreaIO row.....
checking routing blockage.....
checking components.....
checking IO Pins.....
Unplaced Io Pins = 5
checking constraints (guide/region/fence).....
checking groups.....

checking Ptn Pins .....
checking Ptn Core Box.....

checking Preroutes.....
No. of regular pre-routes not on tracks : 0
Design check done.
Report saved in file checkDesign/TF.main.htm.ascii.
*** Message Summary: 0 warning(s), 0 error(s)

0

```

Depth	Name	#Inst	Area (um^2)
0	TF	6	13.52
1			