HDM

ASSIGNMENT

SUBMITTED BY:

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Q. Implement a Band Gap reference Circuit, with Vref = 1.2 V, Temp. coefficient < = 200ppm/0C (for the worst case). You can use any topology of your choice. Also, show Vout vs. VDD and minimize the effect of supply voltage variation in output voltage.

Bandgap Reference :-

A bandgap Voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits.

* It produces a fixed (constant) voltage regardless of powersupply variations, temperature changes or circuit loading from a device.

* A Bandgap reference circuit (BGR) can be built by using the characteristics of variation in voltage with respect to temperature in a diode and a resistor.

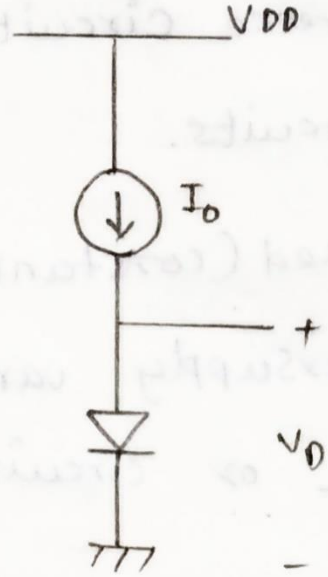
* A diode shows inverse proportionality w.r.t temperature ; i.e. complimentary to absolute temperature (CTAT)

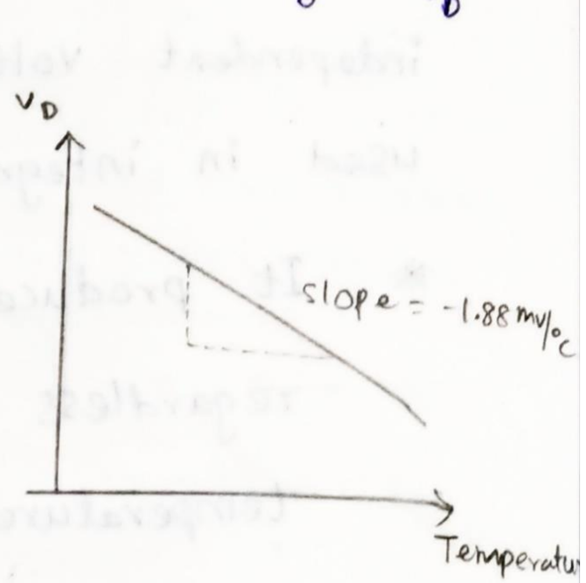
* A resistor shows direct proportionality w.r.t temperature ; i.e; proportional to absolute temperature (PTAT)

* Summung the characteristics of CTAT & PTAT would cancel the variation and would give const. volta

Design of CTAT Circuit

* Consider a diode with diode voltage 'V_D'





* Assume that a constant current is passed through the diode, then the voltage across the diode can be derived from its current equation as

$$I_D = I_s e^{V_D/V_t}$$

$$\therefore V_D = \underbrace{V_T}_{PTAT} \cdot \underbrace{\ln\left(\frac{I_D}{I_s}\right)}_{CTAT}$$

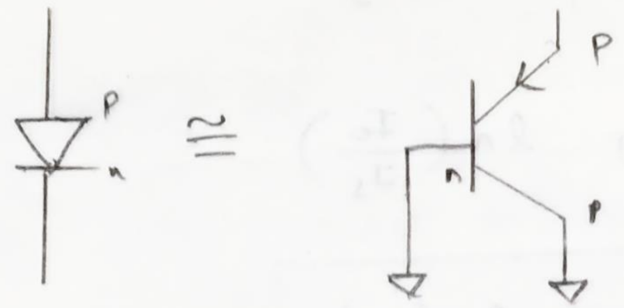
where V_T = Thermal voltage

* To find the variation of diode voltage 'V_D' w.r.t, we differentiate V_D wrt Temp (T) and it's absolute value of change is found as

$$\boxed{\frac{\partial V_D}{\partial T} = -1.88 \text{ mV/°C}}$$

* It is therefore observed that 'V_D' exhibits CTAT characteristics ($\because V_T$ is very low & I_s is high)

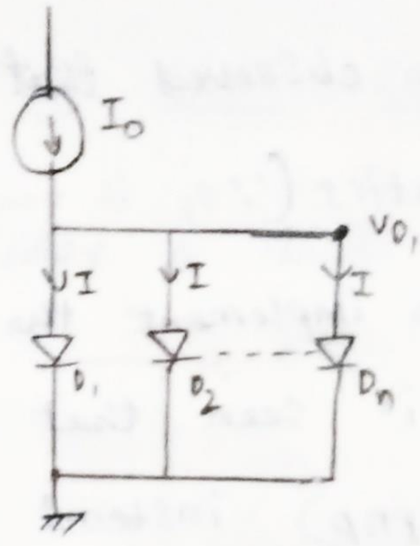
* When we try to implement the above circuit in practise; it is seen that we end up getting a BJT (pnp) instead of a diode, due to current flow characteristics,



Design of PTAT circuit :-

* From above circuitary, it is seen that V_T exhibits PTAT characteristics and I_s exhibits CTAT characteristics, so the CTAT term should be minimised to get PTAT characteristics.

* We can increase the number of diodes in parallel to get dominating PTAT curve



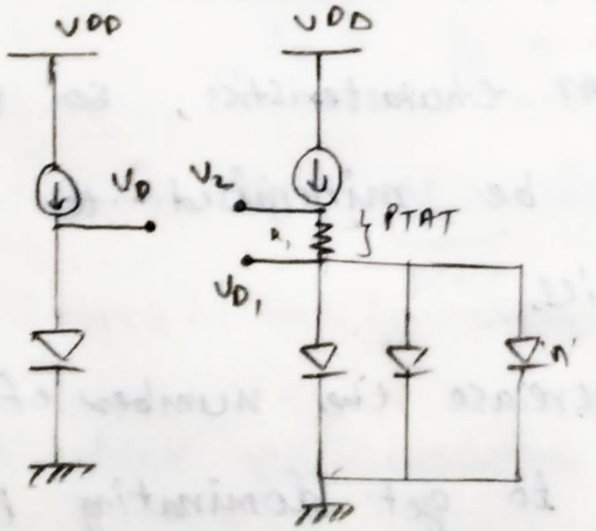
$$V_{D_1} = V_T \ln\left(\frac{I_o}{n I_s}\right) \text{ ——— (1)} \quad \Big| \; n = \text{no. of diodes in parallel} \Big)$$

WKT,

$$V_D = V_T \ln\left(\frac{I_o}{I_s}\right) \text{ ——— (2)}$$

$$\boxed{V_D - V_{D_1} = V_T \ln(n)}$$

* Here, as $\ln(n)$ is a constant; the above equation exhibits PTAT characteristics,



* if we can make the potentials $V_D = V_2$ and the current in the both branches equal then this circuit can act as PTAT

$V_D = V_2$

i.e, $V_D = I_0 R_1 + V_{D1}$

$$V_D - V_{D1} = \underbrace{I_0 R_1}_{PTAT}$$

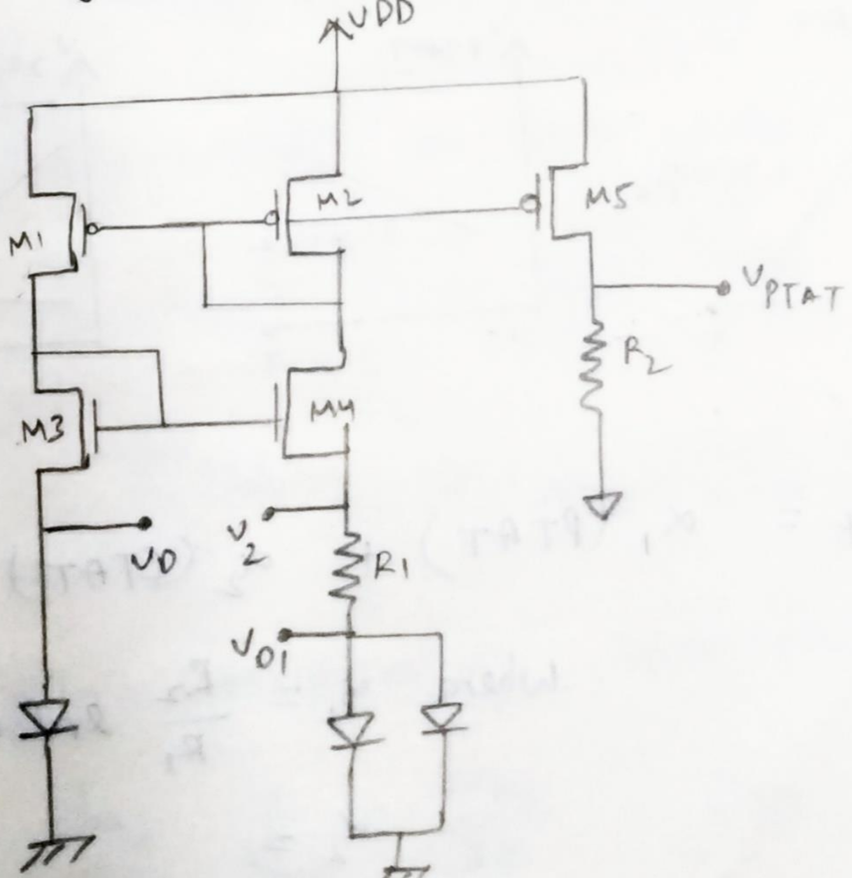
* The voltages $V_D = V_2$ and currents I_0 can be made equal by 2 possible ways.

(i) By using op-amps

(ii) By using current mirrors.

(i) using op-amp :-

(i) using current mirror :-



Voltage across R_2

$$V_{R2} = I_o R_2$$

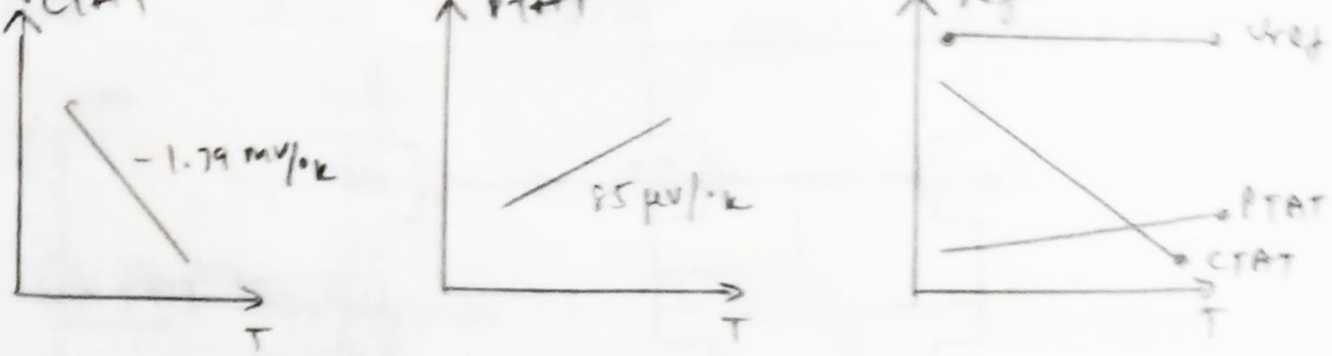
$$V_{R_2} = \frac{R_2}{R_1} \ln(n) \underbrace{V_T}_{PTAT}$$

and $\frac{\partial V_T}{\partial T}$ is found as $\boxed{\frac{\partial V_T}{\partial T} = 86\ \mu V/°K}$

and using these, $\frac{\partial V_D}{\partial T} = -1.79\ mV/°K$

Design of BGR Circuit :-

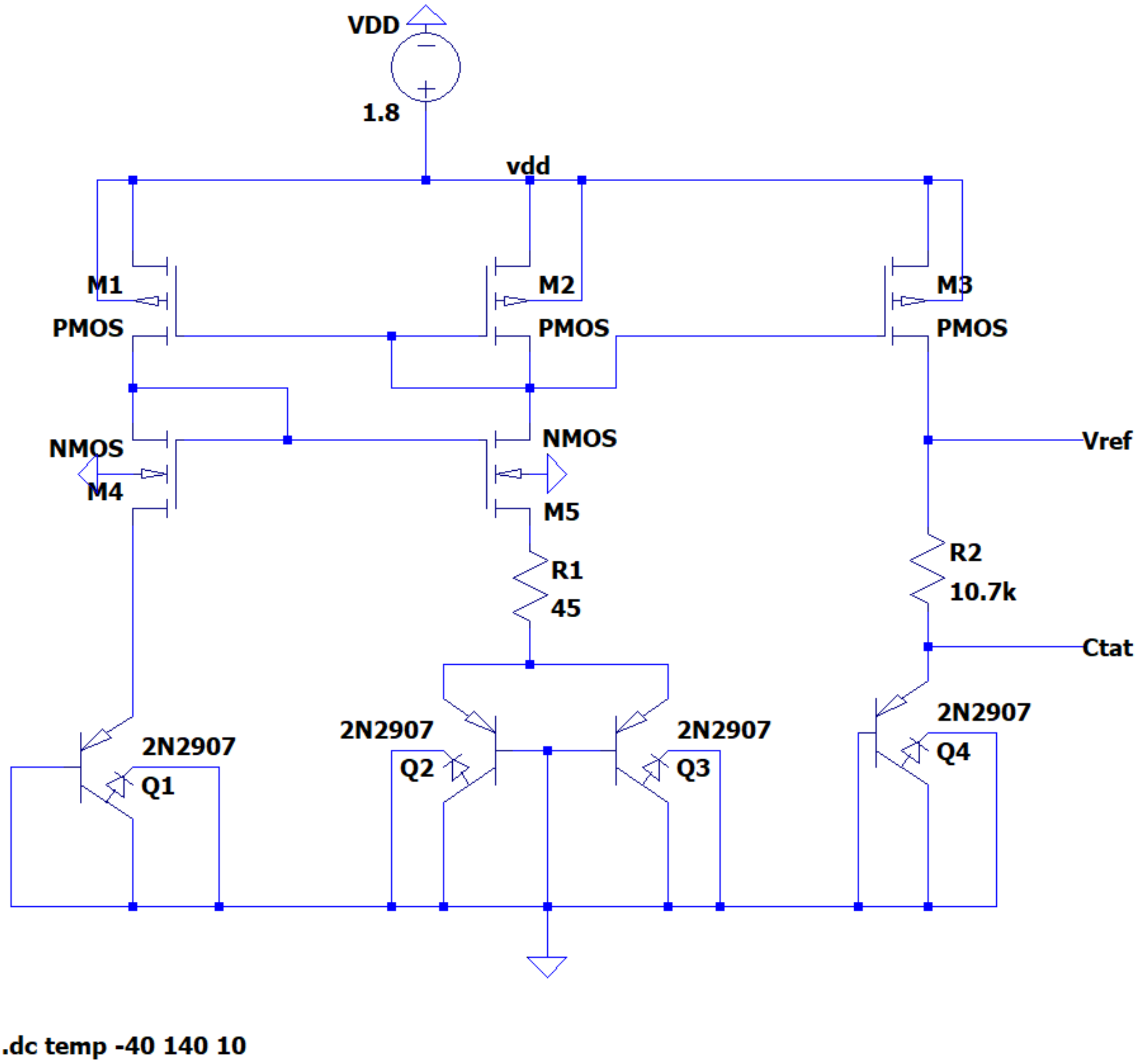
* Summing up the CTAT & PTAT curves we end up getting BGR circuit

* 

$$V_{ref} = \alpha_1 (PTAT) + \alpha_2 (CTAT)$$

where $\alpha_1 = \frac{R_2}{R_1} \ln(n)$

BGR Circuit



VDD
1.8
vdd
M1
PMOS
M2
PMOS
M3
PMOS
NMOS
M4
NMOS
M5
Vref
R2
10.7k
R1
45
Ctat
2N2907
Q1
2N2907
Q2
2N2907
Q3
2N2907
Q4
.dc temp -40 140 10

* as the slope of PTAT is very low and CTAT is very high, we either have to increase PTAT slope or decrease CTAT slope,

* But decreasing CTAT slope means increasing no of diodes in parallel, which is not feasible; so we have to increase PTAT slope to obtain constant BGR curve; i.e; $\alpha_2 = 1$ (constant)

Then $\cancel{V_{ref}} = \alpha_1 (\cancel{85\,\mu V/°K}) - \cancel{1.6\,mV/°K}$

$$V_{ref} = \alpha_1 V_T + V_D$$

differentiate on both sides

$$\frac{\partial}{\partial T}(V_{ref}) = \alpha_1 \frac{\partial V_T}{\partial T} + \frac{\partial V_D}{\partial T}$$

$$\frac{\partial V_{ref}}{\partial T} = \alpha_1 (85\,\mu V/°K) + (-1.79\,mV/°K)$$

* given temperature coefficient = 2200 PPM/°C

i.e; $\frac{1}{V_{ref}} \times \frac{\partial V_{ref}}{\partial T} = 200$

$$\therefore \frac{1}{V_{ref}} \times \frac{\partial V_{ref}}{\partial T} = \frac{1}{V_{ref}}\left[\alpha_1 (85\mu) - 1.6m\right]$$

$$\frac{200 \times 1.2}{10^6} = \alpha_1 \times 85 \times 10^{-6} - 1.6 \times 10^{-3}$$

$$240 = 85\,\alpha_1 - 1790$$

$$\boxed{\alpha_1 = 23.82}$$

WKT,

$$\alpha_1 = \frac{R_2}{R_1} \times \ln(n)$$

if $n = 2$,

Then $$\frac{R_2}{R_1} = \frac{\alpha_1}{\ln(2)}$$

$$= 34.45$$

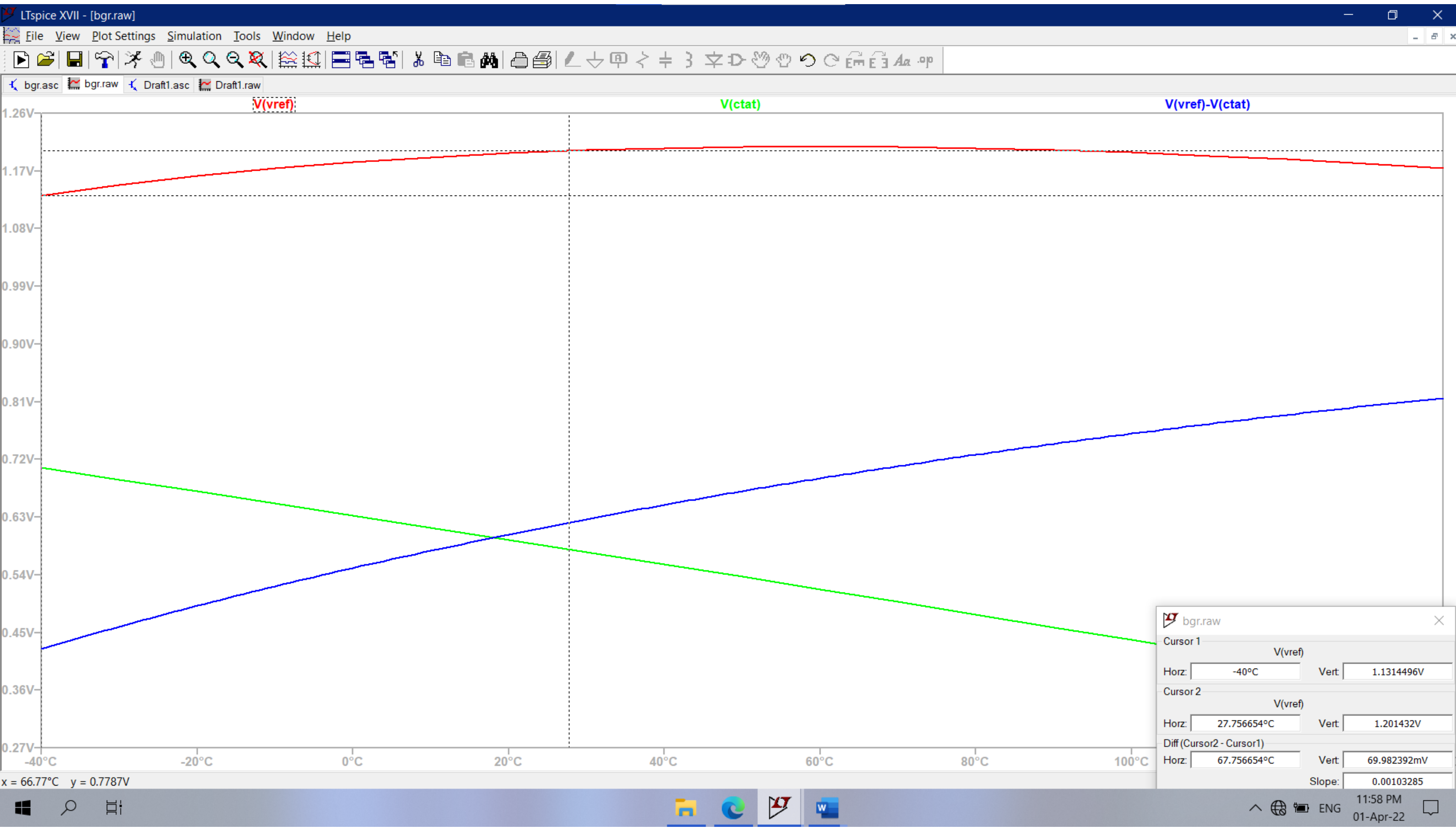
The value of R_2 and R_1 can be varied to get correct value of reference voltage by keeping the ratio $\frac{R_2}{R_1}$ in mind.

CIRCUIT NETLIST

```
* F:\1.Mtech\LTSPICE\spice-examples\BGR\bgr.asc
M1 vdd N001 N002 vdd PMOS l=180n w=1.22u
M2 vdd N001 N001 vdd PMOS l=180n w=1u
M3 vdd N001 Vref vdd PMOS l=180n w=1u
R1 N003 N004 45
R2 Vref Ctat 10.7k
VDD vdd 0 1.8
M4 N005 N002 N002 0 NMOS l=180n w=390n
M5 N003 N002 N001 0 NMOS l=180n w=500n
Q1 0 0 N005 0 2N2907
Q2 0 0 N004 0 2N2907
Q3 0 0 N004 0 2N2907
Q4 0 0 Ctat 0 2N2907
.model NPN NPN
.model PNP PNP
.lib C:\Users\shamb\Documents\LTspiceXVII\lib\cmp\standard.bjt
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\shamb\Documents\LTspiceXVII\lib\ cmp\standard.mos
```

Note : Level 49 MOS model file is used for simulation

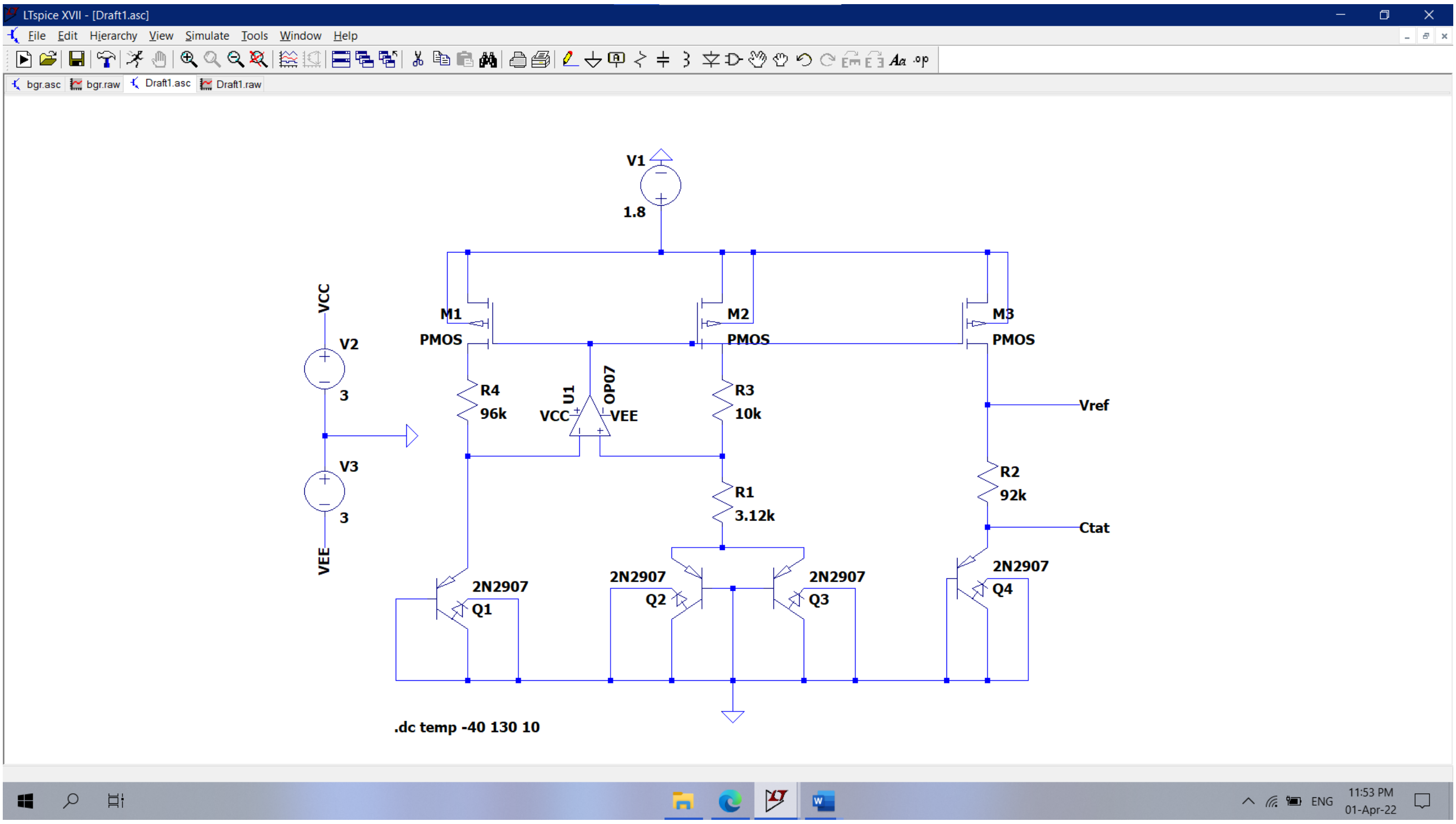
SIMULATION GRAPHS



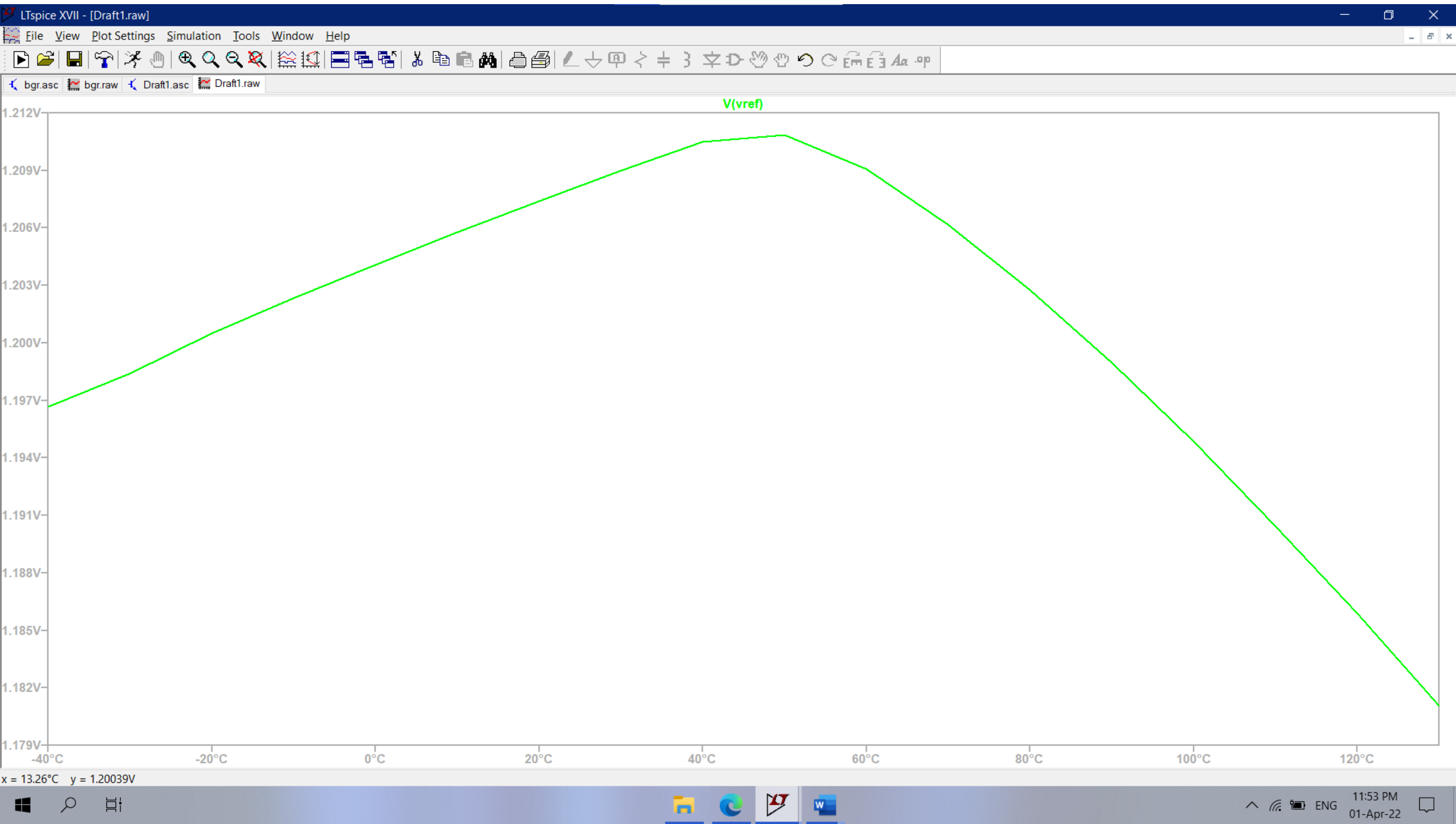
ii) using op-Amp :-

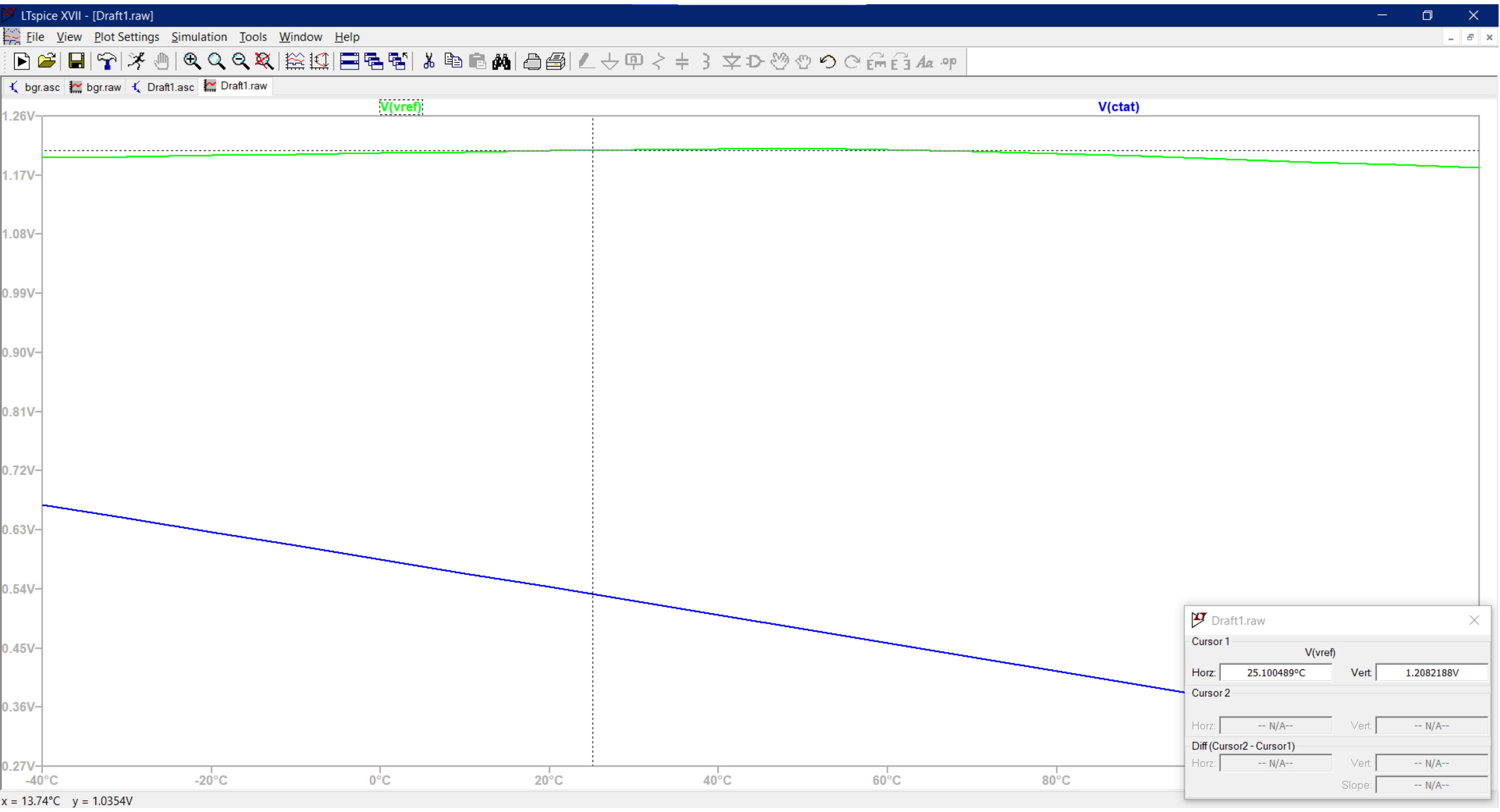
Similar circuit and results can be obtained by taking op-amp for equaling the node currents and $V_D = V_2$ voltages.

BGR using OP-AMP



SIMULATION GRAPHS




LTspice XVII - [Draft1.raw]
File View Plot Settings Simulation Tools Window Help
bgr.asc bgr.raw Draft1.asc Draft1.raw
V(vref)
V(ctat)
1.26V
1.17V
1.08V
0.99V
0.90V
0.81V
0.72V
0.63V
0.54V
0.45V
0.36V
0.27V
-40°C
-20°C
0°C
20°C
40°C
60°C
80°C
Draft1.raw
Cursor 1
V(vref)
Horz: 25.100489°C
Vert: 1.2082188V
Cursor 2
Horz: -- N/A--
Vert: -- N/A--
Diff (Cursor2 - Cursor1)
Horz: -- N/A--
Vert: -- N/A--
Slope: -- N/A--
x = 13.74°C y = 1.0354V