11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

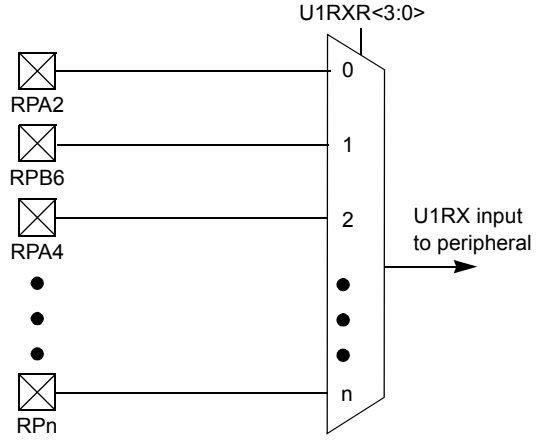
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to ‘1’).

TABLE 11-1: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT4	INT4R	INT4R<3:0>	0000 = RPA0 0001 = RPB3 0010 = RPB4 0011 = RPB15 0100 = RPB7 0101 = RPC7(2) 0110 = RPC0(1) 0111 = RPC5(2) 1000 = Reserved • • • 1111 = Reserved
T2CK	T2CKR	T2CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
$\overline{SS1}$	SS1R	SS1R<3:0>	
REFCLKI	REFCLKIR	REFCLKIR<3:0>	
INT3	INT3R	INT3R<3:0>	0000 = RPA1 0001 = RPB5 0010 = RPB1 0011 = RPB11 0100 = RPB8 0101 = RPA8(2) 0110 = RPC8(2) 0111 = RPA9(2) 1000 = Reserved • • • 1111 = Reserved
T3CK	T3CKR	T3CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
$\overline{U1CTS}$	U1CTSR	U1CTSR<3:0>	
U2RX	U2RXR	U2RXR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
INT2	INT2R	INT2R<3:0>	0000 = RPA2 0001 = RPB6 0010 = RPA4 0011 = RPB13 0100 = RPB2 0101 = RPC6(2) 0110 = RPC1(1) 0111 = RPC3(1) 1000 = Reserved • • • 1111 = Reserved
T4CK	T4CKR	T4CKR<3:0>	
IC1	IC1R	IC1R<3:0>	
IC5	IC5R	IC5R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
$\overline{U2CTS}$	U2CTSR	U2CTSR<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
OCFB	OCFBR	OCFBR<3:0>	
INT1	INT1R	INT1R<3:0>	0000 = RPA3 0001 = RPB14 0010 = RPB0 0011 = RPB10 0100 = RPB9 0101 = RPC9(1) 0110 = RPC2(2) 0111 = RPC4(2) 1000 = Reserved • • • 1111 = Reserved
T5CK	T5CKR	T5CKR<3:0>	
IC2	IC2R	IC2R<3:0>	
$\overline{SS2}$	SS2R	SS2R<3:0>	
OCFA	OCFAR	OCFAR<3:0>	

Note 1: This pin is not available on 28-pin devices.

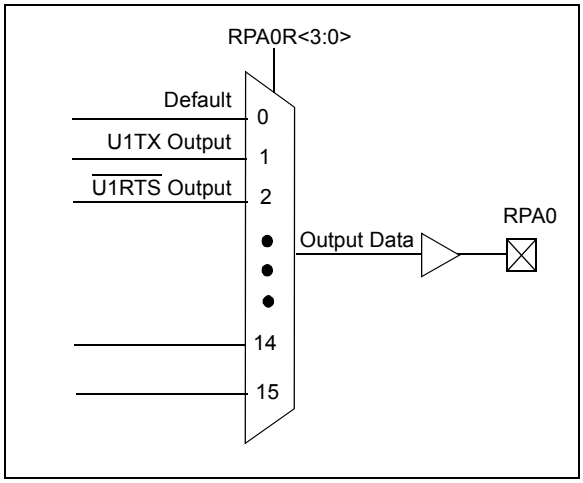
2: This pin is only available on 44-pin devices.

11.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 11-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 11-2 and Figure 11-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0



11.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

11.3.6.1 Control Register Lock Sequence

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the Configuration bit, IOLOCK (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

11.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The Configuration bit, IOL1WAY (DEVCFG3<29>), blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

TABLE 11-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA0	RPA0R	RPA0R<3:0>	0000 = No Connect 0001 = U1TX 0010 = U2RTS 0011 = SS1 0100 = Reserved 0101 = OC1 0110 = Reserved 0111 = C2OUT 1000 = Reserved . . . 1111 = Reserved
RPB3	RPB3R	RPB3R<3:0>	
RPB4	RPB4R	RPB4R<3:0>	
RPB15	RPB15R	RPB15R<3:0>	
RPB7	RPB7R	RPB7R<3:0>	
RPC7	RPC7R	RPC7R<3:0>	
RPC0	RPC0R	RPC0R<3:0>	
RPC5	RPC5R	RPC5R<3:0>	
RPA1	RPA1R	RPA1R<3:0>	0000 = No Connect 0001 = Reserved 0010 = Reserved 0011 = SDO1 0100 = SDO2 0101 = OC2 0110 = Reserved 0111 = C3OUT . . . 1111 = Reserved
RPB5	RPB5R	RPB5R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPB11	RPB11R	RPB11R<3:0>	
RPB8	RPB8R	RPB8R<3:0>	
RPA8	RPA8R	RPA8R<3:0>	
RPC8	RPC8R	RPC8R<3:0>	
RPA9	RPA9R	RPA9R<3:0>	
RPA2	RPA2R	RPA2R<3:0>	0000 = No Connect 0001 = Reserved 0010 = Reserved 0011 = SDO1 0100 = SDO2 0101 = OC4 0110 = OC5 0111 = REFCLKO 1000 = Reserved . . . 1111 = Reserved
RPB6	RPB6R	RPB6R<3:0>	
RPA4	RPA4R	RPA4R<3:0>	
RPB13	RPB13R	RPB13R<3:0>	
RPB2	RPB2R	RPB2R<3:0>	
RPC6	RPC6R	RPC6R<3:0>	
RPC1	RPC1R	RPC1R<3:0>	
RPC3	RPC3R	RPC3R<3:0>	
RPA3	RPA3R	RPA3R<3:0>	0000 = No Connect 0001 = U1RTS 0010 = U2TX 0011 = Reserved 0100 = SS2 0101 = OC3 0110 = Reserved 0111 = C1OUT 1000 = Reserved . . . 1111 = Reserved
RPB14	RPB14R	RPB14R<3:0>	
RPB0	RPB0R	RPB0R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPC9	RPC9R	RPC9R<3:0>	
RPC2	RPC2R	RPC2R<3:0>	
RPC4	RPC4R	RPC4R<3:0>	