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3.	OR Gate	"	8 - 11	
4.	NAND Gate	27 th Dec	12 - 15	
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10.	Half - Adder	26 th feb	36 - 39	
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1. Title : NOT Gate

2. OBJECTIVE :

- To implement and verify NOT gate operations.
- To find the relationship between inputs and output using the NOT IC 7404

3. COMPONENTS:

- 7404 (NOT GATE) IC
- Digital kit
- Connecting wires
- Power supply

4. THEORY:

* INTRODUCTION

- The Output of NOT gate is HIGH, when input is LOW.
- The Output of NOT gate is LOW, when input is HIGH.

* FUNCTIONAL EXPRESSION

- $$y = \bar{A}$$

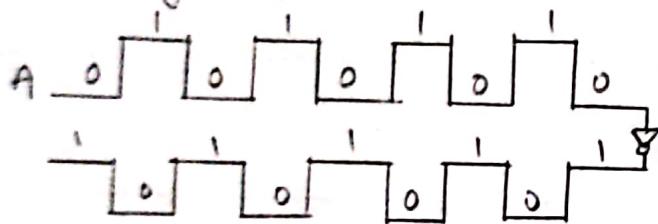


* Fig : Logic circuit

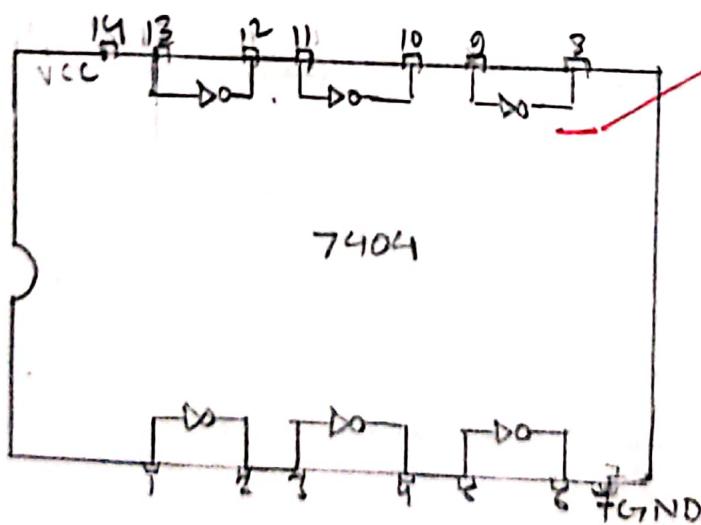
* Truth Table

NOT OPERATION	
Input(A)	Output(\bar{A})
0	1
1	0

* Timing Diagram



* fig:- Timing Diagram for NOT gate



* Pin configuration

5. PROCEDURE :

- Implement the circuit by using 7404 IC
- Adjust connecting wires properly on the digital kit.
- ~~Apply the power supply.~~
- ~~Observe the relationship between I/O.~~

6. RESULT :

As a result in NOT gate we obtain that if we put the input HIGH then, it produce LOW output and when we put the LOW input then it produce HIGH output.

1. TITLE : AND Gate

2. OBJECTIVE :

- To implement and verify AND gate operation
- To find the relationship between inputs and outputs using the AND IC 7408.

3. COMPONENTS :

- 7408 (AND Gate) IC
- Digital kit
- Connecting wires
- Power supply.

4. THEORY :

* Introduction

- The output of AND gate is HIGH, if all the inputs are HIGH.
- The Output of AND gate is LOW, if any one of the inputs is LOW.

* Functional Expression

$$\boxed{y = AB}$$

5. PROCEDURES :

- Implement the circuit by using 7408 IC.
- Adjust connecting wires properly on the digital kit.

Sequence

Truth Table

Inputs		Output
A	B	$A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

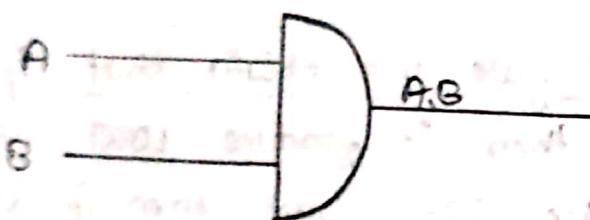


fig: Logic circuit

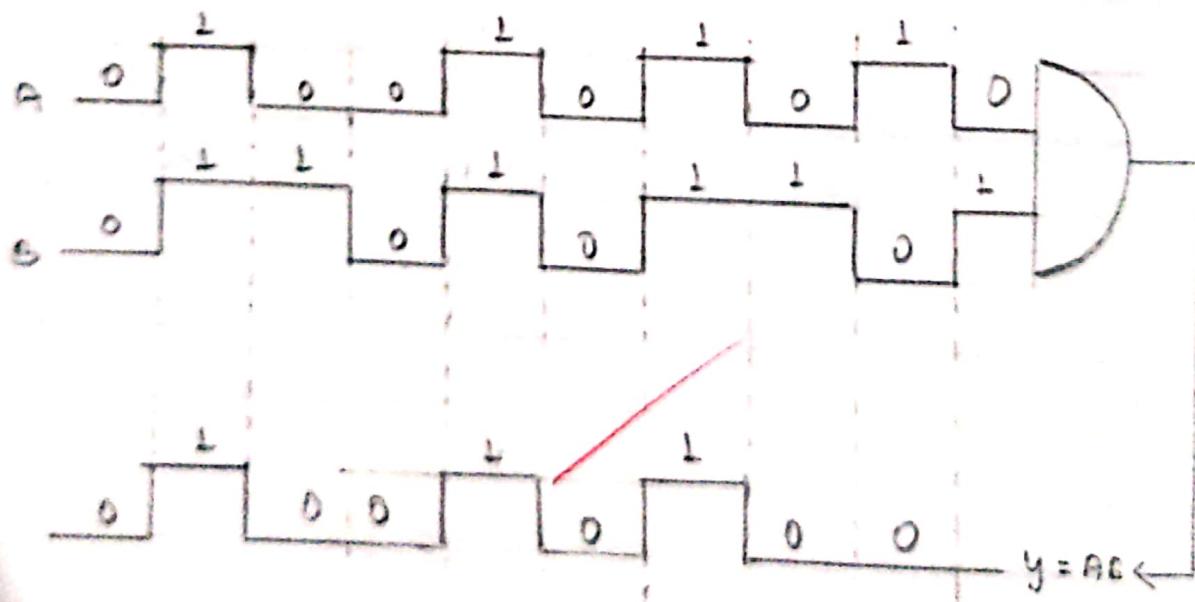


fig: Timing Diagram

- Apply power supply.
- Observe the relationship between I/O.

~~6. RESULT:~~

When all the inputs of AND gate is HIGH then only output becomes HIGH otherwise output will be LOW.

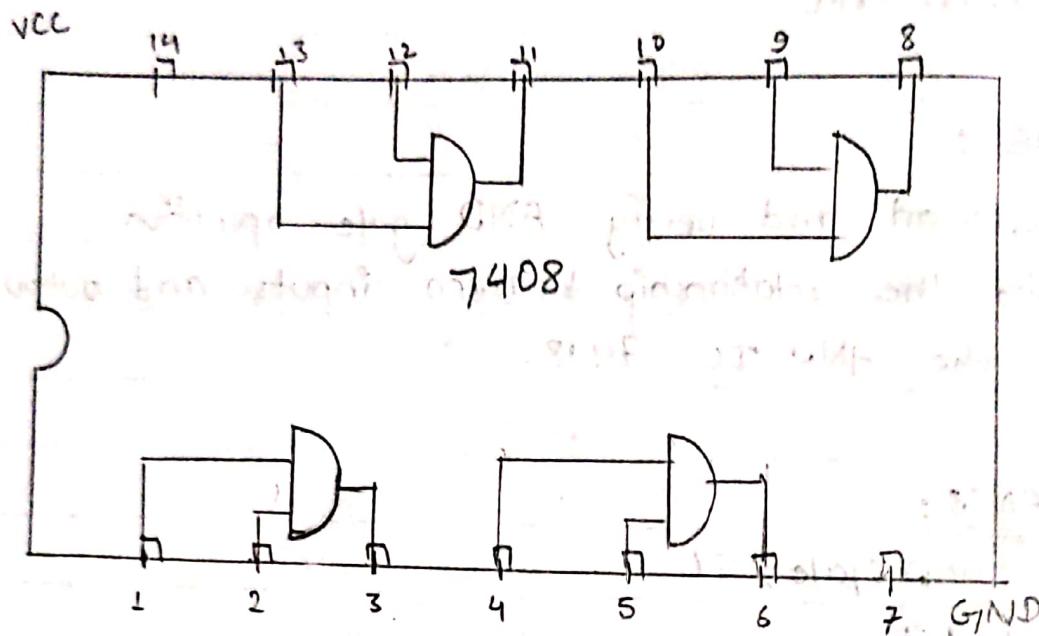


Fig: Pin Diagram



1. TITLE : OR Gate

2. OBJECTIVE:

- To implement and verify OR gate operation.
- To find the relationship between inputs and outputs using OR gate (OR IC 7432)

3. COMPONENTS:

- 7432 (OR gate) IC
- Digital Kit
- Connecting wires
- Power Supply

4. THEORY:

* Introduction:

- The output of OR gate is HIGH if anyone of the inputs is HIGH.

- The output of OR gate is LOW, if all the inputs are LOW.

* Functional Expression:

$$\boxed{y = A + B}$$

TRUTH TABLE

Inout	Output	
A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1

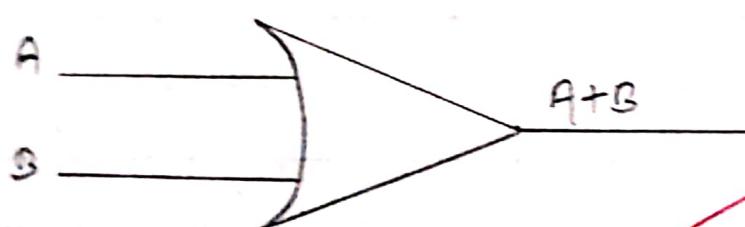


fig:- Logic circuit

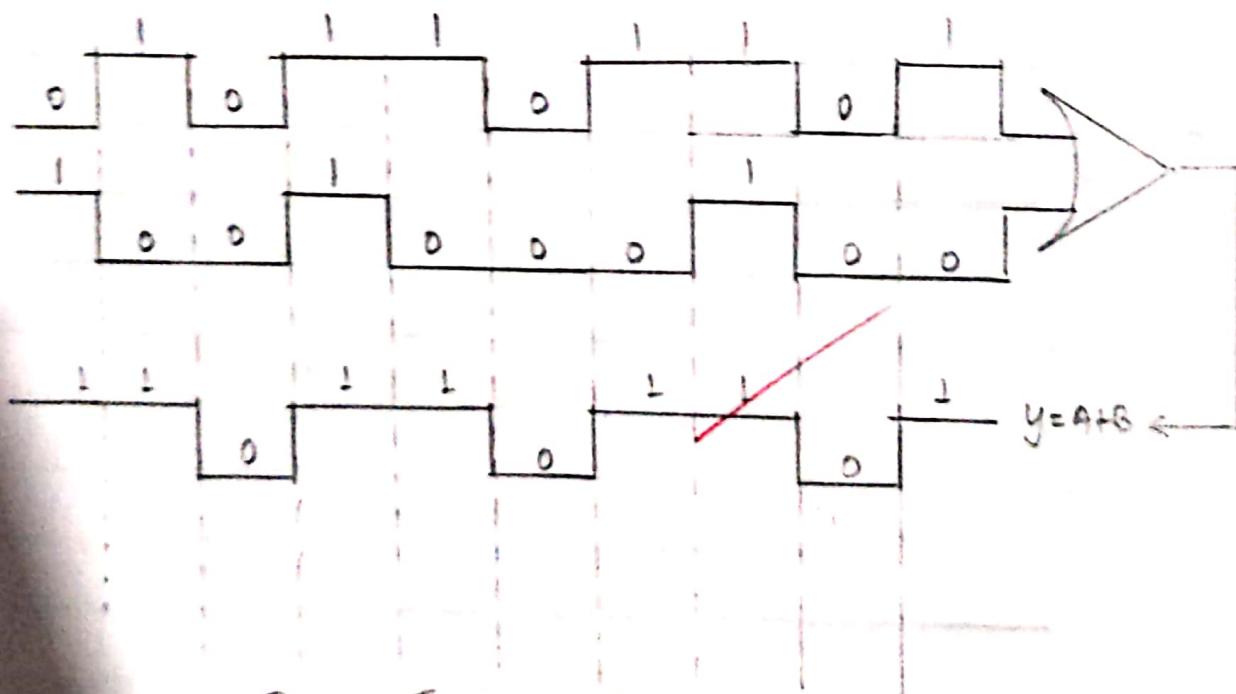


Fig:- Timing Diagram

5. PROCEDURES :

- Implement the circuit by using 7332 IC
- Adjust the connecting wires properly on the digital kit.
- Apply power supply.
- Observe the relationship between I/O.

6. RESULT :

- The output of OR gate is HIGH if anyone of the INPUT is HIGH.
- The output of OR gate is LOW when all the inputs are LOW.

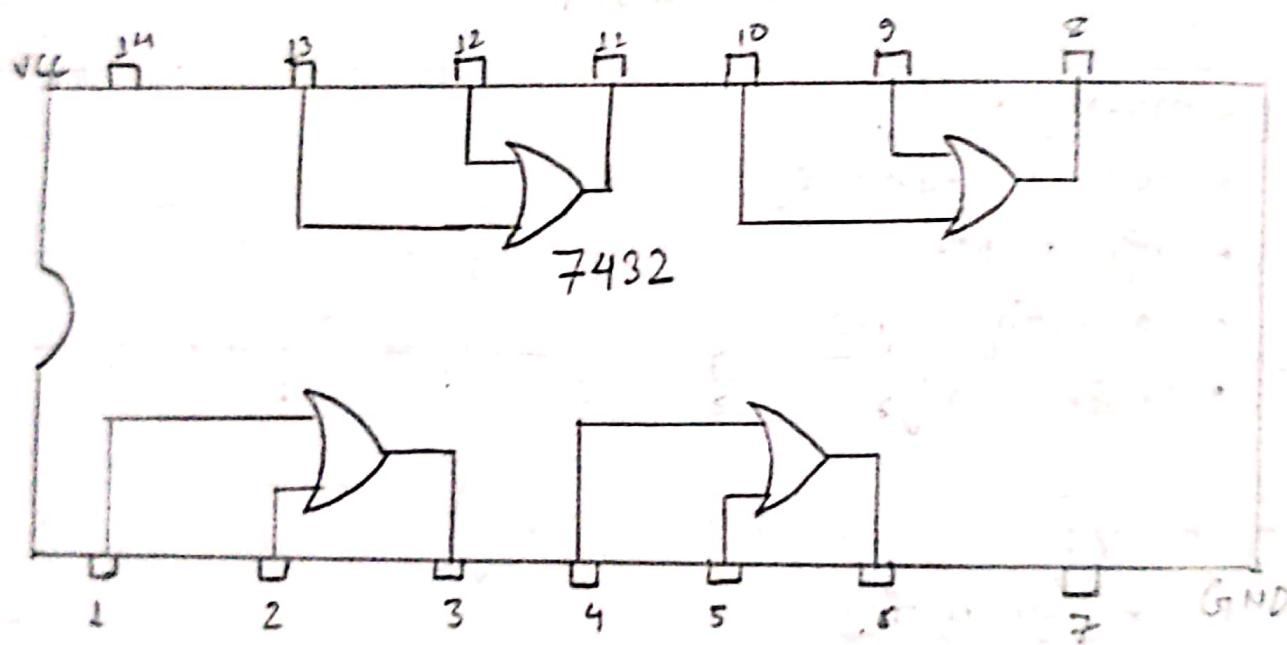


Fig :- Pin Diagram

1. TITLE : NAND Gate

2. OBJECTIVE :

- To implement and verify NAND Gate operation.
- To find the relationship between inputs and outputs using NAND IC Number - 7400

3. COMPONENTS :

- 7400 (NAND gate) IC
- Digital kit
- Connecting wires
- Power supply

4. THEORY :

* Introduction

- The output of NAND gate is HIGH if any one of the inputs is low.
- The output of NAND gate is LOW, if all the inputs are HIGH.

* Functional Expression

$$\bullet \boxed{Y = \overline{A \cdot B}}$$

TRUTH TABLE

Input	Output		
A	B	AB	$\bar{A}B$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

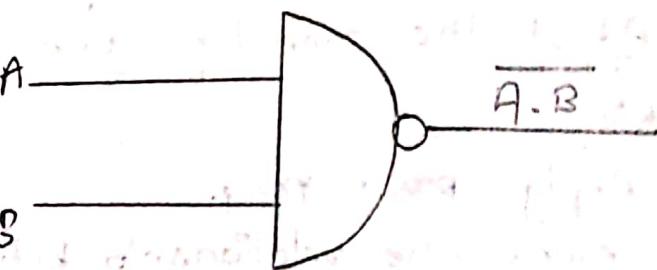


fig:- Logic circuit of NAND gate

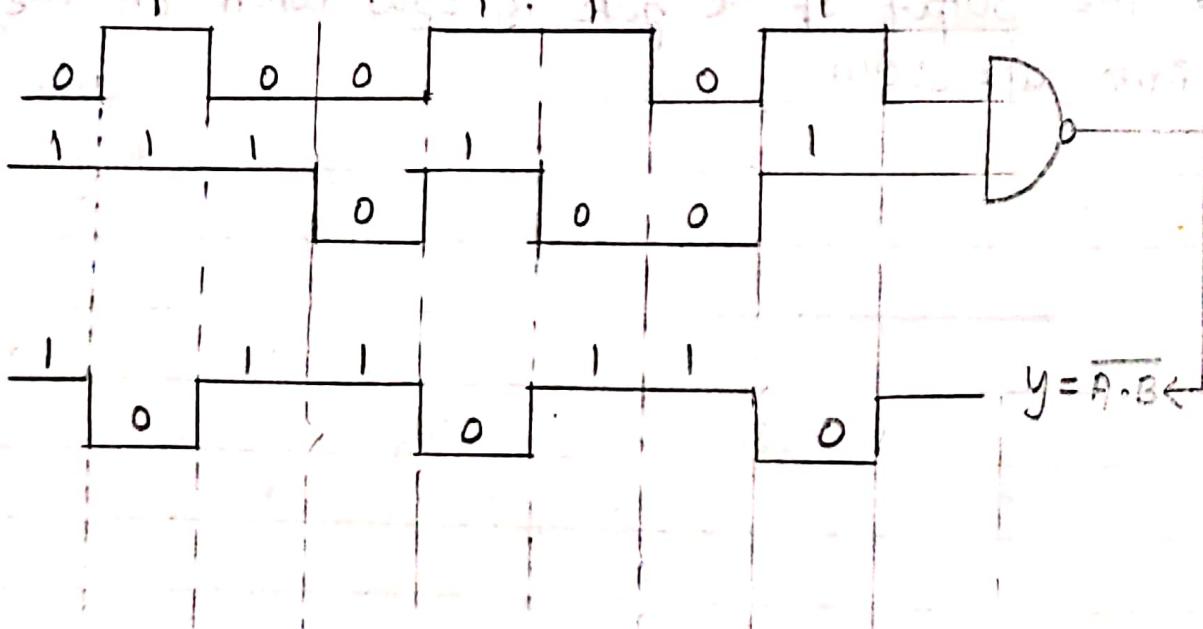


fig:- Timing Diagram

5. PROCEDURE :

- Implement the circuit by using 7400 IC
- Adjust connecting wires properly on digital kit.
- Apply the power supply.
- Observe the relationship between I/O.

6. RESULT :

As a result we obtain the output HIGH when any one of the input is HIGH and output LOW when all the inputs are HIGH.

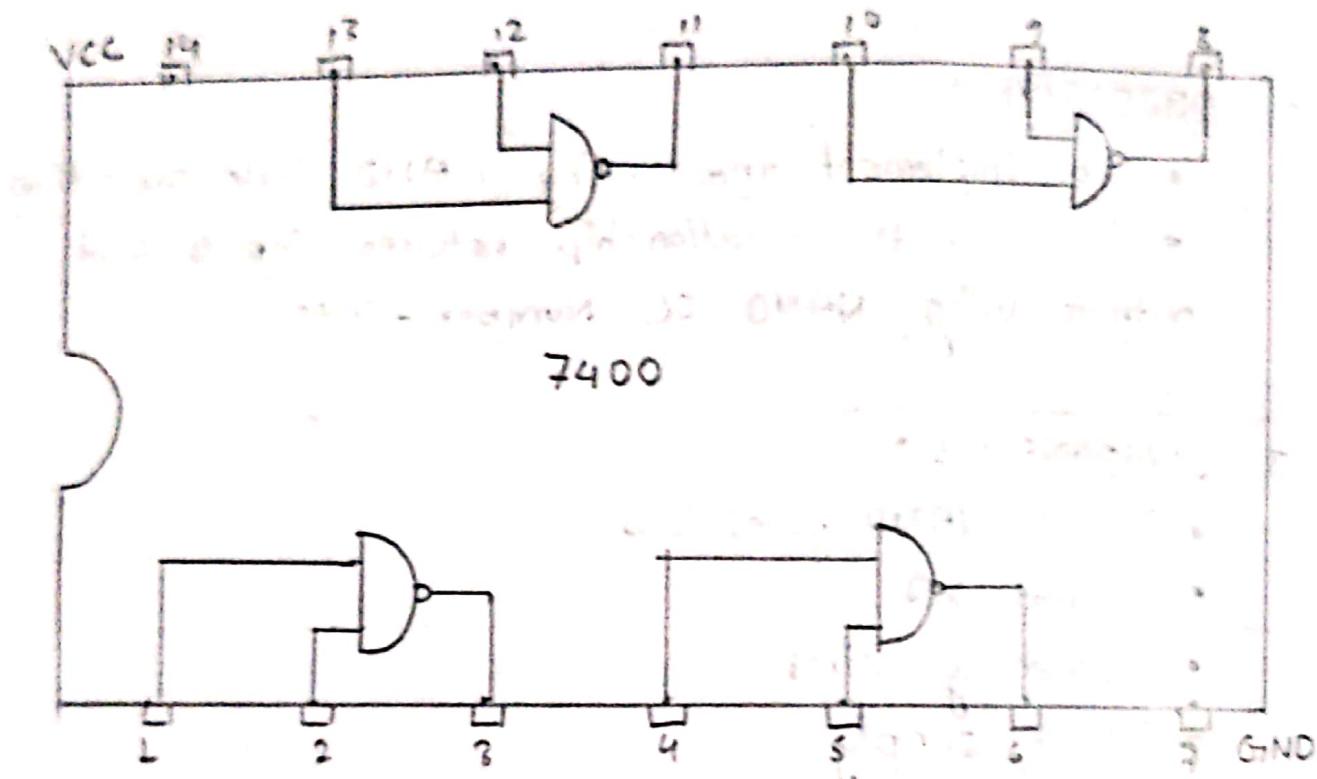


Fig :- Pin Diagram

TITLE : NOR Gate

OBJECTIVE :

- To implement and verify NOR gate operation.
- To find the relationship between I/O using NOR IC Number - 7402.

APPARATUS :

- 7402 (NOR gate) IC
- Digital kit
- Connecting wires
- Power supply.

THEORY :

* Introduction:

- The Output of NOR gate is HIGH if all the inputs is low.
- The Output of NOR gate is LOW if any of the input is HIGH.

* Functional Expression

- $$y = \overline{A+B}$$

TRUTH TABLE

Input	Output	$A+B$	$\bar{A}+\bar{B}$
0 0	0	1	1
0 1	1	0	0
1 0	1	0	0
1 1	1	0	0

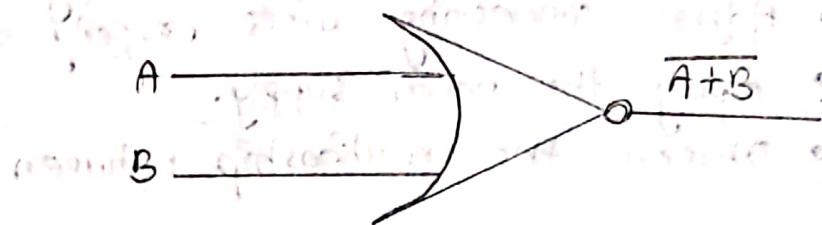


Fig:- Logic circuit of NOR gate

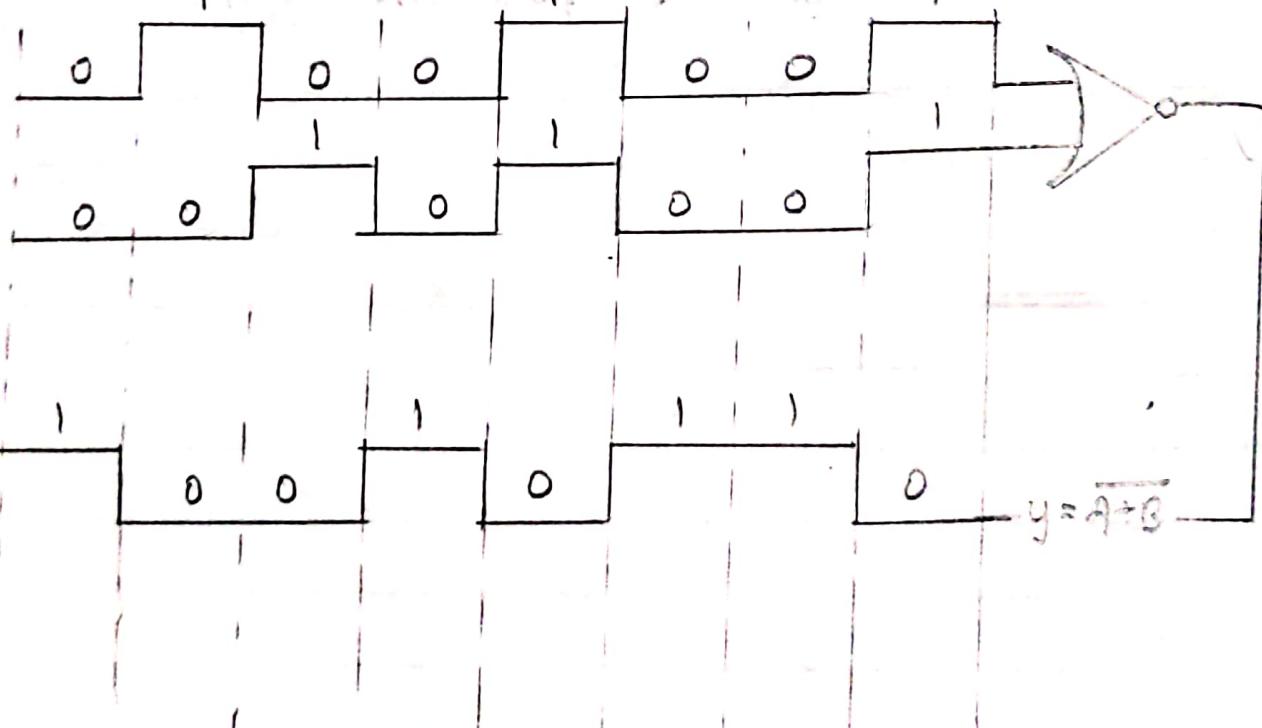


Fig:- Timing Diagram

5. PROCEDURE :

- Implement the circuit by using 7402 IC.
- Adjust connecting wires properly on digital kit.
- Apply the power supply.
- Observe the relationship between I/O.

6. RESULT :

As a result, we get the Output HIGH
when all the inputs are LOW and output LOW
when anyone of the input is HIGH.

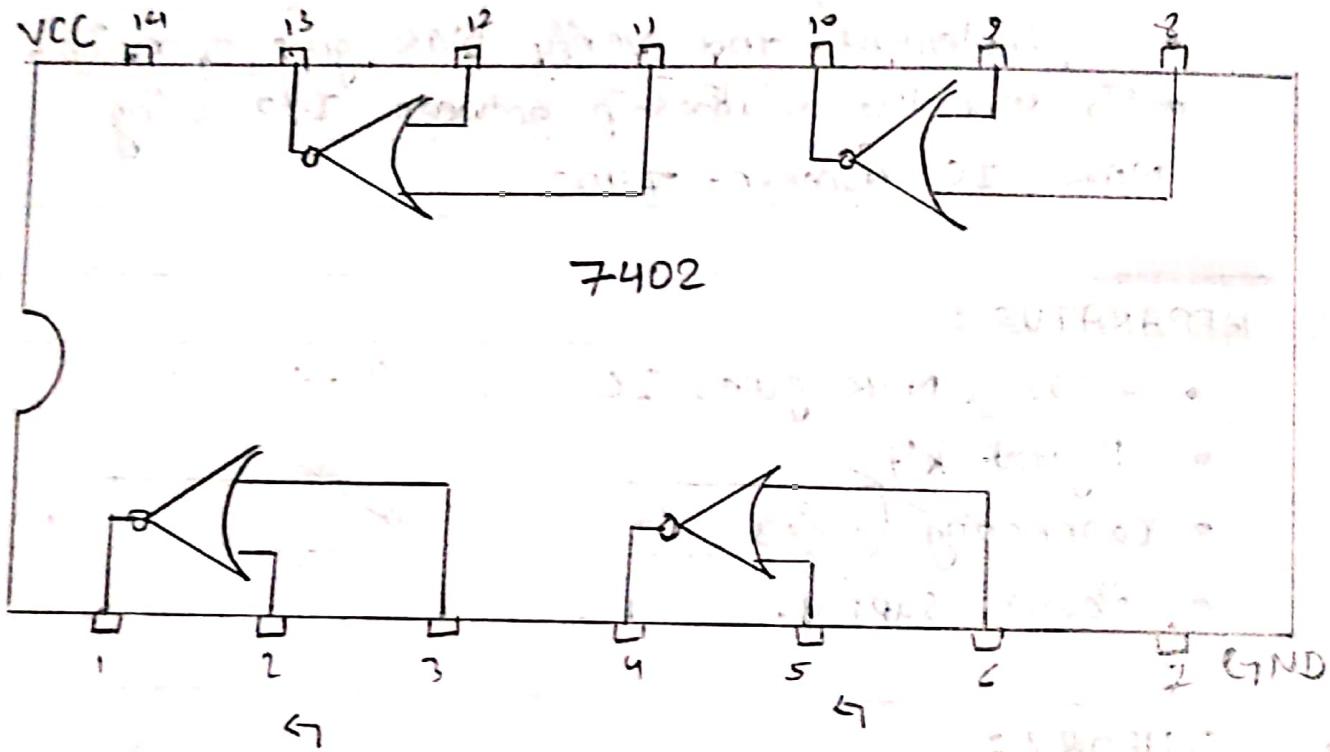


Fig :- Pin configuration.

If both inputs are high, then output will be high.
If one input is high and other is low, then output will be low.



1. TITLE : XOR gate

2. OBJECTIVE :

- To implement and verify XOR gate operation.
- To find the relationship between Inputs and Outputs using XOR IC number - 7486

3. APPARATUS :

- 7486 (XOR gate) IC
- Digital kit
- Connecting wires
- Power supply

4. THEORY :

* Introduction

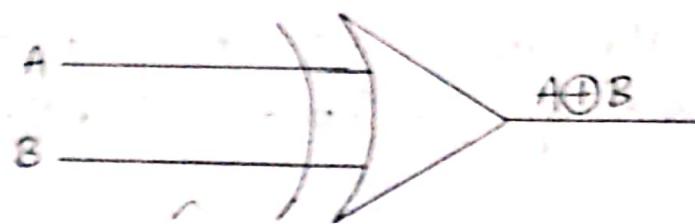
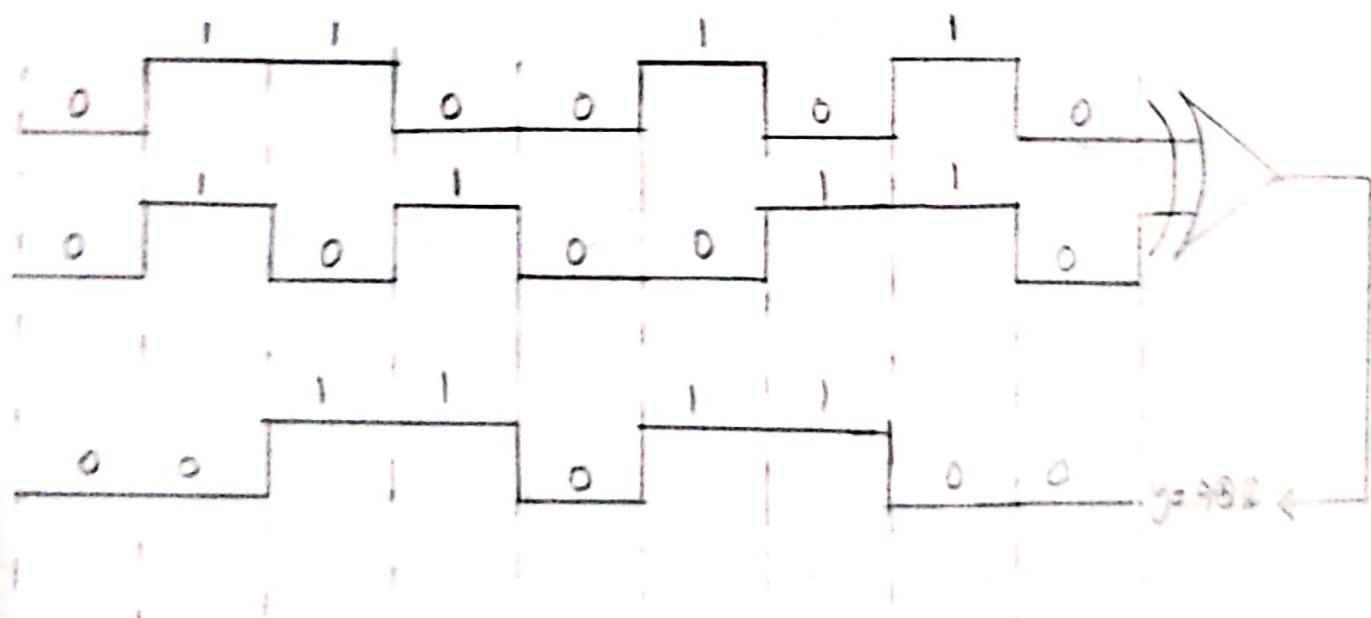
- The output of XOR gate is HIGH when two inputs are at opposite logic level.
- The output of XOR gate is LOW
- XOR gate is an odd no. of 1's detector i.e, odd no. of 1's \Rightarrow Output HIGH.

* Functional Expression

$$y = A \oplus B , A\bar{B} + \bar{A}B$$

Truth Table

Inputs		Outputs					
A	B	\bar{A}	\bar{B}	AB	$\bar{A}B$	$A\bar{B}$	$\bar{A}\bar{B}$
0	0	1	1	0	0	0	0
0	1	1	0	0	1	1	0
1	0	0	1	1	0	1	1
1	1	0	0	0	0	0	0

fig:- Logic circuit of X-OR gatefig:- Timing Diagram

5. PROCEDURE :

- Implement the circuit by using 7486 IC.
- Adjust connecting wires properly in digital kit.
- Apply the power supply.
- Observe the relationship between I/O.

6. RESULT :

As a result, we obtain the result of output HIGH when two inputs are at opposite logic level.

Sagnath

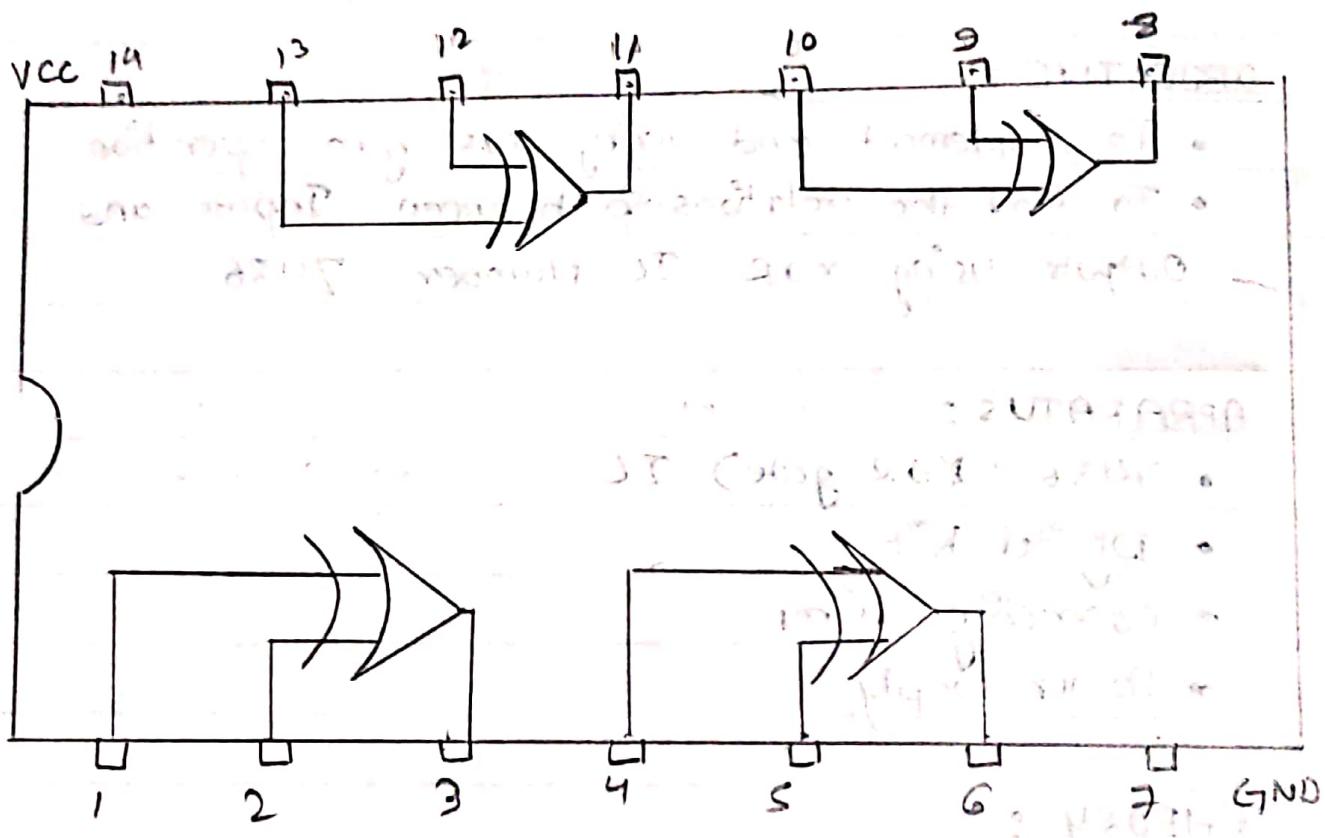


fig:- Pin Configuration

analog multimeter can be connected in
most cases allowing the use of the mult
meter to measure the output voltage
without the need to open the circuit or
remove the probe from the circuit.

Measuring Analog Voltages

1. TITLE : X-NOR Gate

2. OBJECTIVE :

- To implement and verify X-NOR gate operation.
- To find the relationship between Inputs and Output using XNOR IC number - 74266

3. COMPONENTS :

- 74266 (XNOR gate) IC
- Digit Kit
- Connecting wires
- Power supply.

4. THEORY :

* Introduction

- X-NOR is the reverse or complementing form of X-OR
- X-NOR produces output HIGH when two inputs are at same logic level.
- It is known as equivalent gate.

* Functional Expression

$$y = \overline{A \oplus B} , AB + \bar{A}\bar{B}$$

Truth Table

Inputs		Outputs	
A	B	$A \oplus B$	$\bar{A} \oplus B$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

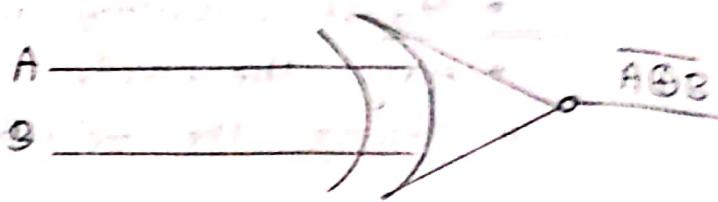


Fig:- Logic circuit of X-NOR gate

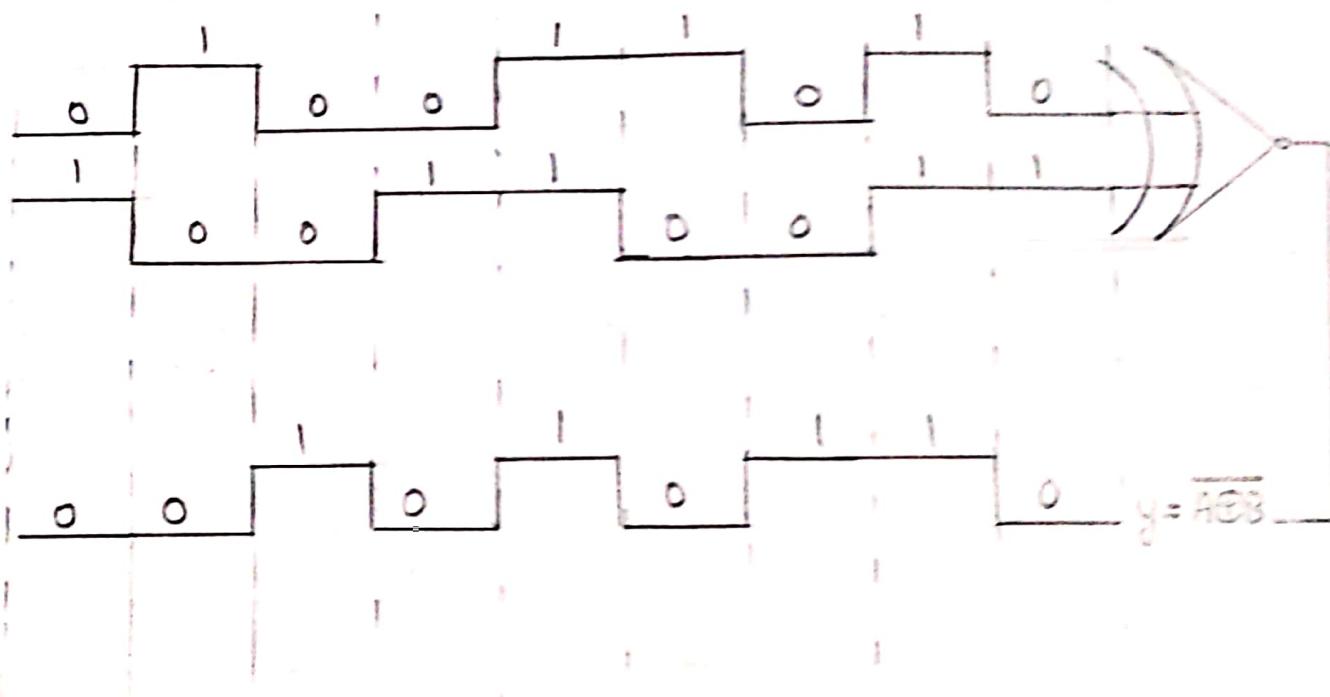


Fig:- Timing Diagram

5. PROCEDURE :

- Implement the circuit by using 74266 IC
- Adjust connecting wires properly in digital kit.
- Apply the power supply.
- Observe the relationship between I/O.

6. RESULT :

As a result, we obtain output HIGH when two inputs are at same logic level. We can also say that when even no. of 1's, output is HIGH

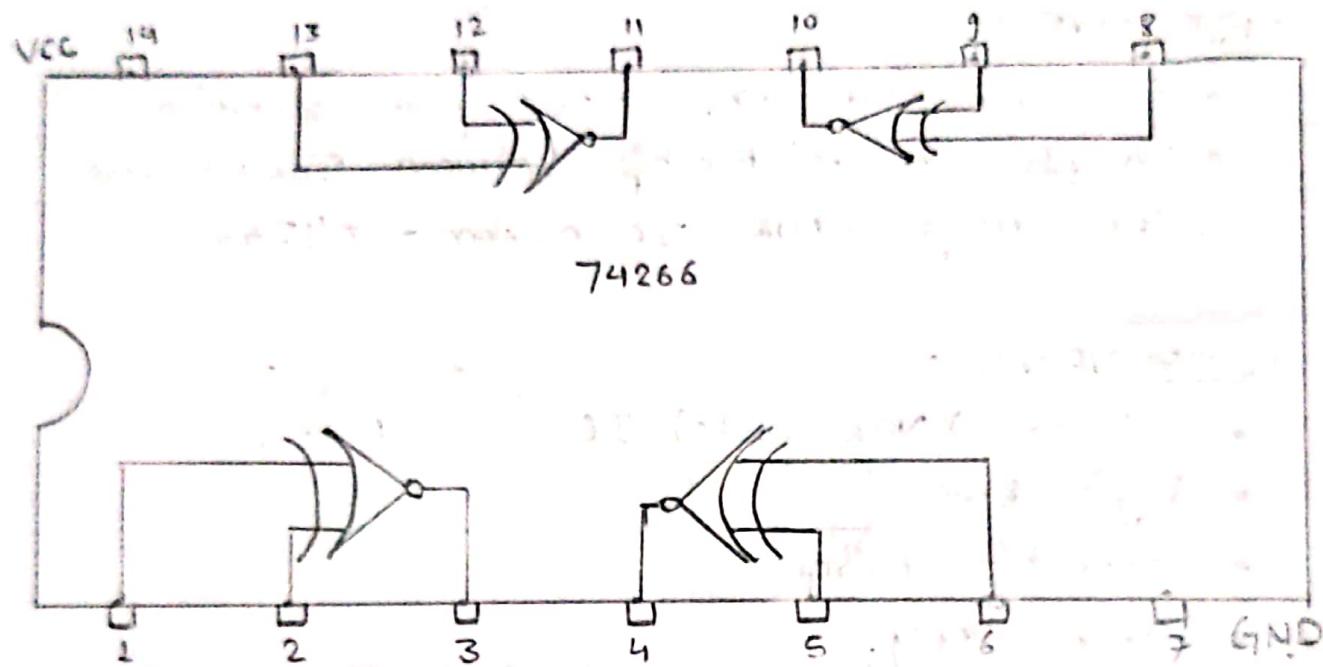


Fig: Pin Configuration

TITLE : Universal Gate

* NAND gate as Universal Gate

OBJECTIVE : To implement the basic gate using
NAND gate or IC 7400

COMPONENTS : - 7400 IC

- Digital Kit
- Connecting wire
- Power Supply

THEORY :

INTRODUCTION :- NAND gate is considered as universal
gate because we can construct any other gates from NAND.

FUNCTIONAL EXPRESSION :- The functional expression
of NAN gate is $\bar{A}\bar{B}$

TRUTH TABLE : To the opposite

CIRCUIT DIAGRAM : To the opposite

Sagarmatha

i) NOT Gate

A	\bar{A}
0	1
1	0

ii) OR Gate

A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1

iii) AND Gate

A	B	$A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

NAND gate as NOT gate

$$A \text{ } \square \text{ } \bar{A} \equiv A \text{ } \square \text{ } \bar{A}$$

NAND gate as AND gate

$$A \text{ } \square \text{ } \bar{AB} \text{ } \square \text{ } AB \equiv A \text{ } \square \text{ } AB$$

NAND gate as OR gate

$$A \text{ } \square \text{ } \bar{A} \text{ } \square \text{ } \bar{B} = A+B \equiv A \text{ } \square \text{ } G$$

PROCEDURE :

- Implement all the basic gate using 7400IC.
- Adjust the connecting wires and digital circuit properly.
- Apply the power supply.
- Verify the truth table for Input and output combination.

RESULT :

- The implementation of $\overline{A} \cdot B \cdot \overline{A} \cdot \overline{B}$ matched the truth table of AND gate
- The implementation of $\overline{A} \cdot \overline{A} \cdot \overline{B} \cdot \overline{B}$ matches the truth table of OR gate
- Implementation of $\overline{A} \cdot A$ matches the truth table of NOT gate
 \therefore All the basic gates being verified gates are verified.

TITLE : Universal gate

* NOR gate as universal gate

OBJECTIVE : Implement the basic gate using NOR gate or 7402 IC.

COMPONENTS :- 7402 IC

- Digital Kit
- Connecting wire
- Power supply

INTRODUCTION :

THEORY : NOR gate is consider as universal gate because we can design other gate from NOR.

FUNCTIONAL EXPRESSION : The functional expression for NOR gate is $\overline{A+B}$.

TRUTH TABLE : To the opposite

CIRCUIT DIAGRAM : To the opposite

Sagnikatha

1) NOT gate

A	\bar{A}
0	1
1	0

2) OR gate

A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1

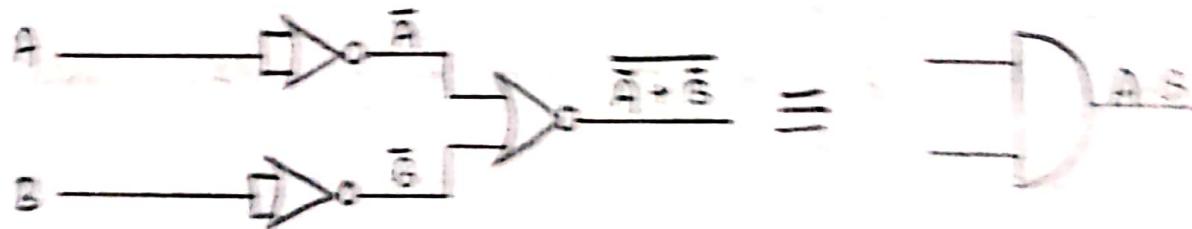
3) AND gate

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

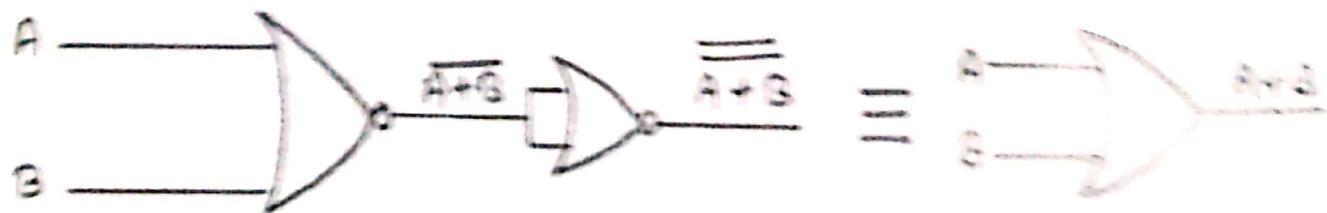
NOR gate as NOT gate



NOR gate as AND gate



NOR gate as OR gate



PROCEDURE :

- Implement the basic gate using NOR IC 7402
- Adjust the connecting wire and digital circuit properly.
- Apply the power supply
- Verify the truth table for input output combination

RESULT :- The implementation of $\overline{A+A} \cdot \overline{B+B}$ matched the truth table of AND gate.

- The implementation of $\overline{A+B} + \overline{A+B}$ matches the truth table of OR gate.
- Implementation of $\overline{A+A}$ matches the truth table of NOT Gate.

TITLE : Half Adder

OBJECTIVES :

- To implement and verify Half-Adder circuit
- To find the relation between inputs and outputs using the X-OR IC 7486 and AND IC 7408

COMPONENTS :

- 7486 (X-OR gate) IC and 7408 (AND gate) IC
- Digital Kit
- Connecting wires
- Power supply

THEORY :

- Half Adder is the simplest combination logic circuit which performs the arithmetic addition of 2 binary digits.
- It has 2 inputs and 2 outputs
- The 2 inputs are two 1 bit numbers A and B & the two outputs are sum (s) of A and B and the carry bit denoted by C

* Functional Expression :

$$\text{sum} = A \oplus B$$

$$\text{carry} = AB$$

Sagarmatha

* Logic symbol

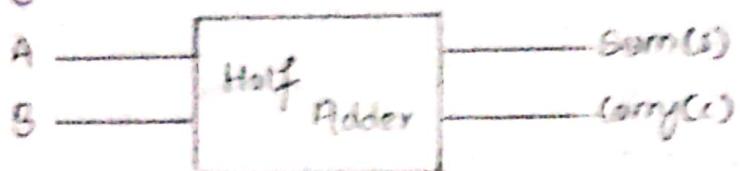


fig:- Block diagram

* Truth Table

Inputs		Outputs	
A	B	Sum(s)	Carry(c)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

* Circuit Diagram

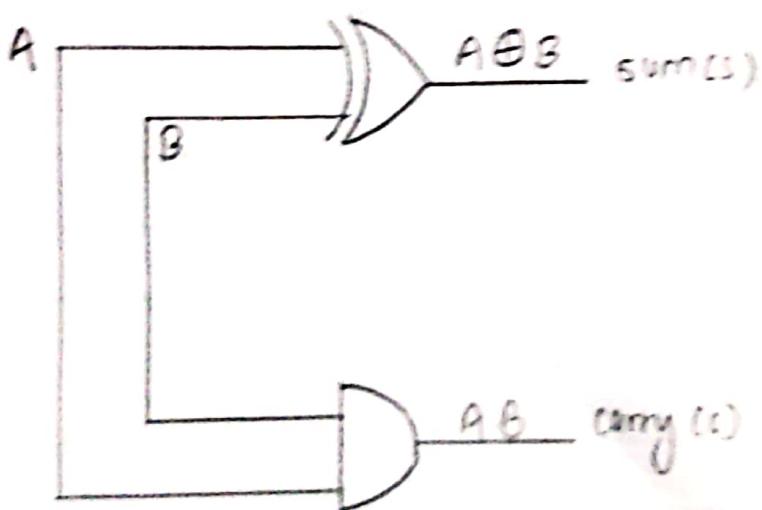


fig:- Implementation of Half Adder

5. PROCEDURE :

- Implement the circuit by using 7486 & 7408 IC.
- Adjust connecting wires properly on the digital kit
- Apply power supply
- Observe the relationship between Input/Output

6. RESULT :

When both the inputs are LOW, Output sum(s) and carry(c) both becomes LOW similarly when one of the input is HIGH and other LOW, output sum(s) becomes HIGH and carry(c) LOW and so on.

1. TITLE: Full Adder

2. OBJECTIVES:

- To implement and verify Full-Adder circuit
- To find the relationship between Inputs and Outputs using the X-OR IC 7486, AND IC 7408 and NOR IC 7432.

3. COMPONENTS:

- 7486 (XOR gate) IC 7408 (AND gate) IC & 7432 (OR gate) IC
- Digital kit
- Connecting wires
- Power supply

4. THEORY:

* Introduction:

- Full Adder is a combinational circuit that forms the sum of 3 input bits. It consists of 3 inputs & 2 outputs.

* Functional expression:

- Sum (s) = $A \oplus B \oplus C$
- Carry (c) = $C(A \oplus B) + AB$

5. PROCEDURES:

- Implement the circuit by using 7486, 7408 & 7432 IC.
- Adjust connecting wires properly on the digital kit.
- Apply power supply
- Observe the relationship between Input / Output.

* Logic symbol

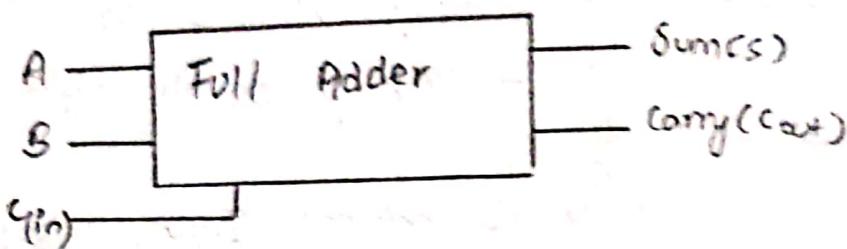


Fig:- Block Diagram

* Truth Table

Inputs			Outputs	
A	B	C	sum(s)	Carry(c)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

6. RESULT :

When all the inputs are LOW, both sum(s) and carry(c) becomes low. Similarly, when one of the input is HIGH, sum(s) becomes HIGH and carry(c) becomes low and so on.

* Circuit - Diagram

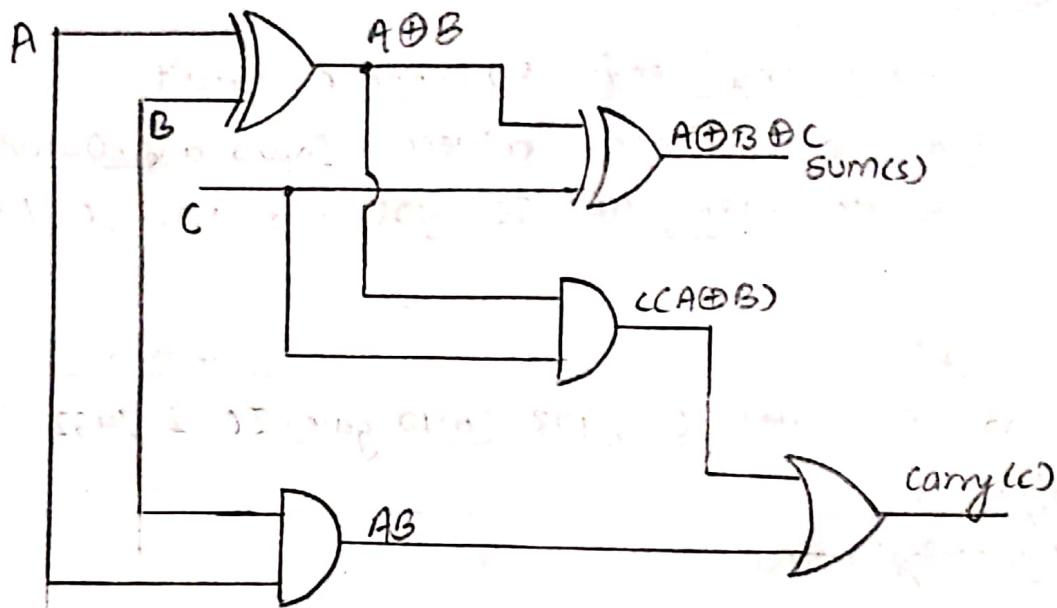


Fig :- Implementation of Full-Adder

1. TITLE : Half - Subtractor

2. OBJECTIVES :

- To implement and verify Half - Subtractor circuit
- To find the relationship between Inputs and Outputs using the X-OR IC 7486, NOT IC 7404 and AND IC 7408.

3. COMPONENTS :

- 7486 (X-OR gate) IC, NOT gate (7404) IC and 7408 (AND gate) IC
- Digital kit
- Connecting wires
- Power supply

4. THEORY :

* Introduction :

- Half subtractor is the combinational circuit used to get the difference between two single bit numbers A(minuend) and B(subtrahend)
- It has 2 outputs : Difference (D) and borrow (bout)

* Functional expression :

- Difference (D) = $A \oplus B$
- Borrow (B_{out}) = $\bar{A}B$

* Logic Symbol

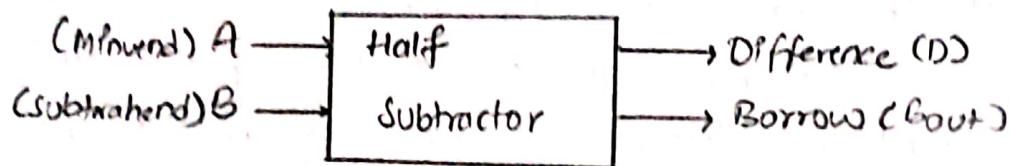


Fig:- Block Diagram

* Truth Table

Inputs		Outputs	
A	B	Difference (D)	Borrow (Bout)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

* Circuit Diagram

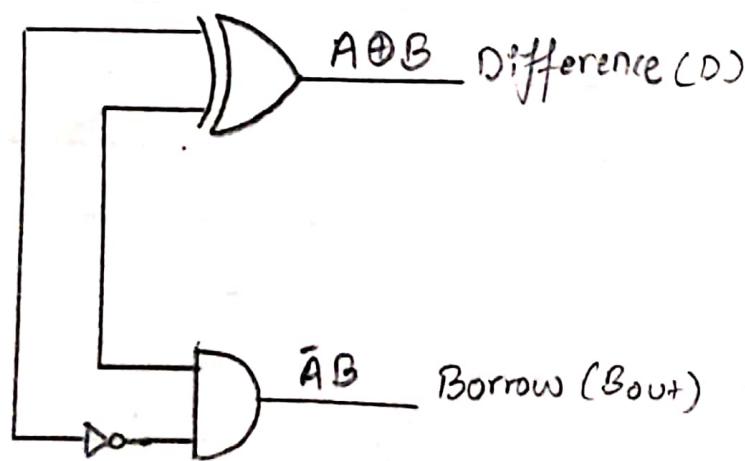


Fig:- Implementation of Half - Subtractor

5. PROCEDURE :

- Implement the circuit by using 7486, 7404 & 7408 IC.
- Adjust connecting wires properly on the digital kit.
- Apply power supply.
- Observe the relationship between Input/ output.

6. RESULT :

When both the inputs are LOW . Difference (D) and Borrow (Bout) are also LOW . similarly , when one of the input is HIGH , Difference (D) tends to be HIGH and Borrow (Bout) becomes LOW and so on.

1. TITLE : Full-Subtractor

2. OBJECTIVES :

- To implement and verify full-subtractor circuit
- To find the relationship between Inputs and Outputs using the XOR IC 7486, NOT IC 7404, AND IC 7408 and OR IC 7432.

3. COMPONENTS :

- 7486 (XOR gate) IC, 7404 (NOT gates) IC, 7408 (AND gate) IC and 7432 (OR gate) IC
- Digital kit
- Connecting wire
- Power supply

4. THEORY :

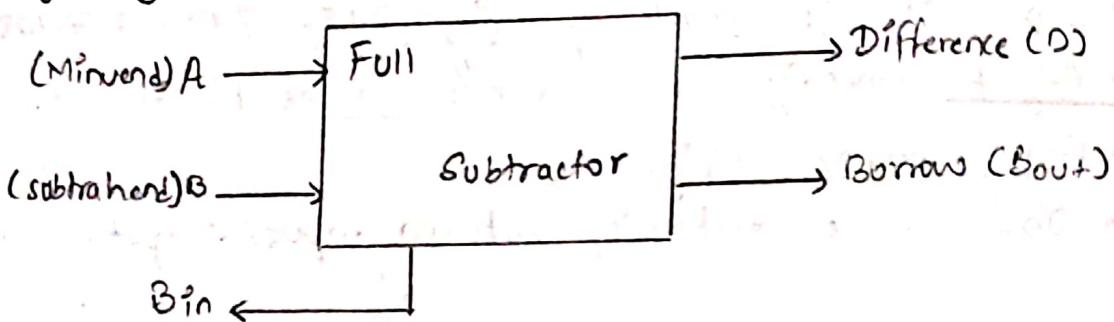
* INTRODUCTION :

- Full subtractor is a combinational logic circuit used to perform subtraction operation among 3 bits, minuend (A), subtrahend (B) & borrow taken from previous stage (B_{in})

* Functional Expression :

- Difference (D) = $A \oplus B \oplus B_{in}$
- Borrow (B_{out}) = $\bar{A}B + B B_{in} + \bar{A}B_{in}$

* Logic symbol



-fig: Block Diagram

* Truth Table

Inputs			Outputs	
A	B	B _{in}	Difference (D)	Borrow (B _{out})
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

5. PROCEDURES :

- Implement the circuit by using 7486, 7404, 74108 & 7432 IC.
- Adjust connecting wire properly on the digital kit.
- Apply power supply.
- Observe the relationship between Input /Output

6. RESULT :

When ~~tooth~~ all the inputs are low , Difference (D) & Borrow (Bout) are also low . Similarly , when one of the inputs is HIGH , Difference (D) tends to be HIGH and Borrow (Bout) becomes LOW moreover , when two of the inputs are HIGH , Difference (D) and Borrow (Bout) tends to be LOW and so on .

* Circuit Diagram

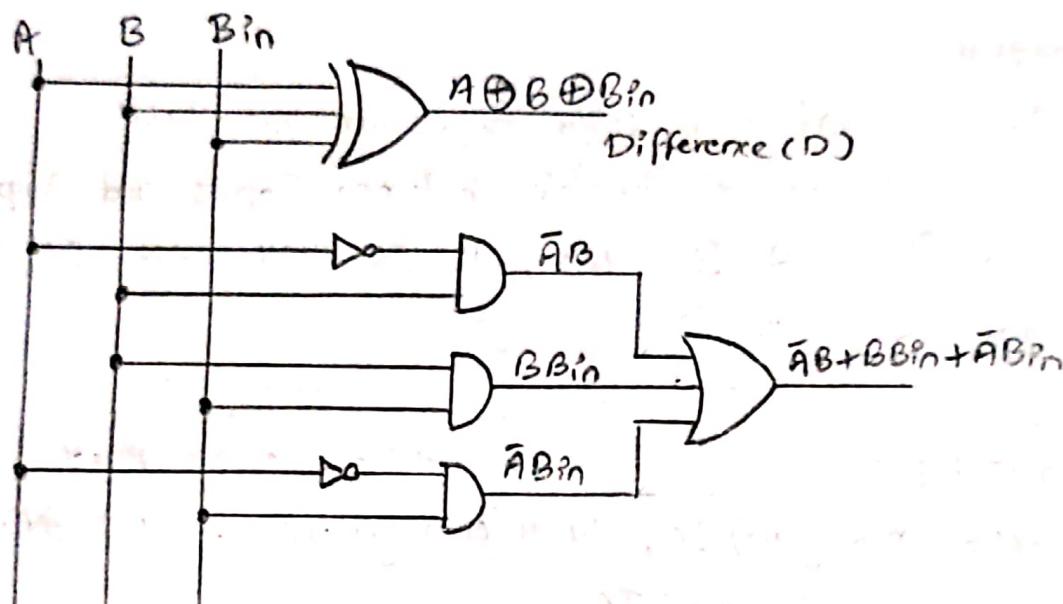


Fig:- Implementation of Full Subtractor

1. TITLE : X-OR gate using NAND gate

2. OBJECTIVE :

- To implement and verify X-OR gate using NAND
- To find the relationship between Input and Output using NAND.

3. APPARATUS :

- IC 7400 (NAND gate)
- Digital kit
- Connecting wires
- Power supply

4. THEORY :

* Introduction

- The X-OR gate using NAND gate is a logic operation which produce HIGH output when inputs are at opposite logic level otherwise result will be low.

combinational

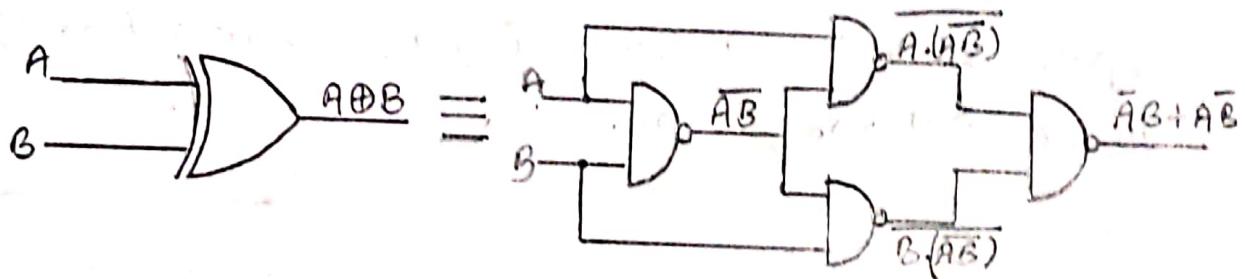
* Functional Expression

- $y = A \oplus B$

* Truth Table

Input		Output
A	B	$y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

* Circuit Diagram



= Fig :- Circuit Diagram of X-OR using NAND

5. PROCEDURE :

- Implement the circuit by using IC 7400
- Adjust connecting wires properly on digital kit.
- Apply power supply.
- Observe the relationship between Input and Output.

6. RESULT :

It gives HIGH output when Input are at opposite logic level. It gives LOW output when Input are at same logic level.

1. TITLE : X-NOR using NOR gate

2. OBJECTIVE :

- To implement and verify X-NOR using NOR gate
- To find relation between input and output using NOR IC 7402.

3. APPARATUS :

- IC 7402 (NOR)
- Digital kit
- Connecting wires
- Power supply

4. THEORY :

* Introduction

• X-NOR gate realizing NOR gate is logical operation. It produces HIGH output when two inputs are at same logic level. It produce LOW output when two inputs are at opposite logic level.

* Functional Expression

$$\bullet \quad y = A \oplus B$$

* Truth Table

Inputs		Outputs
A	B	$y = A \oplus B$
0	0	1
0	1	0
1	0	0
1	1	1

* Circuit Diagram

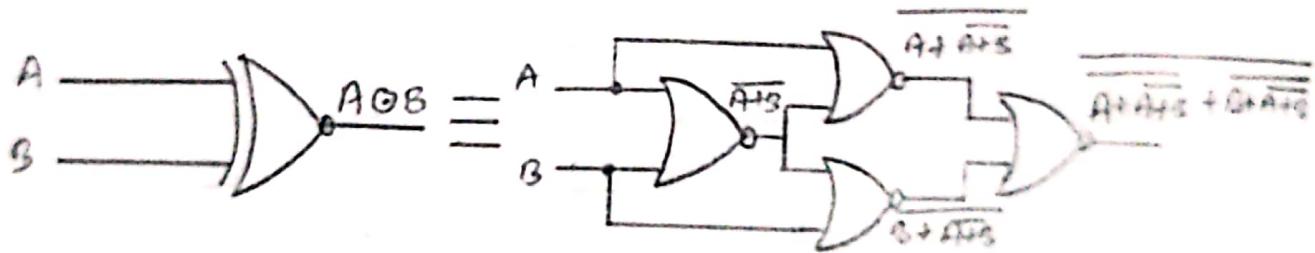


Fig :- Implementation of X-NOR using NOR

5. PROCEDURE :

- Implement the circuit by using NOR IC 7402
- Adjust connecting wires properly on digital kit
- Apply power supply.
- observe the relationship between Input and Output.

6. RESULT :

It gives HIGH output when inputs are at same logic level
and LOW output when inputs are in opposite logic level.

Sagarmatha

TITLE : X-NOR using NAND

OBJECTIVE :

- To implement and verify X-NOR using NAND gate.
- To find relation between input and output using NARID IC 7400.

APPARATUS :

- IC 7402
- Digital Kit
- Connecting wires
- Power supply

THEORY

* Introduction

- X-NOR gate is a logic gate which produce HIGH output when inputs are at same logic level and produce LOW output when inputs are at opposite logic level.

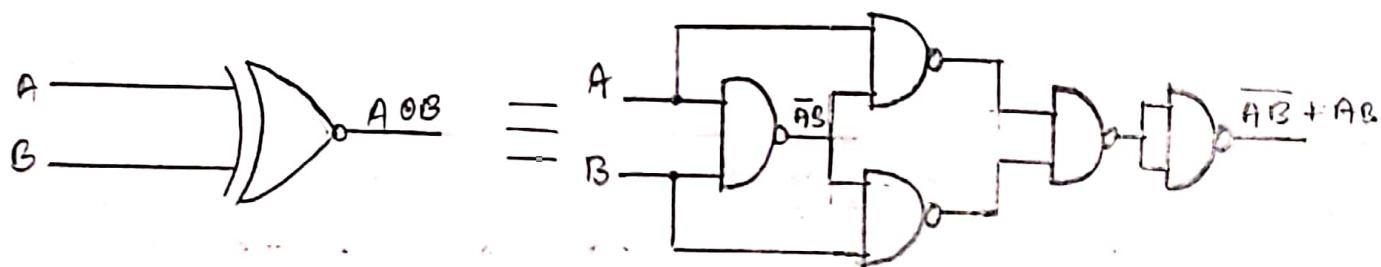
* Functional Expression

- $y = A \oplus B$

* Truth Table

Inputs		Outputs
A	B	$y = A \oplus B$
0	0	1
0	1	0
1	0	0
1	1	1

* Circuit diagram



= Fig:- Implementation of X-NOR using NAND

5. PROCEDURE :

- Implement the circuit by using NAND IC 7400
- Adjust connecting wires on the digital kit
- Apply power supply
- observe the relation between Input and Output.

6. RESULT :

It give HIGH output when inputs are at same logic level and it gives LOW output when inputs are at opposite logic level.

TITLE : X-OR using NOR

OBJECTIVES :

- To implement and verify X-OR using NOR gate.
- To find the relationship between Input and Output using NOR IC. 7402.

APPARATUS :

- IC 7402
- Digital Kit
- Connecting wires
- Power supply

THEORY :

* Introduction

- X-~~OR~~ gate realizing NOR gate is a logic circuit which produce HIGH output when input are at opposite logic level otherwise it will produce LOW output.

* Functional Expression.

- $y = A \oplus B$

* Truth Table

Input		Output
A	B	$y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

* Circuit Diagram

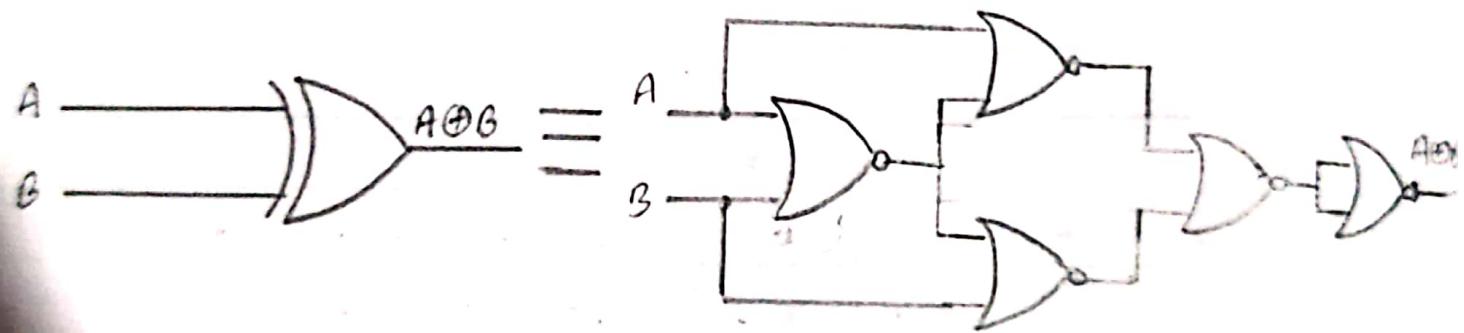


Fig:- Implementation of X-OR using NOR

5. PROCEDURE :

- Implement the circuit by using NOR IC 7402
- Adjust the connecting wires properly in digital kit
- Apply power supply.
- Observe the relationship between Input and Output.

6. RESULT:

It gives HIGH output when the inputs are at opposite logic levels and LOW output when the inputs are at same logic levels.

Sangamithra

1. TITLE: NAND gate using NOR gate

2. OBJECTIVE :

- To implement and verify NAND gate using NOR gate.
- To find the relationship between Input and output using NOR IC 7402.

3. COMPONENTS :

- IC 7402 (NOR gate)
- Digital kit
- Connecting wires
- Power supply

4. THEORY :

* Introduction

- The NAND gate is complement of AND gate. It produce HIGH output when any one input is LOW. It produce LOW output when both inputs are HIGH.

* Functional Expression

- $Y = \overline{A \cdot B}$

Sagarmatha

* Truth Table (CNAND)

Inputs		Output
A	B	$y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

* Circuit Diagram

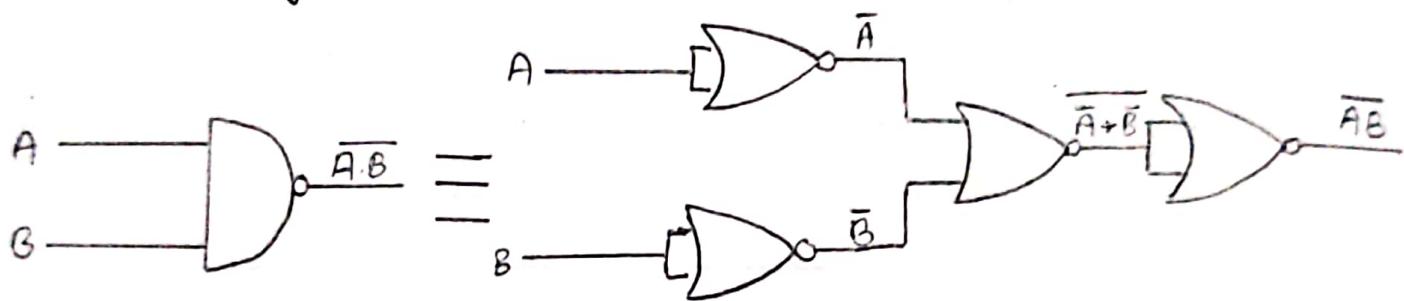


Fig:- Implementation of NAND using NOR gate

5. PROCEDURE :

- Implement the circuit by using NOR IC 7402.
- Adjust connecting wires properly in digital kit.
- Apply power supply.
- Observe the relationship between Input and Output.

6. RESULT :

It gives HIGH output when anyone input is low. It gives low output when all inputs are HIGH.

1. TITLE : NOR gate using NAND gate

2. OBJECTIVE :

- To implement and verify NOR gate using NAND gate
- To find the relationship between Input and Output using 7400 IC.

3. COMPONENTS :

- IC 7400 (NAND gate)
- Digital Kit
- Connecting wires
- Power supply

4. THEORY:

* Introduction

- NOR using NAND gate operation is complement of OR gate. It gives HIGH output when all inputs are LOW otherwise result will be LOW.

* Functional Expression

- $Y = \overline{A+B}$

* Truth Table

Inputs		Output
A	B	$y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

* Circuit Diagram

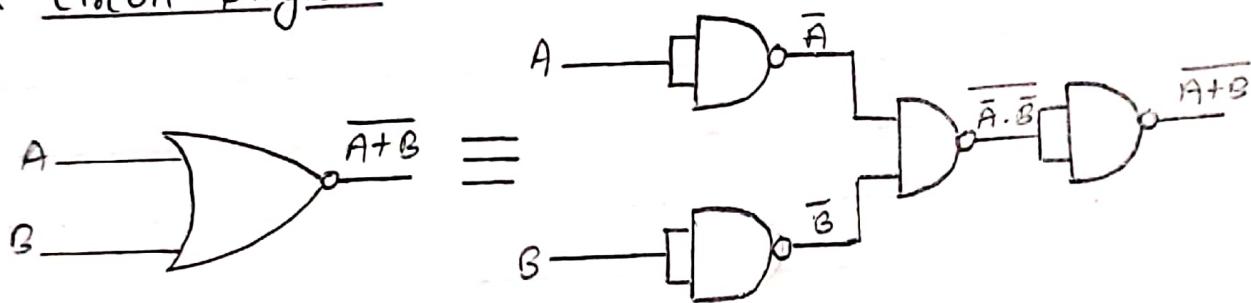


fig:- Implementation of NOR using NAND gate.

5. PROCEDURE :

- Implement the circuit using 7400 IC.
- Adjust connecting wires on the digital kit.
- Apply power supply.
- Observe the relationship between Input and output.

6. RESULT :

— It gives HIGH output when all the inputs are HIGH
otherwise result will be LOW.

TITLE : Decoder

OBJECTIVES:

- To implement and verify 3×8 line Decoder
- To find the relationship between inputs and outputs using 3×8 line Decoder.

Components :

- 7408 (AND gate) IC
- Digital kit
- Connecting wires
- Power supply

THEORY :

* Introduction :

- 3×8 line Decoder will have 3 inputs A, B, C and 8 output lines D0 - D7
- Depending on the value of the code received at input lines, one of 8 output lines is activated at a time.

* functional expression :

* Block Diagram

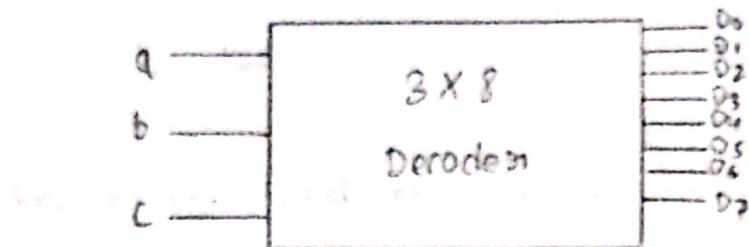


Fig:- Block diagram of 3x8 Decoder

* Truth Table

Inputs			Outputs							
a	b	c	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Following SOP expression:

$$D_0 = \bar{a}\bar{b}\bar{c} \quad D_4 = ab\bar{c}$$

$$D_1 = \bar{a}\bar{b}c \quad D_5 = a\bar{b}c$$

$$D_2 = \bar{a}b\bar{c} \quad D_6 = ab\bar{c}$$

$$D_3 = \bar{a}bc \quad D_7 = abc$$

PROCEDURES :

- Implement the circuit by using 7408 IC.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input / Output.

RESULT :

When all the inputs are Low, Do output tends to be HIGH and when inputs are 0, 0 & 1, D₁ output results HIGH and so on.

* Circuit Diagram

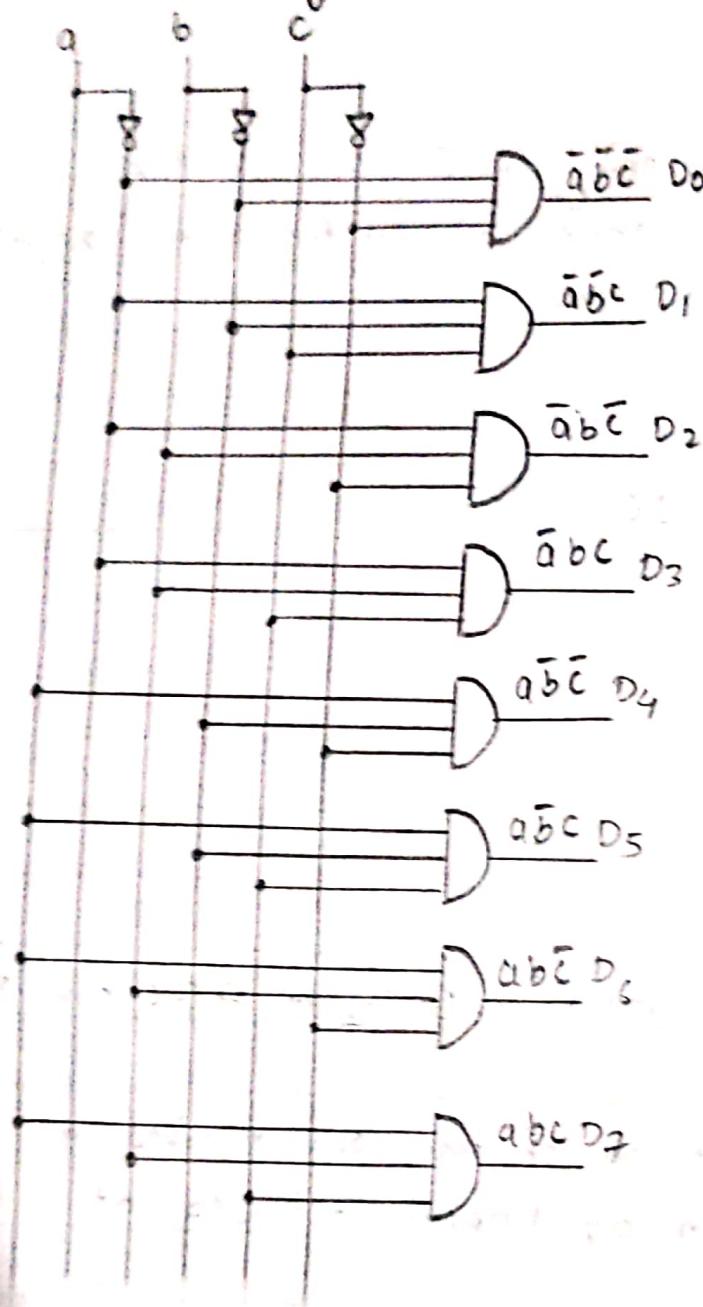


Fig: Circuit Diagram of 3x8 Decoder

TITLE : 8x3 Encoder

OBJECTIVES :

- To implement and verify 8x3 line Encoder
- To find the relationship between inputs and outputs using 8x3 line Encoder.

COMPONENTS :

- 7408 (AND gate) IC & 7432 (OR gates) IC
- Digital kit
- Connecting wires
- Power supply.

THEORY :

* Introduction

- 8x3 Encoder has 8 input lines and only one of the 8 input lines will be activated at a time and the corresponding binary code will be displayed at its output lines.
- 8x3 Encoder has 3 output lines.

* Block Diagram

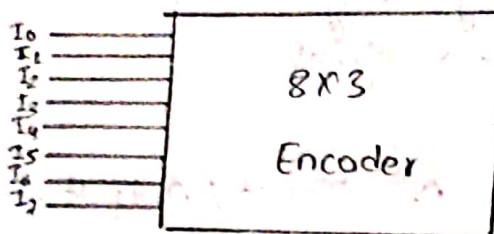


Fig:- Block Diagram of 8x3 Encoder

* Truth Table

Inputs								Outputs		
I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Following Expression

$$A = \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3 I_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 + \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 I_5 \bar{I}_6 \bar{I}_7 + \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 I_6 \bar{I}_7 \\ (I_4 + I_5 + I_6 + I_7)$$

$$B = I_2 + I_3 + I_6 + I_7$$

$$C = I_1 + I_3 + I_5 + I_7$$

PROCEDURE :

- Implement the circuit by using 7432 IC
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/output.

RESULT :

Encoder activates only one input line and corresponding binary code will be displayed at its output lines. When I_2 is activated, output will be generated as 0, 1, 0. Similarly, when I_6 is activated, output will be generated as 1, 1, 0 and so on.

* Circuit Diagram

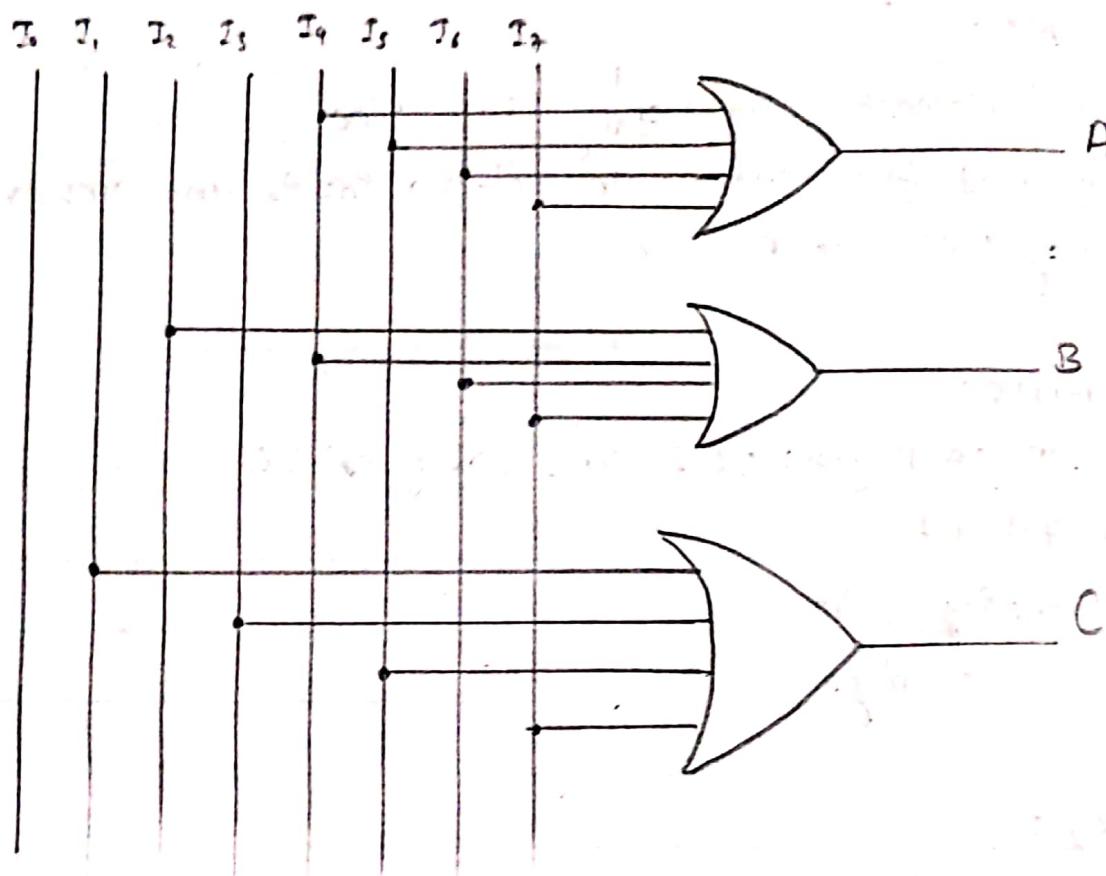


Fig:- Implementation of 8×3 Encoder

PROCEDURE :

- Implement the circuit by using 7432 IC
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/output.

RESULT :

Encoder activates only one input line and corresponding binary code will be displayed at its output lines. When I_2 is activated, output will be generated as 0, 1, 0. Similarly, when I_6 is activated, output will be generated as 1, 1, 0 and so on.

* Block Diagram

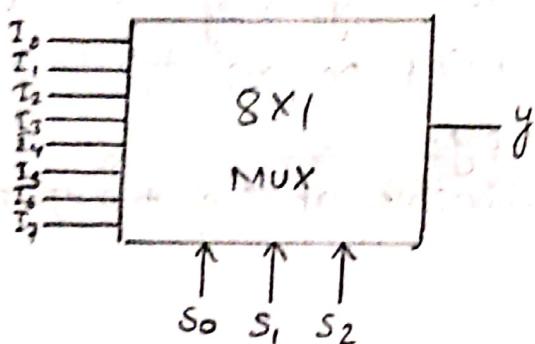


Fig:- Block Diagram of 8x1 MUX

* Functional Table

Inputs			Outputs
S_2	S_1	S_0	y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

TITLE : 8x1 MUX

OBJECTIVES :

- To implement and verify 8x1 line MUX
- To find the relationship between inputs and outputs using 8x1 MUX.

COMPONENTS :

- 7408 (AND gate) IC & 7432 (OR gate) IC
- Digital kit
- Connecting wires
- Power supply.

THEORY :

* Introduction

- 8x1 MUX have 8 input lines and 1 output line and 3 selection lines.
- Out of 8 output lines one is selected depending upon the value of selected lines.

* Circuit Diagram

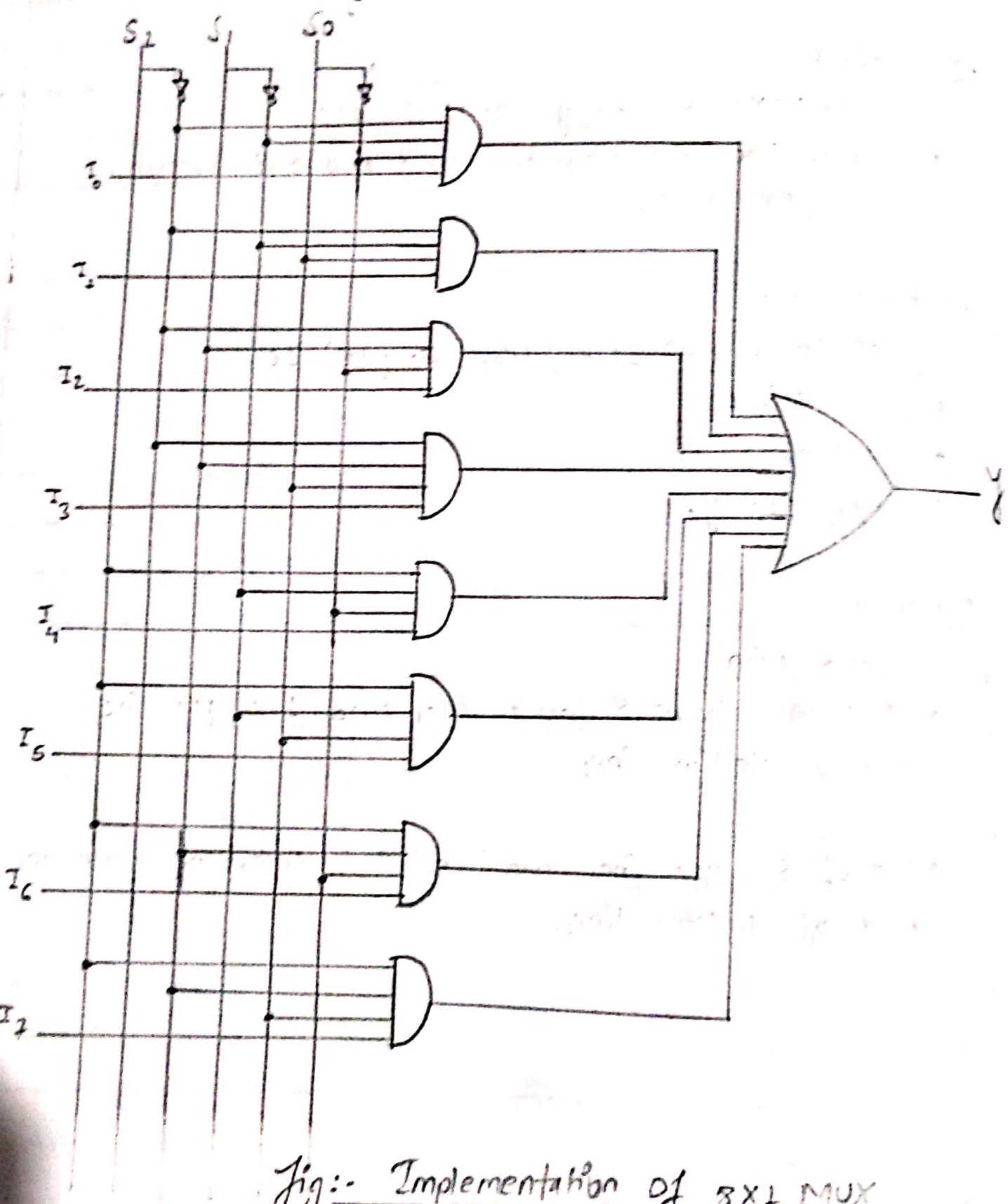


Fig:- Implementation of 8x1 MUX

PROCEDURES :

- Implement the circuit by using 74108 & 74132 IC
- Adjust connecting wires on digit kit properly.
- Apply power supply.
- Observe the relationship of Input/Output

RESULT :

When all three of the selection lines are low, output I_o is HIGH and when the selection lines are 0,0,1 output I_o tends to be HIGH and so on.

TITLE : 1x8 DEMUX

.....

OBJECTIVES :

- To implement and verify 1x8 LINE DEMUX
- To find the relationship between inputs & outputs using 1x8 DEMUX.

APPARATUS :

- 7408 (AND gate) IC
- Digital Kit
- Connecting wires
- Power supply

THEORY :

* Introduction

- 1x8 DEMUX will have 1 input (D) on its input line and 8 output lines ($y_0 - y_7$)
- It has 3 selection lines s_2, s_1 , and s_0 .

* Block Diagram

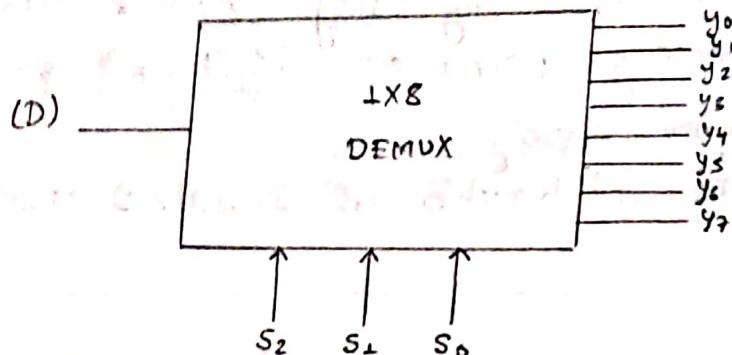


fig:- Block diagram of 1x8 DEMUX

* Truth Table

Data Input (I)	Selection Lines			Outputs							
	\$S_2\$	\$S_1\$	\$S_0\$	\$y_7\$	\$y_6\$	\$y_5\$	\$y_4\$	\$y_3\$	\$y_2\$	\$y_1\$	\$y_0\$
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	0	0	0	0
D	1	0	0	0	0	D	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

PROCEDURE:

- Implement the circuit by using 7408 IC
- Adjust connecting wires on digital Kit
- Apply power supply.
- Observe the relationship of Input/ Output.

RESULT:

When all three selection lines are LOW, y_0 is HIGH.

Similarly when the selection lines are 0,0 and 1, y_1 tends to be HIGH and so on.

* Circuit Diagram

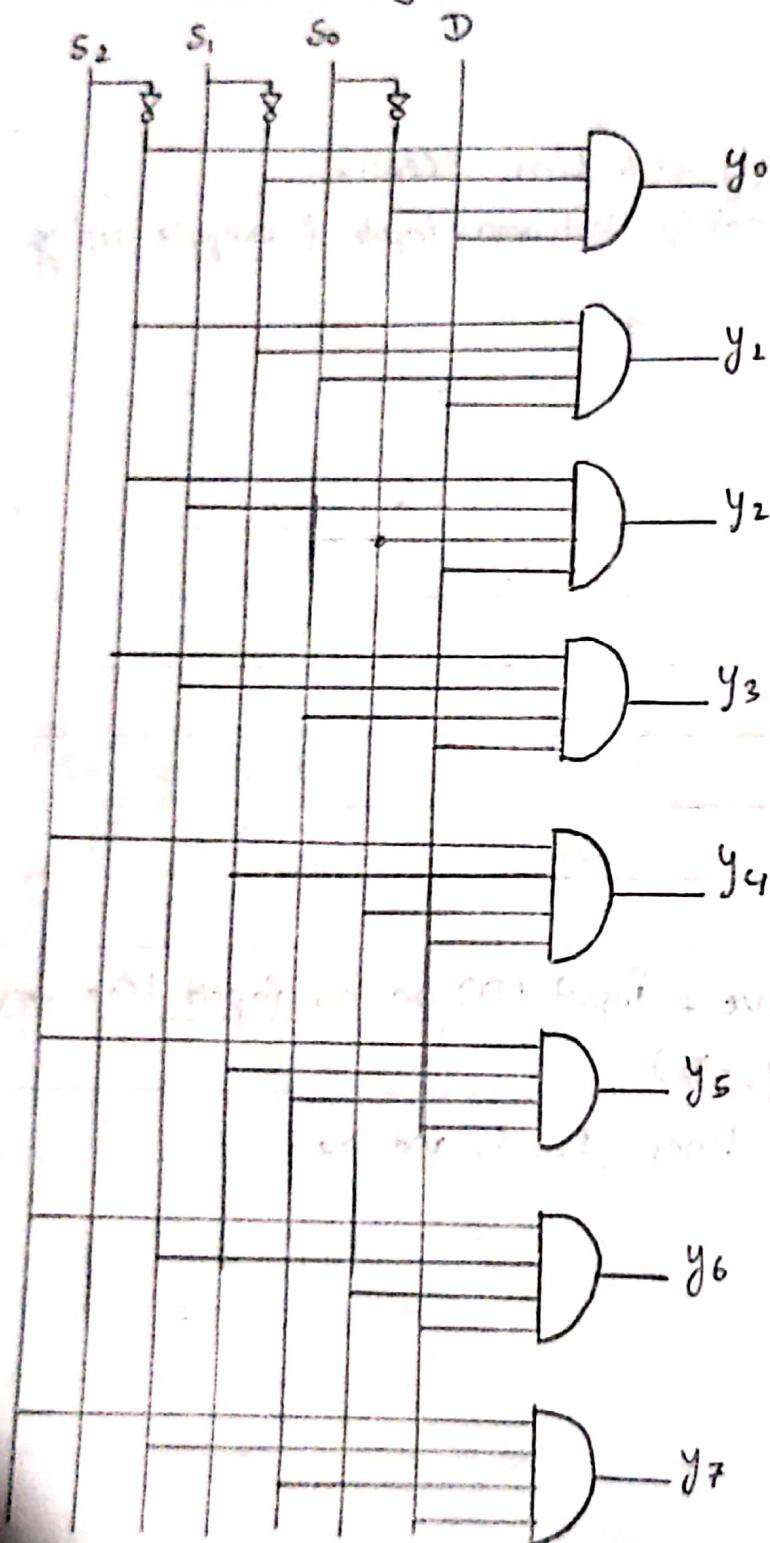


Fig:- Implementation of 1x8 DEMUX