

Title : Serial In Serial OutObjectives :

- To implement and verify SISO register.
- To find the relationship between inputs and outputs using D flip-flop.

Components :

- D flip-flop, AND (7408) IC, OR (7432) IC
- Digital kit
- Connecting wires
- Power supply.

Theory :* Introduction

In SISO register, data are accepted serially that is one bit at a time on a single input line. It produces the standard stored information on its single output only in serial form.

* Circuit Diagram

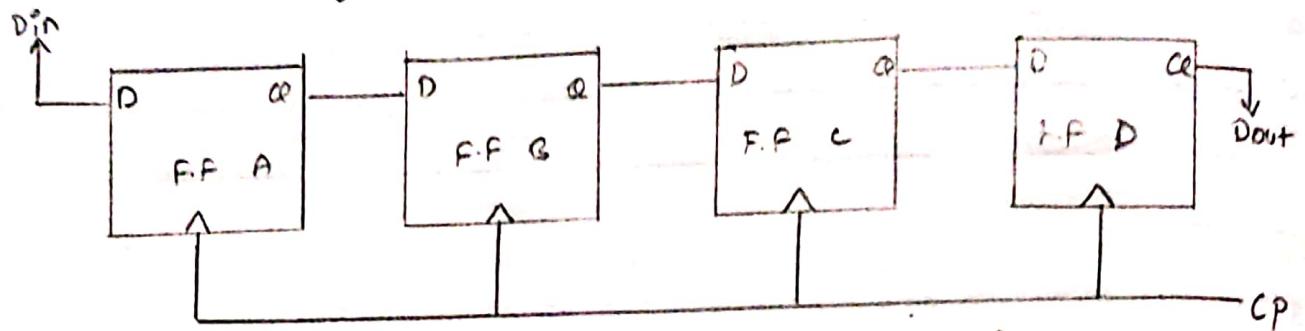


Fig:- Circuit diagram of SISO

* Operation Table : Data = 1101

CLOCK pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	$0 \rightarrow$
1 (\uparrow)	1	0	0	$0 \rightarrow$
2 (\uparrow)	0	1	0	$0 \rightarrow$
3 (\uparrow)	1	0	1	$0 \rightarrow$
4 (\uparrow)	1	1	0	$1 \rightarrow$

PROCEDURE :

- Implement the circuit by using D flip-flop.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

RESULT :

→ The 8150 shift register accepts data serially i.e., one bit at a time on a single line and produces the stored information on its output also in serial form.

* Timing Diagram/wave form

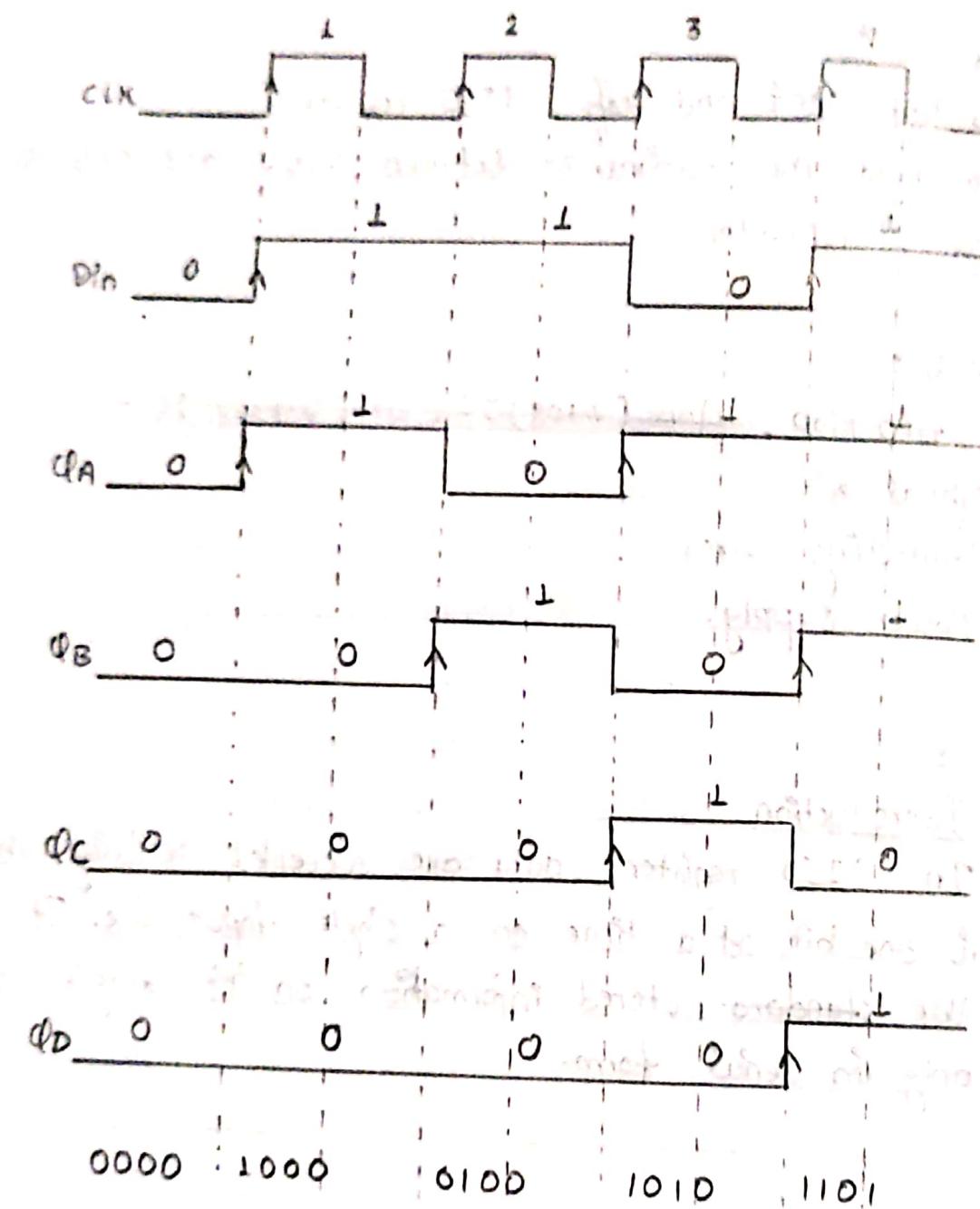


fig:- waveform of SISO register

TITLE : Serial To Parallel Out Register

OBJECTIVES :

- To implement and verify SIPO register
- To find the relationship between inputs & outputs using D flip-flop.

COMPONENTS :

- D flip-flop
- Digital kit
- Connecting wires
- Power supply

THEORY :

* Introduction

→ In SIPO register, data is stored in the register serially while it is received from parallelly.

→ It consists of one serial input and outputs are taken from all flip-flops in parallel.

* Circuit Diagram

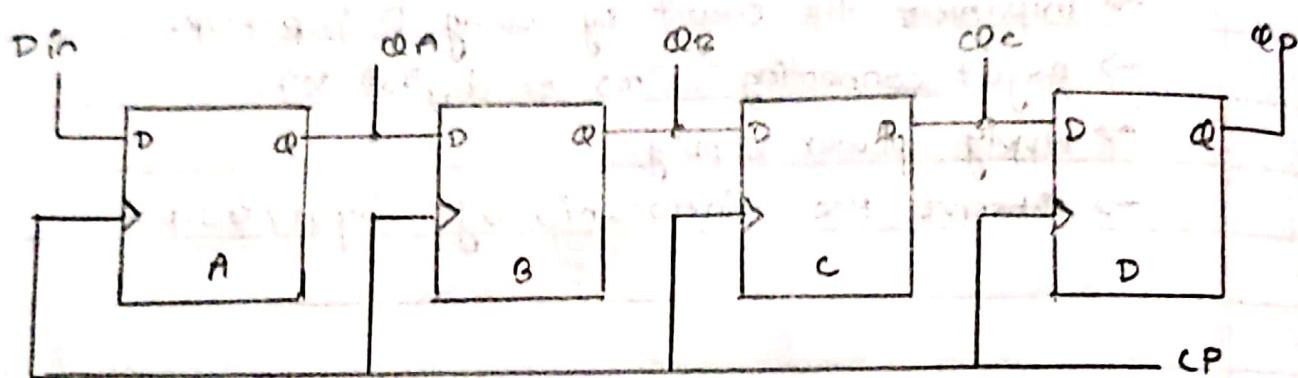


fig:- Circuit diagram for SIPD

* Operational Table

Clock Pulse	Data Input	QA	QB	QC	QD
0	-	0	0	0	0
1(↑)	1	1	0	0	0
2(↑)	1	1	1	0	0
3(↑)	0	0	1	1	0
4(↑)	1	1	0	1	1

PROCEDURES :

- Implement the circuit by usng D flip-flop.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

RESULT:

For Data = +101 in shift right register,
at first clock pulse bit-1 is shifted to F.F-A
then $Q_A = 1$ & $B = Q_C = Q_D = 0$ on second
clock pulse bit-1 is shifted to F.F-A and bit
or result produced by F.F.A is shifted to F.F.B
then $Q_A = 1$, $Q_B = 1$, $Q_C = Q_D = 0$. Output is
produced and so on.

* Timing Diagram

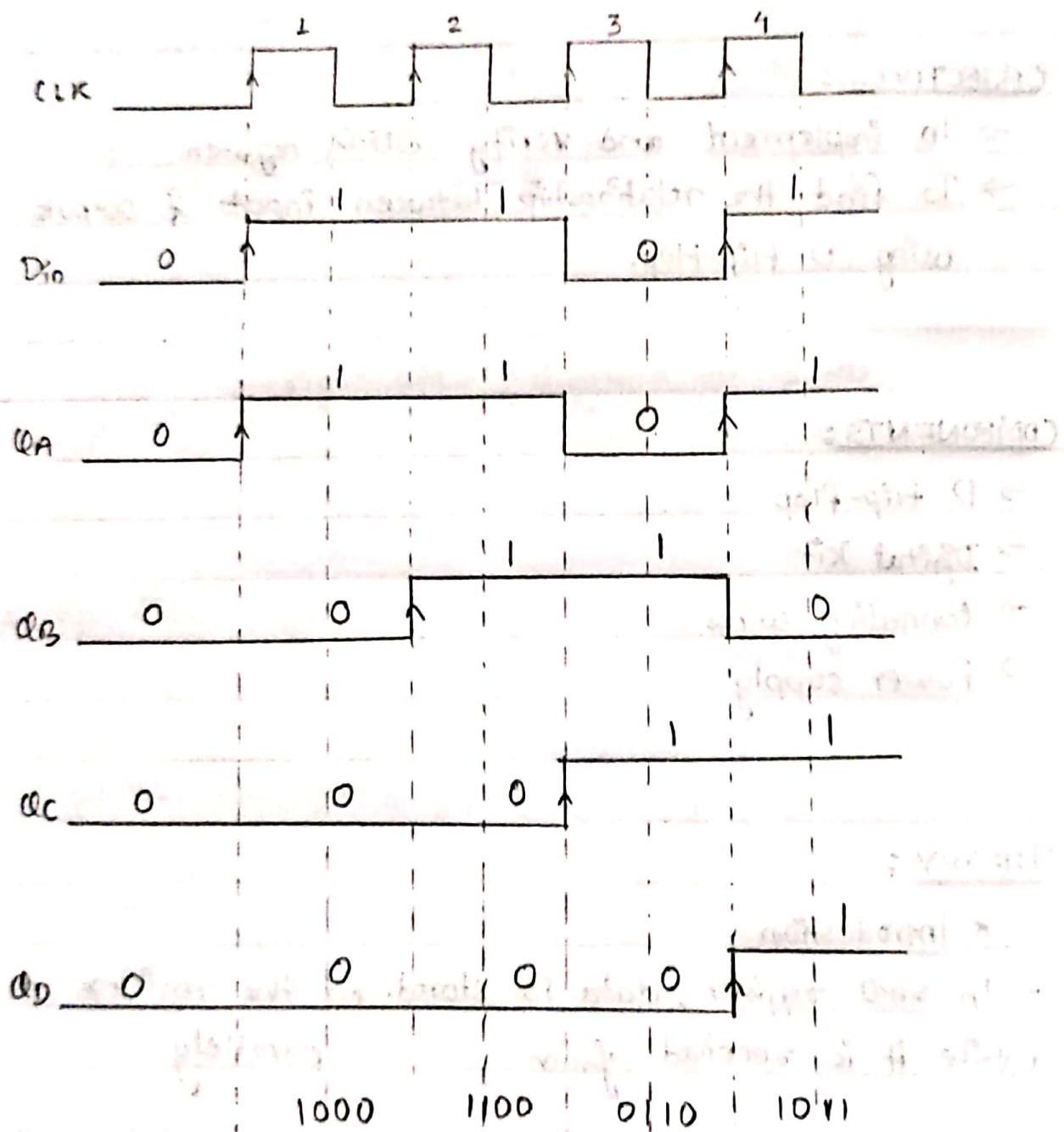


fig:- Waveform of SISO Register

TITLE : Parallel In Serial Out shift Register

OBJECTIVES :

- To implement and verify PISO register.
- To find the relationship between inputs & outputs using D flip-flop.

COMPONENTS :

- D flip-flop, AND (7408) IC, ORC 7432) IC gates.
- Digital kit
- Connecting wires
- Power supply

THEORY :

* Introduction

- In PISO shift register, the data is loaded into register in parallel form while it is received from it serially.

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* Circuit Diagram

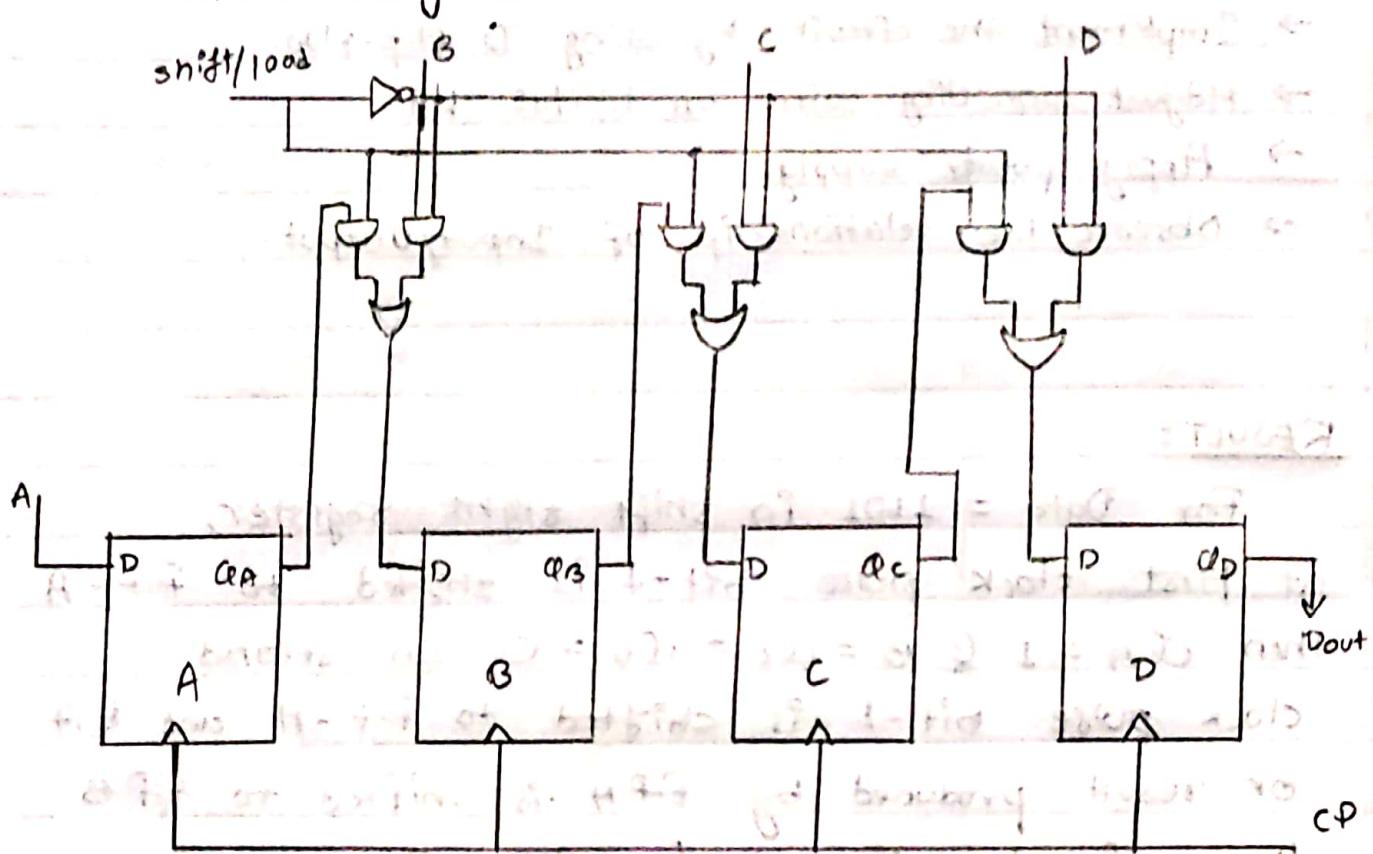


Fig:- Circuit Diagram of PISO register

* Operation table

CLK	shift/load	Data Inputs				Q _A	Q _B	Q _C	Q _D	serial O/p
		A	B	C	D					
0	-	-	-	-	-	0	0	0	0	-
1(↑)	0	1	1	1	0	1	1	1	0	0
2(↑)	1	1	1	1	0	1	1	1	1	1
3(↑)	1	1	1	1	0	1	1	1	1	1
4(↑)	1	1	1	1	0	1	1	1	1	1

PROCEDURE:

- Implement the circuit by using D flip-flop, AND and OR gate.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

RESULT.

* Timing Diagram

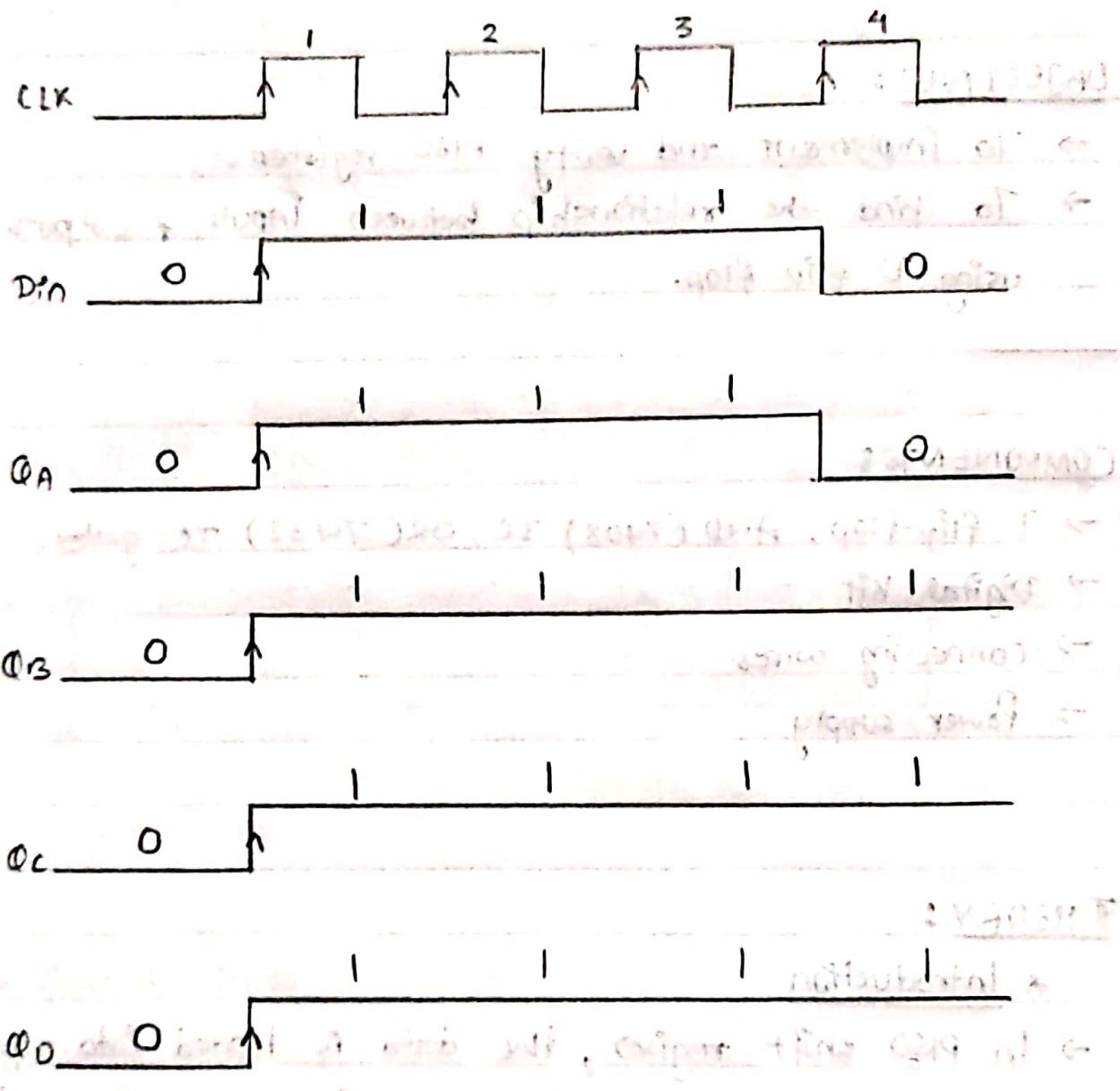


Fig:- Waveform of PISO register

TITLE : Parallel In Parallel Out Register.

OBJECTIVES :

- To implement and verify PIPD register.
- To find the relationship between inputs and outputs using D flip-flop.

COMPONENTS :

- D flip-flop
- Digital kit
- Connecting wires
- Power supply.

THEORY

* Introduction

→ PIPD register is a type of storage device in which both the data loading as well as data retrieval process occurs ⁱⁿ parallel mode.
i.e., Data inputs can be shifted either in or out of the register in parallel.

* Circuit Diagram

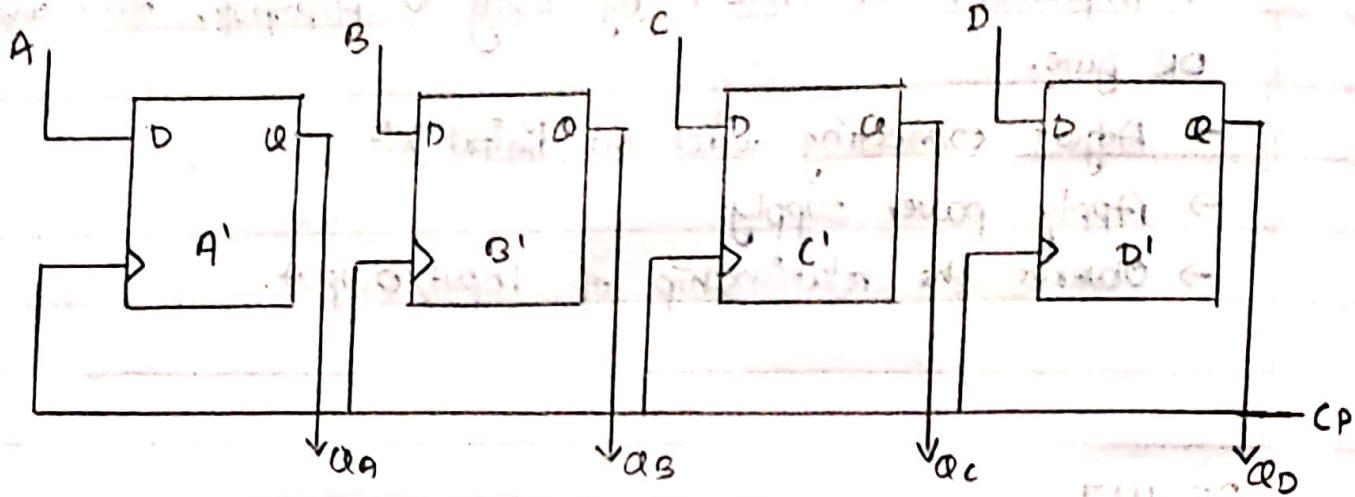


Fig:- parallel in parallel out register

* Operation Table

CLK	Parallel Inputs				Outputs			
	A	B	C	D	QA	QB	QC	QD
0	-	-	-	-	0	0	0	0
1	L	L	0	1	L	L	0	1

PROCEDURE :

- Implement the circuit using D flip-flop.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

RESULT :

- When the 1st clock is high, all the flip-flops give output parallel at the same time in respect to the delta input.

* Timing Diagram of 4 bit PIPo register

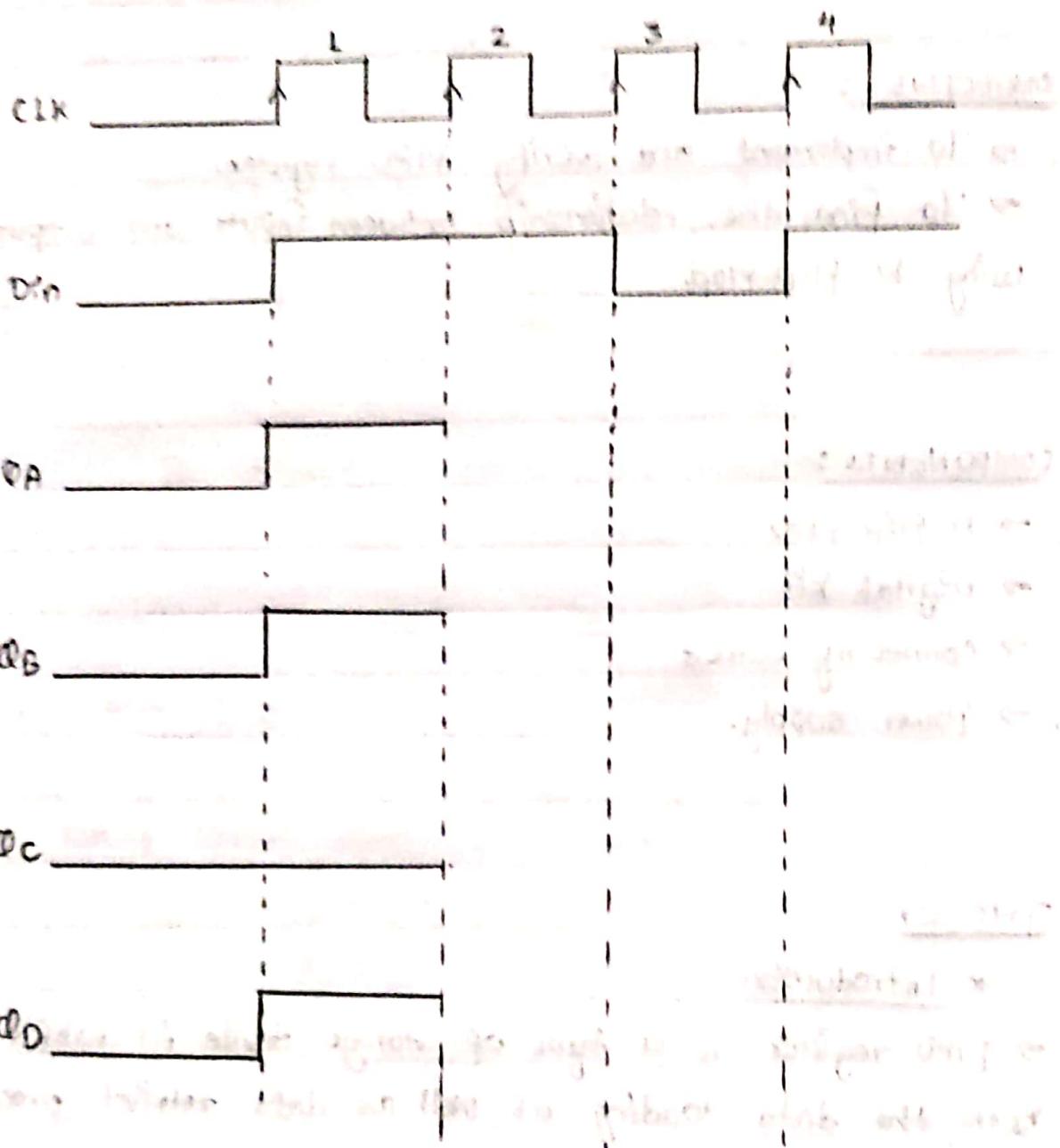


Fig:- Timing Diagram of PIPo register

TITLE : 3 bit Asynchronous (Ripple) up counter

OBJECTIVES :

- To implement and verify 3 bit Ripple up counter.
- To find the relationship between inputs and outputs using T flip-flop.

COMPONENTS :

- T flip-flop
- Digital Kit
- Connecting wires
- Power supply.

THEORY :

* Introduction:

- 3 bit Ripple up counter is capable of counting 8 states.
- In Asynchronous counter, flip-flop are not closed simultaneously.
- They have fixed count sequence, either up or down.

* State Diagram:

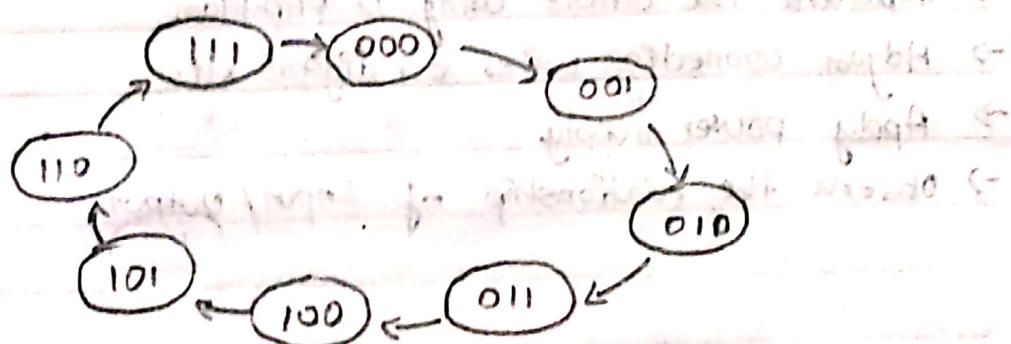


fig:- State Diagram

* Circuit Diagram:

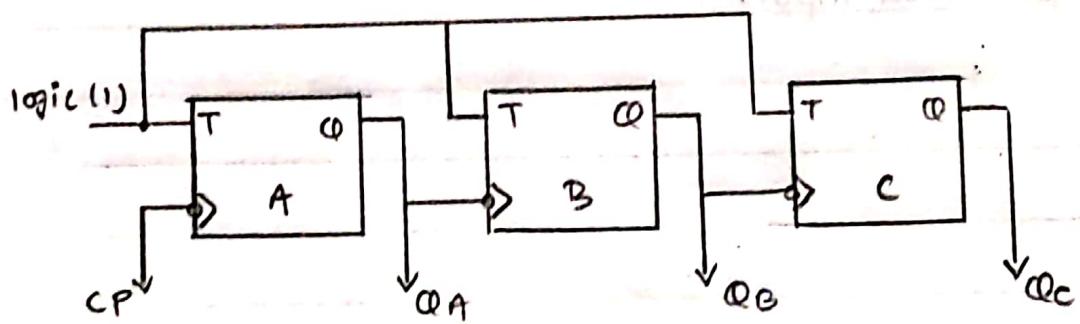


fig:- Circuit Diagram

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PROCEDURE:

- Implement the circuit by using T flip-flop
- Adjust connecting wires on digital kit.
- Apply power supply.

RESULT:

Here, Q_A is always complemented. Q_B is complemented when there is transition from HIGH to LOW on Q_A and so on.

* Truth table: (original working for 3-bit)

CLK	Counter output	State	Decimal no.
	Q _C Q _B Q _A		
Initially	0 0 0	0	0
1 st	0 0 1	1	1
2 nd	0 1 0	2	2
3 rd	0 1 1	3	3
4 th	1 0 0	4	4
5 th	1 0 1	5	5
6 th	1 1 0	6	6
7 th	1 1 1	7	7
8 th	0 0 0	8	8

* Timing Diagram:

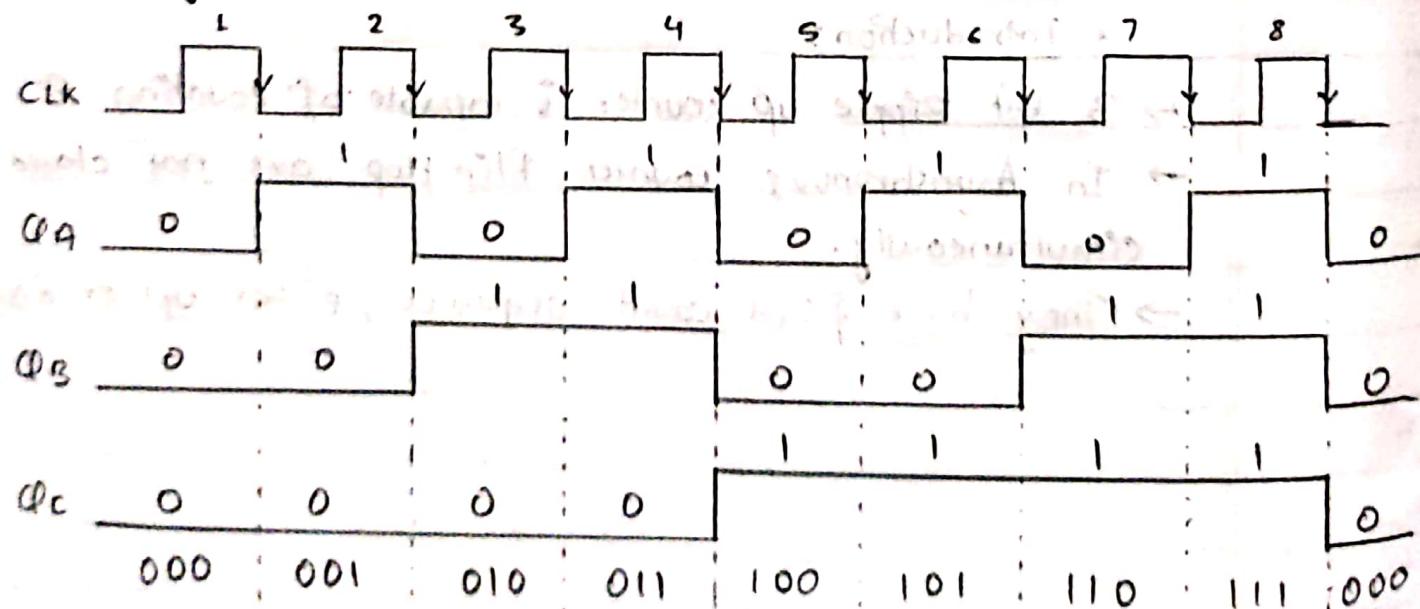


Fig:- Timing Diagram of 3-bit ripple up counter.

TITLE : 3 bit Asynchronous (Ripple) Down counter.

OBJECTIVES:

- To implement and verify 3 bit Ripple Down counter.
- To find the relationship between inputs and outputs using T flip-flop.

COMPONENTS:

- T flip-flop
- Digital kit
- Connecting wires
- Power supply

THEORY:

- * Introduction
- 3 bit ripple Down counter is capable of counting downwards from a maximum of 7 to 0.
- They are not clocked simultaneously.

* State Diagram:

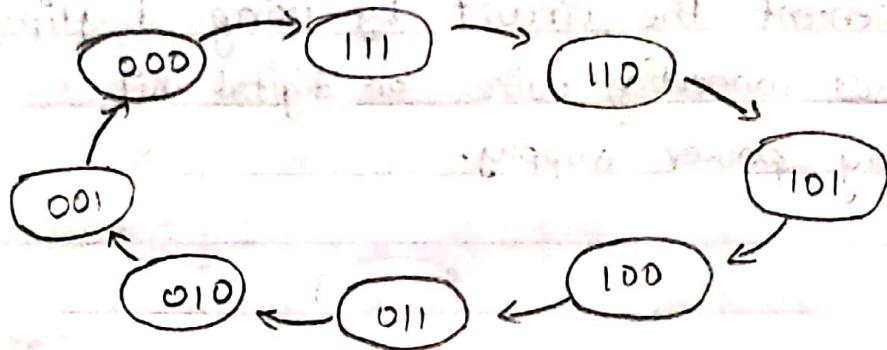


fig:- State Diagram

* Circuit Diagram:

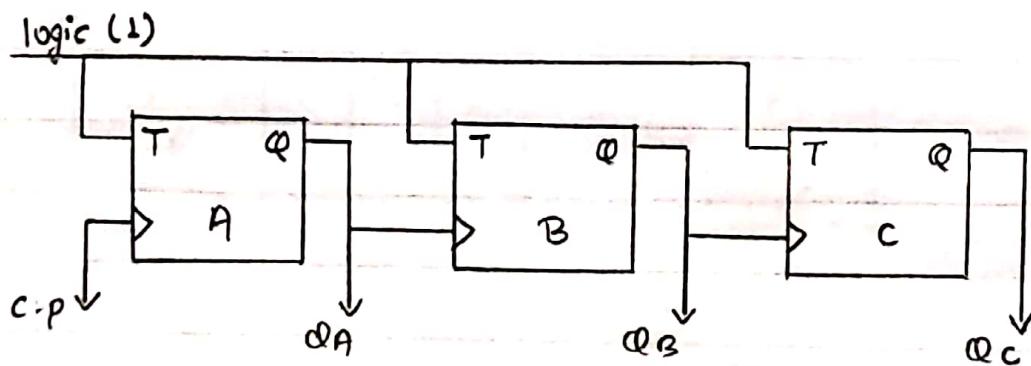


fig:- Circuit Diagram

* Truth Table:

CLK	Counter output			State	Decimal no
	QC	QB	QA		
Initially	0	0	0	1	0
1 st	1	1	1	2	7
2 nd	1	1	0	3	6
3 rd	1	0	1	4	5
4 th	1	0	0	5	4
5 th	0	1	1	6	3
6 th	0	1	0	7	2
7 th	0	0	1	8	1
8 th	0	0	0	9	0

PROCEDURES :

- Implement the circuit by using T flip-flop.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

RESULT :

Here, Q_A is always complemented. Q_B is complemented when there is transition from LOW (0) to HIGH (1) on Clk , and so on.

* Timing Diagram:

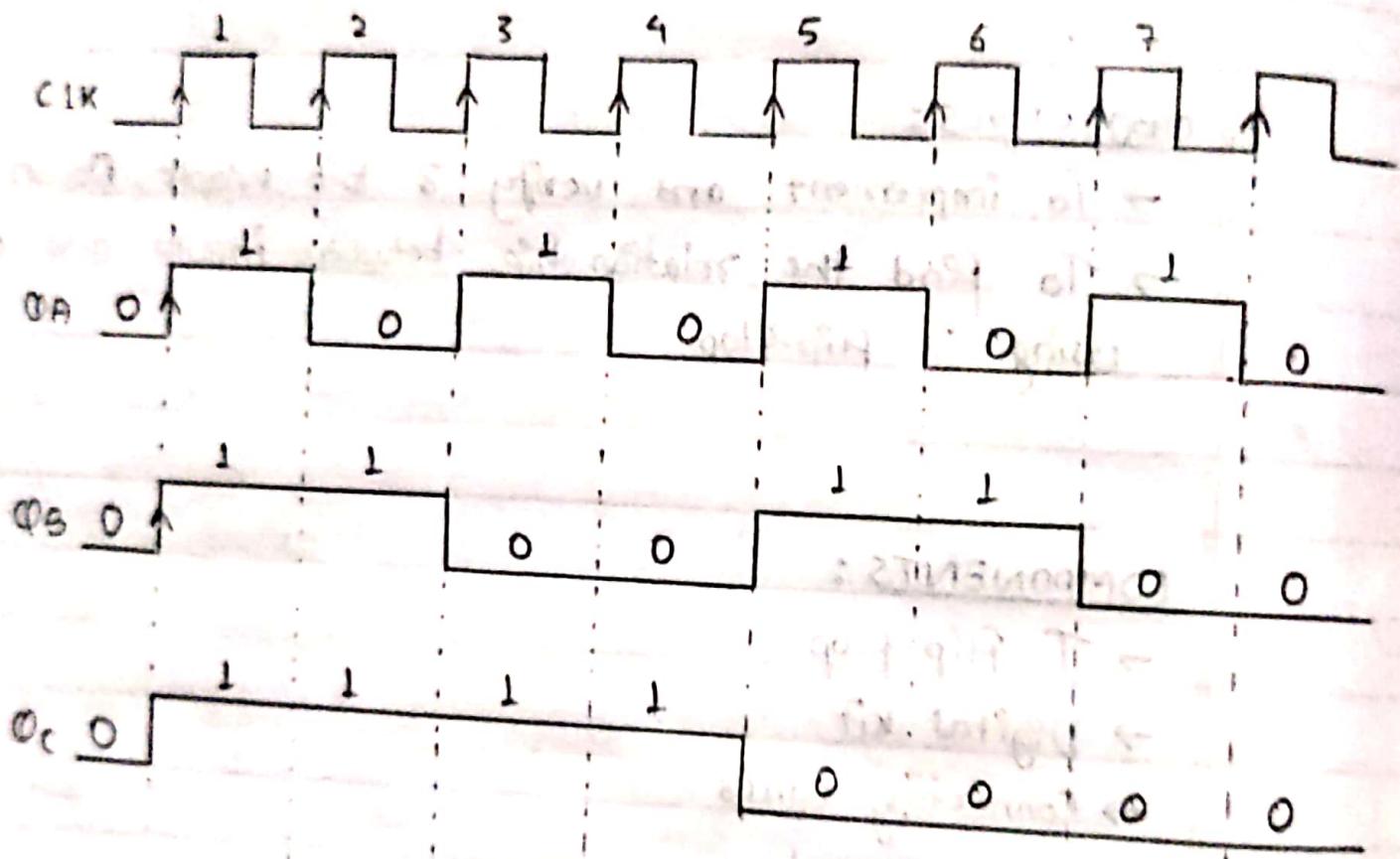


Fig:- Timing Diagram of 3-bit ripple down counter

TITLE : 3 bit synchronous (binary) up counter.

OBJECTIVES :

- To implement and verify 3 bit binary up counter.
- To find the relationship between inputs and outputs using JK flip-flop.

COMPONENTS :

- JK flipflop
- Digital kit
- Connecting wires
- Power supply

THEORY

* Introduction

- 3 bit binary up counter is capable of counting 8 states.
- Clock pulses are applied to the inputs of all flipflops.
- The common pulse triggers all flip-flop simultaneously rather than 1 at a time in succession.

* State Diagram :

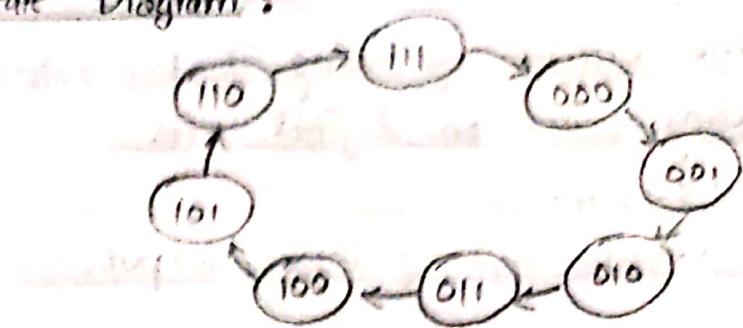


Fig:- state diagram

* Circuit Diagram :-

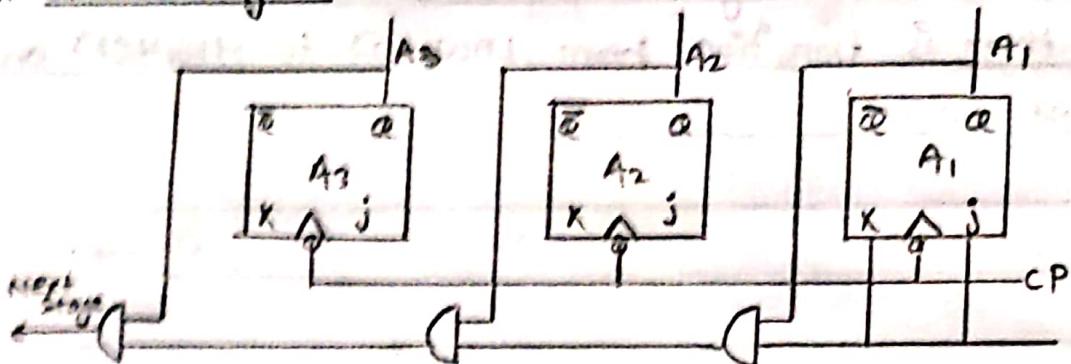


Fig:- circuit diagram

* Truth Table :

CLK	counter outputs			state	decimal
	A ₃	A ₂	A ₁		
Initially	0	0	0	1	0
1 st	0	0	1	2	1
2 nd	0	1	0	3	2
3 rd	0	1	1	4	3
4 th	1	0	0	5	4
5 th	1	0	1	6	5
6 th	1	1	0	7	6
7 th	1	1	1	8	7
8 th	0	0	0	9	8

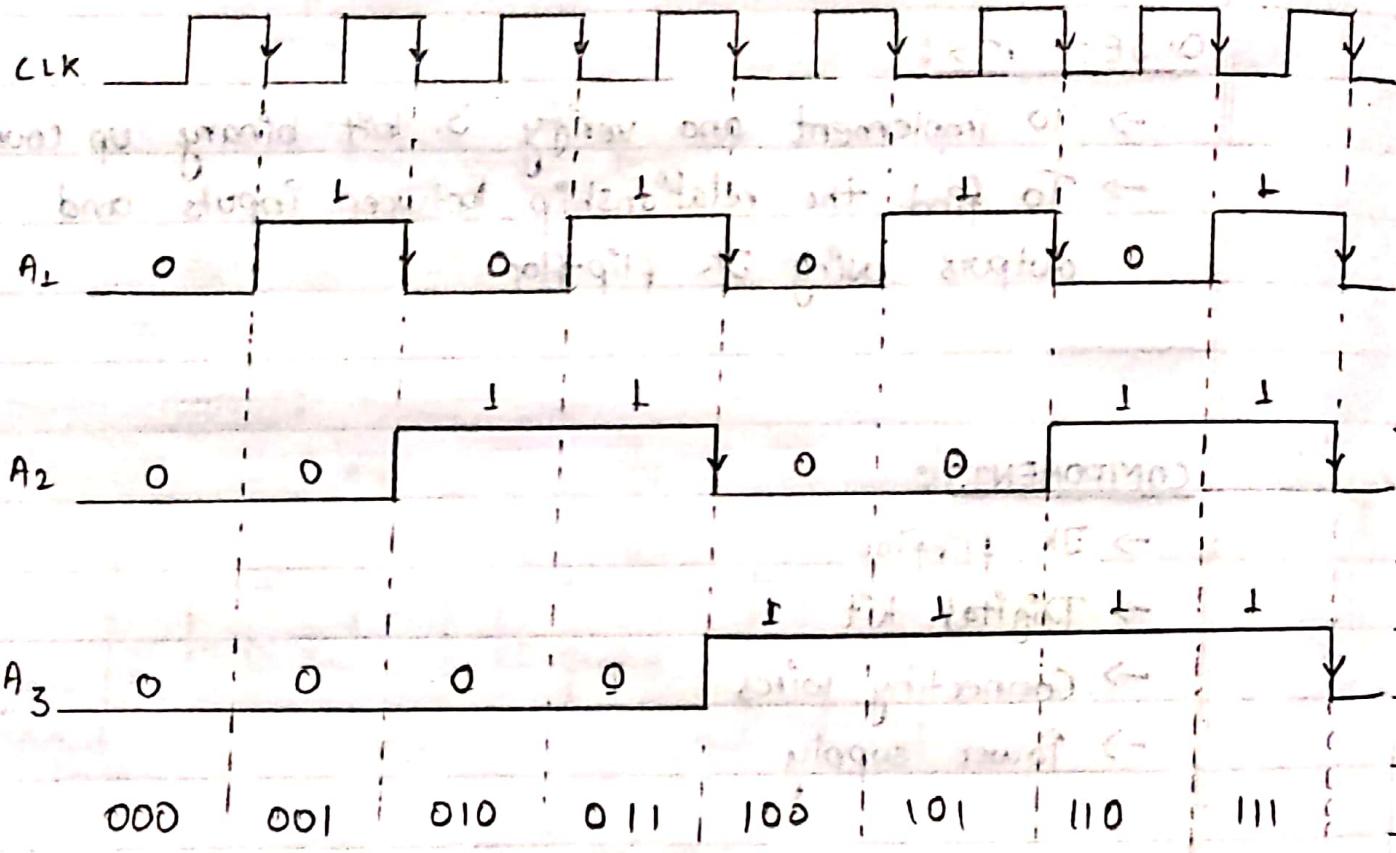
PROCEDURES :

- Implement the circuit by using JK flip-flop.
- Adjust all connecting wires.
- Apply power supply
- Observe the relationship of Input and output.

RESULT :

Here, A_1 is always complemented. A_1 is complemented when A_2 is equal to 1. A_3 is complemented when $A_2, A_1 = 1, 1$. and so on.

* Timing Diagram:



TITLE: 3 bit synchronous (binary) down counter

OBJECTIVES :

- To implement and verify 3 bit synchronous down counter.
- To find the relationship between inputs and outputs using JK flip-flop.

COMPONENTS :

- JK flip-flop
- Digital Kit
- Connecting wires
- Power supply.

THEORY:

- * In dr Introduction
- clock pulses are applied to the inputs of all flip-flops.
- The common pulse triggers all flip-flops simultaneously rather than at a time in succession.
- If $J=K=1$, the flip-flop remains unchanged.
- If $J=K=0$, the flip-flop toggles or complements.

* State Diagram:

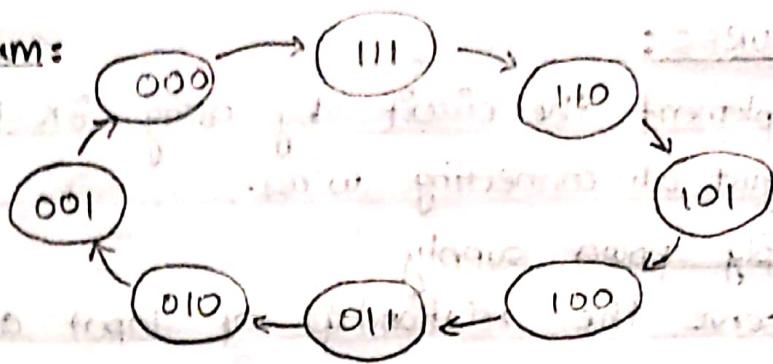


fig:- state diagram

* Circuit Diagram:

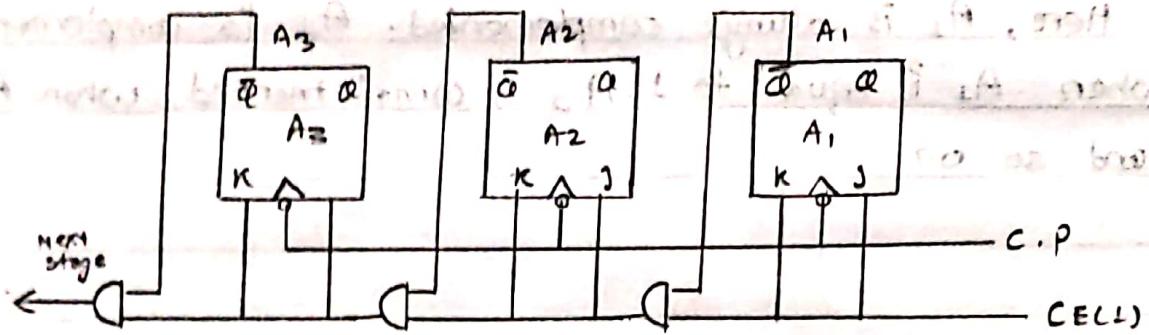


fig:- circuit diagram

* Truth Table:

	CLK	counter outputs			State	Decimal no
		A ₃	A ₂	A ₁		
Initially		0	0	0	1	0
1 st		1	1	1	2	1
2 nd		1	1	0	3	2
3 rd		1	0	1	4	3
4 th		1	0	0	5	4
5 th		0	1	1	6	5
6 th		0	1	0	7	6
7 th		0	0	1	8	7
8 th		0	0	0	9	8

PROCEDURES:

- Implement the circuit using JK-flip-flop.
- Adjust all connecting wires
- Apply power supply.
- Observe the relationship between Input and output.

RESULT:

Here, A_1 is always complemented. A_2 is complemented when $A_1 = 0$, A_3 is complemented when $A_2 = A_1 = 0, 0$ and so on.

* Timing Diagram: (प्रैग्या और स्टॉप्पा फैले देखिए)

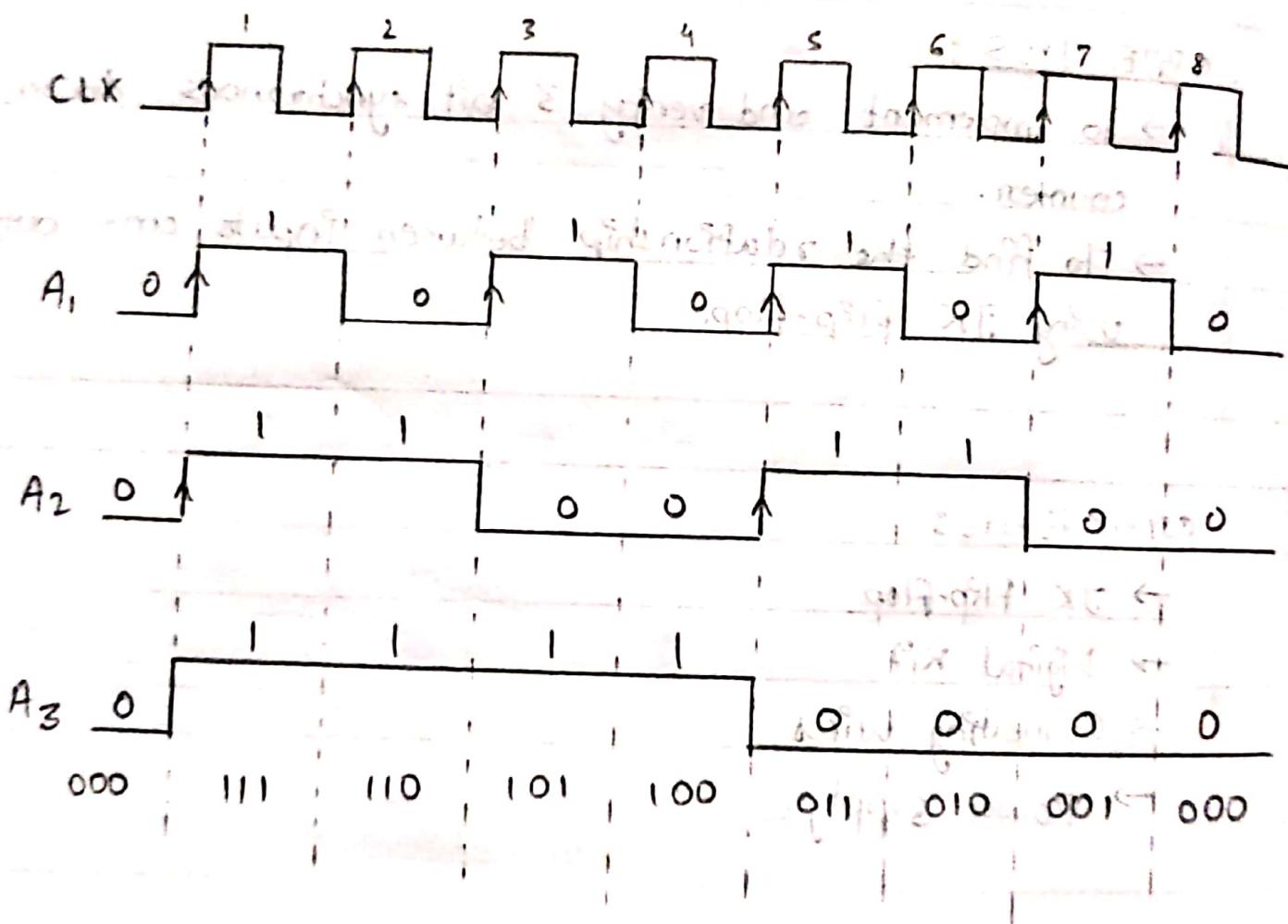


fig:- Timing Diagram of 3-bit binary down counter.

TITLE: SR Latch Using NOR Gate

OBJECTIVES:

- To implement and verify SR latch
- To find the relationship between inputs and outputs using SR latch using NOR gate

APPARATUS REQUIRED:

- 7402 (NOR gate) IC
- Digital kit
- Connecting wires
- Power supply.

THEORY

* Introduction

- SR latch is constructed using the cross coupled connections of two NOR gate.
- It has two inputs SET(S) and RESET(R) and two outputs Q and \bar{Q}

* Block Diagram:

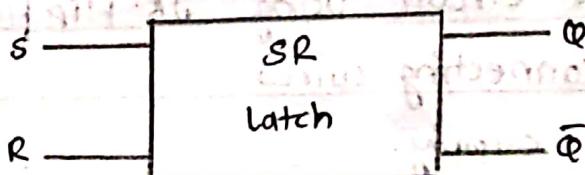


fig:- Graphic symbol.

* Circuit Diagram

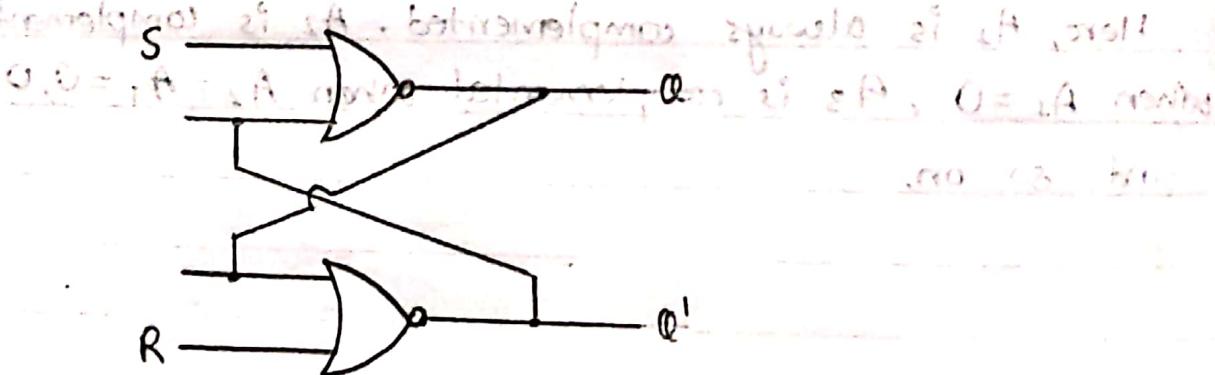


fig:- Circuit Diagram

* Truth Table

S	R	Q	\bar{Q}
0	1	0	1
0	0	0	1
1	0	1	0
0	0	1	0
1	1	0	0

(SET)

(Memory state)

(SET)

(Memory state)

(Invalid state)

PROCEDURE

- Implement the circuit by using 74102 IC
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

RESULT

when $S=0$ and $R=1$, $Q=0$ and $\bar{Q}=1$, which states RESET. similarly, when $S=0$ and $R=0$, $Q=0$ and $\bar{Q}=1$, which means memory state. When $S=1$ and $R=0$, $Q=1$ and $\bar{Q}=0$ which states SET, similarly, when $S=0$ and $R=0$, $Q=1$ and $\bar{Q}=0$ which means memory state. When $S=1$ and $R=1$, $Q=0$ and $\bar{Q}=0$ which is invalid state.

TITLE: SR Latch using NAND Gate

OBJECTIVES:

- To implement and verify SR Latch.
- To find the relationship between inputs and outputs using SR latch using NAND gate.

APPARATUS REQUIRED

- 7400 (NAND gate) IC
- Digital kit
- Connecting wires
- Power supply

THEORY

* Introduction

- SR latch is constructed by using cross coupled connection of two NAND gates.
- It has two inputs SET(s) & RESET(r) and two outputs Q and \bar{Q} .

* Block Diagram:

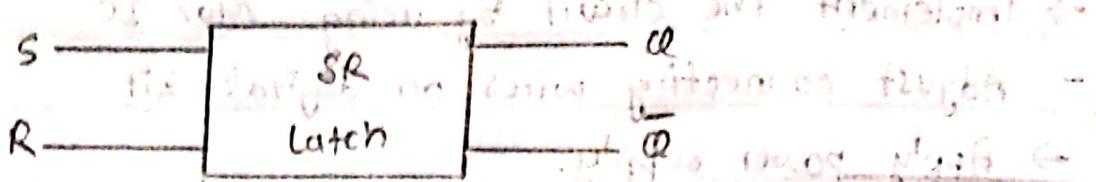


Fig:- Graphic symbol

* Circuit Diagram:

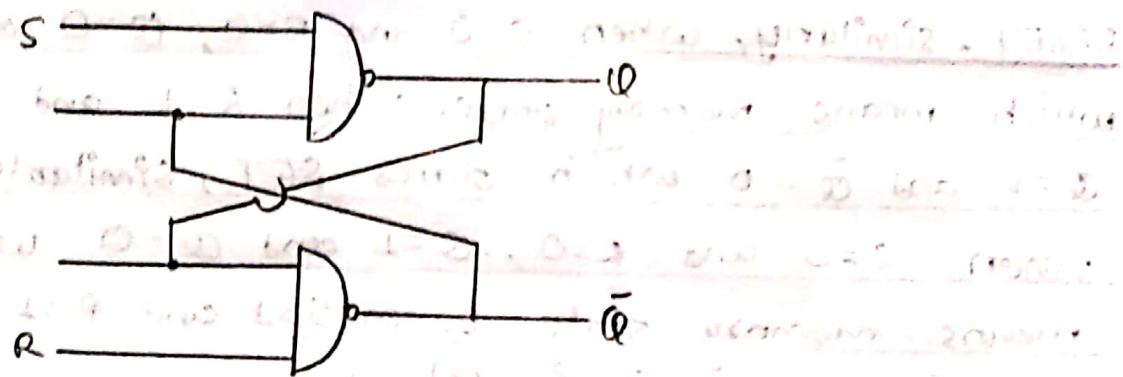


Fig:- Circuit Diagram

* Truth Table:

S	R	Q	\bar{Q}	
0	1	1	0	(SET)
1	1	1	0	(Memory state)
1	0	0	1	(RESET)
1	1	0	1	(MEMORY state)
0	0	1	1	(Invalid state)

Fig:- Truth Table

PROCEDURE :

- Implement the circuit by using 7400 IC.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

RESULT :

when $S=0$ and $R=1$, $Q=1$ and $\bar{Q}=0$, which states SET, similarly, when $S=1$ and $R=1$, $Q=1$ and $\bar{Q}=0$ which means memory state.

when $S=1$ & $R=0$, $Q=0$ & $\bar{Q}=1$, which states RESET. Similarly, when $S=1$ & $R=0$, $Q=0$ & $\bar{Q}=1$ which means memory state.

when $S=0$ & $R=0$, $Q=1$ & $\bar{Q}=1$ which is undetermined or invalid state.

TITLE : SR Latch flip-flop

OBJECTIVES :

- To implement and verify SR flip-flop.
- To find the relationship between inputs and outputs using SR flip-flop.

APPARATUS REQUIRED:

- 7400 (NAND gate) IC
- Digital kit
- Connecting wires
- Power supply.

THEORY

* Introduction

- A basic NAND gate SR flip-flop circuit provides feedback from both of its output back to its opposing inputs and is commonly used in memory circuit of to store a single data bit.
- It consists of the basic NAND latch and two other NAND gates.

* Block Diagram:

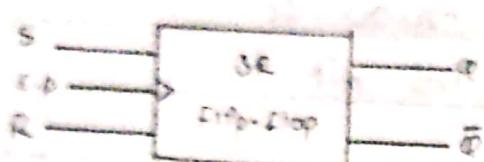


fig:- Logic symbol

* State Diagram:

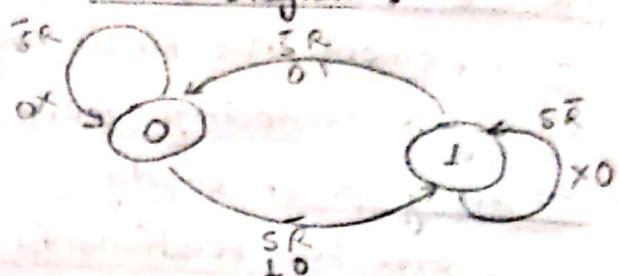


fig:- State diagram

* Circuit Diagram:

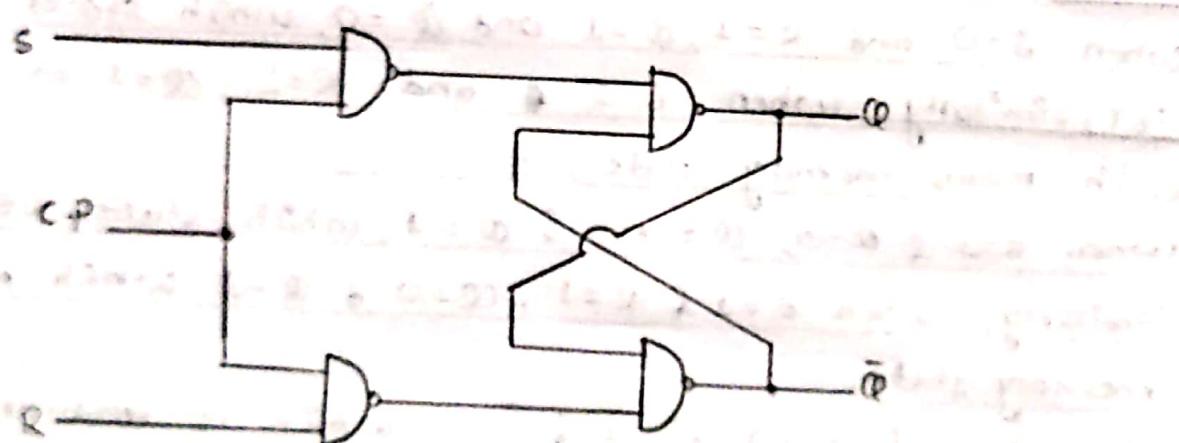


fig:- Circuit Table

* Truth Table:

CLK	S	R	Q	\bar{Q}
0	X	X	Memory	State
1	0	0	Memory	State
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	State

fig:- Truth Table

Functional Expression

$$\rightarrow CQn+1 = S + CQn\bar{Q}$$

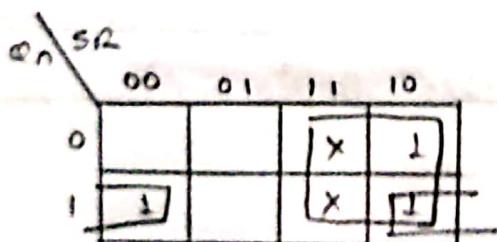
PROCEDURE

- Implement the circuit by using 7400 IC
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship between input/output.

* characteristics Table

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	L	0
0	1	0	L
0	1	L	X
1	0	0	1
1	0	L	0
1	L	0	1
1	L	L	X

* K-map from characteristic table



* Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

TITLE: D-flipflop

OBJECTIVES

- To implement and verify D-flip-flop
- To find the relationship between inputs and outputs using D-flipflop.

APPARATUS REQUIRED

- 7400 (NAND gate) IC
- Digital kit
- Connecting wires
- Power supply

THEORY

Introduction

- D flip-flop is the modification of clock SR flip-flop
- D flip-flop is used to eliminate the possibility of race condition that the SR flip-flop had created.
- It has input D and outputs Q and \bar{Q} .

Functional Expression

$$\rightarrow Q_{n+1} = D$$

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* Block Diagram

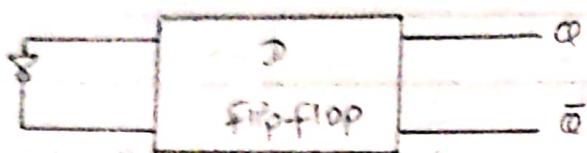


Fig:- Graphic symbol

* State Diagram

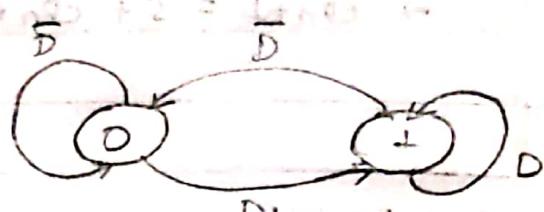


Fig:- State Diagram

* Circuit Diagram

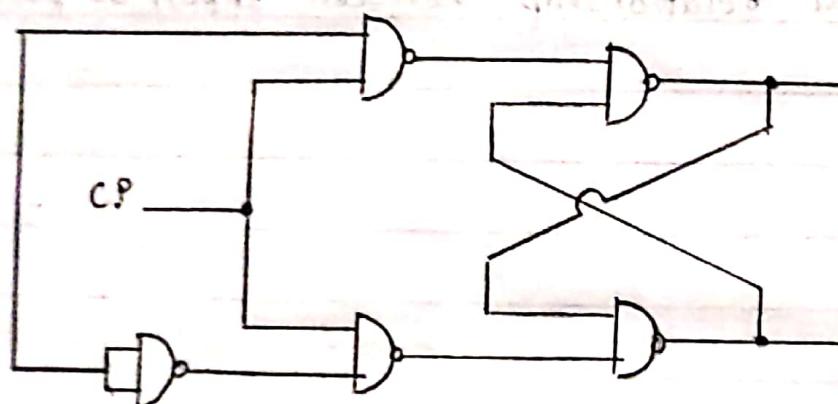


Fig:- Circuit Diagram

* Truth Table

CLK	D	Qout
0	x	Qn
1	0	0
1	1	1

Fig:- Truth Table

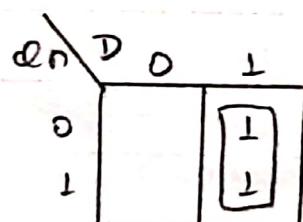
PROCEDURE

- Implement the circuit by using 7400 IC.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of Input/Output.

* Characteristics Table

C_{n+1}	D	C_n
0	0	0
0	1	1
1	0	0
1	1	1

* K-map from characteristics table



$$C_{n+1} = 0$$

* Excitation Table

C_{n+1}	C_n	D
0	0	0
0	1	1
1	0	0
1	1	1

fig:- Excitation Table

TITLE :- JK flipflop

OBJECTIVES

- To implement and verify JK flipflop
- To find the relationship between inputs and outputs using JK flip-flop.

APPARATUS REQUIRED

- 7400 (NAND gate) IC
- Digital Kit
- Connecting wires
- Power supply

THEORY

Introduction

- JK flipflop is the refinement of SR flip-flop to solve the problem of invalid state when both inputs are 1.
- In JK flip-flop, inputs J and K behaves like inputs S & R to 'SET' and 'RESET' the flipflop.
- JK flipflop is used to overcome -not used state in SR flip-flop.

* Logical Diagram

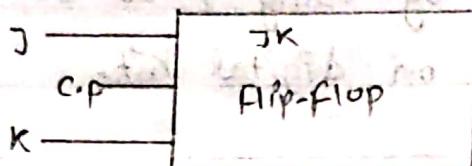


fig:- Block diagram of JK flip-flop

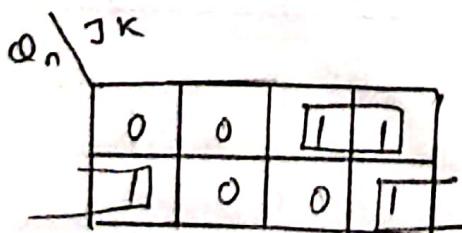
* Truth Table

CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0 (RESET)
1	1	0	1 (SET)
1	1	1	\bar{Q}_n

* Characteristic Table

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

* K-map for Q_{n+1}



$$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K}$$

Functional Expression

$$\rightarrow Q_{n+1} = \overline{Q_n J} + Q_n \overline{K}$$

PROCEDURE

- Implement the circuit by using 7400 IC.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of input/output.

* Excitation Table

Cln	Cln+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

* State Diagram



* Logic Circuit Diagram

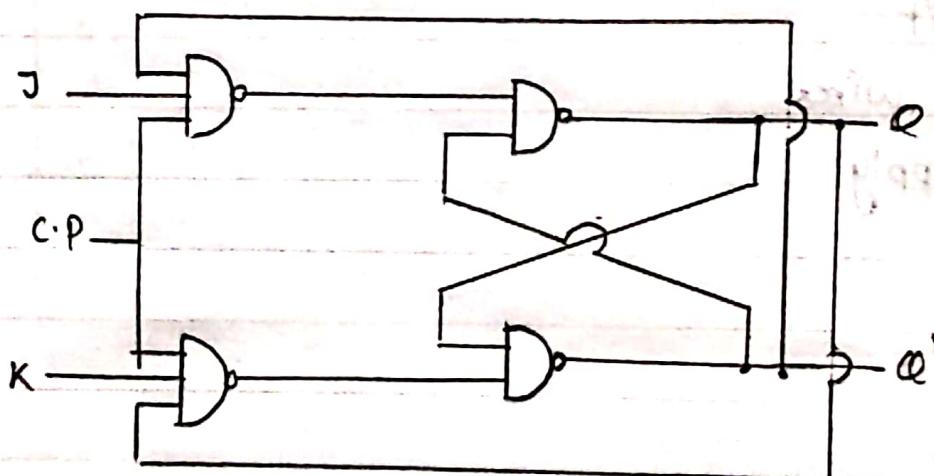


fig:- logic circuit diagram of JK flip-flop.

* TITLE: T-flip flop.

* OBJECTIVE

- To implement and verify T-flip flop.
- To find the relationship between Pinputs and outputs using T-flip flop.

* Apparatus Required

- 7400 (NAND gate) IC
- Digital kit
- connecting wires
- Power supply.

* THEORY

Introduction :-

- T - flip flop is a single input version of JK flip-flop.

functional Expression

$$C_{n+1} = Q_n \oplus T$$

* Logic symbol

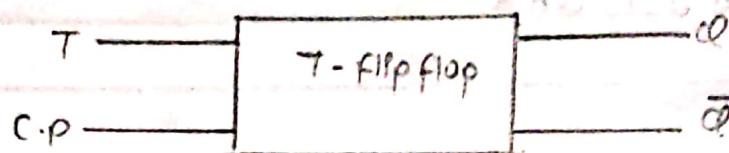


fig:- Block diagram of T-flip flop

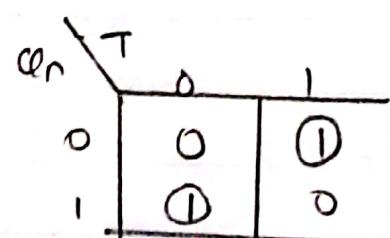
* Truth Table

CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	\bar{Q}_n

* Characteristics Table

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

* K-map for Q_{n+1}



$$\therefore Q_{n+1} = Q_n \oplus T$$

PROCEDURE

- Implement the circuit using 7400 (NAND) IC.
- Adjust connecting wires on digital kit.
- Apply power supply.
- Observe the relationship of I/O.

* Growth Table

Q_n	C_{n+2}	T
0	0	0
0	1	1
1	0	1
1	1	0

* State Diagram



* Logic Circuit Diagram:

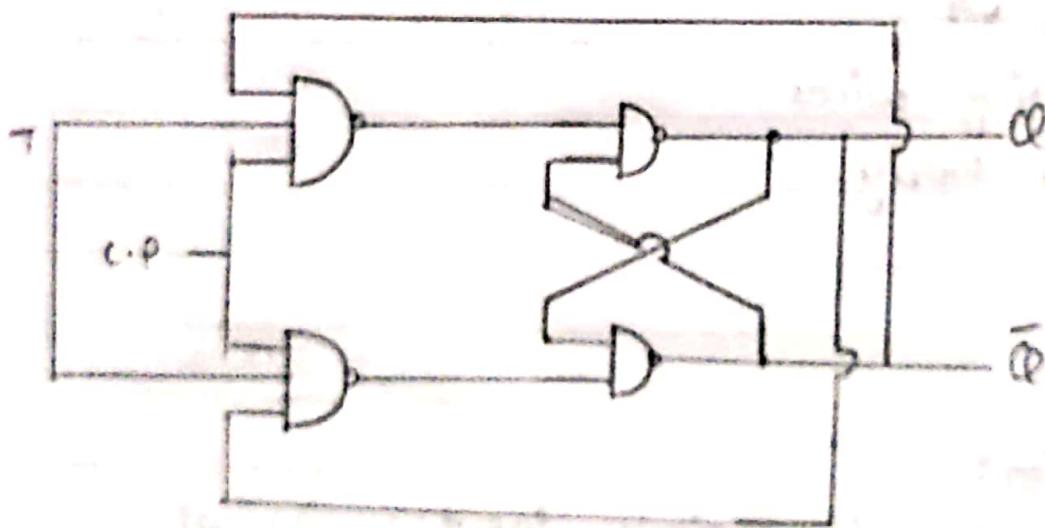


Fig:- Circuit Diagram of T-flip-flop