논리회로설계 HW #5

2019112130 최부광 (004분반)

Source Code	O
Waveform	O

1. Source Code

- delay.v

```
`timescale 1ns/100ps
module delay(output out, input in, ctrl);

        // NOTIF0 gate has delay
        notif0 #(40,60,80) nif0 (out, in, ctrl);
endmodule
```

- delay_tb.v

```
`timescale 1ns/100ps
module delay_tb();
  reg a,b;
  wire y_2130;

  delay d0(.out(y_2130),.in(a),.ctrl(b));

  initial begin
    $dumpfile("output.vcd");
    $dumpvars(0);

    a = 0;
    b = 0;
    #1000 $finish;
  end
always begin
    #100 a = ~a;
    #100 b = ~b;
  end
endmodule
```

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2. Waveform