논리회로설계 HW #4

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Source code	O
Waveform	O

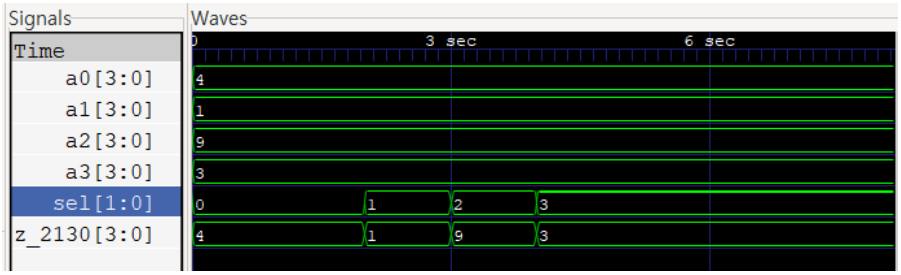
1. Source code

- 4:1 Mux Module

```
module mux4(x0,x1,x2,x3,sel,y);
 input [3:0] x0,x1,x2,x3; // input
 input [1:0] sel; // control
 output reg [3:0] y; // output

 always@(*) begin
  case(sel)
        2'b00: y = x0;
        2'b01: y = x1;
        2'b10: y = x2;
        2'b11: y = x3;
       endcase
 end
endmodule
```

2. Waveform



- Testbench

```
module mux4_tb();
 reg [3:0] a0,a1,a2,a3;
 reg [1:0] sel;
 integer i;
 wire [3:0] out;

 mux4 m1(a0,a1,a2,a3,sel,out); // mux instance

 initial begin
  $dumpfile("output.vcd");
  $dumpvars();
 end

 initial  begin
  a0 = $random; a1 = $random;
  a2 = $random; a3 = $random;
  sel = 0;

  for(i=0; i < 4; i=i+1)
   #1 sel = i;

   #6 $finish;
 end
endmodule
```