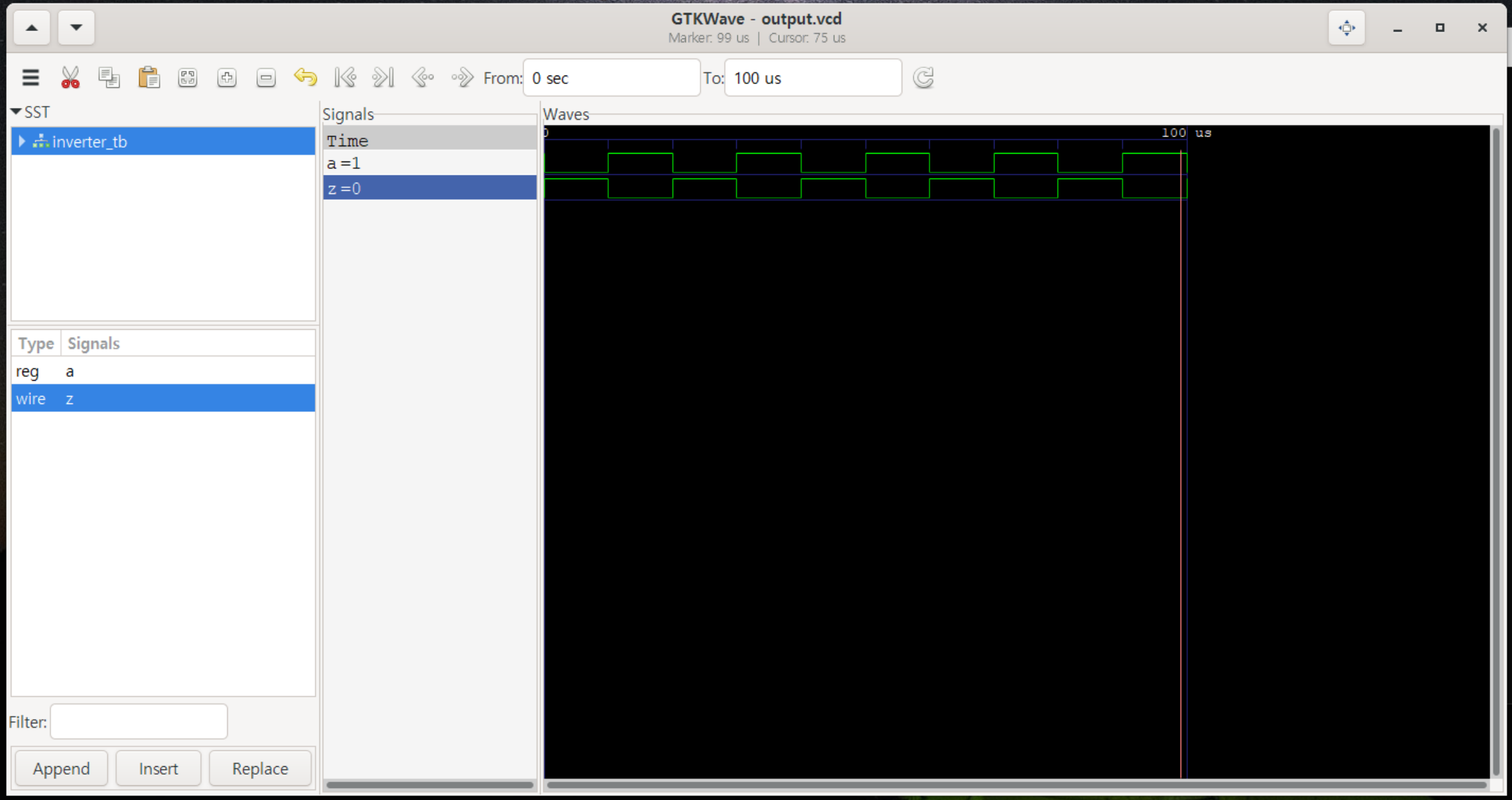
inverter.v | inverter_tb.v

```
1  module inv(a,z);
2    input a;
3    output z;
4
5    assign z = ~a;
6  endmodule
```

inverter.v | inverter_tb.v

```
1  `timescale 1us/1us
2  module inverter_tb();
3    reg a;
4    wire z;
5
6    inv u1(a,z);
7
8    initial begin
9      a = 0;
10     #100 $finish;
11   end
12
13   always begin
14     #10 a = ~a;
15   end
16
17   initial begin
18     $dumpfile("output.vcd");
19     $dumpvars(0);
20   end
21 endmodule
```


GTKWave - output.vcd
Marker: 99 us | Cursor: 75 us
From: 0 sec
To: 100 us
SST
inverter_tb
Type Signals
reg a
wire z
Filter:
Append
Insert
Replace
Signals
Time
a =1
z =0
Waves
100 us