

COMP311: Logic Circuit Design

Spring 2022, Prof. Taigon Song

Final Project. Due: June 22 11:59pm [Total: 150 points]

Additional Document

(last updated: 2022. 6. 15)

1. A figure for reference:

Figure 1 describes how your processor should be designed.

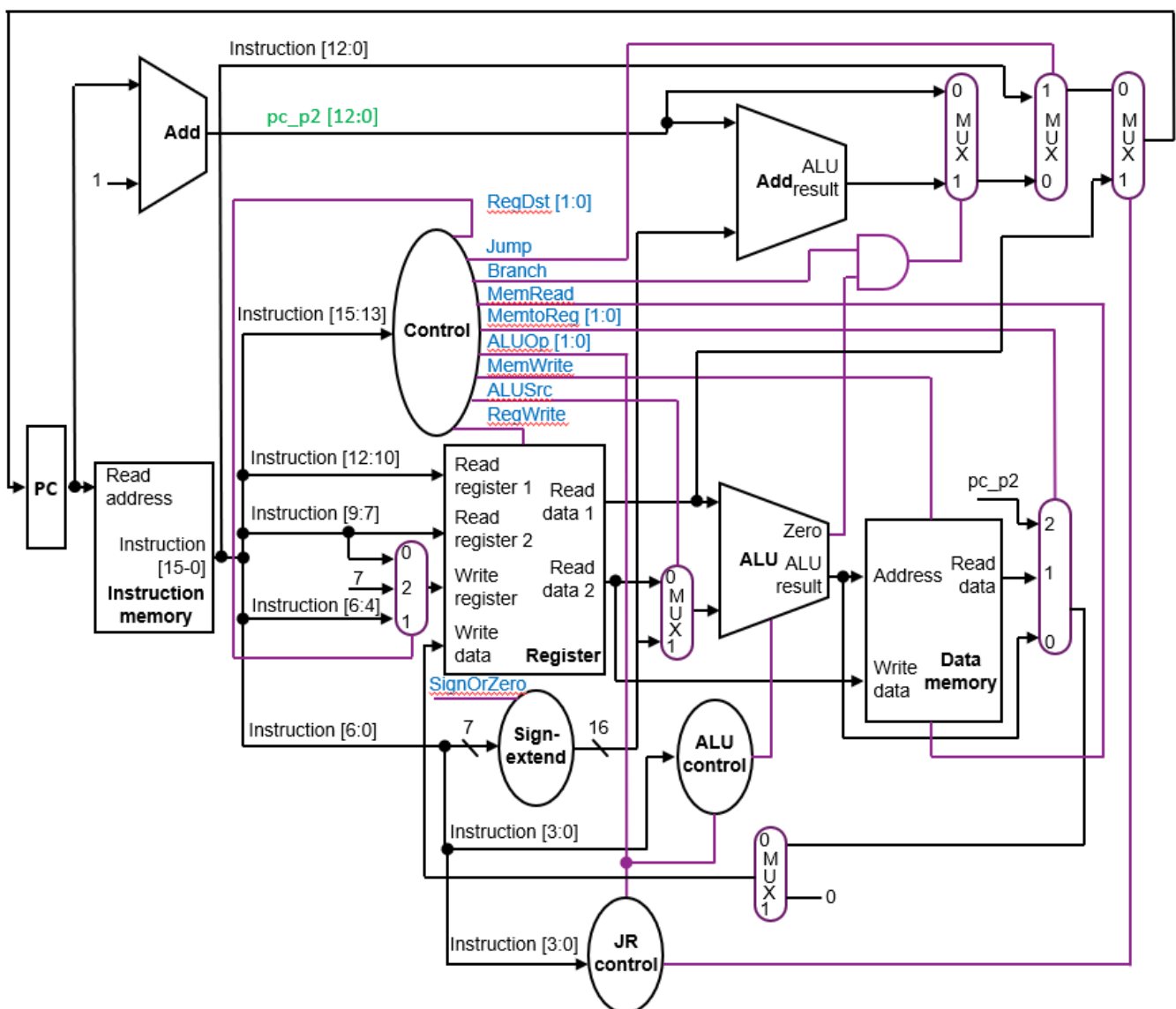


Figure 1 – Full diagram of the 16-bit MIPS architecture

2. Some additional instructions:

- Please print an iVerilog figure like Figure 2. ID should be the last 4 digits of your student ID.
- After “RF[0, 1, 2, 3, 4, 7] is: ”, you should print the according RF values at every ns.
- ‘final PC # processed’ is the PC # that was lastly processed right before ‘0000_0000_0000_0000’.

```
ID:1234, at time      2000 ps, PC = 0, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time      3000 ps, PC = 1, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time      4000 ps, PC = 2, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time      5000 ps, PC = 3, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time      6000 ps, PC = 4, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time      7000 ps, PC = 5, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time      8000 ps, PC = 6, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time      9000 ps, PC = 7, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     10000 ps, PC = 8, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     11000 ps, PC = 9, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     12000 ps, PC = 10, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     13000 ps, PC = 11, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     14000 ps, PC = 12, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     15000 ps, PC = 13, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     16000 ps, PC = 14, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     17000 ps, PC = 15, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     18000 ps, PC = 16, RF[0, 1, 2, 3, 4, 7] is:
ID:1234, at time     19000 ps, PC = 17, RF[0, 1, 2, 3, 4, 7] is:
The final result of $s3 in memory is: 0
```

Figure 2 – How you should display your final results
(the ordering of PC and the final result should be different from this figure)