

# **MOSFET Amplifiers**

- 7.1: Basic Principles
- 7.2: Small Signal operation
- 7.3: Basic Configurations
- 8.2: Biasing
- 8.3: Gain Cell
- 8.5: Cascode Amplifiers
- 8.6: IC Source Follower

# Transistor Applications

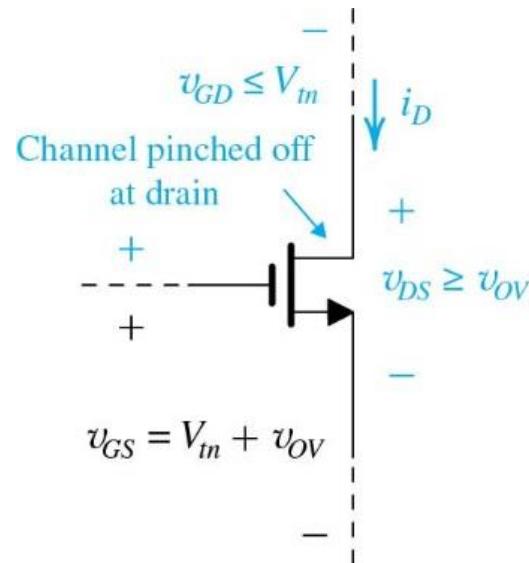
- Two different applications
  - As a switch in design of digital circuits
  - **As a controlled source in the design of amplifiers for analog circuits**

# MOSFET as an Amplifier

- MOSFET's as an Amplifier – the transistor operation in ~~Active~~ (Saturation) Region
- A voltage ( $v_{GS}$ ) controlled current source  $i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2$
- $v_{GS} > V_t$  and  $v_{DS} > v_{GS} - V_t$

$$i_D \propto v_{GS}^2$$

not linear



$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2$$

# Small Signal Model of the MOSFET

- MOSFET is operating in the ~~active~~<sup>Saturation</sup> mode
- The voltage applied between G and S has two components: DC voltage  $V_{GS}$  and an ac signal  $v_{gs}$
- $v_{GS} = V_{GS} + v_{gs}$
- $i_D = I_D + i_d$  .....

## DC Components: Review from Chapter 5

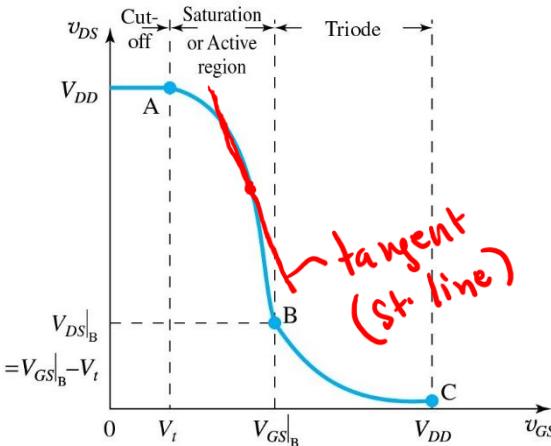
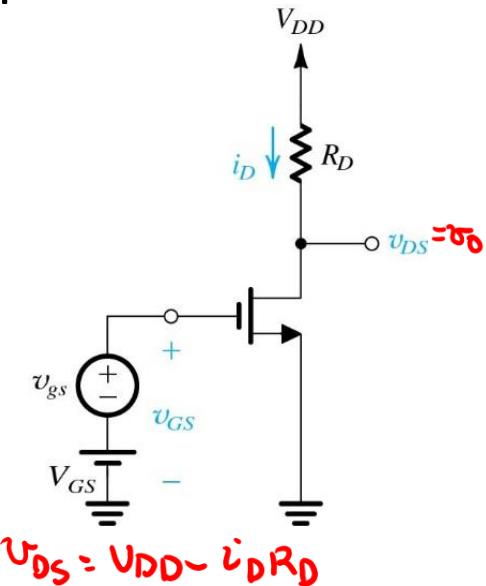
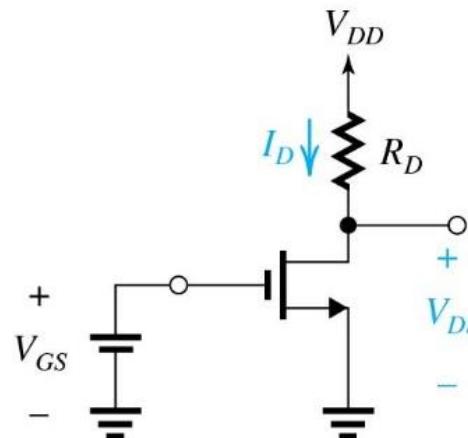
- $I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 = \frac{1}{2} k_n (V_{OV})^2$

$$V_{DS} = V_{DD} - I_D R_D$$

- For Active Region operation:

$$V_{DS} > V_{GS} - V_t$$

$$V_{DS} > V_{OV}$$



# Small Signal Model of the BJT MOSFET

- AC Components:  $i_d$  and  $v_{gs}$

- $v_{GS} = V_{GS} + v_{gs}$

- $i_D = \frac{1}{2} k_n (V_{GS} + v_{gs} - V_t)^2 = \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n v_{gs}^2$

$I_D + i_d = (V_{GS} - V_t + v_{gs})^2$

- For small  $v_{gs}$

- $\frac{1}{2} k_n v_{gs}^2 \ll k_n (V_{GS} - V_t) v_{gs}$

- $v_{gs} \ll 2(V_{GS} - V_t)$

- Or  $v_{gs} \ll 2V_{OV}$

- Last term  $\frac{1}{2} k_n v_{gs}^2$  ignored

- $i_D = I_D + i_d$

- $i_d = k_n (V_{GS} - V_t) v_{gs}$

$V_{GS} \rightarrow DC$

$v_{gs} \rightarrow AC$

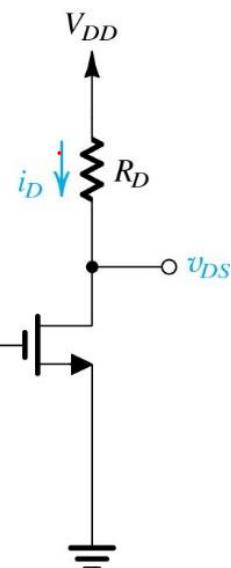
$V_{GS} = DC + AC$

$a^2$

$2ab$

$b^2$

$i_d$

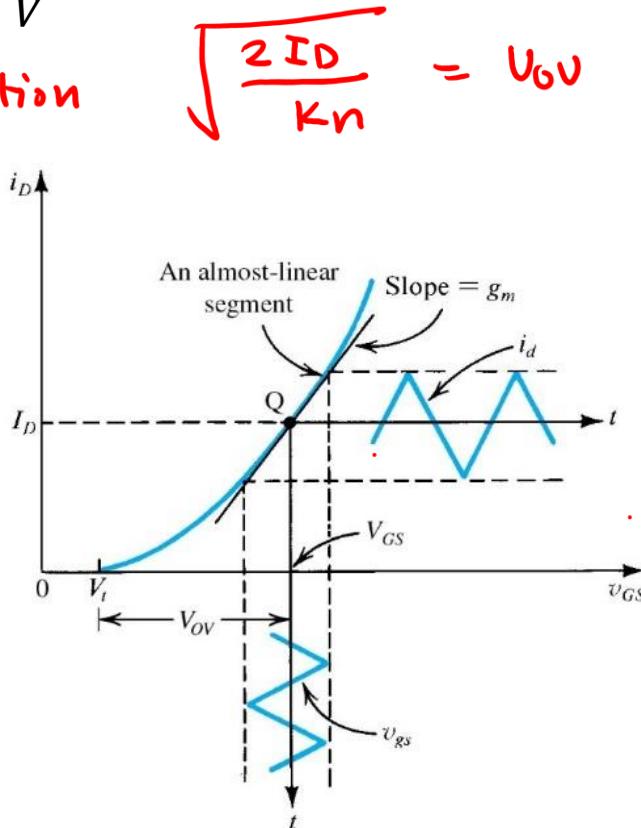


# Small Signal Model of the ~~BJT~~<sup>MOSFET</sup>

- **AC Components:** In linear relationship:  $i_d = k_n(V_{GS} - V_t) v_{gs}$
- $i_d = g_m v_{gs}$ ,  $g_m$  is the transconductance and is equal to the slope of  $i_d - v_{gs}$  characteristics  $\frac{i_d}{v_{gs}} = g_m = k_n(V_{GS} - V_t) = k_n V_{OV}$
- $g_m = \frac{i_d}{v_{gs} V} = k_n(V_{GS} - V_t) = k_n V_{OV}$  in  $\frac{mA}{V}$

$$I_D = \frac{1}{2} k_n (V_{OV})^2 \quad \text{Saturation region operation}$$

$g_m$  is the slope of the curve at  $v_{GS} = V_{GS}$



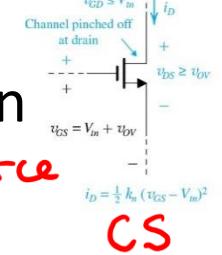
# Small Signal Model of the BJT

MOSFET

A voltage signal  $v_{gs}$  between Gate and Source provides a current  $g_m v_{gs}$  at the drain terminal

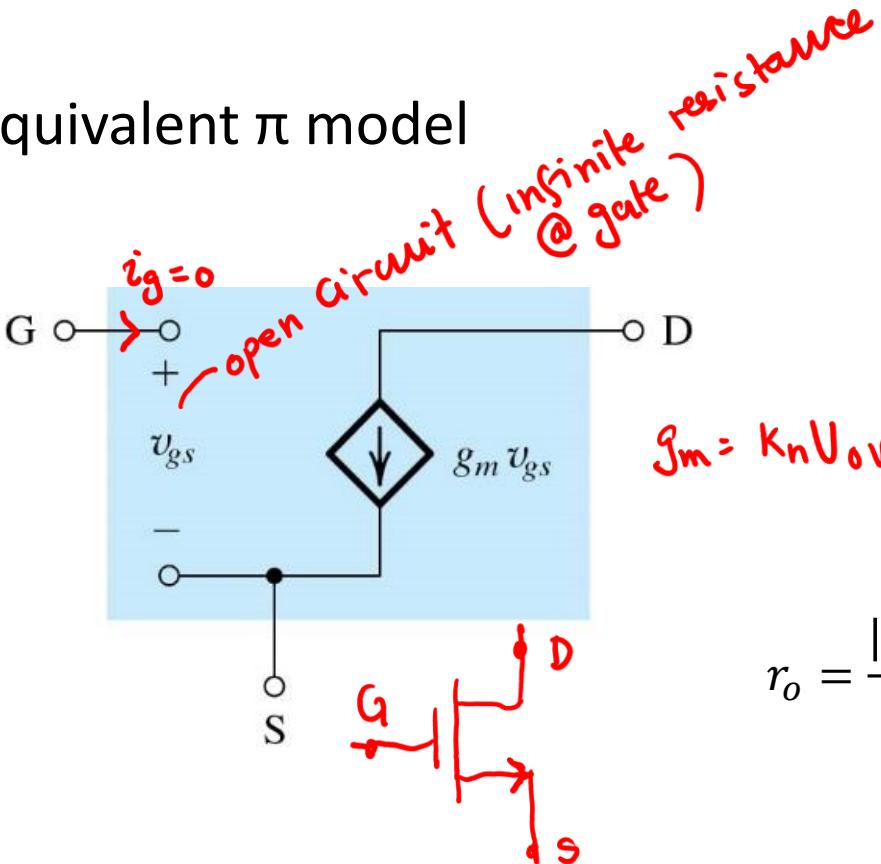
$i_d \rightarrow$  dependent current source

$$i_d = g_m v_{gs}$$



Input resistance of this controlled source is very high – infinite as  $i_g = 0$

Equivalent  $\pi$  model

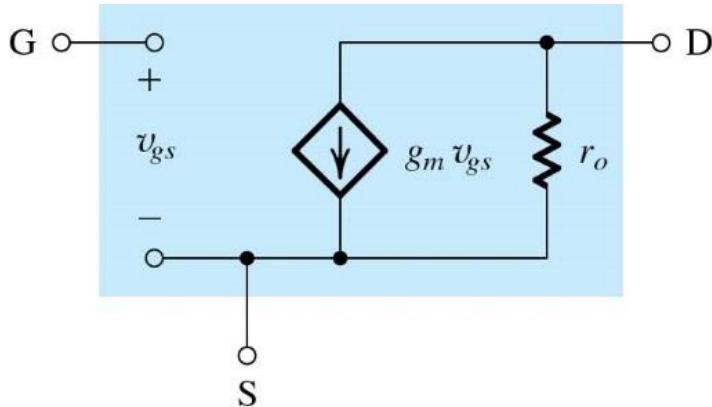


$$g_m = k_n V_{ov}$$

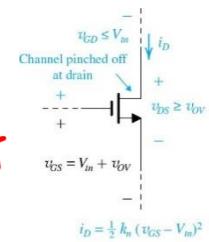
$$r_o = \frac{|V_A|}{I_D}$$



CLM is not ignored

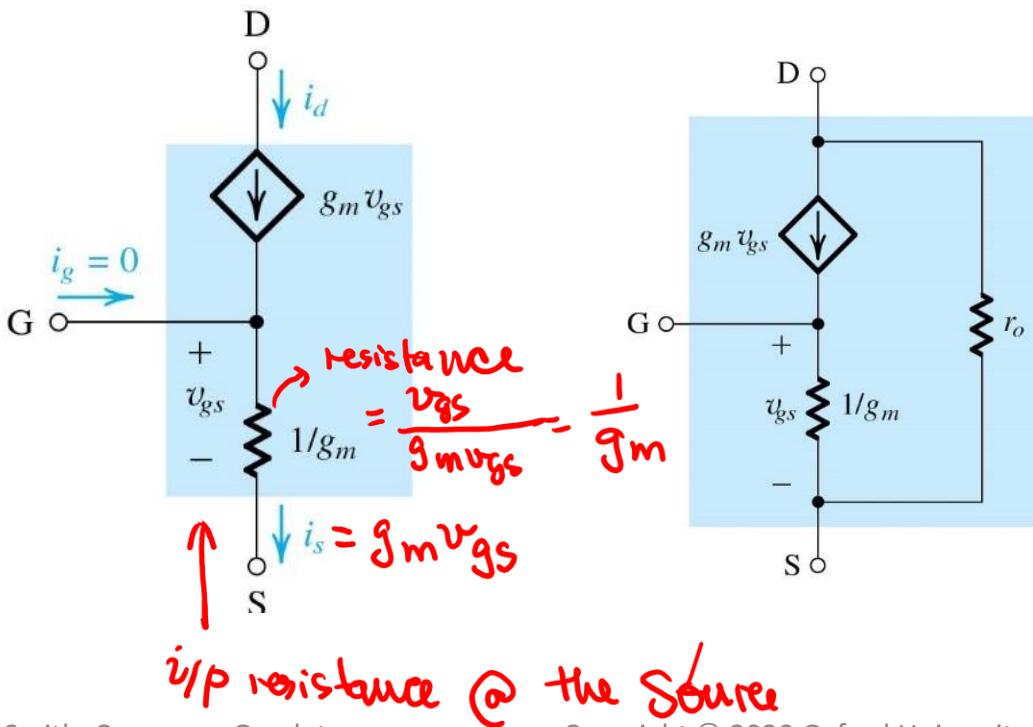


# Small Signal Model of the BJT



- $i_g = 0$
- $i_s = \frac{v_{gs}}{(1/g_m)} = i_d$ : Input resistance at **Source**

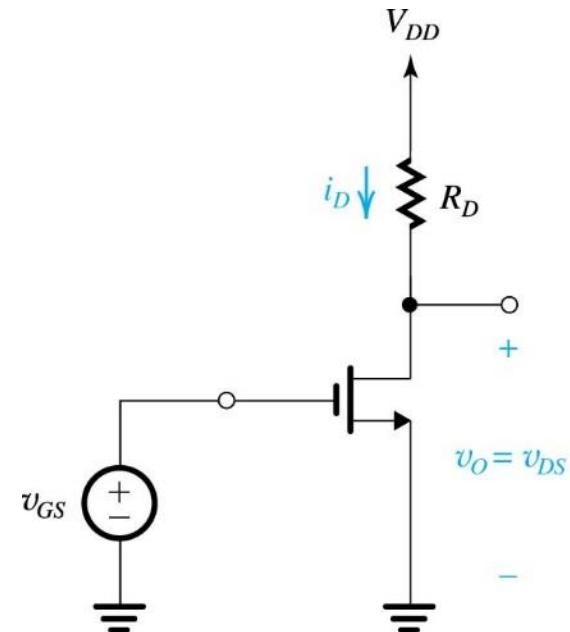
- Equivalent T model



# MOSFET as a Voltage Amplifier

- In the absence of an AC signal, the voltage and currents will settle at their DC ( or quiescent) values. The amplifier works when  $v_{GS}$  varies around its DC value  $V_{GS}$
- Transistor is a transconductance amplifier – input signal is voltage and output signal is current
- Transconductance Amplifier to a Voltage Amplifier

$$v_{DS} = V_{DD} - i_D R_D$$



# Amplifier Circuit Analysis

- The MOSFET behave like BJT's with  $\beta = \infty$  
$$\beta = \frac{i_c}{i_b}$$
- Similar methods of analysis can be carried out for MOSFET amplifier circuits as for the BJT
- In general, MOSFET amplifiers provide lower gain than BJT Amps
- DC Analysis
  - Remove the ac signal and assume all Capacitors are open
  - determine the DC voltage and currents
  - Verify the ~~active~~ mode
- AC Analysis **Saturation**
  - Assume **DC sources** are turned OFF (voltage sources short and current sources open)
  - Replace capacitor with short wires
  - Replace MOSFET with small signal model ( $\pi$  or T model)
  - Solve required AC parameters
    - No-load voltage gain ( $A_{VO}$ )
    - Loaded voltage gain ( $A_V$ )
    - Input resistance:  $R_i$  ( $R_{in}$ )
    - Output resistance:  $R_O$  ( $R_{out}$ )

# MOSFET as a Voltage Amplifier

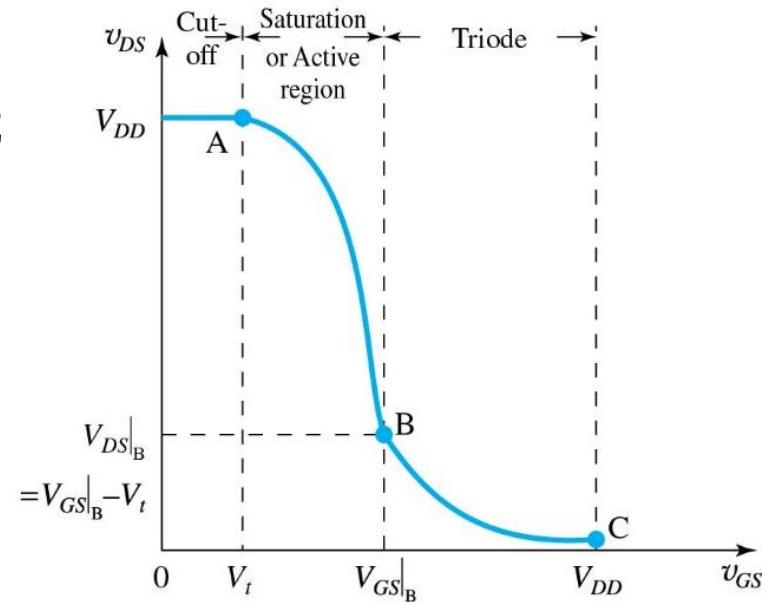
- Voltage Transfer Characteristics – plot of the output voltage ( $v_{DS}$ ) versus the input voltage ( $v_{GS}$ )

$$v_{DS} = V_{DD} - i_D R_D$$

- In Active region:

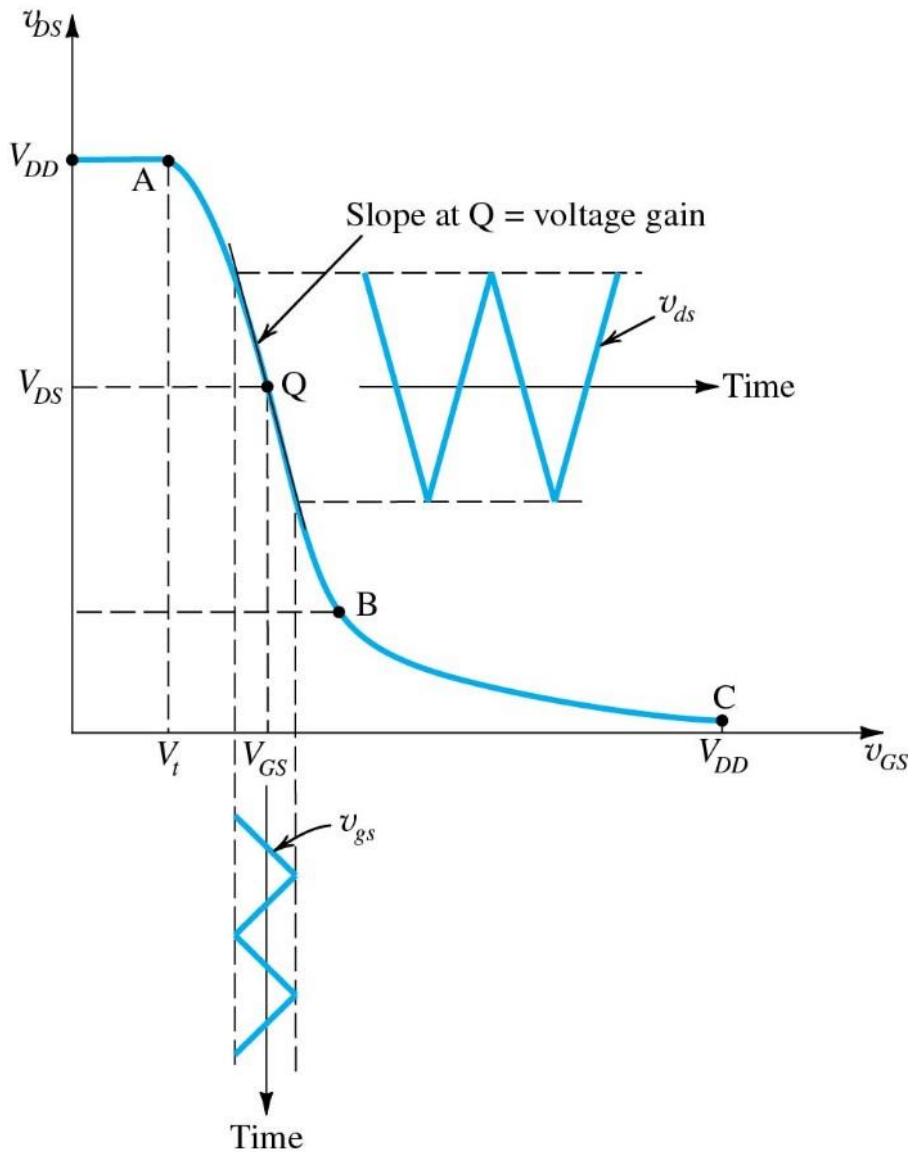
$$v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (V_{GS} - V_t)^2$$

- Non-linear relationship



# MOSFET as a Voltage Amplifier

- linear region



# MOSFET as a Voltage Amplifier – Voltage Gain

- Small – signal Voltage Gain:

$$v_{DS} = V_{DD} - i_D R_D = V_{DD} - (I_D + i_d)R_D = (V_{DD} - I_D R_D) - i_d R_D$$

- $v_{DS} = V_{DS} - i_d R_D$

- $v_{ds} = -i_d R_D = -g_m v_{gs} R_D$

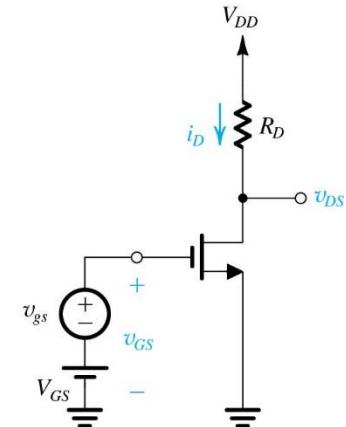
- The voltage gain:

- $A_v = \frac{v_{ds}}{v_{gs}} = -g_m R_D$

- $A_v = \left. \frac{dv_{DS}}{dv_{GS}} \right|_{v_{GS}=V_{GS}} = \left. \frac{d[V_{DD} - \frac{1}{2}k_n R_D (V_{GS} - V_t)^2]}{dv_{GS}} \right|_{v_{GS}=V_{GS}} = -k_n (V_{GS} - V_t) R_D$

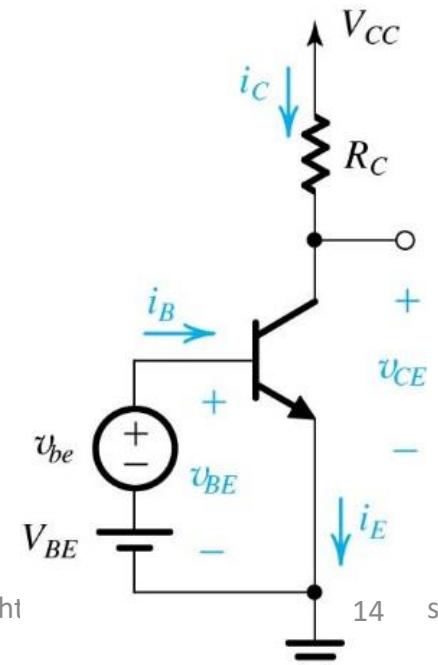
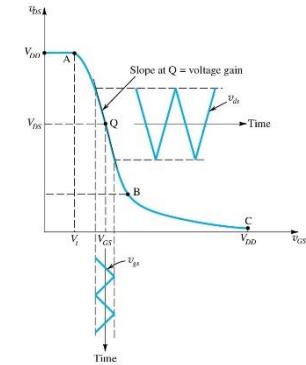
- The gain is negative – amplifier is inverting

- The gain is proportional to the override voltage,  $V_{OV}$



# MOSFET as a Voltage Amplifier – Voltage Gain

- The voltage gain:
- $A_v = \frac{v_{ds}}{v_{gs}} = -k_n(V_{OV})R_D = -\frac{2I_D}{V_{OV}^2} V_{OV} R_D = -\frac{I_D R_D}{V_{OV}/_2}$
- $A_v = -\frac{V_{DD}-V_{DS}}{V_{OV}/_2}$
- The maximum gain is achieved when  $V_{DS}$  is at its minimum value at point B



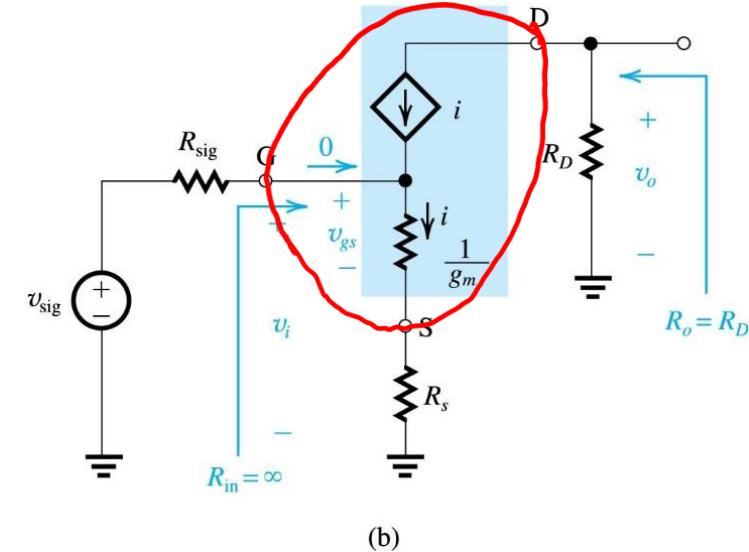
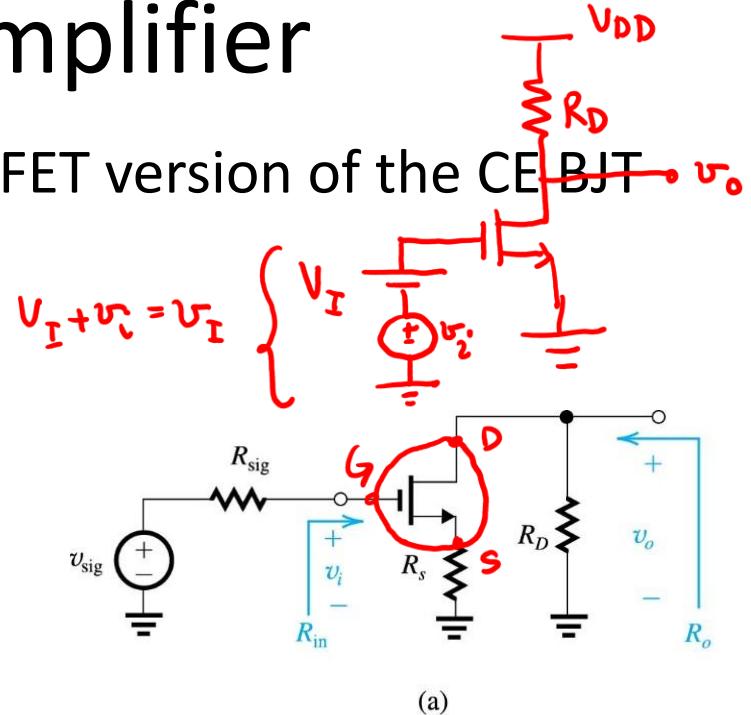
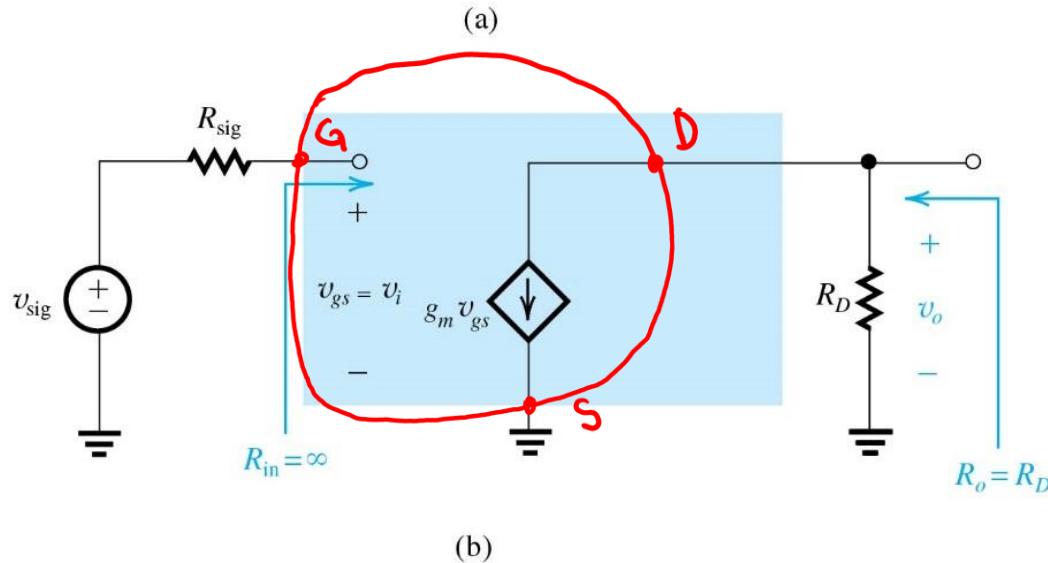
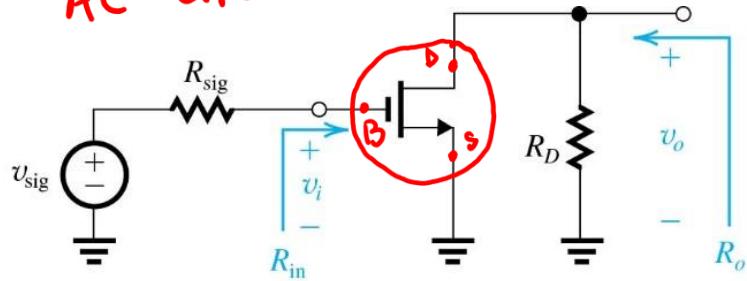
# MOSFET Amplifier – Configurations

- Common Source (CS) Amplifier
- Common Drain (CD) Amplifier
- Common Gate (CG) Amplifier

# MOSFET CS Amplifier

- Common Source (CS) Amplifier – MOSFET version of the CE BJT Amplifier
  - Input at the Gate
  - Output at the Drain

**AC circuit**



# MOSFET CS Amplifier

- Input Resistance,  $R_{in}$  :
- As  $i_G = 0$  in a MOSFET,  $i_i = 0$ :  $R_{in} = \frac{v_i}{i_i} = \infty$
- For a BJT:  $R_{in} = r_\pi + [(\beta + 1)(R_e)]$  MOSFET is a BJT with  $\beta = \infty$

$R_o \rightarrow$  Thevenin's Theorem

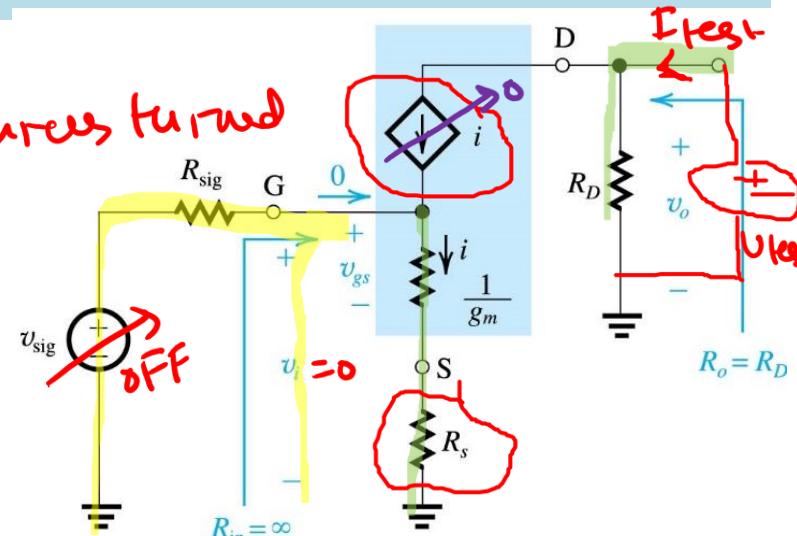
$$R_o = \frac{V_{test}}{I_{test}} \quad [\text{w all independent sources turned OFF}]$$

$$v_{sig} = 0 \Rightarrow v_i = 0 \Rightarrow i_i = i / (R_s + 1/g_m)$$

$$\bullet \text{ Output Resistance, } R_o : \frac{V_{test}}{I_{test}} = R_D$$

$$\bullet \text{ Short the input, } i = 0: R_o = R_D$$

$$\bullet \text{ Same as for the BJT: } R_o = R_C$$



# MOSFET CS Amplifier

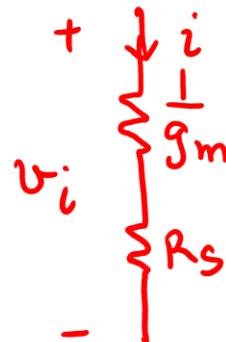
- No-load Voltage Gain  $A_{VO} = \frac{v_o}{v_i} \Big|_{R_L=\infty}$

- $v_o = -iR_D$

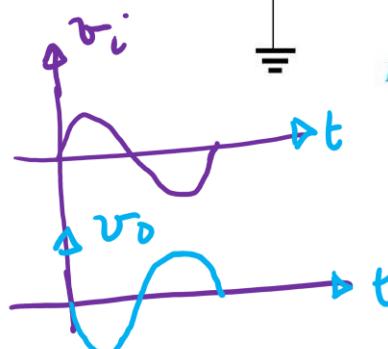
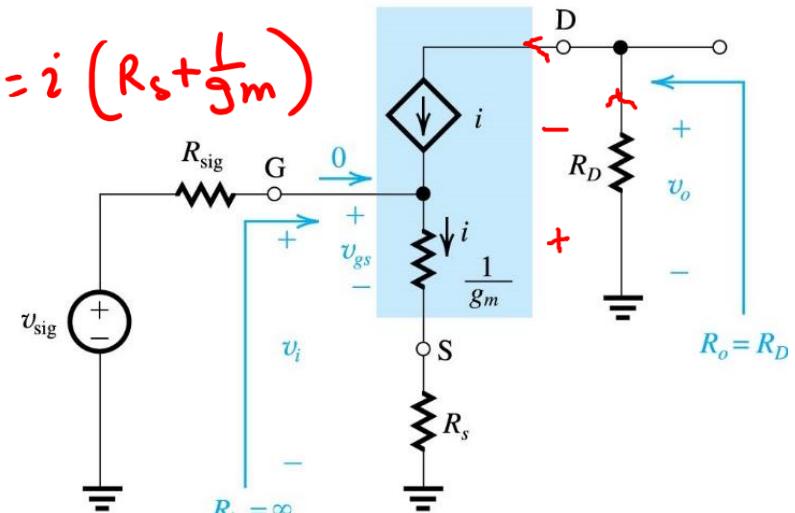
- $i = \frac{v_i}{R_S + \frac{1}{g_m}}$

- $v_o = -\frac{R_D}{R_S + \frac{1}{g_m}} v_i$

- $A_{VO} = -\frac{R_D}{R_S + \frac{1}{g_m}} = -\frac{R_D g_m}{1 + g_m R_S}$



$$v_i = i \left( R_s + \frac{1}{g_m} \right)$$



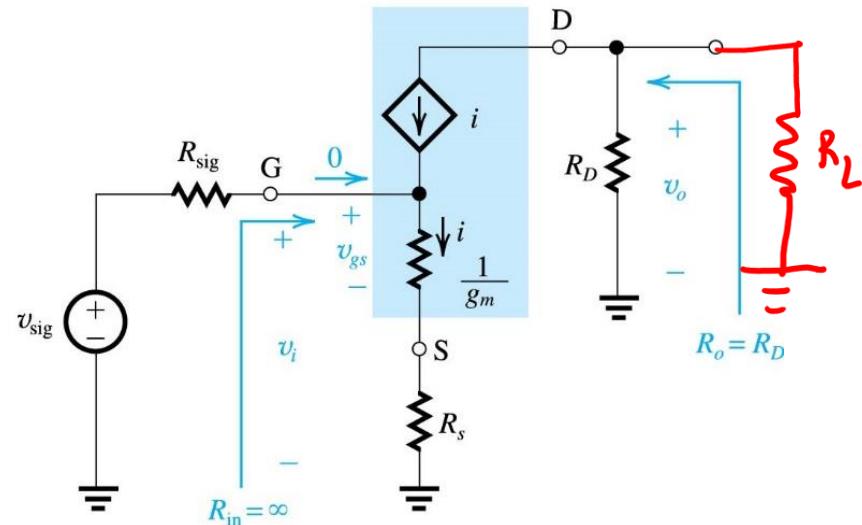
$$- A_{VO} = - \frac{g_m R_C}{1 + g_m R_e}$$

- CS amplifier is inverting by nature
- the gain is largest when  $g_m R_S = 0$ , i.e.  $R_S = 0$

# MOSFET CS Amplifier

- Loaded Voltage Gain  $A_V = \frac{v_o}{v_i} \Big|_{R_L \neq \infty}$

$$A_V = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$$

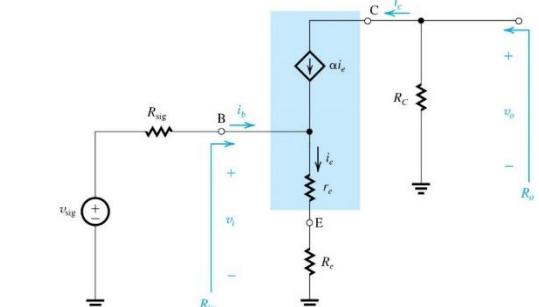
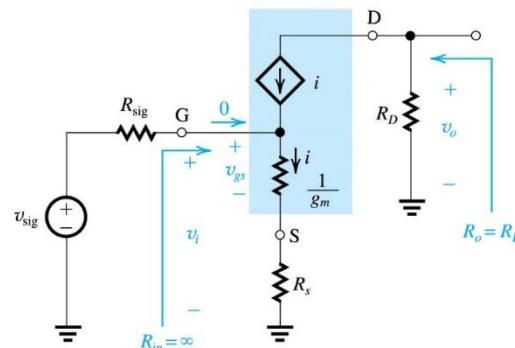


- $|A_V| < |A_{VO}|$  as  $(R_D \parallel R_L) < R_D$
- For a given  $v_i$ ,  $v_o$  decreases when a load is connected
- To minimize the impact of connected load  $R_L$ , set  $R_D \ll R_L$

# MOSFET CS and BJT CE Amplifier Comparison

	CS (MOSFET)	CE (BJT)
$A_{VO}$	$-\frac{R_D g_m}{1 + g_m R_S}$	$-\frac{R_C g_m}{1 + g_m R_e}$
$A_V$	$-\frac{g_m (R_D \parallel R_L)}{1 + g_m R_S}$	$-\frac{g_m (R_C \parallel R_L)}{1 + g_m R_e}$
$R_{in}$	$\infty$	$r_\pi + (\beta + 1)(R_e)$
$R_O$	$R_D$	$R_C$

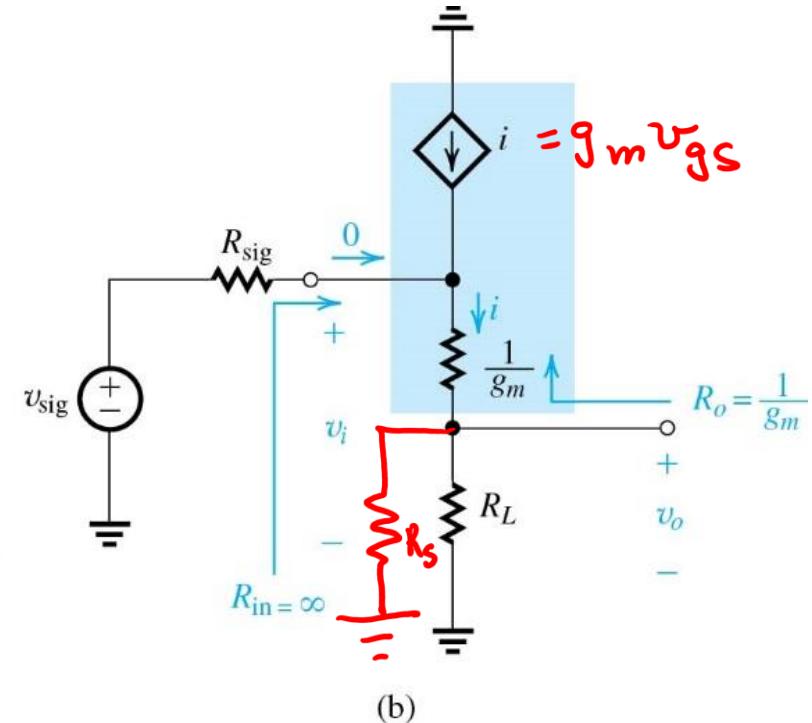
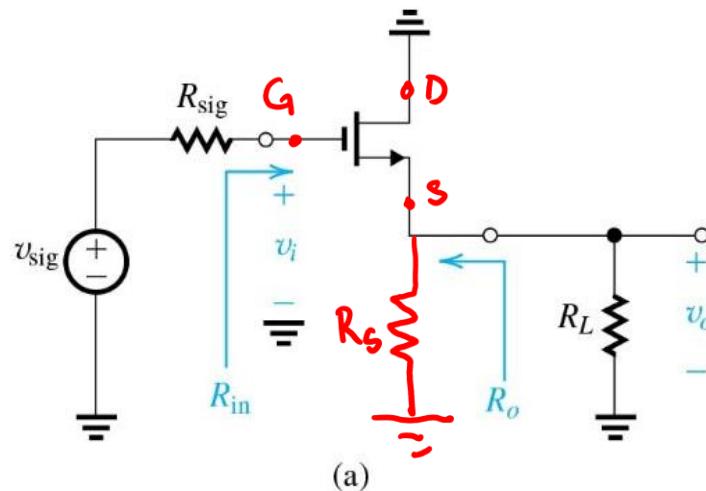
Both configurations are used for majority of the Gain in a multistage amplifier circuit



# MOSFET Common Drain (CD) Amplifier

CC : BJT

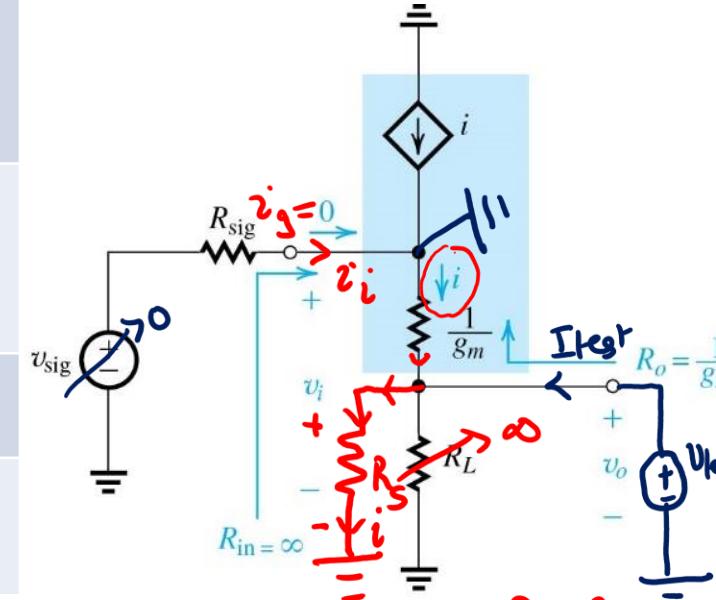
- Common Drain (CD) – Source Follower Amplifier
  - Input at the Gate
  - Output at the Source



# MOSFET CD Amplifier

$$R_{in} = \frac{v_i}{i_v} = \frac{v_i}{0} = \infty$$

	CD (MOSFET)
$A_{VO}$	$\frac{R_S g_m}{1 + g_m R_S}$
$A_V$   $R_L \neq \infty$	$\frac{g_m (R_S \parallel R_L)}{1 + g_m (R_S \parallel R_L)}$
$R_{in}$	$\infty \checkmark$
$R_O$	$R_S \parallel \frac{1}{g_m}$



Non inverting

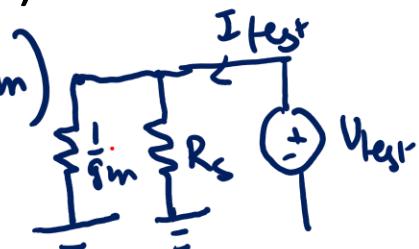
$$A_{V0} = \frac{v_0}{v_i} \Big|_{R_L=\infty} = \frac{j R_S}{j(R_S + \frac{1}{g_m})} = \frac{g_m R_S}{(g_m R_S + 1)} = \frac{g_m R_S}{1 + g_m R_S}$$

$R_{in}$  does not depend on the load (as it did for the BJT CC)

$R_O$  does not depend on the input

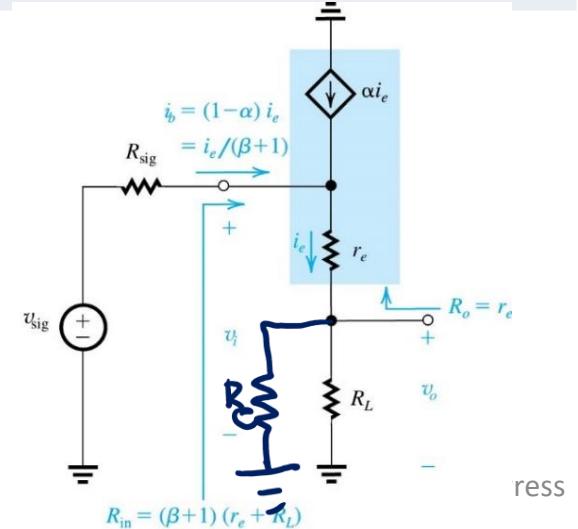
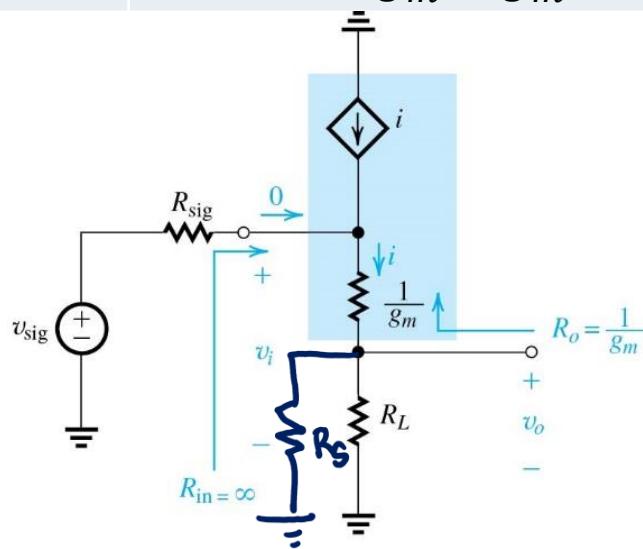
$$R_O = \frac{V_{test}}{I_{test}} \Big| = R_S \parallel \left(\frac{1}{g_m}\right)$$

all independent sources = 0



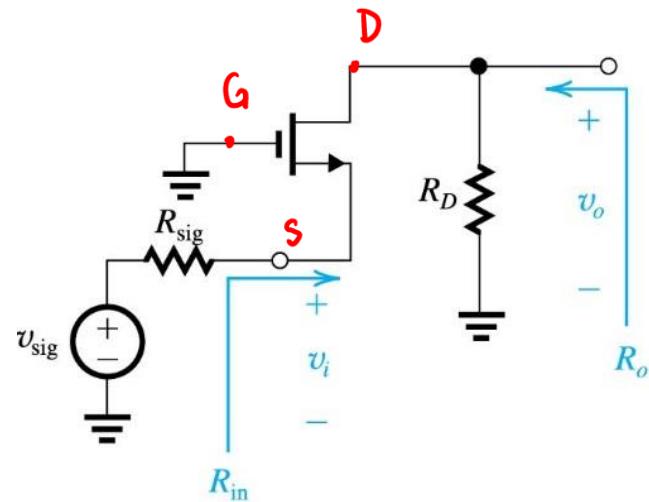
# MOSFET CD and BJT CC Amplifier Comparison

	CD (MOSFET)	CC (BJT)
$A_{VO}$	$\frac{R_S g_m}{1 + g_m R_S}$	$\frac{R_e g_m}{1 + g_m R_e}$
$A_V$	$\frac{g_m (R_S \parallel R_L)}{1 + g_m (R_S \parallel R_L)}$	$\frac{g_m (R_e \parallel R_L)}{1 + g_m (R_e \parallel R_L)}$
$R_{in}$	$\infty$	$r_\pi + (\beta + 1)(R_e \parallel R_L)$
$R_O$	$R_S \parallel \frac{1}{g_m} \approx \frac{1}{g_m}$	$r_e \approx r_e / (1 + R_e)$

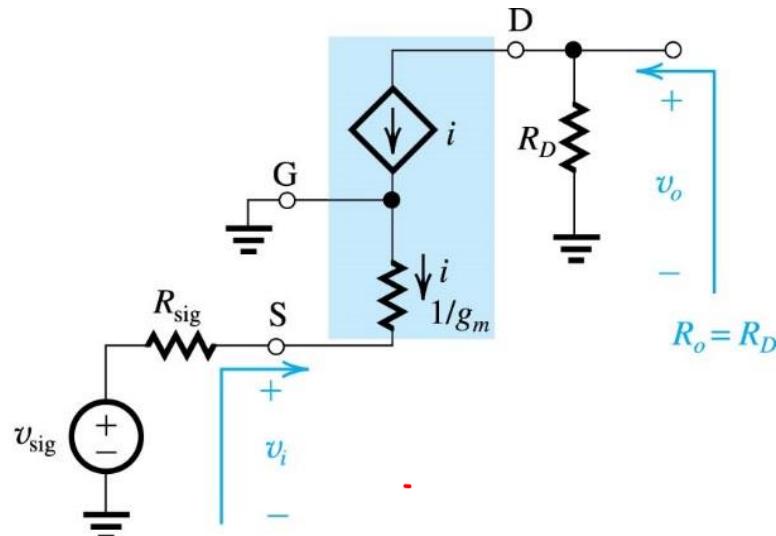


# MOSFET Common Gate (CG) Amplifier

- Common Gate (CG) Amplifier
  - Input at the source
  - Output at the Drain



(a)

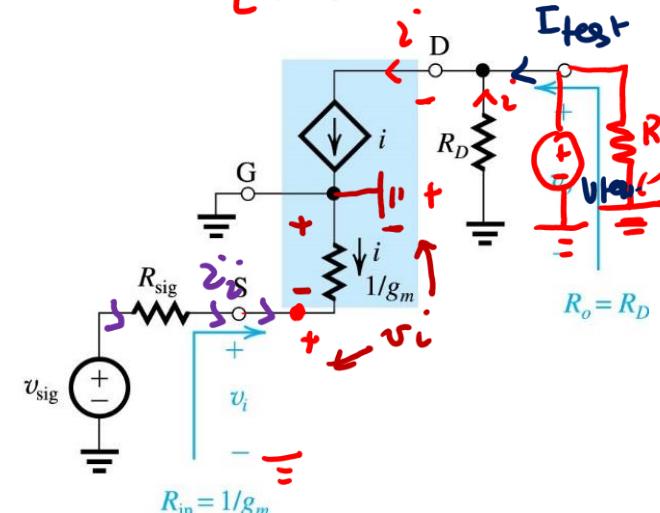


(b)

# MOSFET CG Amplifier

	CG (MOSFET)
$A_{VO}$	$g_m R_D$
$A_V$	$g_m (R_D \parallel R_L)$
$R_{in}$	$\frac{1}{g_m}$
$R_O$	$R_D$

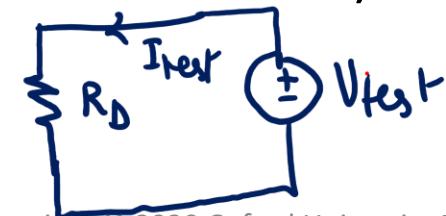
$$A_{VO} = \left. \frac{V_O}{V_i} \right|_{R_L = \infty} = \frac{-i R_D}{-i \frac{1}{g_m}} = g_m R_D$$



$$R_{in} = \frac{v_i}{i} = \frac{-i \left( \frac{1}{g_m} \right)}{(-i)}$$

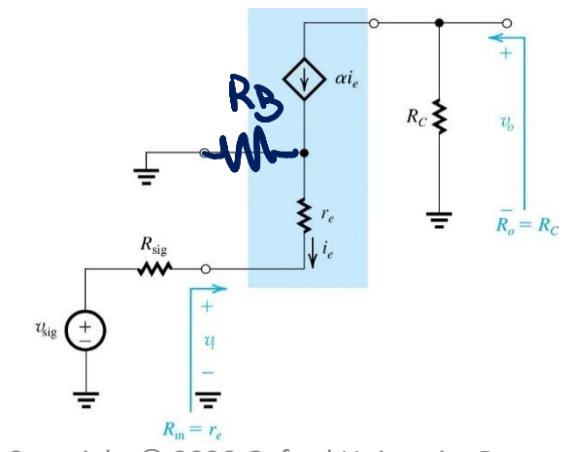
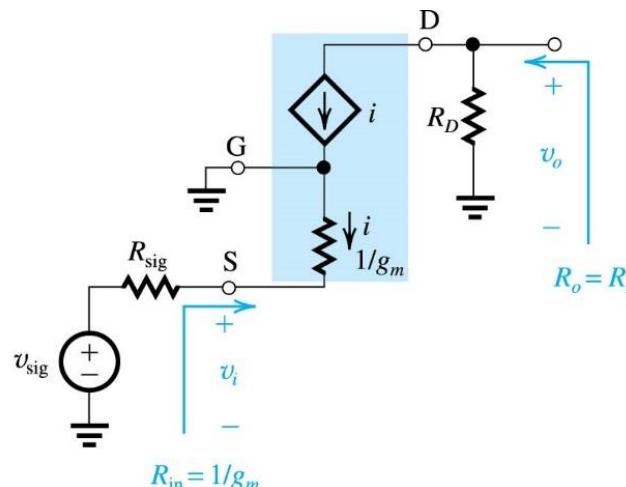
Low  $R_{in}$  - very limited applications (amplify high frequency signals, cables – match the input resistance of the amplifier to the cable)

$$R_O = \frac{V_{test}}{I_{test}} = R_D$$



# MOSFET CG and BJT CB Amplifier Comparison

	CG (MOSFET)	CB (BJT)
$A_{VO}$	$g_m R_D$	$\frac{g_m R_C}{1 + \frac{g_m R_B}{\beta}}$
$A_V$	$g_m (R_D \parallel R_L)$	$\frac{g_m (R_C \parallel R_L)}{1 + \frac{g_m R_B}{\beta}}$
$R_{in}$	$\frac{1}{g_m}$	$r_e + \frac{R_B}{\beta + 1}$
$R_O$	$R_D$	$R_C$



NMOS

# MOSFET Amplifier: Exercise

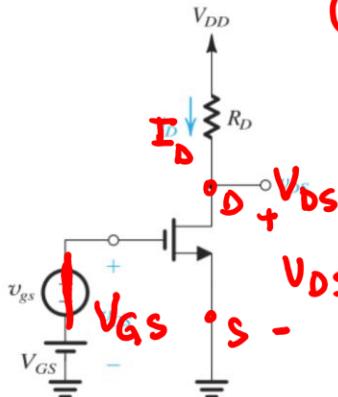
7.4

For the amplifier in Fig. 7.10, let  $V_{DD} = 5$  V,  $R_D = 10$  k $\Omega$ ,  $V_t = 1$  V,  $k'_n = 20 \mu\text{A}/\text{V}^2$ ,  $W/L = 20$ ,  $V_{GS} = 2$  V, and  $\lambda = 0$ . CLM: ignored ( $r_o = \infty$ )

- Find the dc current  $I_D$  and the dc voltage  $V_{DS}$ .
- Find  $g_m$ .
- Find the voltage gain.

(d) If  $v_{gs} = 0.2 \sin \omega t$  volts, find  $v_{ds}$  assuming that the small-signal approximation holds. What are the minimum and maximum values of  $v_{DS}$ ?

@  $V_{GS} = 2$  V > ( $V_t = 1$  V)  $\rightarrow$  MOSFET is ON



Assuming Saturation region operation

$$I_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (V_{GS} - V_t)^2$$

$$I_D = \frac{1}{2} 20 \text{ mA/V}^2 (20) (2-1)^2 = 200 \text{ mA} = 0.2 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 5 - [0.2 \text{ mA} \times 10 \text{ k}\Omega] = 3 \text{ V} \geq (V_{OV})$$

$$V_{DS} \geq V_{OV}$$

$$V_{GD} \leq V_{tn}$$

(b)  $g_m = k_n V_{OV} = k'_n \left( \frac{W}{L} \right) V_{OV}$

$$= 20 \text{ mA/V}^2 (20) (1) = \frac{400}{1000} = 0.4 \text{ mA/V}$$

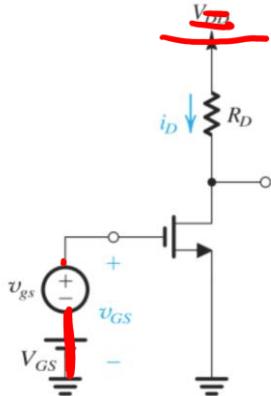
$$V_{OV} = V_{GS} - V_t = 2 - 1 = 1 \text{ V}$$

Saturation region operation confirmed

# MOSFET Amplifier: Exercise

- 7.4 For the amplifier in Fig. 7.10, let  $V_{DD} = 5$  V,  $R_D = 10$  k $\Omega$ ,  $V_t = 1$  V,  $k'_n = 20 \mu\text{A}/\text{V}^2$ ,  $W/L = 20$ ,  $V_{GS} = 2$  V, and  $\lambda = 0$ .
- Find the dc current  $I_D$  and the dc voltage  $V_{DS}$ .
  - Find  $g_m$ .
  - Find the voltage gain.
  - If  $v_{gs} = 0.2 \sin \omega t$  volts, find  $v_{ds}$  assuming that the small-signal approximation holds. What are the minimum and maximum values of  $v_{DS}$ ?

AC circuit



(c)

derived (slides #16 to 18)

$$A_{VO} = \frac{v_o}{v_{gs}} = -g_m R_D = -0.4 \frac{\text{mA/V}}{\text{V}} \times 10^3 \text{K} = -4 \frac{\text{V/V}}{\text{V}}$$

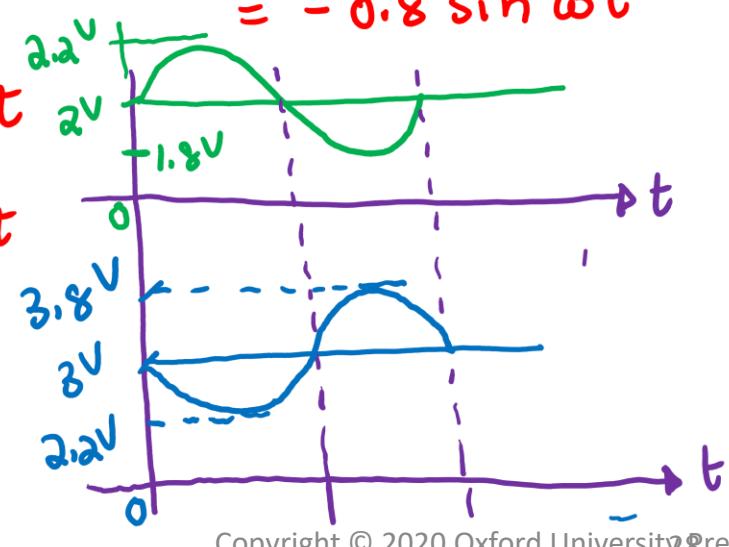
(d)

$$v_{gs} = 0.2 \sin \omega t$$

$$v_{ds} = v_o \Rightarrow \frac{v_{ds}}{v_{gs}} = -4 \Rightarrow v_{ds} = -4 [0.2 \sin \omega t] = -0.8 \sin \omega t$$

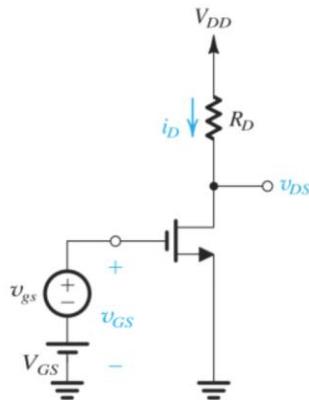
$$v_{gs} = V_{GS} + v_{gs} = 2 + 0.2 \sin \omega t$$

$$v_{ds} = V_{DS} + v_{ds} = 3 - 0.8 \sin \omega t$$



# MOSFET Amplifier: Exercise

- 7.4 For the amplifier in Fig. 7.10, let  $V_{DD} = 5$  V,  $R_D = 10$  k $\Omega$ ,  $V_t = 1$  V,  $k'_n = 20$   $\mu\text{A}/\text{V}^2$ ,  $W/L = 20$ ,  $V_{GS} = 2$  V, and  $\lambda = 0$ .
- Find the dc current  $I_D$  and the dc voltage  $V_{DS}$ .
  - Find  $g_m$ .
  - Find the voltage gain.
  - If  $v_{gs} = 0.2 \sin \omega t$  volts, find  $v_{ds}$  assuming that the small-signal approximation holds. What are the minimum and maximum values of  $v_{ds}$ ?



# MOSFET Amplifier: Exercise

7.8

A PMOS transistor has  $V_t = -1$  V,  $k'_p = 60 \mu\text{A/V}^2$ , and  $W/L = 16 \mu\text{m}/0.8 \mu\text{m}$ . Find  $I_D$  and  $g_m$  when the device is biased at  $V_{GS} = -1.6$  V. Also, find the value of  $r_o$  if  $\lambda$  (at  $L = 1 \mu\text{m}$ ) =  $-0.04 \text{ V}^{-1}$ .

$|V_{GS}| = 1.6 \text{ V} > |V_t| = 1 \text{ V}$  → MOSFET IS ON

Assuming Saturation mode of operation

$$I_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) V_{GS}^2 = \frac{1}{2} \times 60 \frac{\text{mA/V}^2}{\mu\text{m}} \times \left( \frac{16}{0.8} \right) (0.6)^2 = 216 \text{ mA} = 0.216 \text{ mA}$$

$$V_{DS} = |V_{GS}| - |V_{tp}| = 1.6 - 1 = 0.6 \text{ V}$$

$$g_m = k'_p V_{DS} = k'_p \left( \frac{W}{L} \right) V_{DS} = 60 \frac{\text{mA/V}^2}{\mu\text{m}} \times \left( \frac{16}{0.8} \right) \times 0.6 = 0.72 \text{ mA/V}$$

$$g_m = \frac{2 I_D}{V_{DS}}$$

$$r_o = \frac{|V_A|}{I_D} = \frac{1}{|\lambda| I_D}$$

$$r_o = \frac{1}{0.05 \times 0.216 \text{ mA}} = 92.59 \text{ k}\Omega$$

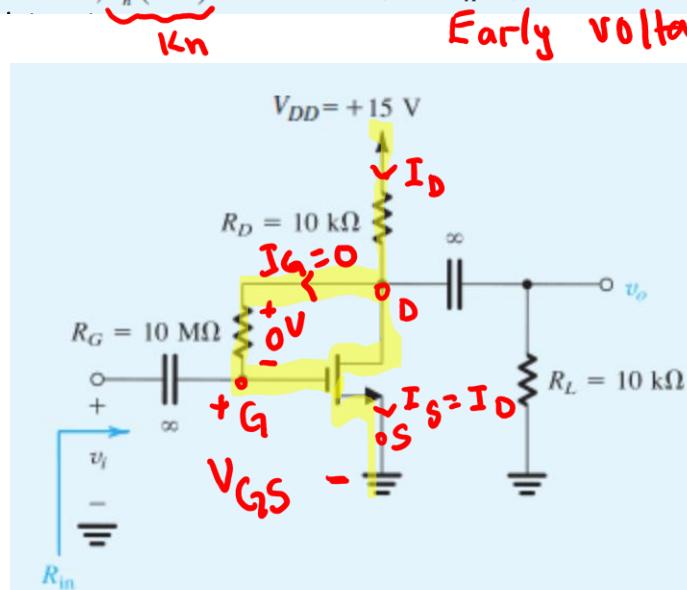
$$|\lambda| = 0.04 @ L = 1 \mu\text{m}$$

$$|\lambda| = \frac{0.04}{1} \times 0.8 = 0.032$$

$$@ L = 0.8 \mu\text{m}$$

# Example 7.3 MOSFET Amplifier: Exercise

Figure 7.16(a) shows a discrete MOSFET amplifier biased with a drain-to-gate resistance  $R_G$ . We will study this biasing arrangement in Section 7.4. The input signal  $v_i$  is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance  $R_L$  via another large capacitor. We want to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has  $V_t = 1.5 \text{ V}$ ,  $k'_n (W/L) = 0.25 \text{ mA/V}^2$ , and  $V_A = 50 \text{ V}$ . Assume that the coupling capacitors are large enough that they act as short circuits at the signal frequencies.



Early voltage [ $r_0 \neq \infty$ ,  $r_0$  will have a finite value]

DC circuit < caps are open  
ac sources  $\rightarrow$  OFF

$$V_D = V_G \Rightarrow V_{GD} = V_G - V_D = 0 \leq [V_t = 1.5]$$

Saturation mode operation

$$I_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (V_{GS} - V_t)^2$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} \Rightarrow V_{DS} = V_{DD} - I_D R_D = V_{GS}$$

$$I_D = \frac{1}{2} 0.25 [15 - I_D 10 - 1.5]^2 = \frac{1}{2} 0.25 [13.5 - 10 I_D]^2$$

$$I_D = \frac{1}{2} 0.25 [13.5^2 + 100 I_D^2 - 270 I_D]$$

$$I_D^2 - 2.78 I_D + 1.8224 = 0$$

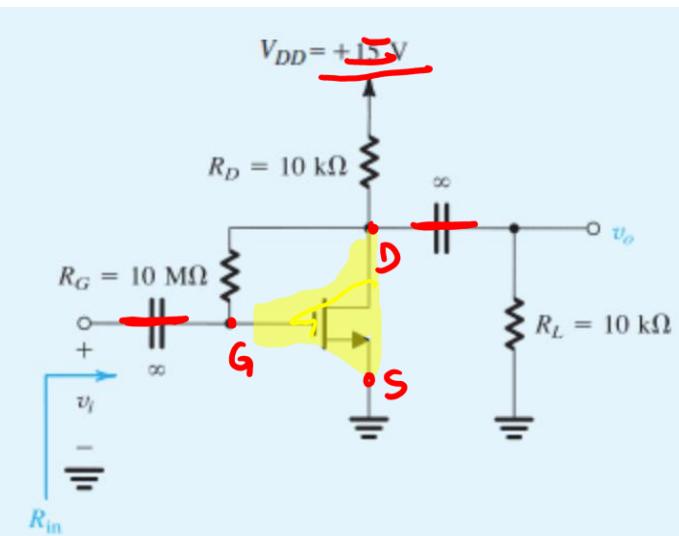
$I_D = 1.72 \text{ mA} \rightarrow V_{DS} = 15 - (1.72 \times 10) = -2.2 \text{ V}$

$V_{DS} > V_{OV}$

$I_D = 1.06 \text{ mA} \rightarrow V_{DS} = 15 - (1.06 \times 10) = 4.4 \text{ V}$

$V_{OV} = 4.4 - 1.5 = 2.9 \text{ V}$

# MOSFET Amplifier: Exercise



$$g_m = k_n V_{DS}$$

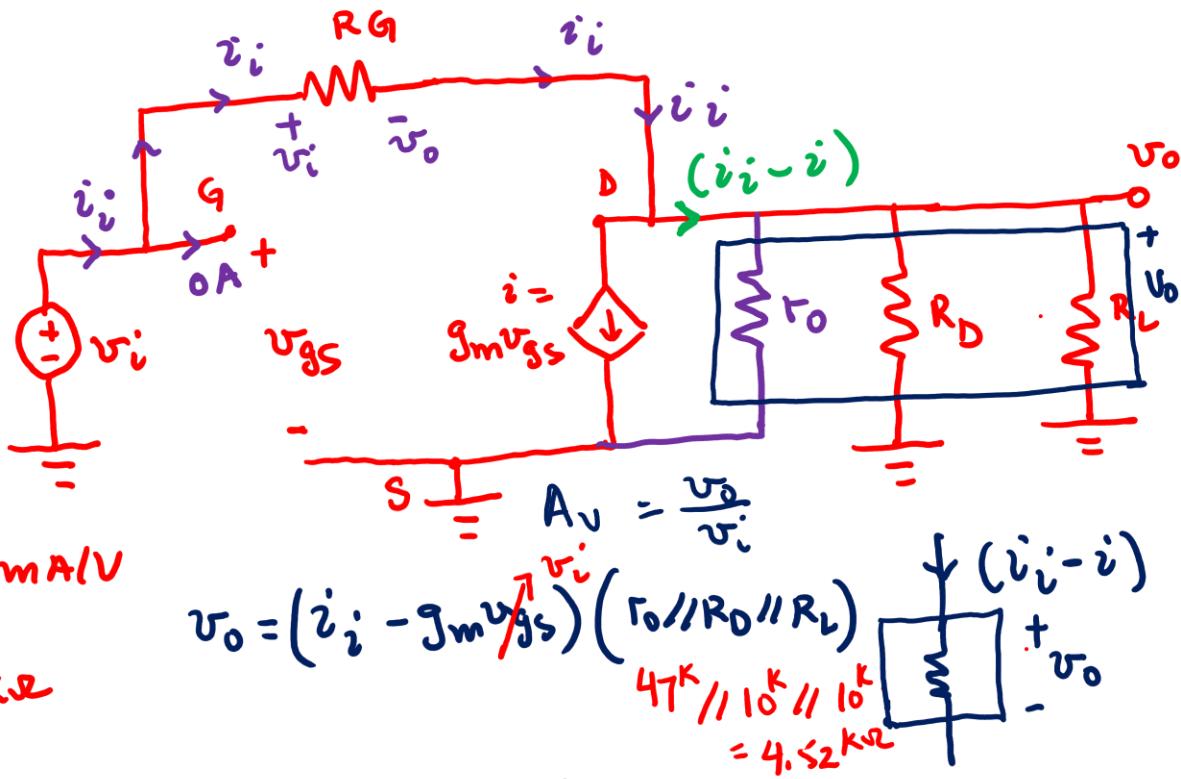
$$= k_n' \left( \frac{W}{L} \right) V_{DS}$$

$$= 0.125 \times 2.9 = 0.725 \text{ mA/V}$$

$$r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega$$

$$\frac{v_o}{v_i} = -3.3 \text{ V/V}$$

AC circuit Analysis *turn off DC sources  
caps → short*



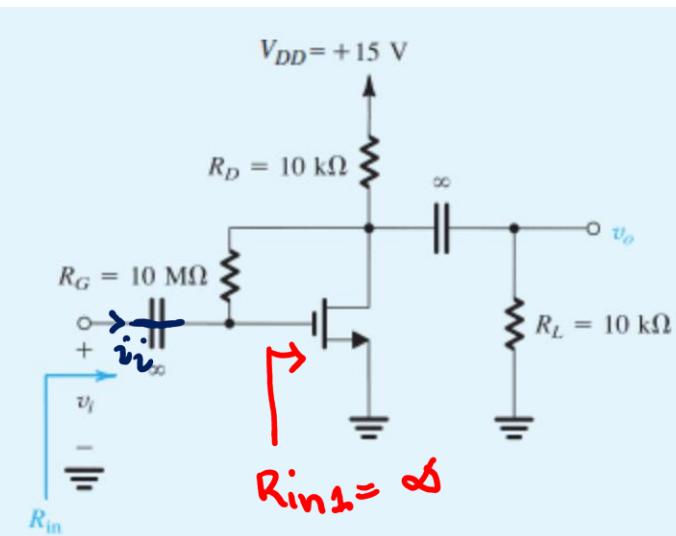
$$v_o = (i_i - g_m v_i) (4.52)$$

$$i_i = \frac{v_i - v_o}{R_G}$$

$$v_o = \left[ \frac{v_i - v_o}{R_G} - \frac{v_{DS}}{g_m} \right] (4.52)$$

$10000 \text{ k}\Omega$

# MOSFET Amplifier: Exercise



$$R_{in} = \frac{v_i}{i_i}$$

$$i_i = \frac{v_i - v_o}{R_G}$$

$$A_v = \frac{v_o}{v_i} = -3.3 \text{ V/V} \Rightarrow v_o = -3.3 v_i$$

$$i_i = \frac{v_i + 3.3 v_i}{R_G} = \frac{(1+3.3) v_i}{R_G}$$

$$\frac{v_i}{i_i} = R_{in} = \frac{R_G}{(1+3.3)} = \frac{10 \text{ M}\Omega}{4.3}$$

$$R_{in} = 2325.58 \text{ k}\Omega$$

$$R_{in} = 2.33 \text{ M}\Omega$$

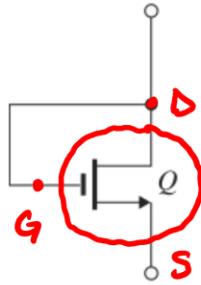
# MOSFET Amplifier: Exercise

Exercise (pg → 396)

Early effect  
is not ignored

- 7.11 Use the T model of Fig. 7.18(b) to show that a MOSFET whose drain is connected to its gate exhibits an incremental resistance equal to  $[(1/g_m) \parallel r_o]$ .

NMOS



Thevenin's Theorem

$$R_U = \frac{U_{test}}{I_{test}}$$

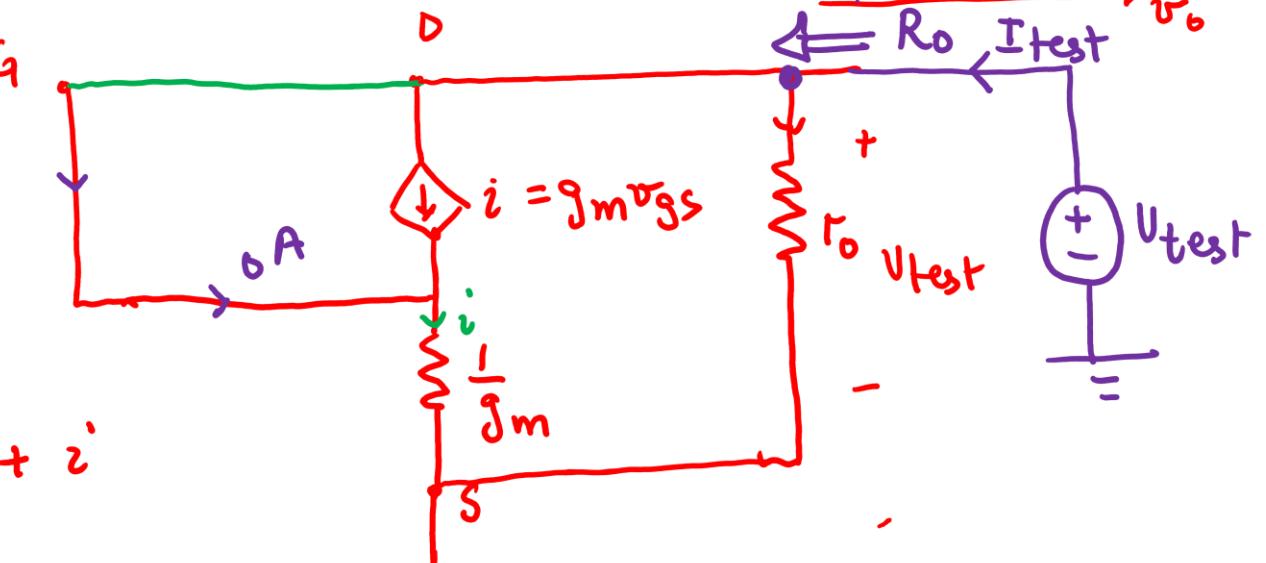
$$KCL \Rightarrow I_{test} = \frac{U_{test}}{r_o} + i$$

$$= \frac{U_{test}}{r_o} + g_m v_{gs}$$

$$I_{test} = \frac{U_{test}}{r_o} + g_m V_{test} = \left[ \frac{1}{r_o} + g_m \right] U_{test}$$

$$R_o = \frac{U_{test}}{I_{test}} = \frac{1}{\frac{1}{r_o} + g_m} =$$

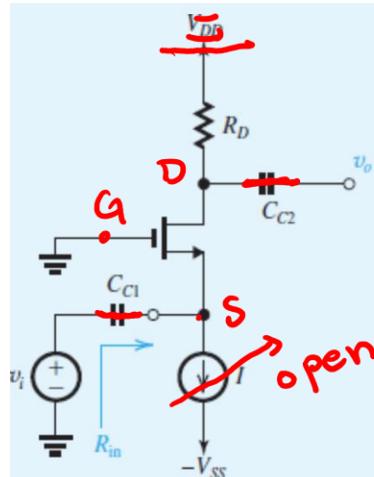
$$= r_o \parallel \left( \frac{1}{g_m} \right)$$



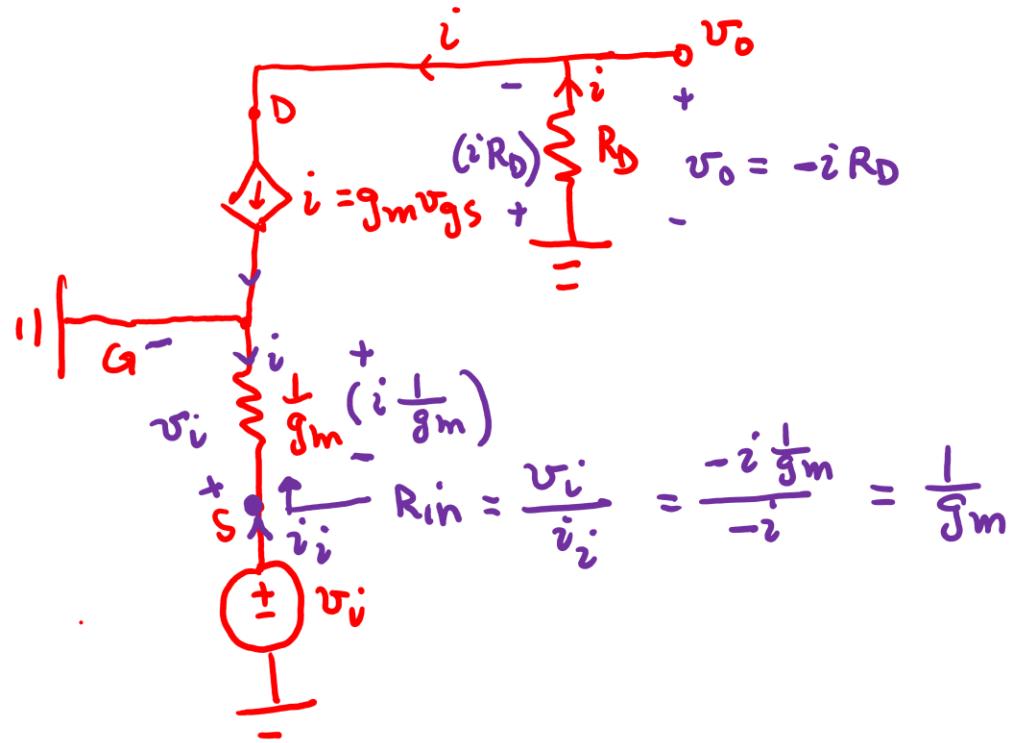
# Example 7.4 MOSFET Amplifier: Exercise

NMOS CG amp.

Figure 7.19(a) shows a MOSFET amplifier biased by a constant-current source  $I$ . Assume that the values of  $I$  and  $R_D$  are such that the MOSFET operates in the saturation region. The input signal  $v_i$  is coupled to the source terminal by a large capacitor  $C_{C1}$ . Similarly, the output signal at the drain is taken through a large coupling capacitor  $C_{C2}$ . Find the input resistance  $R_{in}$  and the voltage gain  $v_o/v_i$ . Neglect channel-length modulation.  $r_0 \rightarrow \infty$



AC Circuit < DC SOURCES OFF  
Caps are short



$$A_{v_o} = g_m R_D$$

Slides 24, 25

# IC Biasing – Current Sources and Current Mirrors

Constant Current Source is generated at one location in an IC chip and is then replicated at various other locations for biasing the various amplifier stages through – CURRENT STEERING

$Q_1 \rightarrow \text{NMOS} \rightarrow \text{Drain } 'G' \text{ Gate are connected together}$

$$V_{GD} \leq V_{tn} \Rightarrow V_G - V_D = 0 \leq V_{tn} \text{ (0.3 to 3V)}$$

$Q_1 \rightarrow \text{saturation region operation confirmed}$

$$I_{D1} = \frac{1}{2} k_n \left( \frac{w}{L} \right), (V_{GS1} - V_{tn})^2$$

$Q_2 \rightarrow \text{NMOS} \rightarrow V_{GS2} = V_{GS1} = V_{GS}$

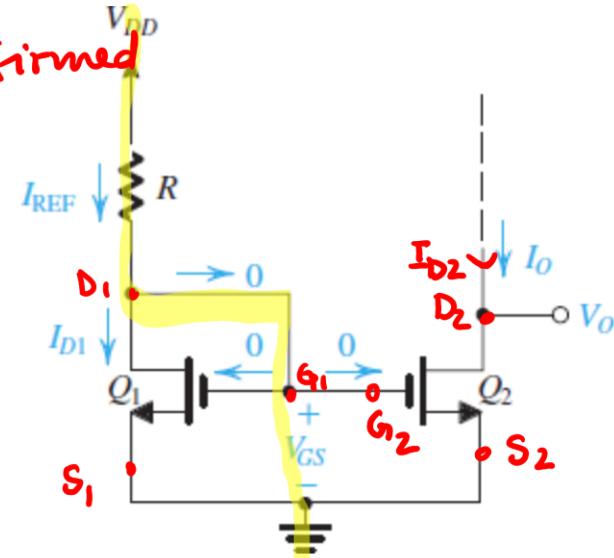
KVL  $\rightarrow$  highlighted path

$$-V_{DD} + I_{REF} R + V_{GS} = 0$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

$$I_{D2} = I_o = \frac{1}{2} k_n \left( \frac{w}{L} \right)_2 (V_{GS} - V_{tn})^2$$

$$\frac{I_o}{I_{REF}} = \frac{I_{D2}}{I_{D1}} = \frac{\frac{1}{2} k_n \left( \frac{w}{L} \right)_2 (V_{GS} - V_{tn})^2}{\frac{1}{2} k_n \left( \frac{w}{L} \right)_1 (V_{GS} - V_{tn})^2} =$$



current Mirror

$$I_o = I_{REF}$$

$$\frac{\left( \frac{w}{L} \right)_2}{\left( \frac{w}{L} \right)_1}$$

# MOS Current Mirror

$I_{REF} \rightarrow$  i/p reference current is supplied by a current source

Source

$$\frac{I_o}{I_{REF}} = \frac{\left(\frac{w}{l}\right)_2}{\left(\frac{w}{l}\right)_1}$$

$Q_2 \rightarrow$  saturation mode (has to be)

$$V_{DS2} \geq V_{OU2} \Rightarrow V_{DS2} \geq (V_{GS} - V_{th})$$

$$V_o \geq V_{OU2}$$

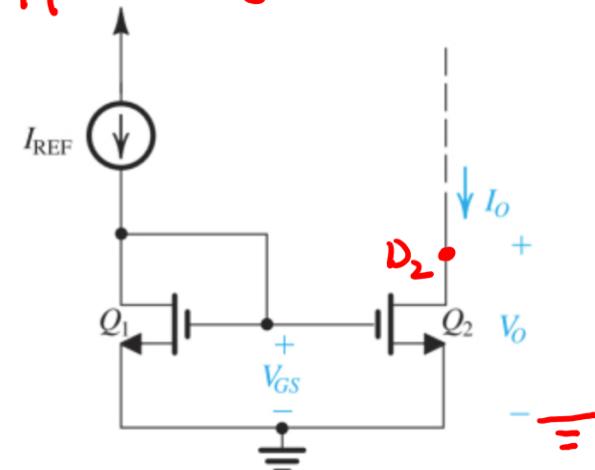
O/p resistance,  $r_o \rightarrow$  cannot be ignored

$$I_o = I_{REF} \quad [V_o = V_{GS}]$$

$$I_{REF} = \frac{1}{2} k_n \left(\frac{w}{l}\right) V_{OU}^2 (1 + \lambda V_{DS1})$$

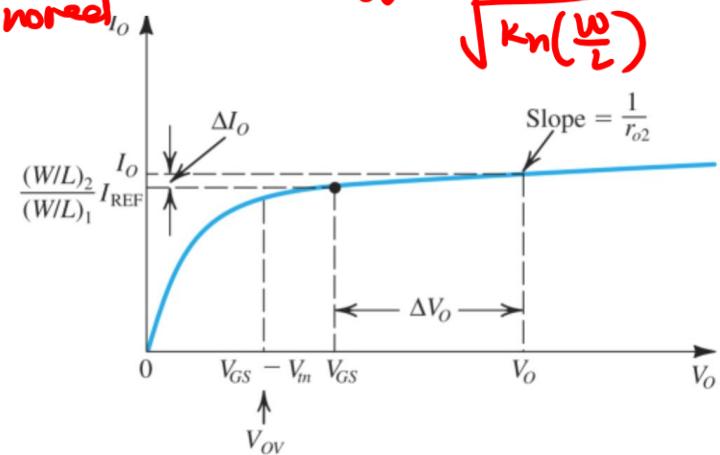
$$I_o = \frac{1}{2} k_n \left(\frac{w}{l}\right)_2 V_{OU}^2 (1 + \lambda V_o)$$

$$\frac{I_o}{I_{REF}} = \frac{\left(\frac{w}{l}\right)_2 (1 + \lambda V_o)}{\left(\frac{w}{l}\right)_1 (1 + \lambda V_{DS1})}$$



$$I_o = \frac{1}{2} k_n \left(\frac{w}{l}\right) V_{OU}^2$$

$$V_{OU} = \sqrt{\frac{2 I_o}{k_n \left(\frac{w}{l}\right)}}$$



# MOS Current Mirror – Example 8.1

Given  $V_{DD} = 3$  V and using  $I_{REF} = 100 \mu\text{A}$ , design the circuit of Fig. 8.1 to obtain an output current whose nominal value is  $100 \mu\text{A}$ . Find  $R$  if  $Q_1$  and  $Q_2$  are matched and have channel lengths of  $1 \mu\text{m}$ , channel widths of  $10 \mu\text{m}$ ,  $V_t = 0.7$  V, and  $k'_n = 200 \mu\text{A/V}^2$ . What is the lowest possible value of  $V_O$ ? Assuming that for this process technology, the Early voltage  $V'_A = 20 \text{ V}/\mu\text{m}$ , find the output resistance of the current source. Also, find the change in output current resulting from a  $+1\text{-V}$  change in  $V_O$ .

$$\textcircled{1} \quad R \Rightarrow$$

$$I_{D1} = \frac{1}{2} k_n' \left( \frac{w}{L} \right) (V_{GS} - V_{tn})^2$$

$$100 \mu\text{A} = \frac{1}{2} 200 \frac{\mu\text{A/V}^2}{\mu\text{m}} \left( \frac{10}{1} \right) (V_{GS} - 0.7)^2$$

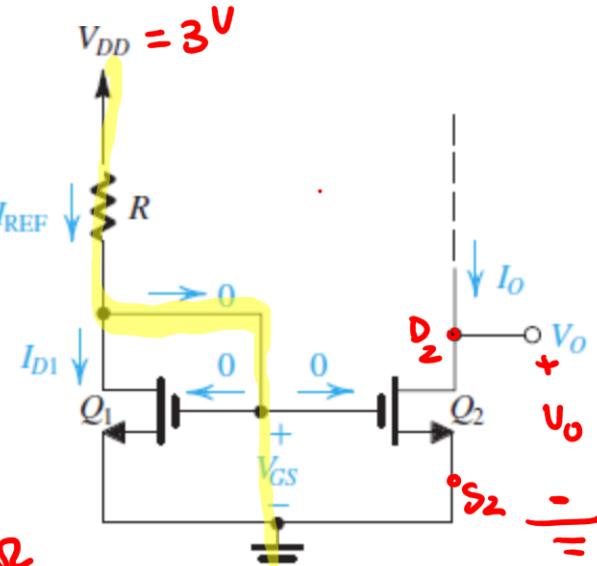
$$V_{GS} - 0.7 = \sqrt{\frac{2 \times 100}{200 \times 10}} \Rightarrow V_{GS} = 1 \text{ V}$$

$$\text{KVL} \Rightarrow -3 \text{ V} + R (100 \mu\text{A}) + 1 = 0 \Rightarrow R = 20 \text{ k}\Omega$$

$$\textcircled{2} \quad V_o = V_{DS2} \geq V_{OVA}$$

$$V_{OVA} = V_{GSA} - V_{tn} = V_{GS} - V_{tn} = 1 - 0.7 = 0.3 \text{ V}$$

$$V_{O,min} = 0.3 \text{ V}$$



# MOS Current Mirror – Example 8.1

Given  $V_{DD} = 3$  V and using  $I_{REF} = 100 \mu\text{A}$ , design the circuit of Fig. 8.1 to obtain an output current whose nominal value is  $100 \mu\text{A}$ . Find  $R$  if  $Q_1$  and  $Q_2$  are matched and have channel lengths of  $1 \mu\text{m}$ , channel widths of  $10 \mu\text{m}$ ,  $V_t = 0.7$  V, and  $k'_n = 200 \mu\text{A/V}^2$ . What is the lowest possible value of  $V_o$ ? Assuming that for this process technology, the Early voltage  $V'_A = 20 \text{ V}/\mu\text{m}$ , find the output resistance of the current source. Also, find the change in output current resulting from a  $+1\text{-V}$  change in  $V_o$ .

$$(3) \quad r_o = \frac{V_A}{I_D} = \frac{V_{A2}}{I_{D2}} = \frac{V_{A2}}{I_o}$$

$$r_o = \frac{20 \times 1}{100 \mu\text{A}} = -0.2 \text{ M}\Omega$$

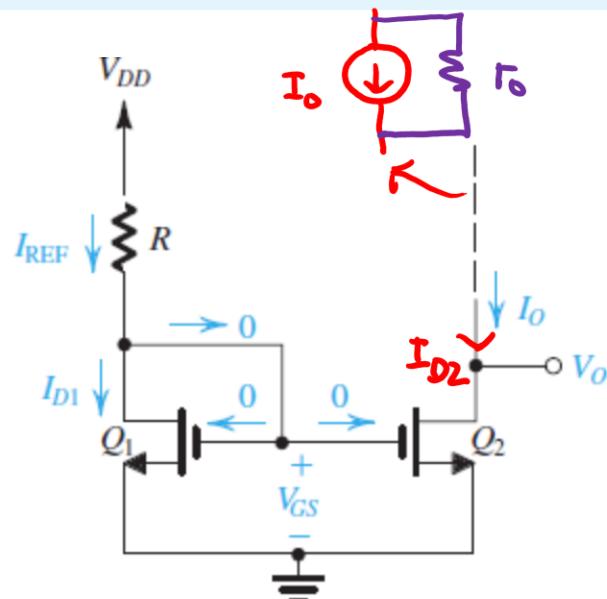
(4) Ohm's law

$$\boxed{V = IR}$$

$$\Delta I = \frac{\Delta V}{r_o} \Rightarrow \Delta I = \frac{1 \text{ V}}{0.2 \text{ M}} = 5 \text{ mA}$$

$$\text{if } V_o = V_{GS} = 1 \text{ V} \quad I_o = I_{REF} = 100 \mu\text{A}$$

$$\text{if } V_o = 2 \text{ V} ; I_o = 100 + 5 = 105 \text{ mA}$$



# Current Steering Circuits

Once a Constant Current has been generated, it can be replicated at various other locations to provide a DC bias for the various amplifier stages in an IC – CURRENT STEERING

$Q_1 \rightarrow$  Saturation region operation + designed value for R  
 $\Downarrow$

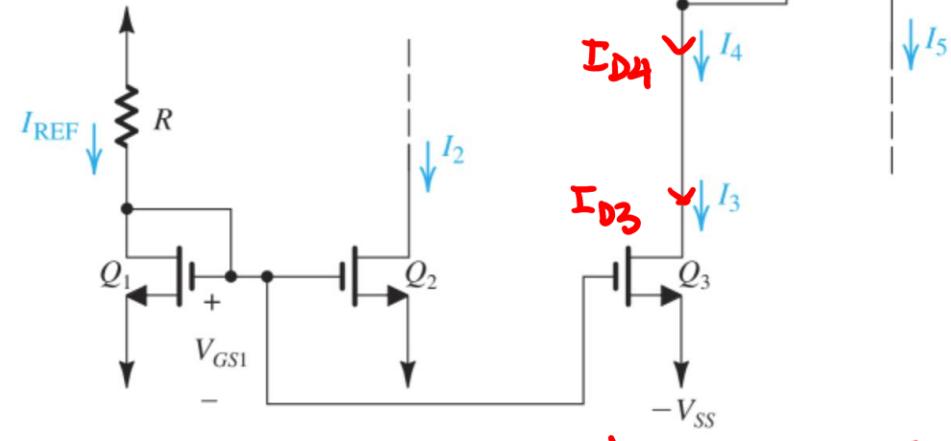
$$I_{REF}$$

$Q_1, Q_2 \rightarrow$  current mirror

$Q_1, Q_3 \rightarrow$  current mirror

$$I_2 = I_{REF} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

$$I_3 = I_{REF} \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1}$$



if  $Q_1, Q_2$  and  $Q_3$  are matched  $\Rightarrow I_2 = I_3 = I_{REF}$

$$I_4 = I_3$$

$Q_4$  and  $Q_5 \rightarrow$  current mirror

$$I_5 = I_4 \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4} = I_3 \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}$$

$$= I_{REF} \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} \times \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}$$

# Current Steering Circuits

Once a Constant Current has been generated, it can be replicated at various other locations to provide a DC bias for the various amplifier stages in an IC – CURRENT STEERING

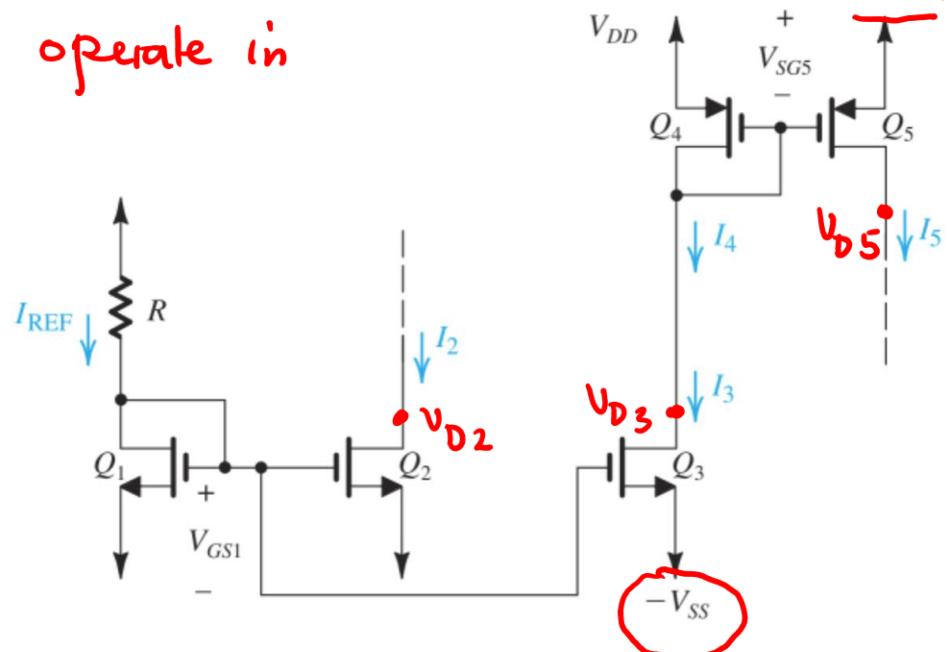
$Q_2$  and  $Q_3$  : What should be the voltage @ their drains to ensure that  $Q_2$  and  $Q_3$  operate in Saturation region

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{OU1}$$

$$\geq -V_{SS} + (V_{GS} - V_{th})$$

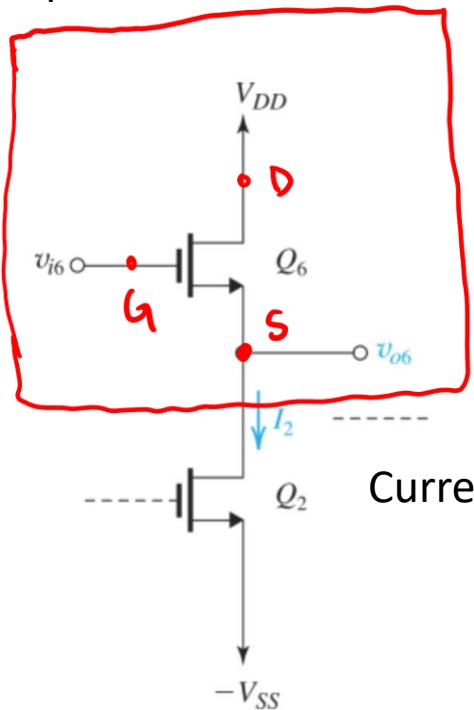
$Q_5$  : What should be the voltage @ its drain to ensure it operates in the . Saturation region

$$V_{D5} \leq V_{DD} - |V_{OU5}|$$



# Current Steering Circuits

The Constant Current  $I_2$  can be used to bias a Source follower amplifier



NMOS

i/p @ Gate :  $v_{i6}$

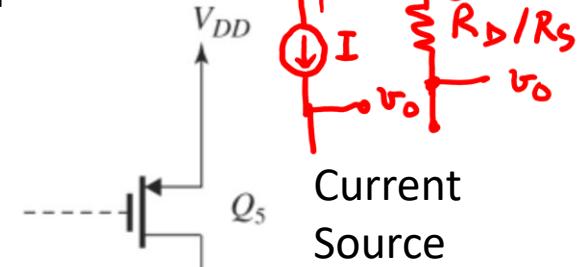
o/p @ Source :  $v_{o6}$

C D (Source follower)  
amplifier

$I_S$   
 $\downarrow I_2$

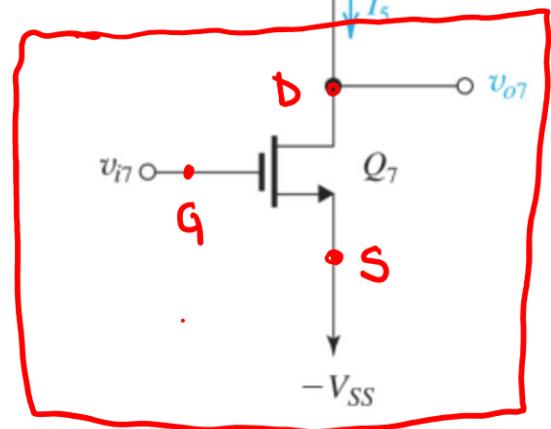
Current Sink

The Constant Current  $I_5$  can be used as the load for a common-Source amplifier



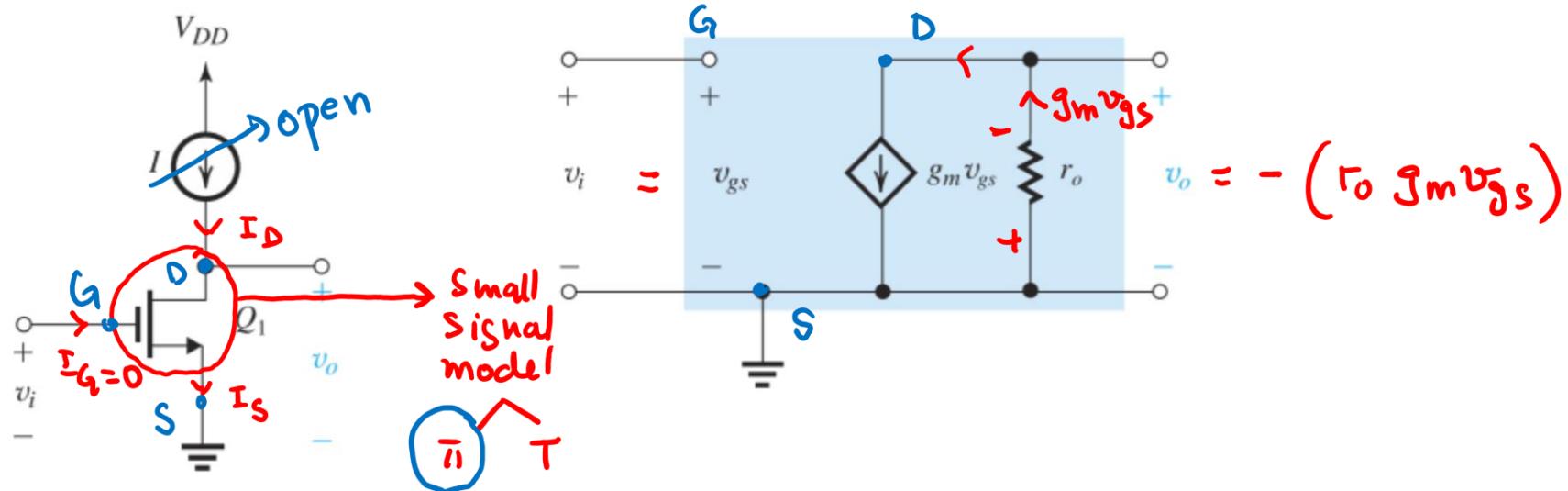
Current  
Source

i/P @ Gate  
o/P @ Drain  
CS amplifier



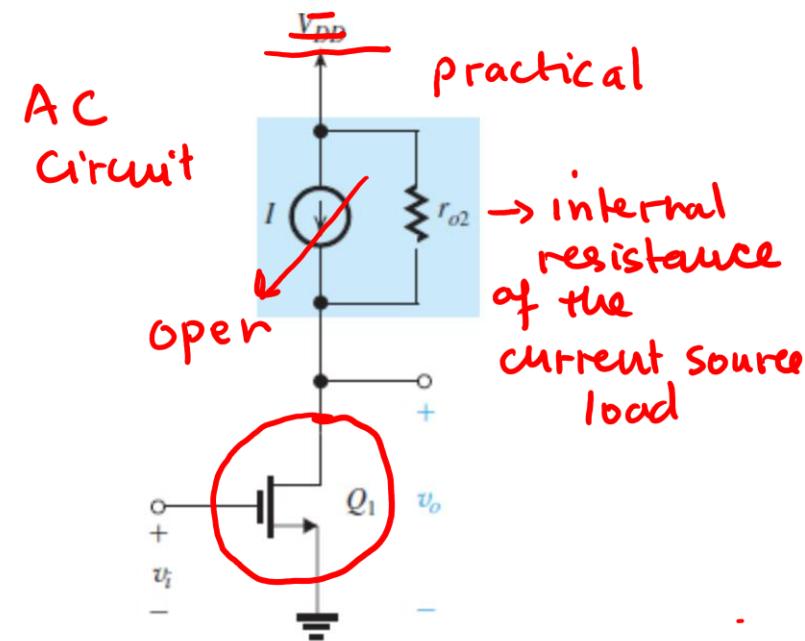
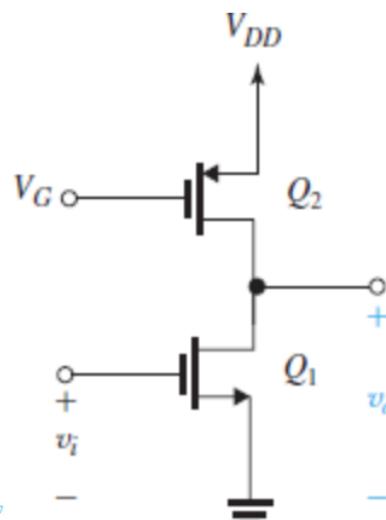
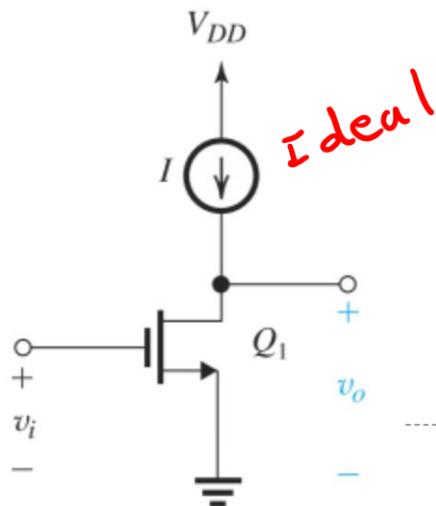
# Common Source (CS) Amplifier with Current Source Load

Ac circuit  $\rightarrow$  turn OFF all DC sources



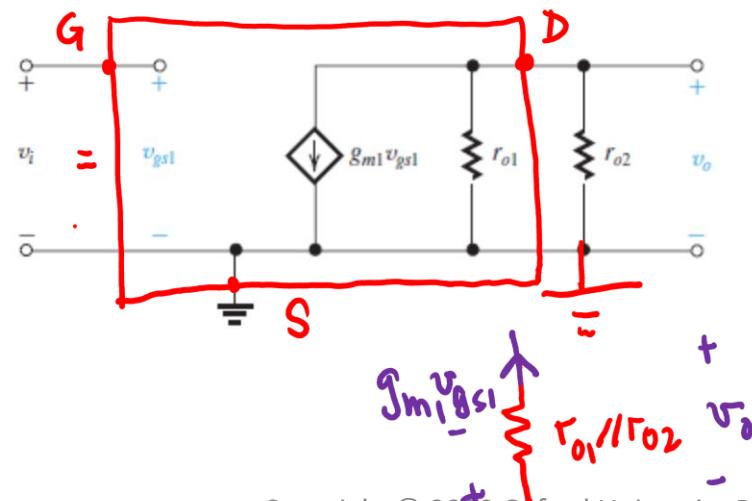
Voltage gain,  $A_{VO} = \frac{v_o}{v_i} = -\frac{\tau_0 g_m v_{GS}}{v_{GS}} = -g_m \tau_0$

# Current Source Load – Effect of Output Resistance



$$A_V = \frac{v_o}{v_i} = \frac{-g_{m1} v_{gs1} (\tau_{o1} // \tau_{o2})}{v_{gs1}}$$

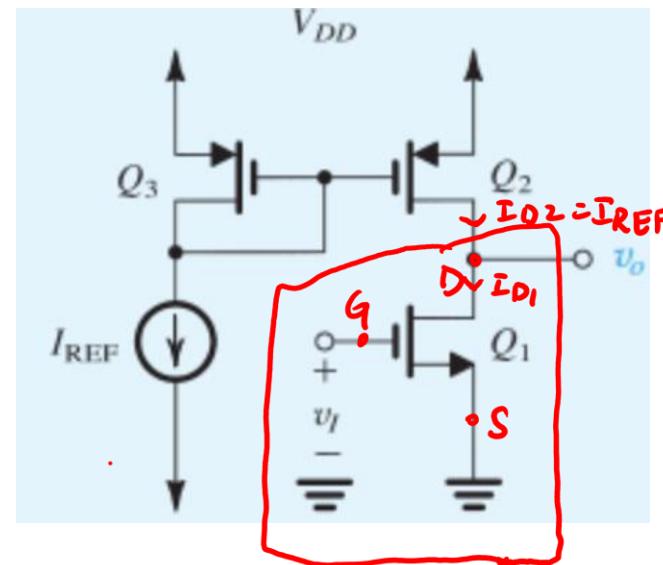
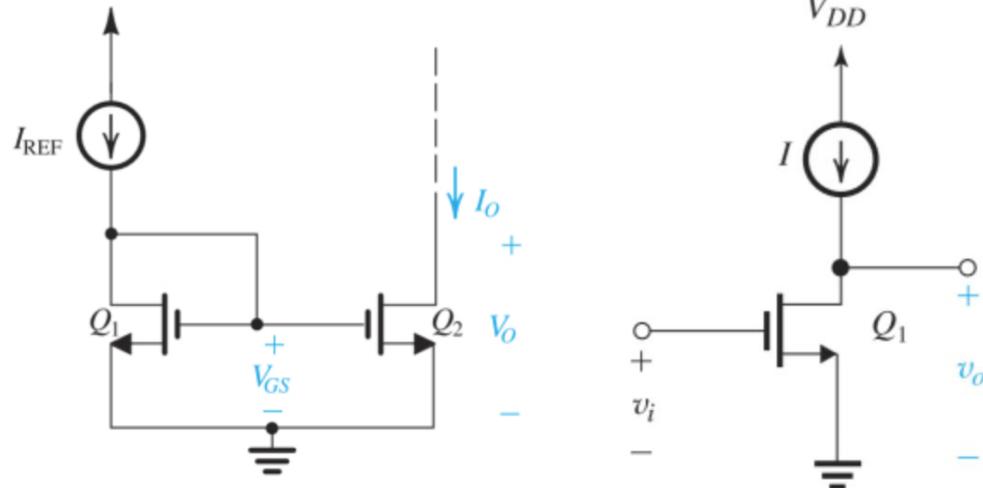
$$A_V = -g_{m1} (\tau_{o1} // \tau_{o2})$$



# CS Amplifier– Example 8.3

Let  $V_{DD} = 1.8$  V,  $V_{tn} = -V_{tp} = 0.5$  V,  $\mu_n C_{ox} = 4 \mu_p C_{ox} = 400 \text{ } \mu\text{A/V}^2$ ,  $|V_A| = 5$  V for all transistors, and  $I_{REF} = 100 \text{ } \mu\text{A}$ .

- (a) Find the dc component of  $v_I$  and the  $W/L$  ratios so that all transistors operate at  $|V_{OV}| = 0.2$  V.
  - (b) Determine the small-signal voltage gain.
  - (c) What is the allowable range of signal swing at the output for almost-linear operation?



# CS Amplifier – Example 8.3

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## DC Value of $U_C$

To operate Q<sub>1</sub> in saturation region

$$V_{O1} = V_{GS1} - V_{tn}$$

$$0.2 = V_I - 0.5 \Rightarrow V_I = 0.7$$

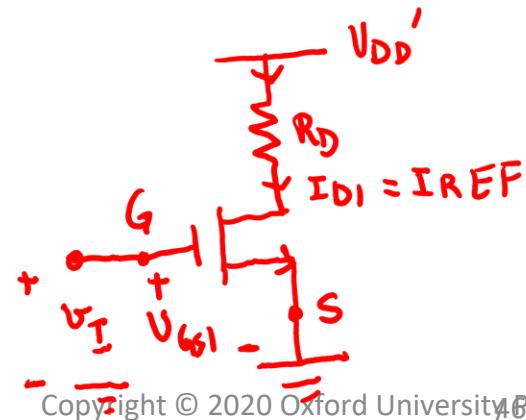
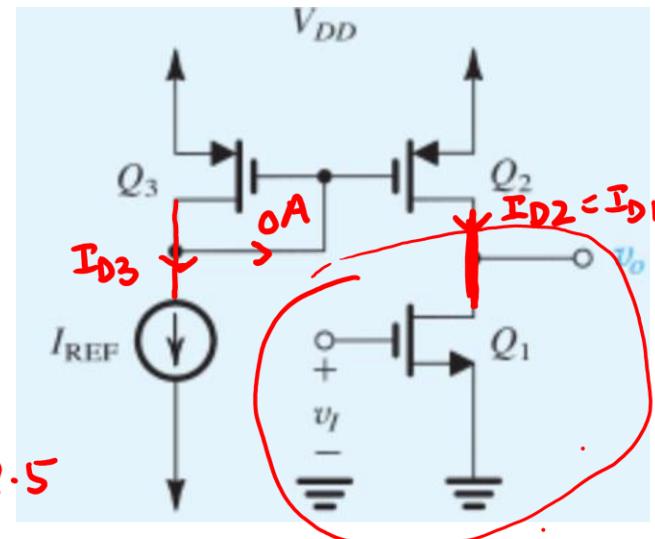
$$I_{D1} = \frac{1}{2} K_n' \left( \frac{\omega}{L} \right) V_{OU}^2$$

$$100^{\text{MA}} = \frac{1}{2} 400^{\text{HA/V2}} \left( \frac{w}{L} \right), 0.2^2 \Rightarrow \left( \frac{10}{L} \right),$$

$$I_{D2}, I_{D3} = \frac{1}{2} k_p' \left( \frac{w}{L} \right)_{2,3} 0.2^2$$

$$100^{MA} = \frac{1}{2} \left( \frac{400}{4} \right)^{MAU2} \left( \frac{w}{l} \right)_{2,3} 0.2^2$$

$$\left(\frac{W}{I}\right)_{2,3} = 50$$



# CS Amplifier– Example 8.3

Let  $V_{DD} = 1.8$  V,  $V_{tn} = -V_{tp} = 0.5$  V,  $\mu_n C_{ox} = 4 \mu_p C_{ox} = 400 \mu\text{A/V}^2$ ,  $|V_A| = 5$  V for all transistors, and  $I_{REF} = 100 \mu\text{A}$ .

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$$I_D = \frac{1}{2} k_n V_{OV}^2$$

slide #44 → derived an expression for the voltage gain

$$A_V = -g_m I \left( \Gamma_{O1} // \Gamma_{O2} \right)$$

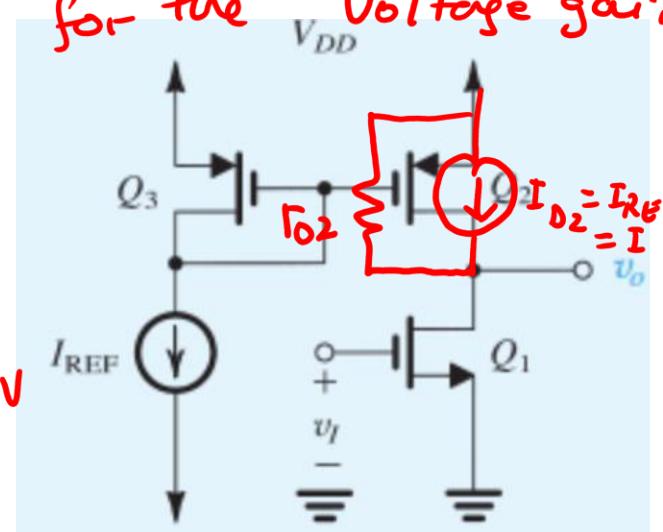
$$g_m = \frac{2 I_D}{V_{OV}} = k_n V_{OV} = k_n \left( \frac{W}{L} \right) V_{OV}$$

$$g_m = 400 \times 12.5 \times 0.2 \text{ mA/V} = 1000 \text{ mA/V} = 1 \text{ mA/V}$$

$$\Gamma_{O1} = \frac{V_{A1}}{I_{D1}} = \frac{5}{100 \text{ mA}} = \frac{5}{0.1 \text{ mA}} = 50 \text{ k}\Omega$$

$$\Gamma_{O2} = \frac{V_{A2}}{I_{D2}} = \frac{5}{100 \mu\text{A}} = 50 \text{ k}\Omega$$

$$A_V = -1 \left( 50 // 50 \right) = -25 \text{ V/V}$$



# CS Amplifier– Example 8.3

Let  $V_{DD} = 1.8$  V,  $V_{tn} = -V_{tp} = 0.5$  V,  $\mu_n C_{ox} = 4 \mu_p C_{ox} = 400 \mu\text{A/V}^2$ ,  $|V_A| = 5$  V for all transistors, and  $I_{REF} = 100 \mu\text{A}$ .

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NMOS  $\rightarrow Q_1$

$$v_{o,\max} ; v_{o,\min}$$

$$v_o \geq v_{ov1}$$

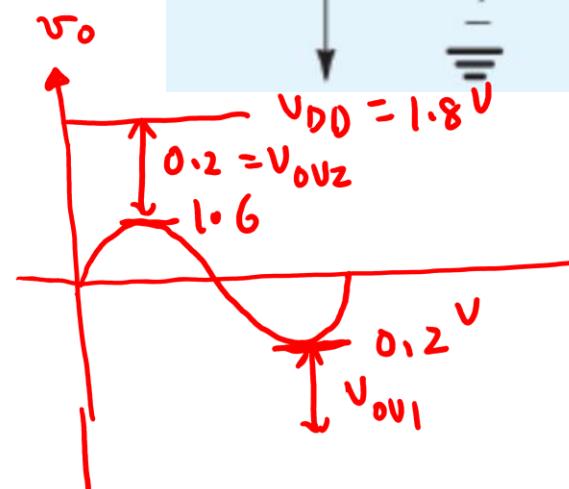
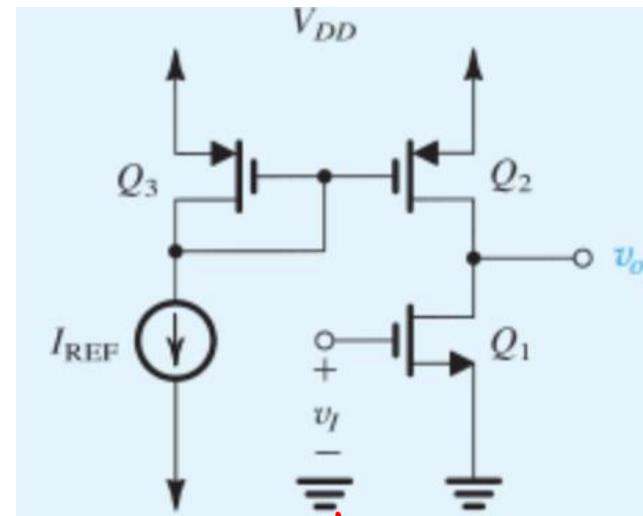
$$v_{o,\min} = v_{ov1} = 0.2 \text{ V}$$

$$v_{o,\max} = V_{DD} - |v_{ova1}|$$

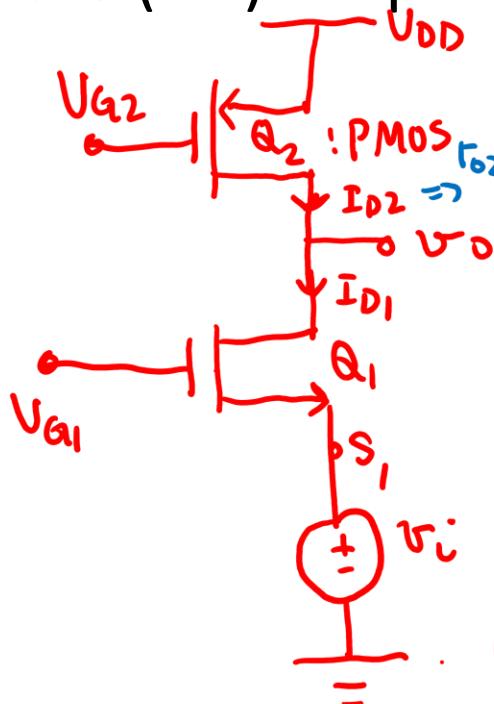
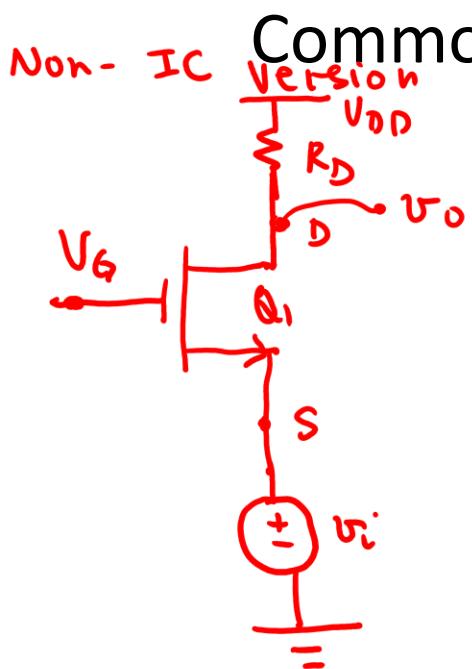
$$= 1.8 - 0.2 = 1.6 \text{ V}$$

$$0.2 \leq v_o \leq 1.6 \text{ V}$$

Slide 41



# Common Gate (CG) Amplifier (IC Version)



Voltage gain =  $A_V = \frac{V_O}{V_i}$

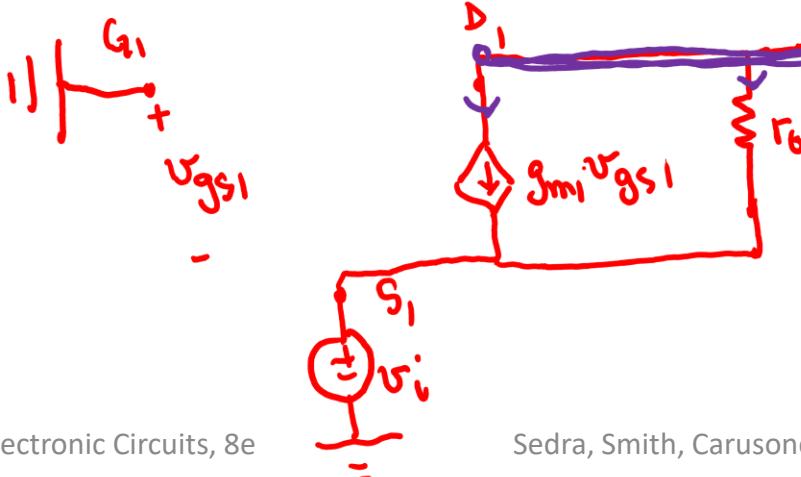
$v_i = -v_{gs1}$

KCL @ node D<sub>1</sub>:

$$g_m v_{gs1} + \frac{v_o - v_i}{r_{o1}} + \frac{v_o - 0}{r_{o2}} = 0$$

$$A_V = \frac{v_o}{v_i} = g_m (r_{o1} // r_{o2})$$

small-signal model



$$-g_m v_i - \frac{v_i}{r_{o1}} + v_o \left( \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right) = 0$$

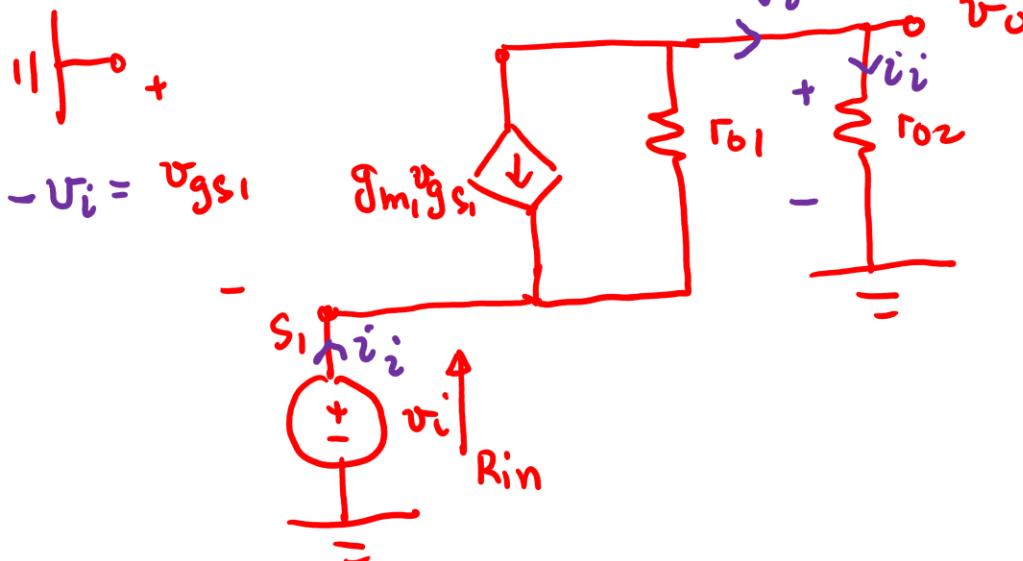
$$v_i \left( g_m + \frac{1}{r_{o1}} \right) = v_o \left( \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)$$

[ $r_{o1} \gg 1$ ]

$$\frac{v_o}{v_i} = \frac{g_m}{\left( \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)} = g_m \frac{1}{\left( \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)}$$

# Common Gate (CG) Amplifier (IC Version)

i/P Resistance ,  $R_{in} = \frac{v_i}{i_i} \Rightarrow i_i = -g_{m1}(-v_i) - \frac{v_o - v_i}{r_{o1}}$



$$v_o = i_i (r_{o2})$$

$$i_i = g_{m1}v_i - \frac{i_i r_{o2}}{r_{o1}} + \frac{v_i}{r_{o1}}$$

$$i_i \left(1 + \frac{r_{o2}}{r_{o1}}\right) = v_i \left(g_{m1} + \frac{1}{r_{o1}}\right)$$

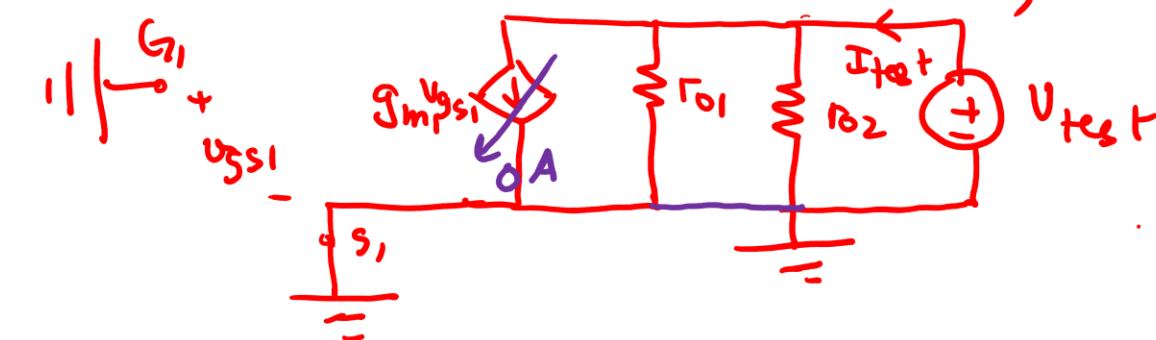
$$[r_{o1} \gg 1]$$

$$\frac{v_i}{i_i} = \frac{1 + \frac{r_{o2}}{r_{o1}}}{g_{m1}}$$

$$= \frac{1}{g_{m1}} + \frac{r_{o2}}{g_{m1} r_{o1}}$$

# Common Gate (CG) Amplifier (IC Version)

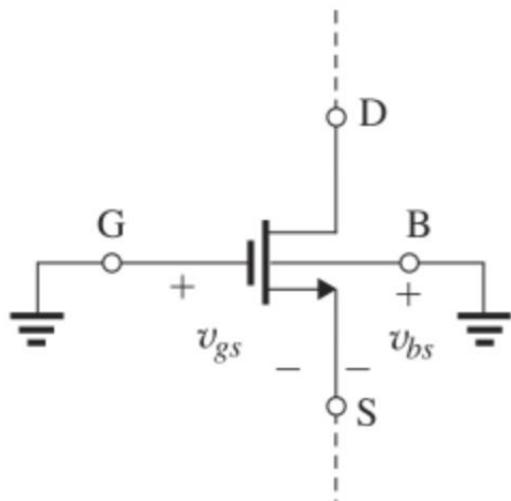
O/P Resistance : Thevenin's Theorem  
 Dependent Source Turn OFF all independent source  
 $v_i = 0V$   
apply a test voltage @ the terminal where  $R_o$  needs to be determined, calculate the test current



$$v_{GS1} = v_{G1} - v_{S1} = 0 - 0 = 0$$

$$R_o = \frac{V_{test}}{I_{test}} = R_{O1} // R_{O2}$$

# Body Effect in CG Amplifier

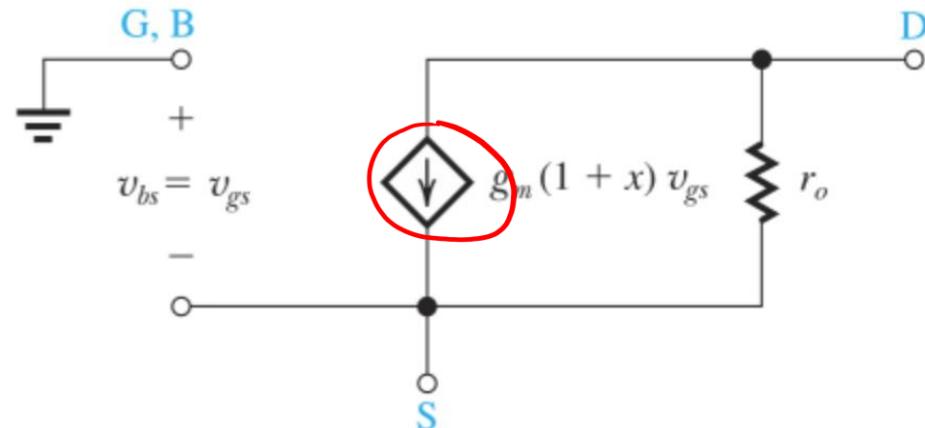


$v_{gs} \rightarrow$  current through drain

$$\text{diamond symbol } g_m v_{gs}$$

$v_{bs} \rightarrow$  current through drain

$$\text{diamond symbol } g_{mb} v_{bs} = \chi g_m v_{bs}$$



$$g_{mb} = \chi g_m$$

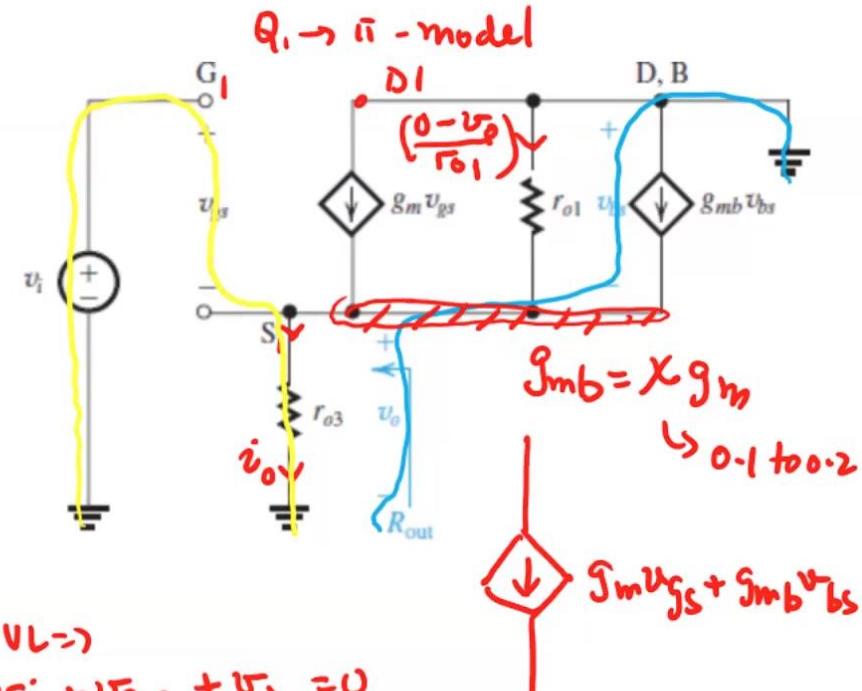
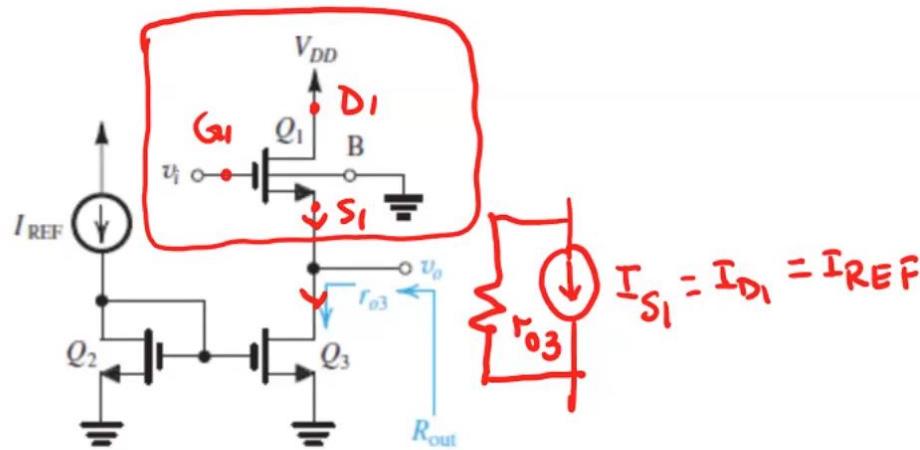
↳ fraction of  $g_m$

$\chi \rightarrow 0.1$  to  $0.2$

total drain current:

$$g_m v_{gs} + \chi g_m v_{bs} \\ = g_m (1 + \chi) v_{gs}$$

# Source Follower - Common Drain (CD) Amplifier



$$\text{Voltage gain, } A_v = \frac{v_o}{v_i}$$

$$v_o = i_o r_{o3} \quad (v_i - v_o) \quad (-v_o)$$

$$v_o = r_{o3} \left( g_m v_{gs} + g_{mb} \frac{v_{bs}}{r_{o1}} - \frac{v_o}{r_{o1}} \right)$$

$$v_o \left[ 1 + g_m r_{o3} + \frac{r_{o3}}{r_{o1}} + r_{o3} g_{mb} \right] = g_m r_{o3} v_i$$

$$[r_{o1} \gg 1 ; r_{o3} \gg 1]$$

$$\frac{v_o}{v_i} = \frac{g_m}{\frac{1}{r_{o3}} + g_m + \frac{1}{r_{o1}}} + g_{mb}$$

$$\text{KVL} \Rightarrow -v_i + v_{gs} + v_o = 0$$

$$v_{gs} = v_i - v_o$$

$$\text{KVL} \Rightarrow +v_{bs} + v_o = 0 \Rightarrow v_o = -v_{bs}$$

$$\frac{g_m}{g_m + X g_m} = \frac{1}{1+X}$$

$$|A_v| \leq 1$$

# Source Follower - Common Drain (CD) Amplifier

$$O/P \text{ Resistance, } R_o = \frac{V_{test}}{I_{test}}$$

$$V_{test} = -V_{gs}$$

$$v_{bs} = v_{gs}$$

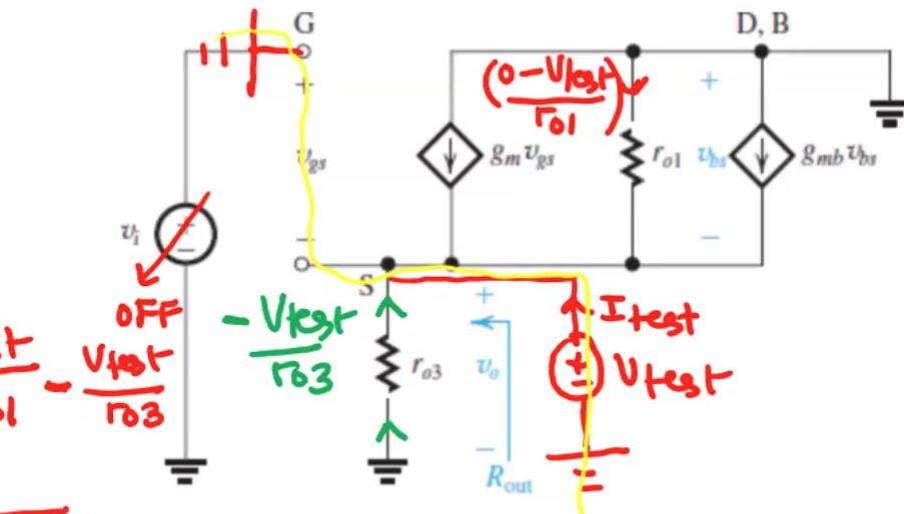
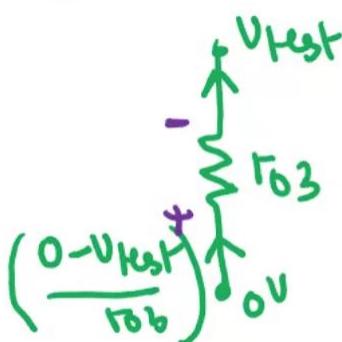
KCL@ S -Vtest

$$-I_{test} = g_m \cancel{v_s} + g_{mb} \cancel{v_{ds}} - \frac{V_{test}}{r_0} - \frac{V_{ds}}{r_0}$$

$$R_0 = \frac{V_{test}}{I_{test}} = \frac{1}{g_m + g_{mb} + \frac{1}{r_o} + \frac{1}{r_{o3}}}$$

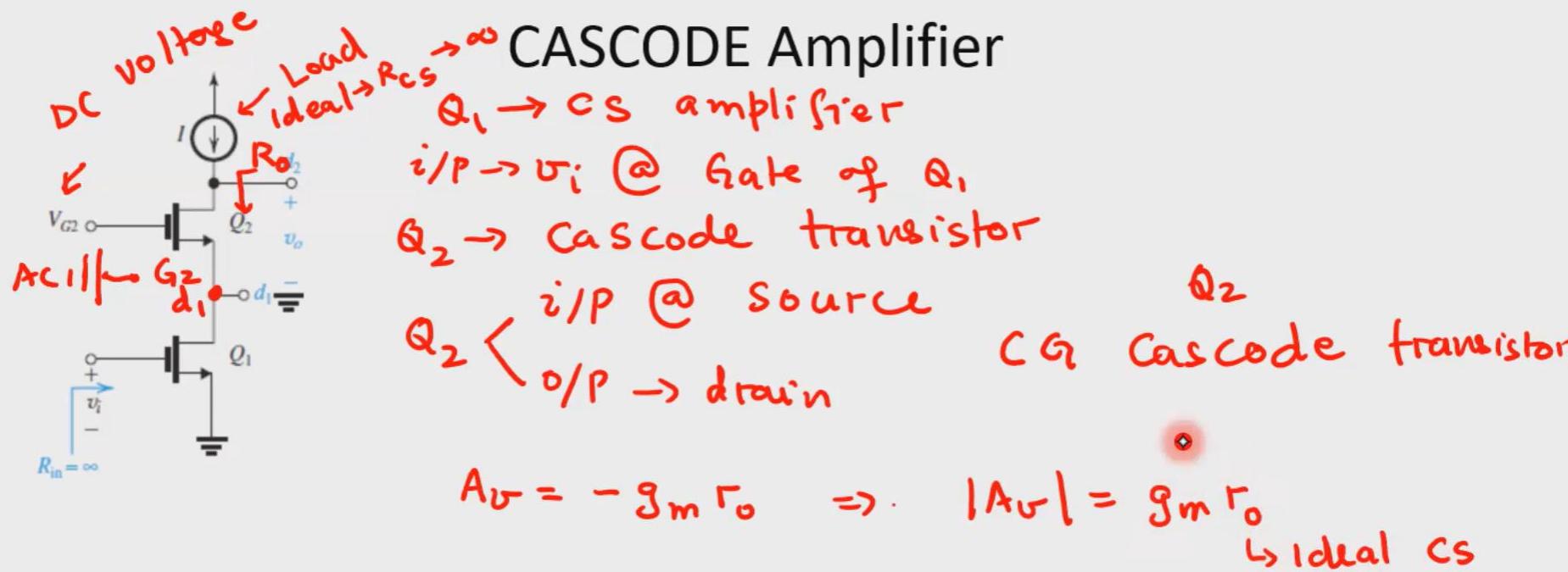
$$R_o = \frac{1}{\frac{1}{g_m} + \frac{1}{g_{mb}} + \frac{1}{r_{o1}} + \frac{1}{r_{o3}}}$$

$$R_0 = \frac{1}{g_m} // \frac{1}{g_{mb}} // r_{01} // r_{03}$$



$$R_o = \frac{1}{\frac{1}{g_m} + \frac{1}{g_{mb}}}$$

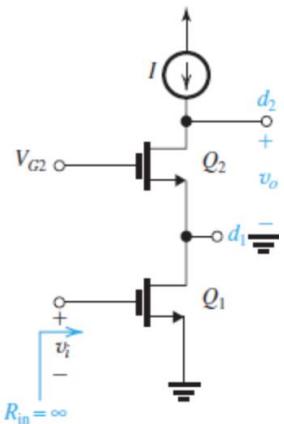
$$R_D = \left(\frac{1}{g_m}\right) // \left(\frac{1}{g_{mb}}\right)$$



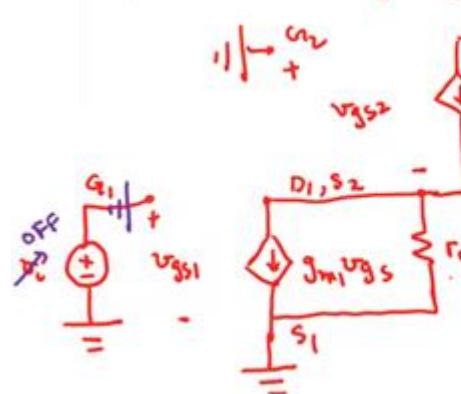
Cascode  $\Rightarrow$  overall o/p is taken  
from the drain of  $Q_2$  (CG stage)

- \* provide high value of  $R_o$
- \* provide high value of the voltage gain.

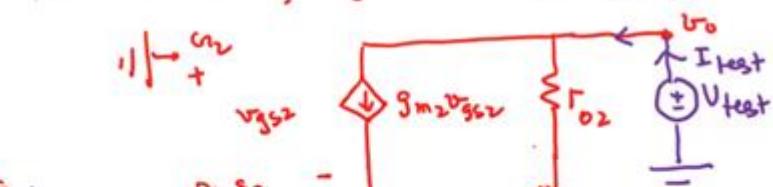
# CASCODE Amplifier



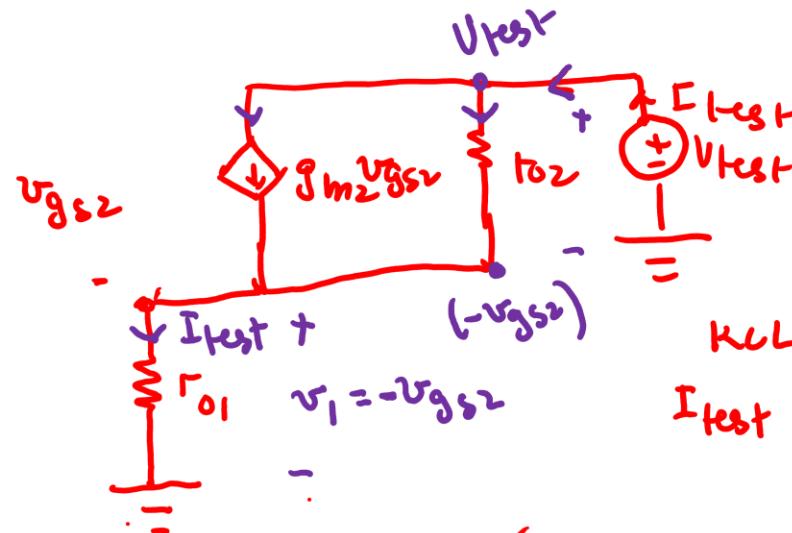
O/P Resistance,  $R_o$



AC circuit



$$G_2 \parallel \frac{v_{gs2}}{I}$$



$$R_o = \frac{U_{test}}{I_{test}}$$

$$KCL \Rightarrow (-I_{test} r_{o1})$$

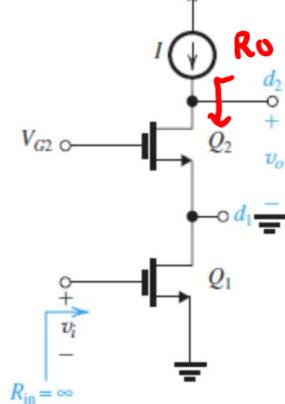
$$I_{test} = g_{m2} v_{gs2} + \left( \frac{U_{test} + v_{gs2}}{r_{o2}} \right)$$

$$I_{test} \left( 1 + g_{m2} r_{o1} + \frac{r_{o1}}{r_{o2}} \right) = \frac{U_{test}}{r_{o2}}$$

$$R_o = \left( 1 + g_{m2} r_{o1} + \frac{r_{o1}}{r_{o2}} \right) r_{o2} = g_{m2} r_{o1} r_{o2} + r_{o2} + r_{o1}$$

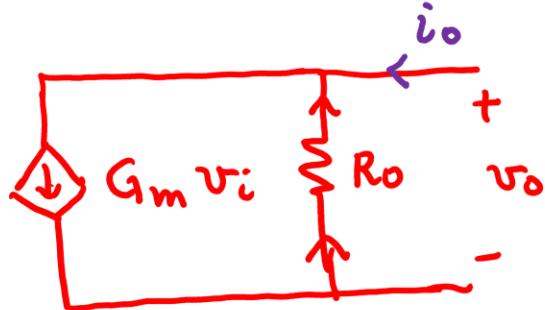
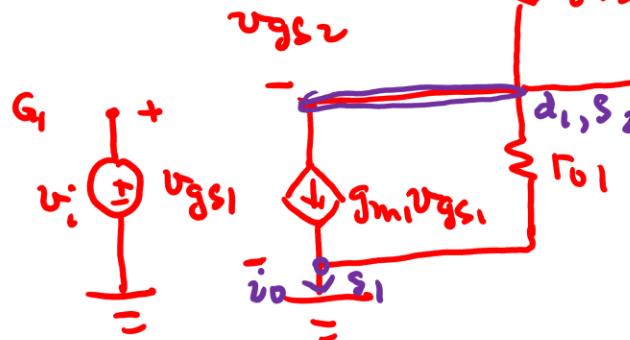
$$R_o \cong g_{m2} r_{o1}, r_{o2}$$

$$r_{01} \gg 1$$



Voltage gain  $\rightarrow$  AC circuit

$$1 + g_2$$



$$A_v = \frac{v_o}{v_i} = -\frac{G_m v_i R_o}{v_i}$$

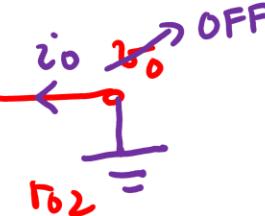
$$= G_m R_o$$

$$\frac{i_o}{v_i} = g_{m1} + \frac{g_{m1}}{g_{m2} r_{02}}$$

$$\frac{i_o}{v_i} = g_{m1}$$

$$\frac{v_o}{v_i} = g_{m1} R_o = g_{m1} (g_{m2} r_{01} r_{02})$$

# CASCODE Amplifier



$$v_{d2s2} = v_{gs2}$$

$$v_{d1s1} = -v_{gs2}$$

$$\left( \frac{i_o}{v_i} \right) R_o \Rightarrow \text{Voltage gain}$$

$$\text{KCL} \Rightarrow i_o = g_{m2} v_{gs2} + \frac{v_{d2s2}}{r_{02}} \quad \dots \quad ①$$

$$\text{KCL}@S_1 \Rightarrow i_o = g_{m1} v_i + \frac{v_{d1s1} (-v_{gs2})}{r_{01}} \quad \dots \quad ②$$

$$① = ②$$

$$g_{m1} v_i = g_{m2} v_{gs2} + \frac{v_{gs2}}{r_{02}} + \frac{v_{gs2}}{r_{01}} = v_{gs2} \left[ g_{m2} + \frac{1}{r_{02}} + \frac{1}{r_{01}} \right]$$

$$g_{m1} v_i = g_{m2} v_{gs2}$$

$$\Rightarrow i_o = g_{m1} v_i + \frac{v_{gs2}}{r_{02}} \frac{g_{m2} v_i}{g_{m2}}$$

$$\frac{v_o}{v_i} = (g_{m1} r_{01}) (g_{m2} r_{02}) \Rightarrow (g_{m1} r_{01})^2 = -(g_{m1} r_{01})^2$$