

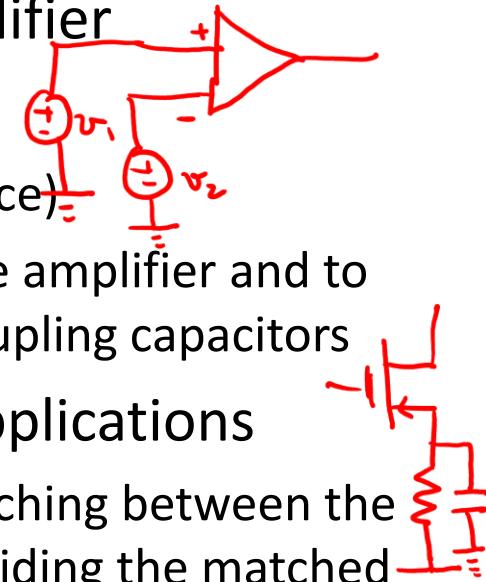
Chapter 9

Differential Amplifiers

MOSFET Based

Differential Amplifiers

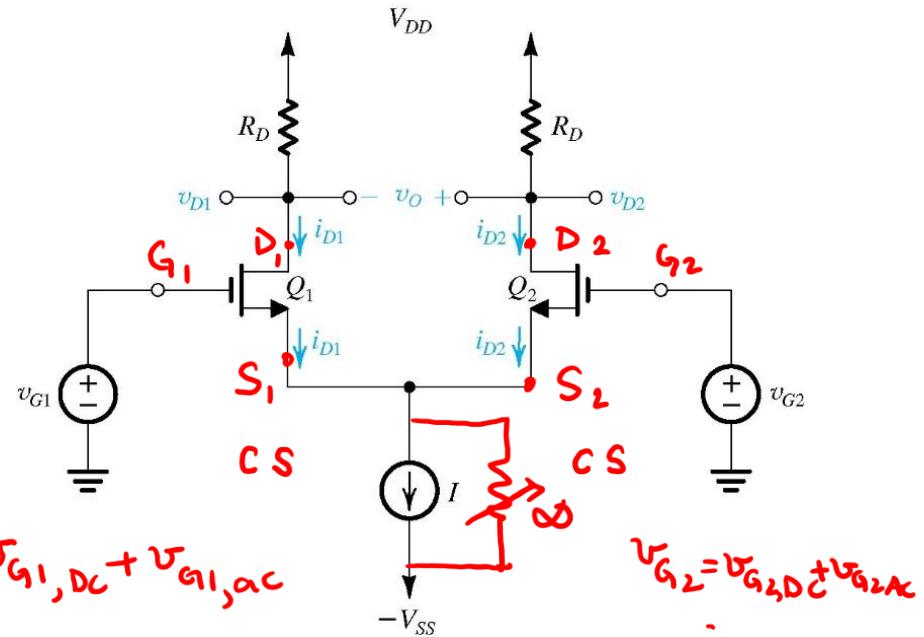
- In some applications, the difference of two signals is need to be amplified
- The input stage of an Op Amp is a differential amplifier
- Advantages:
 - Differential circuits are less sensitive to noise (interference)
 - Differential amplifier configuration enables us to bias the amplifier and to couple amplifier stages together without the need of coupling capacitors
- Differential amplifiers are very well suited for IC applications
 - Performance of the differential pair depends on the matching between the two sides of the circuit – IC fabrication is capable of providing the matched devices whose parameters track over wide ranges of changes in environmental conditions
 - Differential amplifiers utilize more components – IC technology has large no of transistors available at low cost



MOS Differential Amplifiers

- Two matched transistors: Q_1 and Q_2 : $\frac{W}{L}$ ratio same g_m , V_t
- The current source I is ideal (infinite resistance)
- MOSFET's remain in ACTIVE (Saturation) region of operation

BJT **MOSFET**



$$v_{G1} = v_{G1,DC} + v_{G1,AC}$$

$$v_{G2} = v_{G2,DC} + v_{G2,AC}$$

$$v_{G1,DC} = v_{G2,DC}$$

MOS Differential Amplifiers – operation with Common-Mode Input Voltage

- Equal voltages, V_{CM} , applied to two gate terminals
 - V_{CM} : Common-Mode Voltage, $v_{G1} = v_{G2} = V_{CM}$
 - Q_1 and Q_2 matched – I will divide equally between the transistors:
 $i_{D1} = i_{D2} = \frac{I}{2}$ $i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$
 - Voltage at the source: $V_S = V_{CM} - V_{GS}$
 - $\frac{I}{2} = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2$ $i_{D1} = \frac{I}{2} = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$
 - $\frac{I}{2} = \frac{1}{2} k'_n \frac{W}{L} (V_{OV})^2$ $\sqrt{V_{OV}^2} = \sqrt{\frac{I}{k'_n \left(\frac{W}{L} \right)}}$
 - $V_{OV} = \sqrt{\frac{I}{k'_n \left(\frac{W}{L} \right)}}$
 - $v_{D1} = v_{D2} = V_{DD} - \frac{I}{2} R_D$ $V_{D1} = V_{DD} - \frac{I}{2} R_D$ $V_{D2} = V_{DD} - \frac{I}{2} R_D$
- Single ended o/p* *Differential o/p* $\rightarrow V_o = V_o^+ - V_o^- = V_{D2} - V_{D1} = 0$
- $V_{GS} - V_t = V_{OV}$
 $V_{GS} > V_{tN}$: Q_1 and Q_2 to be ON
-

MOS Differential Amplifiers – Input Common-Mode Range (ICMR) $V_{CM,min} \leq V_{CM} \leq V_{CM,max}$

Q_1 and Q_2 : must be operating in saturation region

$$V_{DS} > V_{GS} - V_t$$

$$V_D - V_S \geq V_G - V_S - V_t \Rightarrow V_D \geq V_G - V_t \Rightarrow V_{DD} - \frac{I}{2}R_D \geq V_{CM} - V_t$$

$$V_{DD} - \frac{I}{2}R_D + V_t \geq V_{CM} \Rightarrow V_{CM} \leq V_{DD} - \frac{I}{2}R_D + V_t$$

- $V_{CMmax} = V_t + V_{DD} - \frac{I}{2}R_D$

minimum voltage across I : V_{CS}

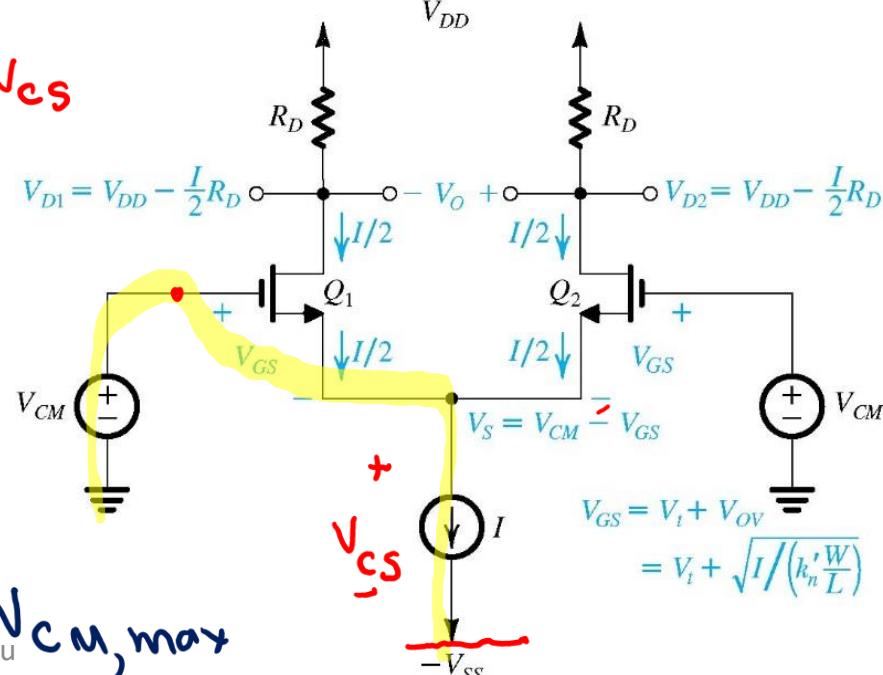
KVL \Rightarrow

$$-V_{CM,min} + V_{GS} + V_{CS} + (-V_{SS}) = 0$$

$$V_{CM,min} = V_{GS} + V_{CS} - V_{SS}$$

- $V_{CMmin} = -V_{SS} + V_{CS} + V_t + V_{OV}$

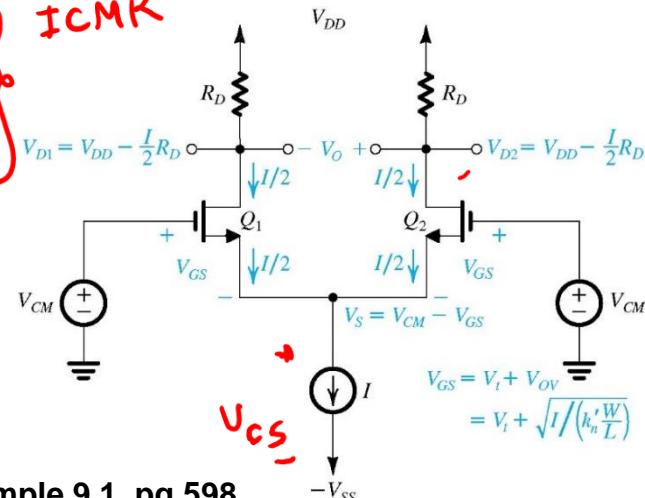
ICMR \Rightarrow $V_{CM,min} \leq V_{CM} \leq V_{CM,max}$



MOS Differential Amplifiers – Exercise

- For the MOS Differential pair with a common-mode voltage V_{CM} applied, as shown in the diagram below, let $V_{DD} = V_{SS} = 1.5 \text{ V}$, $k'_n \frac{W}{L} = 4 \frac{\text{mA}}{\text{V}^2}$, $V_t = 0.5 \text{ V}$, $I = 0.4 \text{ mA}$, and $R_D = 2.5 \text{ k}\Omega$, and neglect channel-length modulation (CLM). Assume that the current source requires a minimum voltage of 0.4 V to operate properly.

- Calculate V_{OV} and V_{GS} for each transistor
- For $V_{CM} = 0$, calculate V_S , I_{D1} , I_{D2} , V_{D1} , and V_{D2}
- Repeat part (2) for $V_{CM} = +1 \text{ V}$
- Repeat part (2) for $V_{CM} = -0.2 \text{ V}$
- Calculate the largest permitted value of V_{CM} ?
- Calculate the smallest value allowed for V_{CM} ?



MOS Differential Amplifiers – Exercise

- Calculate V_{OV} and V_{GS} for each transistor
- For $V_{CM} = 0$, calculate V_S , I_{D1} , I_{D2} , V_{D1} , and V_{D2}

① $I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L} \right) V_{OV}^2$

$$0.2 \text{ mA} = \frac{1}{2} 4 \text{ mA/V}^2 V_{OV}^2 \Rightarrow V_{OV} = \sqrt{\frac{2 \times 0.2}{4}}$$

$$V_{OV} = 0.316 \text{ V}$$

②

$$I_{D1} = I_{D2} = 0.2 \text{ mA}$$

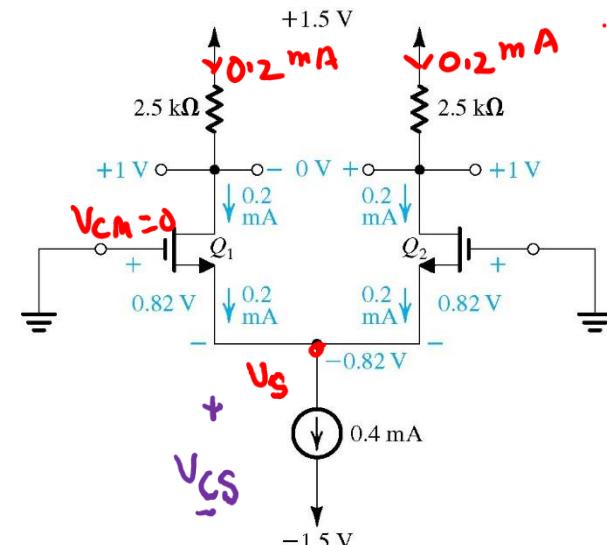
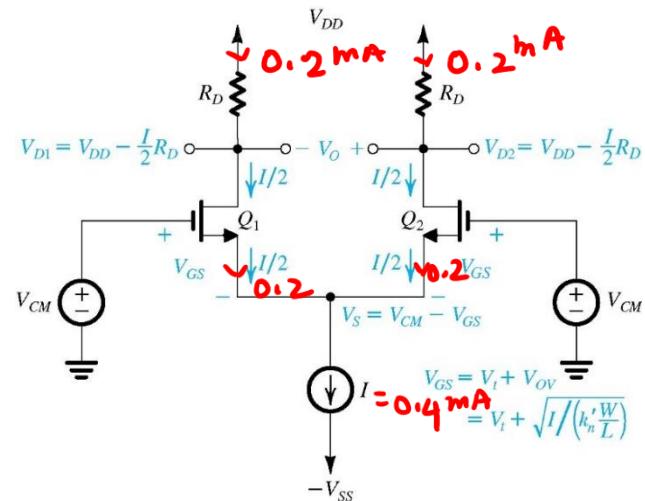
$$V_{D1} = V_{D2} = 1.5 - (2.5 \times 0.2) = 1 \text{ V}$$

$$V_{GS} = V_G - V_S \Rightarrow V_S = -V_{GS}$$

$$V_{GS} \Rightarrow V_{OV} = V_{GS} - V_t \Rightarrow V_{GS} = 0.316 + 0.5 \\ = 0.816 \text{ V}$$

$$V_S = -0.816 \text{ V}$$

$$V_{GS} = -0.816 - (-1.5) = 0.68 > 0.4 \text{ V}$$



MOS Differential Amplifiers – Exercise

③

Repeat part (2) for $V_{CM} = +1\text{ V}$

Repeat part (2) for $V_{CM} = -0.2\text{ V}$

$$③ \quad V_{CM} = 1\text{ V}$$

$$V_{D1} = V_{D2} = 1.5 - (2.5 \times 0.2) = 1\text{ V}$$

$$I_{D1} = I_{D2} = 0.2\text{ mA} \quad [\text{diagram}]$$

$$V_{GS} = V_G - V_S \Rightarrow V_S = V_G - V_{GS} = 1 - 0.816 \\ = 0.184 \approx 0.18\text{ V}$$

$$V_{CS} = V_S - (-1.5) = 0.18 - (-1.5) = 1.68 > 0.4$$

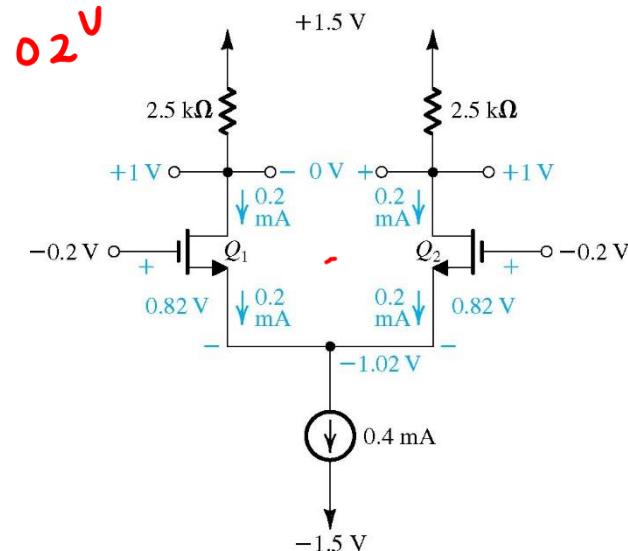
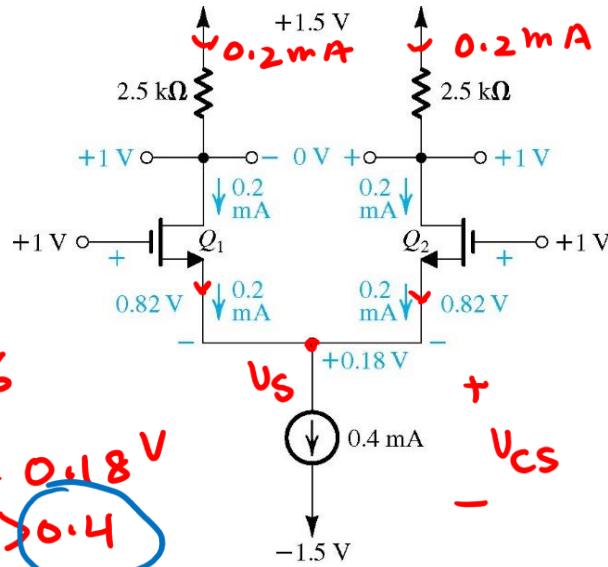
$$④ \quad V_{CM} = -0.2\text{ V}$$

$$V_{GS} = V_G - V_S \Rightarrow V_S = -0.2 - 0.816 = -1.02\text{ V}$$

$$V_{CS} = -1.02 - (-1.5) = 0.48 > 0.4\text{ V}$$

$$I_{D1} = I_{D2} = 0.2\text{ mA}$$

$$V_{D1} = V_{D2} = 1.5 - [2.5 \times 0.2] = 1\text{ V}$$



MOS Differential Amplifiers – Exercise

Calculate the largest permitted value of V_{CM} ?

Calculate the smallest value allowed for V_{CM} ?

$$V_{CMmax} = V_t + V_{DD} - \frac{I}{2} R_D = 0.5 + 1.5 - \frac{0.4}{2} (2.5) = 1.5^V$$

$$V_{CMmin} = -V_{SS} + V_{CS} + \cancel{V_t + V_{OV}} = -1.5 + 0.4 + 0.816 \\ V_{GS} = 0.816 = -0.28^V$$

$$\text{ICMR} \rightarrow -0.28 \leq V_{CM} \leq 1.5^V$$

MOS Differential Amplifiers - Differential Input Voltage

V_{CM} : Common-Mode Voltage

v_{id} : differential input signal

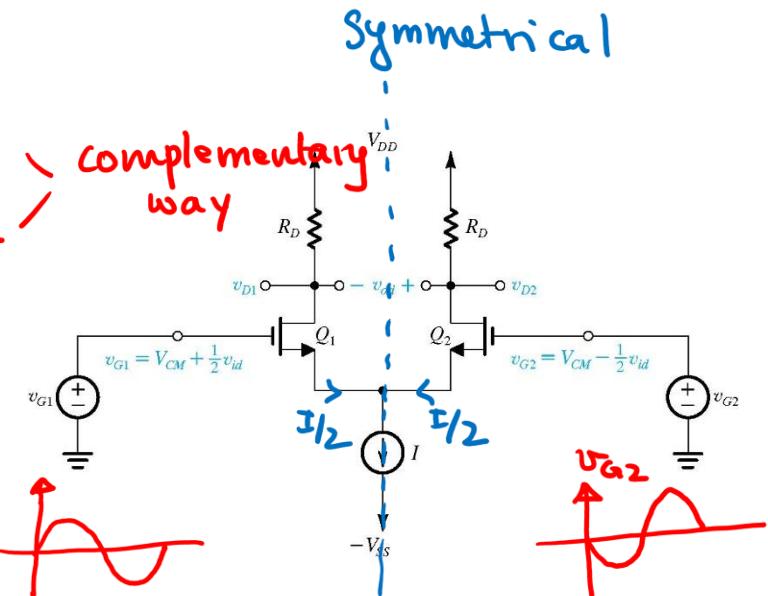
output: Single ended v_{o1}, v_{o2} or Differential v_{od}

$$\frac{1}{2}v_{id} \rightarrow G_1 \quad \text{complementary way}$$

$$\frac{1}{2}v_{id} \rightarrow G_2$$

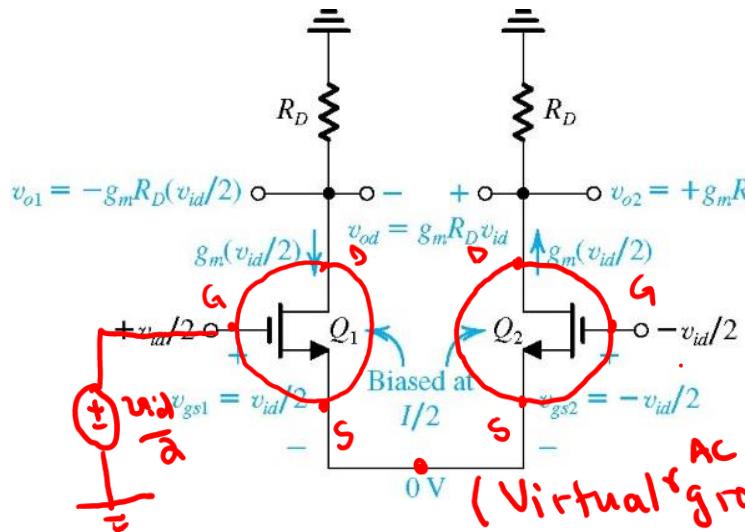
$$v_{od} = v_{o2} - v_{o1}$$

$$= v_{o2} - v_{o1}$$

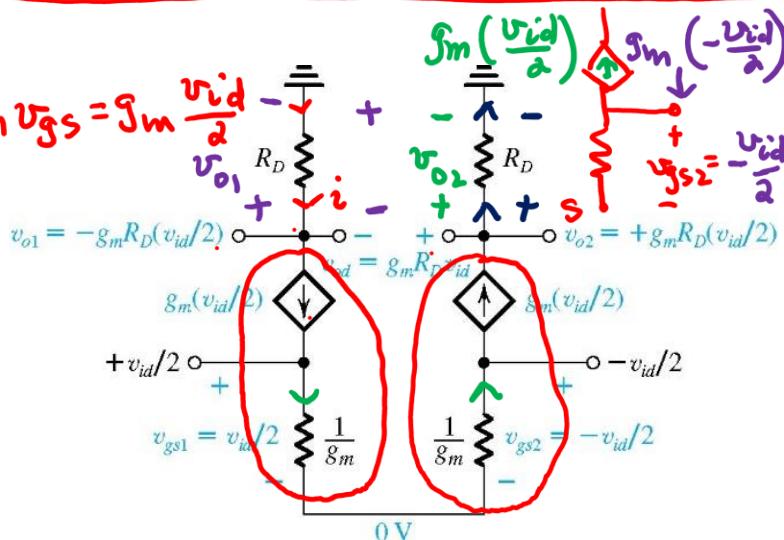
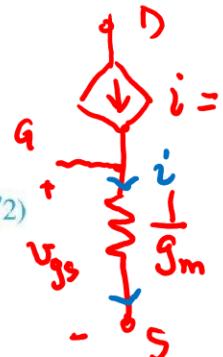


AC Circuit

turn off all DC sources
 V_{DD}, V_{CM}



AC Circuit: MOSFET replaced by small signal t-model



Musone, Gaudet

MOS Differential Amplifiers - Differential Input Voltage

$$v_{o1} = -g_m \frac{v_{id}}{2} R_D$$

$$v_{o2} = g_m \frac{v_{id}}{2} R_D$$

Gain based on Single-ended output

$$A_v = \frac{v_o}{v_{in}}$$

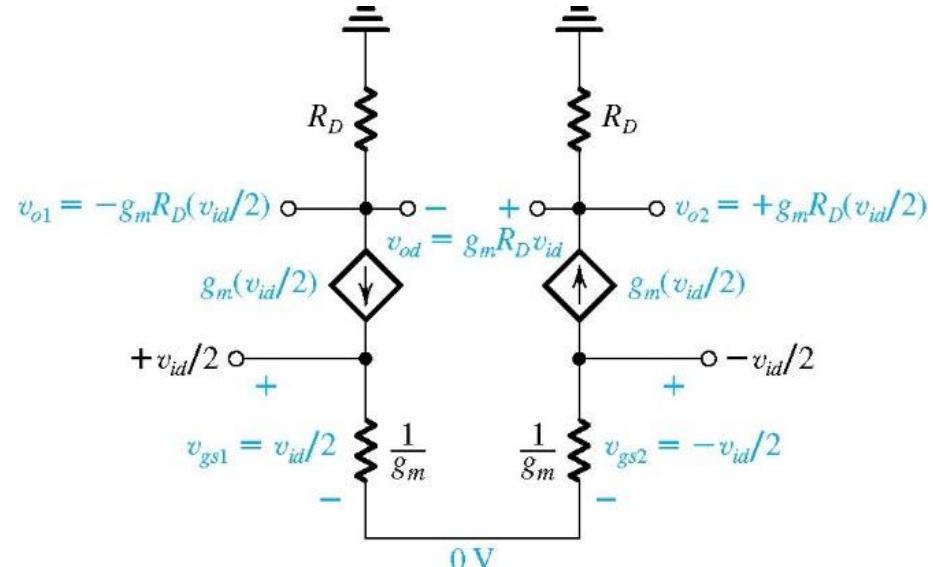
$$\frac{v_{01}}{v_{id}} = -\frac{1}{2} g_m R_D$$

$$\frac{v_{02}}{v_{id}} = \frac{1}{2} g_m R_D$$

Gain based on Differential output $v_{od} = v_{o2} - v_{o1}$

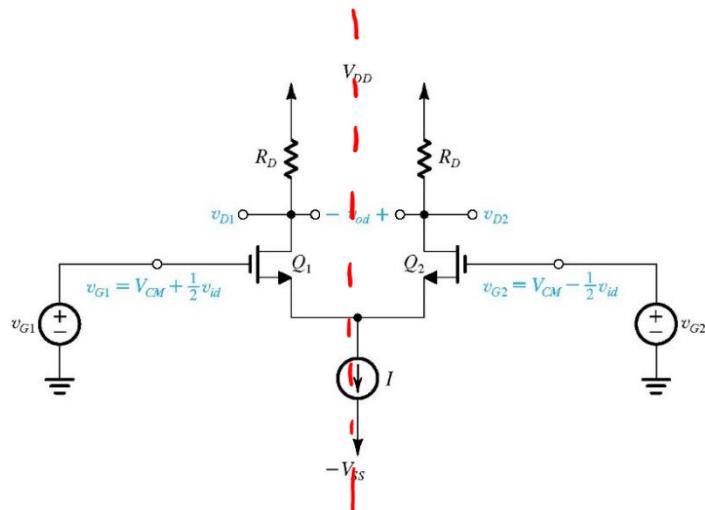
$$A_d = \frac{v_{0d}}{v_{id}} = \frac{v_{02} - v_{01}}{v_{id}} = \frac{g_m R_D}{\frac{v_{id}}{2} + \left(\frac{v_{id}}{2} \right)}$$

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}}$$



$$\frac{v_{id}}{2} + \left(\frac{v_{id}}{2} \right) = v_{id}$$

MOS Differential Amplifiers – Half Circuit

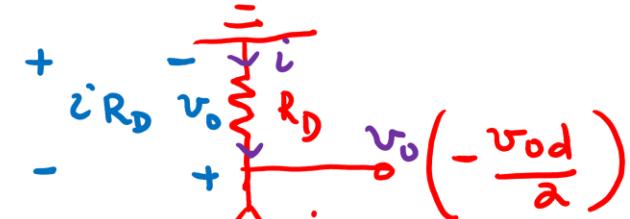
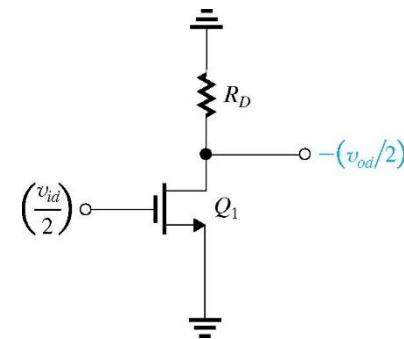


$$A_d = \frac{v_{od}}{v_{id}}$$

$$A_v = \frac{v_o}{v_{in}} = -\frac{iR_D}{i(\frac{1}{g_m})} = -\frac{(-\frac{v_{od}}{2})}{\frac{v_{id}}{2}}$$

$$= g_m R_D$$

AC circuit

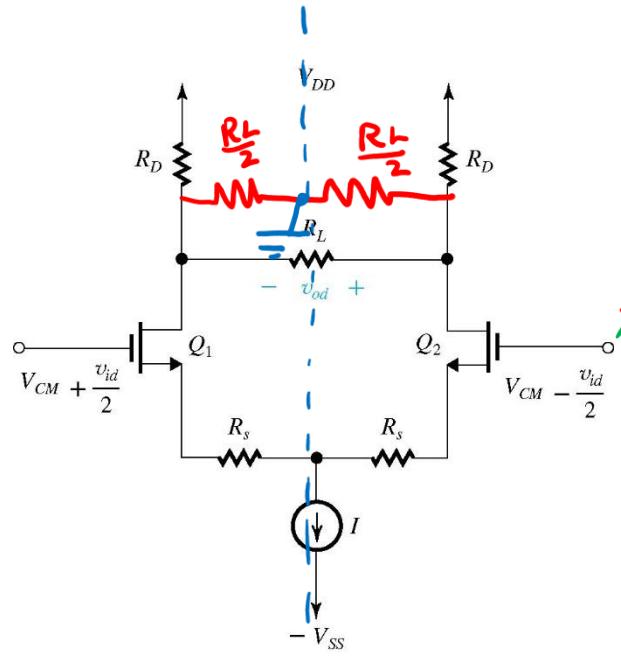


$$A_d = g_m R_D$$

MOS Differential Amplifier – Example 9.2

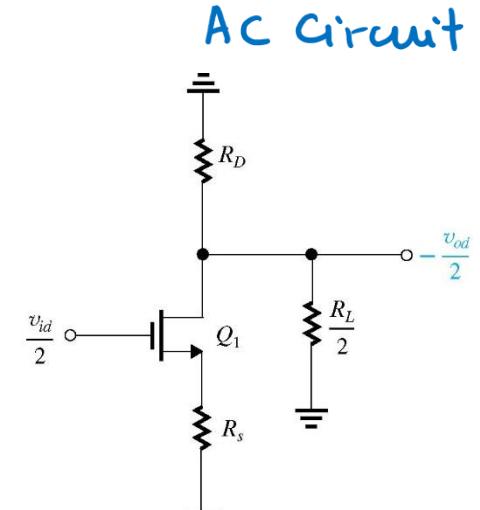
Assume that Q_1 and Q_2 are perfectly matched. Neglect r_o , determine the

Differential Voltage Gain $A_d = \frac{v_{od}}{v_{in}}$

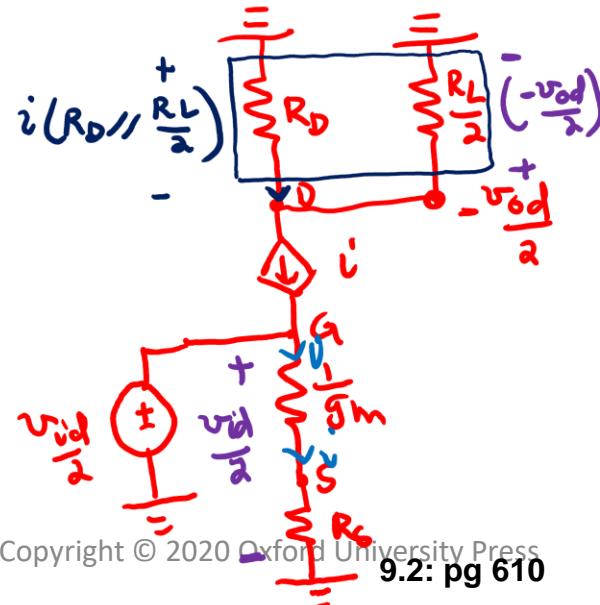


Differential Amplifier Circuit

$$\begin{aligned}
 \frac{v_{id}}{2} &= i \left(\frac{1}{gm} + R_s \right) \\
 + \frac{v_{od}}{2} &= -i \left(R_D // \frac{R_L}{2} \right) \\
 \frac{v_{od}/2}{v_{id}/2} &= \frac{v_{od}}{v_{id}} = Ad \\
 &= \frac{R_D // \frac{R_L}{2}}{\left(\frac{1}{gm} + R_s \right)}
 \end{aligned}$$



Half Circuit



MOS Differential Amplifier with Current Source Loads – Exercise 9.5

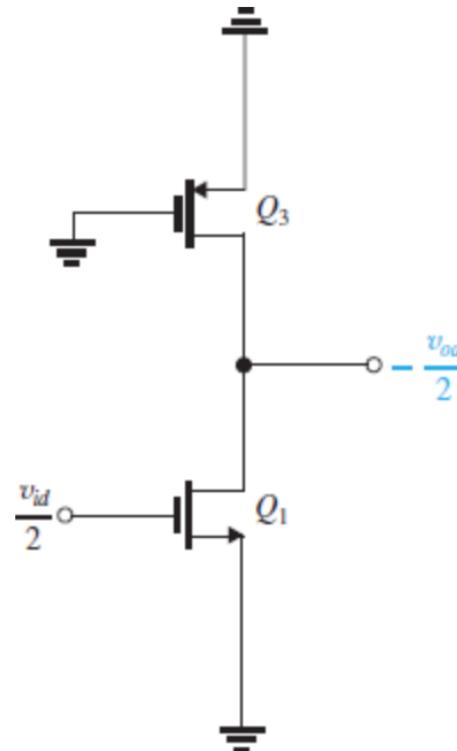
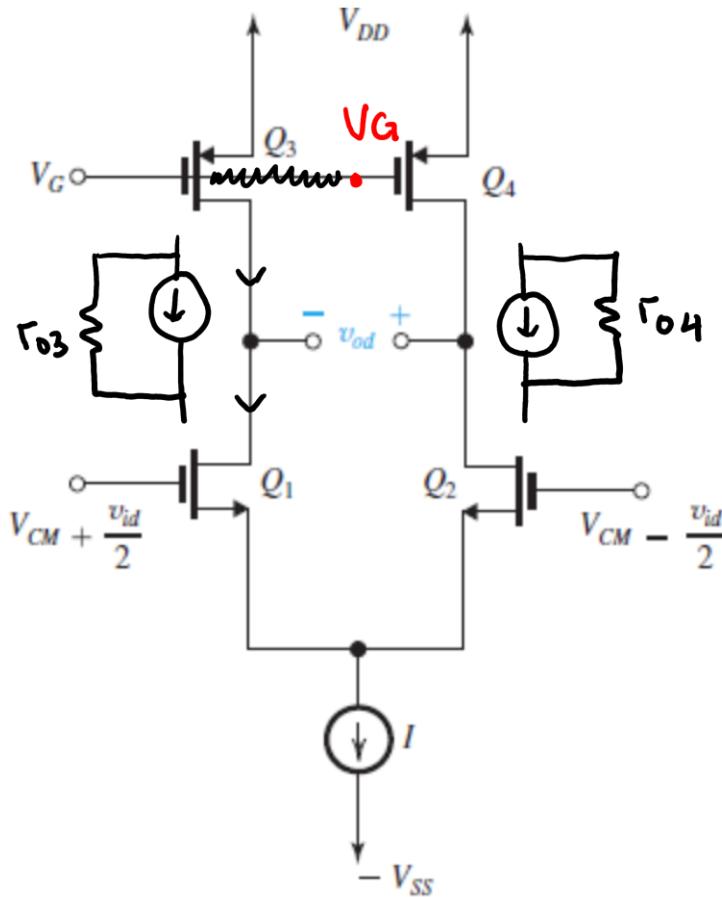
9.5

The differential amplifier of Fig. 9.12(a) is fabricated in a $0.18\text{-}\mu\text{m}$ CMOS technology for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 400 \mu\text{A/V}^2$, $|V_t| = 0.5 \text{ V}$, and $|V_A| = 10 \text{ V}/\mu\text{m}$. If the bias current $I = 200 \mu\text{A}$ and all transistors have a channel length twice the minimum and are operating at $|V_{ov}| = 0.2 \text{ V}$, find W/L for each of Q_1 , Q_2 , Q_3 , and Q_4 , and determine the differential voltage gain A_d .

$$K_h' \quad 4K_p'$$

$$L = 2 \times 0.18 = 0.36 \text{ mm}$$

$$L \quad V_A = V_A' \cdot L = 10 \times 0.36 = 3.6 \text{ V}$$



MOS Differential Amplifier with Current Source Loads – Exercise 9.5

9.5

The differential amplifier of Fig. 9.12(a) is fabricated in a 0.18- μm CMOS technology for which $\mu_nC_{\text{ox}} = 4\mu_pC_{\text{ox}} = 400 \mu\text{A/V}^2$, $|V_t| = 0.5 \text{ V}$, and $|V_A| = 10 \text{ V}/\mu\text{m}$. If the bias current $I = 200 \mu\text{A}$ and all transistors have a channel length twice the minimum and are operating at $|V_{\text{ov}}| = 0.2 \text{ V}$, find W/L for each of Q_1 , Q_2 , Q_3 , and Q_4 , and determine the differential voltage gain A_d .

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{w}{L} \right)_{1,2} (V_{OV1})^2$$

$$100 \text{ mA} = \frac{1}{2} \times 400 \text{ MA/V}^2 \left(\frac{w}{L} \right)_{1,2} 0.2^2$$

$$\left(\frac{w}{L} \right)_{1,2} = 12.5$$

$$w_1 = w_2 = 12.5 \times (2 \times 0.18) = 4.5 \text{ mm}$$

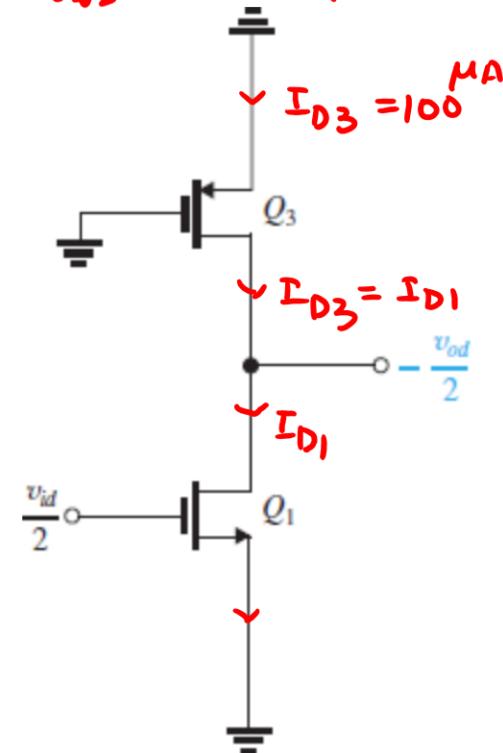
$$I_{D3} = \frac{1}{2} k_p' \left(\frac{w}{L} \right)_{3,4} (V_{OV3})^2$$

$$100 \text{ mA} = \frac{1}{2} \left(100 \text{ MA/V}^2 \right) \left(\frac{w}{L} \right)_{3,4} (0.2)^2$$

$$\left(\frac{w}{L} \right)_{3,4} = 50$$

$$w_3 = w_4 = 50 \times 0.36 = 18 \mu\text{m}$$

$$V_{OV1} = V_{OV2} = V_{OV3} = V_{OV4} = 0.2 \text{ V}$$



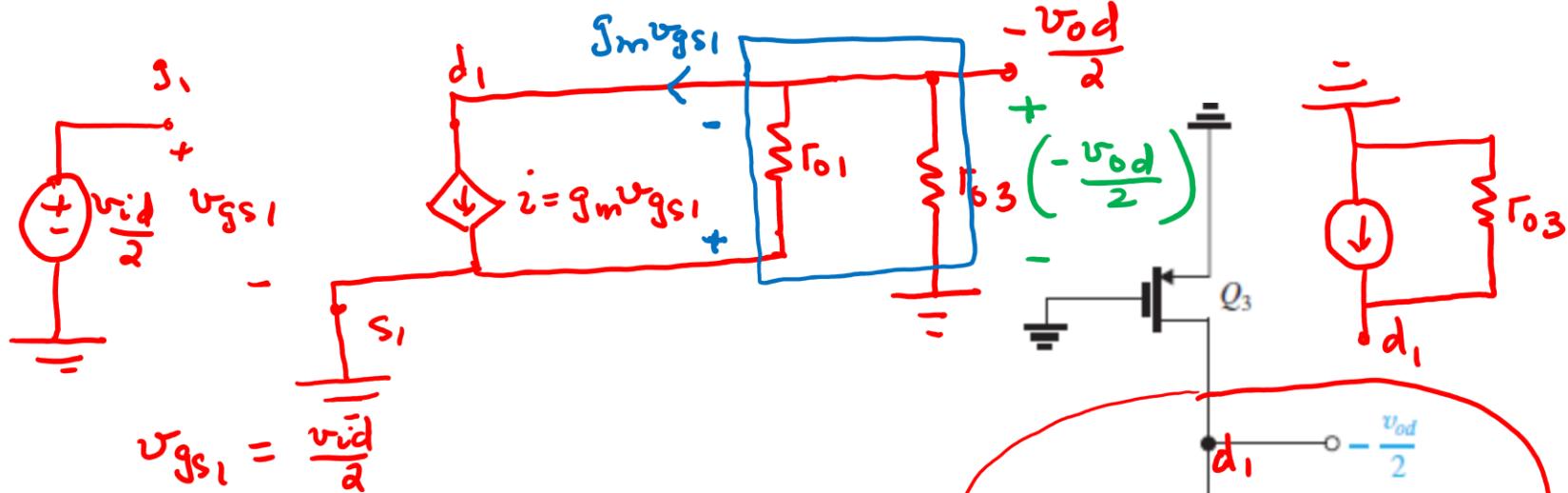
MOS Differential Amplifier with Current Source Loads – Exercise 9.5

9.5

The differential amplifier of Fig. 9.12(a) is fabricated in a $0.18\text{-}\mu\text{m}$ CMOS technology for which $\mu_n C_{ox} = 4\mu_p C_{ox} = 400 \mu\text{A/V}^2$, $|V_t| = 0.5 \text{ V}$, and $|V_A| = 10 \text{ V}/\mu\text{m}$. If the bias current $I = 200 \mu\text{A}$ and all transistors have a channel length twice the minimum and are operating at $|V_{ov}| = 0.2 \text{ V}$, find W/L for each of Q_1 , Q_2 , Q_3 , and Q_4 , and determine the differential voltage gain A_d .

transistor replaced by small-signal model

$$A_d = \frac{v_{od}}{v_{id}}$$

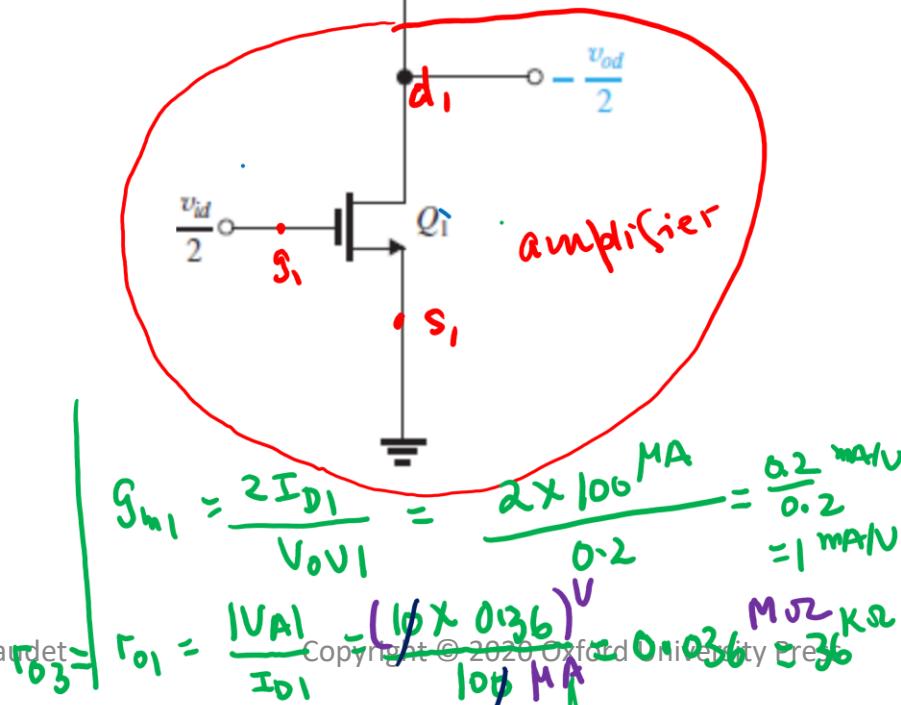


$$\frac{v_{od}}{2} = g_m v_{gs1} (\Gamma_{o1} \parallel \Gamma_{o3})$$

$$\frac{v_{od}}{2} = g_m \frac{v_{id}}{2} (\Gamma_{o1} \parallel \Gamma_{o3})$$

$$A_d = \frac{v_{od}}{v_{id}} = g_m (\Gamma_{o1} \parallel \Gamma_{o3})$$

$$A_d = 1 (36/136) = 18 \text{ V/V}$$



MOS Differential Amplifiers – Exercise

A6.5

Design the circuit in **Fig. 5** to obtain a dc voltage of 0 V at each of the drains of Q_1 and Q_2 when $v_{G1} = v_{G2} = 0$ V. Operate all transistors at $V_{ov} = 0.15$ V and assume that $V_{tn} = 0.35$ V and $K'_n = 400 \mu\text{A/V}^2$. Neglect channel-length modulation.
 $(r_o \rightarrow \infty)$

Determine the values of R , R_D , and the W/L ratios of Q_1 , Q_2 , Q_3 , and Q_4 . What is the input common-mode voltage range for your design?

Exercise 9.6 (Back of the
Differential chapter 9)

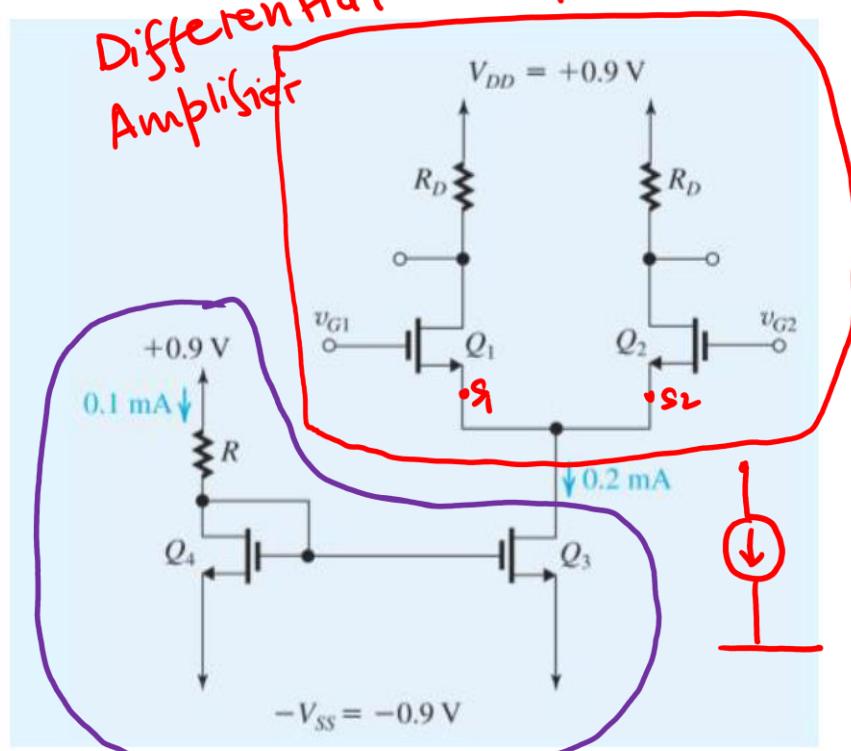
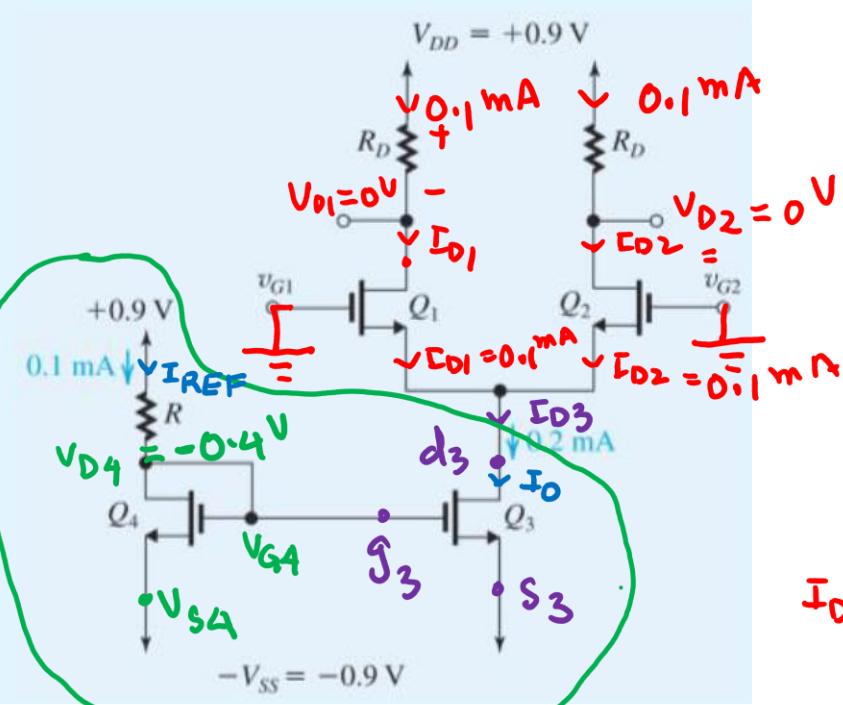


Fig. 5 Current mirror

MOS Differential Amplifiers – Exercise



$$\frac{I_D}{I_{REF}} = \frac{(W/L)_3}{(W/L)_4}$$

$$\frac{0.2 \text{ mA}}{0.1 \text{ mA}} = \frac{44.4}{(W/L)_4}$$

$$\left(\frac{W}{L}\right)_4 = \frac{1}{2} (44.4) = 22.2$$

$$R_D = \frac{0.9 - 0}{0.1 \text{ mA}} = 9 \text{ k}\Omega$$

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L} \right)_{1,2} (V_{DS})_{1,2}^2 = I_{D2}$$

$$0.1 \text{ mA} = \frac{1}{2} 400 \text{ mA/V}^2 \left(\frac{W}{L} \right)_{1,2} (0.15)^2$$

$$\left(\frac{W}{L} \right)_{1,2} = \frac{2 \times 0.1}{0.4 (0.15)^2} = 22.2$$

$$I_{D3} = \frac{1}{2} k_n' \left(\frac{W}{L} \right)_3 (V_{DS})_3^2$$

$$0.2 \text{ mA} = \frac{1}{2} \times 0.4 \text{ mA/V}^2 \left(\frac{W}{L} \right)_3 (0.15)^2$$

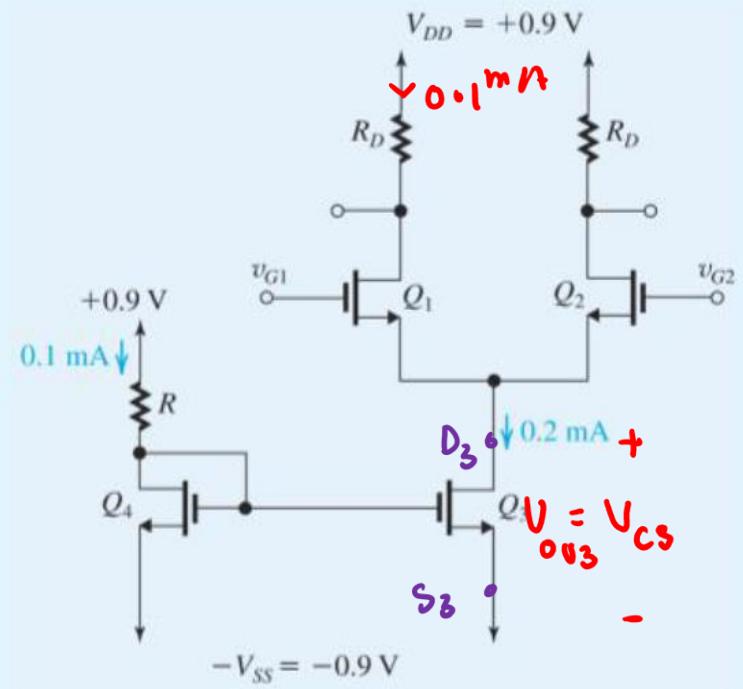
$$\left(\frac{W}{L} \right)_3 = 44.4$$

$$R \Rightarrow R = \frac{0.9 - (-0.4)}{0.1 \text{ mA}}$$

$$R = 13 \text{ k}\Omega$$

$$\begin{cases} V_{DS} = 0.15 \text{ V} \\ V_{GS4} - V_{th} = 0.15 \text{ V} \\ V_{GS4} = 0.15 + 0.35 = 0.5 \text{ V} \\ V_{DS4} = V_{GS4} \\ V_{D4} - V_{S4} = 0.5 \\ V_{D4} = 0.5 + (-0.9) \end{cases}$$

MOS Differential Amplifiers – Exercise



$$V_{DS3} > (V_{GS3} - V_{th})$$

$$V_{DS3} > (V_{GS3})$$

$$V_{DS3} = V_{CS}$$

ICMR

$$\begin{aligned} V_{CM, \max} &= V_{DD} - i_D R_D + V_{th} \\ \text{Slide #5} &\quad \swarrow \\ V_{CM, \min} &= -V_{SS} + V_{CS} + V_{GS} \end{aligned}$$

$V_{CM, \max} \rightarrow Q_1$ and Q_2 remain operating in saturation region

$$V_D - V_S = V_{DS} \geq V_{GS} - V_{th}$$

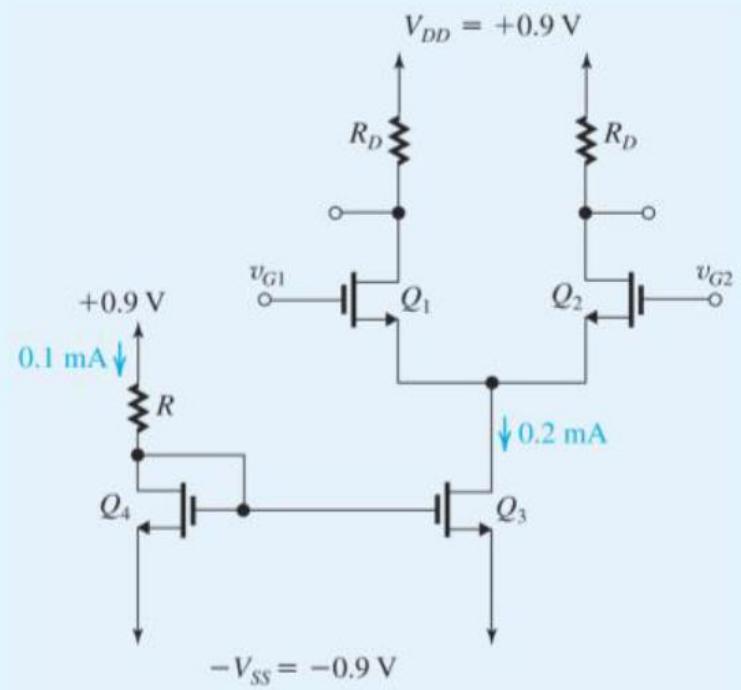
$$V_{CM, \max} = 0.9 - (0.1 \times 9 \text{ K}) + 0.35 = 0.35 \text{ V}$$

$$\begin{aligned} V_{CM, \min} &= -0.9 + (V_{GS} + V_{th}) + V_{CS} \\ &= -0.9 + (0.15 + 0.35) + 0.15 \\ &= -0.25 \text{ V} \end{aligned}$$

ICMR

$$-0.25 \leq V_{CM} \leq 0.35$$

MOS Differential Amplifiers – Exercise



MOS Differential Amplifiers – Exercise

$M_1 \rightarrow Q_1$
 $M_2 \rightarrow Q_2$

MOSFET Transistors

A6.2

Consider the amplifier shown in Fig.2 with M_1/M_2 matched.

- Draw the differential half-circuit of the amplifier.
- Derive an expression the differential gain A_v .

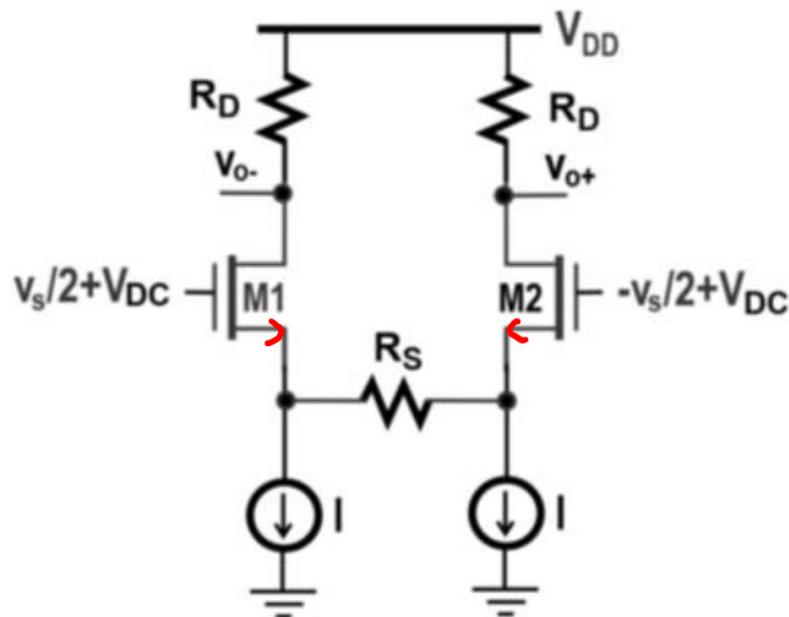
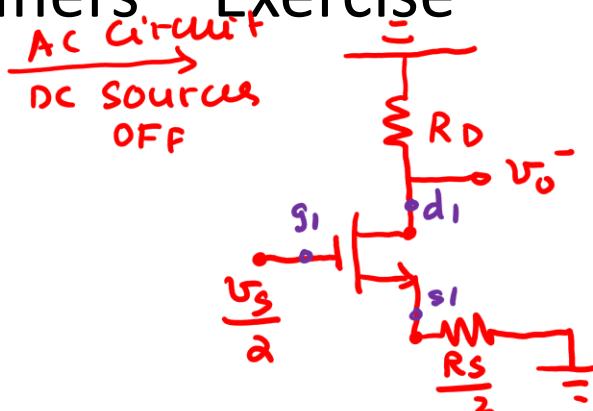
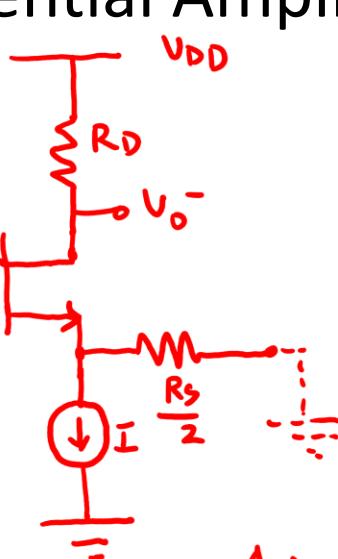
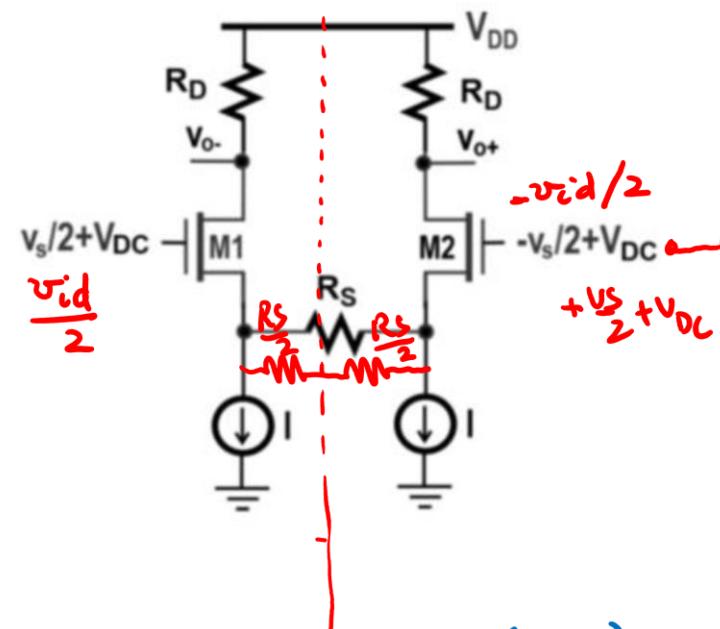


Fig. 2. M_1 and M_2 are NMOS transistors

MOS Differential Amplifiers – Exercise



$$A_d = \frac{v_{od}}{v_{id}} = \frac{v_o^+ - v_o^-}{v_s}$$

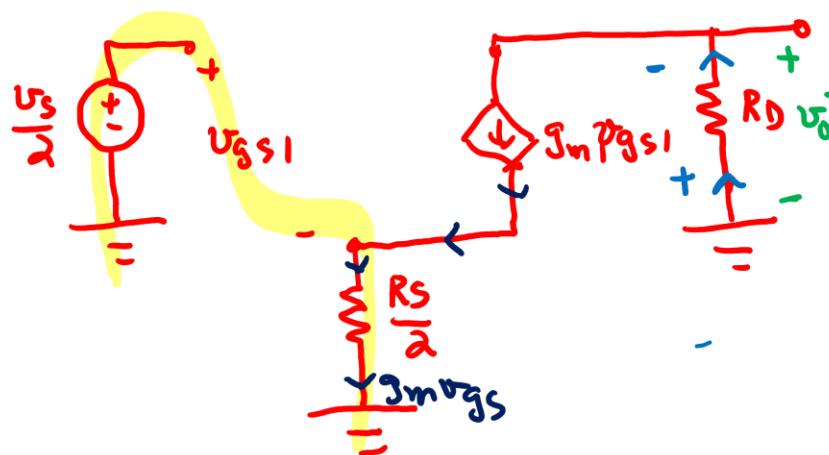
$$v_o^- = -g_{m1} (v_{gs1}) R_D$$

$$\text{KVL} \Rightarrow -\frac{v_s}{2} + v_{gs1} + \frac{R_S}{2} (g_m, v_{gs1}) = 0$$

$$\frac{v_s}{2} = v_{gs1} \left[1 + g_m \frac{R_S}{2} \right]$$

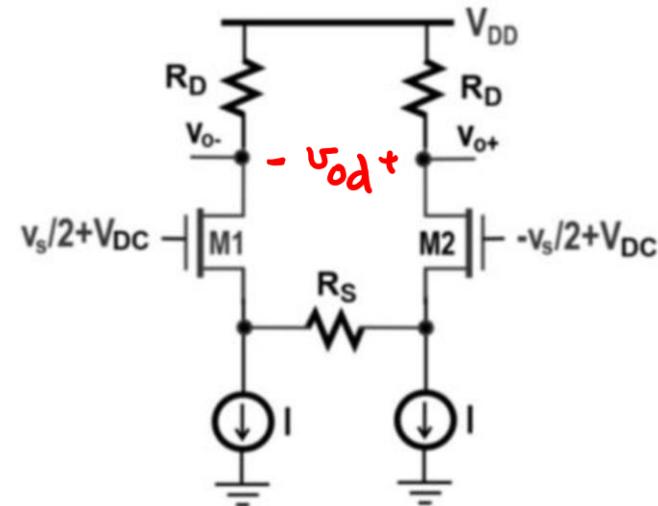
$$v_o^- = -g_{m1} \left[\frac{v_s/2}{1 + g_{m1} \frac{R_S}{2}} \right] R_D$$

$$v_o^+ = g_{m1} \left[\frac{v_s/2}{1 + g_{m1} \frac{R_S}{2}} \right] R_D$$



$$g_{m1} = g_{m2} = g_m$$

MOS Differential Amplifiers – Exercise



$$A_d = \frac{v_o^+ - v_o^-}{v_s}$$

$$= g_m \left[\frac{v_s/2}{1 + g_m \frac{R_S}{2}} \right] R_D + g_m \left[\frac{v_s/2}{1 + g_m \frac{R_S}{2}} \right] R_D$$

v_s

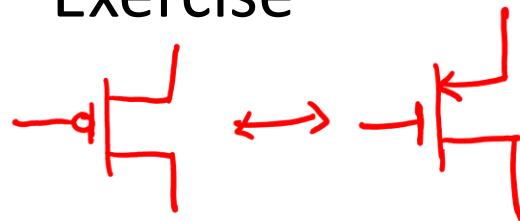
$$\cancel{\times} g_m \left[\frac{v_s}{1 + g_m \left(\frac{R_S}{2} \right)} \right] R_D$$

v_s

$$A_d = \frac{g_m R_D}{1 + g_m \left(\frac{R_S}{2} \right)}$$

$$A_d = \frac{g_m R_D}{1 + g_m \left(\frac{R_S}{2} \right)}$$

MOS Differential Amplifiers – Exercise



A6.3

$$0.5 \text{ k}\Omega = 500 \text{ }\Omega$$

PMOS

Consider amplifier in Fig. 3. Let $V_{tp} = -0.8 \text{ V}$, $K_p(W/L)_{1,2} = 4 \text{ mA/V}^2$, $I = 0.5 \text{ mA}$, $R_D = 5 \text{ k}\Omega$ and $V_{DD} = 2.5 \text{ V}$. Neglect channel length modulation.

- (a) For $v_{in} = 0$, find $V_{OD1,2}$, $V_{SG1,2}$, V_S , and $v_{o-+,DC}$.
- (b) If the minimum required voltage drop across the current source is 0.4 V, find the input common-mode voltage range (ICMR).

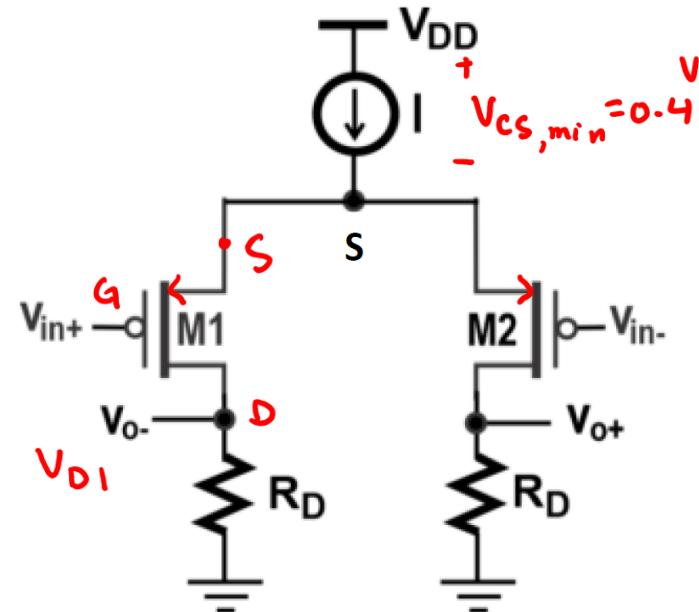


Fig. 3. M_1 and M_2 are PMOS transistors

MOS Differential Amplifiers – Exercise

$$I_{D1} = I_{D2} = 0.25 \text{ mA}$$

$$V_{o,dc}^- = 0.25 \times 0.5 = 0.125 \text{ V} = V_{o,dc}^+$$

$$V_{SG1} = V_s - V_{G1} = V_s$$

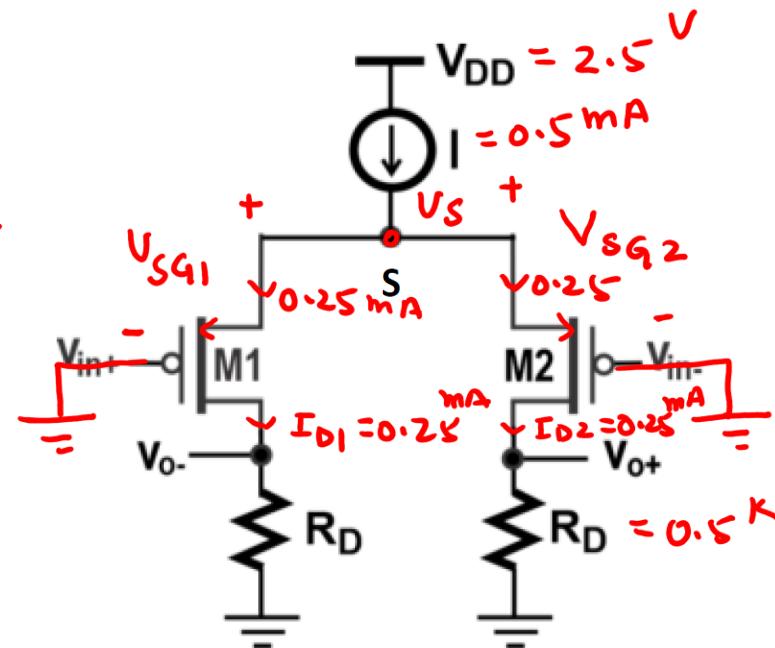
$$I_{D1} = \frac{1}{2} k_p' \left(\frac{W}{L} \right) \cdot \left(V_{SG1} - |V_{tp}| \right)^2$$

$$0.25 \text{ mA} = \frac{1}{2} 4 \text{ mA/V}^2 \left(V_{SG1} - 0.8 \right)^2$$

$$V_{SG1} = 0.8 + \sqrt{\frac{2 \times 0.25}{4}} = 1.15 \text{ V}$$

$$V_s = 1.15 \text{ V}$$

$$V_{SG2} = V_s - V_{G2} = V_s = 1.15 \text{ V}$$



MOS Differential Amplifiers – Exercise

I_{CMR}

$V_{CM, min}$

$V_{CM, max}$

$$V_{CM, max} = V_{D1D} - 2r_D R_D + |V_{TP}|$$

\Rightarrow

$$V_{SG} = V_s - \frac{V_G}{V_{CM}}$$

ICMR
 $-0.675 \leq V_{CM} \leq 0.95$

$$V_s = V_{SG} + V_{CM}$$

$$V_{s, max} = V_{SG} + V_{CM, max}$$

$$2.5 - V_{CS, min} = V_{SG} + V_{CM, max}$$

$$2.5 - 0.4 = 1.15 + V_{CM, max} \Rightarrow V_{CM, max} = 2.5 - 0.4 - 1.15 = 0.95$$

$$V_{CM, min} = -V_{SS} + V_{CS} + V_{GS} \text{ (NMOS)}$$

$V_{CM, min} \rightarrow$ As $V_{CM} \downarrow$, $V_s \downarrow$, until M_1 leaves the saturation region $\Rightarrow V_{SD1} > V_{SG1} - |V_{TP}|$

$$\cancel{V_s - V_{D1}} > V_s - V_{G1} - 0.8 \Rightarrow V_{D1} > V_{G1} + 0.8 \Rightarrow V_{CM}$$

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 $V_{CM, min} = 0.125 - 0.8 = -0.675$

MOS Differential Linear Amplifier – Exercise

A6.6

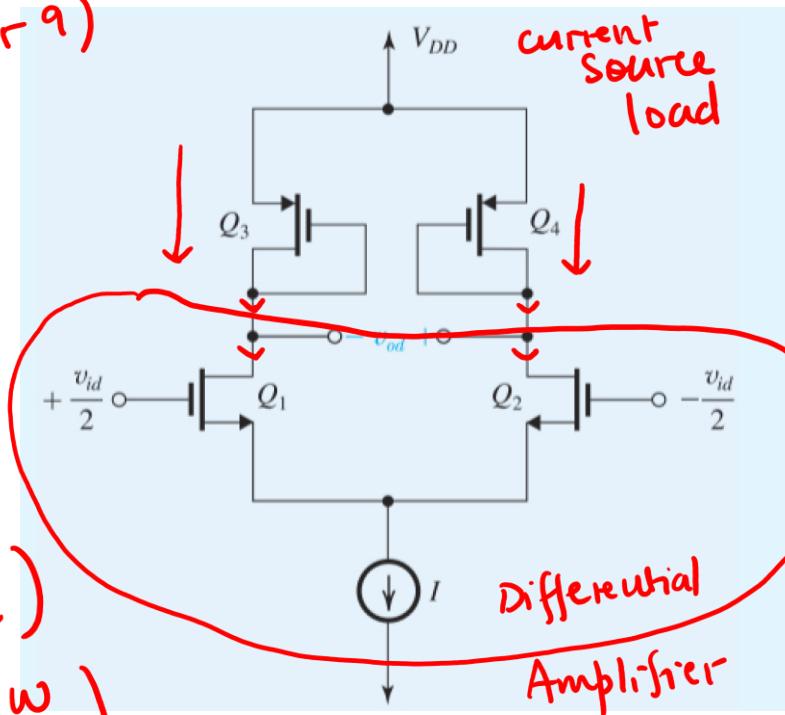
problem 9.19
(Back of chapter 9)

Fig.6 shows a MOS differential amplifier with *diode-connected* PMOS transistors, Q_3 and Q_4 , as loads. Let Q_1 and Q_2 be matched, and Q_3 and Q_4 be matched.

- (a) Find the differential half-circuit and use it to derive an expression for the differential gain A_d in terms of $g_{m1,2}$, $g_{m3,4}$, $r_{o1,2}$, and $r_{o3,4}$.
- (b) Neglecting channel length modulation ($\lambda=0$), find A_d in terms of μ_n , μ_p , $(W/L)_{1,2}$ and $(W/L)_{3,4}$.
- (c) If $\mu_n = 4 \cdot \mu_p$ and all four transistors have the same channel length, find $(W_{1,2}/W_{3,4})$ that results in a differential gain $A_d = 10 \text{ V/V}$.

$$K_n = K_n' \left(\frac{w}{L} \right) = \mu_n C_{ox} \left(\frac{w}{L} \right)$$

$$K_p = K_p' \left(\frac{w}{L} \right) = \mu_p C_{ox} \left(\frac{w}{L} \right)$$



MOS Differential Linear Amplifier – Exercise

$$A_d = \frac{v_{od}}{v_{id}}$$

$$\frac{-v_{od}}{2} = - [g_m \frac{v_{gs1}}{2} (\Gamma_{01}/\Gamma_{03})]$$

$$\frac{v_{od}}{v_{id}} = g_m (\Gamma_{01}/\Gamma_{03}/g_{m3})$$

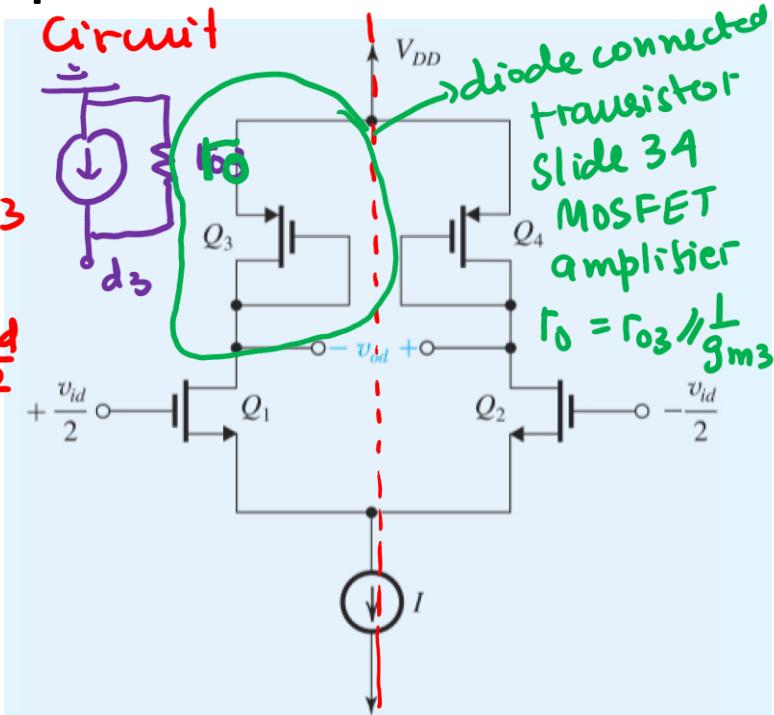
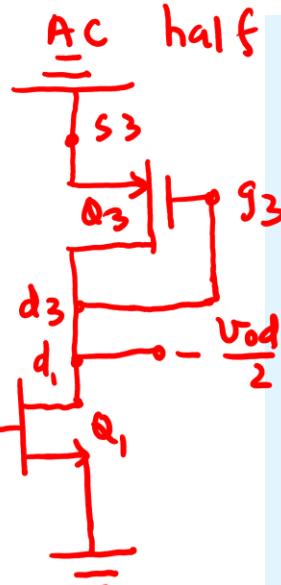
$$A_d = g_m (\Gamma_{01}/\Gamma_{03}/g_{m3}) \frac{v_{id}}{2}$$

Q_1 and Q_2 are matched

$$g_{m1} = g_{m2} \Rightarrow \Gamma_{01} = \Gamma_{02}$$

$\Rightarrow Q_3$ and Q_4 are matched

$$g_{m3} = g_{m4} ; \Gamma_{03} = \Gamma_{04}$$

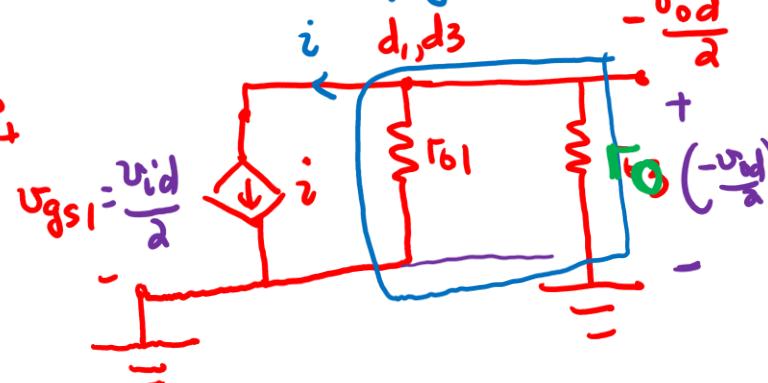


$$A_d = g_{m1,2} \left(\Gamma_{01,2}/\Gamma_{03,4}/g_{m3,4} \right)$$



small signal model

$$i = g_m v_{gs1}$$



Slide #5 - of MOSFET amp

MOS Differential Linear Amplifier – Exercise

$$Ad = \text{Sm}_1 \left(\frac{\Gamma_{01}}{\infty} // \frac{\Gamma_{03}}{\infty} // \frac{1}{\text{Sm}_{3,4}} \right)$$

$$Ad = \frac{g_{m_{1,2}}}{g_{m_{3,4}}} = \frac{g_{m_{1,2}}}{g_{m_{3,4}}}$$

$$A_d = \frac{K_h' \left(\frac{\omega}{L} \right)_{1,2} V_{0U1,2}}{K_p' \left(\frac{\omega}{L} \right)_{3,4} V_{0U3,4}}$$

$$i_D = \frac{1}{2} k_n' \left(\frac{w}{L} \right) V_{00}^2 \Rightarrow V_{0V} = \sqrt{\frac{2 i_D}{k_n' \left(\frac{w}{L} \right)}}$$

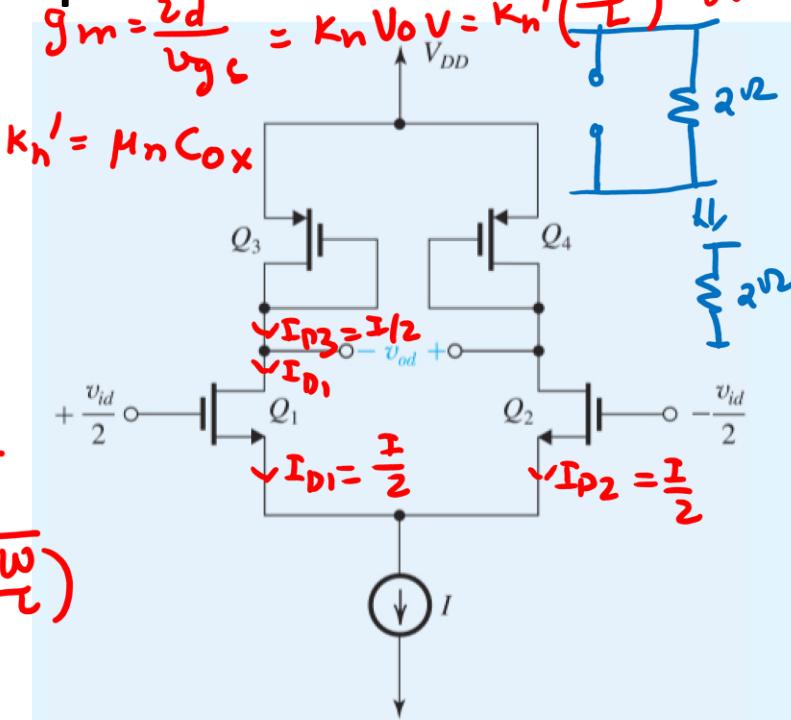
$$A_d = K_n' \left(\frac{w}{L} \right)_{1,2} \sqrt{\frac{\alpha I/X}{K_n' \left(\frac{w}{L} \right)_{1,2}}}$$

$$\frac{K_p' \left(\frac{\omega}{L}\right)_{3,4}}{\sqrt{\frac{2 I/2}{K_p' \left(\frac{\omega}{L}\right)_{3,4}}}}$$

$$Ad = \frac{\int \cancel{K_n} \left(\frac{w}{L} \right)_{1,2}}{\int \cancel{K_p} \left(\frac{w}{L} \right)_{3,4}}$$

$$= \frac{\mu_n C_{0X} \left(\frac{w}{L}\right)_{1,2}}{\mu_p C_{0X} \left(\frac{w}{L}\right)_{3,4}}$$

$$\frac{\sqrt{M_n\left(\frac{w}{L}\right)}_{1,2}}{\sqrt{M_p\left(\frac{w}{L}\right)}_{3,4}}$$



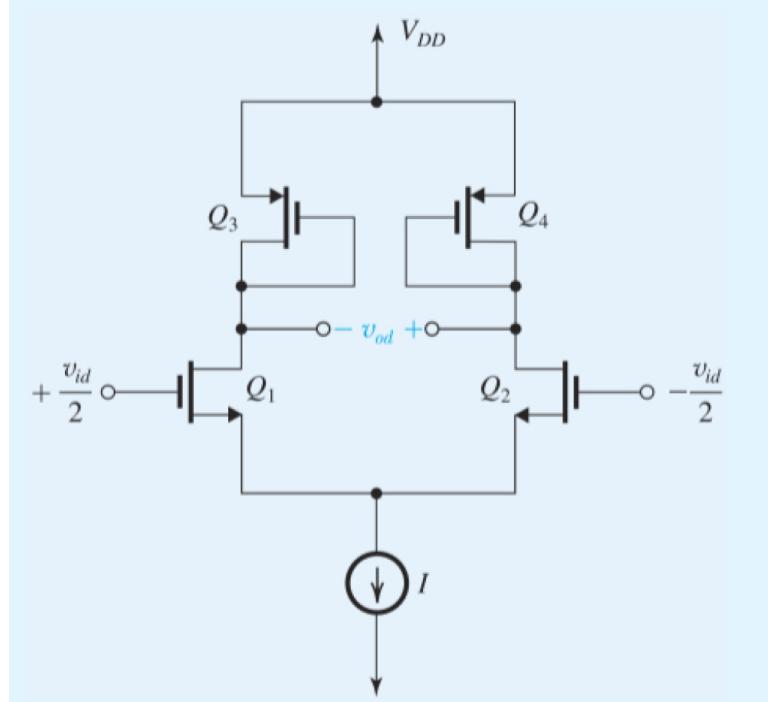
MOS Differential Linear Amplifier – Exercise

(c)

$$I_O = \sqrt{\frac{\mu_n w_{1,2}}{\mu_p w_{3,4}}}$$

$$(I_O)^2 = \frac{4 \mu_p w_{1,2}}{\mu_p w_{3,4}}$$

$$\frac{w_{1,2}}{w_{3,4}} = \frac{100}{4} = 25$$



MOS Differential Linear Amplifier – Exercise

A6.4

Consider the amplifier in Fig. 4. Let $K_n'(W/L)_{1,2} = 2.5 \text{ mA/V}^2$,

$V_t = 0.7 \text{ V}$, and no channel length modulation.

$$[\lambda = 0, r_o \rightarrow \infty]$$

(a) Find the value of V_{DC} .

(b) Find R_D such that $A_v = 8 \text{ V/V}$. $A_d = g_m R_D$ [$R_s \rightarrow \infty$]

(c) Determine the output common-mode voltage $V_{o,CM}$.

(d) Determine the minimum value of $V_{DC,min}$ to ensure M_1 and M_2 operate in saturation.

① DC circuit $\rightarrow \frac{v_s}{2} \rightarrow \text{turned off} = 0$

$$KVL \Rightarrow -V_{DC} + V_{GS1} + (1 \times 1 \text{ mA}) = 0$$

$$V_{DC} = V_{GS1} + 1$$

$$I_{D1} = \frac{1}{2} K_n' \left(\frac{W}{L} \right) \cdot (V_{GS1} - V_t)^2$$

$$0.5 = \frac{1}{2} (2.5) (V_{GS1} - 0.7)^2$$

$$V_{GS1} = 0.7 + \sqrt{\frac{0.5}{2.5}} = 0.7 + 0.632 = 1.33 \text{ V}$$

$$V_{DC} = 1.33 + 1 = 2.33 \text{ V}$$

$V_{DC} \rightarrow \text{CM signal/voltage/i/p}$

$\frac{v_s}{2} \rightarrow \text{differential i/p}$

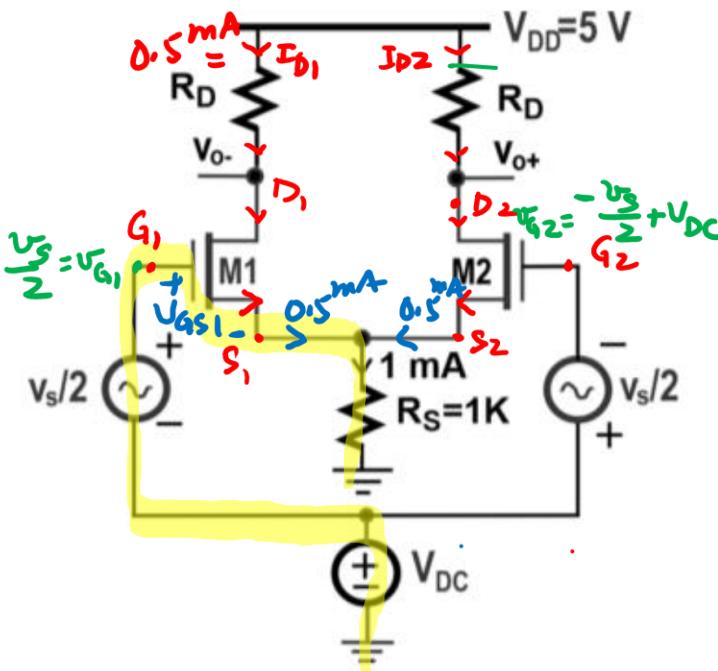


Fig. 4. M_1 and M_2 are NMOS transistors

MOS Differential Linear Amplifier – Exercise

Consider the amplifier in Fig. 4. Let $K_n(W/L)_{1,2} = 2.5 \text{ mA/V}^2$, $V_t = 0.7 \text{ V}$, and no channel length modulation.

(a) Find the value of V_{DC} .

(b) Find R_D such that $A_v = 8 \text{ V/V}$.

AC circuit \rightarrow DC sources OFF

(half circuit)

$$v_o^- = -g_m v_{gs1} R_D$$

KVL \Rightarrow

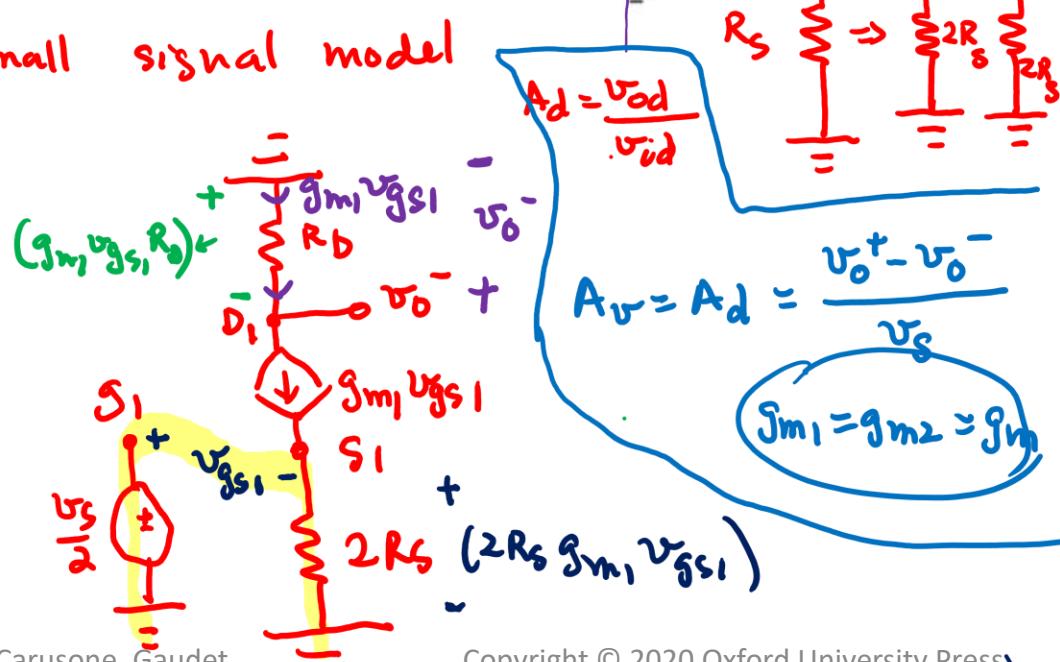
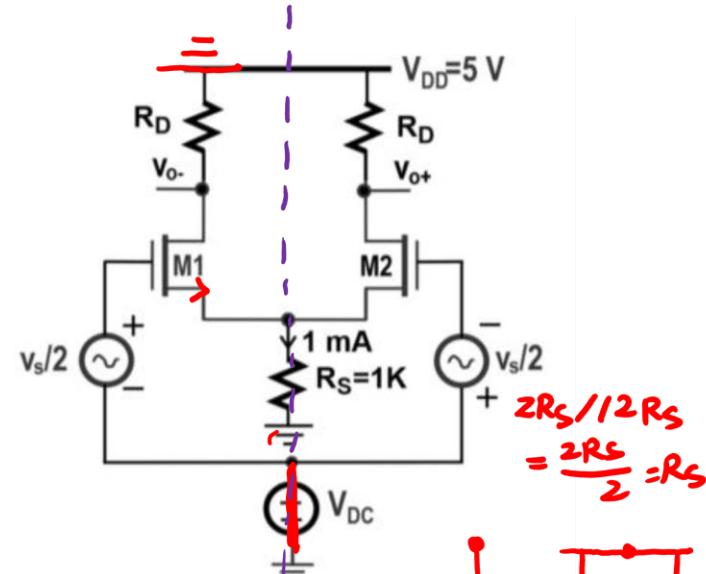
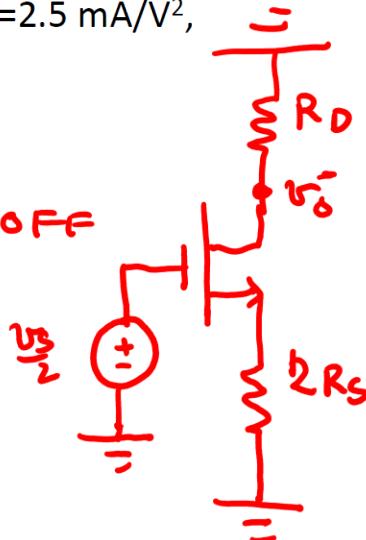
$$\frac{v_s}{2} + v_{gs1} + 2R_s g_m v_{ss1} = 0 \quad \text{small signal model}$$

$$v_{gs1}(1 + 2R_s g_m) = \frac{v_s}{2}$$

$$v_o^- = -g_m R_D \frac{v_s/2}{1 + 2R_s g_m}$$

$$v_o^+ = g_m R_D \frac{v_s/2}{1 + 2R_s g_m}$$

$$A_v = \frac{g_m R_D v_s}{1 + 2R_s g_m} \cdot \frac{1}{v_s}$$



MOS Differential Linear Amplifier – Exercise

Consider the amplifier in Fig. 4. Let $K_n(W/L)_{1,2}=2.5 \text{ mA/V}^2$, $V_t=0.7 \text{ V}$, and no channel length modulation.

- (a) Find the value of V_{DC} .
- (b) Find R_D such that $A_v=8 \text{ V/V}$.

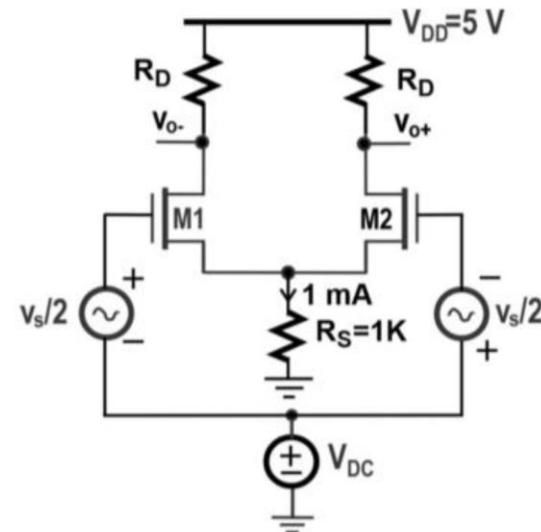
$$A_v = \frac{g_m R_D}{1 + 2 R_S g_m} \Rightarrow R_S = 0 = g_m R_D$$

$$g_m = \frac{2 I_D}{V_{DS}} = \frac{2 \times 0.5}{0.632} = 1.6 \text{ mA/V}$$

$$8 = \frac{1.6 R_D}{1 + 2 \times 1 \times 1.6} \Rightarrow R_D = 21 \text{ k}\Omega$$

if R_S was not considered

$$8 = 1.6 R_D \Rightarrow R_D = 5 \text{ k}\Omega$$

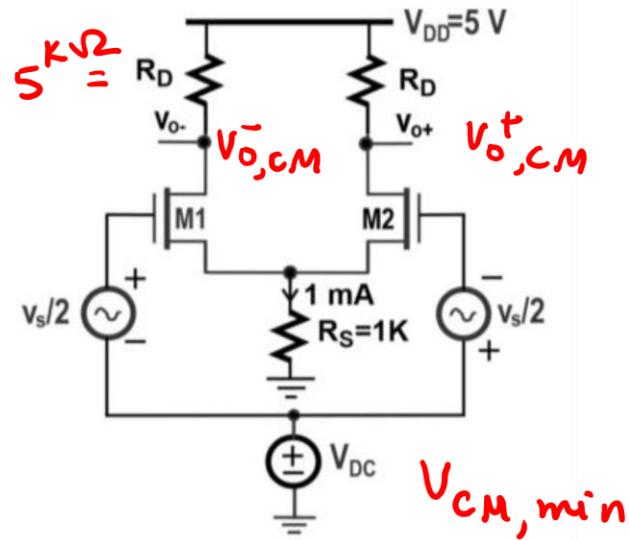


MOS Differential Linear Amplifier – Exercise

- (c) Determine the output common-mode voltage $V_{o,CM}$.
 (d) Determine the minimum value of $V_{DC,min}$ to ensure M_1 and M_2 operate in saturation.

DC circuit

(c) $V_{o,CM} = V_{o,DC} = 5 - (0.5 \times 5)$
 $= 2.5V$



$$V_{DS} \geq V_{GS} - V_{tn}$$



$$V_g - V_s$$



$$V_{CM}$$

MOS Differential Amplifiers – Common Mode Gain and Common Mode Rejection

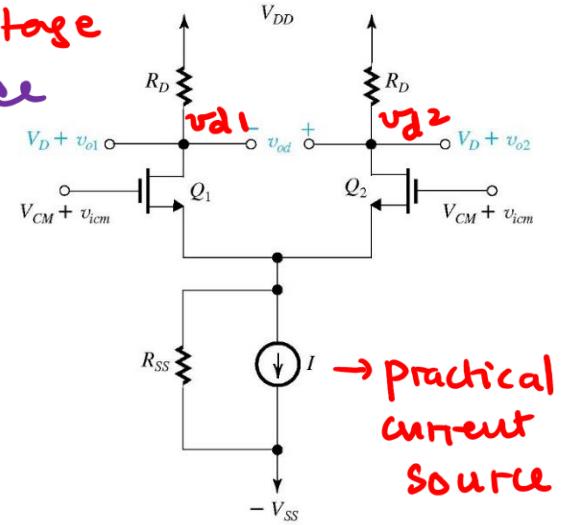
$$v_{od} = v_{d2} - v_{d1}$$

$v_{icm} \rightarrow$ ac common mode i/p voltage
[example : interference]
 $v_{o2} \leftarrow v_{icm} @ Q_2$ (noise)
 $v_{o1} \leftarrow v_{icm} @ Q_1$

$v_D @ d_2$ is from $v_{cm} @ G_2$

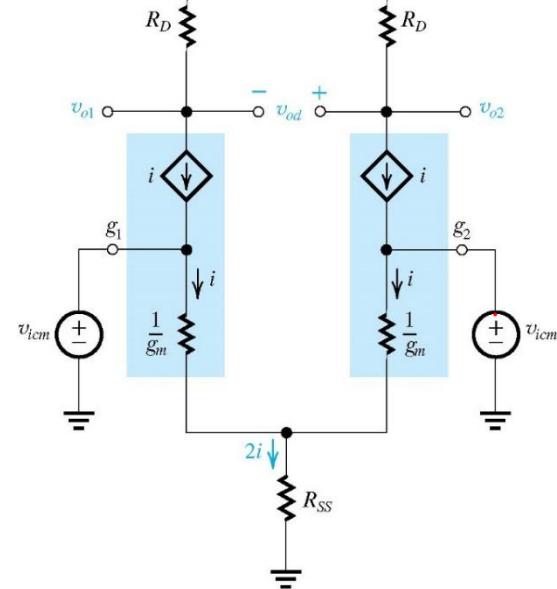
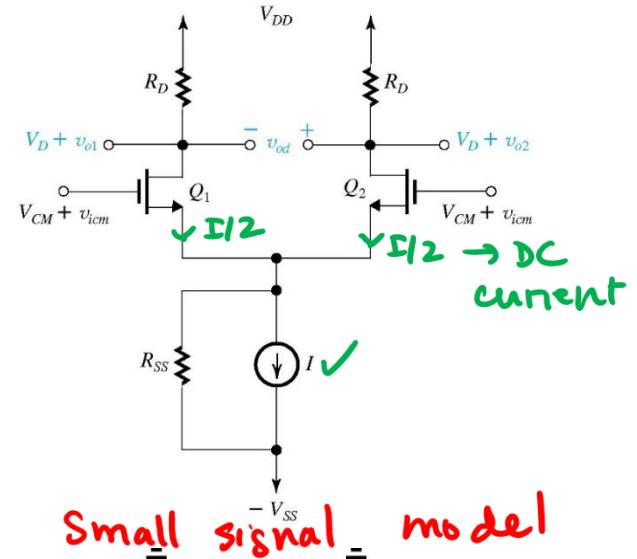
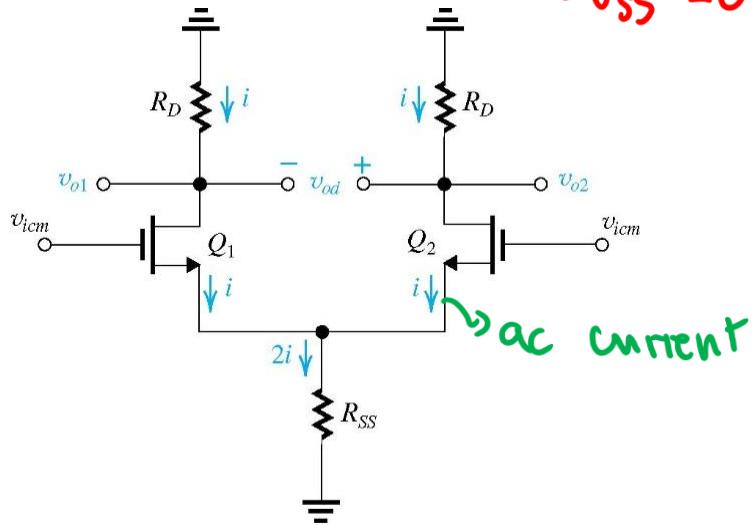
$v_D @ d_1$ is from $v_{cm} @ G_1$

objective \rightarrow how much of v_{icm} makes its way to the amplifier o/p [measure]



MOS Differential Amplifiers – Common Mode Rejection

AC circuit $\rightarrow I \rightarrow OFF ; V_{CM} = 0$
 $V_{SS} = 0$



MOS Differential Amplifiers – Common Mode Rejection

$\kappa v L \Rightarrow$

- $v_{icm} = \frac{i}{g_m} + 2iR_{SS}$
- $i = \frac{v_{icm}}{\left(\frac{1}{g_m}\right) + 2R_{SS}}$
- $v_{o1} = v_{o2} = -R_D i = -\frac{R_D}{\left(\frac{1}{g_m}\right) + 2R_{SS}} v_{icm}$

- $\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{2R_{SS}}$ $\left(2R_{SS} \gg \frac{1}{g_m}\right)$

single ended gain

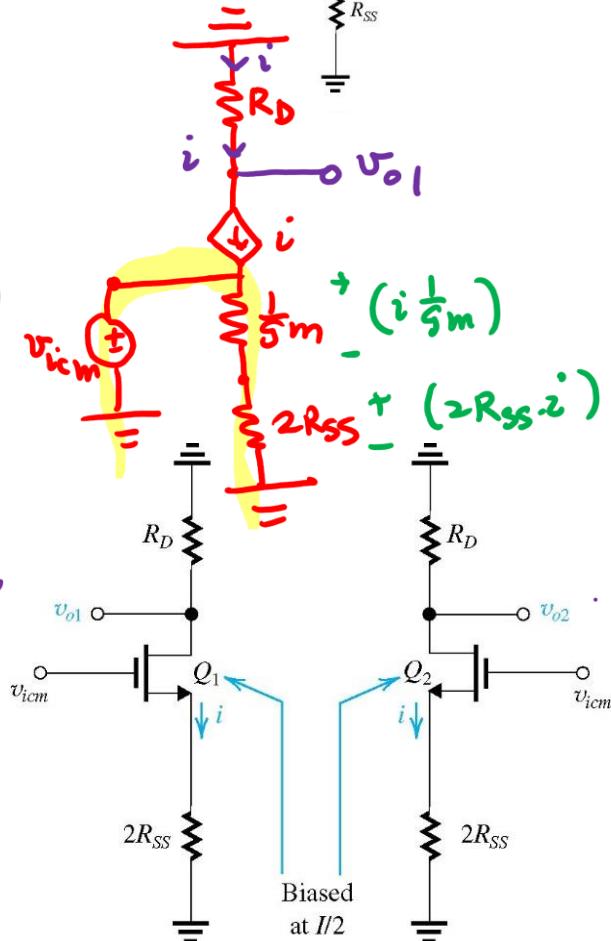
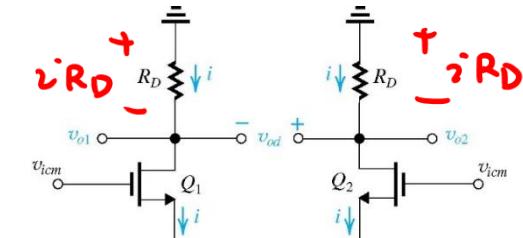
$$A_{CM,SE} = \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}}$$

if R_{SS} is large

$$A_{CM,SE} \approx 0$$

$$v_{od} = v_{o2} - v_{o1} = 0$$

$$A_{CM,d} = 0$$



MOS Differential Amplifiers – Common Mode Rejection

- Effect of R_D mismatch: $v_{icm} = \frac{i}{g_m} + 2iR_{SS}$

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{2R_{SS}}$$

$$v_{o1} = -\frac{R_D}{2R_{SS}} v_{icm}$$

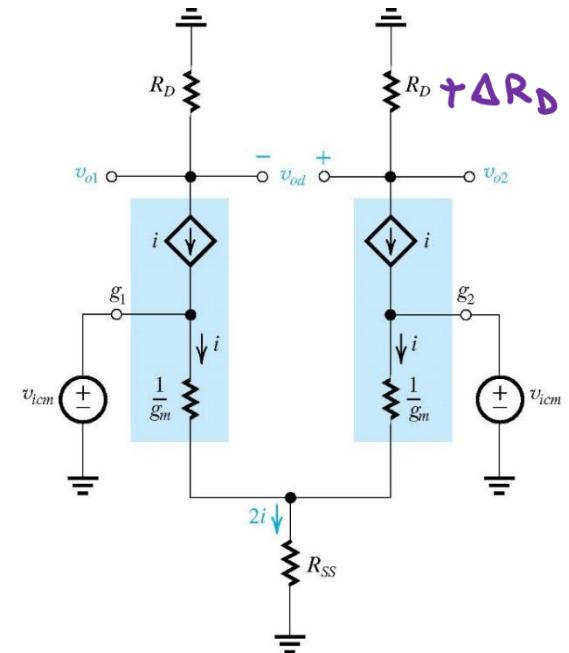
$$v_{o2} = -\frac{(R_D + \Delta R_D)}{2R_{SS}} v_{icm}$$

- The Common mode Gain:

$$A_{cm} = \frac{v_{od}}{v_{icm}} = \frac{v_{o1} + v_{o2}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}} = -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right)$$



Differential gain due to CM signal



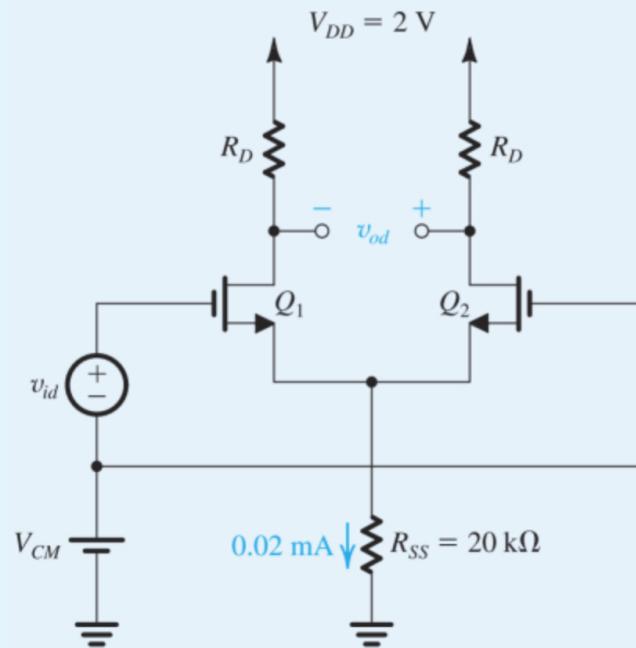
MOS Differential Amplifiers – Common Mode Rejection

- Common-Mode Rejection Ratio (CMRR) – Measure of the effectiveness of the differential amplifier in amplifying differential-mode signals and rejecting common-mode interference
- $$\text{CMRR} = \frac{|A_d|}{|A_{cm}|}$$
 large ← CMRR
- $$\text{CMRR (dB)} = 20 \log \frac{|A_d|}{|A_{cm}|}$$
- $$\text{CMRR} = \frac{(2g_m R_{SS})}{\left(\frac{\Delta R_D}{R_D}\right)}$$
- $$\text{CMRR} = \frac{(2g_m R_{SS})}{\left(\frac{\Delta g_m}{g_m}\right)}$$

MOS Differential Amplifiers – Common Mode Rejection - Exercise

SIM D *9.57 The differential amplifier in Fig. P9.57 utilizes a resistor R_{SS} to establish a 0.02-mA dc bias current. Note that this amplifier uses a single 2-V supply and thus the dc common-mode voltage V_{CM} cannot be zero. Transistors Q_1 and Q_2 have $k'_n W/L = 1\text{mA/V}^2$, $V_t = 0.4\text{ V}$, and $\lambda = 0$.

- Find the required value of V_{CM} .
- Find the value of R_D that results in a differential gain A_d of 15 V/V.
- Determine the dc voltage at the drains.
- Determine the single-ended-output common-mode gain $\Delta V_{D1}/\Delta V_{CM}$. ([Hint](#))
- Use the common-mode gain found in (d) to find the change in V_{CM} that results in Q_1 and Q_2 entering the triode region.



MOS Differential Amplifiers – Common Mode Rejection -

Exercise

(a) $V_{CM} \rightarrow \text{dc value} \rightarrow \text{DC circuit}$

$$v_{id} = 0$$

$$I_{D1} = 0.01 \text{ mA} = \frac{1}{2} k_n' \left(\frac{w}{L} \right)_1 \left(V_{GS1} - V_t \right)^2$$

$$V_{GS1} = 0.4 + \sqrt{\frac{2 \times 0.01}{1}} = 0.54 \text{ V}$$

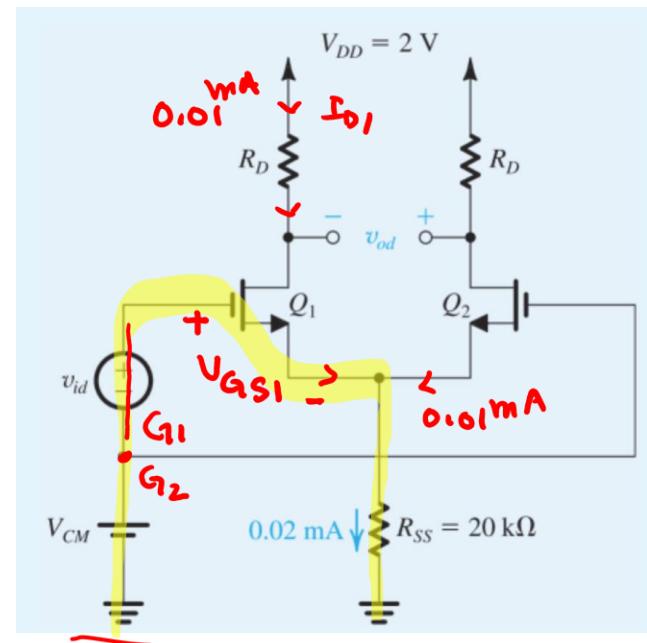
$$\text{KVL} \Rightarrow -V_{CM} + V_{GS1} + 0.02 \times 20 = 0$$

$$V_{CM} = 0.54 + 0.4 = 0.94 \text{ V}$$

(b) $A_d = 15 \text{ V/V} = g_m R_D \Rightarrow [\text{ignoring impact of } R_{SS}]$

$$g_m = \frac{\partial I_{D1}}{\partial V_{GS1}} = \frac{2 \times 0.01}{0.14} = 0.143 \text{ mA/V}$$

$$15 = 0.143 R_D \Rightarrow R_D = 107 \text{ k}\Omega$$



MOS Differential Amplifiers – Common Mode Rejection - Exercise

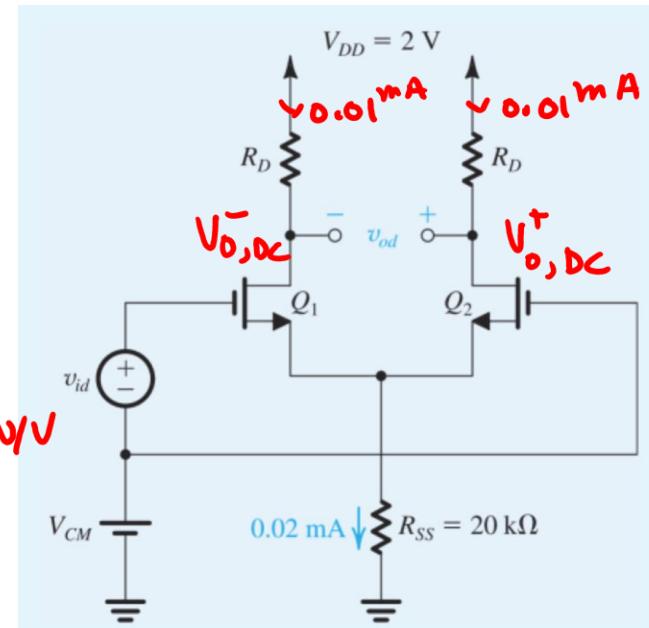
(c)

$$\underline{V_{O,DC}^-} = \underline{V_{O,DC}^+} = 2 - [0.01 \times 107] = \underline{0.93V}$$

(d)

$$A_{CM,SE} = \frac{\Delta V_{DI}}{\Delta V_{CM}} = -\frac{R_D}{\frac{1}{g_m} + 2R_{SS}}$$

$$A_{CM,SE} = \frac{-107}{\frac{1}{0.143} + 2 \times 20} = -2.26 \text{ V/V}$$



$$V_{CM} = V_{CM} + \Delta V_{CM}$$

$$V_{DI} = V_{DI,DC} + \Delta V_{DI}$$

MOS Differential Amplifiers – Common Mode Rejection - Exercise

(e)

Q_1 and Q_2 leaving the Saturation region

$$V_{DS} > V_{GS} - V_{tn}$$

$$V_D - V_S \geq V_G - V_S - V_{tn}$$

$$V_D \geq V_G - V_{tn}$$

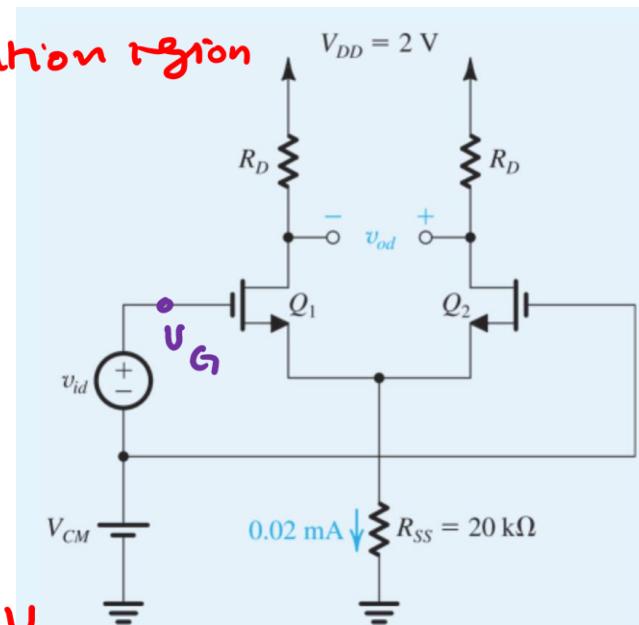
$$V_G - V_{tn} \leq V_D$$

$$V_{CM} + \Delta V_{CM} - V_{tn} \leq V_D + \Delta V_D$$

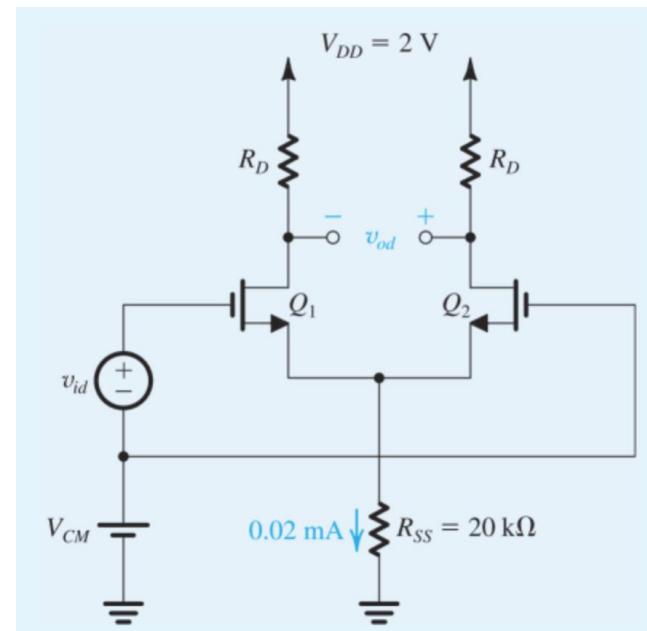
$$\Delta V_{CM} = \frac{V_D + \Delta V_D + V_{tn} - V_{CM}}{0.93 + 0.4 - 0.94} = -2.26$$

$$\frac{\Delta V_D}{\Delta V_{CM}} = -2.26$$

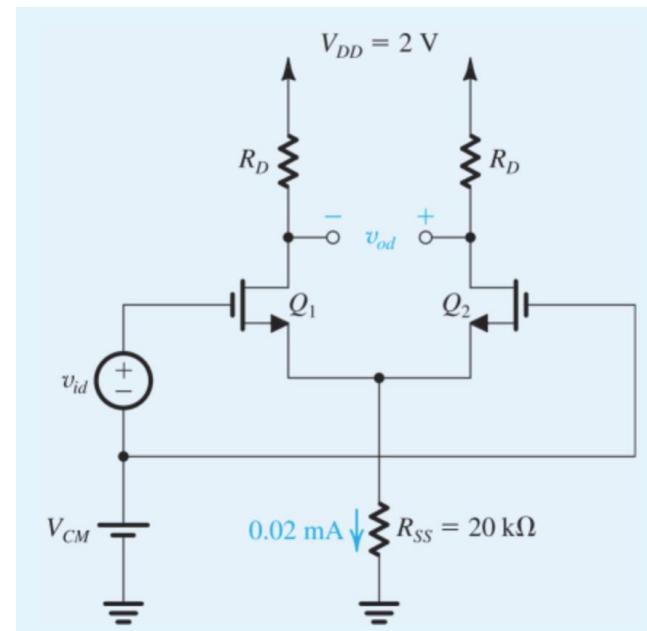
~~$$\Delta V_{CM} (1 + z) = \frac{0.93 + 0.4 - 0.94}{3.26} = 0.12 \text{ V/V}$$~~



MOS Differential Amplifiers – Common Mode Rejection - Exercise



MOS Differential Amplifiers – Common Mode Rejection - Exercise



MOS Differential Linear Amplifier – Exercise

A6.1

Consider the amplifier in Fig. 1. Neglect channel length modulation. Assume I , R_D , and W/L are known, and M_1/M_2 are matched and operate in saturation. Derive expressions for:

- The currents I_{DS1} and I_{DS2} .
- The overdrive voltages V_{OD1} and V_{OD2} .
- The differential gain A_v .

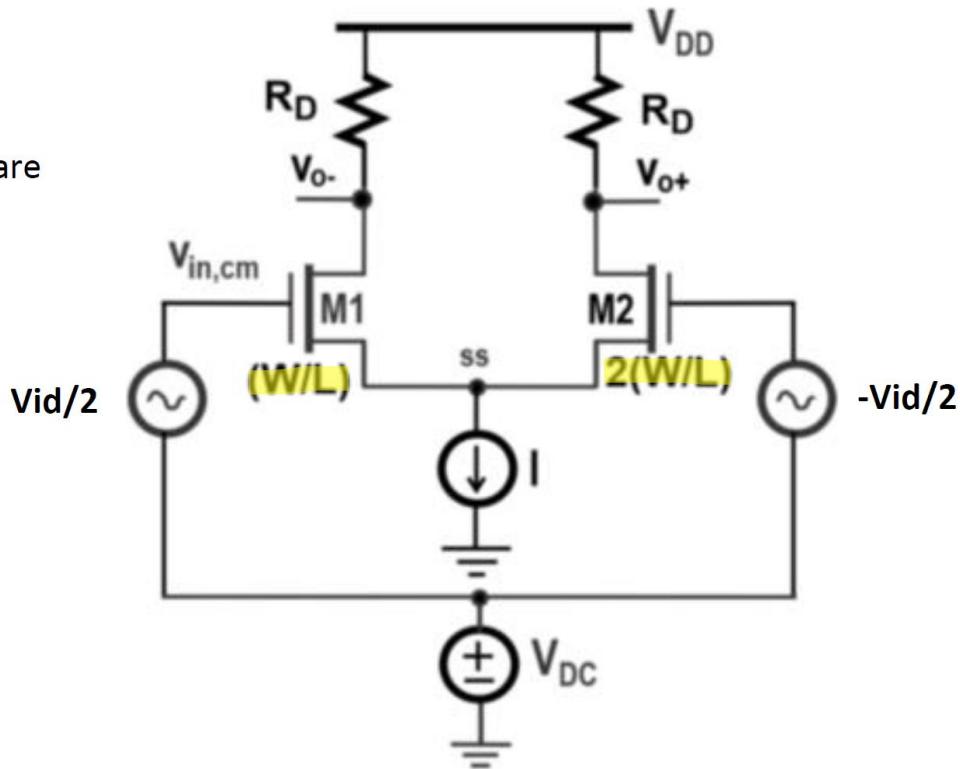


Fig. 1. M_1 and M_2 are NMOS transistors

MOS Differential Linear Amplifier – Exercise

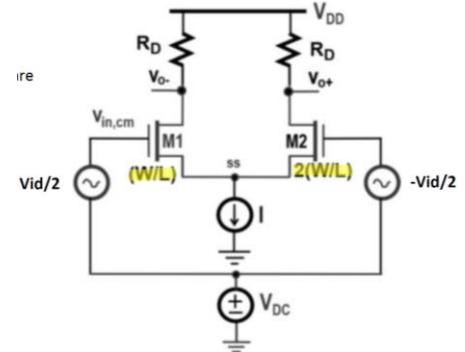


Fig. 1. M_1 and M_2 are NMOS transistors

MOS Differential Linear Amplifier – Exercise

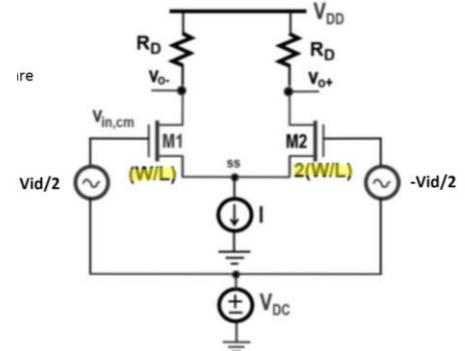


Fig. 1. M_1 and M_2 are NMOS transistors

MOS Differential Linear Amplifier – Exercise

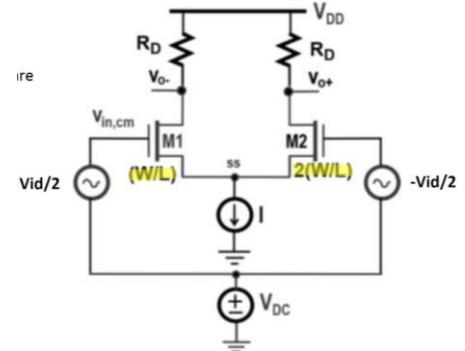


Fig. 1. M_1 and M_2 are NMOS transistors