VLSI_Lab_1-2

SYNTHESIS

Environment

- source Design Compiler
  - tool 2
- 編輯 .synopsys_dc.setup

```
set company {NTUGIEE}
set designer {Student}

set search_path [concat  [list . /opt/CAD/cell_lib/CBDK_IC_Contest_v2.1/SynopsysDC/db ../design] $search_path]
set link_library [list "dw_foundation.sldb" "typical.db" "slow.db" "fast.db"]
set target_library [list "typical.db" "slow.db" "fast.db"]
set symbol_library [list "generic.sdb"]
set synthetic_library [list "dw_foundation.sldb"]
set default_schematic_options {-size infinite}

set hdlin_translate_off_skip_text "TRUE"
set edifout_netlist_only "TRUE"
set verilogout_no_tri true
set plot_command {lpr -Plw}
set hdlin_auto_save_templates "TRUE"
set compile_fix_multiple_port_nets "TRUE"
```

Scripts

- 打開run_sv.tcl 或 run_all_v.tcl 理解裡面的內容

```
# Import Design
analyze -format sverilog -define OLD_VERILOG_STYLE Rgb888ToYuv422.sv
elaborate Rgb888ToYuv422
link

# You can only modify clock period
set cycle 10
set t_in [expr $cycle/2]
set t_out  0.5

# Constraint setting
# Clock constraints
create_clock -name clk -period $cycle [get_ports clk]
set_fix_hold                          [get_clocks clk]
set_dont_touch_network                [get_clocks clk]
set_ideal_network                     [get_ports clk]
set_dont_touch_network                [get_ports rst]
set_ideal_network                     [get_ports rst]
set_clock_uncertainty           0.1   [get_clocks clk]
set_clock_latency               0.5   [get_clocks clk]
```

Run Scripts

- 如果是寫System Verilog, 執行
  - dv -f run_sv.tcl
- 如果是寫Verilog, 執行
  - dv -f run_all_v.tcl

Timing

- 確認slack是不是 ≥ 0

```
                                                          0.00       10.06 f
DP1/U25/Y (NAND2X1)                                       0.10       10.16 r
DP1/U23/Y (NAND3X1)                                       0.10       10.26 f
DP1/o_data_reg_4_/D (DFFRX1)                              0.00       10.26 f
data arrival time                                                    10.26

clock clk (rise edge)                                    10.00       10.00
clock network delay (ideal)                               0.50       10.50
clock uncertainty                                        -0.10       10.40
DP1/o_data_reg_4_/CK (DFFRX1)                             0.00       10.40 r
library setup time                                       -0.14       10.26
data required time                                                   10.26
-----------------------------------------------------------------------------
data required time                                                   10.26
data arrival time                                                   -10.26
-----------------------------------------------------------------------------
slack (MET)                                                          0.00
```

Area

- 確認面積大小
  - Net Interconnect area 不準確，看Total cell area

```
Number of ports:                         1106
Number of nets:                          5517
Number of cells:                         4124
Number of combinational cells:           3933
Number of sequential cells:               161
Number of macros/black boxes:               0
Number of buf/inv:                        954
Number of references:                      13

Combinational area:              46238.873217
Buf/Inv area:                     5973.150548
Noncombinational area:            4766.299053
Macro/Black Box area:                0.000000
Net Interconnect area:          405628.717102

Total cell area:                 51005.172270
Total area:                     456633.889372
```

Gate-level Simulation

- 進入sim資料夾, 輸入指令
  - make SYN=true top
- 看到PASS代表成功!可以進行APR繞線!

```
==================================================================
Scoreboard Reports
------------------------------------------------------------------
Status of [Y]: (correct/error): 1/0
Status of [U]: (correct/error): 1/0
Status of [V]: (correct/error): 1/0
PASS
------------------------------------------------------------------
Simulation complete via $finish(1) at time 533100 PS + 1
./Rgb888ToYuv422_test.sv:17 `WithFinish
ncsim> exit
```

ARP

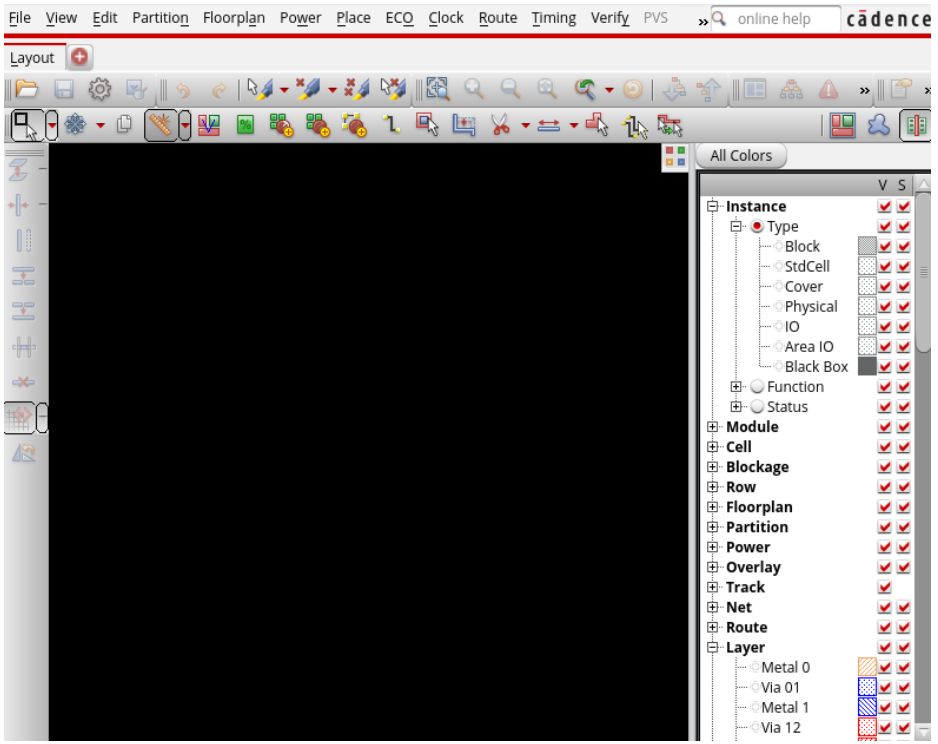
春花秋月何時了，按鈕知多少

洛陽親友如相問，就說我在按按鈕

少壯不努力，老大按按鈕

開啟Innovus GUI介面

- tool 19
- 進入apr資料夾
- innovus (不用加&)



APR

- 請按照Lab1_APR.pdf的步驟完成

Post-layout Simulation

- 拿產生的Rgb888ToYuv422_pr.v做Post-layout simulation
- 改動 design/Rgb888ToYuv42.sv 下 include “Rgb888ToYuv42_syn.v” 的路徑為“ Rgb888ToYuv422_pr.v “
- sim/Rgb888ToYuv422_test.sv 加入 $sdf_annotate("YOUR SDF", dut.u_old_style_verilog_wrapper);
- Makefile no timing check 那行換成 +ncmaxdelays
- 執行 make SYN=true top