Lab1 APR

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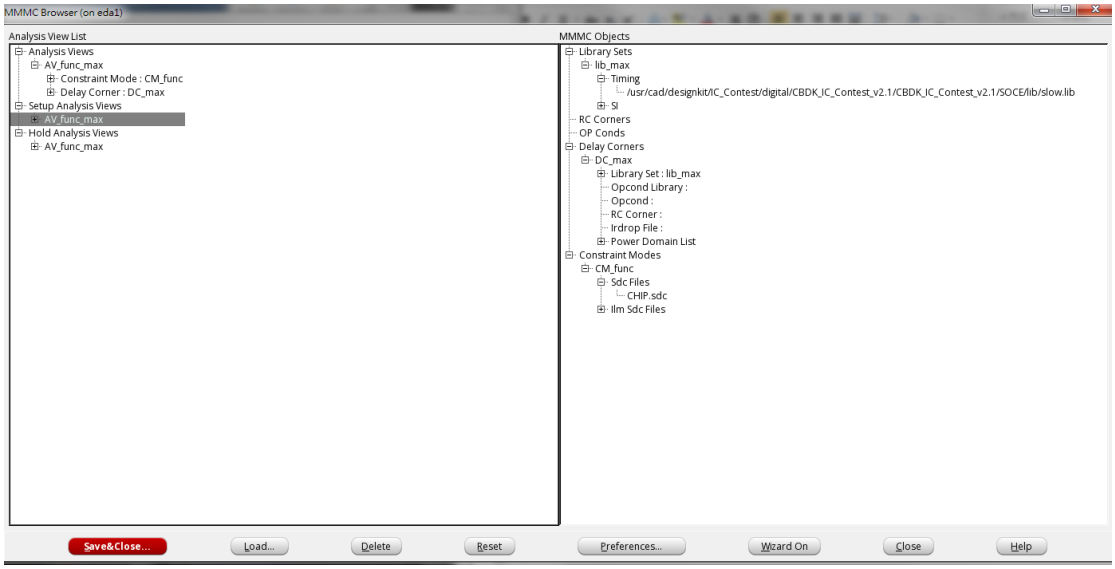
開啟 Innovus GUI 介面

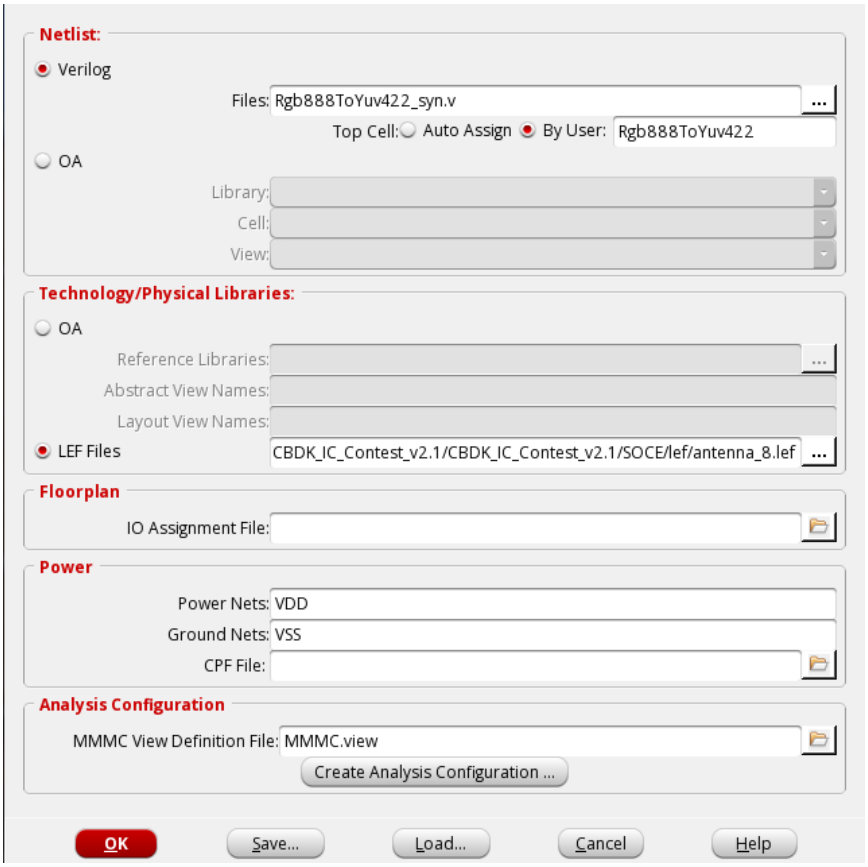
1. unix%　source /usr/cad/cadence/CIC/innovus.cshrc
2. unix%　innovus

Import Design

3. File→Import Design
4. Netlist 選 Verilog，Files 放入合成好的.v 檔，Top Cell 填入最上層的 module (Rgb888ToYuv422)
5. 找到製程資料夾(???/CBDK_IC_Contest_v2.1/SOCE/lef) ， 點選 tsmc13fsg_8lm_cic.lef、antenna_8.lef，close
6. Power : VDD, Ground : VSS
7. 點選 Create Analysis Configuration，如下圖設定，點選 Save & Close

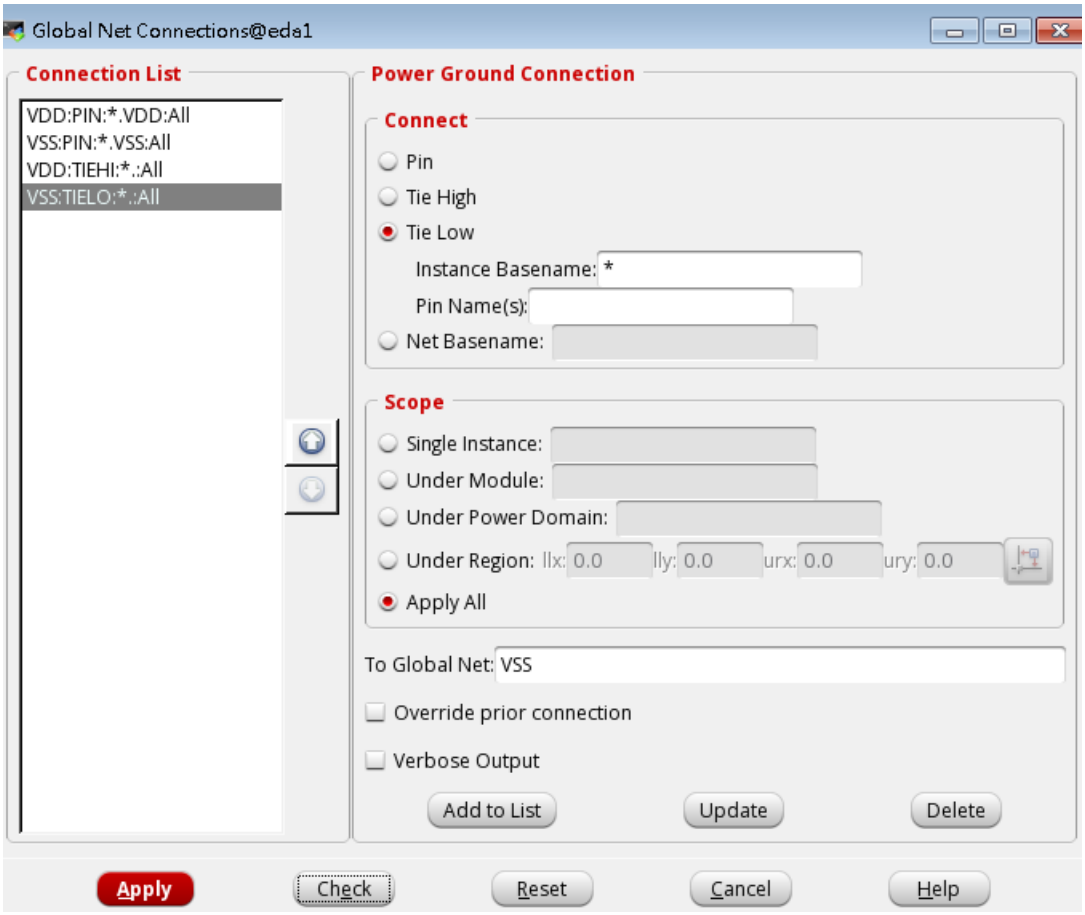


8. 確認與下圖相同後，按 OK



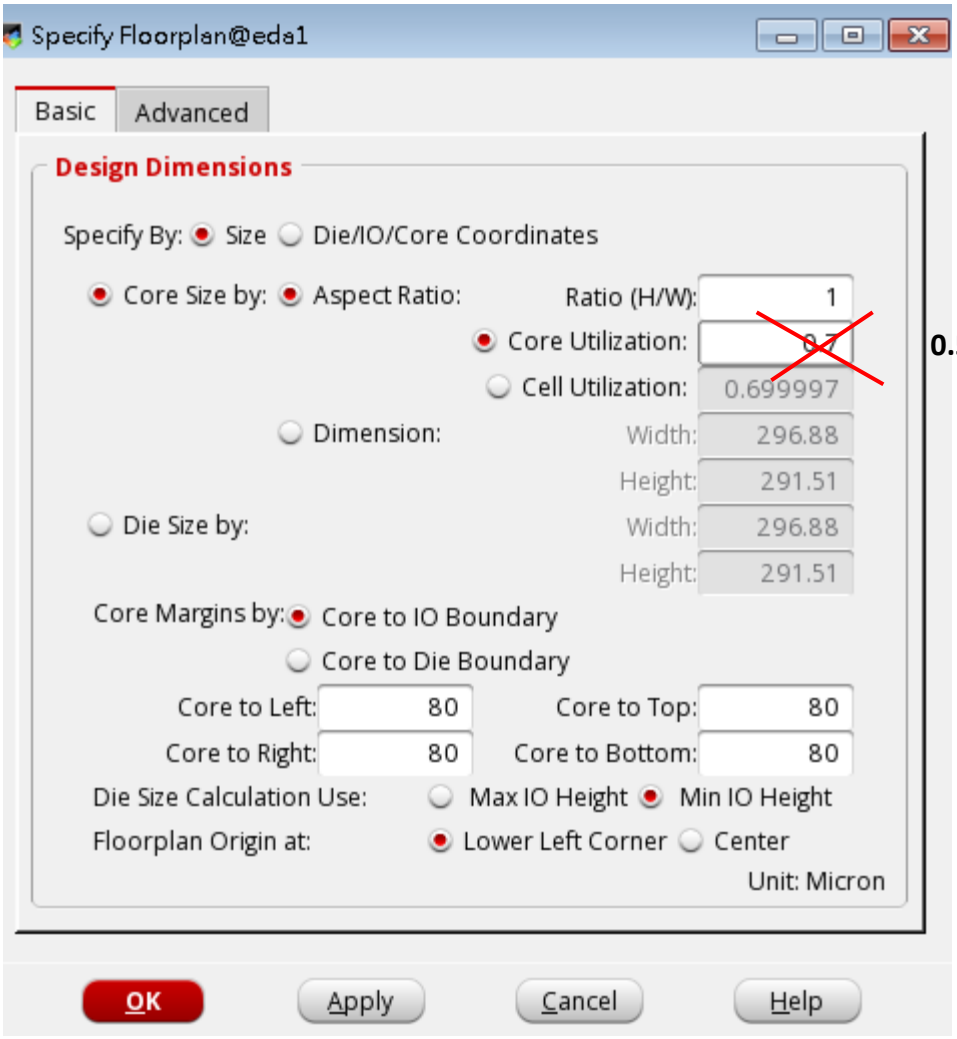
Global Net Connect

9. Power → Connect Global Net
10. Connect: Pin Name VDD, Scope: Apply All, To Global Net: VDD → Add to List
11. Connect: Pin Name VSS, Scope: Apply All, To Global Net: VSS → Add to List
12. Connect: TIEHI, Scope: Apply All, To Global Net: VDD → Add to List
13. Connect: TIELO, Scope: Apply All, To Global Net: VSS → Add to List
14. Apply → Check (可能有 error，但可忽略) → Cancel



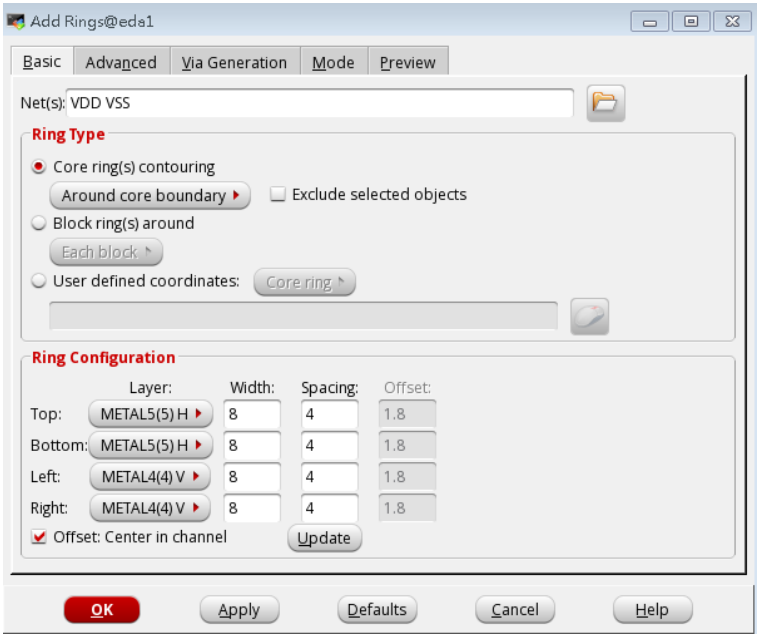
Floorplan

15. Floor plan → Specify Floorplan
16. 如下圖設定→按 OK

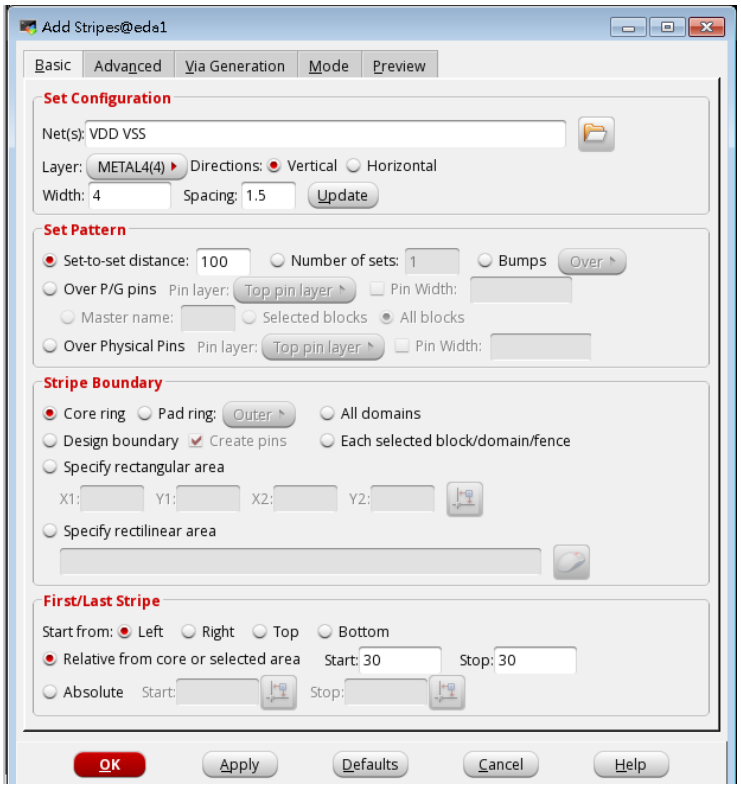


Powerplan

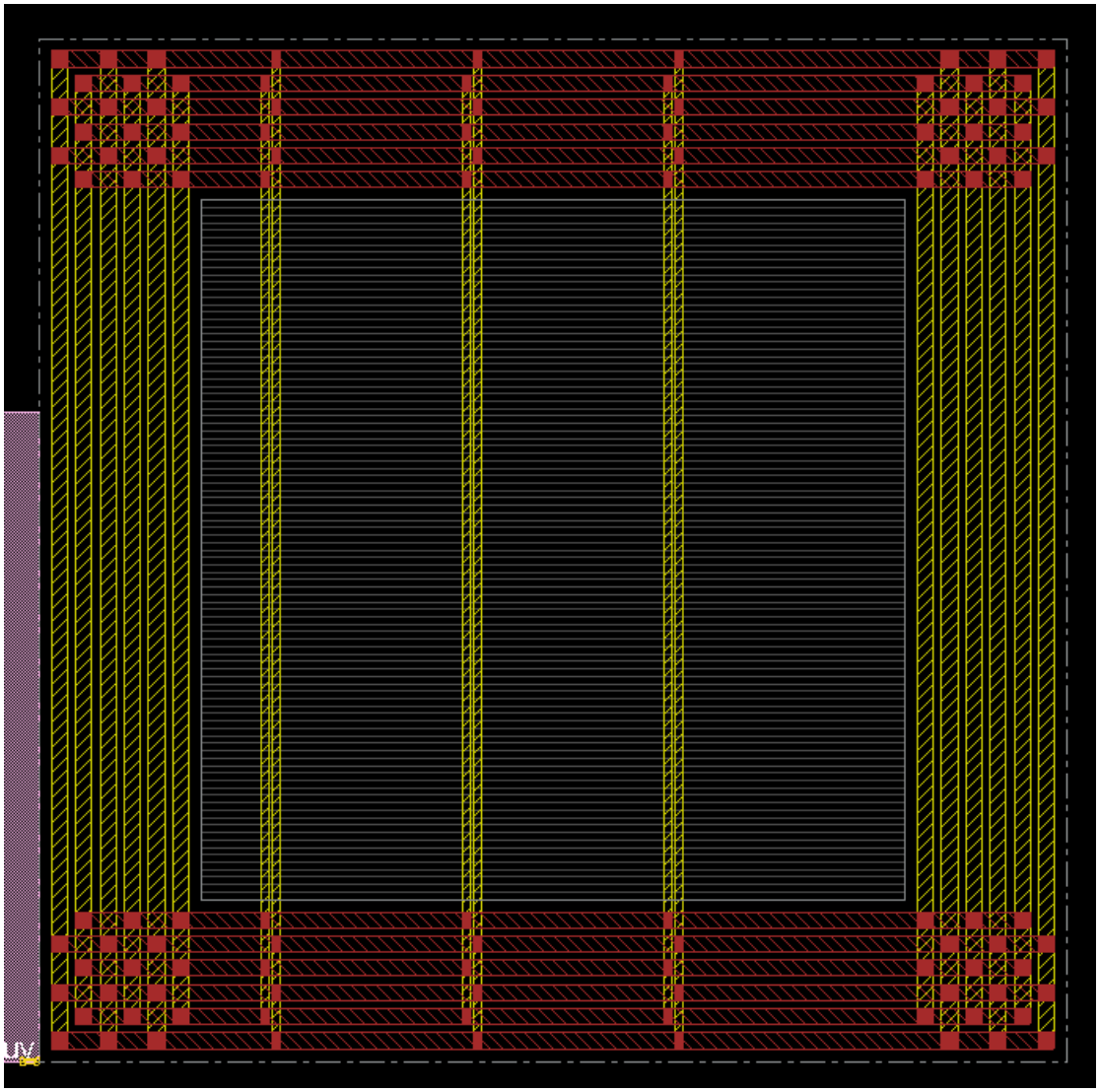
17. Power → Power Planning → Add Ring
18. 如下圖設定



19. 點選 Advanced，勾選 Use wire group，勾選 Interleaving，Number of bits: 3
20. OK
21. Power → Power Planning → Add Stripe
22. 如下圖設定



23. 按 OK，應見到結果如下圖

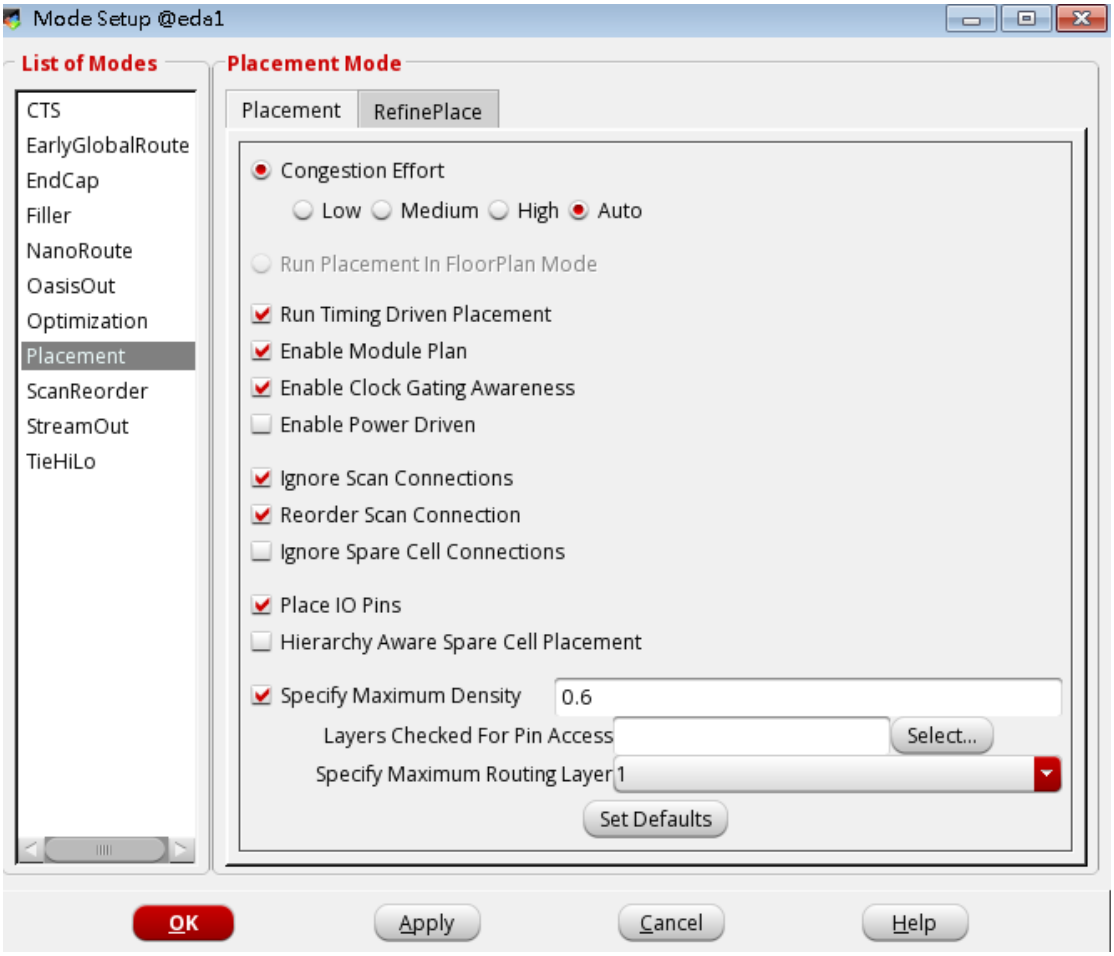


24. Route → Special Rout

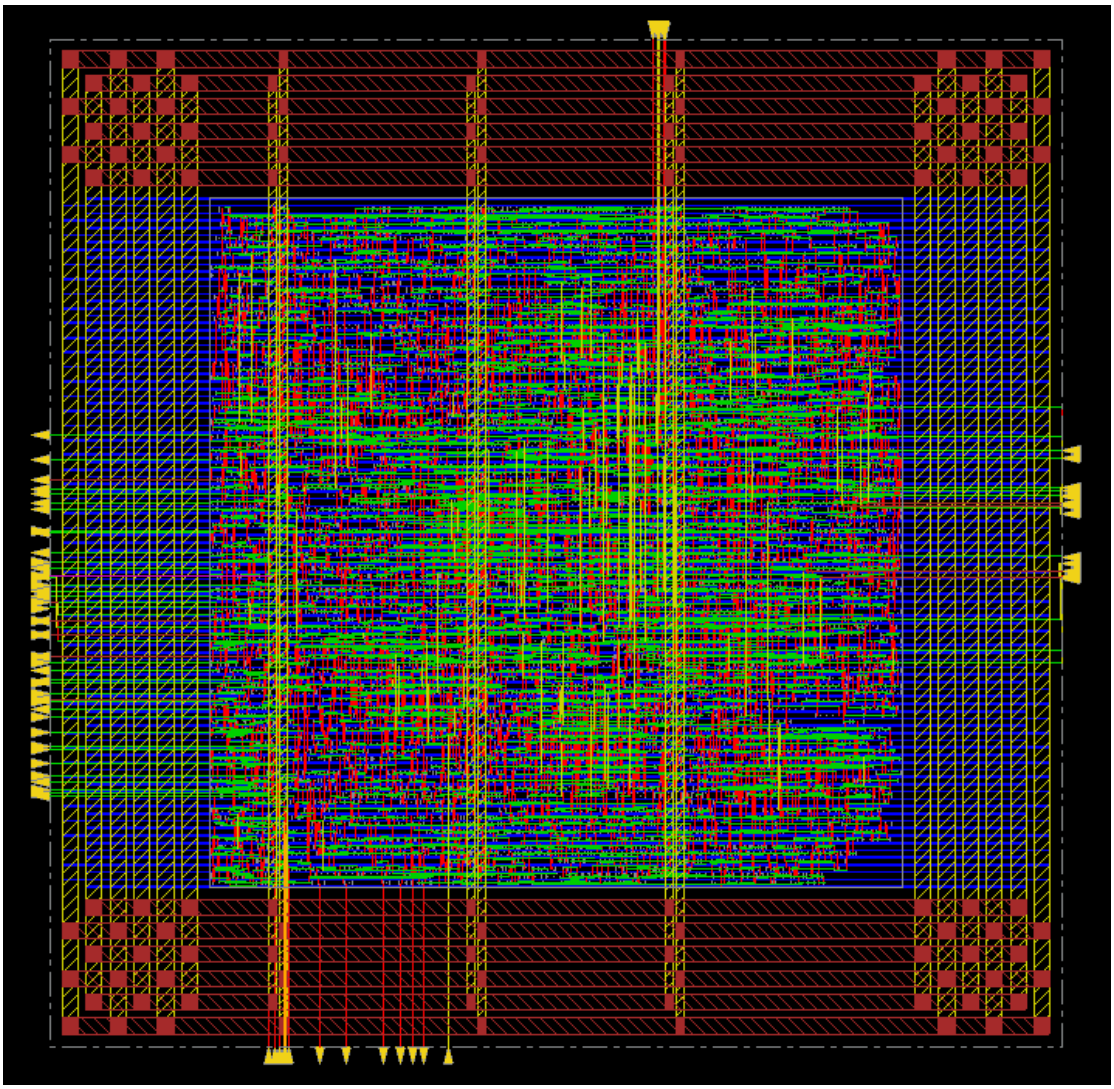
25. Net: VDD VSS, SRout 只勾選 Follow Pins→OK

Placement

26. Place → Place Standard Cells
27. 點選 Mode，勾選 Place IO Pins，勾選 Specify Maximum Density，填入 0.6→OK



28. OK
29. 點選 Physical View，應看到結果類似下圖



30. Place → Check Placement，應要 0 error
31. Timing → Report Timing，Design Stage 選 Pre-CTS → OK
32. 若 WNS < 0 ，執行 ECO → Optimize Design, Design Stage 選 Pre-CTS → OK

Clock Tree Synthesis

33. 將提供的 set_ccopt_property.tcl 放到跑 innovus 的目錄下，其中包含下列三行
    (1) set_ccopt_property buffer_cells { CLKBUF_X1 CLKBUF_X2 CLKBUF_X3 }
    (2) set_ccopt_property clock_gating_cells { CLKGATE_X1 CLKGATE_X2 CLKGATE_X4 CLKGATE_X8 }
    (3) set_ccopt_property update_io_latency false
34. innovus> source set_ccopt_property.tcl
35. innovus> create_ccopt_clock_tree_spec –file ccopt.spec
36. innovus> source ccopt.spec
37. innovus> ccopt_design –cts
38. Timing → Report Timing，Design Stage 選 Post-CTS → OK
39. 若 WNS < 0 ，執行 ECO → Optimize Design, Design Stage 選 Post -CTS → OK
40. Timing → Report Timing，Design Stage 選 Post-CTS，Analysis Type 選 Hold → OK
41. 若 WNS < 0 ，執行 ECO → Optimize Design, Design Stage 選 Post –CTS，勾選 Hold → OK

Route

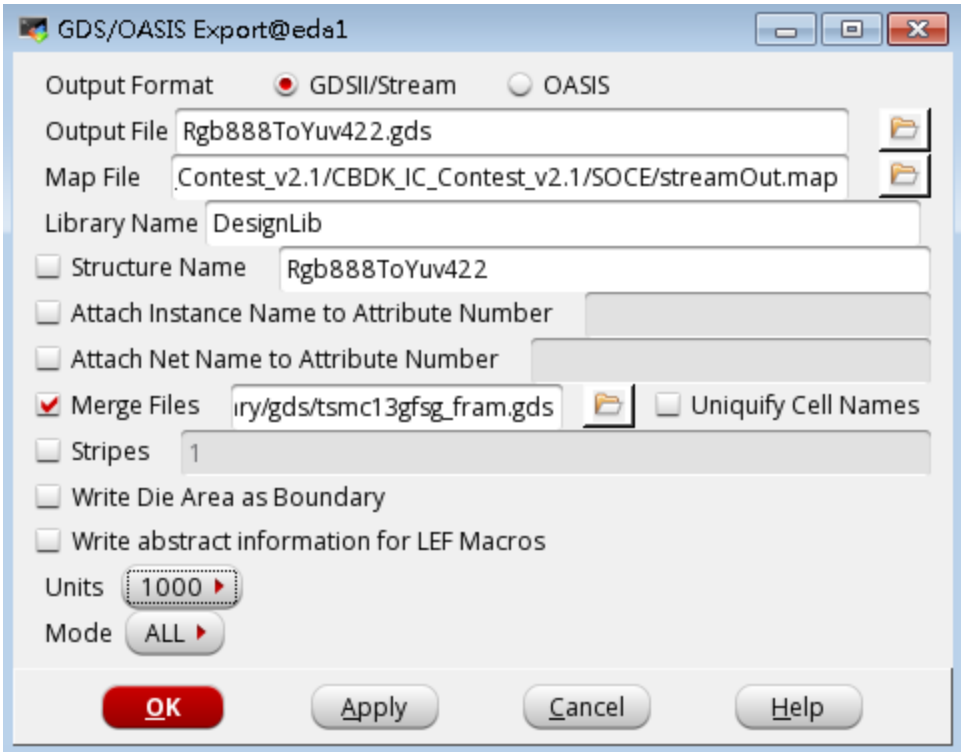
42. Route → NanoRoute → Route
43. 勾選 Optimize Wire、Optimize Via、 Timing Driven→ OK
44. Tool → set Mode → Specify Analysis Mode，Timing Mode 選 On-Chip Variation，勾選 CPPR
45. Timing → Report Timing，Design Stage 選 Post-Route → OK
46. 若 WNS < 0 ，執行 ECO → Optimize Design, Design Stage 選 Post-Route → OK
47. Timing → Report Timing，Design Stage 選 Post-CTS，Analysis Type 選 Hold → OK
48. 若 WNS < 0 ，執行 ECO → Optimize Design, Design Stage 選 Post –CTS，勾選 Hold → OK

Add Core Filler

49. Place → Physical Cells → Add Filler，Cell Name 欄點選 Select 把所有右邊的 cell Add 到左邊的 list 中→ close → OK
50. Verify → Verify Geometry → OK ，應要 0 error
51. Verify → Verify Connectivity → OK，應要 0 error

Save Netlist, SDF & Stream Out

52. File → Save → Netlist，Netlist File 填入 Rgb888ToYuv422_pr.v
53. innovus > write_sdf -max_view AV_func_max Rgb888ToYuv422_pr.sdf
54. File → Save → GDS/OASIS
55. 如下圖設定，若要下線 Merge File 需有 tsmc13gfsg_fram.gds 檔



56. 拿產生的 Rgb888ToYuv422_pr.v 做 Post-layout simulation