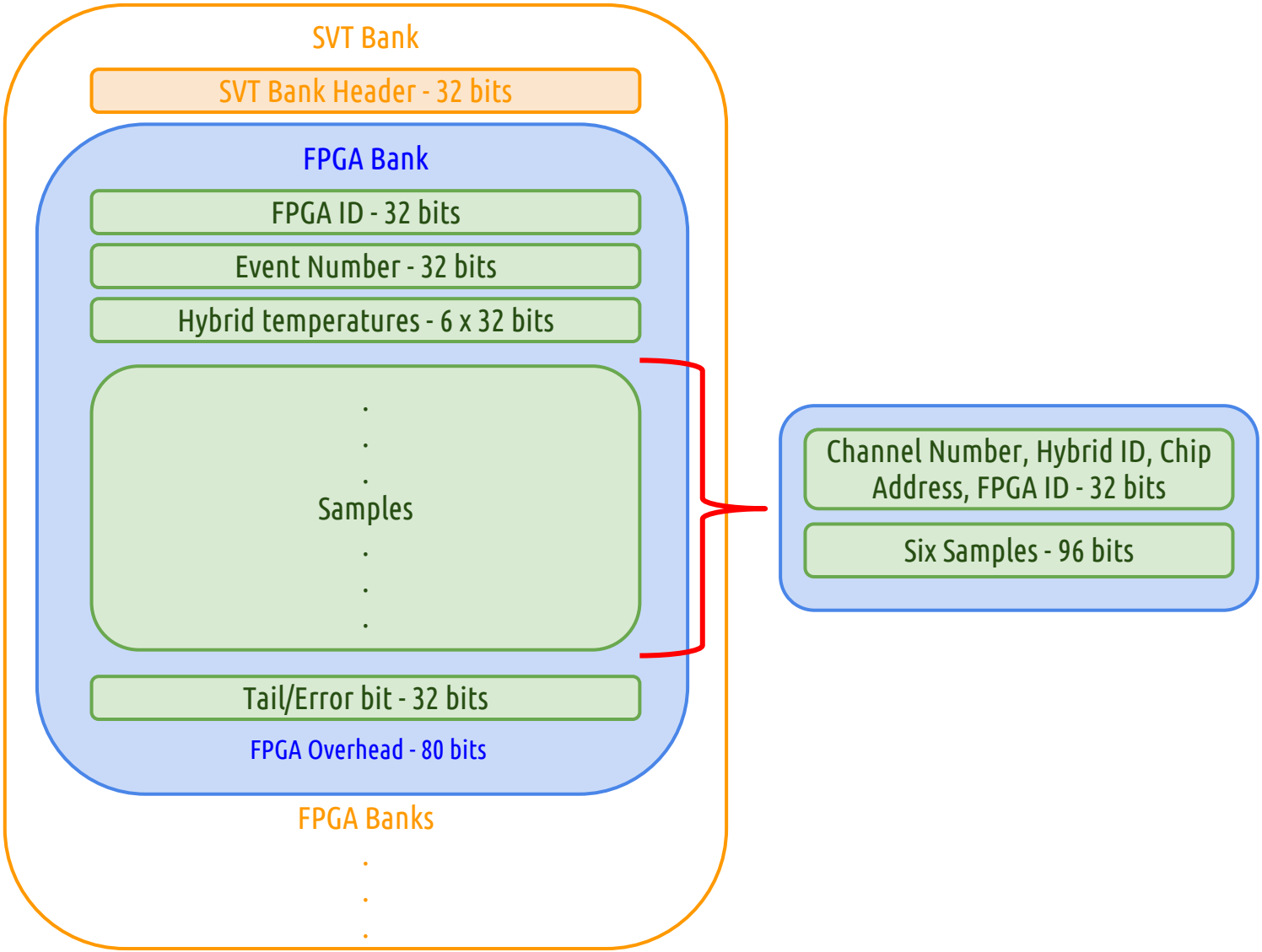
SVT Bank
SVT Bank Header - 32 bits
FPGA Bank
FPGA ID - 32 bits
Event Number - 32 bits
Hybrid temperatures - 6 x 32 bits
Samples
Tail/Error bit - 32 bits
FPGA Overhead - 80 bits
FPGA Banks
Channel Number, Hybrid ID, Chip Address, FPGA ID - 32 bits
Six Samples - 96 bits